PRELIMINARY
DATA SHEET

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AIC-4421A

Drive Manager Chip

adaptec®

AIC-4421A Features

General Features

- 3.0 V to 5.5 V Operation
- Small Package Size (128 pin TQFP and MQFP available)
- Optimized Architecture for Disk Drive Motion Control
- High performance allows for the elimination of a host processor

DSP Core

- 40 ns Cycle Time at 5 Volts
- 16-bit Fixed Point DSP
- 16x16-bit 2's Complement Parallel Multiplier with 32-bit Product
- Single Cycle Multiply and Accumulate
- 36-bit ALU with Two 36-bit Accumulators

Host interface

- Interrupt driven, Bidirectional three wire, Synchronous serial interface
- Configurable as Master

Data Acquisition

- 10-bit, 2's Complement, 2-Step Flash A/D converter
- 8 Channels of Analog Data Input, 6 channels external
- 1.1us Total Mux. and Conversion Time per Channel (Pipeline Mode)
- Dedicated Data Acquisition Sequencer
- Pipelined and Single Channel Conversion Modes
- ALU Register Mapped Data Storage
- Supports Auto-Zeroing Input Processing
- Flexible Input Voltage Ranges Independent of the DAC Output Voltage Ranges

VCM Control

- 12-bit 2's Complement Voltage Output DAC

Servo Decoder/Sequencer

- Programmable Servo Burst Sequencer
- Programmable Servo Timing Mark Sequencer
- Flexible Gating and Control Generation
- User Programmable Control Output Pins
- Allows Servo Format Flexibility
- Programmable Read Channel Interface
- Split Data Sector Support
- Separate clock input available

Spindle Control

- 8-bit Voltage Output DAC
- Digital Speed Control (FLL support)

Power Management

- Power Control Register
- Selectable on a Functional Block Basis

Diagnostic Features

- Real Time Data Output Port for Development and Diagnostics
- RS-232 Port for Diagnostic Terminal

Flexible Drive Management Functions

- General Purpose I/O pins
- Two PWM outputs (GPIOs)
- Drive Fault Signal Generation
- Programmable Arm Electronics Safety Input

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SECTION 1
Overview

1.1 Introduction

This IC utilizes mixed signal CMOS large scale integration to provide the full motion control function for the Tracking and Spin systems of a disk drive. The IC architecture is designed around a high performance, low power DSP core with peripherals optimized to the DSP and the Disk Drive control functions. This combination of processing power and efficient peripherals provides a platform to process more advanced digital control algorithms resulting in higher performance products.

The IC uses a single power supply with performance specified for 5 Volt and 3.3 Volt levels. Many levels of power reduction can be programmed into the unit to match the application. CMOS technology, low-voltage design techniques, and high levels of integration provide a high function density needed to design small form factor drives.

This IC is highly flexible with the choice of format, read channel and host processors. The IC can operate in a "Master" mode in which no other host processor is required. In that mode the Data Path Control and all other drive control functions can be managed by this IC.

Diagnostic functions have been built into the IC to simplify the drive development process. Software and hardware tools are available to support the integration of this IC into the drive system.

1.1.1 Conventions

When describing bit locations in registers or words, the LSb is bit 0 and MSb is bit N, where N is the leftmost or most significant bit. Positive logic prevails in bit state descriptions. Setting a bit, bit N=1, and a bit is a high level are all equivalent statements. Unless noted, performance specifications are valid for a supply voltage of 5.0 V +/- 10%.

1.2 Features

1.2.1 General Features

- 3.0 V to 5.5 V Operation
- Small Package Size (128 pin TQFP and MQFP available)
- Optimized Architecture for Disk Drive Motion Control
- High performance allows for the elimination of a host processor

1.2.2 DSP Core

- 40 ns Cycle Time at 5 Volts
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1.2.3 Host interface

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- Configurable as a Master

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- 10-bit, 2's Complement, 2-Step Flash A/D converter
- 8 Channels of Analog Data Input, 6 channels external
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- Programmable Servo Burst Sequencer
- Programmable Servo Timing Mark Sequencer
- Flexible Gating and Control Generation
- User Programmable Control Output Pins
- Allows Servo Format Flexibility
- Programmable Read Channel Interface
- Split Data Sector Support
- Separate clock input available

1.2.6 VCM Control

- 12-bit 2's Complement Voltage Output DAC

1.2.7 Spindle Control

- 8-bit Voltage Output DAC
- Digital Speed Control (FLL support)

1.2.8 Power Management

- Power Control Register
- Selectable on a Functional Block Basis

1.2.9 Diagnostic Features

- Real Time Data Output Port for Development and Diagnostics
- RS-232 Port for Diagnostic Terminal

1.2.10 Flexible Drive Management Functions

- General-purpose I/O pins
- Two PWM outputs. (GPIOs)
- Drive Fault Signal Generation
- Programmable Arm Electronics Safety Input

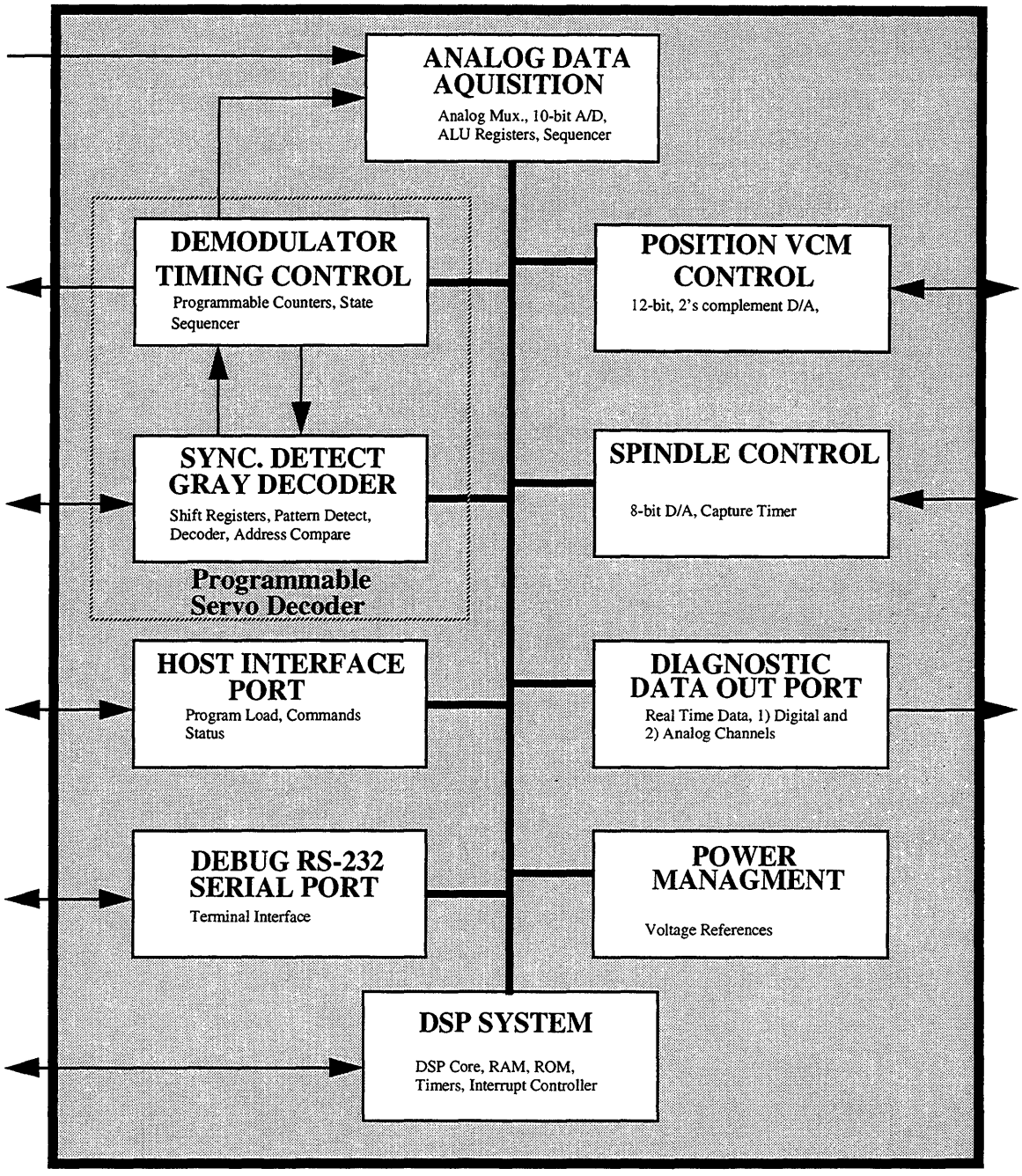

Figure 1-1 Overall Block Diagram

Figure 1-2 shows the block diagram of a typical application.

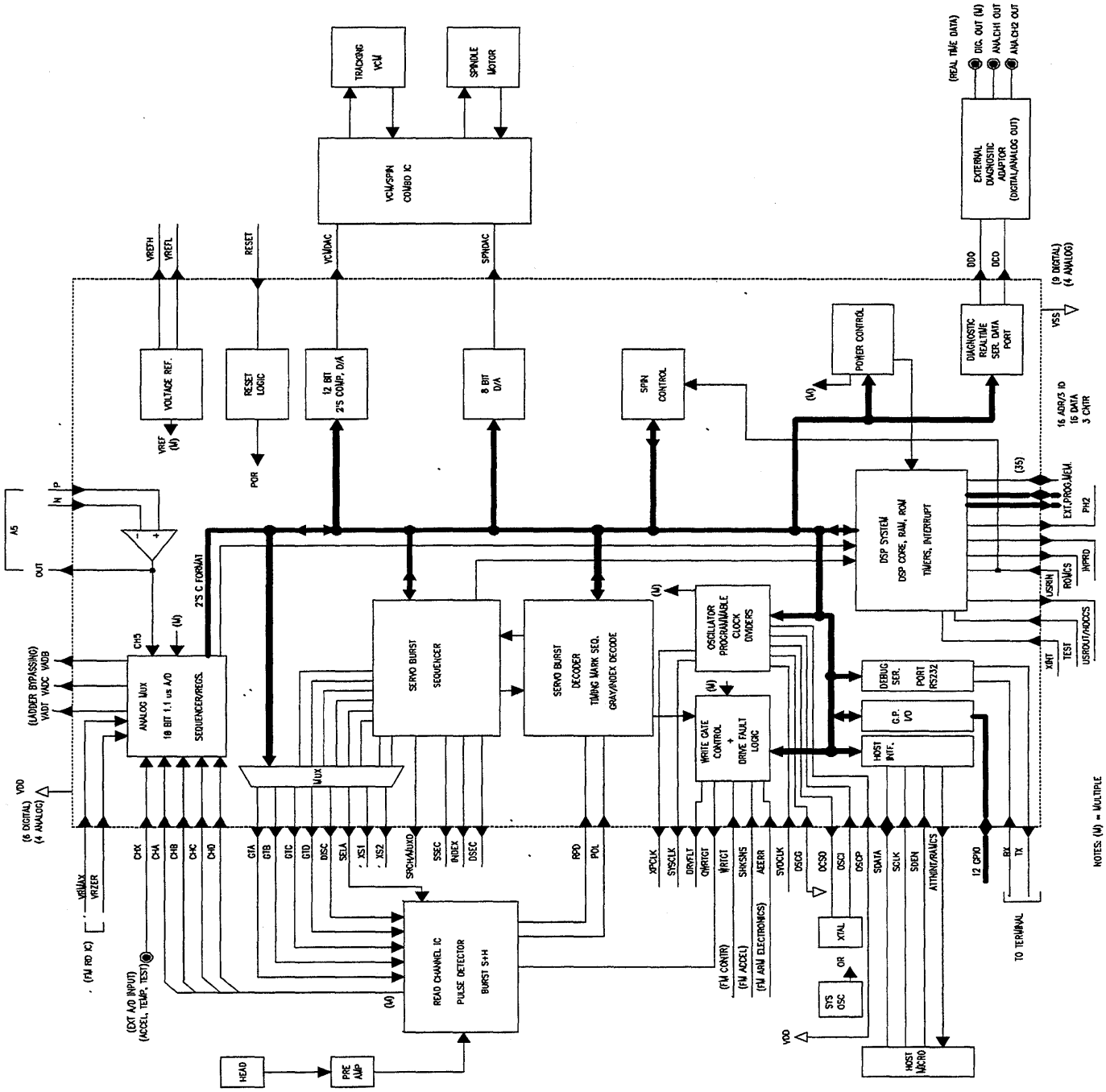

Figure 1-2 Typical Application Block Diagram

2.1 Pin Descriptions

2.1.1 Power and System

Table 2-1 Power and System Pin Descriptions

Pin # TQFP	Type	Name	Description
10, 65, 80, 93, 94, 100, 118	PWR	VDD_D	Digital Positive Power Supply.
11, 23 64, 79, 86, 87, 96, 99, 112, 127	PWR	VSS_D	Digital Power Supply Return. Pin 112 is the substrate connection.
48	PWR	VDD_A	Analog Positive Power Supply for Amplifiers and D/A converters.
51	PWR	VSS_A	Analog Power Return for Amplifiers and D/A converters.
44	PWR	VDD_M	Analog Positive Power Supply for Voltage reference.
43	PWR	VSS_M	Analog Power Supply Return for Voltage reference.
27, 39	PWR	VDD_Q	Analog Positive Power Supply for A/D converter and Multiplexer.
26, 38	PWR	VSS_Q	Analog Power Supply Return for A/D converter and Multiplexer.
95	IN	XIN	XTAL Connection 1 to internal system oscillator. Input for clock from external system oscillator. (SYSCLK).
97	OUT	XOUT	XTAL Connection 2 to internal system oscillator. Leave disconnected when supplying an external clock to the XIN pin.
98	OUT	SYSCLK	System Clock. This output is a buffered clock signal from the XTAL Oscillator or the external clock to the XIN pin.
70	IN	SVOCLK	Servo Clock Input. This clock input may be used by the Servo Decoder/Sequencer instead of SYSCLK.

Table 2-1 Power and System Pin Descriptions (Continued)

Pin # TQFP	Type	Name	Description
92	OUT	XPCLK	External Programmable Clock out.
77	IN low	*RESET	External Reset Input. Schmitt Trigger Input.
46	OUT analog	VREFL	Buffered voltage reference output. Typically used as center of A/D and D/A ranges.
45	OUT analog	VREFH	Buffered voltage reference output. Typically used as maximum positive A/D and D/A ranges.

2.1.2 Analog Data Acquisition

Table 2-2 Analog Data Acquisition Pin Descriptions

Pin # TQFP	Type	Name	Description
42	IN analog	VRZER internal	Voltage Zero Reference. Sets the center of voltage swing for the A/D system when in external reference mode.
41	IN analog	VRMAX external	Voltage Max Reference. Sets the peak voltage swing of the A/D system when in external reference mode.
36 39	OUT analog	VADT 3.145	Bypassing pin for the A/D converter's top of the reference ladder. VADT voltage equals VREFH or VRMAX depending on the bits in the (ADCCMD) register.
37 40	OUT analog	VADC 2.271	Bypassing pin for the A/D converter's center of the reference ladder. VADC voltage equals VREFL or VRZER depending on the bits in the (ADCCMD) register.
40 +3	OUT analog	VADB 1.403	Bypassing pin for the A/D converter's bottom of the reference ladder. VADB voltage = (2*VADC)-VADT.
28	IN analog	CHA	Channel A. Analog input channel to mux.
29	IN analog	CHB	Channel B. Analog input channel to mux.
30	IN analog	CHC	Channel C. Analog input channel to mux.
31	IN analog	CHD	Channel D. Analog input channel to mux.
32	IN analog	CHX	Channel X. Analog input channel to mux.
35	OUT analog	A5OUT	Mux Channel 5 amplifier output and input to mux.
34	IN analog	A5N	Inverting input of Channel 5 amplifier.
33	IN analog	A5P	Non-inverting input of Channel 5 amplifier.

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2.1.3 DSP System

Table 2-3 DSP System Pin Descriptions

Pin # TQFP	Type	Name	Description
85	IN high	USRIN	User defined input directly readable by the DSP or may be used by the spin control circuitry.
117	OUT high/ prog	USROUT /HDCCS	Output defined by the memory configuration register. (MEMCFG) USROUT: User defined output directly controllable by the DSP. HDCCS: The HDC Chip select output.

2.1.4 Servo Decoder

Table 2-4 Servo Decoder/Sequencer Pin Descriptions

Pin # TQFP	Type	Name	Description
63	IN prog	RDP	Read Pulse from the read channel IC pulse detector.
62	IN prog	POL	Pulse Polarity signal from the read channel IC pulse detector.
61	OUT prog	GTA	Gate signal to read channel IC.
60	OUT prog	GTB	Gate signal to read channel IC.
59	OUT prog	GTC	Gate signal to read channel IC.
58	OUT prog	GTD	Gate signal to read channel IC.
57	OUT prog	DISC	Discharge signal to read channel IC.
56	OUT prog	SELA	Control signal to read channel IC. Typically used for AGC control.
76	OUT prog	XS1	Extra gate signal from Servo Burst Sequencer. Could be used as a Beginning of Sector (BOS) Signal.
75	OUT prog	XS2	Extra gate signal from Servo Burst Sequencer. Could be used as a End of Sector (EOS) Signal.
72	OUT high	INDEX	Index Pulse.
73	OUT high	DSEC	Data Sector Pulse.
71	OUT high	SSEC	Servo Sector Pulse (Hard Sector).
74	OUT high	SRCH/ MUXO	Search Window signal. This pin may also be programmed to output one of several Servo Decoder/Sequencer internal signals. (see Decoder Control Register (DECCTL).
68	IN prog	WRTGT	Write Gate input from data path controller.
67	OUT prog	QWRTGT	Qualified Write Gate to write circuits.

Table 2-4 Servo Decoder/Sequencer Pin Descriptions (Continued)

Pin # TQFP	Type	Name	Description
55	IN prog	AEERR	Arm Electronics Error input. This input is exclusive or inclusive ORed (programmable) with QWRTGT to detect an AE error. The active level is also programmable. This is used by the Write Gate Qualification circuitry.
47	IN prog/ analog	SHKSNS	Shock sensor input pin to write gate qualification circuitry. Can be configured as an analog or digital input.
78	BIDIR high	DRVFLT	Drive Fault. This pin can be configured as a Drive Fault output or an input to directly control the SELA pin. (see DECCFG register) This pin has a light pullup current source to insure a high level when not being driven.

2.1.5 Host Interface

Table 2-5 Host Interface Pin Descriptions

Pin # TQFP	Type	Name	Description
88	BIDIR high	SDATA	Serial Data. This bit incorporates an internal high resistance pull-up resistor connected to the VDD_D voltage source.
89	BIDIR high/prog	SCLK	Serial Clock In/Out. Output when in Master Mode.
81	BIDIR low/prog	SDEN	Serial Data Enable. Output when in Master Mode.
25	OUT high/ low	ATTNINT/ *RAMCS	Selectable output determined by the configuration register. (CHPCFG) ATTNINT: Host Interrupt from this IC. RAMCS: Output for the programmable external RAM Chip Select.
116	IN low	*XINT	External interrupt input to the DSP.

2.1.6 VCM Control

Table 2-6 VCM Control Pin Descriptions

Pin # TQFP	Type	Name	Description
49	OUT analog	VCMDAC	12-bit D/A Converter output for VCM system.

2.1.7 Spindle Control

Table 2-7 Spindle Control Pin Descriptions

Pin # TQFP	Type	Name	Description
50	OUT analog	SPNDAC	8-bit D/A Converter output for spindle system.

2.1.8 External Memory Interface

Table 2-8 External Memory Interface Pin Description

Pin # TQFP	Type	Name	Description
111:104	OUT high	CA[15:8]	Common Memory Address.
119:126	OUT high	CA[7:0]/ JMP[5:0], ID[1:0]	Common Memory Address/Option Jumpers and Host Interface ID: These are dual function pins. On the rising edge of RESET, they are sampled to determine configuration option bits and the host interface ID bits and are read through the CHPCFG register. These bits incorporate internal high resistance pull-up resistors connected to the VDD_D voltage source. (See CHPCFG register for details.)
19:12	BIDIR high	CD[15:8]/ BSEL	Common Memory Data. These pins incorporate internal high resistance pull-up resistors connected to the VDD_D voltage source. CD[15]/BSEL serves as the byte select address output, BSEL, when the IC is configured in 8 bit external bus mode.
1:8	BIDIR high	CD[7:0]	Common Memory Data. These pins incorporate internal high resistance pull-up resistors connected to the VDD_D voltage source.
20	OUT low	*CRD	Common Memory Read.
21	OUT low	*CWR	Common Memory Write.
128	OUT low	*ROMCS	Programmable ROM Chip Select for external program Memory.

2.1.9 Other Pins

Table 2-9 Other Pin Descriptions

Pin # TQFP	Type	Name	Description
101	TS OUT high	DDO	Diagnostic Data Out. Serial data output pin of the Diagnostic Data Out Port. On reset, this output is tri-stated. The output can be enabled by setting the DIAGEN bit in the CHPCFG register. This pin also serves as the BMODE external jumper pin.
102	TS OUT high	DCO	Diagnostic Clock Out. Serial clock for the Diagnostic Out Port. On reset, this output is tri-stated. The output can be enabled by setting the DIAGEN bit in the CHPCFG register. This pin also serves as the External User Code Jumper.
90	IN high	RX	Receive. RS-232 port receive pin.

Table 2-9 Other Pin Descriptions (Continued)

Pin # TQFP	Type	Name	Description
91	TS OUT high	TX	Transmit. RS-232 port transmit pin. On reset, this output is tri-stated. The output can be enabled by setting the DIAGEN bit in the CHPCFG register.
103	IN low	*TEST	I.C. factory test pin and HDCCS/APPCS polarity sense mode enable. Tie to RESET to sense polarity on chip selects. Tie to VDD_D for default chip select polarity. Has internal pullup.
115	BIDIR prog	GPIO11/ APPCS	General Purpose I/O. Each pin can be configured as an input or an output. When Application space chip select is enabled in the MEMCTL register GPIO[11]/APPCS functions as the APPCS output pin. APPCS is asserted active low.
114	BIDIR prog	GPIO10/ PWM0	General Purpose I/O. Each pin can be configured as an input or an output. When GPIO10 is disabled in the GPIO configuration register (GPIOCF), a dedicated PWM is enabled on this pin.
113	BIDIR prog	GPIO9/ PWM1	General Purpose I/O. Each pin can be configured as an input or an output. When GPIO9 is disabled in the GPIO configuration register (GPIOCF), a PWM using the SETPON logic is enabled on this pin.
84:82, 69, 66, 54:52, 24	BIDIR prog	GPIO[8:0]	General Purpose I/O. Each pin can be configured as an input or an output.
9	OUT high	PH2	Phi-2 Clock Phase. Use falling edge to clock logic analyzer when tracing external bus. This pin is active only if Internal Trace Mode is enabled.
22	OUT low	*INPRD	Internal Program Memory Read. Logic analyzer control signal used to qualify external bus activity when Internal Trace Mode is enabled.

Figure 2-1 shows the pinouts for the IC Pinout TQFP Package.

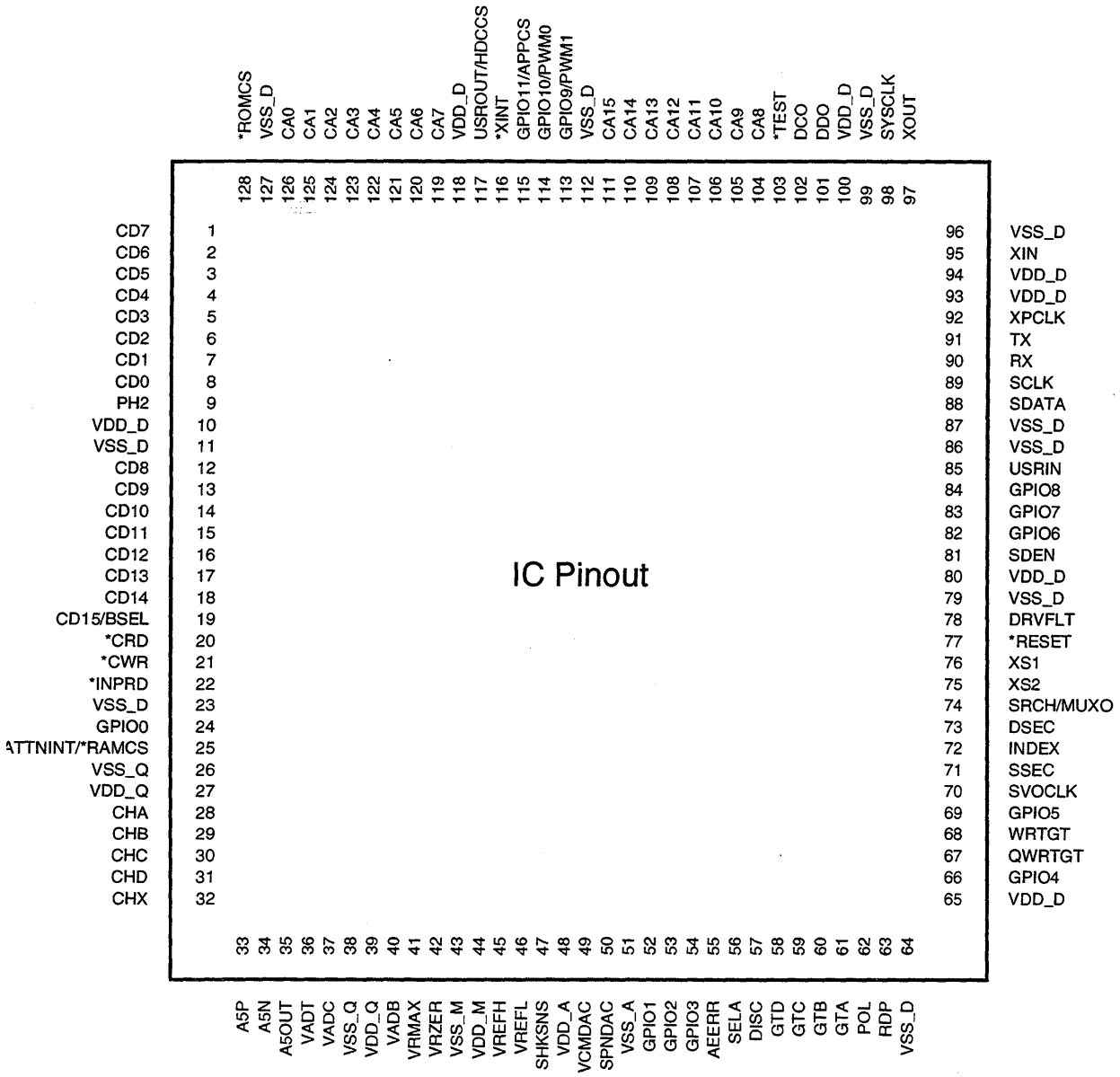

Figure 2-1 IC Pinout TQFP Package (Top View)
(For Reference Only)

Figure 2-2 shows the pinouts for the IC Pinout MQFP Package.

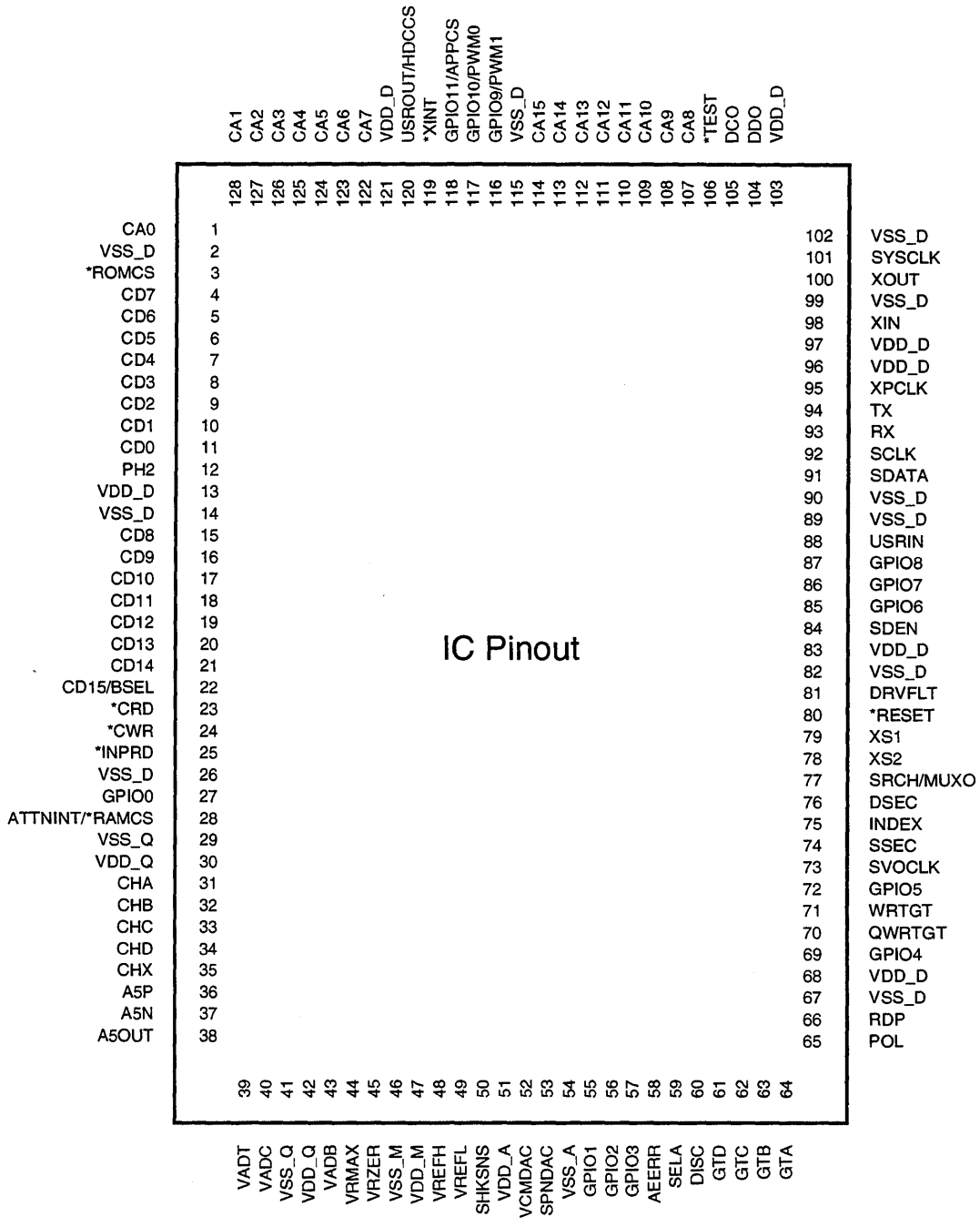

Figure 2-2 IC Pinout MQFP Package (Top View)
(For Reference Only)

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3.1 DSP Core

The chip is designed around a 16-bit general-purpose Digital Signal Processor (DSP) core. The DSP (see Figure 3-1) consists of three main execution units executing in parallel: the Computation unit (CU), the Data Address Arithmetic Unit (DAAU), and the Program Control Unit (PCU). The CU has a 16 x 16 multiplier, 36-bit ALU, and 2 36-bit accumulators. The DSP has a 16 level hardware stack and can be accessed as a Last-In-First-Out (LIFO) data register file. The stack is automatically loaded with the PC whenever a subroutine call or an interrupt occurs, and is popped back on return from subroutine or interrupt respectively.

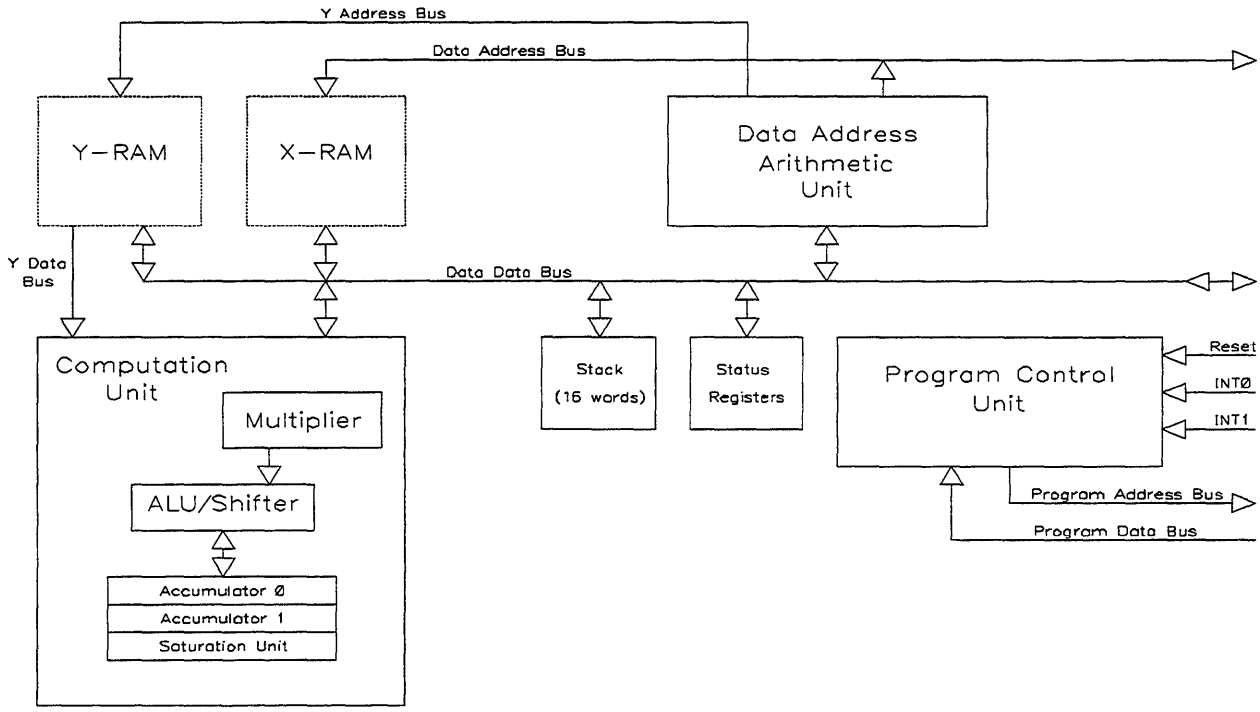


Figure 3-1 DSP Core Block Diagram

3.2 Memories

The DSP core has seven memory regions (see Figure 3-2 for a memory system block diagram) mapped into its program and data address spaces:

- Program ROM
- Program/Data RAM
- X-RAM
- Y-RAM
- Memory Mapped I/O
- External Program/Data Memory
- Shadow Interrupt Vector Memory

The DSP accesses all of its memories and peripherals through three separate buses. The read-only Program Bus gives the DSP access to the 64K program address space and is used to fetch DSP instructions. The bi-directional Data Bus is used by the DSP to fetch instruction operands and to write values to memory in the 64K data address space. The Common Bus is a bi-directional bus used to access memory mapped into both the program and data address spaces. It time multiplexes accesses from both the Program and Data buses. Table 3-1 and Table 3-2 show how these memories are mapped into the program and data address spaces.

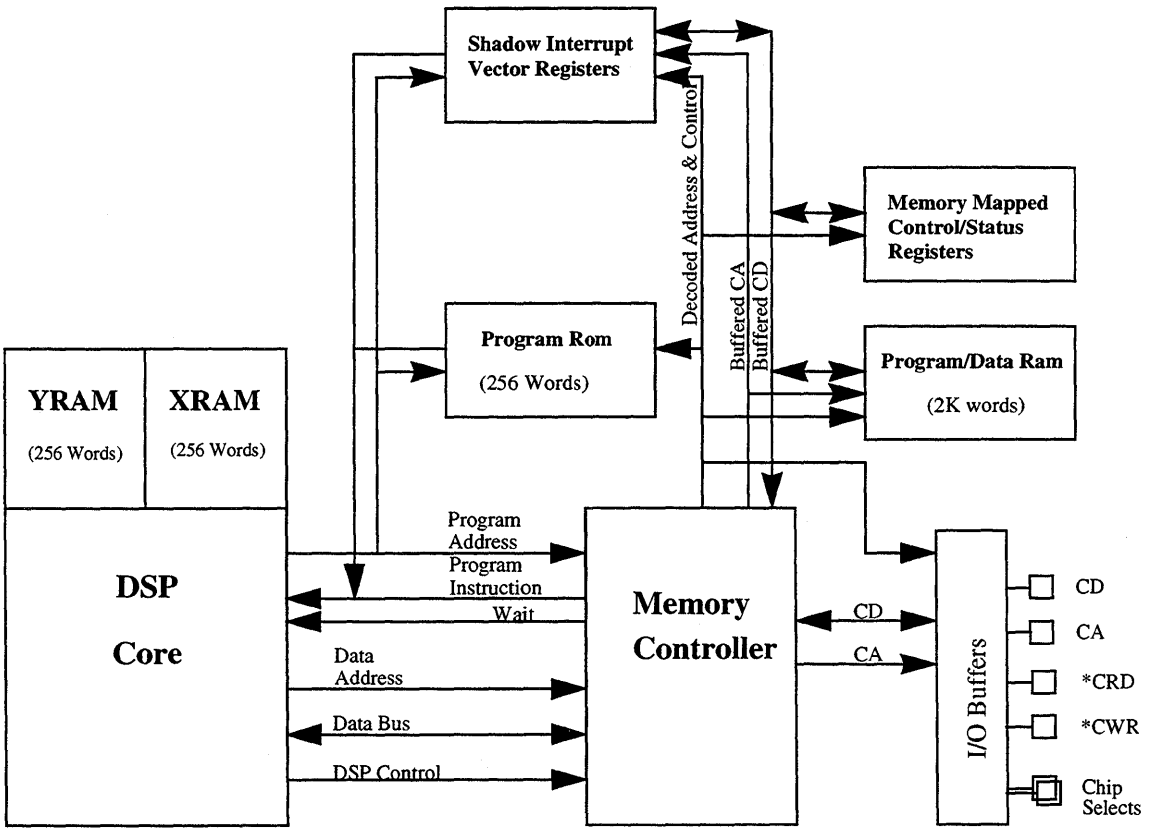


Figure 3-2 DSP-Memory Block Diagram

Table 3-1 Data Memory Map

Memory Name	Start Address	End Address	Comment
X-RAM	0000H	00FFH	256 Word On-core X-RAM.
Reserved	0100H	03FFH	On-core X-RAM Expansion.
Reserved	0400H	0FFFH	
Program/Data RAM (Internal)	1000H	17FFH	2K Internal Data/Program RAM. Same physical memory as in Program Address Map.
Reserved	1800H	1FFFH	
Prog./Data Memory Bank 0 (External)	2000H	3FFFH	8K External RAM – if enabled, a RAMCS is generated, otherwise a ROMCS is generated on a data space access.
Prog/Data RAM Bank 1 (External)	4000H	5FFFH	8K External RAM – if enabled, and more than 1 bank of RAM is enabled, a RAMCS is generated on a data space access, otherwise a ROMCS is generated.
Prog/Data RAM Bank 2 (External)	6000H	7FFFH	8K External RAM – if enabled, and 3 or 4 banks of RAM are enabled, a RAMCS is generated on a data space access, otherwise a ROMCS is generated.
Prog/Data RAM Bank 3 (External)	8000H	9FFFH	8K External RAM – if enabled, and 4 banks of RAM are enabled, a RAMCS is generated on a data space access, otherwise a ROMCS is generated.
PROM program window (external)	A000H	BFFFH	In PROM program mode, reads and writes to this data area generate ROMCS.
Application Space	C000H	CFFFH	Generates APP chip select output. User application address space. HDC wait states are generated.
HDC Chip Select	D000H	DFFFH	Generates the HDC chip select output.
Mem. Mapped I/O	E000H	E0FFH	Memory Mapped I/O.
Burst Seq. RAM	E100H	E17FH	Burst Sequencer Instruction RAM.
Reserved	E180H	E1FFH	
Timing Mark Seq. RAM	E200H	E21FH	Timer Mark Sequencer Instruction RAM.
Reserved	E220H	EEFFH	
Shadow Reset Vec.	EF00H	EF01H	All Shadow Vectors are enabled through the Chip Configuration Register. They are accessible from the data bus only if they are disabled in the Configuration Register.
Reserved	EF02H	EF07H	
Shadow BPI Vec.	EF08H	EF09H	
Shadow Trap Vec.	EF0AH	EF0BH	
Shadow INT0 Vec.	EF0CH	EF0DH	
Shadow INT1 Vec.	EF0EH	EF0FH	
Reserved	EF10H	EFFFH	
Reserved	F000H	FBFFH	Reserved for NICEOS.
Reserved	FC00H	FEFFH	On-core Y-RAM Expansion.
Y-RAM	FF00H	FFFFH	256 Word On-core Y-RAM.

Table 3-2 Program Memory Map

Memory Name	Start Address	End Address	Comments
Reset Vector	0000H	0001H	Reset Interrupt Vector.
Reserved	0002H	0007H	
BPI Vector	0008H	0009H	Break Point Interrupt Vector.
Trap Vector	000AH	000BH	Trap Interrupt Vector.
INT0 Vector	000CH	000DH	Interrupt 0 Vector.
INT1 Vector	000EH	000FH	Interrupt 1 Vector.
Program ROM (Internal)	0010H	00FFH	256 Word Internal Program ROM.
Reserved	0100H	0FFFH	
Program/Data RAM (Internal)	1000H	17FFH	2K Internal Program/Data RAM. This is the same physical memory as in the Data Address Map.
Reserved	1800H	1FFFH	
Program/Data Memory (External)	2000H	3FFFH	8K External RAM – if enabled, a RAMCS is generated, otherwise a ROMCS is generated on a program space access.
Program/Data Memory (External)	4000H	5FFFH	8K External RAM – if enabled and 2 or more RAM banks are selected, a RAMCS is generated, otherwise ROMCS is generated on a program space access.
Program/Data Memory (External)	6000H	7FFFH	8K External RAM – if enabled and 3 or 4 RAM banks are selected, a RAMCS is generated, otherwise ROMCS is generated on a program space access.
Program/Data Memory (External)	8000H	9FFFH	8K External RAM – if enabled and 4 RAM banks are selected, a RAMCS is generated, otherwise ROMCS is generated on a program space access.
Program ROM (External)	A000H	DFFFH	16 K Program space access generates a ROMCS
Program ROM (External)	E000H	EFFFH	4K Program space access generates a ROMCS. EFF0H – User Baud Rate Address EFF1H – User Code Address
Program ROM (External)	F000H	FFFFH	4K Program space access generates a ROMCS. Reserved for NICEOS if using NICE.

The chip contains 256 words of internal Program ROM, the code for which will be supplied by Adaptec. This code will include common routines such as that needed to load the Program RAM with customer code. Because the lower 16 words of this ROM contain the DSP interrupt vectors, a set of "shadow vectors", which can be mapped over the ROM vector locations, has been imple-

mented. This allows the user to configure all interrupt vectors. The user programmable vectors are enabled by writing a 1 to the RAM VECTORs bit in the Chip Configuration Register (see Table 3-6). When enabled, data bus accesses to the shadow vectors are disabled.

2Kwords of internal Program/Data RAM are available which can be used for both application code and user data. The X-RAM and Y-RAM, which are accessible through the data address space, are both 256 words deep. The memory-mapped I/O, also accessible in the data address space, is located on a 256 word page to allow easy access with Direct Addressing Mode.

The Shadow Vector Register set is an internal set of 5 registers allowing the user to replace the normal DSP vectors, which are in ROM with user setable interrupt vectors.

Through an external memory interface, up to four different memory regions can be configured. These four regions are the Program ROM region, the Program/Data RAM region, Application space region, and the HDC region. Each region has its own chip select and can be configured for between zero and three wait states. The RAM CS, APP CS and HDC CS pins are multiplexed with other functions. The use of these pins is configured through the Memory Configuration Register.

The Program ROM region and the Program/Data RAM region combine to form up to 56K words of external program space. Based on the external RAM configuration, various amounts of RAM and ROM are supported as shown in Table 3-3.

Table 3-3 External Program Space RAM/ROM Configurations

Ext. RAM Enable	Ext RAM Bank Select	Maximum RAM	Maximum ROM
0	xx	0K word	56Kword
1	00	8K words	48K words
1	01	16K words	40K words
1	10	24K words	32K words
1	11	32K words	24K words

The HDC Region is used for a seamless interface to various Adaptec Hard Disk Controllers (HDC). The HDC must be configured in Non-multiplexed Intel Bus Mode. On DSP reads from the HDC memory region, the upper 8 bits of a word read as 0's to save having to mask them in code.

3.3 Memory Controller

The Memory Controller directs program and data memory accesses to all of the bus entities. The memory controller performs the following operations:

- Resolves program and data bus contention for the common memory bus
- Generates memory mapped I/O chip selects
- Generates External ROM chip select and wait states
- Generates External RAM chip select and wait states
- Generates Hard Disk Controller (HDC) chip select and wait states.
- Generates Application space (APP) chip select and wait states
- Generates control signals for external memory accesses
- Supports both 8 and 16 bit external data bus widths
- Supports PROM/Flash programing
- Provides internal trace mode
- Shadow Vector Register Control

3.3.1 Common Memory Bus Contention Resolution

Because the DSP has only one address and one data bus to the common memories (Internal Program/Data, and External Program/Data, both accessed via the Common Bus), concurrent program and data accesses across the Common Bus must be serialized. The Memory Controller always assumes and starts a program access on the Common Bus. If, for a given cycle, the Program Bus is not accessing common memory, a 1 cycle dummy transaction is inserted. Any Data Bus cycle to common memory follows the completion of the Program Bus cycle or dummy cycle. Table 3-4 shows the possible combinations of transactions type for each cycle.

Table 3-4 Common Bus Transaction Sequences

Prog. Fetch Destination	Data Fetch Destination	First Transaction Type	Second Transaction Type
Prog. Bus	Data Bus	Program Dummy Cycle	No Cycle
Prog. Bus	Common Bus	Program Dummy Cycle	Data Cycle
Common Bus	Data Bus	Program Cycle	No Cycle
Common Bus	Common Bus	Program Cycle	Data Cycle

3.3.2 Chip Select Generation

The Memory Control block generates the following chip selects:

- Program ROM chip select
- Internal Program/Data RAM chip select
- Memory Mapped I/O chip select (decoded to 256 word page only)
- External Program ROM chip select
- External Program/Data RAM chip select
- External HDC chip select
- External Application space chip select
- Shadow Vector Register chip select

The polarity of HDC_CS and APP_CS chip select signals can be set automatically on chip reset. If the TEST_ pin is asserted with RESET_ (tie the TEST_ and RESET_ inputs together), the level sensed on the chip select pins is latched internally. This value sensed during reset is the de-asserted logic level for the pin. An external pulldown is required for active high chip selects. If TEST_ is tied high (inactive), both chip selects are defaulted to active high. The selected polarity for these chip selects can be verified or changed by the Chip Select Polarity bits in the CHPCFG register.

3.3.3 Wait State Generation

The User can program the four external program/data memory regions to each have between 0 and 3 wait states (1 wait state equals one DSP instruction cycle). Wait States are programmed through the Memory Configuration Register. On Reset, the external memory wait-states default to 3. Although the HDC memory region consists only of address of D000H to DFFFH, HDC wait states are generated on all accesses from address C000H to DFFFH. This allows the user to add additional parallel peripherals in the application space memory range, C000H to CFFFH. Table 3-8 show the memory access times for all combination of Program, Data and Common Bus accesses including wait states.

NOTE: Make sure to add one cycle for data write cycles to common bus.

3.3.4 Support for Both 8- and 16-bit External Bus Widths

The Memory Control block supports both 8 and 16 bit external data bus widths. When the chip is configured for 8 bit external bus width the Memory control block generates two byte wide external bus accesses on CD[07:00] to satisfy each program/data memory access by the DSP core. The Memory Control block is responsible for proper byte to word assembly on reads and word to byte disassembly on writes. The lower byte is accessed first, followed by the upper byte. On read operations the accesses to HDC space are always single byte. Accesses to Application space are single byte in 8 bit mode and word wide in 16 bit mode. Byte addressing is provided by the CD[15]/ BSEL pin. In 8 bit mode this pin acts as an additional byte address bit. The specified number of wait states are generated for each byte access.

3.3.5 PROM/Flash Programing Support

The Memory Control block provides PROM/Flash program support by allowing the mapping of 8K word segments from ROM into the PROM Programming window data space, A000H – BFFFH. Once a segment is mapped, read and write operations can be performed to the PROM as though it were RAM in data space. Accesses to the PROM Programming window data space are always single byte or word. If the chip is configured for 8 bit external bus width, accesses to the

PROM Programing window do NOT generate multiple byte bus accesses nor assemble/disassemble bytes to/from words. This allows maximum flexibility for application code control of the programming process.

Selection of upper or lower byte access is also under software control. A PROM program byte select bit is provided in the MEMCFG register to control the state of the CD[15]/BSEL pin while the chip is in 8 bit bus width – PROM Programming mode. This bit also controls which byte from the internal data bus, upper or lower, is driven out on PROM Programming window data write operations.

To fully program a device, the code goes through each 8K segment twice, once for the low bytes with PROM program byte select = 0, and once for the high bytes with PROM program byte select = 1. Since low and high bytes are multiplexed under control of the byte select bit, there is no need to perform any byte alignment shift operations while programing 8 bit devices. Byte wide write verify operations are simplified by having single byte reads from program window space result in duplicate byte data in both high and low destination register byte positions.

3.3.6 Memory Control Signal Generation

The Memory Control block generates the read and write pulses to the external memory. The timing requirements of these signals are given in the Electrical Specifications chapter of the specification.

3.3.7 Internal Trace Mode

When internal trace mode is enabled two internal memory control signals, DSP clock PH2, Program read are driven to external pins. Internal trace mode also forces the CA[15:00] and CD[15:0] to be driven with address and data on all internal DSP program accesses. By edge triggering a logic analyzer on the negative edge of the PH2 pin while in internal trace mode and using the Program Read signal as a qualifier, all internal program memory references can be traced.

3.3.8 Shadow Vector Register Control

The control of the Shadow Vector Registers is also generated in the Memory Control block. The vector registers are both readable and writable through the data bus (reserved locations read as 0's) when disabled, and not accessible from the data bus when enabled. If the shadow vector registers are disabled in the Memory Configuration register, a program access to the lower 16 words of Program ROM generates a Program ROM chip select and the data is sourced from the Program ROM. If the shadow vector registers are enabled in the Memory Configuration register, a program access to the lower 16 words of Program ROM generates a shadow vector chip select and the data is sourced from the Shadow Vector registers.

Table 3-5 Chip Configuration Register (CHPCFG)

Bit(s)	rw	Reset	Description/Function
15	r	jumper configured	External User Code Jumper – Sampled on reset. See the ROM Code User Guide for details on use. The state of this jumper is determined by the value on pin DCO on the rising edge of reset.
14:10	r	jumper configured	Spare User Jumpers – The state of these jumpers is determined by the value on CA[7:3] on the rising edge of reset.
09	rw	0	Negative USRIN input. Defines the active state of the USRIN input as being a low level if this bit is set.
08	rw	0	Internal debug mode enable. Writing a one to this bit enables tracing of internal memory accesses from external chip pins. Writing a zero disables the PH2 and INTPRD output pins, and disables the tracing of internal read and write operations.
07	rw	jumper configured	BMODE – This bit configures the memory controller to access either 8 or 16 bit wide external memory. This bit is sampled on the rising edge of reset (pin DDO). By default the chip comes up in 8 bit bus mode due to internal pull-up on pin DDO. Setting this bit to 0 configures the memory controller for 16 bit operation.
06:05	rw	jumper configured	Spare User Jumpers – These bits are sampled on the rising edge of reset (bits CA[1:0]). These bits are writeable for User status or data storage.
04	rw	0	Shadow Vectors Enable – Writing a one to this bit enables the Shadow Vector Register Set for interrupts and disables writing to the Shadow Vector Register Set.
03	rw	0	DIAGEN – Writing a one to this bit enables the outputs for the DDO, DCO and TX pins. When reset, these outputs are tri-stated.
02	r	0	Reserved
01	rw	x	APP chip select polarity. Writing a one to this bit causes the chip to generate an active high HDC chip select. If the TEST_ pin is active, the inactive level of this chip select is determined by the level of the GPIO[11]/APPCS pin on the rising edge of *RESET.
00	rw	x	HDC chip select polarity. Writing a one to this bit causes the chip to generate a active high HDC chip select. If the TEST_ pin is active, the inactive level of this chip select is determined by the level of the USROUT/HDCCS pin on the rising edge of *RESET.

Table 3-6 Chip Revision Register (CHPREV)

Bit(s)	rw	Reset	Description/Function
15:08	r	00h	Reserved – reads as 00h
07:00	r	03h	Chip Revision

Table 3-7 Memory Configuration Register (MEMCFG)

Bit(s)	rw	Reset	Description/Function
15:13	rw	000	PROM Program window select. When PROM program mode is enabled, this field selects which of 8 possible 8K word segments of external ROM space is mapped to the PROM programming window data space, A000H – BFFFH. In PROM programing mode, accesses to the programming window data space result in the value stored here being driven on the upper three Common Memory Address lines.
12	rw	0	PROM program byte select. This bit controls the state of the CD[15]/BSEL pin when both PROM programing mode, and 8 bit bus modes are enabled. This allows program controlled access to both upper and lower byte addresses for 8 bit PROM programming. This bit also controls which byte (upper or lower) of common bus data is presented on the lower 8 Common Memory Data lines. When this bit is written to a one the upper byte is selected. The lower byte is selected when written to a zero.
11	rw	1	APP Chip Select Enable – setting this bit enables the generation of the APP chip select, changing the function of the GPIO[11]/APPCS pin from GPIO[11] to APPCS. If TEST_ pin is active, the APP_CS is disabled.
10:09	rw	11	HDC/APP Wait States – the number of wait states generated to both the User Application and HDC memory regions.
08	rw	1	HDC Chip Select Enable – setting this bit enables the generation of the HDC chip select, changing the function of the USROUT/HDCCS pin from USROUT to HDCCS.
07:06	rw	11	External ROM Wait States – number of wait states generated during external ROM accesses.
05:04	rw	11	External RAM Wait States – number of wait states generated to memory banks selected by the External RAM Bank Select. Wait States are generated only if External RAM is enabled.
03:02	rw	11	External RAM Bank Select – number of banks of RAM to include in RAMCS generation. 00 – 1 bank, 01 – 2 banks, 10 – 3 banks, and 11 – 4 banks. On chip reset this defaults to 4 banks selected.
01	rw	1	External RAM Enable – setting this enables generation of the external RAM chip select, changing the function of the ATTNINT/RAMCS pin from ATTNINT to RAMCS.
00	rw	0	PROM program mode select. Writing a one to this bit enables the mapping of one 8K word section of external ROM to a programming window data space, A000H – BFFFH. Writing a one to this bit also forces the memory controller to do single byte reads and writes from the program window address space when the chip is in 8 bit bus mode.

Table 3-8 Memory Access Cycle Times (16-bit Mode)

Program Bus Access	Data Bus Access	Memory Cycles to Complete Access
Program ROM	None	1
Program ROM	X/Y RAM	1
Program ROM	Mem. Map. I/O	1
Program ROM	Internal RAM	2
Program ROM	External Mem.	2 + (Wait States for accessed memory region)
Program ROM	Vector RAM	1
Vector RAM	None	1
Vector RAM	X/Y RAM	1
Vector RAM	Mem. Map. I/O	1
Vector RAM	Internal RAM	2
Vector RAM	External Mem	1 + (Wait States for accessed memory region)
Internal RAM	None	1
Internal RAM	X/Y RAM	1
Internal RAM	Mem. Map. I/O	1
Internal RAM	Internal RAM	2
Internal RAM	External Mem.	2 + (Wait States for accessed memory region)
Internal RAM	Vector RAM	1
External Mem.	None	1 + (Wait States for accessed memory region)
External Mem.	X/Y RAM	1 + (Wait States for accessed memory region)
External Mem.	Mem. Map. I/O	1 + (Wait States for accessed memory region)
External Mem.	Internal RAM	2 + (Wait States for accessed memory region)
External Mem.	External Mem.	(Wait States for accessed prog. mem. region + 1) + (Wait States for accessed data mem. region + 1)
External Mem.	Vector RAM	1 + (Wait States for accessed memory region)

Note: For any Writes to the common bus, one extra cycle should be added.

Table 3-9 Memory Access Cycle Times (8-bit Mode)

Program Bus Access	Data Bus Access	Memory Cycles to Complete Access
Program ROM	None	1
Program ROM	X/Y RAM	1
Program ROM	Mem. Map. I/O	1
Program ROM	Internal RAM	2
Program ROM	External Mem.	2 + (Wait States for accessed memory region)* 2
Program ROM	Vector RAM	1
Vector RAM	None	1
Vector RAM	X/Y RAM	1
Vector RAM	Mem. Map. I/O	1
Vector RAM	Internal RAM	2
Vector RAM	External Mem	1 + (Wait States for accessed memory region)*2
Internal RAM	None	1
Internal RAM	X/Y RAM	1
Internal RAM	Mem. Map. I/O	1
Internal RAM	Internal RAM	2
Internal RAM	External Mem.	2 + (Wait States for accessed memory region)*2
Internal RAM	Vector RAM	1
External Mem.	None	1 + (Wait States for accessed memory region)*2
External Mem.	X/Y RAM	1 + (Wait States for accessed memory region)*2
External Mem.	Mem. Map. I/O	1 + (Wait States for accessed memory region)*2
External Mem.	Internal RAM	2 + (Wait States for accessed memory region)*2
External Mem.	External Mem.	((Wait States for accessed prog. mem. region + 1) + (Wait States for accessed data mem. region + 1))*2
External Mem.	Vector RAM	1 + (Wait States for accessed memory region)*2

Note: For any Writes to the common bus, one extra cycle should be added.

SECTION 4
DSP Peripherals

4.1 Clock Generator

4.1.1 Oscillator

The IC supports two basic clock oscillator configurations: Crystal (XTAL) Controlled Oscillator and an External Oscillator. When using the Crystal Controlled Oscillator, the XIN and XOUT pins are connected to an external crystal along with the additional components as shown below. When using an External Oscillator to provide a clock to the IC, the XIN pin is tied to the external clock signal and the XOUT pin is not connected (float). The base internal clock (System Clock or SYSCLK) is generated directly from the oscillator.

The XTAL oscillator is configured as a Pierce oscillator. The XTAL therefore operates in a antiresonant or parallel resonant mode with the external components. The internal oscillator amplifier is an inverting amplifier. The DC Bias path is provided by R1. The external resistors R1 and R2 in conjunction with the tuning components L1, C1, and C2 allow for the adjustment of the gain and power level of the XTAL oscillator circuit. The output of the Oscillator (XOUT) is amplified/ detected internally and becomes the source for SYSCLK.

As with any high frequency circuit all high frequency design and layout practices should be followed: Short lead lengths, low capacitance and inductance traces, and high quality RF components need to be used. The oscillator circuit and XTAL should not be in close proximity to noisy high speed circuits. In addition the layout should minimize loop areas within the circuit to prevent noise pickup by current coupling. The capacitance between the XIN pin and XOUT pin should be minimized. Meanwhile, capacitance between both of these signals and ground enhances stabiltiy for the circuit. To aid with this, a trace should be run between the traces from these pins to the XTAL and be connected to the VSS_D pin between the oscillator pins (other end floating). Increasing the separation between the two XTAL traces will help to reduce the capacitance between them.

The choice of external components depend on the vibrational mode of the XTAL selected. If a third harmonic mode XTAL is selected, use the six component values listed in Table 4-3. If a fundamental mode XTAL is selected use the four component values listed in Table 4-3. These component values are calculated assuming that an XTAL is used with the XTAL parameters in the ELECTRICAL SPECIFICATIONS. They are general guide lines and due to the interactions of the XTAL and the external components other solutions may exist.

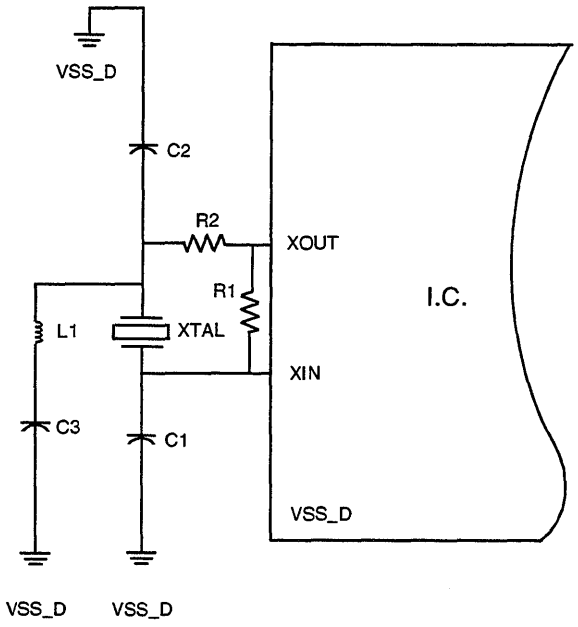


Figure 4-1 Crystal Oscillator Schematic

Table 4-1 Crystal Oscillator External Components (Third Overtone Mode)

XTAL Frequency Range (MHz)	C1	C2	L1	C3	R1	R2
30.0 to 50.0	36 pF	68 pf	0.47 uH	820 pF	100K	30.1

Table 4-2 Crystal Oscillator External Components (Fundamental Mode)

XTAL Frequency Range (MHz)	C1	C2	L1	C3	R1	R2
30.0	22 pF	22 pf	none	none	100K	30.1
36.0	30 pF	30 pf	none	none	100K	30.1
40.0	33 pF	33 pf	none	none	100K	30.1

4.1.2 DSP Clock

The DSP core is driven by an internally generated (from SYSCLK divided by two), two phase (PHI1, PHI2), non-overlapping clock. The base instruction cycle time of the DSP core is equal to the SYSCLK divided by 2.

4.1.3 Bus Clock

Bus Clock is the clock used to generate all bus cycles external to the DSP core. Bus Clock has a frequency of SYSCLK divided by 2. Bus Clock high corresponds to PHI1 of the DSP clock and Bus Clock low to PHI2.

4.1.4 Servo Clock

Servo Clock is a separate input into the IC. It can be used as the base clock for all of the Servo logic, including the Servo Burst Sequencer, the Timing Mark Sequencer and the Data Synchronization logic.

4.1.5 Peripheral Clocks

Numerous clocks are generated internally to clock the various function blocks. Table 4-3 gives a summary of all internal clocks.

Table 4-3 Internal Clock Summary

Clock Name	Clock Frequency	Description/Function
System Clock (SYSCLK)	External Input	Base System Clock
Servo Clock (SVOCLK)	External Input	External DCLK Source
BusClock	System Clock / 2	DSP peripheral bus clock
BusClock2	Bus Clock / 2	Diag Data Out shift clock
BusClock8	Bus Clock / 8	Spin Capture logic
DCLK	SYSCLK / (1 -> 15) or SVOCLK / (1 -> 15)	Servo Burst Seq., Timing Mark Seq, Sector Timing logic
CCLK	DCLK / (1 -> 15)	Index Latch and Gray Shift Reg.
ACLK1	Bus Clock / (1 ->32) * 2	Analog Acquisition and Sample Clock. (see SHCLK)
ACLK2	PW= (1/Bus Clock)*(1-8) Freq. = ACLK1 freq.	Analog Acquisition Coarse Compare Clock
ACLK3	PW= (1/Bus Clock)*(1-8) Freq. = ACLK1 freq.	Analog Acquisition Fine Compare Clock (same PW as ACLK2)
ARCLK	Bus Clock/84	Analog Refresh Clock. Used by the Voltage reference circuitry. No user access or adjustment.
XPCLK	SYSCLK / (1 -> 32)	Programmable Clock Out
PCLK	SYSCLK or $VOCLK	Used in The Data Synchronizer when in Phase Detection Mode.
SHCLK	(same frequency as ACLK1)	Used by the Analog Shock Sensor input circuit.

The programmable clocks among these are programmed through two clock configuration registers. Table 4-4 and Table 4-5 give the definitions of these registers.

Table 4-4 Clock Configuration Register 1 (CLCFG1)

Bit(s)	rw	Reset	Description/Function
15	rw	0	PCLK Source Select. 0 = SYSCLK. 1 = SVOCLK pin. This clock is the Data Synchronizer phase mode clock source.
14	rw	0	DCLK Source Select. 0 = SYSCLK. 1 = SVOCLK pin.
13	r	0	Reserved – this bit reads as 0.
12:08	rw	00000	External Clock Divisor. System Clock is divided by this value + 1 to produce the External Clock. (XPCLK)
07:04	rw	0000	CCLK Divisor. DCLK is divided by this value + 1 to produce CCLK
03:00	rw	0000	DCLK Divisor. SYSCLK/SVOCLK is divided by this value + 1 to produce DCLK.

Table 4-5 Clock Configuration Register 2 (CLCFG2)

Bit(s)	rw	Reset	Description/Function
15:12	r	0000	Reserved. These bits read as 0's.
11:08		0000	SCLK Divisor. Bus Clock is divided by this value + 1 to produce the Peripheral Interface Master Mode SCLK.
07:05	rw	000	ACLK2 and ACLK3 Pulse Width. The Pulse Width of the high state of ACLK2 and ACLK3 is (this number + 1) of Bus Clock cycles. (See performance specification section for timing requirements.)
04:00	rw	00000	ACLK1 Divisor. Bus Clock is divided by ((this value + 1) * 2) to produce ACLK1. These divisor bits also set the frequency of the free running SHCLK used by the Analog Shock Sensor input circuit. (See performance specification section for ACLK1 timing requirements.)

4.2 RS-232C Serial Port

The IC has one standard RS-232C serial communications port. It is accessed through four memory-mapped I/O registers which sit on the DSP data bus:

- Baud Rate Register
- Status Register
- Transmit Register
- Receive Register

The RS-232C serial port has a fixed setup of 8 data bits, 1 stop bit and no parity.

The baud rate is programmable through the Baud Rate Register (see Table 4-6 for the bit definitions and Table 4-7 for typical baud rate count values). The baud rate count required for any given baud rate and system clock frequency is calculated from the following formula:

Baud Rate Count = System Clk (MHz) / (32 * Baud Rate)

The Status Register (Table 4-8) contains all read status bits and the transmit in progress status bit. Writing to the low byte of the Transmit Register initiates a transmit on the RS-232C serial port.

Table 4-6 Serial Port Baud Rate Register (SPBAUD)

Bit(s)	rw	Reset	Description/Function
15:10	r	00h	These bits are reserved for future use. They are not writable. They read as 0's.
09:00	rw	041h	Baud Rate Count – This value determines the baud rate at which the RS-232C port operates. Refer to Table 4-7 for Baud Rate Count values for common baud rates. The default baud rate is 19,200 and assumes a 40MHz system clock.

When the transmit is complete a TXCMP interrupt, if not masked, will be generated. The low byte of the Receive Register is used for receive data. It is valid if the RXVLD bit is set in the status register. Reading the Receive Register clears the RXVLD bit. When a character is transferred from the receive shift register to the Receive Register, a RXCMP interrupt (if not masked) will be generated. The base clock rate of the serial port is the system clock divided by 32.

Table 4-7 Baud Rate Generator Values

Baud Rate	20MHz Clk	30MHz Clk	36MHz Clk	40MHz Clk	50MHz Clk
1200	0x209	0x30D	0x3AA	0x412	0x516
2400	0x104	0x187	0x1D5	0x209	0x28B
4800	0x082	0x0C3	0x0FE	0x104	0x145
9600	0x041	0x062	0x075	0x082	0x0A2
19,200	0x021	0x031	0x03A	0x041	0x051
38,400	0x010	0x018	0x01D	0x020	0x028

Table 4-8 Serial Port Status Register (SPSTAT)

Bit(s)	rw	Reset	Description/Function
15:04	r	000H	Reserved – These bits are reserved for future use. They are not writable and they read as 0.
03	rw	0	Loop Mode – Setting to one internally connects TX to RX allowing testing of transmit and receive functionality.
02	r	0	TXINPG – When set, this bit indicates a transmit is in progress. A new transmit should only be initiated when this bit is 0. This is a read only bit.
01	rw	0	RXOVRN – When set, this bit indicates a receive overrun has occurred. The data in the Receive Register is valid, but at least one character was lost. This bit is write one to clear.
00	r	0	RXVLD – when set, this bit indicates there is a valid character in the Receive Register. This bit is cleared by reading the Receive Register or by a RXOVRN occurring.

Table 4-9 Serial Port Transmit Register (TXCHAR)

Bit(s)	rw	Reset	Description/Function
15:08	r	00H	Reserved – These bits are reserved for future use. They are not writable and they read as 0.
07:00	rw	FFH	Transmit Data – Writing this byte initiates a transmit.

Table 4-10 Serial Port Receive Register (RXCHAR)

Bit(s)	rw	Reset	Description/Function
15:08	r	00H	Reserved – These bits are reserved for future use. They are not writable and they read as 0.
07:00	r	00H	Receive Data – when the RXVLD bit is set in the Serial Port Status Register, reading this register will return the receive data.

4.3 Diagnostic Data Out Port

The Diagnostic Data Out Port (see Figure 4-2) consists of three serially linked 16-bit data registers and one 16-bit control register, all of which are both readable and writable by the DSP. This port's intended use is to shift real-time values out of the chip to a stand-alone board containing D/A's, logic analyzer connectors, oscilloscope test points, etc. To utilize the Diagnostic Serial Port, first load the three data registers with the desired data. Writing to the control register then initiates the shifting which continues for 48 clock cycles. The shift frequency is Bus Clock / 2. On the falling edge of the clock, the registers are shifted out MSB first. Diagnostic Register Two is shifted out first, followed by Diag. Reg. One and finally Diag. Reg. Zero. The rising edge of Data Out Clock should be used externally to latch data.

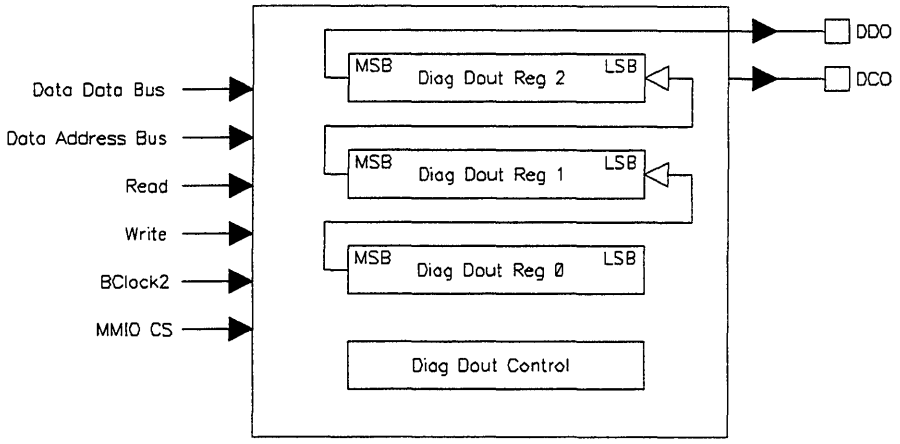


Figure 4-2 Diagnostic Data Out Port

Table 4-11 Diagnostic Data Out Control Register (DIAGDC)

Bit(s)	rw	Reset	Description/Function
15:00	w	0000h	A write to this location initiates DDO the shift clock

Table 4-12 Diagnostic Data Out Data Register 2 (DIAGD2)

Bit(s)	rw	Reset	Description/Function
15:00	rw	0000h	Diagnostic Data Out Word 2

Table 4-13 Diagnostic Data Out Data Register 1 (DIAGD1)

Bit(s)	rw	Reset	Description/Function
15:00	rw	0000h	Diagnostic Data Out Word 1

Table 4-14 Diagnostic Data Out Data Register 0 (DIAGD0)

Bit(s)	rw	Reset	Description/Function
15:00	rw	0000h	Diagnostic Data Out Word 0

4.4 Timer

The IC has 1 general purpose programmable 16-bit timer. The timer has a Control Register, Initial Count Register and Current Count Register. Tables 4-15 through 4-17 give the bit definitions and descriptions for these three registers. The timer generates an interrupt on its 0x0000 -> TM0SET transition. This interrupt is maskable in the Interrupt Mask Register. The base clock for the timer is the Bus Clock.

Table 4-15 Timer Control Register (TM0CTL)

Bit(s)	rw	Reset	Description/Function
15:09	r	000H	Reserved – These bits are reserved for future use. They are not writable and they read as 0.
08	rw	0	Periodic/Single Shot – the state of this bit determines the behavior of the counter when it reaches 0. If set, (Periodic Mode), it is reloaded from the TM0SET register and continues counting. If clear, (Single Shot Mode), it stops upon reaching zero.
07	rw	0	Run/Stop – Writing this bit to one causes the counter to be loaded from it's Initial Count Register and begin down-counting. Writing zero to this bit halts the counter. If the counter is in Single Shot mode, this bit is reset when the count reaches zero.
6:0	rw	00h	Prescale – The clock into the timer (Bus Clock), is divided by the (prescale value + 1) to generate the final clock for the counter.

Table 4-16 Timer Initial Count Register (TM0SET)

Bits	rw	Reset	Description/Function
15:0	rw	0000H	Initial Count – This 16-bit value is loaded into the counter whenever the Run/Stop bit transitions from a 0 to a 1, or if the counter is in Periodic mode, when the count reaches zero. The counter counts down from this value to 0x0000. This register is both writable and readable.

Table 4-17 Timer Current Count Register (TM0CNT)

Bits	rw	Reset	Description/Function
15:0	r	0000H	Current Count – This 16-bit value is the current value in the counter. This register is read only.

4.5 Interrupts

The DSP supports two general purpose, maskable, vectored interrupts, INT1 and INT0, with INT0 being the highest priority. Both interrupts can be masked internally to the DSP core.

INT0 is dedicated to the Servo Sector Interrupt (SSI). The SSI is the logical OR of Search Window Open (SRCH), the Data Acquisition Sequencer Inuserterrupt, the Burst Sequencer Interrupt, and the SETPON interrupt. These inputs must be enabled in the Interrupt Mask Register to contribute to the OR. INT1 is the logic OR of all other enabled interrupts. generated by the Interrupt Control Block.

The Interrupt Control Block consists of two registers: the Interrupt Mask Register, and the Interrupt Pending Register.

The Interrupt Mask Register (Table 4-18) is used to selectively enable interrupts from asserting the INT0 or INT1 input to the DSP. Setting an interrupt's mask bit to 1 in the Interrupt Mask Register enables that interrupt, and conversely, setting the mask bit to 0 disables the interrupt.

All interrupts, with the exception of the Shock Interrupt are edge triggered. The Shock Interrupt is active on a high level. An external interrupt is generated on the falling edge of the XINT pin.

Table 4-18 Interrupt Mask Register (INTMSK)

Bit(s)	rw	Reset	Function/Description
15:12	r	0000	Reserved – These bits are reserved for future use. They are not writable and they read as 0.
11	rw	0	SETPON Interrupt
10	rw	0	Burst Sequencer Interrupt
09	rw	0	Acquisition Sequencer Interrupt
08	rw	0	Search Window Open Interrupt
07	r	00	Shock Interrupt
06	r	0	Reserved – This bit reads as 0.
05	rw	0	Spindle Interrupt
04	rw	0	External Interrupt
03	rw	0	Command Pending/Master Mode Xfer Complete Interrupt
02	rw	0	Timer 0 = Zero Interrupt
01	rw	0	RS-232C Receive Complete Interrupt
00	rw	0	RS-232C Transmit Complete Interrupt

The Interrupt Pending Register (Table 4-19) can be read to determine which interrupts are currently pending. If an interrupt's pending bit is set to 1, it indicates that this device has issued an interrupt and is in need of service. Writing a 1 to the pending bit of an interrupt will cause that interrupt's pending bit to reset to 0. The bits of this register will be set if a device interrupts regardless of whether an interrupt is masked in the Interrupt Mask Register or in the DSP itself.

Table 4-19 Interrupt Pending Register (INTPND)

Bit(s)	rw	Reset	Description/Function
15:12	r	0	Reserved – These bits are reserved for future use. They are not writable and they read as 0.
11	rw	0	SETPON Interrupt
10	rw	0	Burst Sequencer Interrupt
09	rw	0	Acquisition Sequencer Interrupt
08	rw	0	Search Window Open
07	r	0	Shock Interrupt
06	r	0	Reserved – This bit reads as 0
05	rw	0	Spin Interrupt
04	rw	0	External Interrupt
03	rw	0	Command Pending/Master Mode Xfer Complete Interrupt
02	rw	0	Timer 0 = Zero Interrupt
01	rw	0	RS-232C Receive Complete Interrupt
00	rw	0	RS-232C Transmit Complete Interrupt

4.6 General Purpose Input/Output

Fourteen general purpose input / output (GPIO) bits are available to the user. These bits are configured and accessed through three registers. The GPIOCL register controls, on a bit by bit basis, whether a bit is an input or an output. All fourteen bits default to be inputs on reset. Setting a GPIOCL bit to 1 changes that GPIO to an output. The GPIODT register reads the state of GPIOs configured as inputs and sets the state of GPIOs configured as outputs. Reading the GPIODT register will return the logic level on the chip pins of all the GPIOs. Writing the GPIODT register will affect the logic level on the chip pins of only the GPIOs configured as outputs in the GPIOCL register. GPIO bits 14-12 are multiplexed on the Peripheral Interface pins SDATA, SCLK and, SDEN. To use these GPIO's, Peripheral Interface GPIO mode must be enabled in the MSTCTL register. GPIO bit 11 is multiplexed with the Memory Interface pin APPCS. To use this pin as a GPIO, the APPCS functionality must be disabled in the MEMCFG register. GPIO bits 10 and 9 and multiplexed with the two PWM generators. To configure either pin as a PWM generator, the GPIO function must be disabled in the GPIOCF register. To support 3-state logic, GPIO bits 1 and 0 can have their internal pullup resistors disabled, by setting the appropriate bits in the GPIOCF register.

Table 4-20 General Purpose I/O Control Register (GPIOCL)

Bit(s)	rw	Reset	Description/Function
15	rw	0	Reserved
14	rw	0	GPIO Bit 14 Control – 1 = output, 0 = input. This function is multiplexed with the SDEN pin. To enable this function, Peripheral Interface GPIO Mode must be enabled in the MSTCTL register.
13	rw	0	GPIO Bit 13 Control – 1 = output, 0 = input. This function is multiplexed with the SCLK pin. To enable this function, Peripheral Interface GPIO Mode must be enabled in the MSTCTL register.
12	rw	0	GPIO Bit 12 Control – 1 = output, 0 = input. This function is multiplexed with the SDATA pin. To enable this function, Peripheral Interface GPIO Mode must be enabled in the MSTCTL register.
11	rw	0	GPIO Bit 11 Control – 1 = output, 0 = input This function is multiplexed with the APPCS pin. To enable this function, APPCS mode must be disabled in the MEMCFG register.
10	rw	0	GPIO Bit 10 Control – 1 = output, 0 = input
09	rw	0	GPIO Bit 9 Control – 1 = output, 0 = input
08	rw	0	GPIO Bit 8 Control – 1 = output, 0 = input
07	rw	0	GPIO Bit 7 Control – 1 = output, 0 = input
06	rw	0	GPIO Bit 6 Control – 1 = output, 0 = input
05	rw	0	GPIO Bit 5 Control – 1 = output, 0 = input
04	rw	0	GPIO Bit 4 Control – 1 = output, 0 = input
03	rw	0	GPIO Bit 3 Control – 1 = output, 0 = input
02	rw	0	GPIO Bit 2 Control – 1 = output, 0 = input
01	rw	0	GPIO Bit 1 Control – 1 = output, 0 = input
00	rw	0	GPIO Bit 0 Control – 1 = output, 0 = input

Table 4-21 General Purpose I/O Data Register (GPIODT)

Bit(s)	rw	reset	Description/Function
15	r	0	Reserved
14	rw	0	GPIO Bit 14. This function is multiplexed with the SDEN pin. To enable this function, Peripheral Interface GPIO Mode must be enabled in the MSTCTL register.
13	rw	0	GPIO Bit 13. This function is multiplexed with the SCLK pin. To enable this function, Peripheral Interface GPIO Mode must be enabled in the MSTCTL register.
12	rw	0	GPIO Bit 12. This function is multiplexed with the SDATA pin. To enable this function, Peripheral Interface GPIO Mode must be enabled in the MSTCTL register.
11	rw	0	GPIO Bit 11. Multiplexed w/APP_CS. To use as GPIO, disable APP_CS function in MEMCFG.
10	rw	0	GPIO Bit 10. Multiplexed w/PWM.
09	rw	0	GPIO Bit 9. Multiplexed w/PWM.
08	rw	0	GPIO Bit 8
07	rw	0	GPIO Bit 7
06	rw	0	GPIO Bit 6
05	rw	0	GPIO Bit 5
04	rw	0	GPIO Bit 4
03	rw	0	GPIO Bit 3
02	rw	0	GPIO Bit 2
01	rw	0	GPIO Bit 1
00	rw	0	GPIO Bit 0

Table 4-22 General Purpose I/O Configuration Register (GPIOCF)

Bit(s)	rw	reset	Description/Function
15:11	r	0	Reserved
10	rw	0	Enable Dedicated PWM on GPIO[10]
09	rw	0	Enable SETPON PWM on GPIO[9]
08:02	r	0	Reserved
01	rw	0	Disable Internal Pullup on GPIO[1]
00	rw	0	Disable Internal Pullup on GPIO[0]

SECTION 5
Peripheral Port Interface

5.1 Highlights

When configured in Master Mode, the Peripheral Port Interface serves as a bi-directional, 3 wire, synchronous serial output interface intended to communicate with various peripherals chips. Due to the variety in serial interfaces used by various vendors, the Peripheral Port Interface is fully programmable. The User can program the length of both the command and data portions of a transfer, the polarity of the clock and enable lines, and the shift direction of the data. Following the completion of the transfer, a flag is raised which the DSP can detect either by polling a bit or through an interrupt.

5.2 Master Mode Operation

When programmed for Master Mode the Peripheral Interface becomes a fully configurable Master for a 3-wire synchronous serial bus. Master Mode is selected by setting the "Master Mode Enable" bit in the Master Mode Control Register (MSTCTL).

5.2.1 Master Mode Serial Interface

In Master mode, the three Peripheral Interface pins are configured as follows:

- SDATA is bi-directional
- SCLK and SDEN are outputs

All characteristics of the Peripheral Interface are programmable:

- Programmable SCLK frequency: BUSCLK / (1 -> 16)
- Programmable SCLK polarity
- Programmable Shift Direction: MSB or LSB first
- Programmable SDEN polarity
- Programmable Command packet length: (0 -> 16 bits)
- Programmable Data packet length: (1 -> 16 bits)

The SCLK frequency is set in the Clock Configuration 2 Register (CLCFG2). The remaining

features are all controlled through the Master Control Register (MSTCTL).

Table 5-1 Master Mode – Serial Interface Control Register (MSTCTL)

Bit(s)	rw	Reset	Description/Function
15	rw	0	MSB first – Determines the sequence of the data shifted out. When set to a one, the MSB bit is shifted out as the first bit.
14	rw	0	SCLOCK polarity –When set to a one the data is shifted out on the rising edge of the clock. The slave clocks the data-in on the falling edge of the clock.
13	rw	0	SDEN polarity – When set to a one, the SDEN signal is active high to the slave.
12	rw	0	SDEN disable – When set, SDEN is not asserted during a serial transfer.
11	rw	0	Read Data Turnaround mode. When clear, one SCLK cycle turnaround delay is inserted between last command bit sent out and first data bit read in on SDATA line.
10	rw	0	Peripheral Port GPIO Enable – if set, the SCLK, SDATA, and SDEN pins become GPIO's controlled through the two GPIO registers. Peripheral Port Master Enable (below) must be for this bit to take effect.
09	rw	0	Peripheral Port Master Enable – if set, Peripheral Port is configured as a Master. The default is slave mode.
08	rw	0	Command Packet Enable – When set, enables the shifting of the Command Packet portion of a serial transfer.
07:04	rw	0000	Command Length – this value + 1 is the number of bits shifted out of HSTDT1 register
03:00	rw	0000	Data Length — this value + 1 is the number of bits shifted into or out of the HSTDT2 register.

A Master Mode transaction is initiated by writing to the MMTCTL register. Writing a 1 to bit 0 starts a write transaction and writing a 0 to bit 0 starts a read transaction. Immediately following the start of a transaction the Peripheral Interface shifts out the Command Packet previously loaded into the HSTDT1 registers. After the Command Packet has been transferred, the Data Packet is either shifted out of or into the HSTDT2 register depending on whether the transaction was a read or a write. After the transfer is complete, the Master Mode Transfer Complete bit (multiplexed with the Command Pending bit) is set in the INTPND register and also on the USERIN1 bit of the DSP. It is cleared by writing a 1 to its bit in the INTPND register, or any access to the MMTCTL, HSTDT1, or HSTDT2.

Table 5-2 Master Mode Transfer Control Register (MMTCTL)

Bits(s)	rw	Reset	Description/Function
15:01	w		Reserved
00	w		When in Master Mode, writing a 1 to this bit initiates a Master Mode Write transfer. Writing a 0 to this bit initiates a Master Mode Read transfer.

To avoid bus contention on read transfers, one SCLK cycle may be inserted between the Control packet, driven from the Peripheral Interface, and the Data packet, driven from the peripheral device. This is only true for reads; Serial writes do not have the extra SCLK between the Control packet and Data Packet, both of which are driven from the Peripheral Interface. See bit 11 of the MSTCTL register.

Figure 5-1 and Figure 5-2 give examples of both a Master Mode read and write cycle.The configuration for this example would be as follows:

- Shift MSB first
- SDEN polarity = 0
- SCLK polarity = 1
- Command Packet enabled
- Command Length = 3
- Data Length = 7
- Read Data Turnaround mode = 0

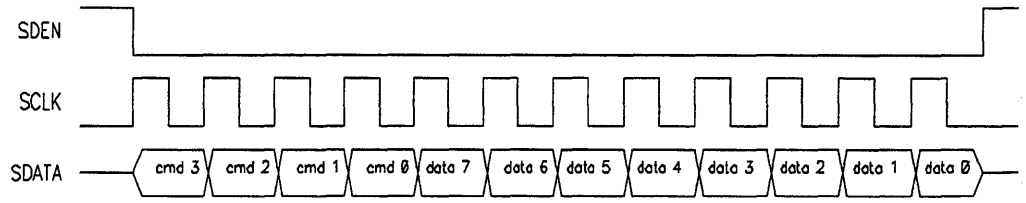


Figure 5-1 Master Mode Write Timing Example

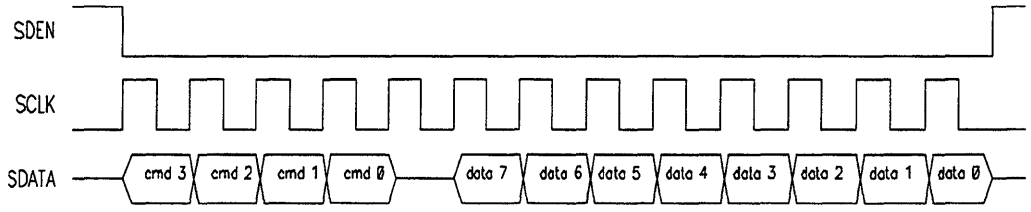


Figure 5-2 Master Mode Read Timing Example

5.3 Master Mode – Data Registers

The HSTDT1 register is used for the Command Packet, and HSTDT2 is used for the Data Packet. When shifting out MSB first, the circuit begins with the bit denoted by the Command Length or Data Length field of the MSTCTL register and works toward bit 0. When shifting out LSB first, shifting will begin with bit 0 and work up until the bit position specified by either Command Length or Data Length has been shifted out.

Table 5-3 Host Interface Data 1 Register (HSTDT1)

Bit(s)	rw	Reset	Description/Function
15:00	rw	0000h	Host Interface Data 1 – Used as the source of the Command packet

Table 5-4 Host Interface Data 2 Register (HSTDT2)

Bit(s)	rw	Reset	Description/Function
15:00	rw	0000h	Host Interface Data 2 – This register is the source/destination of the Data portion of a serial transfer.

6.1 Highlights

The Servo Decoder, with its programmable sequencers, processes the information contained in the servo field of an embedded disk servo system. Serial data from the pulse detector in the read channel IC is the primary input to this section. The internal Data Synchronizer has a programmable data cell length and two modes of bit detection, pulse detection and phase detection. Rotary synchronization is maintained by the programmable Timing Mark Sequencer, and Burst Sequencer. Index Bit detection and Gray Code decoding functions are performed. Index and Servo Sector signals are generated as well as a Data Sector signal for implementing split data field formats.

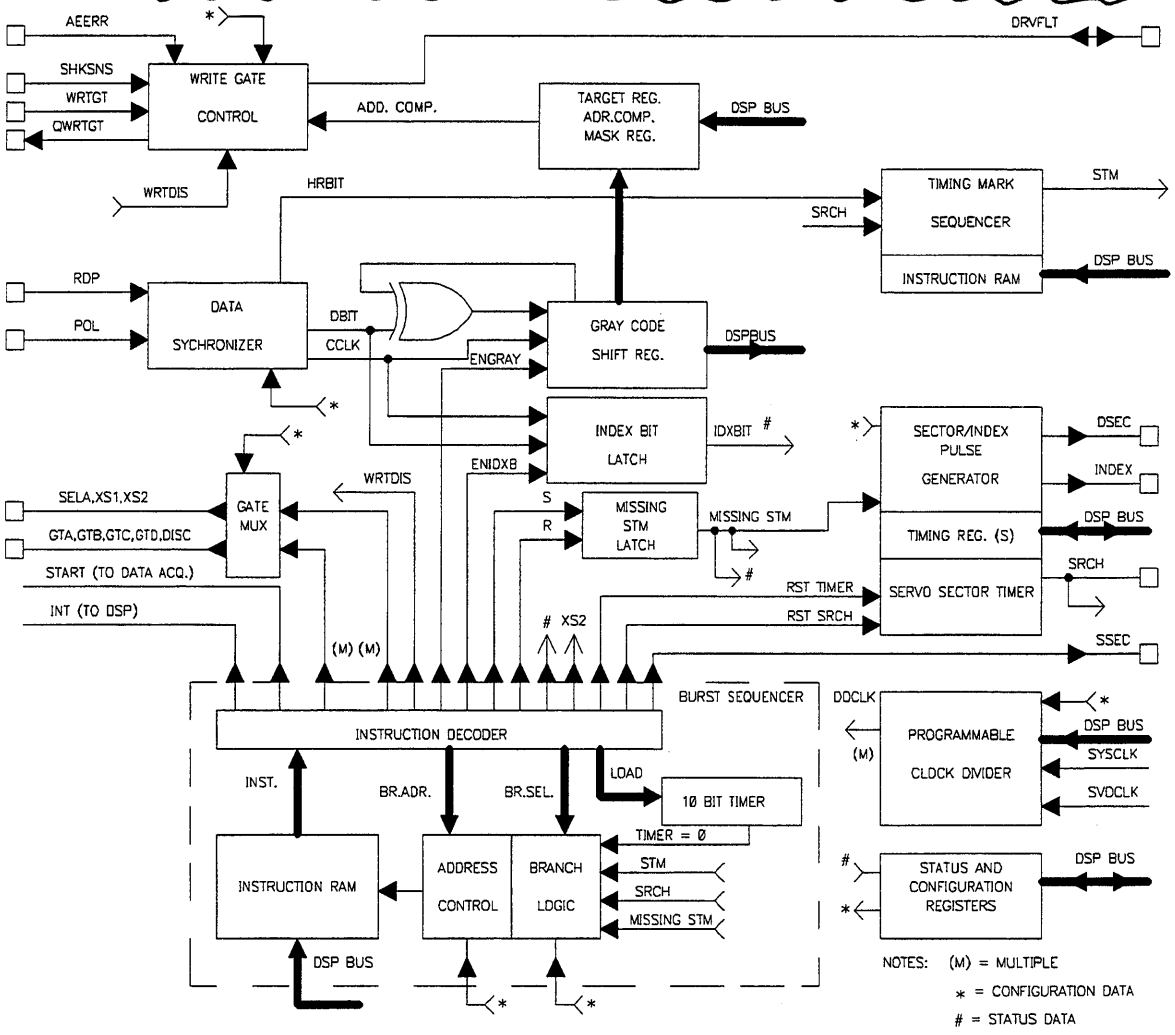


Figure 6-1 Servo Decoder/Sequencer Block Diagram

Programmable gating to the burst sampling circuitry in the Read Channel IC is provided as well as control signals for it's AGC circuitry. Interrupts, start pulse for the Analog Data Acquisition system, and auxiliary output pins, are programmable in the Burst Sequencer. Track Address compare, rotary timing information, external Shock input signal, and internal status states are used to qualify the Write Gate signal.

6.2 Functional Description

6.2.1 Data Synchronizer

The data synchronizer accepts serial digital data from the Read Channel IC in three different formats, (1) RDP/POL, (2), RDP only, and (3), NRZ. The format of the data expected from the Read Channel is selected in the Decoder Configuration Register (DECCFG). The active level of the RDP and/or POL for all three formats can also be defined via the DECCFG register.

With the RDP/POL format, which is the default, the Read Channel provides two signals: Read Data Pulse (RDP), which is the qualified pulse that occurs at the peaks of the read data carrier and Polarity (POL), which is the signal that specifies the polarity of that pulse.

With the RDP only format, the data synchronizer receives only RDP from the Read Channel. The data synchronizer contains the circuitry to synthesize a POL like signal. To utilize this functionality, one of the Burst Sequencer outputs (GT_A, GT_B, etc.), must be looped back into the POL input. This signal will serve as the reset for a Toggle flip-flop, which is clocked by the trailing edge of the RDP pulse. The output of this T flip-flop is the internal synthesized polarity signal. The Burst Sequencer should be programmed to hold the gate tied to POL low until such a time in the servo pattern that it can guarantee the polarity of the next pulse into the data synchronizer. At this time the gate should be driven high, releasing the reset of the Toggle flip-flop, which will then toggle with each RDP pulse, thus generating the internal polarity signal.

With the NRZ format, the data synchronizer receives only one signal from the Read Channel in which both pulse and polarity information is encoded. The rising edge of the signal indicates a pulse of one polarity and the falling edge of the signal indicates a pulse of the other polarity. This signal should be connected to the RDP input of the chip.

The Data Synchronizer generates three output data streams used within the Servo Decoder block: HRBIT, DBIT, and CCLK.

HRBIT is used by both the Timing Mark Sequencer and the Burst Sequencer for synchronization purposes. It is generated by synchronizing positive and/or negative pulses (as per the configuration in the DECCFG register) from the Read Channel to DCLK. The DCLK period determines the minimum spacing between two consecutive pulses of the same polarity. If for example, DCLK has a 25ns period (40 MHz), the minimum positive-positive or negative-negative pulse spacing is 25ns.

DBIT and CCLK are used in the Servo Decoder when shifting in Servo Header and Track Address bits. DBIT is the logic value of a particular bit-cell and CCLK is the clock which shifts a bit into the shift register. The Data Synchronizer supports two detection modes for generating DBIT and CCLK: Pulse Mode or Phase Mode.

In Pulse Mode, a DBIT with a value of logic 1 is defined as the presence of a positive, negative or either pulse (configured in the DECCFG register) on RDP within a window defined by X DCLK cycles. A DBIT with a value of logic 0 is defined as the absence of the selected pulses within the window. The number of DCLKs per window is configured in the CCLK Divisor field in the

CLCFG1 register. Figure 6-2 shows a block diagram of the Pulse Mode logic and Figure 6-3 shows some example timing for Pulse Mode.

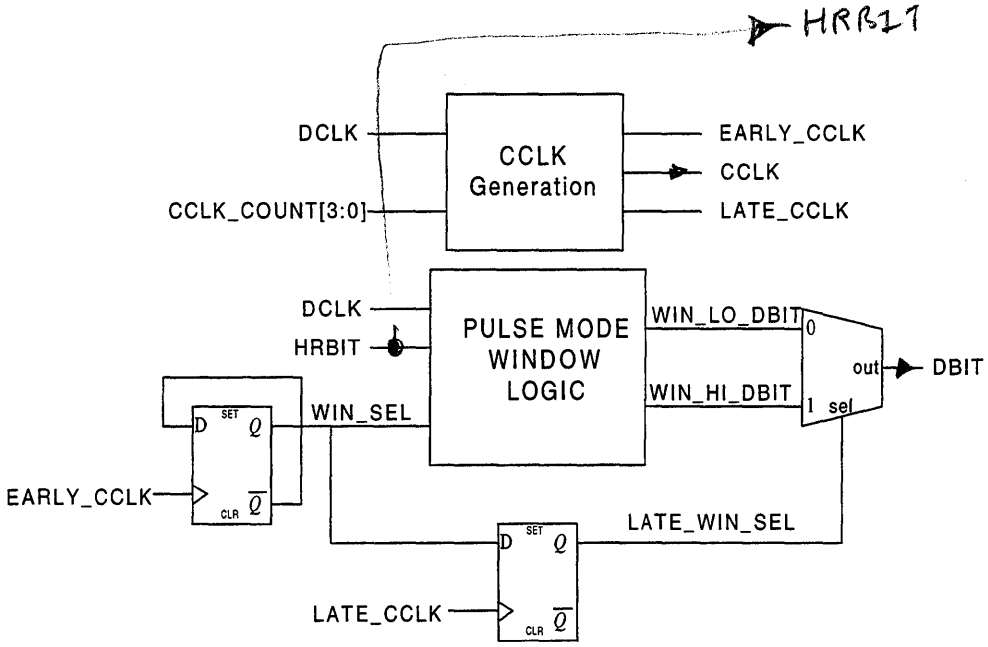
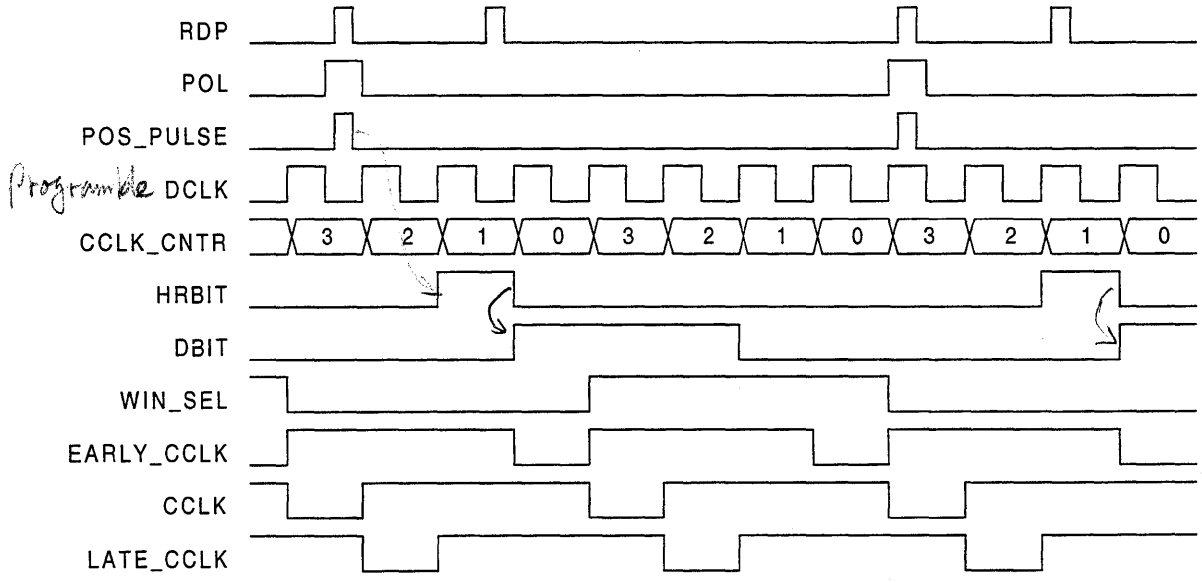


Figure 6-2 Data Synchronizer, Pulse Mode Block Diagram



Note: CCLK Divisor (CLKCGFG1[7:4]) = 0011

Figure 6-3 Data Synchronizer Timing (Pulse Mode Detection)

In Phase Mode, the value of a bit-cell is determined by the phase relationship between the positive pulse and the negative pulse. If the negative pulse occurs within the first half of the cell, DBIT is 1. If the negative pulse occurs in the second half of the cell, the DBIT is 0. The location of the half cell boundary is timed from positive pulse using PCLK. The number of clock half-cycles to the half cell boundary is programmable in the Decoder Control Register (DECCTL). The source for PCLK is either the Servo Clock pin (SVOCLK) or SYSCLK as determined in the Clock configuration Register 1 (CLCFG1). The half cell counter uses both edges of the selected clock for increased resolution. CCLK is generated directly from the positive pulse of a bit-cell. Figure 6-4 shows a block diagram of the Phase Mode logic and Figure 6-3 shows some example timing for Phase Mode.

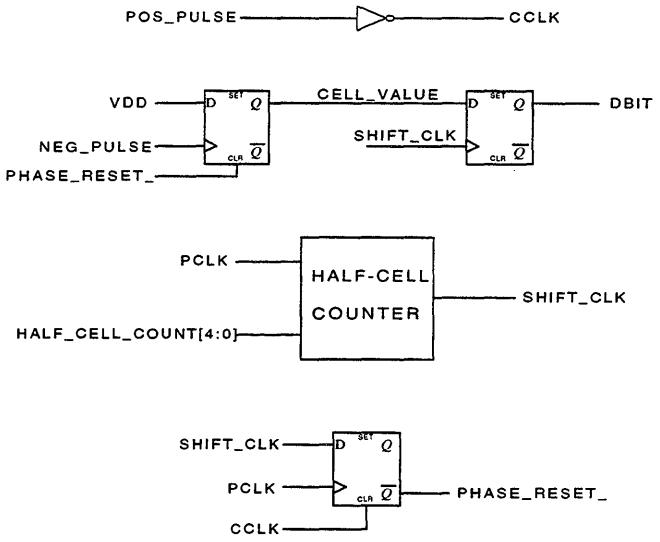


Figure 6-4 Data Synchronizer, Phase Mode Block Diagram

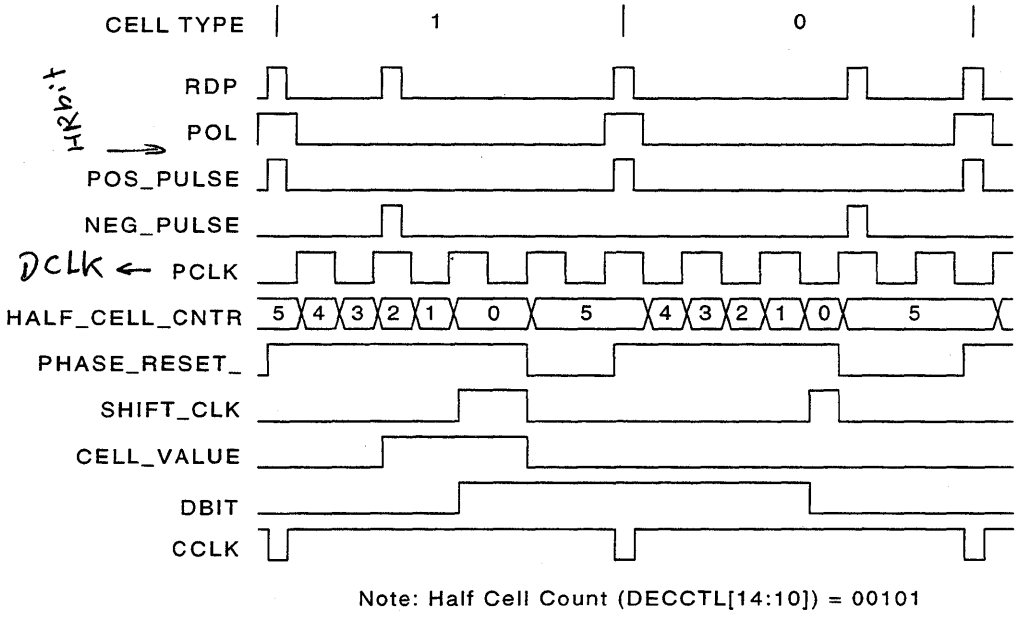


Figure 6-5 Data Synchronizer Timing (Phase Mode Detection)

The data synchronizer (for HRBIT generation and for Pulse Mode) as well as all other Servo Decoder/Sequencer circuits are timed by Decode Clock (DCLK). This clock has a programmable divider (in the CLCFG1 register) to allow operation at the System Clock (SYSCLK) frequency, or at a lower frequency for power savings or format considerations. The Servo Clock pin (SVOCLK) may be selected rather than SYSCLK for the input to the DCLK divider allowing the optimization of both the DSP cycle time and the Servo Decoder/Sequencer rate.

6.2.2 Servo Header and Gray Code Detection

Two 16-bit shift registers are available for loading Servo Header and Gray Code information from a servo sector: the Index Shift Register (INDXSH) and the Gray Code Shift Register (GRAYSH). Each of these shift registers has a corresponding Target Register and Mask Register. The Target register is loaded with the expected information from the servo sector. The mask register is loaded with a mask indicating which bits are valid for comparison (1 = valid bit). This allows for easy configuration of various gray code lengths and for different servo field information.

Both 16 bit shift registers are loaded with the data bits from the Data Synchronizer when enabled by the appropriate Burst Sequencer signals. Bits are shifted into the INDXSH Register when the INDX_SHIFT_EN bit of the burst sequencer is set and bits are shifted into the GRAYSH register when the GRAY_SHIFT_EN bit of the burst sequencer is set. Gray-encoded data will be converted to binary as it is shifted if the GRAY_DECODE bit of the burst sequencer is a logic one along with the shift enable. The binary coarse position data can be read by the DSP and is also used in the Write Gate qualification circuitry.

To facilitate debugging of the Burst Sequencer maps, the GRAY_DECODE function can be overridden by setting a bit in the Decoder Control register (DECCTL). This is useful for comparing the Gray-encoded data shifted into INDXSH and GRAYSH to the data coming off the heads, without having to modify the Burst Sequencer maps.

6.2.3 Write Gate Qualification

Circuitry is provided to qualify the write gate from the data path controller before being used by the write circuitry. (see Figure 6-6) The active level of Write Gate and the Qualified Write Gate is selectable in the DFLCFG register. All of the following conditions must be met before a write gate is allowed: The Write Disable bit in the Decoder Control register must be inactive. (This provides a means for the DSP to block the write gate if the "at speed" and "on track" conditions are not met.) The coarse position information from the Gray Code shift register and Index shift register must match the value in their respective Target Register. A write disable signal from the Burst Sequencer must be inactive. The Missing STM Latch must be inactive. The Shock Input Latch must not be active. And the AE WR ERR and AE RD ERR Latches must not be set. Safety Mask bits are provided in (WRGTDF) Write Gate / Drive Fault Register to allow for testing or diagnostics. These will allow the write gate to pass without intervention by the selected safety. Qualified Writer Gate can also be gated by Servo Sector (SSEC) if enabled via the DFLCFG "Servo Sector gates QWRTGT" control bit.

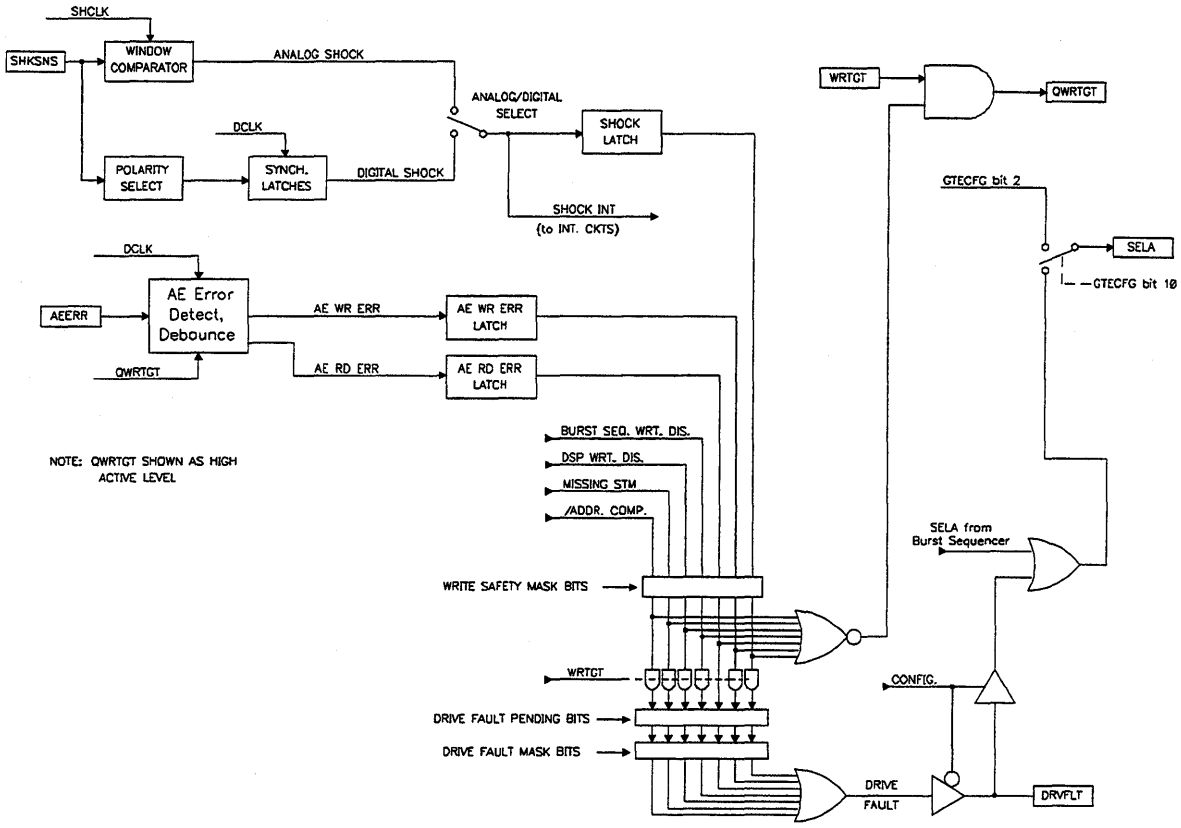


Figure 6-6 Write Gate/Drive Fault Circuits

6.2.4 Shock Sensor Input

The Shock Sensor Input pin can be configured for a digital or an analog input signal. If configured for a digital input signal the active level can be specified. If configured for an analog signal the input pin SHKSNS is processed initially by a sampling mode window comparator circuit before being used in the Write Gate Qualification circuit. The sampling architecture ignores narrow noise spikes that could cause false "Shock Events" (see Performance Specifications section for characteristics) The "Shock Event" is latched and that latched output can be included in the Write Gate Qualification and Drive Fault circuits. The non-latched shock signal is used by the Interrupt logic.

6.2.5 Drive Fault Signal

A Drive Fault can be generated on the DRVFLT pin if that pin is configured as an output (see DFLCFG). Its alternate use is as an input to be OR'ed with the Burst Sequencer Signal that controls the SELA output. (See Figure 6-6.)

The Drive Fault is generated if the QWRTGT is blocked by one of the safety paths or if the AE RD Latch is set. Each one of these conditions can be blocked by a bit in the WRGTDF Register. To support headerless applications, the Missing STM drive fault can be configured to generate a drive fault on reads as well as writes. The mode is enabled by setting a bit in the DFLCFG register.

6.2.6 AE Error Input

An input is provided for including the fault monitoring of the (AE) Arm Electronics or Head Interface Electronics. (see Figure 6-6) By default, a fault is reported by the AE by reversing the polarity of the QWRTGT signal and returning it to the AEERR pin. The AE pin is then XORed with the QWRTGT pin, with a result of logic 1 indicating an error. This XOR function can be disabled by setting the AEERR XOR Disable bit in the Drive Fault Configuration Register (DFLCFG). In this mode, an AE error is indicated by a logic one (after the possible inversion with Negative AEERR set in the DFLCFG register) on the AEERR input. This comparison can be blanked for a programmable number of DCLKs whenever QWRTGT makes a transition by setting the AEERR Blank Count in the DFLCFG Register to a non-zero value. If the AEERR pin indicates an error when QWRTGT is in its active level (write) the AE WR ERR Latch is set. If the AEERR pin indicates an error when QWRTGT is at its inactive level (read) the AE RD ERR Latch is set. These latches can be included in the Write Gate Qualification and Drive Fault Circuits.

6.2.7 Timing Mark Sequencer

The Timing Mark Sequencer is a fully programmable sequencer optimized for the detection of disk drive timing mark patterns. The sequencer works from the principle that a timing mark can be described as a series of spaces, in which there should be no data bits, and windows, in which a data bit should be found. See Figure 6-7 for an example of a 2 of 3 timing mark in which the first bit and either of the final two bits must be detected for a valid timing mark.

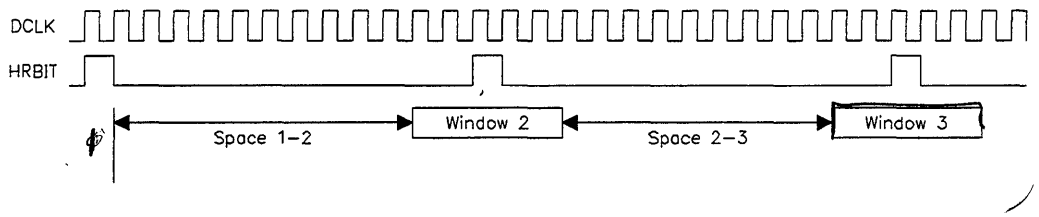


Figure 6-7 2 of 3 Timing Mark Example

The Sequencer RAM is loaded with instructions from the DSP data bus (see Appendix A for a memory map of the sequencer RAM). In addition to this bus, the Timing Mark Sequencer has three inputs, Search Window Open (SRCH), High Resolution Bit (HRBIT) and Decode Clock (DCLK), and one output, Servo Timing Mark (STM). The SRCH input enables the sequencer to search for the address mark. The HRBIT input is the synchronized data from the read channel, and the DCLK input is a programmable clock from the Programmable Clock Generator. The Servo Timing Mark output is a bit in the sequencer instruction which is asserted when a timing mark is found. The following sections will describe the major blocks of the Timing Mark Sequencer. Refer to Figure 6-8.

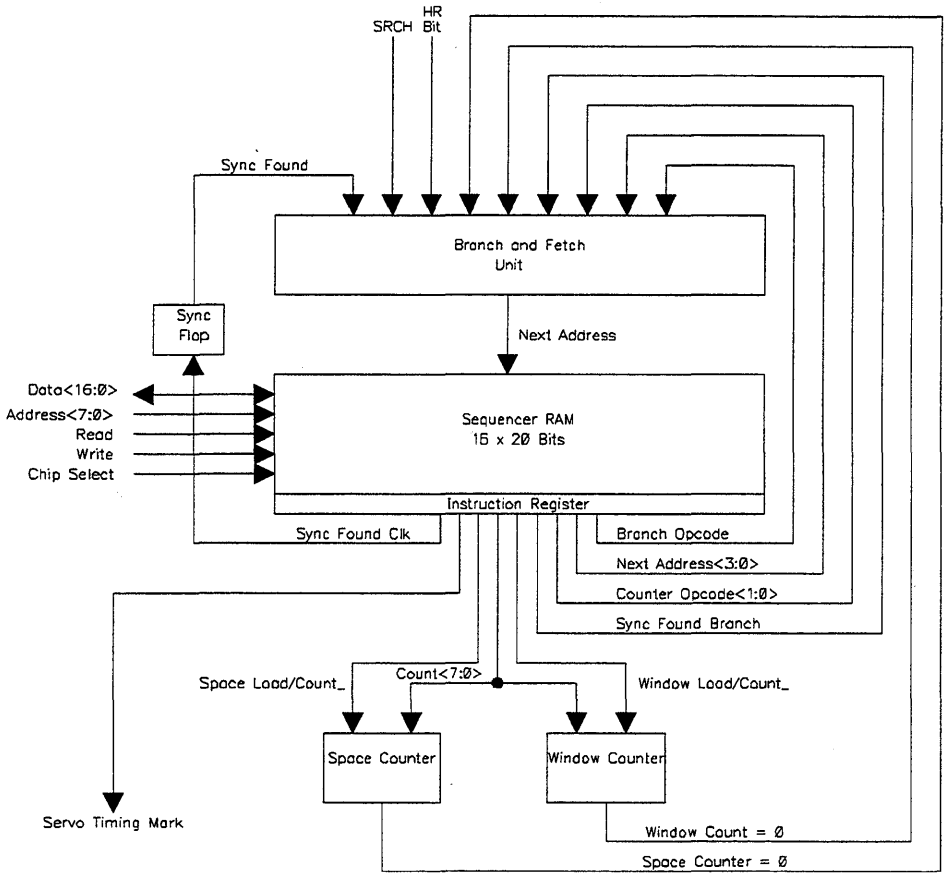
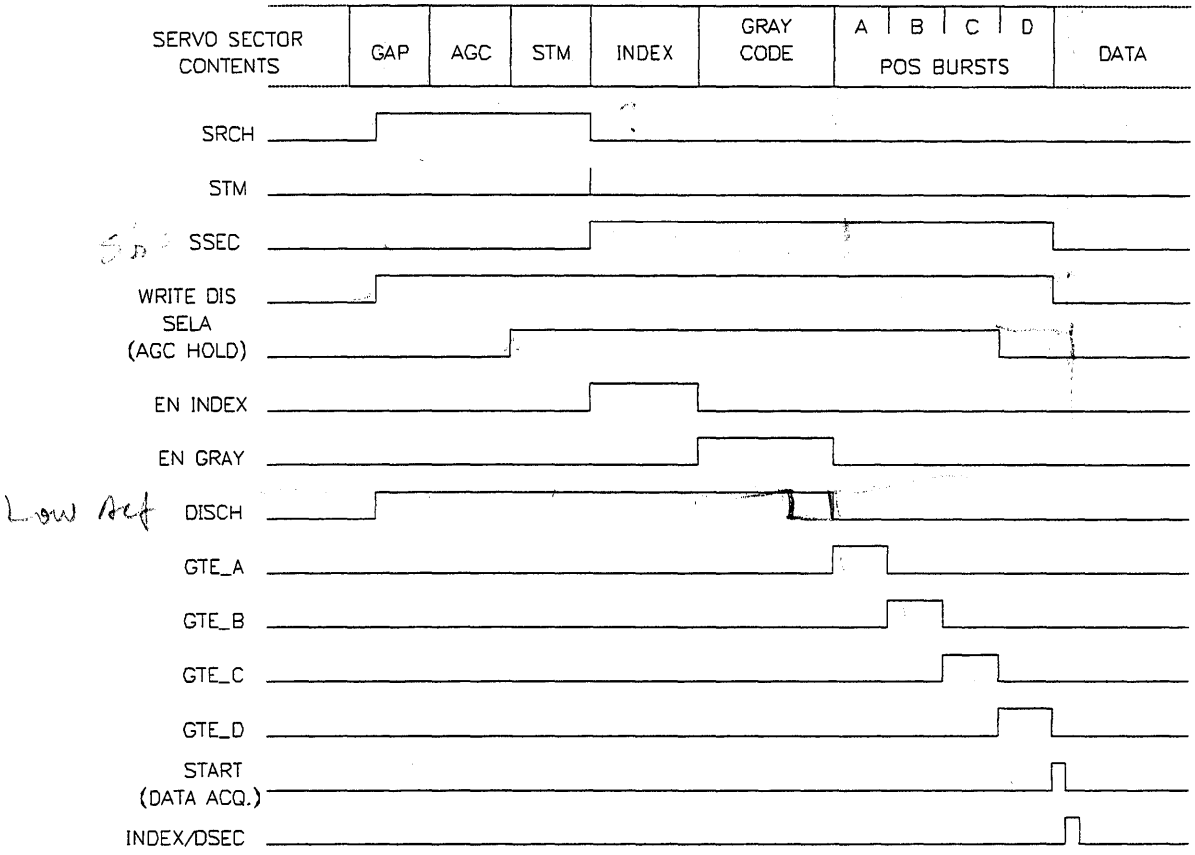


Figure 6-8 Timing Mark Sequencer Block Diagram

Timing Mark Sequencer instructions are 20 bits in length. Table 6-1, "Timing Mark Sequencer Instruction Format," on page 53 and Figure 6-9 details the format and function of the bits in the instruction.



NOTE: ALL CHANGES OCCUR ON DCLK'S RISING EDGE

The Burst Sequencer consi
ter, Next Address Control l
DCLK rate. The format of
instruction in three consecu
this specification.

uction Decoder regis-
imer is clocked at the
DSP loads each
ry in the Appendix of

Typically, the Burst Sequer
allow for servo patterns wh
Sequencer to 'see' HRBITs
on the presence of an HRB
the presence of an HRBIT i
Reset bit of the Burst Sequ

ta Synchronizer. To
k (requiring the Burst
r to detect and branch
= 1. When enabled,
Flag bit. The Flag

The following Burst Sequencer pseudo code illustrates the use of this mode:

0 Set GRAY_SHIFT_EN, Reset FLAG – shift in gray bits

1 Release Flag Reset, Branch on Flag bit to 3 – branch on presence of HRBIT

2 Resync error, go somewhere to handle – did not see HRBIT

3 Set GRAY_SHIFT_EN, Reset FLAG – shift in additional gray bits

Table 6-2 Burst Sequencer Instruction Format

Bit(s)	Name	Description/Function
38	Gray Decode	When active, bits shifted into either the Gray Shift Register or the Index Shift Register will be Gray Decoded.
37	Set Missing STM	Sets the "Missing STM" Latch.
36	Reset Missing STM	Resets the "Missing STM" Latch. Reset overrides Set if both set and reset are active.
35	Flag Set	Sets the Flag bit in the Status Register to the DSP. This bit can be used as intermediate storage or by the branch circuitry or to provide status to the DSP. To allow for servo patterns which include sync bits other than the timing mark, it is also possible to have the flag bit set by the presence of HRBIT on the rising edge of DCLK. This feature is enabled by setting a bit in the DECCTL register.
34	Flag Reset	Resets the Flag bit in the Status Register to the DSP. Reset overrides Set if both bits are active.
33	Search Reset	Resets the Search Window (SRCH) when active.
32	Timer Reset	Resets the Sector Timer when active.
31	Gate A	GTA pin is High when this bit is "1". Can be used to gate the Read Channel IC's Position Burst Detectors.
30	Gate B	GTB pin is High when this bit is "1". Can be used to gate the Read Channel IC's Position Burst Detectors.
29	Gate C	GTC pin is High when this bit is "1". Can be used to gate the Read Channel IC's Position Burst Detectors.
28	Gate D	GTD pin is High when this bit is "1". Can be used to gate the Read Channel IC's Position Burst Detectors.
27	Discharge	DISC pin is High when this bit is "1". Can be used to discharge the Read Channel IC's Position Burst Detectors.
26	Select A	SELA pin is High when this bit is "1". Can be used for AGC Control or other gate.
25	Extra Select 2	XS2 pin is High when this bit is "1". Can be used for extra gate signal, for (BOS), or for sync.

Bit(s)	Name	Description/Function
24	Extra Select 1	XS1 pin is High when this bit is "1". Can be used for extra gate signal, (EOS) or for sync.
23	Write Disable	Disables a write during a Servo Sector by blocking the Qualified Write Gate (QWRTGT)
22	Enable Gray Code Shift	Allows the CCLK from the Data Synchronizer to shift in the Gray Code bits into the Gray Shift Register. This is the window for the Gray Code Field. ** (see programming notes)
21	Enable Index Shift	Allows the CCLK from the Data Synchronizer to shift in the Index bits into the Index Shift Register. This is the window for the Index Field. ** (see programming notes)
20	Servo Sector	SSEC pin is high in all states that this bit is set.
19	Start Data Acquisition	The rising edge of this bit starts the Analog Data Acquisition System. This bit must go inactive for one DCLK before asserting again.
18:16	Branch Type	000 – Never Branch. Always execute the next sequential instruction when the state timer times out. 001 – Missing STM. Branch if Missing STM Latch is set. * 010 – SRCH. Branch if the Search Window is open. * 011 – STM and SRCH. Branch if the Servo Timing Mark is detected and the Search Window is Open. * 100 – Flag. Branch if the Flag bit in the Decoder Status Register is set. * 101 – Branch Bit. Branch if the Branch Bit is set in the Decoder Control Register. * 110 – Branch Bit Timed. Branch when timer = 0 if the Branch Bit is set in the Decoder Control Register. * 111 – Unconditional Branch, always branch immediately. Note:* = Go to next sequential instruction when the state timer times out.
15	Interrupt	An interrupt is sent to the DSP if this bit is set.
14:10	Branch Address	This is th e 5-bit branch address which is taken if the branch condition specified in the Branch Type field is true.
09:00	Timer Load Value	This value is loaded into the State Timer at the beginning of an instruction. The instruction is executed for this time period + 1 unless a branch condition becomes valid. (1 is the minimum value that should be specified. A 0 is not valid) A value of 1 gives you 2 periods.

** Programming notes:

Enable Index Latch and Enable Gray Code Shift need to remain active for 2 DCLKs after the actual data window to allow for the latching of the data. In practice Enable Index Latch would be lengthened by two DCLKs and Enable Gray Code Shift would be delayed 2 DCLKs on the rising and falling edges.

6.2.9 Sector Timing Control

The timing input reference for the generation of the index and sector signals is the Servo Timing Mark (STM) from the Timing Mark Sequencer The Timing resolution of the counters is controlled by DCLK. An example of a typical track timing is shown in Figure 6-11.

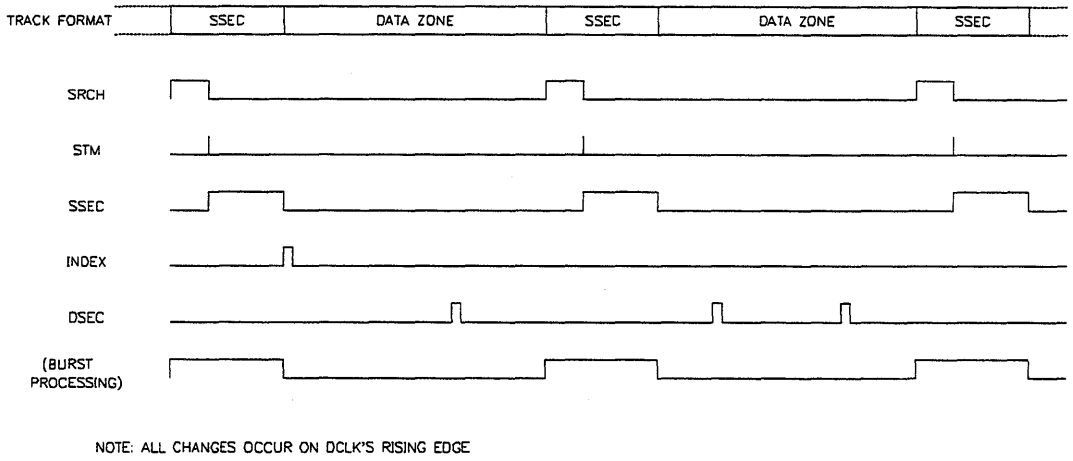


Figure 6-11 Track Timing Example

All timing in the Sector Timing Control section uses a 16 bit up counter that is reset each time a Servo Timing Mark (STM) is detected by means of the Burst sequencer commanding a reset. The value of the counter is captured in the Sector Time register just prior to the reset. This value can be read by the DSP for spin at-speed checks. The resolution of the counter is determined by DCLK, (see Figure 6-12). The Servo Sector (SSEC) signal is controlled by the Burst Sequencer. It is typically set at the Servo Timing Mark and is reset at the end of the Servo Sector. The Data Synchronizer can change the Data Bit definition and detection modes as a function of this signal. For example, this allows for the Servo Timing Mark (STM) to be detected using both polarities of pulses whereas single polarity pulses may be selected for the other fields.

The Data Sector (DSEC) signal is pulsed at a programmable time delay(s) after a Servo Timing Mark is detected. A maximum of eight can be generated at any locations, during the data field, in order to implement split data field formats. The timing information is updated by the DSP before the end of the Servo Sector. The eight PULTMx registers must be loaded in increasing order, i.e. if 3 DSECs are required, PULTM0-PULTM2 must be used, if 6 DSECs are required, PULTM0 – PULTM5 must be used. All unused PULTM registers should be loaded with 0xFFFF. These registers are always writable, but may be read only of the Sector Timer is disabled (DECCTL[3] = 0).

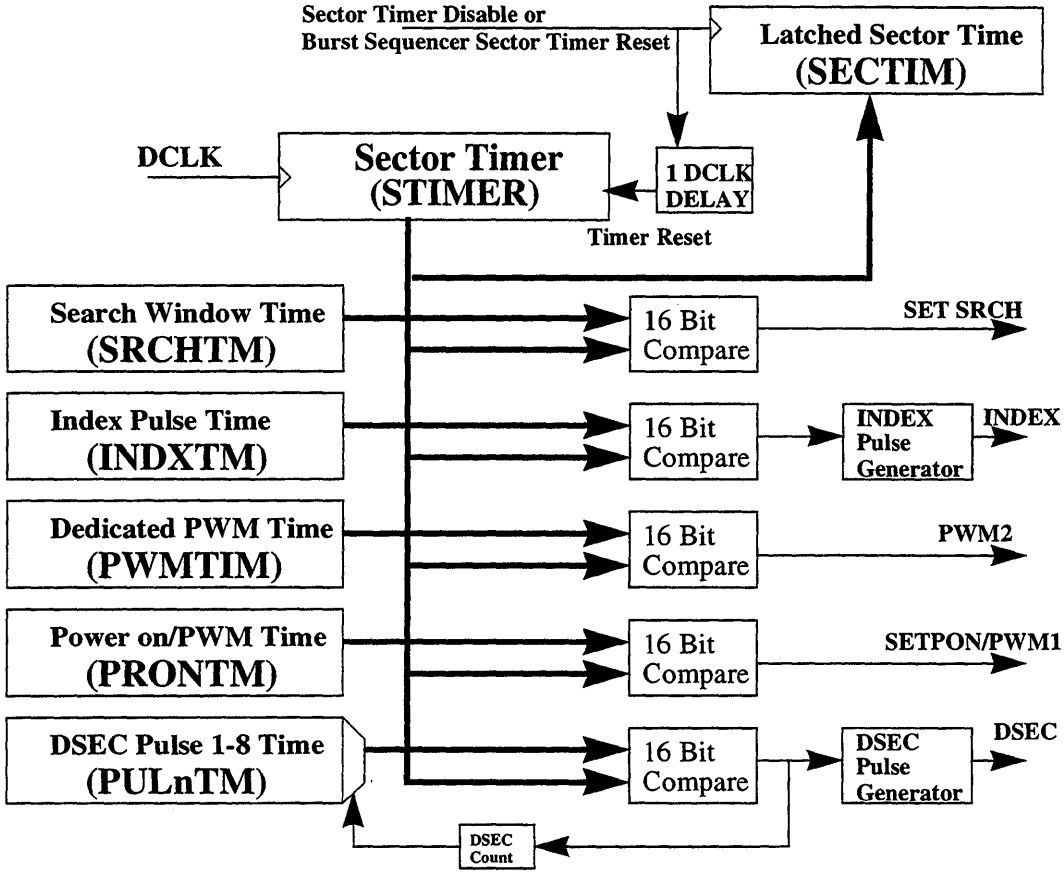


Figure 6-12 Sector Timing Control

An Index pulse (INDEX) can be generated a programmable time delay(s) after a Servo Timing Mark is detected, by loading the INDXTM register with the desired DCLK count. After the Index pulse is generated, another Index pulse will NOT be generated until the INDXTM register is re-written.

The pulse width of the INDEX and DSEC signals are programmable from 4 DCLKs wide to 16 DCLKs in steps of 4 clock periods.

The Search Window Open (SRCH) signal is set at a programmable time delay after the last timing mark and is set such that it comes up in the gap before the next expected Servo Sector. When this signal is high it allows the Timing Mark Sequencer to search for the Servo Timing Mark. The time is determined by the value loaded in the Search Time register. The Search Time register can be updated by the DSP as a function of the missing STM latch to implement missing STM algorithms. During the initial synchronization, the DSP can open the Search Window by setting a bit in the Decoder Control Register. This bit is reset and the STM Found bit is set in the status register when a Servo Timing Mark is found and the burst sequencer commands a SRCH reset. SRCH may also be reset by writing a bit in the Decoder Status register (DECSTA).

The SRCH pin can be programmed to output one of several internal Servo Decoder/Sequencer signals to aid in development and testing. The pin signal selection does not affect the function of the internal SRCH signal. The choice of signal is determined by bits in the Decoder Control Register (DECCTL). The default signal at power up is SRCH.

The SETPON signal produces a pulse (one timer count wide) used by the power management system when the value in the Power On Time Register (PRONTM) equals the Sector timer count. This is used to sequence up circuitry prior to a servo burst or SRCH going active. This signal can also generate an interrupt between Servo Bursts for over sampling or other functions. (see Interrupts section)

The Sector Timing Control block also controls up to two PWM generators. The PWM output pins are multiplexed with the GPIO[10:9] pins. The function of the GPIO/PWM pins is configured in the GPIOCF register. The first PWM generator has a dedicated compare register, PWMTIM, and the second PWM generator shares the SETPON compare register. If the second PWM generator is enabled in the GPIOCF register, the SETPON functionality is lost. When a pin is configured for PWM mode, the pin goes high when the TIMER_RESET is asserted in the Burst Sequencer, and then goes low when the timer value matches the corresponding compare register.

6.2.10 Sequencer/Decoder Registers

The configuration of this subsystem is setup during initialization by writing to the Decoder Configuration register. The Decoder Control register is used to control and input information to the Decoder/Sequencer. The Decoder Status register is read by the DSP to obtain status information from the Decoder/Sequencer subsystem.

The 8 Gate, Discharge, and Select pins that are normally controlled by the Burst Sequencer can be controlled directly by the DSP by setting bits in the Decoder Control register. This allows for control of the Read Channel IC between bursts. This also provides additional user-defined outputs if they are not used by the Burst Sequencer

Table 6-3 Drive Fault Configuration Register (DFLCFG)

Bit(s)	rw	Reset	Description / Function
15	r	0	Reserved
14	rw	0	Servo Sector gates QWRTGT. When set this bit allows Servo Sector (SSEC) from the burst sequencer unmaskable disable control of QWRTGT.
13	rw	0	If set, Missing STM Drive Faults will be generated during reads.
12	rw	0	DRVFLT pin enable. If this bit is set the DRVFLT pin is driven by the internal "Drive Fault" signal. If this bit is reset the DRVFLT pin is an input that is OR'ed with the Burst Sequencer signal that generated the SELA output. (See GTECFG bit 10.)
11	rw	0	Negative QWRTGT. Defines the active state of the QWRTGT output as being a low level if this bit is set.
10	rw	0	Negative WRTGT. Defines the active state of the WRTGT input as being a low level if this bit is set.
9	rw	0	If set, AEERR XOR is disabled.
8	rw	0	Negative AEERR. Defines the active state of the AEERR input as being a low level if this bit is set.
7:0	rw	A0h	AEERR Blank Time

Table 6-4 Write Gate Disable Drive Fault Register (WRGTDF)

Bit(s)	rw	Reset	Description / Function
15	rw	0	Reserved
14	rw	0	DSP Write Gate Disable, Mask bit. Safety is disabled if this bit is set.
13	rw	0	Burst Sequencer Write Gate Disable, Mask bit. Safety is disabled if this bit is set.
12	rw	0	Missing STM Write Gate Disable, Mask bit. Safety is disabled if this bit is set.
11	rw	0	Index/Address Compare Write Gate Disable, Mask bit. Safety is disabled if this bit is set.
10	rw	0	Shock Write Gate Disable, Mask bit. Safety is disabled if this bit is set.
9	rw	0	AE Write Error Write Gate Disable, Mask bit. Safety is disabled if this bit is set.
8	rw	0	AE Read Error Write Gate Disable, Mask bit. Safety is disabled if this bit is set.
7	r	0	Reserved
6	rw	0	DSP Write Disable, Drive Fault Mask bit. A Drive Fault will be generated if the QWRTGT is blocked by this safety and this bit is reset.
5	rw	0	Burst Sequencer Write Disable, Drive Fault Mask bit. A Drive Fault will be generated if the QWRTGT is blocked by this safety and this bit is reset.
4	rw	0	Missing STM Write Disable, Drive Fault Mask bit. A Drive Fault will be generated if the QWRTGT is blocked by this safety and this bit is reset.
3	rw	0	Index/Address Compare Write Disable, Drive Fault Mask bit. A Drive Fault will be generated if the QWRTGT is blocked by this safety and this bit is reset.
2	rw	0	Shock Write Disable, Drive Fault Mask bit. A Drive Fault will be generated if the QWRTGT is blocked by this safety and this bit is reset.
1	rw	0	AE Write Error Write Disable, Drive Fault Mask bit. A Drive Fault will be generated if the QWRTGT is blocked by this safety and this bit is reset.
0	rw	0	AE Read Error Write Disable, Drive Fault Mask bit. A Drive Fault will be generated if the "AE RD ERR" latch is set and this bit is reset.

Table 6-5 Drive Fault Pending Register (DFLTPD)

Bit(s)	rw	Reset	Description / Function
15:7	r	0	Reserved.
6	rw	0	DSP Write Disable, Drive Fault Pending. Writing a "1" to this location resets it.
5	rw	0	Burst Sequencer Write Disable, Drive Fault Pending. Writing a "1" to this location resets it.
4	rw	0	Missing STM Write Disable, Drive Fault Pending. Writing a "1" to this location resets it.
3	rw	0	Index/Address Compare Write Disable, Drive Fault Pending. Writing a "1" to this location resets it.
2	rw	0	Shock Write Disable, Drive Fault Pending. Writing a "1" to this location resets it.
1	rw	0	AE Write Error Write Disable, Drive Fault Pending. Writing a "1" to this location resets it.
0	rw	0	AE Read Error Write Disable, Drive Fault Pending. Writing a "1" to this location resets it.

Table 6-6 Data Sector Pulse 1 Time Register (PUL1TM)

Bit(s)	rw	Reset	Description / Function
15:00	rw	x	This register contains a value equal to the number of DCLKs after resetting the sector timer that the first DSEC pulse will be generated. A minimum value of 0x0002 is required. Writing 0x0000 to this register disables this function.

Table 6-7 Data Sector Pulse 2 Time Register (PUL2TM)

Bit(s)	rw	Reset	Description / Function
15:00	rw	x	This register contains a value equal to the number of DCLKs after resetting the sector timer that the second DSEC pulse will be generated. A minimum value of 0x0002 is required. Writing 0x0000 to this register disables this function.

Table 6-8 Data Sector Pulse 3 Time Register (PUL3TM)

Bit(s)	rw	Reset	Description / Function
15:00	rw	x	This register contains a value equal to the number of DCLKs after resetting the sector timer that the third DSEC pulse will be generated. A minimum value of 0x0002 is required. Writing 0x0000 to this register disables this function.

Table 6-9 Data Sector Pulse 4 Time Register (PUL4TM)

Bit(s)	rw	Reset	Description / Function
15:00	rw	x	This register contains a value equal to the number of DCLKs after resetting the sector timer that the fourth DSEC pulse will be generated. A minimum value of 0x0002 is required. Writing 0x0000 to this register disables this function.

Table 6-10 Data Sector Pulse 5 Time Register (PUL5TM)

Bit(s)	rw	Reset	Description / Function
15:00	rw	x	This register contains a value equal to the number of DCLKs after resetting the sector timer that the fifth DSEC pulse will be generated. A minimum value of 0x0002 is required. Writing 0x0000 to this register disables this function.

Table 6-11 Data Sector Pulse 6 Time Register (PUL6TM)

Bit(s)	rw	Reset	Description / Function
15:00	rw	x	This register contains a value equal to the number of DCLKs after resetting the sector timer that the sixth DSEC pulse will be generated. A minimum value of 0x0002 is required. Writing 0x0000 to this register disables this function.

Table 6-12 Data Sector Pulse 7 Time Register (PUL7TM)

Bit(s)	rw	Reset	Description / Function
15:00	rw	x	This register contains a value equal to the number of DCLKs after resetting the sector timer that the seventh DSEC pulse will be generated. A minimum value of 0x0002 is required. Writing 0x0000 to this register disables this function.

Table 6-13 Data Sector Pulse 8 Time Register (PUL8TM)

Bit(s)	rw	Reset	Description / Function
15:00	rw	x	This register contains a value equal to the number of DCLKs after resetting the sector timer that the eighth DSEC pulse will be generated. A minimum value of 0x0002 is required. Writing 0x0000 to this register disables this function.

Table 6-14 Decoder Configuration Register (DECCFG)

Bit(s)	rw	Reset	Description / Function
15	rw	0	Detection Mode B. Defines the detection mode used by the data synchronizer. 0 = pulse detection mode. 1 = phase detection mode. This bit is used when SSEC is high.
14	rw	0	Detection Mode A. Defines the detection mode used by the data synchronizer. 0 = pulse detection mode. 1 = phase detection mode. This bit is used when SSEC is low.
13	rw	0	Negative POL. Defines the active state of the input POL as being a low level when this bit is set. A low level in would indicate a positive pulse if this bit is set. A high level in would indicate a positive pulse if this bit is reset.
12	rw	0	Negative RDP. Defines the active state of the input RDP as being a low level when this bit is set. The negative edge of the input signal will indicate a pulse if this bit is set. The positive edge of the input signal would indicate a pulse if this bit is reset.
11	rw	0	Shock Sensor pin Mode Select. When this bit is set the SHKSNS pin is processed as an analog signal using an internal window comparator. When this bit is reset the SHKSNS pin is processed as a digital signal whose active level is defined by bit 10.
10	rw	0	Negative SHKSNS. Defines the active state of the input SHKSNS as being low level when set. If this bit is reset, a high level on the SHKSNS pin indicates a "shock" event. This bit is only valid if bit 11 is low. (digital Shock Sensor mode)
09	rw	0	Synthesized Polarity Mode – when set, RDP polarity is synthesized.
08	rw	0	Block Data Pulse Enable. If this bit is set, the DSEC and INDEX pulses will be blocked in sectors that have the "Missing STM" latch set.
07:05	rw	0...0	INDEX/DSEC pulse width. Sets the pulse width of the INDEX and DSEC signals to (this number of DCLKs times 4) + 1. A zero value disables the pulse generator.
04	rw	0	NRZ Mode – when set data synchronizer is configured for NRZ type RDP data.
03	rw	0	Positive Pulse Enable B. Decodes positive pulses as bits in the Data Synchronizer when set. (bits 2 and 3 may be both set for all pulses) This bit is used when SSEC is high.
02	rw	0	Negative Pulse Enable B. Decodes negative pulses as bits in the Data Synchronizer when set. (bits 2 and 3 may be both set for all pulses) This bit is used when SSEC is high.
01	rw	0	Positive Pulse Enable A. Decodes positive pulses as bits in the Data Synchronizer when set. (bits 0 and 1 may be both set for all pulses) This bit is used when SSEC is low.
00	rw	0	Negative Pulse Enable A. Decodes negative pulses as bits in the Data Synchronizer when set. (bits 0 and 1 may be both set for all pulses) This bit is used when SSEC is low.

Table 6-15 Decoder Control Register (DECCTL)

Bit(s)	rw	Reset	Description / Function
15	r	0	Reserved
14:10	rw	0000	Half Cell Count. The binary value of these bits are loaded into the Half Cell Counter in the Data Synchronizer at the beginning of a cell. (mode 1 phase detect). This defines the location of the center of the bit cell. This value +1 is the number of PCLK half-cycles from the positive pulse (RDP tailing edge) to the center of the cell.
09:07	rw	000	SRCH pin Signal Output Select: 000 = SRCH 001 = HRBIT 010 = DBIT 011 = CCLK 100 = GRAY_DECODE 101 = STM 110 = INDX_SHIFT_EN 111 = GRAY_SHIFT_EN
06	rw	0	Set Flag on HRBIT When set, the presence of HRBIT will set the Burst Seq. Flag bit.
05	rw	0	Master Gray Decode Disable – When set, the Gray Decoding of bits shifted into either the Gray or Index Shift Registers will be disabled, regardless of the state of the GRAY_DECODE bit of the Burst Sequencer.
04	rw	0	Open Search Window. Setting this bit raises SRCH which starts the Timing Mark sequencer looking for a Servo Timing Mark. Used for initial acquisition. It is reset by the Burst Sequencer when a Servo Timing Mark (STM) is found by means of the reset SRCH line. This bit sets the SRCH window independent of the set search command from the sector timer. A reset from the Burst Sequencer or (DECSTA) register overrides this set. Writing a 0 to this location will not reset this bit.
03	rw	0	Sector Timer Enable. Allows the Sector Timer to run when high. Resets the timer when it is low.
02	rw	0	Burst Branch. The Burst Sequencer will branch if this bit is set and the Branch Type field is set for this branch type.
01	rw	0	Write Disable. The QWRTGT signal is inactive if this bit is set.
00	rw	0	Burst Sequencer Run Enable. When this bit is low the instruction counter is held a instruction 00000b. All Instruction decoder outputs are 0. This allows the loading of the Instruction RAM. When the bit is set high the instruction at 00000b executes.

Table 6-16 Decoder Status Register (DECSTA)

Bit(s)	rw	Reset	Description / Function
15	rw	0	Missing STM. This bit is high if the "Missing STM" latch is set. Writing a 1 to this bit will clear this status bit.
14	rw	0	Reserved.
13	r	1	Index/Address Compare. This bit is active when the Masked comparison of the Index & Gray Code registers to their corresponding target register is valid.
12	r	0	Decoder Flag Bit. This bit is set and reset by the Burst Sequencer to save intermediate results or to signal conditions to the DSP.
11	rw	0	Servo Timing Mark Detected. This bit is set if the Timing Mark Sequencer output (STM) goes active. This bit is reset by writing a one to this bit location.
10	r	0	Reserved
09	r	0	INDEX. Indicates the state of the INDEX signal.
08	r	0	DSEC. Indicates the state of the DSEC signal.
07	r	0	SRCH. Indicates the state of the SRCH signal.
06:05	rw	0	Reserved.
04	rw	0	AE Write Error Latch. This latch is set if the AEERR pin is not at the same logic level as QWRTGT when QWRTGT is indicating a write. This condition is checked after a time period to "debounce" the signal. Writing a "1" to this location resets it. The latch output is used by the Write Gate Qualification and Drive Fault circuits if it is enabled.
03	rw	0	AE Read Error Latch. This latch is set if the AEERR pin is not at the same logic level as QWRTGT when QWRTGT is indicating that a write is not allowed (read mode). This condition is checked after a time period to "debounce" the signal. Writing a "1" to this location resets it. The latch output is used by the Write Gate Qualification and Drive Fault circuits if it is enabled.
02	rw	0	Shock Input Latch. This bit is set if a "Shock" signal is applied to the SHKSNS pin. The Shock signal can be defined as a digital active high or low signal or an analog signal. (see Performance Specifications section for details.) Writing a "1" to this location resets it. The latch output is used by the Write Gate Qualification and Drive Fault circuits if it is enabled.
01	r	0	Reserved
00	w	0	Reset SRCH. Writing a "1" to this bit Resets the Search Window (SRCH).

Table 6-17 Target Address Register (TGTADR)

Bit(s)	rw	Reset	Description / Function
15:00	rw	x	This register contains the binary Gray Code Target Track Address for the Write Gate Qualifier Address Compare circuitry. This register is updated by the DSP at the beginning of a seek.

Table 6-18 Address Compare Mask Register (ADRMSK)

Bit(s)	rw	Reset	Description / Function
15:00	rw	0	This register contains Gray Code mask bits used in the Write Gate Qualifier Address Compare circuitry. When a bit location is set in this register the Address Compare circuit will not require a bit match in that location. (don't care). This allows for the use of 1 to 16 bit Gray Code lengths.

Table 6-19 Gray Code Shift Register (GRAYSH)

Bit(s)	rw	Reset	Description / Function
15:00	rw	x	This register contains the binary Track Address decoded from the Gray Code field in the last Servo Sector. This is read by the DSP for coarse position information and is used for the Write Gate Qualifier Address Compare circuitry. This location can be written only if the "Enable Gray Code Shift" signal from the Burst Sequencer is low.

Table 6-20 Gating Configuration Register (GTECFG)

Bit(s)	rw	Reset	Description / Function
15	rw	0	Gate A Aux. Enable. Gives bit 7 direct pin control.
14	rw	0	Gate B Aux. Enable. Gives bit 6 direct pin control.
13	rw	0	Gate C Aux. Enable. Gives bit 5 direct pin control.
12	rw	0	Gate D Aux. Enable. Gives bit 4 direct pin control.
11	rw	0	Discharge Aux. Enable. Gives bit 3 direct pin control.
10	rw	0	Select A Aux. Enable. Gives bit 2 direct pin control. If this bit is set it also overrides the optional control of the Select A pin by the Drive Fault pin. (see DFLCFG bit 12)
09	rw	0	Extra Select 2 Aux. Enable. Gives bit 1 direct pin control.
08	rw	0	Extra Select 1 Aux. Enable. Gives bit 0 direct pin control.
07	rw	0	Gate A Aux. Has pin control when bit 15 is set.
06	rw	0	Gate B Aux. Has pin control when bit 14 is set.
05	rw	0	Gate C Aux. Has pin control when bit 13 is set.
04	rw	0	Gate D Aux. Has pin control when bit 12 is set.
03	rw	0	Discharge Aux. Has pin control when bit 11 is set.
02	rw	0	Select A Aux. Has pin control when bit 10 is set.
01	rw	0	Extra Select 2 Aux. Has pin control when bit 9 is set.
00	rw	0	Extra Select 1 Aux. Has pin control when bit 8 is set.

Table 6-21 Index Target Register (IDXTGT)

Bit(s)	rw	Reset	Description / Function
15:00	rw	x	This register contains the binary Index Target for the Write Gate Qualifier Address Compare circuitry, allowing for gray codes beyond 16 bits and head information to be included in the address compare. This register is updated by the DSP at the beginning of a seek.

Table 6-22 Index Compare Mask Register (IDXMSK)

Bit(s)	rw	Reset	Description / Function
15:00	rw	0	This register contains mask bits used in the Write Gate Qualifier Index Address Compare circuitry. When a bit location is set in this register the Index Address Compare circuit will not require a bit match in that location. (don't care). This allows for the use of 1 to 16 bit Index Code lengths.

Table 6-23 Index Shift Register (INDXSH)

Bit(s)	rw	Reset	Description / Function
15:00	rw	x	This register contains the binary Index Address decoded from the Index field in the last Servo Sector. This is read by the DSP for coarse position information and is used for the Write Gate Qualifier Address Compare circuitry. This location can be written only if the "Enable Index Shift" signal from the Burst Sequencer is low.

Table 6-24 Sector Time Register (SECTIM)

Bit(s)	rw	Reset	Description / Function
15:00	r	x	This register contains the value of the Sector Timer captured when the timer was last reset. This is usually done by the Burst Sequencer when a Servo Timing Mark is found.

Table 6-25 Search Window Time Register (SRCHTM)

Bit(s)	rw	Reset	Description / Function
15:00	rw	x	This register contains a value that is compared to the Sector Timer. When this value is reached, the Search Window (SRCH) is set that enables the Timing Mark Sequencer. A minimum value of 0x0002 is required. Writing 0x0000 to this register disables this function. A reset from the Burst Sequencer or the (DECSTA) register overrides this set.

Table 6-26 Sector Timer Register (STIMER)

Bit(s)	rw	Reset	Description / Function
15:00	r	x	This register contains the present value of the Sector Timer.

Table 6-27 Power On Time Register (PRONTM)

Bit(s)	rw	Reset	Description / Function
15:00	rw	x	This register contains a value equal to the number of DCLKs after resetting the sector timer that a power on (SETPON) pulse will be sent to the Power Management System and an Interrupt may be generated. A minimum value of 0x0002 is required. Writing 0x0000 to this register disables this function. This register also servers as the PWM1 timer when enabled. See Table 6-29 for a description of the PWM functionality.

Table 6-28 Index Pulse Time Register (INDXTM)

Bit(s)	rw	Reset	Description / Function
15:00	rw	x	This register contains a value equal to the number of DCLKs after resetting the sector timer that the Index pulse will be generated. A minimum value of 0x0002 is required. Writing 0x0000 to this register disables this function.

Table 6-29 Dedicated PWM Time Register (PWMTIM)

Bit(s)	rw	Reset	Description / Function
15:00	rw	x	This register contains a value equal to the number of DCLKs after resetting the sector timer that the Dedicated PWM generator pin (if enabled in the GPIOCF register) will go high. A minimum value of 0x0002 is required. Writing 0x0000 to this register disables this function.

7.1 Highlights

The Analog Data Acquisition system consists of an 8 channel analog multiplexer with buffer amplifiers, a 10 bit 2-step Flash A/D converter, dedicated storage registers and an Acquisition Sequencer.

The A/D convertor provides the digital data in 2's complement, fixed point format. The output data is aligned with the DSP bits 11 through 2 with the upper 4 bits a sign extension of the A/D MSb and with the lower 2 bits set to 0. This eliminates any front end DSP processing of the data such as format conversion and blanking and allows headroom for initial calculations. Six of the 8 data storage registers are general purpose ALU registers allowing immediate access to the converted data by the DSP without data moves.

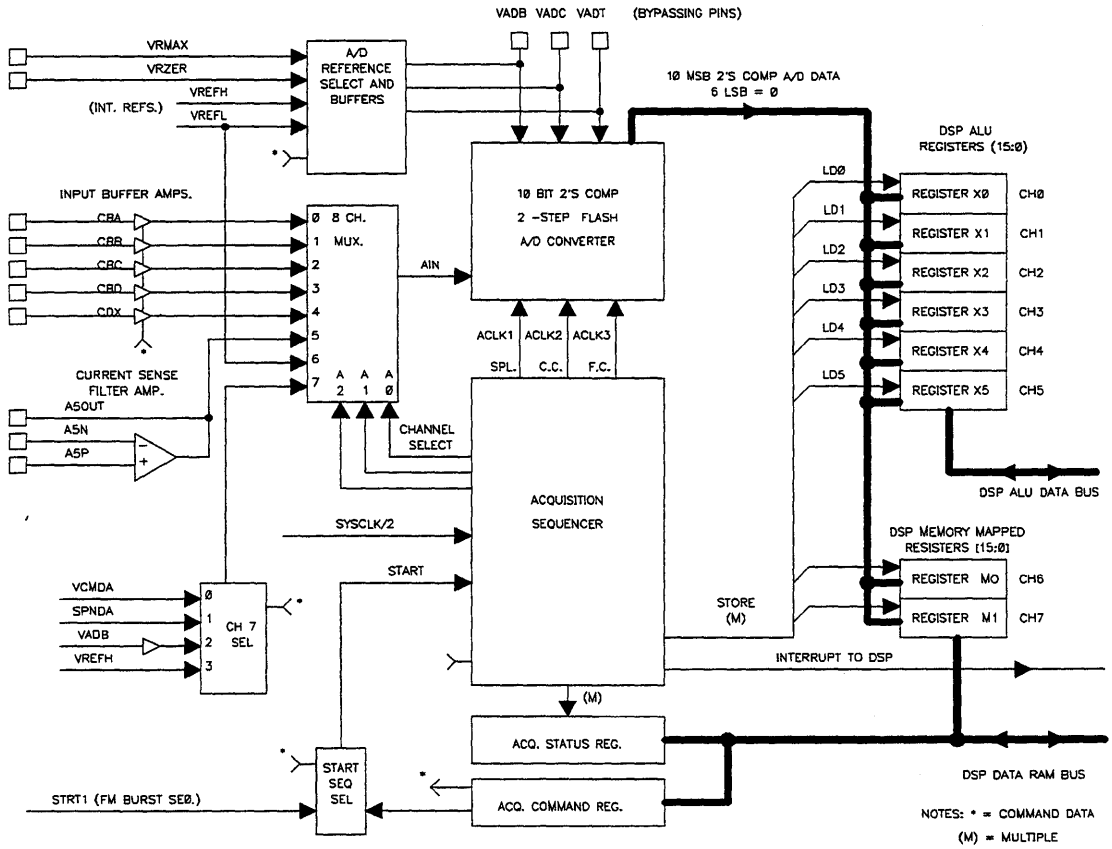


Figure 7-1 Analog Data Acquisition Block Diagram

The Acquisition Sequencer provides for automatic data conversion and storage without using the DSP for sequencing. This system architecture minimizes the use of DSP instruction times and program memory for data input and reserves them for algorithm processing.

7.2 Functional Description

The analog multiplexer has 8 channels. Five channels are available externally to read the position burst and normalization or reference information from the demodulator circuitry in the read channel IC. These channels (0 – 4) have internal high impedance buffer amplifiers at their input. Each of these channels independently may be configured to use the buffer amplifier or directly connect to the Analog Multiplexer. An additional channel (5) is connected to the output of an internal op. amp. that may be used to scale and filter the VCM current sense information. One channel (6) is connected to the analog signal reference voltage VREFL. This voltage is the "zero reference" or center of swing for all internal analog signals. The internal signal source for the last channel (7) is selected by bits in the Acquisition Command Register. (see Table 7-1) These signals may be used for internal calibrations.

Table 7-1 Acquisition Command Register (ADCCMD)

Bit(s)	rw	Reset	Description / Function
15	rw	0 1	Max. Voltage Ref. Select. Selects the maximum positive input voltage reference for the A/D convertor. 0 = internal (VREFH) 1= external (VRMAX)
14	rw	0	Zero Voltage Ref. Select. Selects the input voltage "zero" reference for the A/D convertor. This sets the center of swing for the A/D input channels. 0 = internal (VREFL) 1= external (VRZER)
13:12	rw	00	Channel 7 Select. 00 = VCM D/A output 01 = SPIN D/A output 10 = VADB + Buffer Shift Voltage 11 = Max. Ref. VREFH
11:09	rw	000	DSP Interrupt. The DSP will be sent an interrupt after the channel N is stored. N is the binary channel address represented by these bits. Bit 11 is MSB. Interrupt can be masked if no interrupt is desired.
08	rw	0	Burst Sequencer Start Enable. Setting this bit allows a start pulse from the Burst sequencer to start the "pipeline" conversion sequence.
07	rw	0	Single Channel Mode Interrupt Enable. If this bit is set, an interrupt will be sent to the DSP after the single channel conversion data has been stored.
06	rw	0	Reserved.
05	rw	0	Sequencer Enable. Setting this bit allows the sequencer to run when is receives a start pulse. Resetting this bit to "0" stops the sequencer and returns it to its reset state. This bit will override the start pulse so it must be made active before sequencing can start.
04:02	rw	0	Single Channel Mode Channel Address. These bits contain the binary channel address for a single channel conversion. Bit 4 is MSB.

Table 7-1 Acquisition Command Register (ADCCMD) (Continued)

Bit(s)	rw	Reset	Description / Function
01	rw	0	Pipeline Mode Start. Setting this bit will start the sequencer converting the 8 channels. This bit is reset by the sequencer after it starts. If both bits 0 and 1 are set, pipeline mode will start.
00	rw	0	Single Channel Mode Start. Setting this bit starts a single channel conversion. This bit is reset by the sequencer after it starts. If both bits 0 and 1 are set, pipeline mode will start.

The A/D convertor zero reference and voltage swing are determined by two external inputs or the internal voltage references. The external voltage references inputs allow for referencing the inputs to the read channel IC. The A/D reference sources are selected by bits in the Acquisition Command Register.

The center ladder buffer driving VADC and the lower ladder buffer driving VADB can be disabled during initial configuration by bits in the REFTRM register. This allows for sensing input voltage ranges that include ground. The VADB terminal would be tied to Analog ground. The VADC buffer can be disabled to minimize external parts count or an external reference can be provided by a two resistor divider between VADT and VADB to provide a lower ladder impedance.

The Acquisition Sequencer has two modes. The "Pipeline" mode and the "Single Channel" mode.

All timing is determined by the programmable clock ACLK1. The sequencer selects the analog input channel, sequences the A/D convertor, and stores the digital data.

In "pipeline" mode the sequencer can be started by the Burst Sequencer, or the DSP. The source of the start command is determined by bits in the Acquisition Command Register. When started, the sequencer selects Channel 0 of the multiplexer. The 2-step Flash A/D convertor is then stepped through it's conversion sequence. Finally the digital data is stored in the first DSP General Purpose register. This sequence is repeated until all 8 channels are converted and sequentially stored. Channels (0) through (5) are stored in DSP General Purpose registers which allows access to the data without data move instructions. Channels (6) and (7) are stored in Memory Mapped registers. (see Figure 7-2 and Figure 7-2) The sequencer then goes to its reset state until another start pulse is detected.

Figure 7-2 shows the timing of the A/D conversion sequence in "pipeline" mode. When a start is detected, the Acquisition Clock (ACLK1) starts. The analog multiplexer is switched to channel 0 on the falling edge of ACLK1 and the multiplexer output is sampled by the Coarse and Fine comparators while ACLK1 is high.

The coarse comparators alternately connect to the multiplexer output and the reference ladder. The charge balance comparators have two modes, balance (BAL) and compare (CMP). Alternating between these modes Auto-Zeros the offset. The results of the coarse comparison selects a range for the fine comparators. The fine comparators then compare the sampled input to their reference ladder. The fine comparison data is then combined with the coarse comparison data to provide the "Corrected Data". This is then stored in it's register and the Busy Bit for that channel is reset at the falling edge of ACLK1. This process is repeated for the other 7 channels in a pipeline manner with

sequences overlapping as shown.

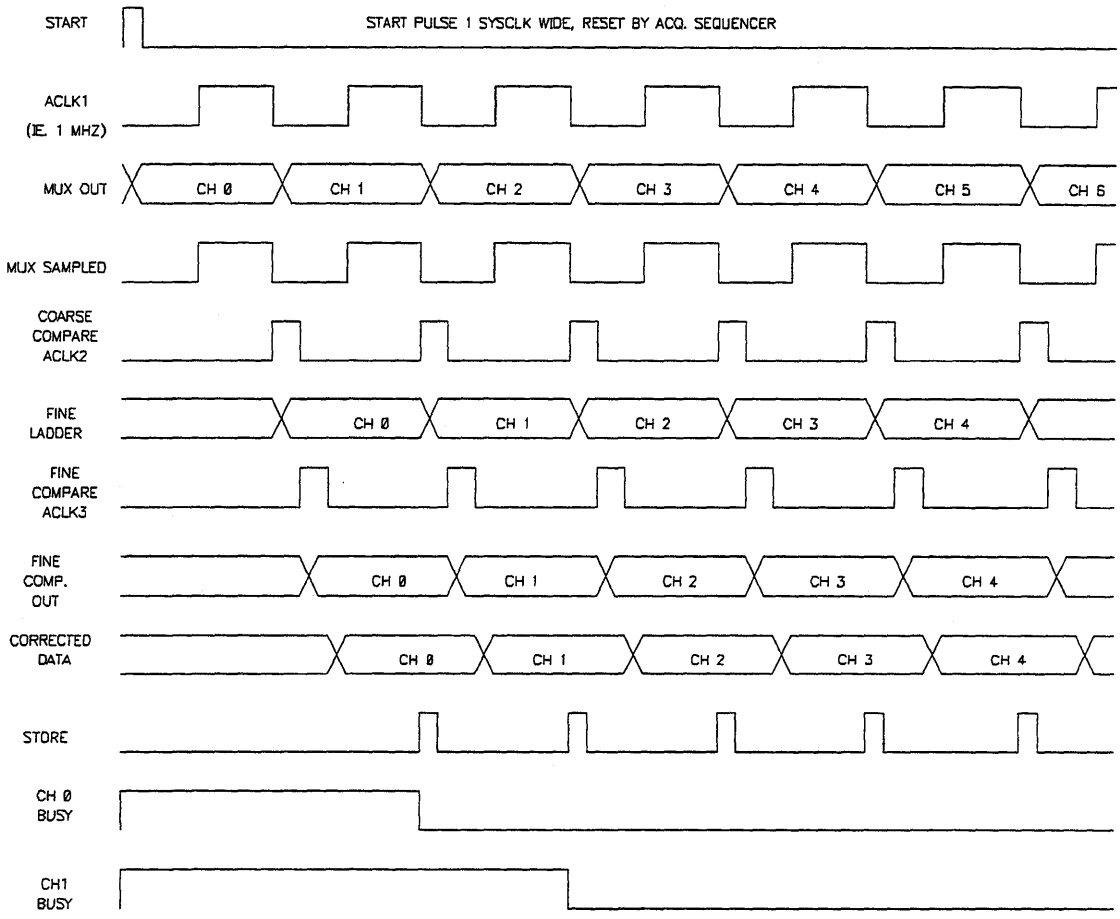


Figure 7-2 Pipeline A/D Converter Timing

An interrupt can be sent to the DSP after any channel has been converted and stored. This is controlled by bits in the Acquisition Command Register. The Acquisition Status Register (see Table 7-2) provides "Conversion Busy" bits such that the DSP can poll the state of the acquisition process. When a start pulse is detected all 8 Busy bits are set. As each channel is stored the associated channel Busy bit is reset. The DSP can read these bits to determine when to read a channel's register. These also can be monitored if a shortened conversion sequence is desired. Writing the reset bit in the Acquisition Command register will reset the sequencer back to its reset state where it will remain until the next start pulse is detected. In this manner the conversion process can be truncated.

ACLK2 and ACLK3 are adjustable pulse width clocks timed off the falling edge of ACLK1 and ACLK2 respectively. These are adjusted by setting bit values in the Clock Configuration Register 2 (CLCFG2). The timing is adjustable to allow for variation in the SYSCLK frequency. The timing requirements are listed in the Performance Specifications section.

Table 7-2 Acquisition Status Register (ADCSTA)

Bit(s)	rw	Reset	Description / Function
15	rw	0	Reserved
14	r	0	ADC Borrow Bit. For Factory Tests.
13	r	0	ADC Carry Bit. For Factory Tests.
12	rw	0	CHX (channel 4) Buffer Enable. Input is buffered when this bit is high and is direct to the Analog Mux and A/D when this bit is low.
11	rw	0	CHD (channel 3) Buffer Enable. Input is buffered when this bit is high and is direct to the Analog Mux and A/D when this bit is low.
10	rw	0	CHC (channel 2) Buffer Enable. Input is buffered when this bit is high and is direct to the Analog Mux and A/D when this bit is low.
09	rw	0	CHB (channel 1) Buffer Enable. Input is buffered when this bit is high and is direct to the Analog Mux and A/D when this bit is low.
08	rw	0	CHA (channel 0) Buffer Enable. Input is buffered when this bit is high and is direct to the Analog Mux and A/D when this bit is low.
07	r	0	Channel 7 Busy Bit
06	r	0	Channel 6 Busy Bit
05	r	0	Channel 5 Busy Bit
04	r	0	Channel 4 Busy Bit
03	r	0	Channel 3 Busy Bit
02	r	0	Channel 2 Busy Bit
01	r	0	Channel 1 Busy Bit
00	r	0	Channel 0 Busy Bit

In "Single Channel" mode a single channel can be converted and stored. This supports Auto-zeroing or allows for sampling between servo sectors. The conversion process is started by writing the Single Channel Mode Channel Address and the Single Channel Mode Start bit in the Acquisition Command register. The associated busy bit will be active until the data is stored. The timing for a single channel convert is as shown for channel 0 in Figure 7-2. An interrupt can be sent to the DSP after the storage of the data if this is set in the Acquisition Command Register.

The "Pipeline" mode has priority so the "Single Channel" mode should only be started when there is enough time to complete the sequence before the "Pipeline" mode starts. "Single Channel" mode data will be lost if overlap occurs.

Table 7-3 Data Storage Registers (ADCCH0 – ADCCH5)

Bit(s)	rw	Reset	Description / Function
15:12	rw	0	Sign Extension bits which equal bit 11.
11:02	rw	0	A/D converter channel 0 – 5 storage registers. These are general purpose DSP registers. Bit 11 is the MSb.
01:00	rw	0	Reads 0 after a channel is stored.

Table 7-4 Data Storage Registers (ADCCH6, ADCCH7)

15:12	rw	0	Sign Extension bits which equal bit 11.
11:02	rw	0	A/D converter channel 6 and 7 storage registers. These memory mapped I/O registers. Bit 11 is the MSb.
01:00	rw	0	Reads 0 after a channel is stored.

8.1 Highlights

The VCM DAC is a 12-bit, 2's complement, current steering type DAC with a buffered voltage output stage. The DAC word is left-justified (i.e., the 12 most significant bits of this register are used by the converter), making use of the saturation capability of the DSP in Q15 format.

8.1.1 VCM DAC Register

(The 12-bit command to the external VCM current control loop.)

Table 8-1 VCM DAC Register (VCMDAC)

Bit(s)	rw	Reset	Description/Function
15:04	rw	00	12-bit VCM current command.
03:00	r	00	Reserved (Read as zeros)

The voltage range of the VCM DAC is defined to be:
from $\{2 \cdot (VREFL) - VREFH\}$ to $\{VREFH\}$.

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9.1 Highlights

The IC contains an 8 bit current steering type DAC with a buffered voltage output stage. It may be used as the command for the spindle current control loop. In addition, a 16-bit counter is available for speed error measurement. The counter preset, capture, and interrupt features necessary for performing speed control are included.

9.2 Speed Regulation

The IC provides the necessary interface to perform frequency-locked speed control of the spindle motor. Flexibility in clock rate selection is provided to ensure maximum resolution accuracy. In addition, several methods of interval feedback are possible. The designer may opt to perform spindle speed correction once per revolution or once every (N) servo sector(s). The motor current (and hence the torque) generally has fewer frequency components when once-per-revolution feedback is used.

Interval feedback is available as SPNINT from one of four sources according to Table 9-1.

Table 9-1 Source of SPNINT

Source	INTSRC1	INTSRC0
USRIN pin (could be the once-around signal from spindle driver I.C., or any suitable frequency indicator)	0	0
INDEX	0	1
SSEC (Servo Sector)	1	0
/SRCH	1	1

The source of SPNINT is programmed by the INTSRC bits in register SPNCTL. The first option is to feed the motor once-around signal into the USRIN pin. By default, USRIN is an active high signal. If USRIN is active low, it can be inverted internally by setting the Negative USRIN bit in the CHPCFG register. The SPNCNT register should be loaded with 0x00 (N-1), causing a single revolution to effect a SPNINT interrupt. The second option is to select the internal INDEX signal (drive-decoded index) as the SPNINT source. Again, SPNCNT should be loaded with 0x00. The third option for the source of SPNINT is by counting any number of servo sectors (requires head to be over data). The number of events (servo sectors) required to capture the spindle speed down-counter is loaded into the 8-bit Spindle Count register SPNCNT. Finally, /SRCH (inverted SRCH signal) can be chosen as the source of SPNINT. Regardless of the source of SPNINT, the SPNCNT register determines how many events occur before the interrupt is generated (1-256). The CNTENA bit in the SPNCTL register must be low to write the SPNCNT register.

Figure 9-1 shows the options for SPNINT source selection.

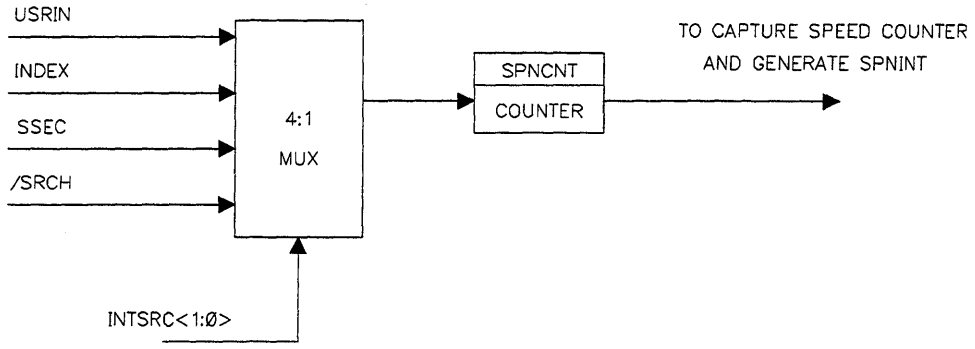

Figure 9-1 Spindle Interrupt Source Selection for Speed Regulation

For speed control using frequency feedback at once per revolution, the desired motor rotation period is programmed into the Spindle Period register (SPNTIM) as the number of clocks to be counted in one revolution At interrupt time, the contents of the SPNTIM register are transferred to a 16-bit down-counter and the previous contents of the down-counter are latched into a holding register (SPDERR). A SPNINT interrupt is generated when the counter is latched.

When the DSP is free from any servo burst processing task, the SPDERR register can be read and compared to the ideal motor period, and the speed control function may be performed (loop compensator calculation and DAC update).

For speed control at once per servo sector, the number written to the Spindle Period register would be the number of clocks corresponding to the motor rotational period divided by the number of servo sectors.

The 16-bit down counter can be configured to saturate at 0x8000 after first having counted down through 0x0000 by setting the Speed Error Saturation Enable bit in the SPNCTL register. Note that this mode does not in any way limit the initial SPNTIM count, i.e. if the SPNTIM contains 0xA000, the 16-bit counter would counter from 0xA000 down through 0x8000 to 0x0000 and then saturate when it again reaches 0x8000.

Figure 9-2 shows the speed regulation circuitry.

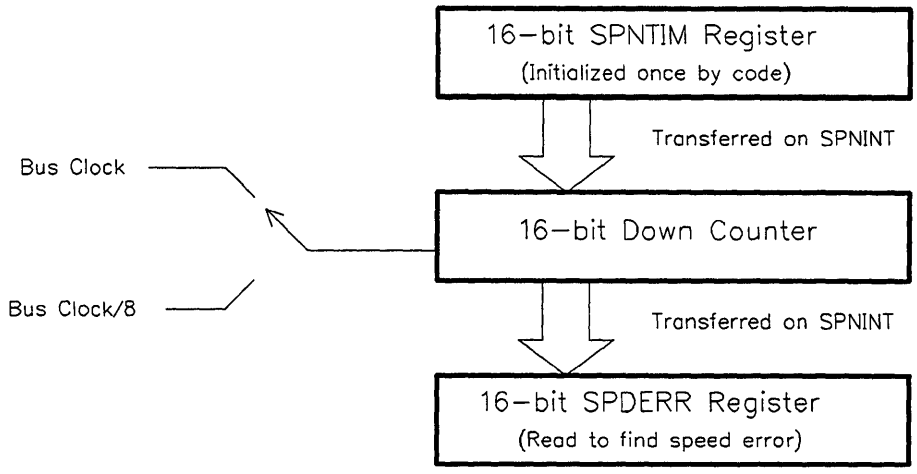

Figure 9-2 Speed Regulation Hardware

9.2.1 Spindle DAC Register

(The 8-bit command to the external spindle current or voltage control loop.)

Table 9-2 Spindle DAC Register (SPNDAC)

Bit(s)	rw	Reset	Description/Function
15:08	rw	00	Reserved (Read as zeros).
07:00	r	00	8-bit spindle current command.

The output voltage range of the Spindle DAC is defined to be:

$$\text{from } \{\text{VSS\_A}\} \text{ to } \{2 \cdot (VREFH - VREFL)\}.$$

9.2.2 Spindle Period Register

The 16-bit count Preset for the spindle speed down-counter is written to this register (SPNTIM).

Table 9-3 Spindle Period Register (SPNTIM)

Bit(s)	rw	Reset	Description/Function
15:00	rw	00	Number of clocks to determine nominal motor rotational period.

9.2.3 Speed Error Register

The 16-bit difference (error) between the desired motor period and the actual motor period.

Table 9-4 Speed Error Register (SPDERR)

Bit(s)	rw	Reset	Description/Function
15:00	r	00	16-bit, 2's complement difference (error) between the desired motor period and the actual motor period.

9.2.4 Spindle Count Register

The lower 8 bits of this register are loaded with (N-1), where N is the desired count of events needed to capture the speed timer and generate a SPNINT.

Table 9-5 Spindle Count Register (SPNCNT)

Bit(s)	rw	Reset	Description/Function
15:08	r	00	Reserved (Read as zeros)
07:00	rw	00	Event Count minus one. One less than the number of rising edges of USRIN, INDEX, SSEC, or /SRCH needed to capture speed timer and generate SPNINT.

9.2.5 Spindle Control Register

The Spindle control register, SPNCTL, is defined as follows:

Table 9-6 Spindle Control Register (SPNCTL)

Bit(s)	rw	Reset	Description/Function
15:05	r	000	Reserved (read as zeros)
04	rw	0	Spin Period Error Saturation. If set, the Speed Error Counter saturates at 0x8000, after first having counted through 0x0000.
03	rw	0	CNTENA: Counter Enable 0=Stopped, 1=Counting
02	rw	0	CLKSRC: Determines clock to the speed down-counter 0=Bus Clock, 1= Bus Clock/8
01:00	rw	00	<INTSRC1:INTSRC0>: Source of SPNINT (Refer to Table 9-1)

10.1 Power Control

10.1.1 Highlights

The Power control module provides the IC the capabilities to optimize the power dissipation of the chip in two modes: Auto and static.

In static mode the power down of each Analog module or the clock for each digital module is controlled by a specific bit in the Power control register and the wake up is either by DSP or an external event based on the module functionality.

In Auto mode, all the modules not needed for servo control are powered down by the DSP and the wake up is by start search (SRCH) and SETPON.

10.1.2 Functional Description

The Power control module is based on a single I/O mapped control/status register where a set bit signifies the specific module is powered up and a reset bit signifies a module is in stand-by (for digital) or powered down for analog.

The timers, the diag data out port and Host interface do not require a specific power control bit, they are designed to draw power only when used.

Table 10-1 Reset and Power Control Register (PWRCTL)

Bits(s)	rw	Reset	Description/ Function
13:15	r	1	Reserved
12	rw	1	Oscillator power-down start-up mode. Writing a zero to this bit causes the oscillator signal to the internal logic to be gated by an internally generated oscillator ready signal. Writing a one overrides this feature.
11	rw	1	XPCLK- Controls the clock to the input of the XPCLK programmable divider. *Wake-up* from power down mode is by setting this bit or following a reset.
10	rw	1	SYSCLK pin - Controls the clock from the Master Oscillator circuit to the SYSCLK pin. *Wake-up* from power down mode is by setting this bit or following a reset.
09	rw	1	Master Oscillator Power Down - Controls the Master Oscillator. If this bit is asserted (cleared) and the DSP sets the STOP bit in its ST0 register, the Master Oscillator is halted. See the section on the DSP system. *Wake-up* from power down mode is by External Interrupt or following a reset.

Table 10-1 Reset and Power Control Register (PWRCTL) (Continued)

Bits(s)	rw	Reset	Description/ Function
08	rw	1	RS-232 -Controls the clock to the RS232 serial port Module. When set the module clock is running all time. When reset the clock is running only when needed during transmit or receive operation. *Wake-up* from standby mode is accomplished by setting this bit, following a reset, any transition on the RX line or writing to the Transmit register
07	rw	1	Sequencer - Controls the clock to the servo mark sequencer and the servo burst decoder sequencer logic. When set the clock is running. When reset, the Burst sequencer, the Timing mark sequencer and the Data sync are in stand-by mode while the data acquisition section will be running all the time. *Wake-up* from standby mode is achieved by setting this bit, following a reset or a Servo search (SRCH) active.
06	rw	1	A/D -Controls the power to the A/D and the data Acquisition Module. When set, the Power to the module is "ON". When reset the Power to the module is turned "OFF". *Wake-up* from Power down mode is achieved by setting this bit, following a reset or a Servo search (SRCH) active. When Power is restored, the module requires a certain delay, specified in the Performance Section, to reach a stable state. User must insure this delay to meet the specified performance.
05	rw	1	A/D Ladder - Since the A/D ladder requires a longer delay to reach stability than the A/D, this bit works in conjunction with the Acquisition bit above (bit 06). If this bit is set, the A/D ladder module is never powered down. When reset to a zero, the power control follows the A/D power mode. *Wake-up* from Power down mode is achieved by setting this bit, following a reset or a SETPON signal active. When Power is restored, the module requires a certain delay, specified in the Performance Section, to reach a stable state. User must insure this delay to meet the specified performance.
04	rw	1	A/D Mux and CH5 amp – Controls the power to the front end A/D MUX and the Channel 5 Amplifier of the A/D. When set, the Power to the module is "ON". When reset the Power to the module is turned "OFF". *Wake-up* from Power down mode is achieved by setting this bit or following a reset. When Power is restored, the module requires a certain delay, specified in the Performance Section, to reach a stable state. User must insure this delay to meet the specified performance.
03	rw	1	VCMDAC – Controls the power to the VCM DAC and the Shock Sensor circuitry. When set the power/bias to the DAC is "ON". When reset the power/ bias to the DAC is turned "OFF". *Wake-up* from Power down mode is achieved by setting this bit or following a reset. When Power is restored, the module requires a certain delay, specified in the Performance Section, to reach a stable state. User must insure this delay to meet the specified performance. The SPNDAC must be powered on to use the VCMDAC due to a common bias generator.

Table 10-1 Reset and Power Control Register (PWRCTL) (Continued)

Bits(s)	rw	Reset	Description/ Function
02	rw	1	SPNDAC, Spindle – Controls the power to the Spindle DAC and all the logic related to the spindle module including the spindle control logic. When set the Power to the module is "ON". When reset the Power to the module is turned "OFF". *Wake-up* from Power down mode is achieved by setting this bit or following a reset. When Power is restored, the module requires a certain delay, specified in the Performance Section, to reach a stable state. User must insure this delay to meet the specified performance.
01	rw	1	VOLTREF & rest – Controls the power to the Voltage reference module and all the remaining hardware modules that are not affected by any of the other power control bits. When set, the Power to the Voltage reference module is "ON" and the clocks are running. When reset the Power to the Voltage reference module is turned "OFF" and the clocks are inhibited. *Wake-up* from Power down mode is achieved by setting this bit or following a reset. When Power is restored, the module requires a certain delay, specified in the Performance Section, to reach a stable state. User must insure this delay to meet the specified performance.
00	rw	1	Auto - When this bit is reset by the DSP at the end of the servo processing, the clock to all the hardware associated with the servo burst processing (i.e. Burst decoder, burst sequencer, Analog acquisition) is stopped, the A/D is powered down as well as the A/D ladder if specified by bit 05. If this bit is set by the DSP while auto mode is in progress, all the modules related are powered back on. *Wake-up* is achieved upon detection of a set or start servo search going active. (SRCH) for the A/D and sequencers and by SETPON for the A/D ladder.

park_done

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10.1.3 Power Control Summary

Table 10-2 Power Control Summary

Function	Wake up by (set)	Sleep (Reset)	Typical Recovery time (5v & 40 MHz)	Typical Power Dissipation
XPCLK	DSP, Reset	DSP	TBD	TBD
SYSCLK pin	DSP, Reset	DSP	TBD	TBD
Master Oscillator	Reset or any interrupt.	DSP	TBD	TBD
DSP	Reset, Servo search or any unmasked interrupt.	Stopped by setting the stop bit in the DSP's status register.	12 clocks (SYSCLK)	TBD
RS232	DSP, Reset, Rdx & write to Xmit register	DSP	2 clocks (SYSCLK)	TBD
Sequencer	DSP, Reset, Servo search (SRCH) in auto mode.	DSP	2 clocks (SYSCLK)	TBD
A/D Ladder and Ladder Buffers	DSP, Reset, SETPON in auto mode.	DSP	20 us	24 mW (analog supply)
A/D	DSP, Reset, Servo search (SRCH) in auto mode.	DSP	5 us	21 mW (analog supply)
VCMDAC / Shock sensor circuit	DSP, Reset	DSP	200 us (@ 99% of FV in 10 us)	17 mW (analog supply)
SPNDAC, DAC bias, spindle.	DSP, Reset	DSP	100 ms (@99% of FV in 1 ms)	13 mW (analog supply)
A/D Mux., CH5 Amp.	DSP, Reset	DSP	100 ms (@99% of FV in 1 ms)	12 mW (analog supply)
Voltage reference, Ref. buffers, and rest.	DSP, Reset	DSP	500 ms (@99% of FV in 10 ms)	53 mW (Analog Supply)

10.2 Voltage References

10.2.1 Highlights

The IC contains a bandgap reference and amplifiers to provide stable voltage references to the A/D, DACs, and to buffered external output pins. The A/D converter's references alternatively may be determined from external reference input pins independent of the DAC references. The reference and amplifier configuration is shown in Figure . The voltage level of the references and therefor the DAC voltage swing is selectable by means of a bit in the (REFTRM) register. This allows the optimization of voltage swings for 5 Volt and 3.3 Volt supply levels. Two 3 bit DACs are also accessible through that register to allow for factory tests.

The (REFTRM) register also contains two bits that can Enable / Disable the Center or Bottom Amplifiers that drive the A/D Ladder VADC and VADB respectively. This feature allows the ladder to be connected to ground for signal swings that include ground or allows it to be driven from an external source if desired.

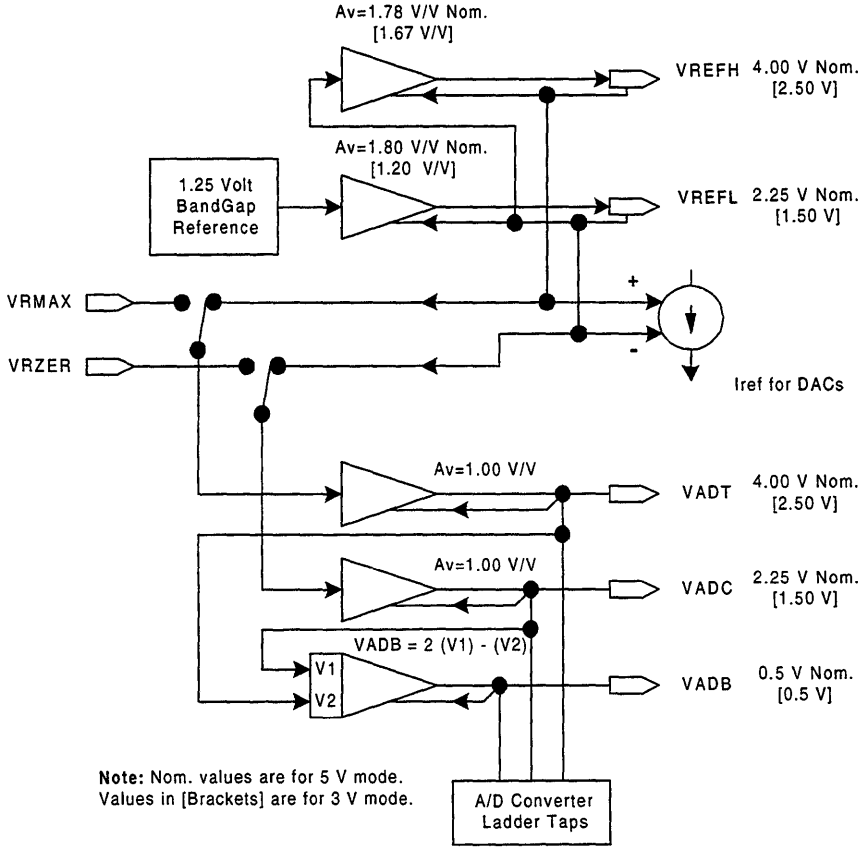

Figure 10-1 Voltage Reference Generation

Table 10-3 VREFL Trimming Register (REFTRM)

Bit(s)	rw	Reset	Description/Function
15:09	r	00h	Reserved (read as zeros)
08	rw	1	VADC Ladder Buffer Enable. When this bit is set the Buffer Amplifier driving VADC is enabled.
07	rw	1	VADB Ladder Buffer Enable. When this bit is set the Buffer Amplifier driving VADB is enabled.
06	rw	0	REFLVL. Voltage Reference Levels selection. 0 for 5 Volt systems 1 for 3 Volt (3.3V nom.) systems (see performance specifications section for levels) Note: REFLVL = 1 is for VDD = 3.3 V nom. and should not be used for extended periods of time at VDD = 5.0 V nom.
05:03	rw	100	PTAT[0:2]. Band Gap Adjustment DAC bits. For Factory Tests.
02:00	rw	100	REFG[0:2]. Reference Gain Control DAC bits. For Factory Tests.

11.1 Absolute Maximum Ratings

Table 11-1 Absolute Maximum Ratings

Parameter	Conditions	Min	Nom	Max	Units
Supply Voltage	VDD-VSS no damage full function	-0.3		6.0 5.5	V
Input Voltage		VSS -0.5		VDD +0.5	V
Storage Temperature		-65		150	deg C
Lead Temperature	10 seconds			300	deg C

11.2 Recommended Operating Conditions

Table 11-2 Recommended Operating Conditions

Parameter	Conditions	Min	Nom	Max	Units
Supply Voltage	VDD-VSS	3.0		5.5	V
Ambient Temperature		0	25	70	deg C
Clock In or Xtal Frequency	VDD = 4.5 - 5.5V VDD = 3.0 - 3.6 V			50 30	MHz
Ext. Clock In Duty Cycle		40		60	%
Ext. Clock In Rise Time and Fall Time				5.0	ns
XTAL Vibrational Mode	Fundamental or Third Overtone (1)		-		-
XTAL Series (or Motional) Resistance	(1)			40.0	Ohms
XTAL Shunt Capacitance	(1)			8.0	pF

Table 11-2 Recommended Operating Conditions (Continued)

Parameter	Conditions	Min	Nom	Max	Units
XTAL Circuit Total Shunt Capacitance	Includes XTAL Shunt Capacitance and PCB Capacitance. (1)			12.0	pF
XTAL Quality Factor Q	(1)	15,000			-
XTAL Drive Level	(1) VDD = 5.0 V		500		uW
Reset Pulse Width External Clock	Power remains on.	12			SYS CLKs
Reset Pulse Width Internal Oscillator supplying SYSCLK	From the time VDD_D reaches 90% of nominal during power up.	30.0			ms

NOTES:

(1) XTAL characteristics listed here assume that the external component values used in the oscillator are those listed in the CLOCK GENERATOR section of this specification. Other combinations may be valid (see the DSP PERIPHERALS chapter).

12.1 General

Table 12-1 General Performance Specifications

Parameter	Conditions	Min	Nom	Max	Units
Supply Current (see Power Control)	VDD = 5.0 V SYSCLK = 50 MHz All Systems On All Sleep VDD = 3.3 V SYSCLK = 30 MHz All Systems On All Sleep			 TBD TBD TBD TBD	 ma ua ma ua
Master Oscillator XTAL Frequency Range (Generates SYSCLK)	VDD = 5.0 V VDD = 3.3 V	10 TBD		50 TBD	MHz
Master Oscillator Output Duty Cycle (SYSCLK)	VDD = 5.0 V VDD = 3.3 V	40 TBD		60 TBD	%
System Clock (SYSCLK) Frequency Range	VDD = 5.0 V VDD = 3.3 V			50.0 TBD	MHz
VREFL Tolerance (5 V System)	VDD=5.0V Iout = +/-500 ua REFLVL = 0 Ta = 25 deg. C	2.183	2.250	2.408	V (1)
VREFH Gain Tolerance (5 V System)	VDD=5.0V Iout = +/- 500 ua REFLVL = 0 Ta = 25 deg. C For VREFL=2.25V VREFH=4.00 Nom	1.742X	1.778X	1.813X	VREFL

Table 12-1 General Performance Specifications

Parameter	Conditions	Min	Nom	Max	Units
VREFL Tolerance (3 V System)	VDD=3.3V Iout = +/-275 ua REFLVL = 1 Ta = 25 deg. C	1.425	1.500	1.575	V
VREFH Gain Tolerance (3 V System)	VDD=3.3V Iout = +/-275 ua REFLVL = 1 Ta = 25 deg. C For VREFL=1.50V VREFH=2.50 Nom	1.633X	1.667X	1.700X	VREFL
VREFL Voltage TC	VDD = 5.0 V, 3.3 V Tref = 25 deg. C			+/-250.0	ppm/ deg. C
VREFL, VREFH Output Drive Capability.	VDD = 5.0 V REFLVL = 0 VDD = 3.3 V REFLVL = 1 Ta = 25 deg. C External Load Current should be static during conversions.	+/-500.0 +/-275.0			uA
VREFL PSRR	VDD = 100 mV p-p f = 10 Hz (5 V System) (3 V System)		 20.0 30.0		dB

NOTES:

(1) Bits 0:5 of the REFTRM register may be written to center the +/-5% tolerance band around the nominal value; i.e., @E03Dh = 0194h.

12.2 Digital I/O Characteristics

Table 12-2 Digital I/O Performance Specifications

Parameter	Conditions	Min	Nom	Max	Units
High Level Input Voltage - V_{ih}	VDD=3.0 - 5.5V	2.0			V
Low Level Input Voltage - V_{il}	VDD=3.0 - 5.5V			0.8	V
High Level Output Voltage 1 - V_{oh1}	VDD=3.0 - 5.5V IOH=-4.0 mA IOH=-100 uA	 2.4 VDD-.5			 V V
Low Level Output Voltage 1 - V_{ol1}	VDD=3.0 - 5.5V IOL=4.0 mA			0.5	V
High Level Output Voltage 2 - V_{oh2} (CA,CD, CWR, CRD, SYSCLK, EXTCLK)	VDD=3.0 - 5.5V IOH=-8.0 mA IOH=-100 uA	 2.4 VDD-.5			 V V
Low Level Output Voltage 2 - V_{ol2} (CA, CD, CWR, CRD, SYSCLK, EXTCLK)	VDD=3.0 - 5.5V IOL=8.0 mA			0.5	V
Input Leakage Current	VSS<VIN<VDD			+/-10	uA
Input Pullup Current	All GPIO and Inputs except: OSCI, ...TBD Vin = 2.4 V	TBD		TBD	uA
Input Capacitance	Ftest=1.0MHz			10	pF
Output Rise Time	Load = 20pF			5	ns
Output Fall Time	Load = 20pF			5	ns

12.3 Analog Data Acquisition (5 Volt)

Table 12-3 Analog Data Acquisition Performance Specifications (5 Volt) (1)

Parameter	Conditions	Min	Nom	Max	Units
A/D Converter:					
Resolution		1024 10		1024 10	Levels Bits
Digital Format					2's Comp.
Conversion Time Including Mux. Pipeline Mode.	SYSCLK=48 Mhz Divide=24 (*2) ACLK1=1 MHz 8 Channels: Per. Channel:			9.0 1.1	us us
Conversion Time Including Mux. Single Channel Mode.	SYSCLK=48 Mhz Divide=24 (*2) ACLK1= 1 MHz 1 Channel:			2.0	us
Differential Nonlinearity (case 1)	VRMAX-VRZER= 1.75 V	-1.0		+1.0	LSB (2)
Differential Nonlinearity (case 2)	VRMAX-VRZER= 0.5 V	-3.0		+3.0	LSB (2)
Integral Nonlinearity (case 1)	VRMAX-VRZER= 1.75 V	-4.0		+4.0	LSB (3)
Integral Nonlinearity (case 2)	VRMAX-VRZER= 0.5V	-6.0		+6.0	LSB (3)
Zero Reference Range (VRZER)	For Specified Performance.	1.75		2.75	V
Max Reference Range (VRMAX)	For Specified Performance.	VRZER+0.5		VDDQ - 0.5	V
Reference Inputs DC Leakage Current	Within Their Ranges Ta = 25 deg. C	-500		+500	nA
Reference Buffers Offset Voltage	VADC-VREFL VADC-VRZER VADT-VREFH VADT-VRMAX	-25.0 -30.0		+25.0 +30.0	mV mV

Table 12-3 Analog Data Acquisition Performance Specifications (5 Volt) (1)

Parameter	Conditions	Min	Nom	Max	Units
VADB Buffer Gain Tolerance	100*[((VADC-VADB)/(VADT-VADC))-1]	+2.5		-2.5	%
Reference Inputs Capacitance				15	pF
Input Multiplexer/ Buffer Amps:					
Input Voltage Range (w/ o buffers)	VADT=VDD-0.5V VADB=VSS+0.5V	VSSQ + 0.5		VDDQ - 0.5	V
Input Voltage Range (w buffers)		VSSQ		VDDQ - 1.5	V
Zero-Scale Error (w/o buffers)	bipolar zero code Relative to VADC.	-15.0		+15.0	mV
Zero-Scale Drift (w/o buffers)			+/-75.0		uV/ deg C
Gain Error	with or w/o buffers	-5.0		+5.0	%FS
Channel to Channel Matching Error (w buffers)	Vladder = 3.5V			6	LSB
Channel to Channel Matching Error (w/o buffers)	Vladder = 3.5V			4	LSB
Buffer Voltage Shift		+0.75		+1.15	V
Small Signal Bandwidth	From input pin to ADC T+H. (Information only. Not tested.)		3.0		MHz
Input Bias Current	with or w/o buffers (see Figure 12-1) Ta = 25 deg. C	-500		+500	nA
Input Capacitance (w/o buffers)	switched mux. and sampling cap. (see Figure 12-1)		15		pF
Input Capacitance (w buffers)	static cap. (see Figure 12-1)		9		pF
CH5 Amplifier:					
Input Offset Voltage		-20.0		+20.0	mV
Input Bias Current	Ta = 25 deg. C	-500		+500	nA

Table 12-3 Analog Data Acquisition Performance Specifications (5 Volt) (1)

Parameter	Conditions	Min	Nom	Max	Units
Input Offset Current	Ta = 25 deg. C	-100		+100	nA
Input Common Mode Range		VSSQ +0.5		VDDQ -1.5	V min.
Open Loop Voltage Gain	No Load	80			dB
Gain Bandwidth Product	Ftest=100KHz No Load	3.0	9.0		MHZ
Output Impedance	Ftest=10KHz to 10MHz Ftest=1Hz		300 22.0		Ohms KOhms
Slew Rate	AV=+1, -1 RL=10K CL=20pF		5.0		V/us
Output Voltage Swing	RL=10K to Opposite Supply	VSSQ +1.0		VDDQ -1.0	V min.
Output Drive Capability	Ta = 25 deg. C	+/-500			uA

NOTES:

(1) Unless specified, values are at Ta= 0 to 70 deg. C and VDDQ = 5.0 V +/- 10%.
(2) Guaranteed Monotonic.
(3) Code Transition Deviation from Best Fit Straight Line.

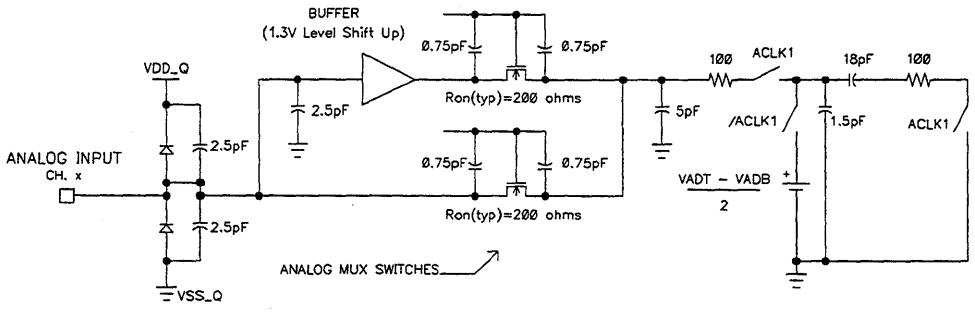

Figure 12-1 Analog Input Equivalent Circuit

12.4 Analog Data Acquisition (3 Volt)

Table 12-4 Analog Data Acquisition Performance Specification (3 Volt) (1)

Parameter	Conditions	Min	Nom	Max	Units
A/D Converter:					
Resolution		1024 10		1024 10	Levels Bits
Digital Format					2's Comp.
Conversion Time Including Mux. Pipeline Mode.	SYSCLK=30 Mhz Divide=15 (*2) ACLK1=1 MHz 8 Channels: Per. Channel:			9.0 1.1	us us
Conversion Time Including Mux. Single Channel Mode.	SYSCLK=30 Mhz Divide=15(*2) ACLK1=1 MHz 1 Channel			2.0	us
Differential Nonlinearity (case 1)	VRMAX-VRZER= 1.00V	-1.0		+1.0	LSB (2)
Differential Nonlinearity (case 2)	VRMAX-VRZER= 0.5 V	-3.0		+3.0	LSB (2)
Integral Nonlinearity (case 1)	VRMAX-VRZER= 1.00 V	-3.0		+3.0	LSB (3)
Integral Nonlinearity (case 2)	VRMAX-VRZER= 0.5V	-5.0		+5.0	LSB (3)
Zero Reference Range (VRZER)	For Specified Performance.	1.25		1.75	V
Max Reference Range (VRMAX)	For Specified Performance.	VRZER+0.5		VDDQ -0.5	V
Reference Inputs DC Leakage Current	Within Their Ranges Ta = 25 deg. C	-500		+500	nA
Reference Buffers Offset Voltage	VADC-VREFL VADC-VRZER VADT-VREFH VADT-VRMAX	-25.0 -30.0		+25.0 +30.0	mV mV

Table 12-4 Analog Data Acquisition Performance Specification (3 Volt) (1)

Parameter	Conditions	Min	Nom	Max	Units
VADB Buffer Gain Tolerance	100*[((VADC-VADB)/(VADT-VADC))-1]	+3.5		-3.5	%
Reference Inputs Capacitance				15	pF
Input Multiplexer/ Buffer Amps:					
Input Voltage Range (w/ o buffers)	VADT=VDD-0.5V VADB=VSS+0.5V	VSSQ +0.5		VDDQ -0.5	V
Input Voltage Range (w buffers)		VSSQ		VDDQ -1.5	V
Zero-Scale Error (w/o buffers)	bipolar zero code Relative to VADC.	-10.0		+10.0	mV
Zero-Scale Drift (w/o buffers)			+/-75.0		uV/ deg C
Gain Error	w/o buffers	-5.0		+5.0	%FS
Channel to Channel Matching Error (w buffers)	Vladder = 2.0V			10	LSB
Channel to Channel Matching Error (w/o buffers)	Vladder = 2.0V			4	LSB
Buffer Voltage Shift		+0.75		+1.15	V
Small Signal Bandwidth	From input pin to ADC T+H. (Information only. Not tested.)		2.5		MHz
Input Bias Current	with or w/o buffers (see Figure 12-1) Ta = 25 deg. C	-500		+500	nA
Input Capacitance (w/o buffers)	switched mux. and sampling cap. (see Figure 12-1)		15		pF
Input Capacitance (w buffers)	static cap. (see Figure 12-1)		9		pF
CH5 Amplifier:					
Input Offset Voltage		-18.0		+18.0	mV

Table 12-4 Analog Data Acquisition Performance Specification (3 Volt) (1)

Parameter	Conditions	Min	Nom	Max	Units
Input Bias Current	Ta = 25 deg. C	-500		+500	nA
Input Offset Current	Ta = 25 deg. C	-100		+100	nA
Input Common Mode Range		VSSQ+0.5		VDDQ-1.5	V min.
Open Loop Voltage Gain	No Load	60			dB
Gain Bandwidth Product	Ftest=100KHz No Load	1.5	3.0		MHZ
Output Impedance	Ftest=10KHz to 10MHz Ftest=1Hz		300 22.0		Ohms KOhms
Slew Rate	AV=+1, -1 RL=10K CL=20pF		3.0		V/us
Output Voltage Swing	RL=10K to Opposite Supply	VSSQ+0.75		VDDQ-0.75	V min.
Output Drive Capability	Ta = 25 deg. C	+/-275			uA

NOTES:

(1) Unless specified, values are at Ta= 0 to 70 deg. C and VDDQ = 3.3 V +/- 300 mV.
(2) Guaranteed Monotonic.
(3) Code Transition Deviation from Best Fit Straight Line.

Table 12-5 ACLKn Timing Requirements

Name	Fig.	Description	Min.	Max.	Units
Tclpw	12-2	ACLK1 high (sample) pulse width. [adjustable]	500		ns
Tclc2	12-2	ACLK1 falling to ACLK2 rising. [fixed internally]	0		ns
Tc2pw	12-2	ACLK2 high (coarse compare) pulse width. [adjustable]	175		ns
Tc2c3	12-2	ACLK2 falling to ACLK3 rising. [fixed internally]	0		ns

Table 12-5 ACLKn Timing Requirements

Name	Fig.	Description	Min.	Max.	Units
Tc3pw	12-2	ACLK3 high (fine compare) pulse width. [adjustable]	200		ns
Tc3cl	12-2	ACLK3 falling to ACLK1 rising. [function of adjustments]	50		ns
Tdv	12-2	ACLK1 rising to data valid. [fixed internally]	25		ns
Tmsu	12-2	Mux set-up time. [fixed internally]	500		ns
Tmh	12-2	Mux hold time. [fixed internally]	50		ns

(see CLCFG2 register for adjustment proceedure)

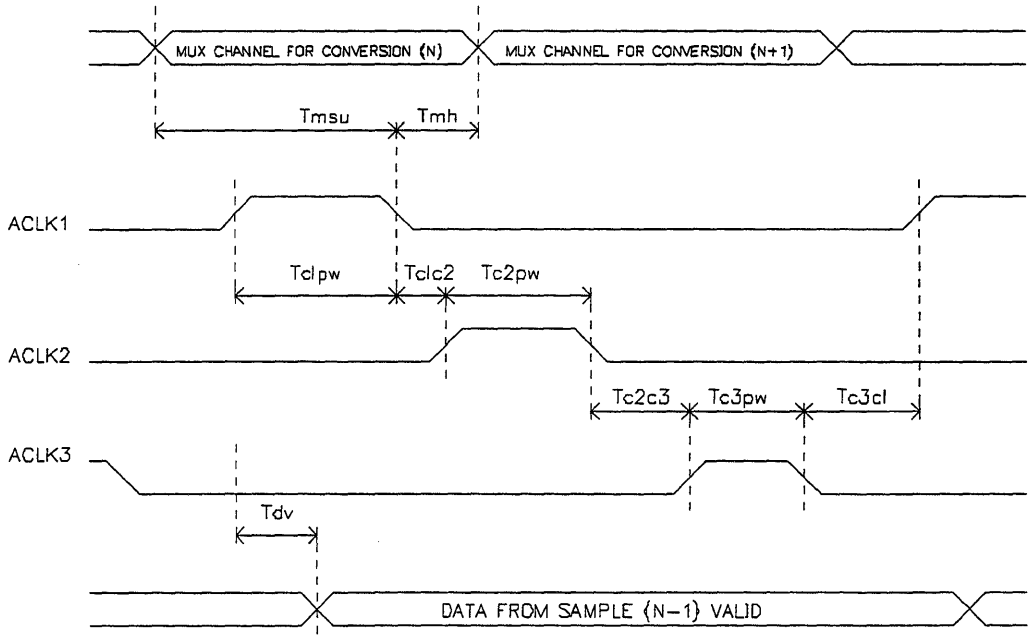

Figure 12-2 ACLKn Timing Requirements

12.5 Shock Sensor Input

Table 12-6 Shock Sensor Input (1)

Parameter	Conditions	Min	Nom	Max	Units
Shock Sensor Input:					
Window Comparator Thresholds (Vth)	AC coupled input (see Figure 12-4)		+/- 50		mV
Window Threshold Tolerance	VDD=5.0V+/- 10% VDD=3.3V+/-0.3V	-20 -15		+20 +15	%
Detection Pulse Width	vin = +/-(1.1* Vth) SHCLK = 1 MHz (Analog Mode)	10			us
Noise Rejection Pulse Width (2)	vin = +/-(1.1* Vth) SHCLK = 1 MHz Pulse Rep. Rate < SHCLK/2 (Analog Mode)			1	us
Write Gate Disable Time	(Digital Mode)			100	ns
Input Bias Current	(see Figure 12-3) Ta = 25 deg. C Vin = VREFL	-500		+500	nA
R(dc) Value (Suggested)	(see Figure 12-4) see bias current			20.0	KOhm
C(ac) Value (Suggested)	(see Figure 12-4)	0.01			uF
R(out) Value (Suggested)	(see Figure 12-4)			40	KOhm

NOTES:

(1) Unless specified, values are at Ta= 0 to 70 deg. C and VDDQ = 5.0 V +/- 10% (REFLVL=0) or 3.3V +/- 300mV (REFLVL=1).

(2) Pulses breaking the Window threshold with a Pulse Width narrower than this will be rejected.

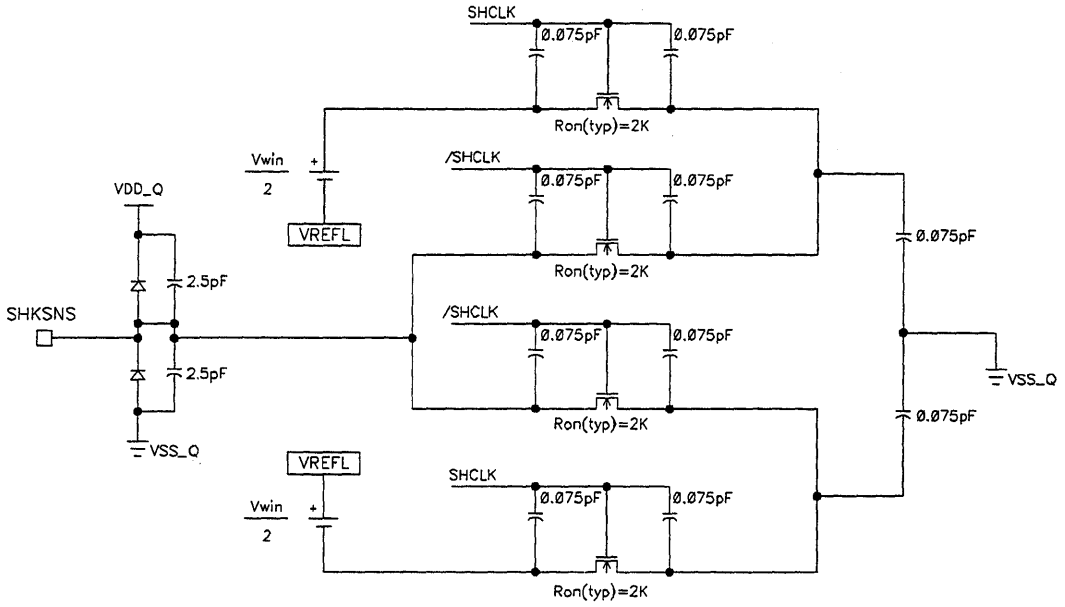

Figure 12-3 SHKSNS Pin Input Equivalent Circuit

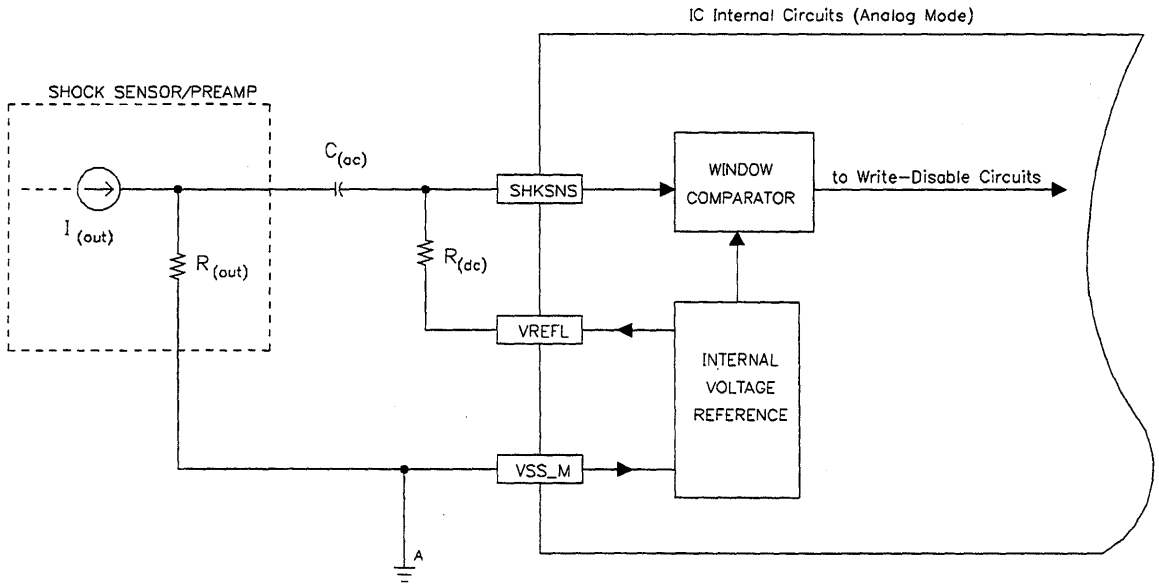

Figure 12-4 Analog Shock Sensor Input Connections

12.6 VCM DAC (5 Volt)

Table 12-7 VCM DAC Analog Performance Specifications (5 Volt) (1)

Parameter	Conditions	Min	Nom	Max	Units
Resolution			12		Bits
Nominal Output Voltage Range	Vout<(VDDA-1.0) RL=20K to VREFL	0.5		4.0	V
Differential Nonlinearity	Codes 0 to 2047 and -1 to -2048 Codes -1 to 0	- 1 -1		+ 1 +5	LSB (2)
Integral Nonlinearity		- 8		+ 8	LSB (3)
Bipolar Offset	Ref. to VREFL Ta=25 deg. C	- 25		+ 25	mV
Bipolar Zero Drift	Ref. to VREFL	-75		+75	uV/ deg. C
Full Scale Gain Error	Offset-corrected Gain Error Ref. to [VREFL +/- (VREFH-VREFL)] Ta=25 deg. C	-5.0		+5.0	%FS
Full Scale Gain Drift	Ref. to [VREFL +/- (VREFH-VREFL)]	-200		+200	ppm/ deg. C
Settling Time (case 1)	to +/- 1 LSB, <256 LSB step, RL=20K, CL=50pF to VREFL to 99% of F.V.		 0.5	2.0	us
Settling Time (case 2)	to +/- 1 LSB, Full span step, RL=20K, CL=50pF to VREFL to 99% of F.V.		 2.0	8.0	us
Input Coding					2's Comp.
Output Impedance	Vout<(VDDA-1.0) f = 10Hz to 1 MHz			100	Ohms
Drive Capability	Ta = 25 deg. C	-500		+500	uA
PSRR	DAC at Mid-Scale f = 10 Hz		20.0		dB

NOTES:

(1) Unless specified, values are at Ta= 0 to 70 deg. C and VDDA = 5.0 V +/- 10%.
(2) Guaranteed Monotonic.
(3) Code Transition Deviation from Best Fit Straight Line.

12.7 VCM DAC (3 Volt)

Table 12-8 VCM DAC Analog Performance Specifications (3 Volt) (1)

Parameter	Conditions	Min	Nom	Max	Units
Resolution			12		Bits
Nominal Output Voltage Range	Vout<(VDDA-1.0) RL=20K to VREFL	0.5		2.5	V
Differential Nonlinearity	Codes 0 to 2047 and -1 to -2048 Codes -1 to 0	- 1 -1		+ 1 +5	LSB (2)
Integral Nonlinearity		- 12		+ 12	LSB (3)
Bipolar Offset	Ref. to VREFL Ta=25 deg. C	- 25		+ 25	mV
Bipolar Zero Drift	Ref. to VREFL	-75		+75	uV/ deg. C
Full Scale Gain Error	Offset-corrected Gain Error Ref. to [VREFL +/- (VREFH-VREFL)] Ta = 25 deg. C	-6.0		+6.0	%FS
Full Scale Gain Drift	Ref. to [VREFL +/- (VREFH-VREFL)]	-200		+200	ppm/ deg. C
Settling Time (case 1)	to +/- 1 LSB, <256 LSB step, RL=20K, CL=50pF to VREFL to 99% of F.V.		 0.5	2.0	us
Settling Time (case 2)	to +/- 1 LSB, Full span step, RL=20K, CL=50pF to VREFL to 99% of F.V.		 2.0	8.0	us

Table 12-8 VCM DAC Analog Performance Specifications (3 Volt) (1)

Parameter	Conditions	Min	Nom	Max	Units
Input Coding					2's Comp.
Output Impedance	Vout<(VDDA-1.0) f = 10Hz to 1 MHz			100	Ohms
Drive Capability	Ta = 25 deg. C	-275		+275	uA
PSRR	DAC at Mid-Scale VDD = 100 mV p-p f = 10 Hz		30.0		dB

NOTES:

(1) Unless specified, values are at Ta= 0 to 70 deg. C and VDDA =3.3 V +/- 300 mV.
(2) Guaranteed Monotonic.
(3) Code Transition Deviation from Best Fit Straight Line.

12.8 Spindle DAC (5 Volt)

Table 12-9 Spindle DAC Analog Performance Specifications (5 Volt) (1)

Parameter	Conditions	Min	Nom	Max	Units
Resolution			8		Bits
Nominal Output Voltage Range	RL= 5K to VSS_A codes 0 to7 below Vout min.	0.1		3.5	V
Differential Nonlinearity	codes 8 to 255	- 1		+ 1	LSB (2)
Integral Nonlinearity	codes 8 to 255	- 2		+ 2	LSB (3)
Full Scale Gain Error	Offset-corrected Gain Error Ref. to 2*(VREFH-VREFL) Ta = 25 deg. C	-10.0		+10.0	%FS
Full Scale Gain Drift	Ref. to 2*(VREFH-VREFL)	-250		+250	ppm/ deg. C
Settling Time	to +/- 1 LSB, codes 8 to 255, RL=20K, RL=50pF to VSSA to 99% of F.V.		 1.0	10.0	us
Input Coding					Binary
Output Impedance	f = 10 Hz to 1 MHz			100	Ohms
Drive Capability	Ta = 25 deg. C	+/- 500			uA
PSRR	DAC at Full-Scale VDD = 100 mV p-p f = 10 Hz		20.0		dB

NOTES:

(1) Unless specified, values are at Ta= 0 to 70 deg. C and VDDA = 5.0 V +/- 10%.
(2) Guaranteed Monotonic.
(3) Code Transition Deviation from Best Fit Straight Line.

12.9 Spindle DAC (3 Volt)

Table 12-10 Spindle DAC Analog Performance Specifications (3 Volt) (1)

Parameter	Conditions	Min	Nom	Max	Units
Resolution			8		Bits
Nominal Output Voltage Range	RL= 5K to VSS_A codes 0 to 13 below Vout min.	0.1		2.0	V
Differential Nonlinearity	codes 14 to 255	- 1		+ 1	LSB (2)
Integral Nonlinearity	codes 14 to 255	- 3		+ 3	LSB (3)
Full Scale Gain Error	Offset-corrected Gain Error Ref. to 2*(VREFH-VREFL) Ta = 25 deg. C	-11.0		+11.0	%FS
Full Scale Gain Drift	Ref. to 2*(VREFH-VREFL)	-250		+250	ppm/ deg. C
Settling Time	to +/- 1 LSB, codes 14 to 255, RL=20K, CL=50pF to VSSA to 99% of F.V.		 1.0	10.0	us
Input Coding					Binary
Output Impedance	f = 10 Hz to 1 MHz			100	Ohms
Drive Capability	Ta = 25 deg. C	+/- 275			uA
PSRR	DAC at Full-Scale VDD = 100 mV p-p f = 10 Hz		30.0		dB

NOTES:

(1) Unless specified, values are at Ta= 0 to 70 deg. C and VDDA = 3.3 V +/- 300mV.
(2) Guaranteed Monotonic.
(3) Code Transition Deviation from Best Fit Straight Line.

12.10 Servo Decoder/Sequencer

Table 12-11 Servo Decoder/Sequencer Performance Specifications

Parameter	Conditions	Min	Nom	Max	Units
Servo Clock (SVOCLK) Input Frequency Range	VDD=5.0V VDD=3.3V			50.0 TBD	MHz
Servo Clock (SVOCLK) Input Duty Cycle	VDD=5.0V	40		60	%
RDP Minimum Pulsewidth Reqd.	VDD=5.0V	10			ns
POL to RDP Setup Time	VDD=5.0V	1			ns
POL to RDP Hold Time	VDD=5.0V	1			ns
DBIT, CCLK bit cell width		1		16	SYS CLK periods
Burst Sequencer State Time		1		1023	DCLK periods

12.11 Host Interface

.In all the following timing specifications, T is the System Clock (SYSCLK) period.

Table 12-12 Host Interface Timing Specifications

Name	Fig.	Description	Min.	Max.	Units
tsclkp	12-5	SCLK period	2T		ns
tsclkh		SCLK high time	T - 5		ns
tsclkl		SCLK low time	T - 5		ns
tsclkr		SCLK rise time, load = 20pF		5	ns
tsclkf		SCLK fall time, load = 20pF		5	ns
tsdenh	12-5	SDEN hold time	T - 5		ns
tsdatv	12-5	SDATA valid time		20	ns
tsdati	12-5	SDATA invalid time		0	ns
tsdats	12-5	SDATA setup time	5		ns

Table 12-12 Host Interface Timing Specifications

Name	Fig.	Description	Min.	Max.	Units
tsdath	12-5	SDATA hold time	5		ns
tsdatf	12-5	SDATA floating time		T	ns
tsdatnf	12-5	SDATA driven time	0	10	ns
tsdatfr	12-5	SDATA floating time (response)		T - 5	ns
tsdatnfr	12-5	SDATA driven time (response)	T/2 - 5	10	ns
tsdenrc	32	SDEN Recovery Time	4T		ns

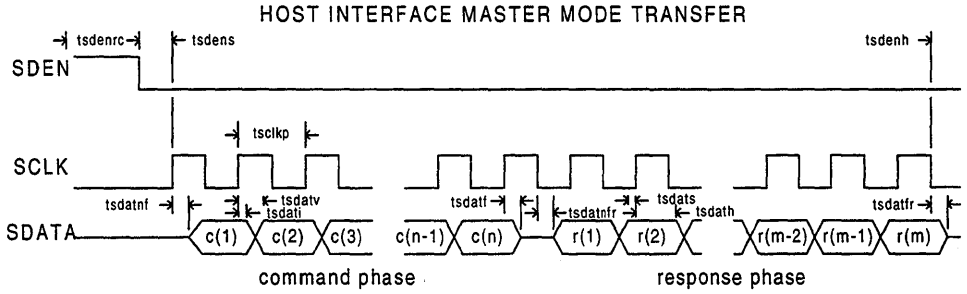

Figure 12-5 Synchronous Serial Port Timing Specifications (see Table 12-12)

12.12 External Memory Interface

In all the following timing specifications, T is the System Clock (SYSCLK) period.

Table 12-13 External Memory Interface Timing Specifications

Name	Fig.	Description	Min.	Max.	Units
Tcav	12-6, 12-7	Common Address Valid		18	ns
Tcah	12-6, 12-7	Common Address Hold	0		ns
Trdv	12-6	Common Read Valid	T	T + 5	ns
Trdh	12-6	Common Read Hold	0	8	ns
Twrv	12-7	Common Write Valid		T + 5	ns
Twrh	12-7	Common Write Hold	0	T + 5	ns
Tcsv	12-6, 12-7	Chip Select Valid		15	ns
Tcsh	12-6, 12-7	Chip Select Hold	0		ns
Tcdf	12-6, 12-7	Common Data Floating	0	4	ns
Tcdnf	12-7	Common Data Not Floating	T - 1	T + 3	ns
Tscd	12-6	Common Data Setup	20		ns
Thcd	12-6	Common Data Hold	0		ns
Tcdv	12-7	Common Data Valid		T + 17	ns
Tcdi	12-7	Common Data Invalid	0		ns

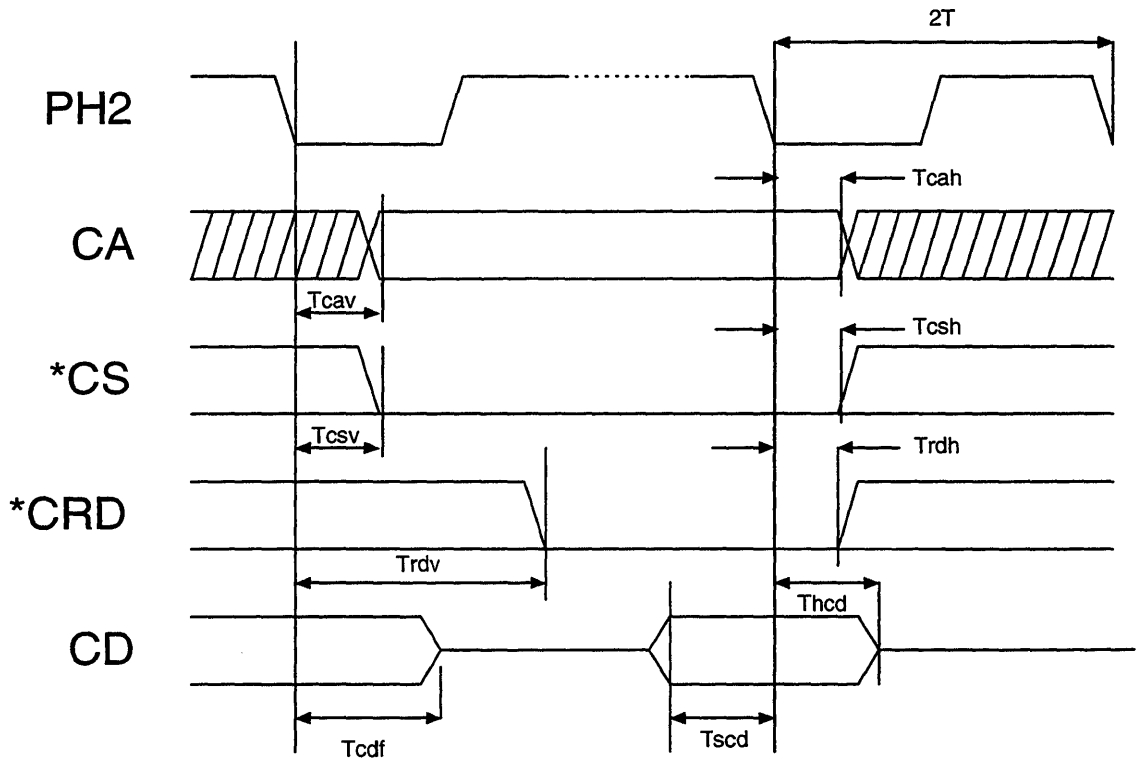

Figure 12-6 External Memory Read (see Table 12-13)

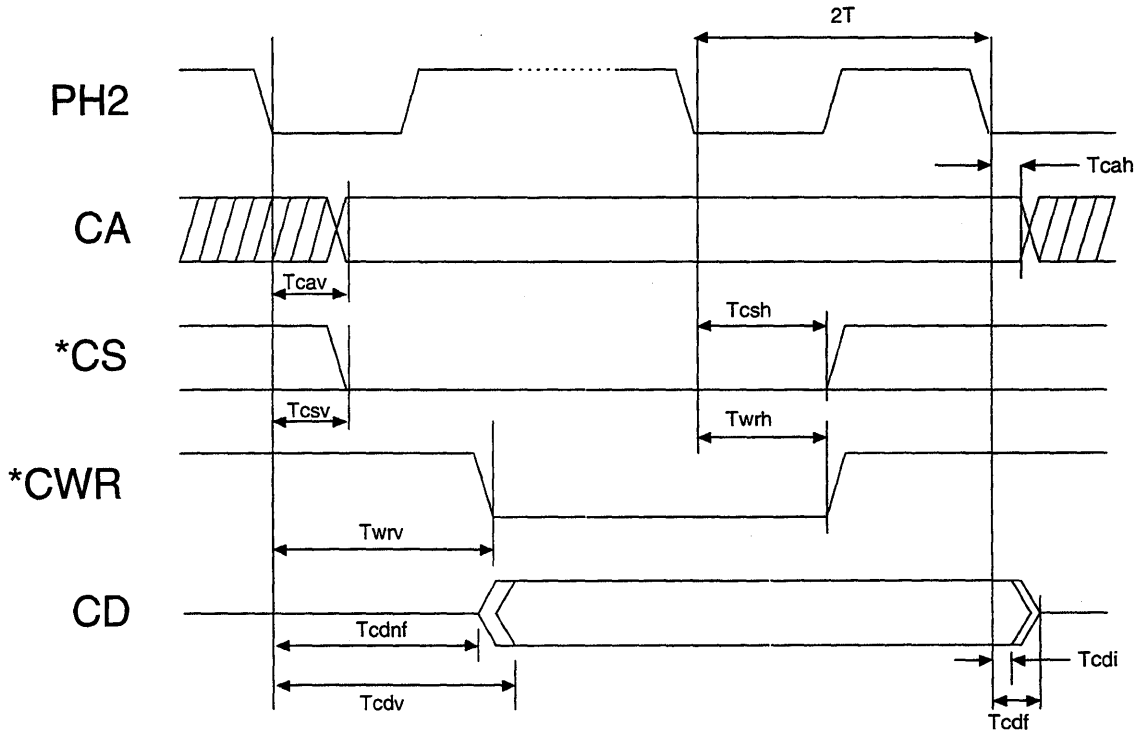

Figure 12-7 External Memory Write (see Table 12-13)

Table 12-14 Diagnostic Data Out Timing Specifications

Name	Fig.	Description	Min.	Max.	Units
Tddov	12-8	Diag. Data Out Valid		10	ns
Tddoh	12-8	Diag Data Out Hold	0		ns

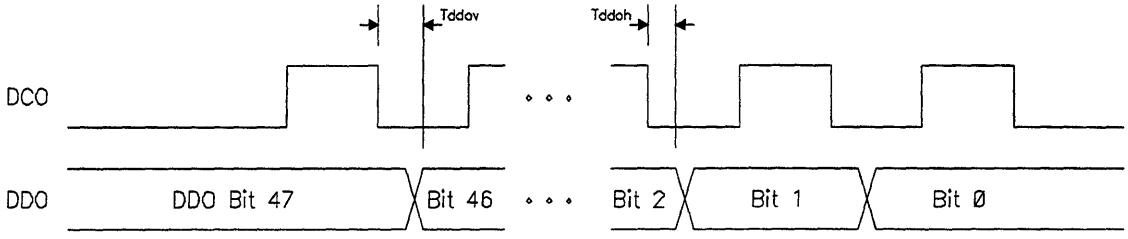

Figure 12-8 Diagnostic Data Out Timing (see Table 12-14)

12.13 DSP System

Table 12-15 DSP System Timing Specifications

Name	Fig.	Description	Min.	Max.	Units
Tuipw		User Input Pulse Width	2T + 10		ns
Tintpw		External Interrupt/Shock Pulse Width	10		ns

12.14 Clock Out

Table 12-16 Clock Out Timing Specifications

Name	Fig.	Description	Min.	Max.	Units
Tclkor		Clk Out Rise Time, 50pF Load	5		ns
Tclkof		Clk Out Fall Time, 50pF Load	5		ns
Duty		Clk Out Duty Cycle	40	60	%

12.15 Power Control (5 Volt)

Table 12-17 Power Control Specifications by Functional Block (5 Volt) (1)

Functional Block	Conditions	Power Dissipation (mW)	Recovery Time
XPCLK		TBD	TBD
SYSCLK pin		TBD	TBD
Master Oscillator		TBD	TBD
DSP		TBD	12 SYSCLKs
RS232		TBD	2 SYSCLKs
Sequencer		TBD	2 SYSCLKs
A/D Ladder.	R_{LAD} = 700 Ohm, $V_{LAD}=V_{ADT}-V_{ADB}$ = 3.5V, $I_{LAD}=V_{LAD}/R_{LAD}$ PD = I_{LAD}*VDD_Q No Load	24 (Analog Supply)	20 us
A/D Converter and Acquisition logic.		21 (Analog Supply)	5 us
VCMDAC/ Shock Sensor Ckt. (note: SPNDAC must be on to use VCMDAC)	No Load	17 (Analog Supply)	200 us (@99%of FV in 10 us)
SPNDAC, DAC Bias, and spindle control	No Load	13 (Analog Supply)	100 ms (@99%of FV in 1 ms)
A/D MUX and CH5 AMP	No Load	12 (Analog Supply)	100 ms (@99%of FV in 1 ms)
Voltage References, Reference Buffers, Ladder Buffers, and rest of circuitry	No Load	53 (Analog Supply)	500 ms (@99%of FV in 10 ms)

NOTE: VDD_x = 5.0V, SYSCLK =50 MHz, Ta = 25 deg.C.

12.16 Power Control (3 Volt)

Table 12-18 Power Control Specifications by Functional Block (3 Volt) (1)

Functional Block	Conditions	Power Dissipation (mW)	Recovery Time
XPCLK		TBD	TBD
SYSCLK pin		TBD	TBD
Master Oscillator		TBD	TBD
DSP		TBD	12 SYSCLKs
RS232		TBD	2 SYSCLKs
Sequencer		TBD	2 SYSCLKs
A/D Ladder.	R_{LAD} = 700 Ohm, $V_{LAD}=V_{ADT}-V_{ADB}$ = 2.0 V, $I_{LAD}=V_{LAD}/R_{LAD}$ PD = I_{LAD}*VDD_Q No Load	10 (Analog Supply)	20 us
A/D Converter and Acquisition logic.		15 (Analog Supply)	5 us
VCMDAC/ Shock Sensor Ckt. (note: SPNDAC must be on to use VCMDAC)	No Load	5 (Analog Supply)	200 us (@99%of FV in 10 us)
SPNDAC, DAC Bias, and spindle control	No Load	6 (Analog Supply)	100 ms (@99%of FV in 1 ms)
A/D MUX and CH5 AMP	No Load	5 (Analog Supply)	100 ms (@99%of FV in 1 ms)
Voltage References, Reference Buffers, Ladder Buffers, and rest of circuitry	No Load	19 (Analog Supply)	500ms (@99%of FV in 10 ms)

NOTE: VDD_x = 3.3V, SYSCLK =30 MHz, Ta = 25 deg.C.

13.1 I/O Register Summary

13.1.1 Analog Data Acquisition Registers

Acquisition Command (ADCCMD)	Acquisition Status (ADCSTA)	Data Storage M0-M1 (ADCCH6, ADCCH7)	Data Storage (ADCCH0-ADCCH5)
E000h (R/W)	**E001h (RO)**	**E002h – E003h (R/W)**	**ext0 – ext5 (R/W)**
15 – External Max VREF select	15 – Reserved (R/W)	15 – Sign Extension	15 – Sign Extension
14 – External Zero-volt Ref select	14 – ADC Borrow bit	14 – Sign Extension	14 – Sign Extension
13 – Channel 7 select – Bit 1	13 – ADC Carry bit	13 – Sign Extension	13 – Sign Extension
12 – Channel 7 select – Bit 0	12 – CHX (4) Buffer Enable (R/W)	12 – Sign Extension	12 – Sign Extension
11 – Interrupt on Channel – Bit 2	11 – CHD (3) Buffer Enable (R/W)	11 – 2's Comp. value bit 9	11 – 2's Comp. value bit 9
10 – Interrupt on Channel – Bit 1	10 – CHC (2) Buffer Enable (R/W)	10 – 2's Comp. value bit 8	10 – 2's Comp. value bit 8
09 – Interrupt on Channel – Bit 0	09 – CHB (1) Buffer Enable (R/W)	09 – 2's Comp. value bit 7	09 – 2's Comp. value bit 7
08 – Burst sequencer start enable	08 – CHA (0) Buffer Enable (R/W)	08 – 2's Comp. value bit 6	08 – 2's Comp. value bit 6
07 – Single channel interrupt enable	07 – Channel 7 Busy	07 – 2's Comp. value bit 5	07 – 2's Comp. value bit 5
06 – Reserved	06 – Channel 6 Busy	06 – 2's Comp. value bit 4	06 – 2's Comp. value bit 4
05 – Sequencer Enable	05 – Channel 5 Busy	05 – 2's Comp. value bit 3	05 – 2's Comp. value bit 3
04 – Single channel address – bit 2	04 – Channel 4 Busy	04 – 2's Comp. value bit 2	04 – 2's Comp. value bit 2
03 – Single channel address – bit 1	03 – Channel 3 Busy	03 – 2's Comp. value bit 1	03 – 2's Comp. value bit 1
02 – Single channel address – bit 0	02 – Channel 2 Busy	02 – 2's Comp. value bit 0	02 – 2's Comp. value bit 0
01 – Pipeline Mode Start	01 – Channel 1 Busy	01 – Reads 0 after conversion	01 – Reads 0 after conversion
00 – Single Channel Conv Start	00 – Channel 0 Busy	00 – Reads 0 after conversion	00 – Reads 0 after conversion

13.1.2 Programmable Clock Generator Registers

Clock Configuration Reg 1 (CLCFG1)	Clock Configuration Reg 2 (CLCFG2)
E008h (R/W)	**E009h h ((R/W)**
15 – PCLK source 0=SYS, 1=SVO	15 – Reads 0
14 – DCLK source 0=SYS, 1=SVO	14 – Reads 0
13 – Reads 0	13 – Reads 0
12 – External Clock divide Bit 4	12 – Reads 0
11 – External Clock divide Bit 3	11 – SCLK divide – Bit 3
10 – External Clock divide Bit 2	10 – SCLK divide – Bit 2
09 – External Clock divide Bit 1	09 – SCLK divide – Bit 1
08 – External Clock divide Bit 0	08 – SCLK divide – Bit 0
07 – CCLK divide – Bit 3	07 – ACLK2 & 3 width – Bit 2
06 – CCLK divide – Bit 2	06 – ACLK2 & 3 width – Bit 1
05 – CCLK divide – Bit 1	05 – ACLK2 & 3 width – Bit 0
04 – CCLK divide – Bit 0	04 – ACLK1 divide – Bit 4
03 – DCLK divide – Bit 3	03 – ACLK1 divide – Bit 3
02 – DCLK divide – Bit 2	02 – ACLK1 divide – Bit 2
01 – DCLK divide – Bit 1	01 – ACLK1 divide – Bit 1
00 – DCLK divide – Bit 0	00 – ACLK1 divide – Bit 0

13.1.3 Diagnostic Data Out Port Registers

DDOP Register – 0 (DIAGD0)	DDOP Register – 1 (DIAGD1)	DDOP Register – 2 (DIAGD2)	DDOP Control Register (DIAGDC)
E010h (R/W)	**E011h (R/W)**	**E012h (R/W)**	**E013h (WO)**
15 – Data – Bit 15	15 – Data – Bit 15	15 – Data – Bit 15	15 – Data value is Don't Care
14 – Data – Bit 14	14 – Data – Bit 14	14 – Data – Bit 14	14 – Data value is Don't Care
13 – Data – Bit 13	13 – Data – Bit 13	13 – Data – Bit 13	13 – Data value is Don't Care
12 – Data – Bit 12	12 – Data – Bit 12	12 – Data – Bit 12	12 – Data value is Don't Care
11 – Data – Bit 11	11 – Data – Bit 11	11 – Data – Bit 11	11 – Data value is Don't Care
10 – Data – Bit 10	10 – Data – Bit 10	10 – Data – Bit 10	10 – Data value is Don't Care
09 – Data – Bit 09	09 – Data – Bit 09	09 – Data – Bit 09	09 – Data value is Don't Care
08 – Data – Bit 08	08 – Data – Bit 08	08 – Data – Bit 08	08 – Data value is Don't Care
07 – Data – Bit 07	07 – Data – Bit 07	07 – Data – Bit 07	07 – Data value is Don't Care
06 – Data – Bit 06	06 – Data – Bit 06	06 – Data – Bit 06	06 – Data value is Don't Care
05 – Data – Bit 05	05 – Data – Bit 05	05 – Data – Bit 05	05 – Data value is Don't Care
04 – Data – Bit 04	04 – Data – Bit 04	04 – Data – Bit 04	04 – Data value is Don't Care
03 – Data – Bit 03	03 – Data – Bit 03	03 – Data – Bit 03	03 – Data value is Don't Care
02 – Data – Bit 02	02 – Data – Bit 02	02 – Data – Bit 02	02 – Data value is Don't Care
01 – Data – Bit 01	01 – Data – Bit 01	01 – Data – Bit 01	01 – Data value is Don't Care
00 – Data – Bit 00	00 – Data – Bit 00	00 – Data – Bit 00	00 – Data value is Don't Care

13.1.4 Host Interface Port Registers

Host Data 1 (HSTDT1)	Host Data 2 (HSTDT2)	Master Mode Control Register (MSTCTL)	Master Mode Transfer Control Register (MMTCTL)
E019h (R/W)	**E01Ah (R/W)**	**E028h (RW)**	**E029h (WO)**
15 -Host Data 1 Bit 15	15 -Host Data 2 Bit 15	15 – 0=LSB first, 1=MSB first	15 – Reads 0
14 – Host Data 1 Bit 14	14 – Host Data 2 Bit 14	14 – SCLOCK polarity	14 – Reads 0
13 – Host Data 1 Bit 13	13 – Host Data 2 Bit 13	13 – SDEN polarity	13 – Reads 0
12 – Host Data 1 Bit 12	12 – Host Data 2 Bit 12	12 – SDEN disable	12 – Reads 0
11 – Host Data 1 Bit 11	11 – Host Data 2 Bit 11	11 – Read Data Turnaround Mode	11 – Reads 0
10 – Host Data 1 Bit 10	10 – Host Data 2 Bit 10	10 – Peripheral port GPIO enable	10 – Reads 0
09 – Host Data 1 Bit 09	09 – Host Data 2 Bit 09	09 – Peripheral Port Master Enable	09 – Reads 0
08 – Host Data 1 Bit 08	08 – Host Data 2 Bit 08	08 – Command Packet Enable	08 – Reads 0
07 – Host Data 1 Bit 07	07 – Host Data 2 Bit 07	07 – Command Length Bit 03	07 – Reads 0
06 – Host Data 1 Bit 06	06 – Host Data 2 Bit 06	06 – Command Length Bit 02	06 – Reads 0
05 – Host Data 1 Bit 05	05 – Host Data 2 Bit 05	05 – Command Length Bit 01	05 – Reads 0
04 – Host Data 1 Bit 04	04 – Host Data 2 Bit 04	04 – Command Length Bit 00	04 – Reads 0
03 – Host Data 1 Bit 03	03 – Host Data 2 Bit 03	03 – Data Length Bit 03	03 – Reads 0
02 – Host Data 1 Bit 02	02 – Host Data 2 Bit 02	02 – Data Length Bit 02	01 – Reads 0
01 – Host Data 1 Bit 01	01 – Host Data 2 Bit 01	01 – Data Length Bit 01	01 – Reads 0
00 – Host Data 1 Bit 00	00 – Host Data 2 Bit 00	00 – Data Length Bit 00	00 – 0=Master Read, 1=Master Write

13.1.5 Interrupt Control Registers

INTERRUPT MASK (INTMSK)	INTERRUPT PENDING (INTPND)
E030h (R/W)	**E031h (R/W)**
15 – Reads 0	15 – Reads 0
14 – Reads 0	14 – Reads 0
13 – Reads 0	13 – Reads 0
12 – Reads 0	12 – Reads 0
11 – SETPON interrupt	11 – SETPON interrupt
10 – INT0 Burst Sequencer	10 – INT0 Burst Sequencer
09 – INT0 Acquisition Sequencer	09 – INT0 Acquisition Sequencer
08 – INT0 Search Window Open	08 – INT0 Search Window Open
07 – Shock Interrupt	07 -Shock Interrupt
06 – Reads 0	06 – Reads 0
05 – Spin Interrupt	05 – Spin Interrupt
04 – EXINT – External interrupt	04 – EXINT – External interrupt
03 – Peripheral port interrupt	03 – Peripheral port interrupt
02 – Timer 0 count becomes 0000H	02 – Timer 0 count becomes 0000H
01 – RXCMP – RS-232 recv complete	01 – RXCMP – RS-232 recv complete
00 – TXCMP – RS-232 xmit complete	00 – TXCMP – RS-232 xmit complete

13.1.6 Configuration Registers

4420 Configuration (CHPCFG)	Chip Revision (CHPREV)	Memory Configuration (MEMCFG)
E034h (R/W)	**E035h (RO)**	**E036h (R/W)**
15 – 1 = ROM Execute User Code (RO)	15 – Reads 0	15 – Flash Program Window Bit 2
14 – spare jumper (RO)	14 – Reads 0	14 – Flash Program Window Bit 1
13 – spare jumper (RO)	13 – Reads 0	13 – Flash Program Window Bit 0
12 – spare jumper (RO)	12 – Reads 0	12 – Flash Program Upper-byte select
11 – spare jumper (RO)	11 – Reads 0	11 – 0=GPIO[11], 1=APP chip select
10 – spare jumper (RO)	10 – Reads 0	10 – HDC/APP Wait States Bit 1
09 – Negative USRIN enable	09 – Reads 0	09 – HDC/APP Wait States Bit 0
08 – Internal Bus Trace Enable	08 – Reads 0	08 – 0=USROUT, 1=HDC chip select
07 – 0=16-Bit, 1=8-Bit External Bus	07 – Reads 0	07 – Ext ROM Wait States Bit 1
06 – Chip ID bit-1	06 – Reads 0	06 – Ext ROM Wait States Bit 0
05 – Chip ID bit-0	05 – Reads 0	05 – Ext RAM Wait States Bit 1
04 – Shadow Vectors Enable	04 – Reads 0	04 – Ext RAM Wait States Bit 0
03 – Enable DDO, DCO, and TX	03 – Reads 0	03 – Number Ext RAM Banks Bit 1
02 – Reads 0	02 – Reads 0	02 – Number Ext RAM Banks Bit 0
01 – APP chip select active hi enable	01 – Reads 1	01 – 0=ATTNINT, 1=RAMCS
00 – HDC chip select active hi enable	00 – Reads 1	00 – PROM program mode enable

13.1.7 VCM DAC Register

VCM DAC (VCMDAC)
E039h (R/W)
15 -2's Complement value bit 11
14 – 2's Complement value bit 10
13 – 2's Complement value bit 9
12 – 2's Complement value bit 8
11 – 2's Complement value bit 7
10 – 2's Complement value bit 6
09 – 2's Complement value bit 5
08 – 2's Complement value bit 4
07 – 2's Complement value bit 3
06 – 2's Complement value bit 2
05 – 2's Complement value bit 1
04 – 2's Complement value bit 0
03 – Reads 0
02 – Reads 0
01 – Reads 0
00 – Reads 0

13.1.8 Power Control Registers

Power Control (PWRCTL)	VREFL Trimming (REFTRM)
E03Ch (R/W)	**E03Dh (R/W)**
15 – Reserved	15 – Reads 0
14 – Reserved	14 – Reads 0
13 – Reserved	13 – Reads 0
12 – Osc power-down start-up mode	12 – Reads 0
11 – XPCLK enable	11 – Reads 0
10 – SYSCLK pin enable	10 – Reads 0
09 – Master Oscillator enable	09 – Reads 0
08 – RS-232 module clock enable	08 – VADC Ladder Buffer Enable
07 – Sequencer clock enable	07 – VADB Ladder Buffer Enable
06 – A/D & Acquisition enable	06 – REFLVL select: 0=5v, 1=3v
05 – A/D Ladder enable	05 – Band Gap Adjust DAC – bit 2
04 – A/D mux & CH5 amp enable	04 – Band Gap Adjust DAC – bit 1
03 – VCMDAC & shock enable	03 – Band Gap Adjust DAC – bit 0
02 – SPNDAC enable	02 – Ref Gain Control DAC – bit 2
01 – VOLTREF enable	01 – Ref Gain Control DAC – bit 1
00 – Auto sleep/wakeup enable	00 – Ref Gain Control DAC – bit 0

13.1.9 RS-232 Serial Port Registers

Serial Port Baud Rate (SPBAUD)	Serial Port Status (SPSTAT)	Serial Port Receive (RXCHAR)	Serial Port Transmit (TXCHAR)
E040h (R/W)	**E041h (R/W)**	**E042h (R/W)**	**E043h (R/W)**
15 – Reads 0	15 – Reads 0	15 – Reads 0	15 – Reads 0
14 – Reads 0	14 – Reads 0	14 – Reads 0	14 – Reads 0
13 – Reads 0	13 – Reads 0	13 – Reads 0	13 – Reads 0
12 – Reads 0	12 – Reads 0	12 – Reads 0	12 – Reads 0
11 – Reads 0	11 – Reads 0	11 – Reads 0	11 – Reads 0
10 – Reads 0	10 – Reads 0	10 – Reads 0	10 – Reads 0
09 – Baud Rate Count – Bit 09	09 – Reads 0	09 – Reads 0	09 – Reads 0
08 – Baud Rate Count – Bit 08	08 – Reads 0	08 – Reads 0	08 – Reads 0
07 – Baud Rate Count – Bit 07	07 – Reads 0	07 – Receive Data – Bit 07	07 – Transmit Data – Bit 07
06 – Baud Rate Count – Bit 06	06 – Reads 0	06 – Receive Data – Bit 06	06 – Transmit Data – Bit 06
05 – Baud Rate Count – Bit 05	05 – Reads 0	05 – Receive Data – Bit 05	05 – Transmit Data – Bit 05
04 – Baud Rate Count – Bit 04	04 – Reads 0	04 – Receive Data – Bit 04	04 – Transmit Data – Bit 04
03 – Baud Rate Count – Bit 03	03 – Enable Diagnostic Loop	03 – Receive Data – Bit 03	03 – Transmit Data – Bit 03
02 – Baud Rate Count – Bit 02	02 – Transmit in progress (RO)	02 – Receive Data – Bit 02	02 – Transmit Data – Bit 02
01 – Baud Rate Count – Bit 01	01 – Receive overrun occurred	01 – Receive Data – Bit 01	01 – Transmit Data – Bit 01
00 – Baud Rate Count – Bit 00	00 – Valid Rcv character (RO)	00 – Receive Data – Bit 00	00 – Transmit Data – Bit 00

13.1.10 Write Gate Qualification/Drive Fault Registers

DRIVE FAULT CONFIGURATION (DFLCFG)	WRITE GATE DISABLE DRIVE FAULT (WRGTDF)	DRIVE FAULT PENDING (DFLTPD)
E044h (R/W)	**E045h (R/W)**	**E046h (R/W)**
15 – Reserved	15 – Reserved	15 – Reserved
14 – Reserved	14 – DSP write disable mask	14 – Reserved
13 – Enable STM Missing DF on read	13 – Seq write disable mask	13 – Reserved
12 – 1 = DRVFLT pin Output enable	12 – Missing STM write disable mask	12 – Reserved
11 – 1 = Negative QWRTGT output	11 – Index/Address write disable mask	11 – Reserved
10 – 1 = Negative Write Gate Input	10 – Shock write disable mask	10 – Reserved
09 – 1 = Disable AEERR XOR	09 – AE WR error write disable mask	09 – Reserved
08 – 1 = Enable Negative AEERR	08 – AE RD error write disable mask	08 – Reserved
07 – AEERR blank time – bit 7	07 – Reserved	07 – Reserved
06 – AEERR blank time – bit 6	06 – DSP drive faultmask	06 – DSP drive fault (1-to-clr)
05 – AEERR blank time – bit 5	05 – Seq drive fault mask	05 – Sequencer drive fault (1-to-clr)
04 – AEERR blank time – bit 4	04 – Missing STM drive fault mask	04 – Missing STM drive fault (1-to-clr)
03 – AEERR blank time – bit 3	03 – Index/Address drive faultmask	03 – Index/Address drive fault (1-to-clr)
02 – AEERR blank time – bit 2	02 – Shock drive fault mask	02 – Shock WR drive fault (1-to-clr)
01 – AEERR blank time – bit 1	01 – AE WR error drive fault mask	01 – AE WR Err drive fault (1-to-clr)
00 – AEERR blank time – bit 0	00 – AE RD error drive fault mask	00 – AE RD Err drive fault (1-to-clr)

13.1.11 Servo Decoder/Sequencer Registers

DSEC Pulse 1 Time (PUL1TM)	DSEC Pulse 2 Time (PUL2TM)	DSEC Pulse 3 Time (PUL3TM)	DSEC Pulse 4 Time (PUL4TM)
E048h (R/W)	E049h (R/W)	E04Ah (R/W)	E04Bh (R/W)
15 – DSEC 1 pulse time – Bit 15	15 – DSEC 2 pulse time – Bit 15	15 – DSEC 3 pulse time – Bit 15	15 – DSEC 4 pulse time – Bit 15
14 – DSEC 1 pulse time – Bit 14	14 – DSEC 2 pulse time – Bit 14	14 – DSEC 3 pulse time – Bit 14	14 – DSEC 4 pulse time – Bit 14
13 – DSEC 1 pulse time – Bit 13	13 – DSEC 2 pulse time – Bit 13	13 – DSEC 3 pulse time – Bit 13	13 – DSEC 4 pulse time – Bit 13
12 – DSEC 1 pulse time – Bit 12	12 – DSEC 2 pulse time – Bit 12	12 – DSEC 3 pulse time – Bit 12	12 – DSEC 4 pulse time – Bit 12
11 – DSEC 1 pulse time – Bit 11	11 – DSEC 2 pulse time – Bit 11	11 – DSEC 3 pulse time – Bit 11	11 – DSEC 4p ulse time – Bit 11
10 – DSEC 1 pulse time – Bit 10	10 – DSEC 2 pulse time – Bit 10	10 – DSEC 3 pulse time – Bit 10	10 – DSEC 4 pulse time – Bit 10
09 – DSEC 1 pulse time – Bit 09	09 – DSEC 2 pulse time – Bit 09	09 – DSEC 3 pulse time – Bit 09	09 – DSEC 4 pulse time – Bit 09
08 – DSEC 1 pulse time – Bit 08	08 – DSEC 2 pulse time – Bit 08	08 – DSEC 3 pulse time – Bit 08	08 – DSEC 4 pulse time – Bit 08
07 – DSEC 1 pulse time – Bit 07	07 – DSEC 2 pulse time – Bit 07	07 – DSEC 3 pulse time – Bit 07	07 – DSEC 4 pulse time – Bit 07
06 – DSEC 1 pulse time – Bit 06	06 – DSEC 2 pulse time – Bit 06	06 – DSEC 3 pulse time – Bit 06	06 – DSEC 4 pulse time – Bit 06
05 – DSEC 1 pulse time – Bit 05	05 – DSEC 2 pulse time – Bit 05	05 – DSEC 3 pulse time – Bit 05	05 – DSEC 4 pulse time – Bit 05
04 – DSEC 1 pulse time – Bit 04	04 – DSEC 2 pulse time – Bit 04	04 – DSEC 3 pulse time – Bit 04	04 – DSEC 4 pulse time – Bit 04
03 – DSEC 1 pulse time – Bit 03	03 – DSEC 2 pulse time – Bit 03	03 – DSEC 3 pulse time – Bit 03	03 – DSEC 4 pulse time – Bit 03
02 – DSEC 1 pulse time – Bit 02	02 – DSEC 2 pulse time – Bit 02	02 – DSEC 3 pulse time – Bit 02	02 – DSEC 4 pulse time – Bit 02
01 – DSEC 1 pulse time – Bit 01	01 – DSEC 2 pulse time – Bit 01	01 – DSEC 3 pulse time – Bit 01	01 – DSEC 4 pulse time – Bit 01
00 – DSEC 1 pulse time – Bit 00	00 – DSEC 2 pulse time – Bit 00	00 – DSEC 3 pulse time – Bit 00	00 – DSEC 4 pulse time – Bit 00

DSEC Pulse 5 Time (PUL5TM)	DSEC Pulse 6 Time (PUL6TM)	DSEC Pulse 7 Time (PUL7TM)	DSEC Pulse 8 Time (PUL8TM)
E04Ch (R/W)	E04Dh (R/W)	E04Eh (R/W)	E04Fh (R/W)
15 – DSEC 5 pulse time – Bit 15	15 – DSEC 6 pulse time – Bit 15	15 – DSEC 7 pulse time – Bit 15	15 – DSEC 8 pulse time – Bit 15
14 – DSEC 5 pulse time – Bit 14	14 – DSEC 6 pulse time – Bit 14	14 – DSEC 7 pulse time – Bit 14	14 – DSEC 8 pulse time – Bit 14
13 – DSEC 5 pulse time – Bit 13	13 – DSEC 6 pulse time – Bit 13	13 – DSEC 7 pulse time – Bit 13	13 – DSEC 8 pulse time – Bit 13
12 – DSEC 5 pulse time – Bit 12	12 – DSEC 6 pulse time – Bit 12	12 – DSEC 7 pulse time – Bit 12	12 – DSEC 8 pulse time – Bit 12
11 – DSEC 5 pulse time – Bit 11	11 – DSEC 6 pulse time – Bit 11	11 – DSEC 7 pulse time – Bit 11	11 – DSEC 8 pulse time – Bit 11
10 – DSEC 5 pulse time – Bit 10	10 – DSEC 6 pulse time – Bit 10	10 – DSEC 7 pulse time – Bit 10	10 – DSEC 8 pulse time – Bit 10
09 – DSEC 5 pulse time – Bit 09	09 – DSEC 6 pulse time – Bit 09	09 – DSEC 7 pulse time – Bit 09	09 – DSEC 8 pulse time – Bit 09
08 – DSEC 5 pulse time – Bit 08	08 – DSEC 6 pulse time – Bit 08	08 – DSEC 7 pulse time – Bit 08	08 – DSEC 8 pulse time – Bit 08
07 – DSEC 5 pulse time – Bit 07	07 – DSEC 6 pulse time – Bit 07	07 – DSEC 7 pulse time – Bit 07	07 – DSEC 8 pulse time – Bit 07
06 – DSEC 5 pulse time – Bit 06	06 – DSEC 6 pulse time – Bit 06	06 – DSEC 7 pulse time – Bit 06	06 – DSEC 8 pulse time – Bit 06
05 – DSEC 5 pulse time – Bit 05	05 – DSEC 6 pulse time – Bit 05	05 – DSEC 7 pulse time – Bit 05	05 – DSEC 8 pulse time – Bit 05
04 – DSEC 5 pulse time – Bit 04	04 – DSEC 6 pulse time – Bit 04	04 – DSEC 7 pulse time – Bit 04	04 – DSEC 8 pulse time – Bit 04
03 – DSEC 5 pulse time – Bit 03	03 – DSEC 6 pulse time – Bit 03	03 – DSEC 7 pulse time – Bit 03	03 – DSEC 8 pulse time – Bit 03
02 – DSEC 5 pulse time – Bit 02	02 – DSEC 6 pulse time – Bit 02	02 – DSEC 7 pulse time – Bit 02	02 – DSEC 8 pulse time – Bit 02
01 – DSEC 5 pulse time – Bit 01	01 – DSEC 6 pulse time – Bit 01	01 – DSEC 7 pulse time – Bit 01	01 – DSEC 8 pulse time – Bit 01
00 – DSEC 5 pulse time – Bit 00	00 – DSEC 6 pulse time – Bit 00	00 – DSEC 7 pulse time – Bit 00	00 – DSEC 8 pulse time – Bit 00

Decoder Configuration (DECCFG)	Decoder Control (DECCTL)	Decoder Status (DECSTA)	Target Address (TGTADR)
E050h (R/W)	**E051h (R/W)**	**E052h (R/W)**	**E053h (R/W)**
15 – SSEC-HI detection mode	15 – Reserved	15 – STM Missing (1-to-clr)	15 – Target Track Address – bit 15
14 – SSEC-LO detection mode	14 -Half Cell Count – bit 4	14 – Reserved	14 – Target Track Address – bit 14
13 – Negative POL level active	13 – Half Cell Count – bit 3	13 – Index/Address Compare (RO)	13 – Target Track Address – bit 13
12 – Negative RDP edge active	12 – Half Cell Count – bit 2	12 – Decoder Flag bit (RO)	12 – Target Track Address – bit 12
11 – 0=digital, 1= analog SHKSNS pin	11 – Half Cell Count – bit 1	11 – STM Detected latch (1 to clr)	11 – Target Track Address – bit 11
10 – Negative SHKSNS enable	10 – Half Cell Count – bit 0	10 – Reserved	10 – Target Track Address – bit 10
09 – 1 = Synthesized POL enable	09 – SRCH signal select – bit 2	09 – INDEX signal (RO)	09 – Target Track Address – bit 09
08 – Block Data Pulse Enable	08 – SRCH signal select – bit 1	08 – DSEC signal (RO)	08 – Target Track Address – bit 08
07 – INDEX/DSEC pulse width – bit 2	07 – SRCH signal select – bit 0	07 – SRCH signal (RO)	07 – Target Track Address – bit 07
06 – INDEX/DSEC pulse width – bit 1	06 – Enable Set Flag on HRBIT	06 – Reserved	06 – Target Track Address – bit 06
05 – INDEX/DSEC pulse width – bit 0	05 – Master Disable shift EXOR	05 – Reserved	05 – Target Track Address – bit 05
04 – 1=enable NRZ mode	04 – Set SRCH (1-to-set)	04 – AE Write error latch (1-to-clr)	04 – Target Track Address – bit 04
03 – Positive Pulse Enable B	03 – Enable Sector Timer	03 – AE Read error latch (1-to-clr)	03 – Target Track Address – bit 03
02 – Negative Pulse Enable B	02 – Burst Branch	02 – Shock detected (1-to-clr)	02 – Target Track Address – bit 02
01 – Positive Pulse Enable A	01 – Write Disable	01 – Reserved	01 – Target Track Address – bit 01
00 – Negative Pulse Enable A	00 – Burst Seq'r Run Enable	00 – Reset SRCH (1 to clr)	00 – Target Track Address – bit 00

Address Compare Mask (ADRMSK)	Gray Code Shift (GRAYSH)	Gating Configuration (GTECFG)	Index Target (IDXTGT)
E054h (R/W)	**E055h (R/W) or ext6 (R/W)**	**E056h (R/W)**	**E057h (R/W)**
15 – Address Compare Mask – bit 15	15 – Binary Track Address – bit 15	15 – Gate A Aux Enable	15 – INDEX Target – bit 15
14 – Address Compare Mask – bit 14	14 – Binary Track Address – bit 14	14 – Gate B Aux Enable	14 – INDEX Target – bit 14
13 – Address Compare Mask – bit 13	13 – Binary Track Address – bit 13	13 – Gate C Aux Enable	13 – INDEX Target – bit 13
12 – Address Compare Mask – bit 12	12 – Binary Track Address – bit 12	12 – Gate D Aux Enable	12 – INDEX Target – bit 12
11 – Address Compare Mask – bit 11	11 – Binary Track Address – bit 11	11 – Discharge Aux Enable	11 – INDEX Target – bit 11
10 – Address Compare Mask – bit 10	10 – Binary Track Address – bit 10	10 – Select A Aux Enable	10 – INDEX Target – bit 10
09 – Address Compare Mask – bit 09	09 – Binary Track Address – bit 09	09 – Extra Sel 2 Aux Enable	09 – INDEX Target – bit 09
08 – Address Compare Mask – bit 08	08 – Binary Track Address – bit 08	08 – Extra Sel 1 Aux Enable	08 – INDEX Target – bit 08
07 – Address Compare Mask – bit 07	07 – Binary Track Address – bit 07	07 – Gate A Aux	07 – INDEX Target – bit 07
06 – Address Compare Mask – bit 06	06 – Binary Track Address – bit 06	06 – Gate B Aux	06 – INDEX Target – bit 06
05 – Address Compare Mask – bit 05	05 – Binary Track Address – bit 05	05 – Gate C Aux	05 – INDEX Target – bit 05
04 – Address Compare Mask – bit 04	04 – Binary Track Address – bit 04	04 – Gate D Aux	04 – INDEX Target – bit 04
03 – Address Compare Mask – bit 03	03 – Binary Track Address – bit 03	03 – Discharge Aux	03 – INDEX Target – bit 03
02 – Address Compare Mask – bit 02	02 – Binary Track Address – bit 02	02 – Select A Aux	02 – INDEX Target – bit 02
01 – Address Compare Mask – bit 01	01 – Binary Track Address – bit 01	01 – Extra Sel 2 Aux	01 – INDEX Target – bit 01
00 – Address Compare Mask – bit 00	00 – Binary Track Address – bit 00	00 – Extra Sel 1 Aux	00 – INDEX Target – bit 00

Index Compare Mask (IDXMSK)	Index Shift (INDXSH)	Latched Sector Time (SECTIM)	Search Window Time (SRCHTM)
E058h (R/W)	**E059h (R/W) or ext7 (R/W)**	**E05Ah (RO)**	**E05Bh (R/W)**
15 – INDEX Mask – bit 15	15 – INDEX – bit 15	15 – Sector Timer Value – bit 15	15 – Search Window Enable Cnt – bit 15
14 – INDEX Mask – bit 14	14 – INDEX – bit 14	14 – Sector Timer Value – bit 14	14 – Search Window Enable Cnt – bit 14
13 – INDEX Mask – bit 13	13 – INDEX – bit 13	13 – Sector Timer Value – bit 13	13 – Search Window Enable Cnt – bit 13
12 – INDEX Mask – bit 12	12 – INDEX – bit 12	12 – Sector Timer Value – bit 12	12 – Search Window Enable Cnt – bit 12
11 – INDEX Mask – bit 11	11 – INDEX – bit 11	11 – Sector Timer Value – bit 11	11 – Search Window Enable Cnt – bit 11
10 – INDEX Mask – bit 10	10 – INDEX – bit 10	10 – Sector Timer Value – bit 10	10 – Search Window Enable Cnt – bit 10
09 – INDEX Mask – bit 09	09 – INDEX – bit 09	09 – Sector Timer Value – bit 09	09 – Search Window Enable Cnt – bit 09
08 – INDEX Mask – bit 08	08 – INDEX – bit 08	08 – Sector Timer Value – bit 08	08 – Search Window Enable Cnt – bit 08
07 – INDEX Mask – bit 07	07 – INDEX – bit 07	07 – Sector Timer Value – bit 07	07 – Search Window Enable Cnt – bit 07
06 – INDEX Mask – bit 06	06 – INDEX – bit 06	06 – Sector Timer Value – bit 06	06 – Search Window Enable Cnt – bit 06
05 – INDEX Mask – bit 05	05 – INDEX – bit 05	05 – Sector Timer Value – bit 05	05 – Search Window Enable Cnt – bit 05
04 – INDEX Mask – bit 04	04 – INDEX – bit 04	04 – Sector Timer Value – bit 04	04 – Search Window Enable Cnt – bit 04
03 – INDEX Mask – bit 03	03 – INDEX – bit 03	03 – Sector Timer Value – bit 03	03 – Search Window Enable Cnt – bit 03
02 – INDEX Mask – bit 02	02 – INDEX – bit 02	02 – Sector Timer Value – bit 02	02 – Search Window Enable Cnt – bit 02
01 – INDEX Mask – bit 01	01 – INDEX – bit 01	01 – Sector Timer Value – bit 01	01 – Search Window Enable Cnt – bit 01
00 – INDEX Mask – bit 00	00 – INDEX – bit 00	00 – Sector Timer Value – bit 00	00 – Search Window Enable Cnt – bit 00

Current Value of Sector Timer (STIMER)	Power On Time (PRONTM)	Index Pulse Time (INDXTM)	Dedicated PWM Time (PWMTIM)
E05Ch (RO)	**E05Dh (R/W)**	**E05Eh (R/W)**	**E05Fh (R/W)**
15 – Sector Timer Value – bit 15	15 – Power On Timer Value – bit 15	15 – INDEX pulse time – bit 15	15 – PWM Timer Value – bit 15
14 – Sector Timer Value – bit 14	14 – Power On Timer Value – bit 14	14 – INDEX pulse time – bit 14	14 – PWM Timer Value – bit 14
13 – Sector Timer Value – bit 13	13 – Power On Timer Value – bit 13	13 – INDEX pulse time – bit 13	13 – PWM Timer Value – bit 13
12 – Sector Timer Value – bit 12	12 – Power On Timer Value – bit 12	12 – INDEX pulse time – bit 12	12 – PWM Timer Value – bit 12
11 – Sector Timer Value – bit 11	11 – Power On Timer Value – bit 11	11 – INDEX pulse time – bit 11	11 – PWM Timer Value – bit 11
10 – Sector Timer Value – bit 10	10 – Power On Timer Value – bit 10	10 – INDEX pulse time – bit 10	10 – PWM Timer Value – bit 10
09 – Sector Timer Value – bit 09	09 – Power On Timer Value – bit 09	09 – INDEX pulse time – bit 09	09 – PWM Timer Value – bit 09
08 – Sector Timer Value – bit 08	08 – Power On Timer Value – bit 08	08 – INDEX pulse time – bit 08	08 – PWM Timer Value – bit 08
07 – Sector Timer Value – bit 07	07 – Power On Timer Value – bit 07	07 – INDEX pulse time – bit 07	07 – PWM Timer Value – bit 07
06 – Sector Timer Value – bit 06	06 – Power On Timer Value – bit 06	06 – INDEX pulse time – bit 06	06 – PWM Timer Value – bit 06
05 – Sector Timer Value – bit 05	05 – Power On Timer Value – bit 05	05 – INDEX pulse time – bit 05	05 – PWM Timer Value – bit 05
04 – Sector Timer Value – bit 04	04 – Power On Timer Value – bit 04	04 – INDEX pulse time – bit 04	04 – PWM Timer Value – bit 04
03 – Sector Timer Value – bit 03	03 – Power On Timer Value – bit 03	03 – INDEX pulse time – bit 03	03 – PWM Timer Value – bit 03
02 – Sector Timer Value – bit 02	02 – Power On Timer Value – bit 02	02 – INDEX pulse time – bit 02	02 – PWM Timer Value – bit 02
01 – Sector Timer Value – bit 01	01 – Power On Timer Value – bit 01	01 – INDEX pulse time – bit 01	01 – PWM Timer Value – bit 01
00 – Sector Timer Value – bit 00	00 – Power On Timer Value – bit 00	00 – INDEX pulse time – bit 00	00 – PWM Timer Value – bit 00

13.1.12 Spindle Control Registers

Spindle DAC Current (SPNDAC)	Spindle Period (SPNTIM)	Speed Error (SPDERR)
E060h (R/W)	**E061h (R/W)**	**E062h (R/W)**
15 – Reads 0	15 – Desired rotation period Bit 15	15 – Index spindle period count Bit 15
14 – Reads 0	14 – Desired rotation period Bit 14	14 – Index spindle period count Bit 14
13 – Reads 0	13 – Desired rotation period Bit 13	13 – Index spindle period count Bit 13
12 – Reads 0	12 – Desired rotation period Bit 12	12 – Index spindle period count Bit 12
11 – Reads 0	11 – Desired rotation period Bit 11	11 – Index spindle period count Bit 11
10 – Reads 0	10 – Desired rotation period Bit 10	10 – Index spindle period count Bit 10
09 – Reads 0	09 – Desired rotation period Bit 09	09 – Index spindle period count Bit 09
08 – Reads 0	08 – Desired rotation period Bit 08	08 – Index spindle period count Bit 08
07 – Binary bit 7	07 – Desired rotation period Bit 07	07 – Index spindle period count Bit 07
06 – Binary bit 6	06 – Desired rotation period Bit 06	06 – Index spindle period count Bit 06
05 – Binary bit 5	05 – Desired rotation period Bit 05	05 – Index spindle period count Bit 05
04 – Binary bit 4	04 – Desired rotation period Bit 04	04 – Index spindle period count Bit 04
03 – Binary bit 3	03 – Desired rotation period Bit 03	03 – Index spindle period count Bit 03
02 – Binary bit 2	02 – Desired rotation period Bit 02	02 – Index spindle period count Bit 02
01 – Binary bit 1	01 – Desired rotation period Bit 01	01 – Index spindle period count Bit 01
00 – Binary bit 0	00 – Desired rotation period Bit 00	00 – Index spindle period count Bit 00

Spindle Control (Spnctl)	Spin Count Register (SPNCNT)
E065h (R/W)	**E066h (R/W)**
15 – Reads 0	15 – Reads 0
14 – Reads 0	14 – Reads 0
13 – Reads 0	13 – Reads 0
12 – Reads 0	12 – Reads 0
11 – Reads 0	11 – Reads 0
10 – Reads 0	10 – Reads 0
09 – Reads 0	09 – Reads 0
08 – Reads 0	08 – Reads 0
07 – Reads 0	07 – Spin Event Count Bit 7
06 – Reads 0	06 – Spin Event Count Bit 6
05 – Reads 0	05 – Spin Event Count Bit 5
04 – Enable SPDERR Saturation	04 – Spin Event Count Bit 4
03 – Enable Spin Counters	03 – Spin Event Count Bit 3
02 – CLKSRC: 0=bus; 1=bus/8	02 – Spin Event Count Bit 2
01 – Spin Interrupt Source Bit 1	01 – Spin Event Count Bit 1
00 – Spin Interrupt Source Bit 0	00 – Spin Event Count Bit 0

13.1.13 Timer Registers

Timer-0 Control (TM0CTL)	Timer-0 Initial Count (TM0SET)	Timer-0 Current Count (TM0CNT)
E070h (R/W)	**E071h (R/W)**	**E072h (RO)**
15 – Reads 0	15 – Initial Timer Count – Bit 15	15 – Current Timer Count – Bit 15
14 – Reads 0	14 – Initial Timer Count – Bit 14	14 – Current Timer Count – Bit 14
13 – Reads 0	13 – Initial Timer Count – Bit 13	13 – Current Timer Count – Bit 13
12 – Reads 0	12 – Initial Timer Count – Bit 12	12 – Current Timer Count – Bit 12
11 – Reads 0	11 – Initial Timer Count – Bit 11	11 – Current Timer Count – Bit 11
10 – Reads 0	10 – Initial Timer Count – Bit 10	10 – Current Timer Count – Bit 10
09 – Reads 0	09 – Initial Timer Count – Bit 09	09 – Current Timer Count – Bit 09
08 – Mode: 0 = one-shot; 1 = periodic	08 – Initial Timer Count – Bit 08	08 – Current Timer Count – Bit 08
07 – Timer count enable/start	07 – Initial Timer Count – Bit 07	07 – Current Timer Count – Bit 07
06 – Timer prescale – Bit 6	06 – Initial Timer Count – Bit 06	06 – Current Timer Count – Bit 06
05 – Timer prescale – Bit 5	05 – Initial Timer Count – Bit 05	05 – Current Timer Count – Bit 05
04 – Timer prescale – Bit 4	04 – Initial Timer Count – Bit 04	04 – Current Timer Count – Bit 04
03 – Timer prescale – Bit 3	03 – Initial Timer Count – Bit 03	03 – Current Timer Count – Bit 03
02 – Timer prescale – Bit 2	02 – Initial Timer Count – Bit 02	02 – Current Timer Count – Bit 02
01 – Timer prescale – Bit 1	01 – Initial Timer Count – Bit 01	01 – Current Timer Count – Bit 01
00 – Timer prescale – Bit 0	00 – Initial Timer Count – Bit 00	00 – Current Timer Count – Bit 00

13.1.14 General-Purpose I/O Registers

General-purpose I/O Control (GPIOCL)	General-purpose I/O Data (GPIODT)	General-purpose I/O Configuration (GPIOCF)
E080h (R/W)	**E081h (R/W)**	**E082h (R/W)**
15 – Reads 0 (RO)	15 – Reads 0 (RO)	15 – Reads 0 (RO)
14 – Output Enable – Bit 14 (SDATA)	14 – Input/Output Data – Bit 14 (SDATA)	14 – Reads 0 (RO)
13 – Output Enable – Bit 13 (SCLK)	13 – Input/Output Data – Bit 13 (SCLK)	13 – Reads 0 (RO)
12 – Output Enable – Bit 12 (SDEN)	12 – Input/Output Data – Bit 12 (SDEN)	12 – Reads 0 (RO)
11 – Output Enable – Bit 11 (APPCS)	11 – Input/Output Data – Bit 11 (APPCS)	11 – Reads 0 (RO)
10 – Output Enable – Bit 10	10 – Input/Output Data – Bit 10	10 – Enable DEDICATED PWM GPIO[10]
09 – Output Enable – Bit 09	09 -Input/Output Data – Bit 09	09 – Enable SETPON PWM GPIO[09]
08 – Output Enable – Bit 08	08 – Input/Output Data – Bit 08	08 – Reads 0 (RO)
07 – Output Enable – Bit 07	07 – Input/Output Data – Bit 07	07 – Reads 0 (RO)
06 – Output Enable – Bit 06	06 – Input/Output Data – Bit 06	06 – Reads 0 (RO)
05 – Output Enable – Bit 05	05 – Input/Output Data – Bit 05	05 – Reads 0 (RO)
04 – Output Enable – Bit 04	04 – Input/Output Data – Bit 04	04 – Reads 0 (RO)
03 – Output Enable – Bit 03	03 – Input/Output Data – Bit 03	03 – Reads 0 (RO)
02 – Output Enable – Bit 02	02 – Input/Output Data – Bit 02	02 – Reads 0 (RO)
01 – Output Enable – Bit 01	01 – Input/Output Data – Bit 01	01 – Disable Internal Pullup GPIO[01]
00 – Output Enable – Bit 00	00 – Input/Output Data – Bit 00	00 – Disable Internal Pullup GPIO[00]

13.1.15 Manufacturing Test Registers

Manufacturing Test Register (MFGTST)
E084h (R/W)
15 – atest Bit 3
14 – atest Bit 2
13 – atest Bit 1
12 – atest Bit 0
11 – test_spin
10 – test_acq
09 – test_servo
08 – test_rs232
07 – break_dividers
06 – test_timer
05 – test_rom
04 – test_pine
03 – en_pine
02 – en_16bit_parl
01 – en_parallel
00 – en_dataspace_acc

13.1.16 Burst Sequencer RAM

SEQ Address	MMIO Address	Reserved	MMIO Address	Reserved	Timer & Latch Controls	MMIO Address	Pin Values (Gates)	Sequencer Signals	BR Type	MMIO Address	Interrupt	Branch Address	Timer Load Value
00	E100		E101			E102				E103			
01	E104		E105			E106				E107			
02	E108		E109			E10A				E10B			
03	E10C		E10D			E10E				E10F			
04	E110		E111			E112				E113			
05	E114		E115			E116				E117			
06	E118		E119			E11A				E11B			
07	E11C		E11D			E11E				E11F			
08	E120		E121			E122				E123			
09	E124		E125			E126				E127			
0A	E128		E129			E12A				E12B			
0B	E12C		E12D			E12E				E12F			
0C	E130		E131			E132				E133			
0D	E134		E135			E136				E137			
0E	E138		E139			E13A				E13B			
0F	E13C		E13D			E13E				E13F			
10	E140		E141			E142				E143			
11	E144		E145			E146				E147			
12	E148		E149			E14A				E14B			
13	E14C		E14D			E14E				E14F			
14	E150		E151			E152				E153			
15	E154		E155			E156				E157			
16	E158		E159			E15A				E15B			
17	E15C		E15D			E15E				E15F			
18	E160		E161			E162				E163			
19	E164		E165			E166				E167			
1A	E168		E169			E1A6				E16B			
1B	E16C		E16D			E16E				E16F			
1C	E170		E171			E172				E173			
1D	E174		E175			E176				E177			
1E	E178		E179			E17A				E17B			
1F	E17C		E17D			E17E				E17F			
	Bit:	f:0	Bit:	f:7	6:0	Bit:	f:8	7:3	2:0	Bit:	f	e:a	9:0

13.1.17 Timing Mark Sequencer RAM

SEQ Address	MMIO Address	Reserved	Branch Address	MMIO Address	Branch & Timer Controls	Count Values
00	E200			E201		
01	E202			E203		
02	E204			E205		
03	E206			E207		
04	E208			E209		
05	E20A			E20B		
06	E20C			E20D		
07	E20E			E20F		
08	E210			E211		
09	E212			E213		
0A	E214			E215		
0B	E216			E217		
0C	E218			E219		
0D	E21A			E21B		
0E	E21C			E21D		
0F	E21E			E21F		
	BIT:	f:4	3:0	BIT:	f:8	7:0

13.1.18 Vector Shadow RAM

Vector Shadow RAM (SHADOWS C:0000H – C:000FH)
EF00h – EF0Fh
15 – Opcode – Bit 15
14 – Opcode – Bit 14
13 – Opcode – Bit 13
12 – Opcode – Bit 12
11 – Opcode – Bit 11
10 – Opcode – Bit 10
09 – Opcode – Bit 09
08 – Opcode – Bit 08
07 – Opcode – Bit 07
06 – Opcode – Bit 06
05 – Opcode – Bit 05
04 – Opcode – Bit 04
03 – Opcode – Bit 03
02 – Opcode – Bit 02
01 – Opcode – Bit 01
00 – Opcode – Bit 00

14.1 AIC-4421 MQFP Packaging Specifications

Figure 14-1 shows the physical dimensions of the AIC-4421's 128-pin MQFP package.

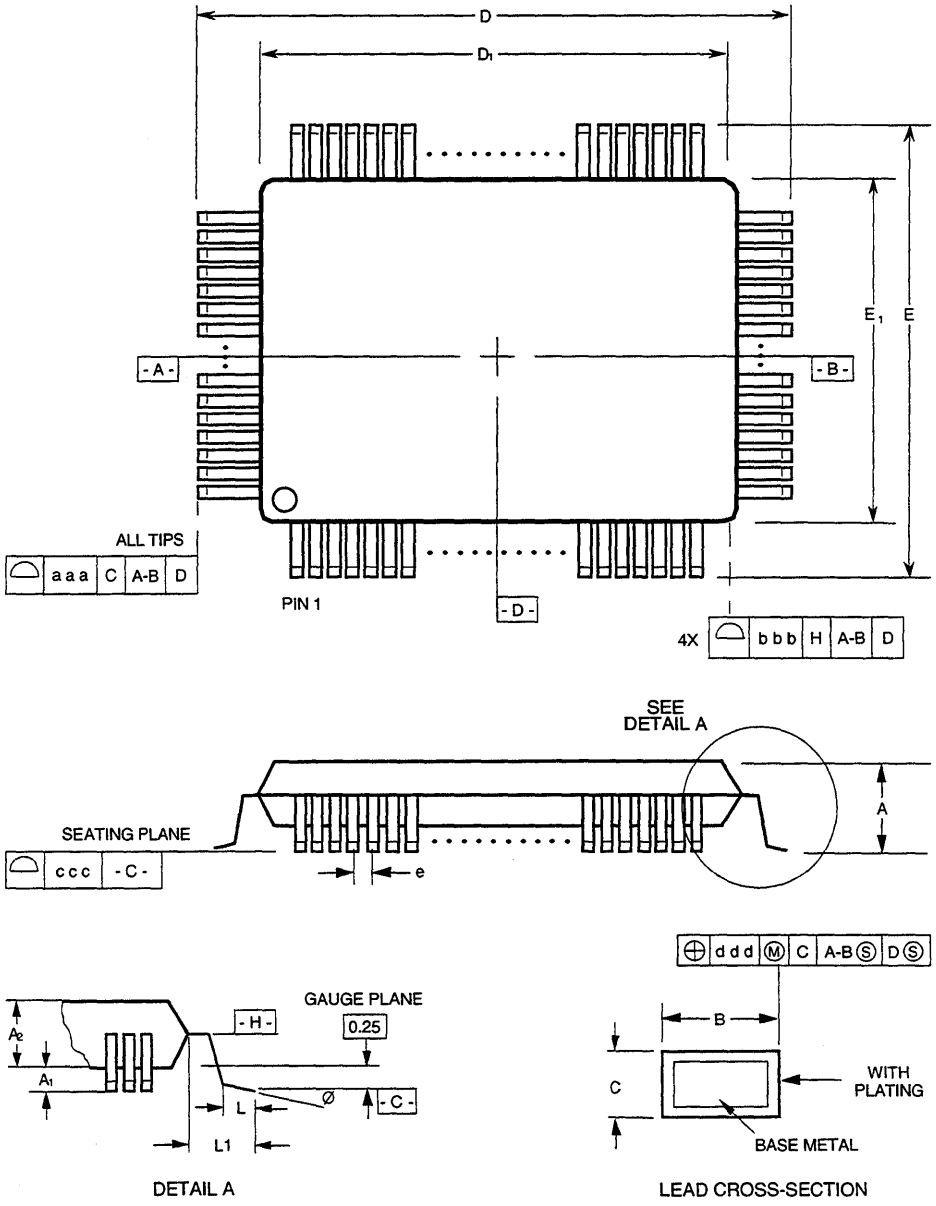

Figure 14-1 128-Pin MQFP Package Outline

Table 14-1 AIC-4421 MQFP Package Dimensions

SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	3.40	-	-	0.134
A1	0.25	-	-	.010	-	-
A2	2.55	2.80	3.05	0.100	0.110	0.120
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.13	-	0.23	0.005	-	0.009
D	22.95	23.20	23.45	0.904	0.913	0.923
D1	19.90	20.00	20.10	0.783	0.787	0.791
E	16.95	17.20	17.45	0.667	0.677	0.687
E1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.50 BSC			0.02 BSC		
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 BSC			0.063 BSC		
Ø	0 deg	3.5 deg	7 deg	0 deg	3.5 deg	7 deg
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

**NOTES:*

1. *Controlling dimensions are in millimeters (mm).*
2. *Datums A-B and -D- to be determined at datum plane -H-.*
3. *Reference plane -H- is located at mold parting line and is coincident with bottom of lead where it exits plastic body.*
4. *Dimensions D and E to be determined at seating plane -C-.*
5. *Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.*
6. *Dimension B does not include dambar protrusion. Allowable protrusion shall be .08 mm total in excess of B dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07 mm*
7. *The dimensions shown in lead cross-section apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.*
8. *A1 is defined as the distance from the seating plane to the lowest point of the package body.*
9. *Solder plate thickness shall be 200 microinches minimum.*

14.2 AIC-4421 TQFP Packaging Specifications

Figure 14-2 shows the physical dimensions of the AIC-4421's 128-pin TQFP package.

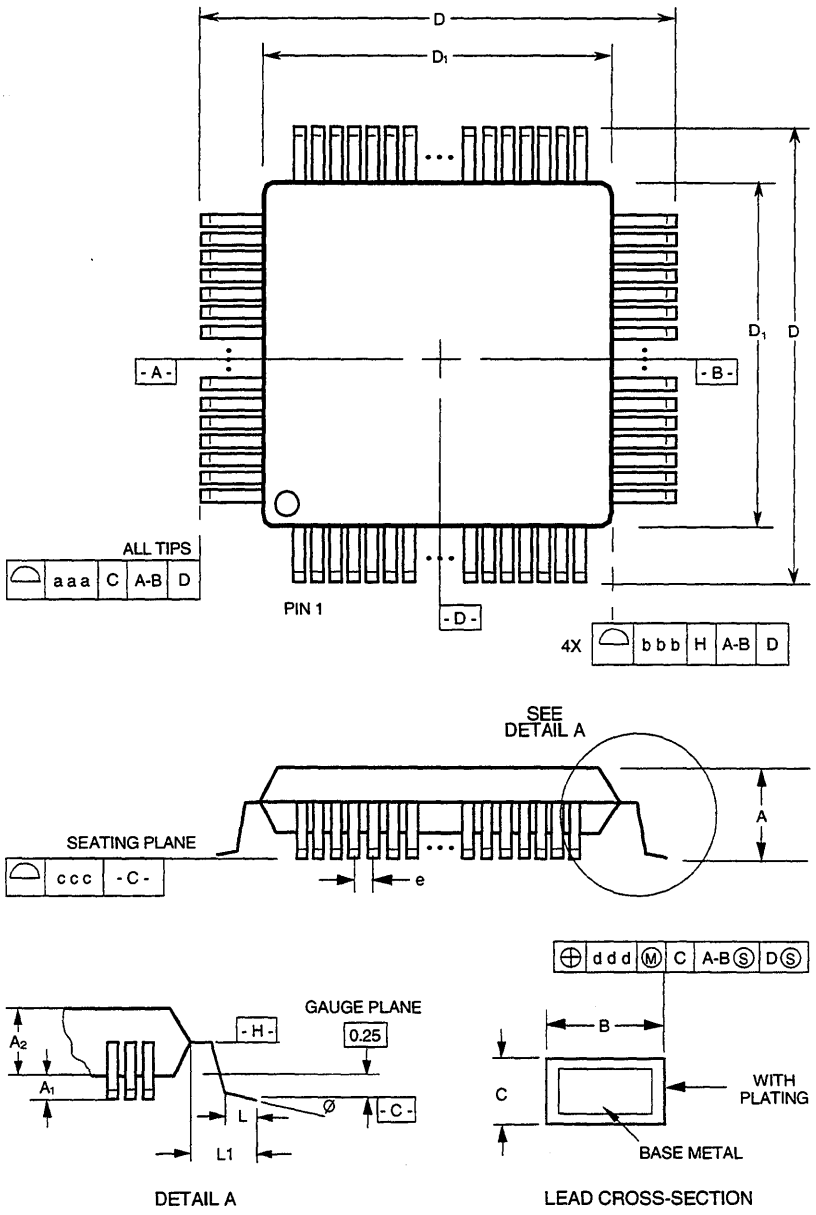

Figure 14-2 128-Pin TQFP Package Outline

Table 14-2 AIC-4421 TQFP Package Dimensions

SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.13	0.18	0.23	0.005	0.007	0.009
C	0.09	-	0.20	0.004	-	0.008
D	16.00 BSC			0.630 BSC		
D1	14.00 BSC			0.551 BSC		
E	16.00 BSC			0.630 BSC		
E1	14.00 BSC			0.551 BSC		
e	0.40 BSC			0.0157 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 BSC			0.039 BSC		
Ø	0 deg	3.5 deg	7 deg	0 deg	3.5 deg	7 deg
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

**NOTES:*

1. *Controlling dimensions are in millimeters (mm).*
2. *Datums A-B and -D- to be determined at datum plane -H-.*
3. *Reference plane -H- is located at mold parting line and is coincident with bottom of lead where it exits plastic body.*
4. *Dimensions D to be determined at seating plane -C-.*
5. *Dimensions D1 do not include mold protrusion. Allowable protrusion is .25 mm per side. Dimensions D1 are maximum plastic body size dimensions including mold mismatch.*
6. *Dimension B does not include dambar protrusion. Allowable protrusion shall be .08 mm total in excess of B dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07 mm*
7. *The dimensions shown in lead cross-section apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.*
8. *A1 is defined as the distance from the seating plane to the lowest point of the package body.*
9. *Solder plate thickness shall be 200 microinches minimum.*

SECTION 15
Additional References

Please see the following Adaptec user documents for additional information regarding this IC.

- Digital Signal Processor - DSP Core Programmer's Manual, PN: 700175-011
- Macro Assembler and Linker - DM_ASM and DM_CoffLink User's Manual, PN: 700174-011
- C-Language Compiler - DM_C Compiler User's Manual, PN: 700216-011
- Debugger - DM_DBG Programmer's User's Manual, PN: 700176-011
- AIC-4421 Drive Manager Chip ROM Code User's Guide, PN: 700245-011

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