1 Introduction

About This Chapter

Read this chapter to find out

- General information about the AIC-7850 single-chip SCSI host adapter
- How the AIC-7850 interfaces with commercially available PCI chipsets

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▼▼▼▼▼ 1

Introduction

The AIC-7850 is a completely integrated, single-chip SCSI host adapter for motherboard applications. Since the AIC-7850's architecture is similar to the AIC -7870, the AIC-7850 is software compatible to the AIC-7870. All SCSI sequences are managed by the PhaseEngine, a high-performance on-chip 10 MIPS RISC processor. Fast SCSI-2 technology, capable of transfer speeds of up to 10 MBytes/sec, maximizes I/O throughput in high-performance PCs and workstations for optimal utilization of the 133 MBytes/sec PCI local bus. The AIC-7850 is tested extensively over a large matrix of operating systems, peripherals and systems to ensure a high degree of compatibility and reliability.

The AIC-7850 incorporates all the functionality of a high-performance SCSI host adapter in a single-chip solution. The PCI host interface, the SCSI protocol controller, a powerful 10 MIPS processor and a large 128-byte FIFO are all provided in a 100-pin plastic quad flat pack (PQFP) package. The smaller footprint single-chip solution economizes on valuable motherboard space and saves add-in slots for other functions.

The AIC-7850's bus master host interface and SCSI PhaseEngine are very effective in offloading the host CPU and other system resources, resulting in maximum system performance.

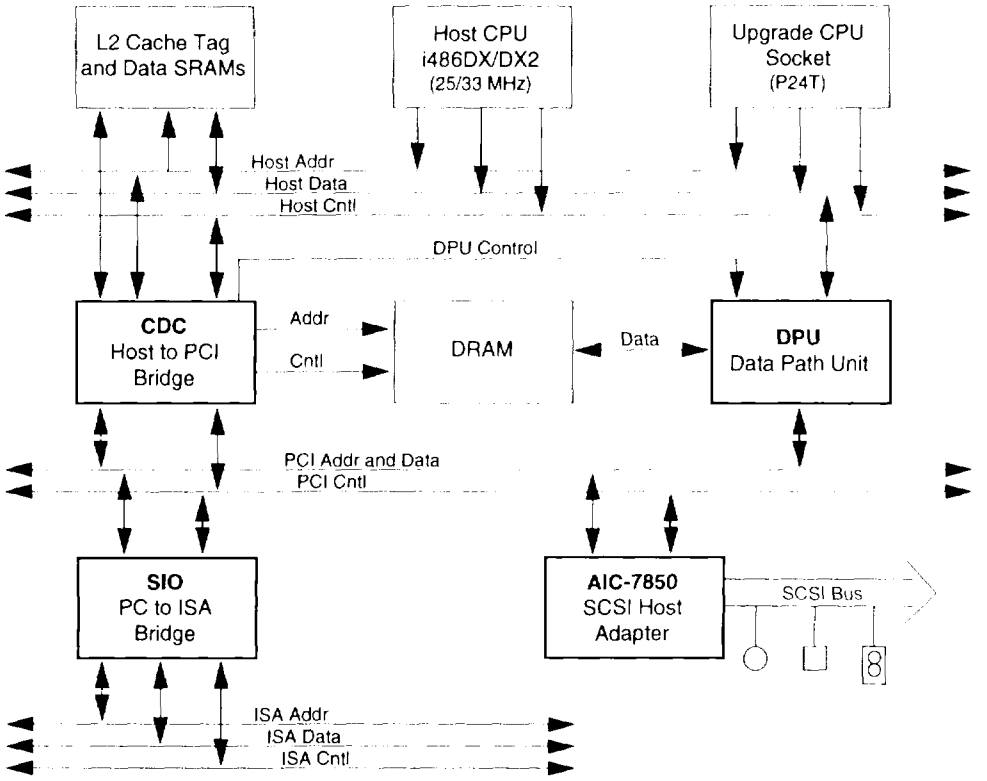
The PCI host interface on the AIC-7850 supports the 32-bit PCI Rev. 2.0 interface with bus master burst data transfers up to the maximum rate of 133 MBytes/sec. Data is parity protected throughout its journey through the chip. The large 128-byte FIFO maximizes DMA transfers and reduces system latencies. The AIC-7850 supports the requisite PCI configuration space and allows AIC-7850 register mapping to either memory or I/O address space. The 10 MIPS SCSI PhaseEngine controls SCSI phase operations and thereby functions as an I/O coprocessor which offloads the host CPU. The SCSI PhaseEngine is microprogrammed by the controlling driver software and can execute complete SCSI commands, from start to finish, independent of any host processor intervention. With SCB swapping software the AIC-7850 can have up to 255 SCSI commands outstanding. On-chip advanced power management functions dramatically decrease power consumption with Sleep, Suspend, and Resume features.

This document describes the major features of the AIC-7850 architecture as they apply to the design and usage of the device in PCI motherboard designs.

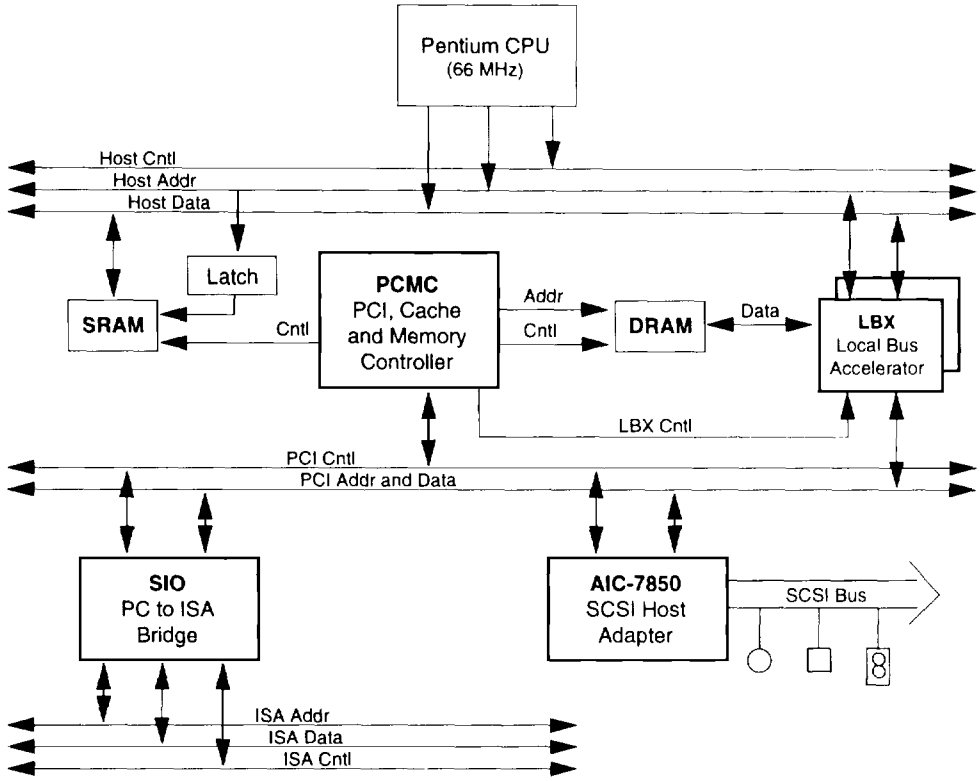
Connecting into the Motherboard

The AIC-7850 connects directly to a PCI 32-bit bus as specified in the PCI Rev 2.0 specification. All of the required signals for a PCI master are supported by the device including SERR# and PERR#. The INTA# interrupt resource is also used. The AIC-7850 will operate up to the maximum 33 MHz PCI clock interface. The following diagrams illustrate the AIC-7850 interface with commercially available PCI chipsets. Note it is assumed that SCSI boot BIOS capability, if required, is integrated into the motherboard system BIOS.

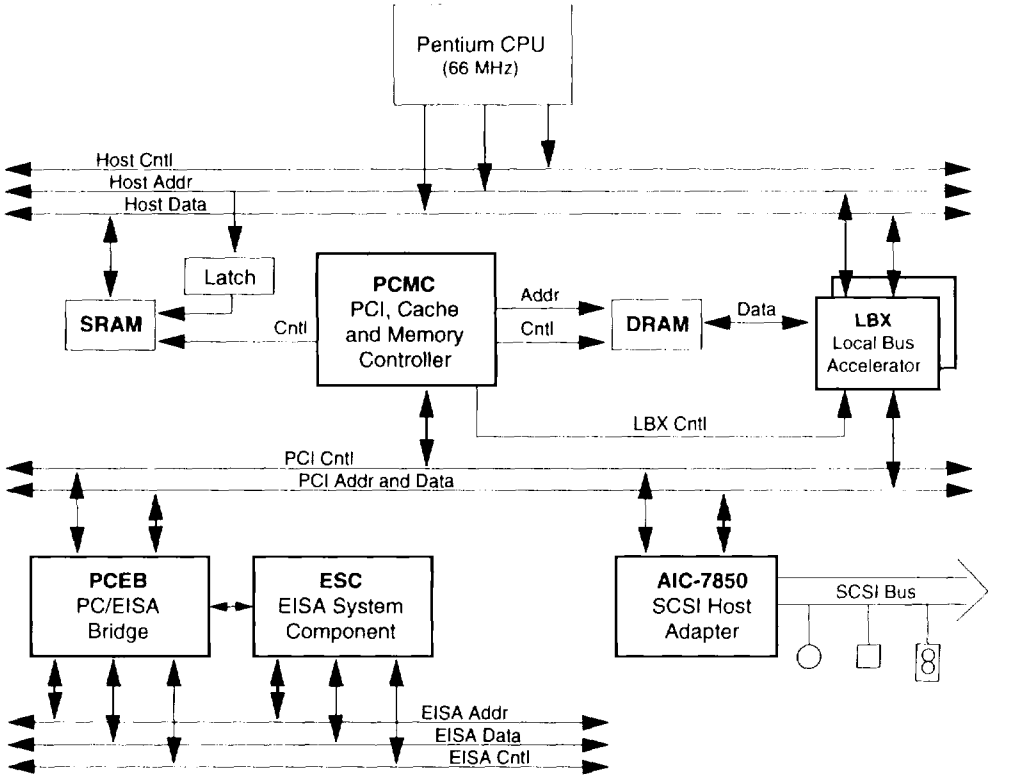
Interfacing the AIC-7850 to the Intel 82420 PCI Chipset



Interfacing the AIC-7850 to the Intel 82430 PCI Chipset (ISA Version)



Interfacing the AIC-7850 to the Intel 82430 PCI Chipset (EISA Version)



2 Architectural Overview

About This Chapter

Read this chapter to find out

- An architectural and operational overview of the AIC-7850
- An overview of the clocking and reset operations of the AIC-7850
- The AIC-7850 power connection and decoupling arrangement

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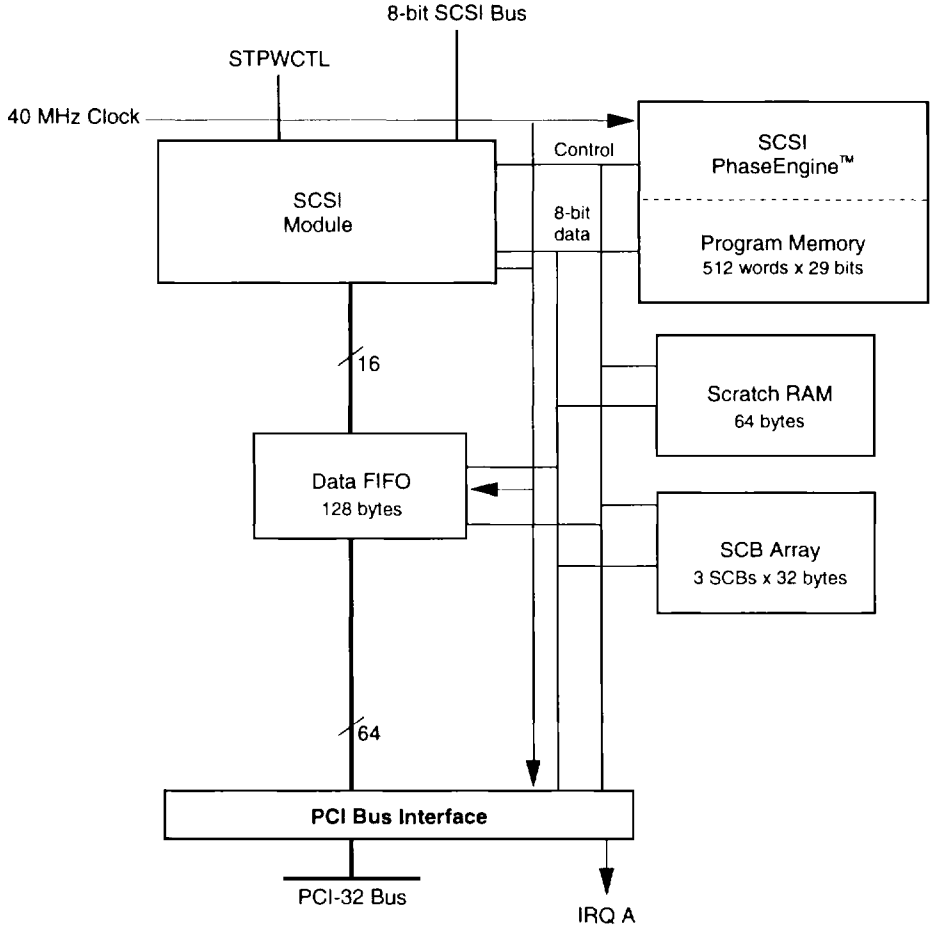
AIC-7850 Block Diagram

The AIC-7850, like the AIC-7870, is based on the original Adaptec AIC-7770 architecture using modified versions of the SCSI PhaseEngine, data FIFO, and SCSI controller combined with a totally new host interface. This architecture allows a host CPU to totally off-load a SCSI I/O operation to the AIC-7850 with no significant impact on system bus utilization.



The built-in SCSI PhaseEngine gives the AIC-7850 its own onboard processing intelligence. This allows it to off-load I/O from the host CPU and independently handle the entire data transfer operation. The SCSI PhaseEngine is programmable and uses its own self-contained microcode program which is downloaded to the AIC-7850 by the host at initialization. In operation, the host processor initiates an I/O service by downloading a SCSI Command Block (SCB) to the AIC-7850. The SCB contains all the information needed by the AIC-7850 to independently execute the entire SCSI operation. With SCB swapping software, up to 255 commands may be active in the ACI-7850 at once. The

AIC-7850 supports a 33 MHz PCI-32 interface directly. To maximize bus usage, the AIC-7850 features a 128 byte data FIFO organized as 16 Quad words.

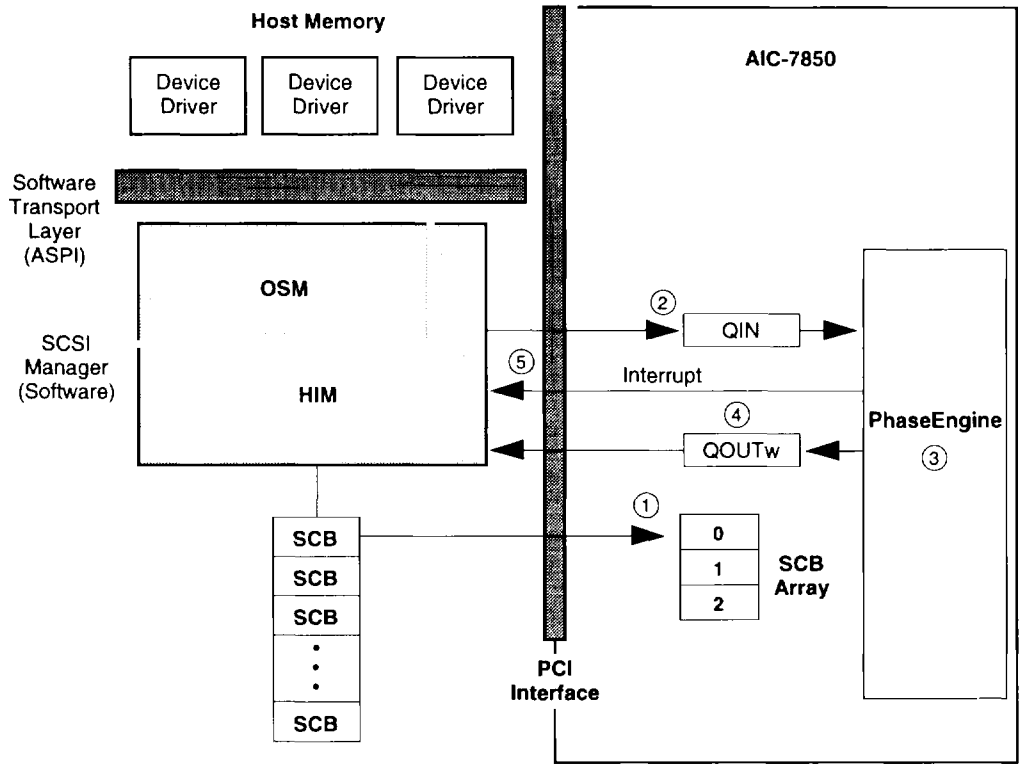
The AIC-7850 SCSI controller features an 8-bit bus. In addition, a control output is available to turn SCSI bus terminators off and on.

Operations Overview

The host initiates a SCSI I/O operation with the AIC-7850 by downloading a data structure called an SCB (SCSI Command Block). The SCB contains enough information for the AIC-7850 to independently carry out the requested SCSI operation. The AIC-7850 is code compatible with the AIC-7870 and runs with AIC-7870 software drivers. Full details of the AIC-7850/AIC-7870 software support will be presented later in this manual, but as illustrated here, a layered software architecture is utilized.

The SCSI manager is a software module which handles all software interface to the AIC-7850. The SCSI manager is made up of an Operating System Module (OSM) and Hardware Interface Module (HIM). The OSM contains code that is specific to the operating system being used and has no knowledge of the physical hardware details. The HIM handles all hardware operations and presents a generic interface to the OSM. As a fundamental building block of all AIC-7850/AIC-7870 software, the HIM is used in all Adaptec AIC-7870 software drivers and is available for use in software development for non-Adaptec supported operating systems.

SCSI SCBs are passed to the HIM by the OSM which in turn are sent to the AIC-7850 for execution. The HIM can manage as many SCB's as it has memory allocated by the OSM. There can be up to 255 simultaneously active SCSI commands through SCB swapping.



The typical sequence which the HIM uses to start a new SCB in the AIC-7850 is as follows:

1 An SCB is downloaded by the HIM.

2 A pointer to the SCB just loaded is posted into the QINFIFO.

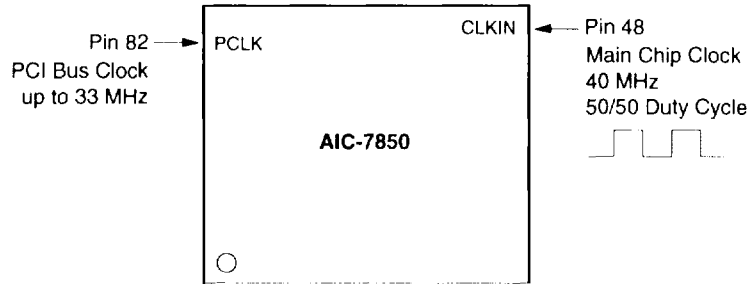
3 As part of its scanning operation, the PhaseEngine checks the QINFIFO for new SCBs and finds the one just posted.

4 Upon SCB completion, the PhaseEngine posts the pointer of the completed SCB into the QOUTFIFO.

5 The PhaseEngine interrupts the HIM to report a completed SCB without pausing and checks the QINFIFO for any new SCBs.

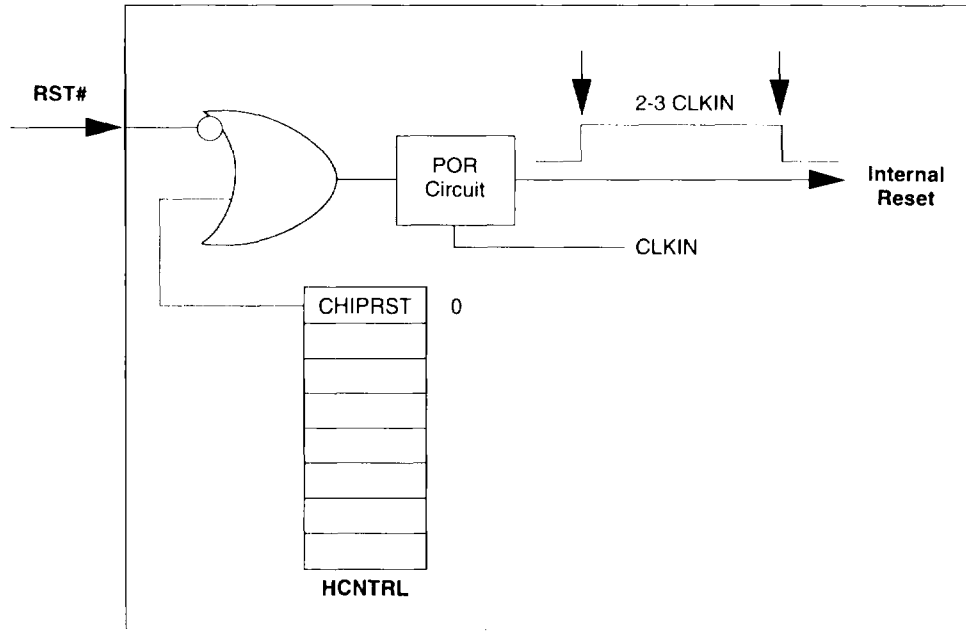
Clocking

The main clocking source for the AIC-7850 comes from the 40 MHz input on pin 48, CLKIN. This clock should have a 50/50 duty cycle. Slight variations of the 40 MHz frequency may be used, although chip timings will change proportionally. The chip also takes in the PCI bus clock for bus synchronization and can work with up to a 33 MHz PCI CLK.



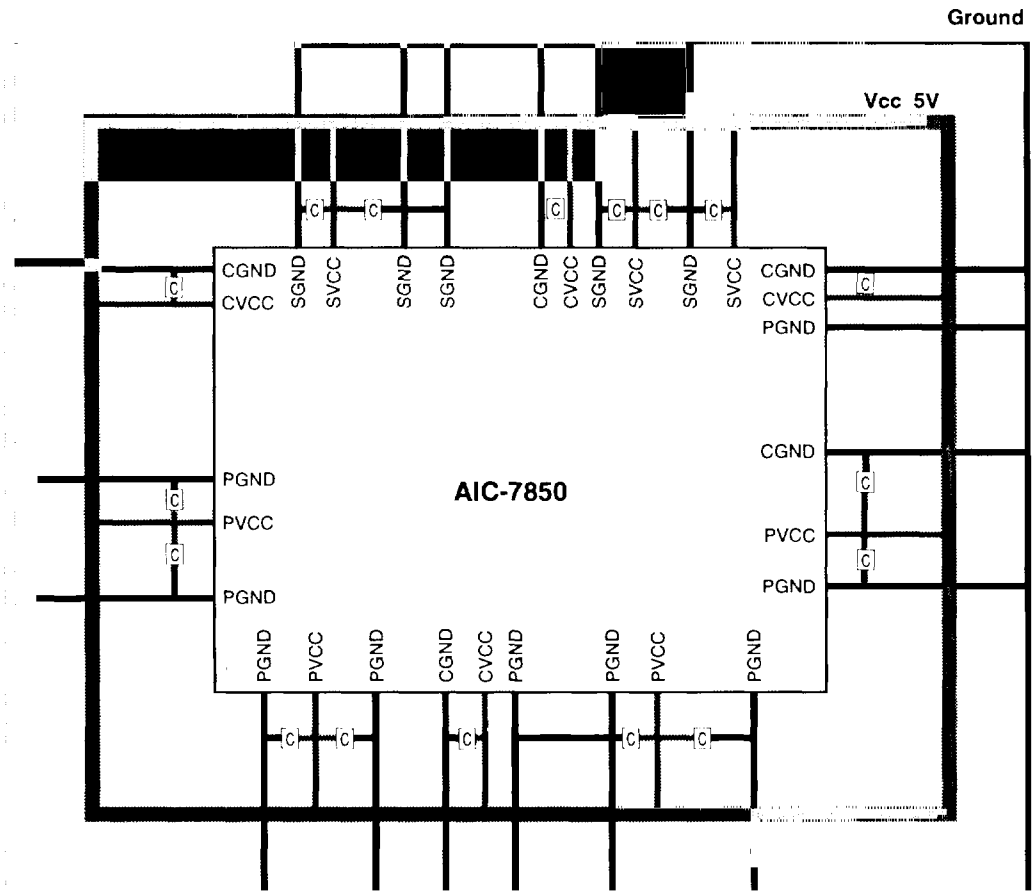
Reset Operations

The entire AIC-7850 is externally reset through an active low on the PCI RST# pin. All of the logic in the device, with the exception of the PCI configuration space, can also be software reset by writing a one to the CHIPRST bit in the HCNTRL register. Either reset condition activates an internal POR circuit which generates a minimum 2-3 chip clock reset pulse to the entire chip regardless of the duration of the reset input. In addition to being synchronized with the CLKIN, resets to the PCI configuration space are also synchronized with the PCI bus PCLK.



Power Connection and Decoupling

The AIC-7850 utilizes 30 Vcc and ground connections organized into three different power nets. The different power nets are core logic, PCI bus and SCSI bus. To avoid coupling signals from bus-to-bus, the nets are *not* internally connected to each other. It is required that the grounds of the different nets be externally connected to the same ground potential, typically to the same ground plane. The Vcc and ground connections of each net should be decoupled from each other to maintain signal stability on that net. Shown below is a minimal decoupling arrangement, however, many decoupling arrangements are possible depending on the specific implementation.



CGND = Core Logic GND
CVCC = Core Logic Vcc

SGND = SCSI GND
SVCC = SCSI Vcc

PGNC = PCI GND
PVCC = PCI Vcc

3 Architectural Details

About This Chapter

Read this chapter to find out

- Information regarding the PCI interface, SCSI interface and PhaseEngine of the AIC-7850
- Host data FIFO operations and status indicators

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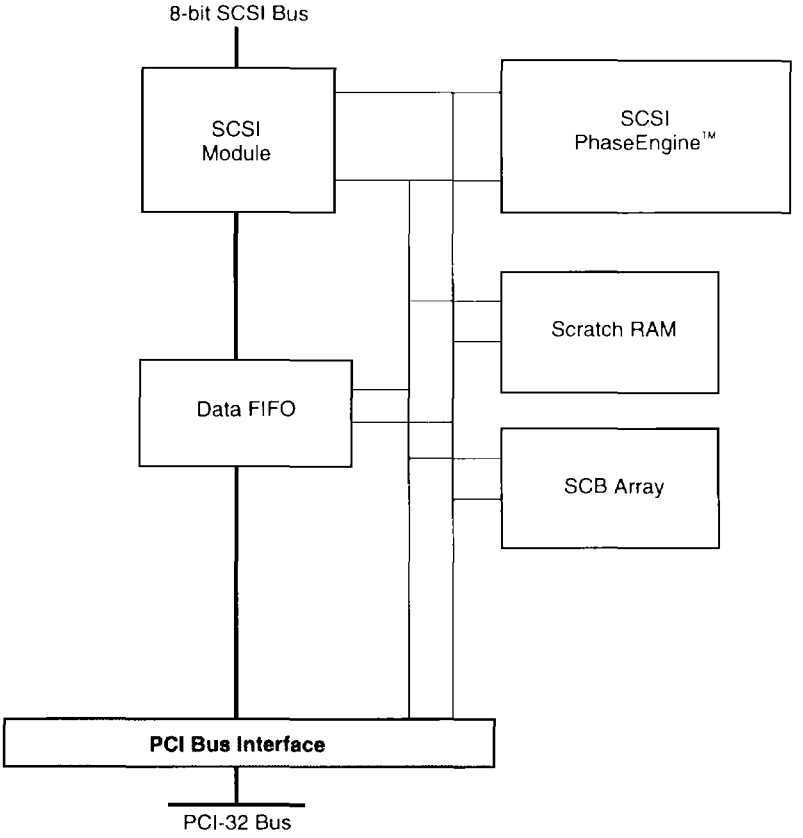
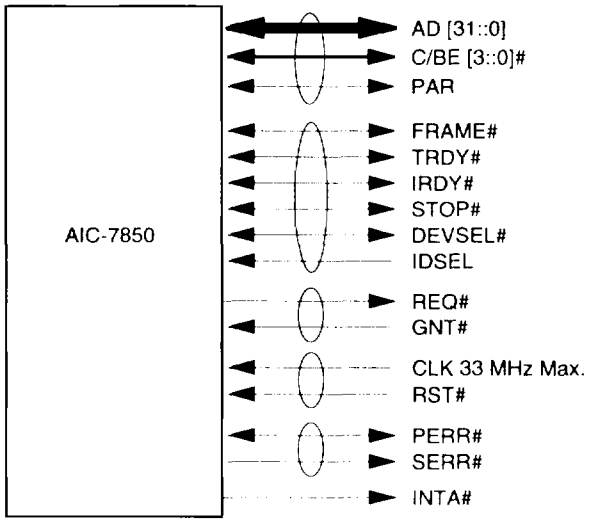
PCI Interface

The AIC-7850 connects directly to the PCI 32-bit bus as a bus master and slave with no additional logic required. It can work at the full 33 MHz PCI clock rate and will support data bursts up to the 133 MByte/sec 32-bit burst rate.



PCI Signals

The AIC-7850 supports all of the required PCI-32 signals including the newly mandatory PERR# and SERR# functions. Full PCI parity is maintained on the entire data path through the chip. The device also takes advantage of the INTA# resource to operate.



Supported PCI Bus Commands

The AIC-7850 PCI slave interface supports the required I/O, Memory and Configuration Read/Write commands. It also supports the following commands for enhanced system cache management:

- Memory Read Multiple
- Memory Read Line default to Memory Read command
- Memory Write and Invalidate default to Memory Write command

The AIC-7850 PCI master interface supports Memory Read and Memory Write commands for transferring data between system memory and the AIC-7850 data FIFO.

The extended memory commands (Memory Read Multiple, Memory Read Line, and Memory Write and Invalidate) are supported and work in conjunction with the Cache Line Size register to give the system cache controller advance knowledge of the minimum amount of data to expect for the transfer. The decision to use either the Memory Read Line or Memory Read Multiple command for Cache Line Transfers is determined by the CACHETHEN bit in the DSCOMMAND register.

		AIC-7850 Support	
C/BE# [3:0]	Command Type	Target	Master
0000	Interrupt Acknowledge	No	No
0001	Special Cycle	No	No
0010	I/O Read	Yes	No
0011	I/O Write	Yes	No
0100	Reserved	No	No
0101	Reserved	No	No
0110	Memory Read	Yes	Yes
0111	Memory Write	Yes	Yes
1000	Reserved	No	No
1001	Reserved	No	No
1010	Configuration Read	Yes	No
1011	Configuration Write	Yes	No
1100	Memory Read Multiple	**	Yes
1101	Dual Address Cycle	No	Yes
1110	Memory Read Line	**	Yes
1111	Memory Write and Invalidate	*	Yes

* Defaults to Memory Write
** Defaults to Memory Read

PCI Configuration Support

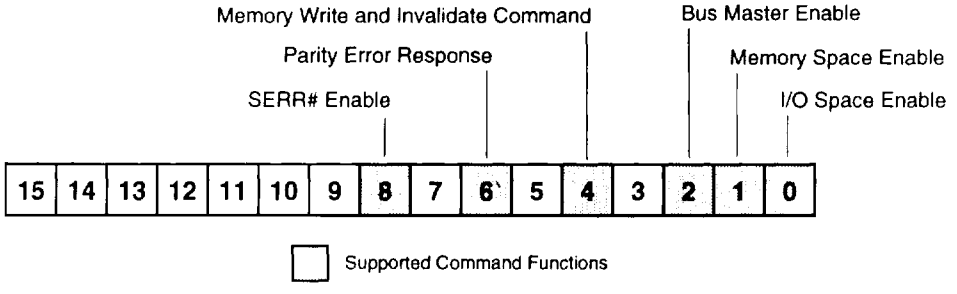
The AIC-7850 PCI interface supports the required 64-byte PCI configuration space header and also adds a DEVCONFIG control register at location 40h and DEVSTATUS status register at location 41h. The Adaptec registered PCI vendor ID is 9004h and the Adaptec device ID for the AIC-7850 is 7850h. The device uses a base class of 01h (mass storage controller) and subclass of 00h (SCSI bus controller). The AIC-7850 supports two base address registers in order to map its device space registers into both PCI I/O and memory address spaces. The chip contain a 256-byte Device register space for operation.

31 — 16	15 — 0	
Device ID **5078h**	Vendor ID **9004h**	00h
Status	Command	04h
Base Class **01h** / Subclass **00h**	Prog Interf **00h** / Revision ID **02h**	08h
N/A / Header Type **00h**	Lat Timer / Cache LS	0Ch
Base Address 0		10h
Base Address 1		14h
N/A		18h
N/A		1Ch
N/A		20h
N/A		24h
Reserved		28h
Reserved		2Ch
N/A		30h
Reserved		34h
Reserved		38h
Max_Lat **04h** / Min_Gnt **04h**	IRQ Pin **01h** / IRQ Line	3Ch
Reserved	DEVSTATUS / DEVCONFIG	40h

AD[10:08] Function Number = 0
AD[01:00] Config Type = 0

PCI Command Register

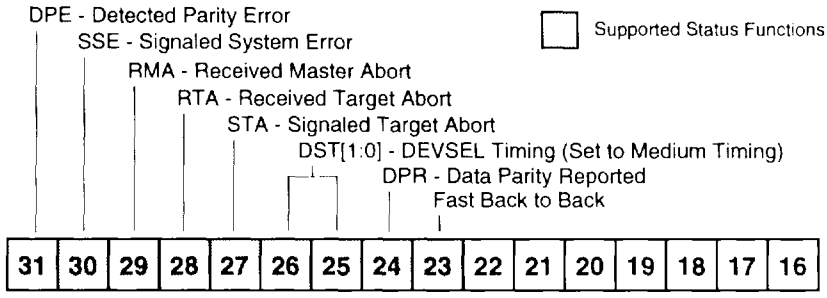
The AIC-7850 supports the PCI command register functions as indicated below.



PCI Configuration Space Offset 05:04h

PCI Status Register Functions Supported

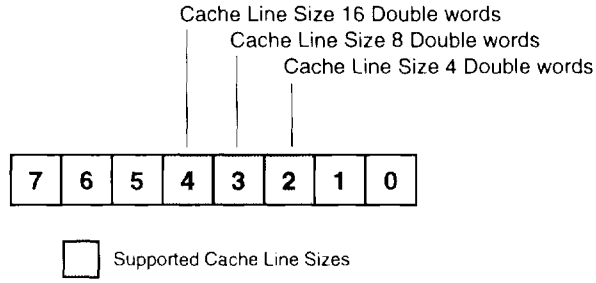
All of the defined PCI status indicators are supported and available in the AIC-7850. Several of the status functions are dually available from both the Configuration Status register and the PCISTATUS register mapped at the AIC-7850 Device register address M86h. This allows the controlling software to obtain PCI status without having to do a configuration access cycle.



PCI Configuration Space Offset 07:06h

Cache Line Size Register

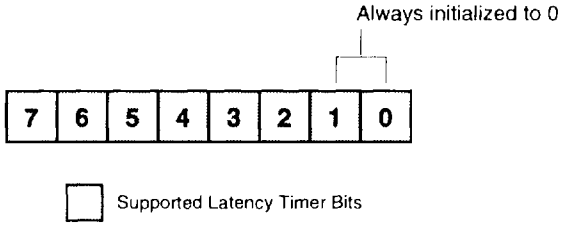
The Cache Line Size register is used in conjunction with the extended PCI bus memory commands: Memory Read Line, Memory Read Multiple, and Memory Write and Invalidate. The cache line size choices available are 4, 8, 16 double words.



PCI Configuration Space Offset 0Ch

Latency Timer

The Latency Timer register specifies in units of PCI bus clocks that a master may remain on the bus after it's GNT# has been deasserted. The timer is enabled with the clock that indicates the master FRAME# is asserted and is re-initialized when FRAME# is deasserted. The AIC-7850 Latency Timer may be initiated in increments of four PCI clocks.

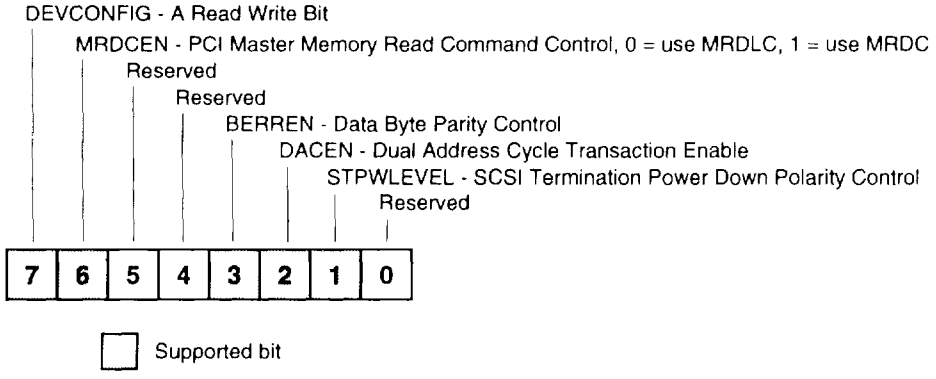


PCI Configuration Space Offset 0Dh

Device Specific Registers in PCI Configuration Space

To control chip specific functions, the AIC-7850 maps an 8-bit register at 40h in the PCI configuration space as shown below. Controlled in this register are configuration choices for AIC-7850 hardware features such as termination power-down control, memory port timing, data and SCB parity checking, and PCI memory cycle control.

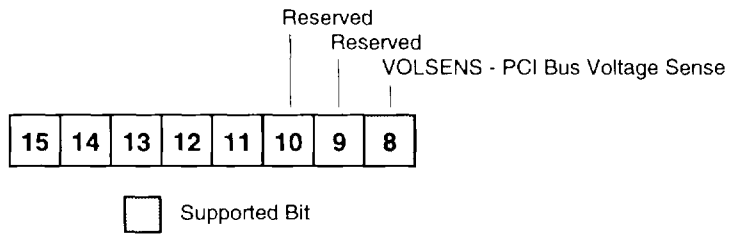
DEVCONFIG Register



PCI Configuration Space Offset 40h

A Status register called DEVSTATUS is located at 41h and reports the state of the signaling voltage being used on the PCI bus.

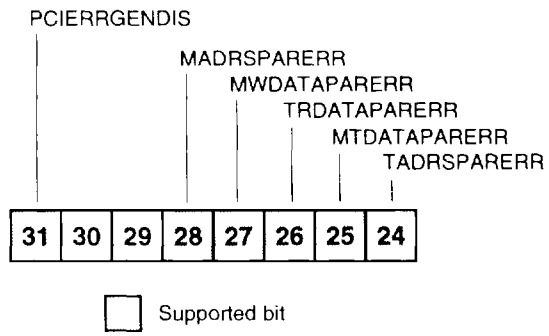
DEVSTATUS Register



PCI Configuration Space Offset 41h
Read Only

A PCI bus parity error generation register, PCIERRGEN is located at 43h which allows address or data parity errors to be generated for testing proper PCI bus components actions to these errors.

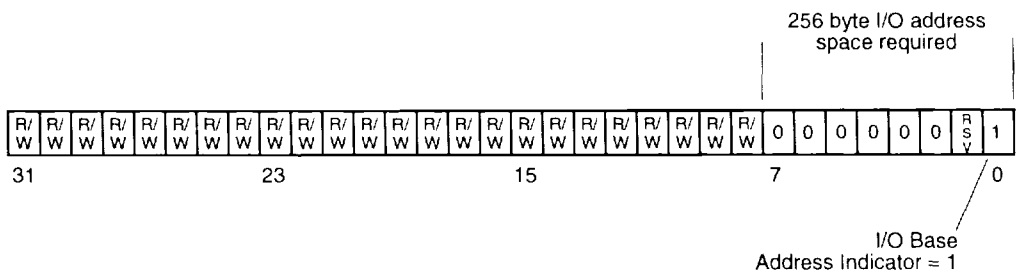
PCIERRGEN Register



PCI Configuration Space Offset 43h

Base Address Register (I/O)

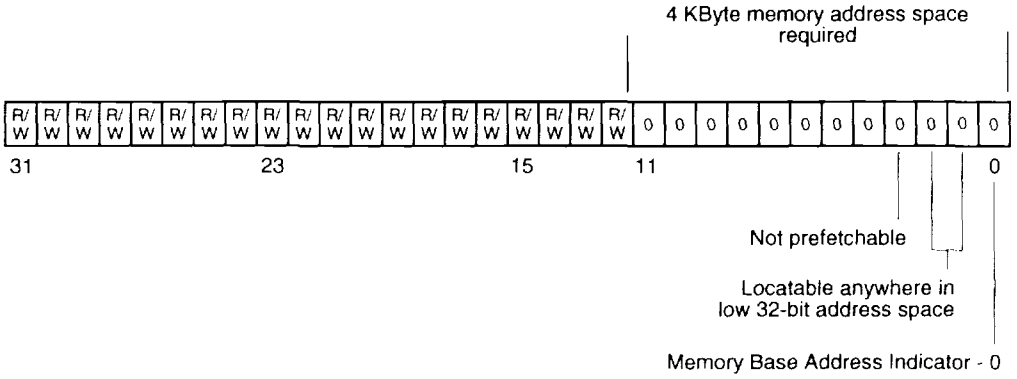
The AIC-7850 supports two PCI base address mapping registers, one for I/O space mapping and one for memory space mapping of its control register set. The same set of AIC-7850 device registers are accessible from either I/O or memory space. The AIC-7850 control register set occupies a 256-byte space which is requested through the PCI Base Address I/O register. The AIC-7850 may be located anywhere in low 32-bit I/O address space.



PCI Configuration Space Offset 10h

Base Address Register (Memory)

The same set of AIC-7850 device registers that are accessible through I/O space is accessible through memory space. The PCI Base Address (memory) register requests 4 KBytes of memory address space to be reserved for the AIC-7850. The AIC-7850 may be located anywhere in low 32-bit memory space.

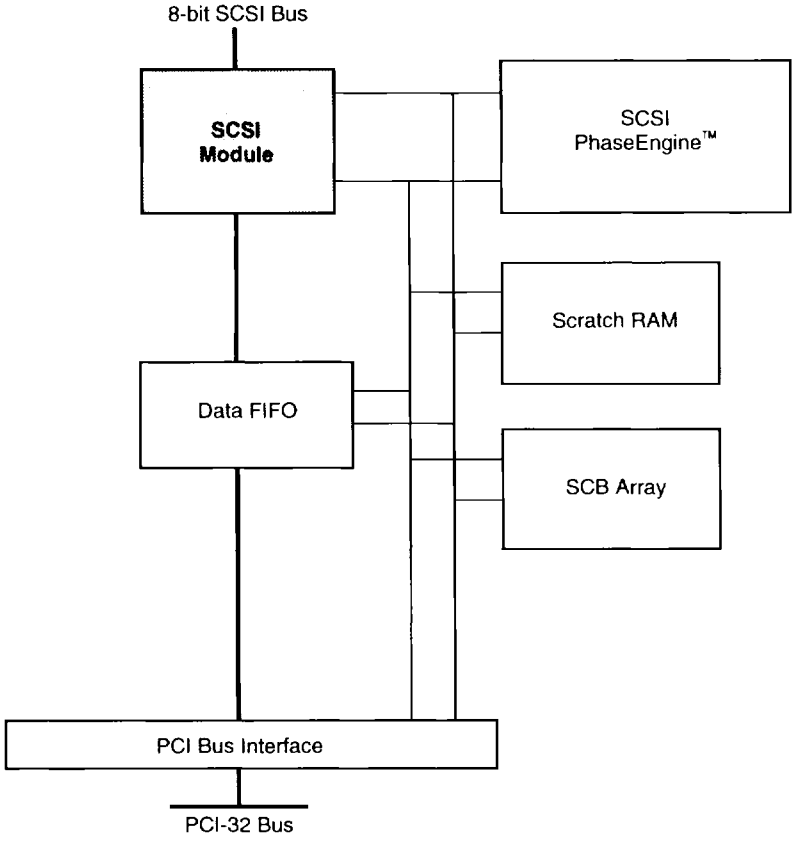


PCI Configuration Space Offset 14h

SCSI Interface

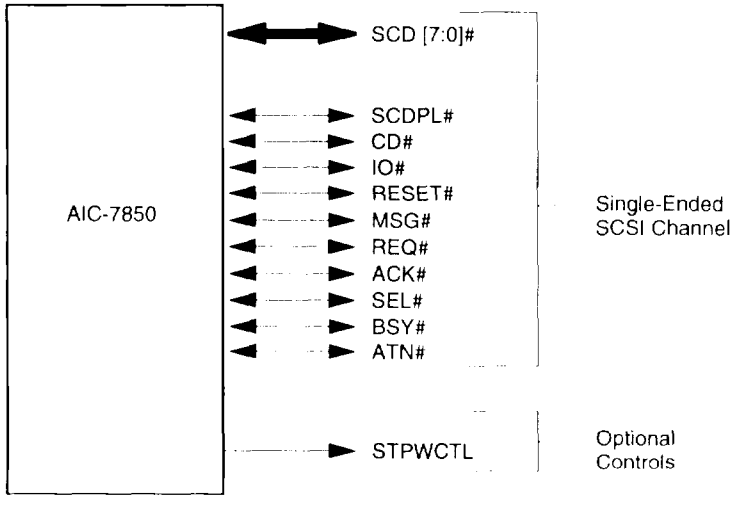
The AIC-7850 SCSI module is based on previously proven Adaptec SCSI core designs and offers 8-bit SCSI operation at 10 Mtransfers Fast SCSI rates. This gives data transfer rates of 10 MBytes/sec. The SCSI module also offers active negation outputs and a SCSI terminator power-down control. Active negation outputs help to reduce the chance of data errors by actively driving both polarities of the SCSI bus signal to avoid indeterminate voltage levels. The SCSI terminator power-down control is essential in power-sensitive systems to control power consumption of the SCSI terminators, which are the major power components in SCSI subsystems. The polarity of the power-down control is programmable in the DEVCONFIG register.

Synchronous SCSI offsets up to 15 REQs can be handled. The SCSI output drivers on the AIC-7850 can directly drive a 48 mA single-ended SCSI bus with no additional drivers.



SCSI Bus

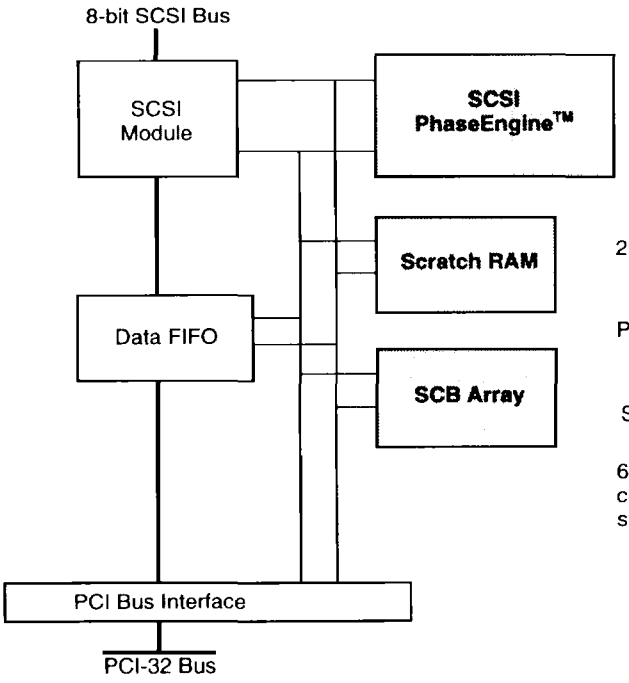
The AIC-7850 SCSI data bus is eight bits with odd parity generated. During chip power-down, all inputs are disabled to reduce power consumption.



The PhaseEngine

The AIC-7850 PhaseEngine comprises the on-chip intelligence that allows the AIC-7850 to execute the SCB commands sent to it. It is an Adaptec custom design specifically designed to handle SCSI bus phase operations. The PhaseEngine utilizes a loadable 2 KByte control store RAM which is microprogrammed by a software driver at initialization. The instruction word of the PhaseEngine is 29 bits wide with parity protection generated over individual bytes of the instruction word.

To provide storage for intermediate values and configuration parameters, the chip features a 64-byte general purpose scratch RAM with parity protection.



29-bit RISC based PhaseEngine
- 2 KBytes of microcode RAM
- Adaptec custom design

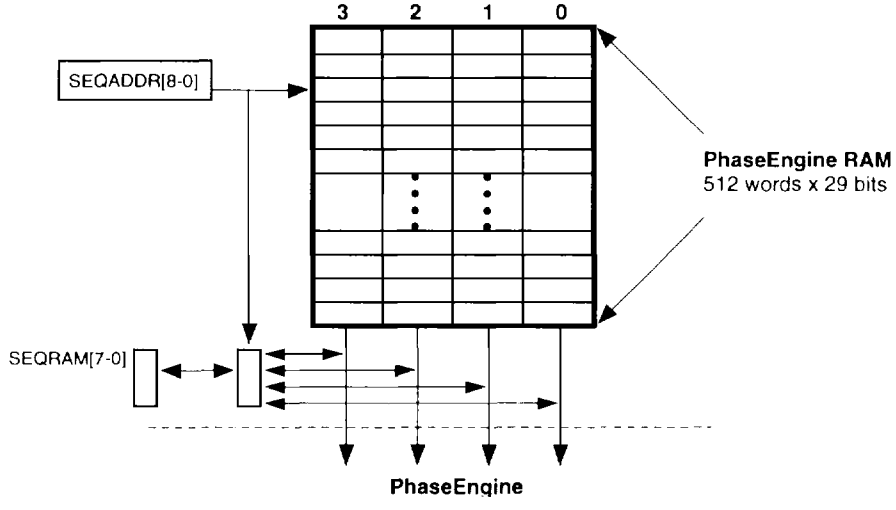
PhaseEngine Firmware
- Reduces SCSI overhead to 30 microseconds

SCB Array
- Three 32-byte SCSI control blocks

64-byte scratch RAM for storage of configuration information and working storage area.

PhaseEngine Program Loading

The microcode program which runs the AIC-7850 PhaseEngine is downloaded by the controlling driver software or BIOS at power-up initialization. The microprogram memory area consists of 512 words x 29 bits of SRAM storage. Individual bytes within each 29-bit word are parity protected. The microprogram is downloaded by first pausing or resetting the PhaseEngine, then setting the LOADRAM bit in SEQCTL. The starting PhaseEngine program word location is next set in the SEQADDR0 and SEQADDR1 registers respectively. Program bytes are then written to the SEQRAM register low byte first for each 29-bit word until the entire program is downloaded. SEQADDR will increment automatically for each new PhaseEngine word location.



PhaseEngine Instruction Set

The PhaseEngine utilizes a specialized instruction set (shown below) that compiles down to a single 29-bit word for each instruction. Each instruction carries with it the operation to be performed, and all operands required for the operation. Code compilation is performed using the *Microsoft ®Macro Assembler* with a special macro include file in which all PhaseEngine instructions are defined.

Move
- **mov** destination,source [ret]
- **mvi** destination,immediate [ret]

Logical
- **not** destination[,source] [ret]
- **and** destination, immediate/A [,source] [ret]
- **or** destination,immediate/A [,source] [ret]
- **xor** destination,immediate/A [,source] [ret]

Arithmetic
- **add** destination,immediate/A [,source] [ret]
- **adc** destination, immediate/A [,source] [ret]
- **inc** destination [,source] [ret]
- **xor** destination [,source] [ret]

Flag Operations
- **clc** [mov destination,immediate/A] [ret]
- **stc** [destination] [ret]

Shift, Rotates
- **shl** destination [,source], number [ret]
- **shr** destination [,source], number [ret]
- **rol** destination [,source], number [ret]
- **ror** destination [,source], number [ret]
- **rel** destination [,source] [ret]
- **xchng** destination [,source] [ret]

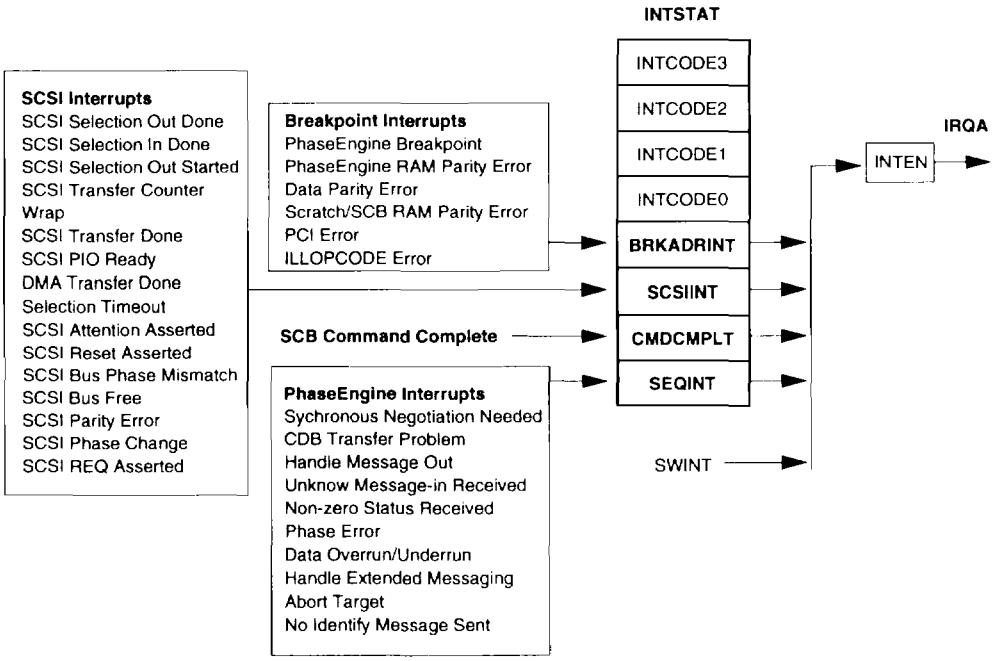
Branches
- **jmp/jc/jnc/call** address
- **mov** source **jmp/jc/jnc/call** address
- **mvi** source **jmp/jc/jnc/call** address
- **or** source immediate **jmp/jc/jnc/call** address
- **test** source immediate/A **jz/jnz** address
- **cmp** source,immediate/A **je/jne** address
- **ret**

Status and Interrupt Sources

A multitude of status and interrupt sources are available in the AIC-7850 to assist the driver software in controlling and managing SCSI operations. The many status and interrupt sources are used for four basic purposes:

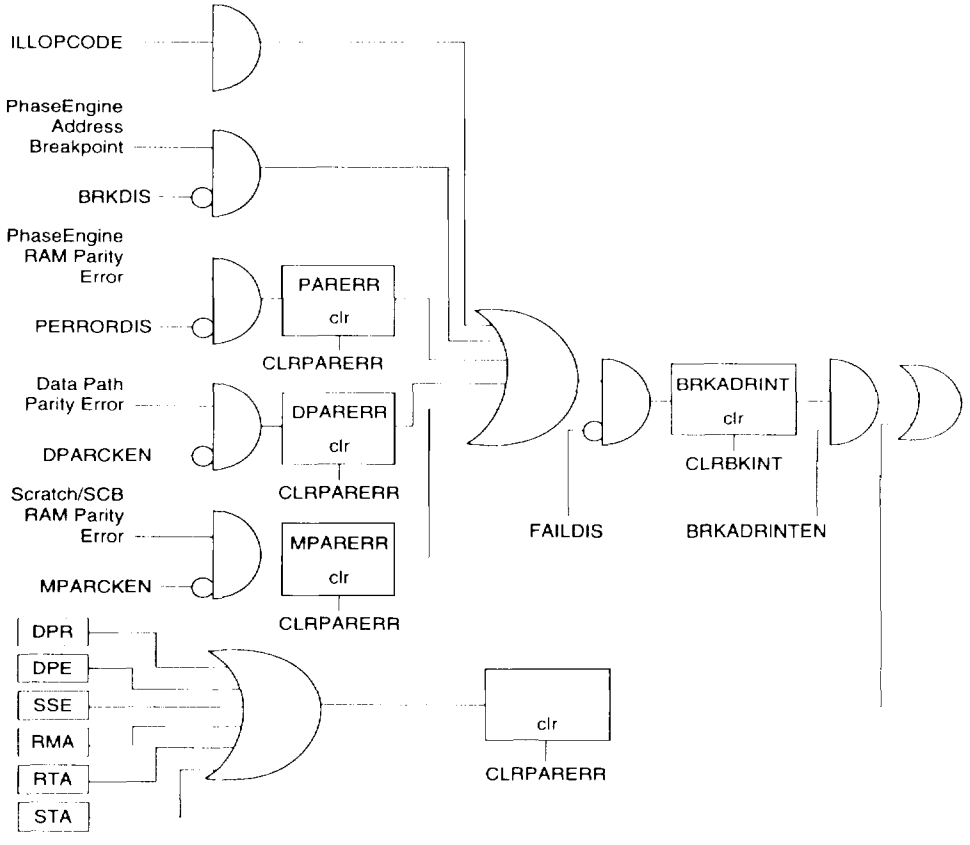
- Normal driver operations
- Necessary driver intervention in PhaseEngine operations
- Error condition posting
- Diagnostic test support

Interrupt sources from the various parts of the AIC-7850 are routed through the INTSTAT register, where their status may be read, then ultimately combined to drive the IRQA# pin if interrupts are enabled. The active logic level of the IRQA# signal is active low. The SEQINT reports conditions where host assistance is required to handle a SCSI bus condition. The exact help needed is coded into the INTCODE [3:0] bits in the upper part of the INSTAT register. CMDCMPLT reports the normal completion of a SCB sent down to the chip by the host driver software. SCSIINT reports an error or phase condition on the SCSI bus. Each of the SCSIINT sources may be individually enabled/disabled as necessary.



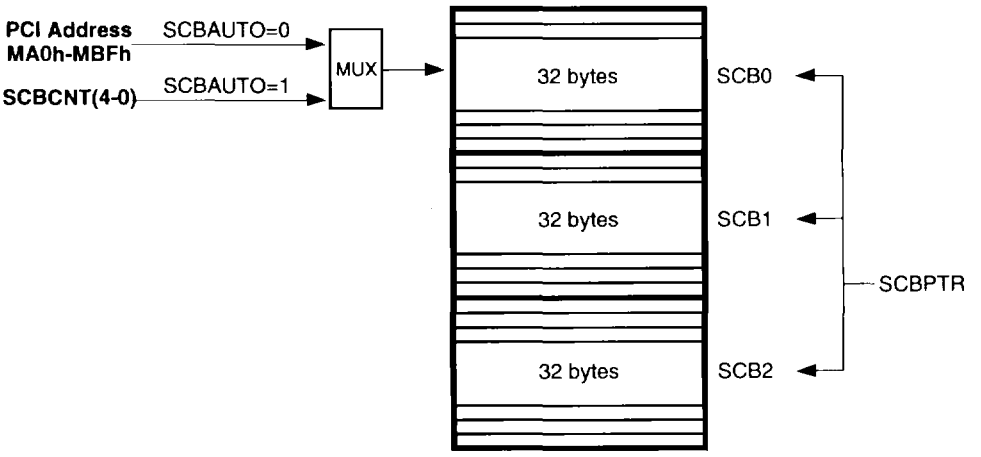
Parity and Error Checking

The BRKADRINT interrupt actually comprises several interrupt and status sources as illustrated below. During code debug and development work it reports attainment of a PhaseEngine breakpoint address. During normal operation it represents PhaseEngine or data path parity errors and PCI bus errors. Six of the PCI configuration status indicators are gated for interrupt generation. BRKADRINT is unique among the other interrupt sources in that it has multiple levels of enable/disable control.



Internal SCB Array

A SCSI I/O operation is started by downloading a 32-byte SCSI Command Block (SCB) to the AIC-7850. The SCB contains all of the information needed by the AIC-7850 to independently execute the requested I/O operation. Each SCB is stored in a separate RAM area in the chip with a particular SCB accessed by setting the SCBPTR. Each SCB byte may be individually addressed or, for the convenience of downloading an entire SCB, the autoincrementing pointer SCBCNT (4-0) may be used. When SCBAUTO is set to one, the AIC-7850 as slave supports Double word PCI Burst accesses to the SCB Array. Once a new SCB is started, it may be swapped out in order to allow other SCB's to be downloaded and started. Through swapping, up to 255 SCB's may be active on the SCSI bus simultaneously.



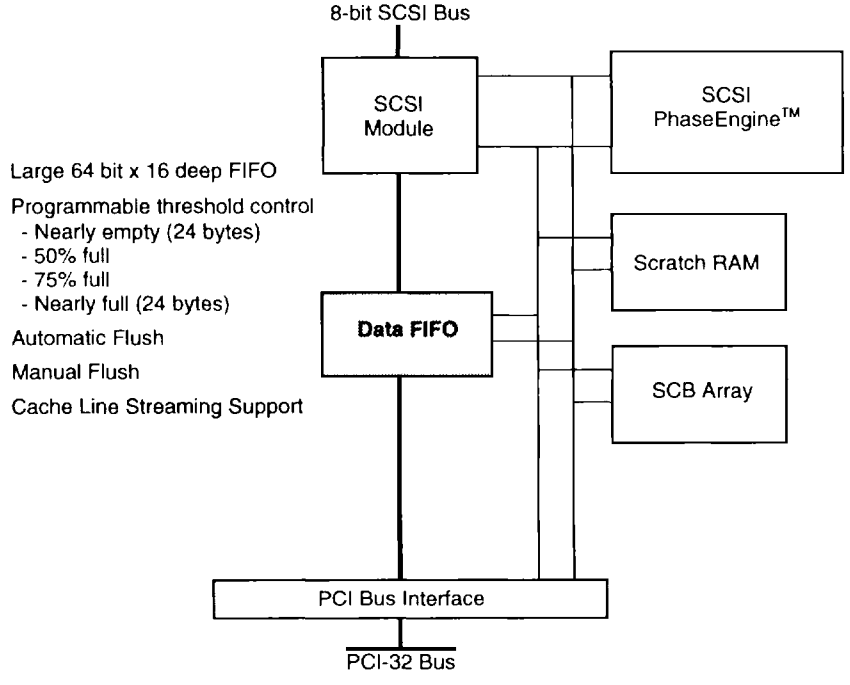
SCB Definition

SCBs are organized as 32-byte arrays with some fields having a dual usage depending upon whether the host software driver or PhaseEngine is looking at the SCB. In operation, the host software driver only sends the first 19 bytes of which only the first 12 bytes (0 through 11) are set by the driver. The last seven bytes (12 through 18) are only used by the PhaseEngine and are set to 0 for PhaseEngine convenience. All SCSI commands involving any data transfer are handled as a Scatter/Gather transfer, even though there may be only a few data bytes involved. For further information on the SCB fields, refer to the *HIM Technical Reference Manual*.

Offset	SCB Contents	# of Bytes
00	Control	1
	7 = Reject MDP message	
	6 = Disconnect Enable	
	5 = Tag Enable	
	4 = Reserved	
	3 = Waiting	
	2 = Disconnected	
	1,0 00 - Simple Queue	
	01 - Head of Queue	
	10 - Ordered Queue	
	11 - Illegal	
01	Target ID, Channel, LUN	1
02	Scatter/Gather Segment Count	1
03	Scatter/Gather List Pointer	4
07	SCSI Command Pointer	4
11	SCSI Command Length	1
12	Reserved	1
13	Reserved	1
14	Target Status	1
15	Residual Data Count	3
18	Residual Scatter/Gather Segment Count	1
19	Data Pointer	4
23	Data Count	3
26-31	Reserved	6

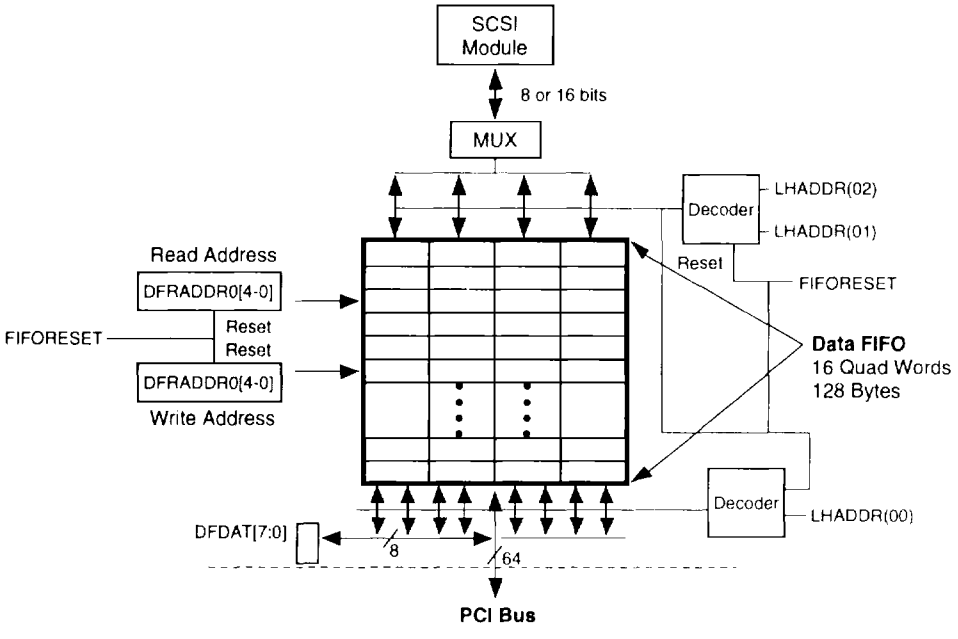
Host Data FIFO

The host data FIFO performs data buffering and speed matching between the SCSI module and the PCI bus interface. It is organized as 16 Quad words for 128 bytes total. Data through the FIFO and associated data paths is parity protected throughout its journey through the chip. The host FIFO control circuitry features programmable threshold control which allows the choice of a FIFO capacity trip point based on the relative speeds of the SCSI and PCI buses. This feature helps to maximize bus usage by keeping the AIC-7850 on the bus for the maximum period of time.



Data FIFO Operations

Data from the SCSI module is multiplexed into the FIFO data array to build the 64-bit Quad words. Along with the data bytes, parity is also passed along as the data is transferred. The host or AIC-7850 PhaseEngine can read or write individual bytes in the FIFO by setting either the DFRADDR0 or DFWADDR0 pointers into the array. Individual bytes in the FIFO array are selected by the lowest three bits of the host address register.



Data FIFO Threshold Control

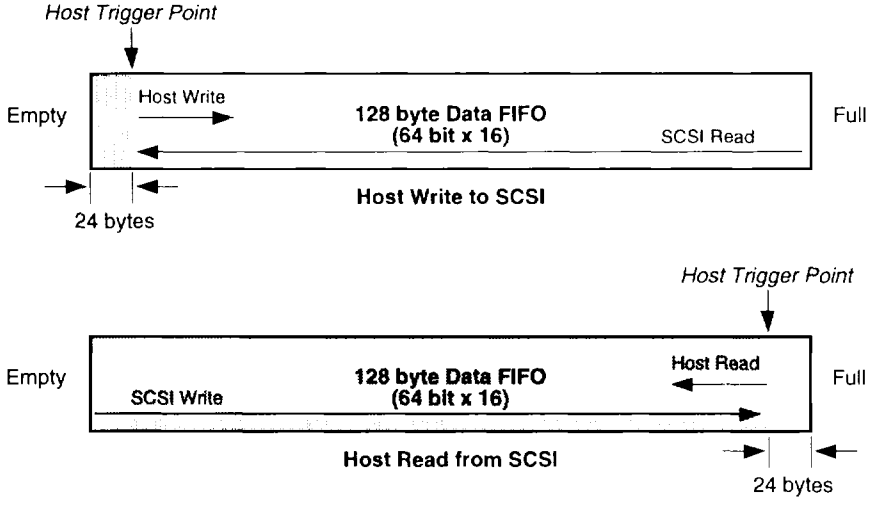
To maximize host and SCSI bus usage, the AIC-7850 features data FIFO controls and status indicators. Integrated with the AIC-7850 Bus Master DMA and SCSI control circuits, they allow maximum utilization of the host and SCSI buses based on the speed differential between the host and SCSI devices. These controls however, are only in effect when CACHETHEN is inactive. When CACHETHEN is active the host trigger points are:

- For SCSI Write, whenever space is available in the DFIFO for storage of a cache line of data.
- For SCSI Read, whenever a cache line of data is available in the DFIFO.

The PCI Cache Line Read command issued is Memory Read Multiple when CACHETHEN is inactive and Memory Read Line when CACHETHEN is active.

Since the PCI bus data transfer rate (133 MByte burst) is much faster than the SCSI bus transfer rate (10 MByte/sec), the thresholds shown here are used. On a write to the SCSI bus, the PCI bus master controller waits until the data FIFO is almost empty before arbitrating for the PCI bus and filling the data FIFO. Since the PCI bus can transfer data much faster than the SCSI bus, the FIFO eventually fills up and the PCI bus is relinquished. The reverse case is used on data reads from the SCSI bus.

Host Much Faster Than SCSI
DFTHRSH1 = 1, DFTHRSH0 = 1



4 How the AIC-7850 Works

About This Chapter

Read this chapter to find out

- The steps involved in the PhaseEngine process and execution
- How the AIC-7850 handles data transfers as Scatter/Gather operations

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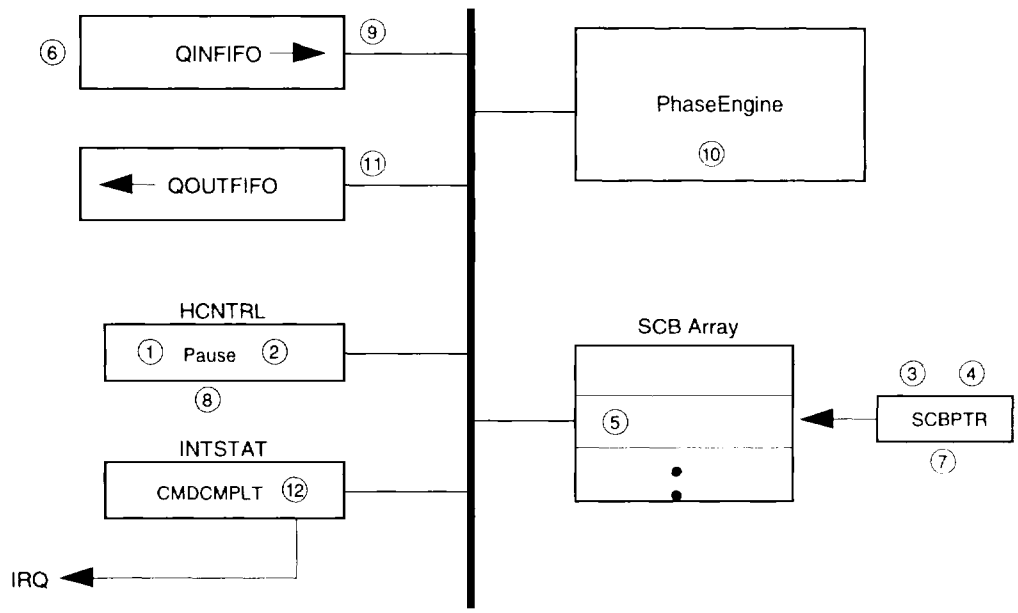
Starting a PhaseEngine SCB

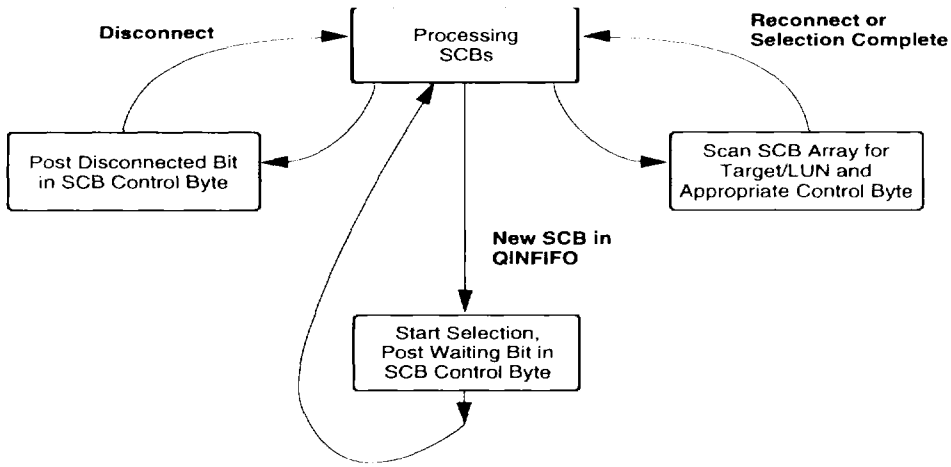


A detailed sequence of the steps involved when starting a new SCB are as follows:

1. Host saves the current value in SCBPTR for later restoration.
2. Host sets SCBPTR with the SCB to load.
3. Host downloads an SCB.
4. Host posts the pointer of the SCB just loaded into the QINFIFO.
5. Host restores the SCBPTR in preparation for starting up the PhaseEngine.
6. As part of its scanning operation, the PhaseEngine checks the QINFIFO for new SCBs and finds the one just posted.
7. Phase Engine executes the new SCB.
8. Upon SCB completion, the PhaseEngine posts the SCB pointer to the QOUTFIFO.
9. PhaseEngine posts the CMDCMPLT bit in INTSTAT to interrupt the host.

PhaseEngine SCB Processing

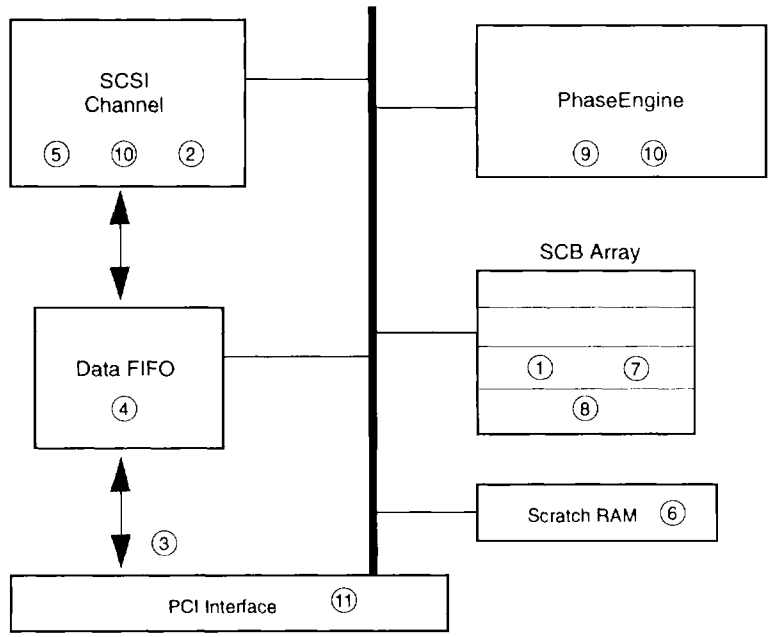
The AIC-7850 PhaseEngine processes SCBs in the order they are received with new SCBs being started when older SCB operations are idle due to wait for selection or a SCSI bus disconnect. When operations for an idled SCB reactivate, the PhaseEngine scans the SCB array for the SCB corresponding to the Target/LUN reactivating. Upon finding it, the PhaseEngine restarts operations until the next disconnect or SCB completion.



SCBs in progress may be aborted by removing their status identifiers when they are idle (waiting for selection or reconnection) so that the PhaseEngine will not find them when the operation restarts. In this abnormal condition, the PhaseEngine generates an interrupt back to the host to handle this situation which the host originally created. To abort an active SCB, the host can manually raise the SCSI bus attention line to cause the PhaseEngine to see an abnormal SCSI bus condition and generate an interrupt back to the host.

PhaseEngine SCB Execution

After being passed a new SCB, the AIC-7850 PhaseEngine begins working on the SCB at its next opportunity. The basic steps involved in SCB execution are described below:



1 As soon as the PhaseEngine frees up from working on other SCBs, it begins execution of a new SCB. Other SCBs that were being worked on may merely be disconnected.

2 Using the target information in the SCB, the PhaseEngine has the SCSI channel arbitrate for the bus and select the specified target.

3 When selection completes, the PhaseEngine has the host interface use the SCSI command pointers in the SCB to DMA the SCSI command from host memory directly out to the target.

4 In preparation for the upcoming data transfer, the PhaseEngine has the host interface use the Scatter/Gather list pointers in the SCB to DMA in the segment pointer information. The pointers are used to set up the transfer control registers in preparation for data transfer.

5 The target changes to Data phase and DMA data transfer begins.

6 As the transfer progresses, the temporary Scatter/Gather pointers in scratch RAM are updated to the next segments in the list.

7 When the target disconnects, the PhaseEngine saves the residual data pointers and transfer counts back in the SCB to await reconnection.

8 With the target disconnected, the PhaseEngine starts or continues a new SCB.

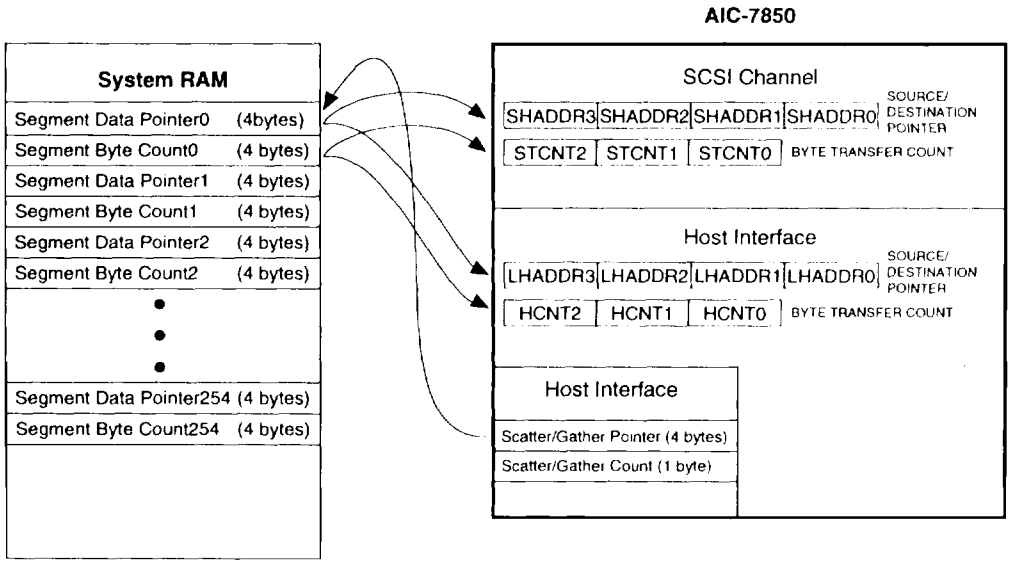
9 With the target(s) disconnected and no new SCB to work on, the PhaseEngine goes to sleep.

10 When the target reconnects, the PhaseEngine wakes up, restores pointers and continues the transfer where it left off. Alternately, when a new SCB is posted by the driver, the PhaseEngine wakes up and starts processing it.

11 Upon command completion, the PhaseEngine posts the finished SCB in the QOUTFIFO and interrupts the host.

Scatter/Gather Operations

The AIC-7850 handles all data transfers as Scatter/Gather operations even though only a few bytes may need to be transferred. To do a multisegment transfer, the host driver first builds a Scatter/Gather list in system memory. It then passes a pointer to the start of the list and a segment count to the AIC-7850 in the SCB. When executing the Scatter/Gather operation, the AIC-7850 fetches the information for each segment in sequence from the list in system memory and loads it into its host interface and SCSI channel control registers for transfer operations. As each Scatter/Gather segment is completed, the next segment in the list is automatically fetched until the segment count goes to zero. Using an 8-bit segment counter, up to 255 segment Scatter/Gather operations may be performed. For more information on Scatter/Gather list format and SCB operation refer to the *HIM Technical Reference Manual*.



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5 AIC-7850 Power Management

About This Chapter

Read this chapter to find out

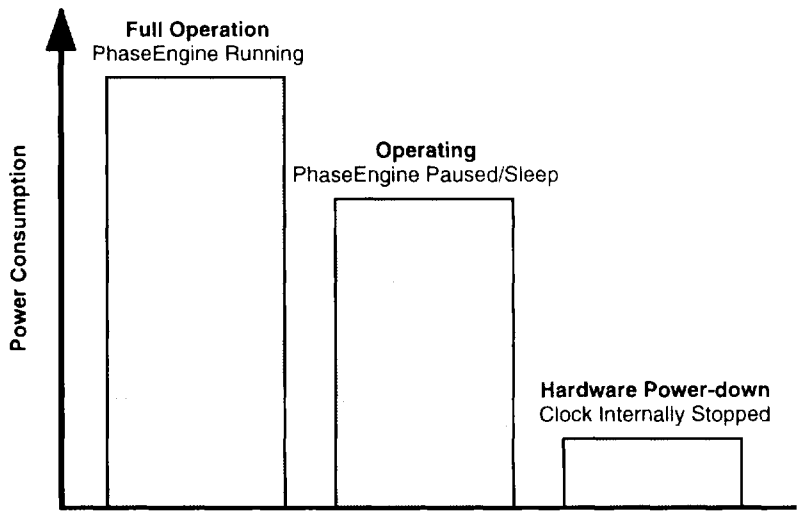
- The power management of the AIC-7850
- The Hardware Power-down Mode for the AIC-7850

▼▼▼▼▼ 5

Power Consumption Operating Modes

The AIC-7850 features mechanisms to control the power consumption of itself and the SCSI bus termination in a system. SCSI bus termination is controlled through a control output called STPWCTL which is used to enable or disable monolithic active terminators. An application of this feature is shown later in a discussion of active terminators.

The AIC-7850 features power management with three levels of *decreasing* power consumption. The highest level of power consumption is when the device is in full operation with the on-board PhaseEngine running. When the PhaseEngine is in Pause Mode or Sleep, Power Mode consumption decreases since the PhaseEngine's 2 KByte memory and internal dual I/O bus are no longer in operation. In Pause Mode, the AIC-7850 responds to SCSI bus conditions, such as a reset, by generating interrupts back to the host system with the host driver restarting the PhaseEngine after servicing the interrupt. The lowest power consumption occurs when the clock is completely stopped to the device.

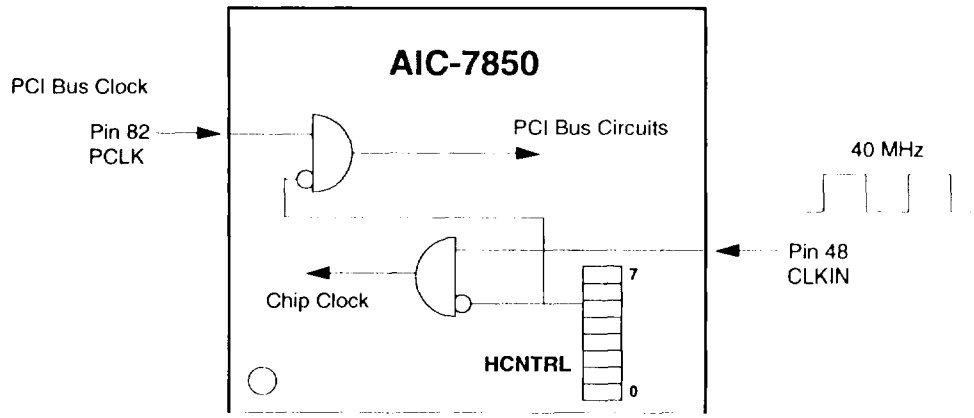


The PhaseEngine may place itself into Sleep Mode only when it is cycling in the idle portion of it's instruction loop waiting for a SCSI phase change, a DMADONE status or a new SCB posting. When one of these occur, the PhaseEngine will wake up and begin processing the condition without interrupting the host driver.

AIC-7850 Hardware Power-down

In Hardware Power-down Mode, the clock is stopped to most of the chip circuits with only a small leakage current left flowing. In this mode, the device is completely asleep and oblivious to anything happening around it, with the exception of responding to accesses for PCI configuration space ID and hardware power-down control.

The AIC-7850 Hardware Power-down Mode achieves power savings by turning off the clock to a majority of the chip circuits. While powered down, no operations may be performed, although the host can still read and write the PCI configuration registers, device ID, and host control register. Power-down is entered/exited by writing bit 6, POWRDN, of the Host Control register (M87H); however, in order to do this, the PhaseEngine must be paused by setting PAUSEACK = 1.



6 AIC-7850 Motherboard Layout

About This Chapter

Read this chapter to find out

- The footprint of the AIC-7850 package
- SCSI design requirements when cabling to target peripherals and laying out PC boards
- SCSI termination methods and cable impedance requirements
- PCI design requirements for layout to PCI Bus

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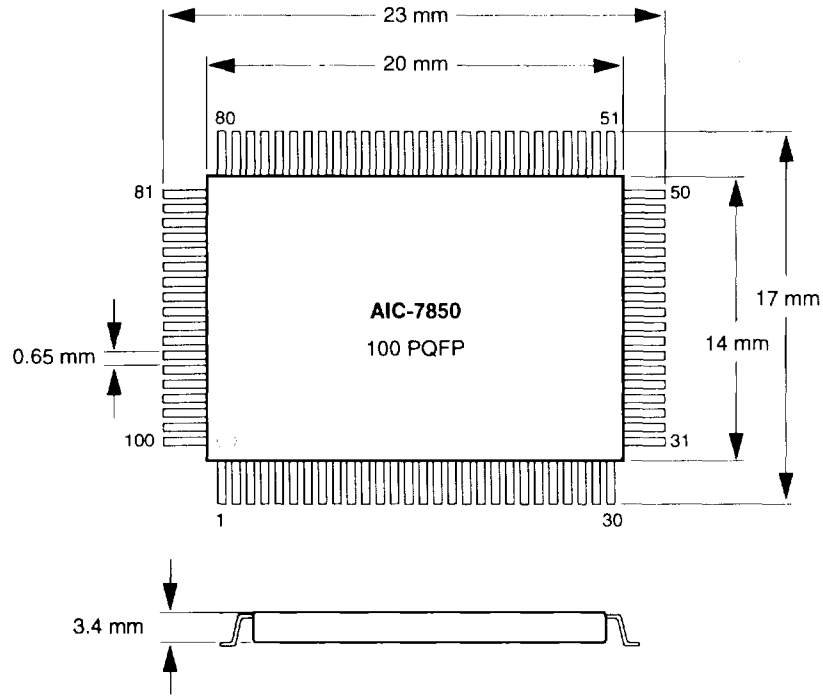
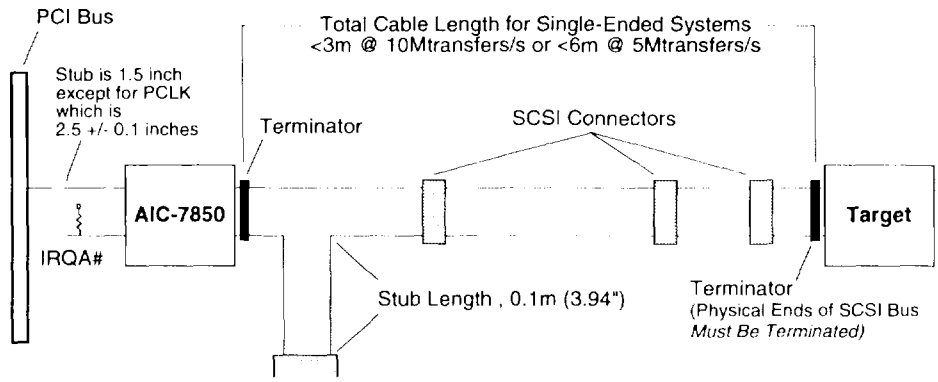
Footprint on the Motherboard

The AIC-7850 comes in a 20 x 14 mm, 100-pin Plastic Flat Pack. The height of the package is only 3.4 mm.



SCSI-3 Cabling and PC Board Layout Requirements

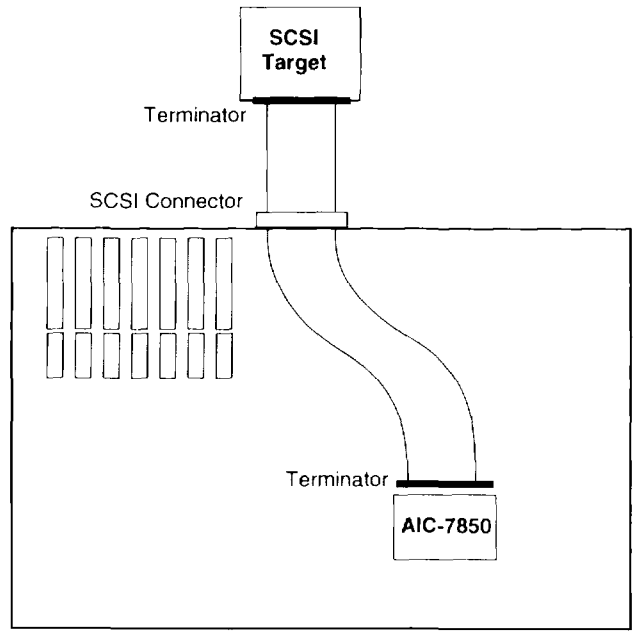
The layout and routing of SCSI circuits on motherboards are controlled by the SCSI specification requirements for cabling and termination as shown below. SCSI designs must follow these requirements both when cabling to target peripherals and laying out PC boards.



Motherboard Layout With External SCSI Targets Only

The simplest motherboard and cabling situation is where there are only external SCSI targets. In this situation, the AIC-7850 will always be the physical end of the cable so a permanently installed terminator can be placed next to the chip. The AIC-7850 may be located anywhere on the motherboard since it forms one physical end of the SCSI cable. However, for best results, it should be located as close to the rear SCSI connector as possible, in order to minimize cabling losses and impedance discontinuities.

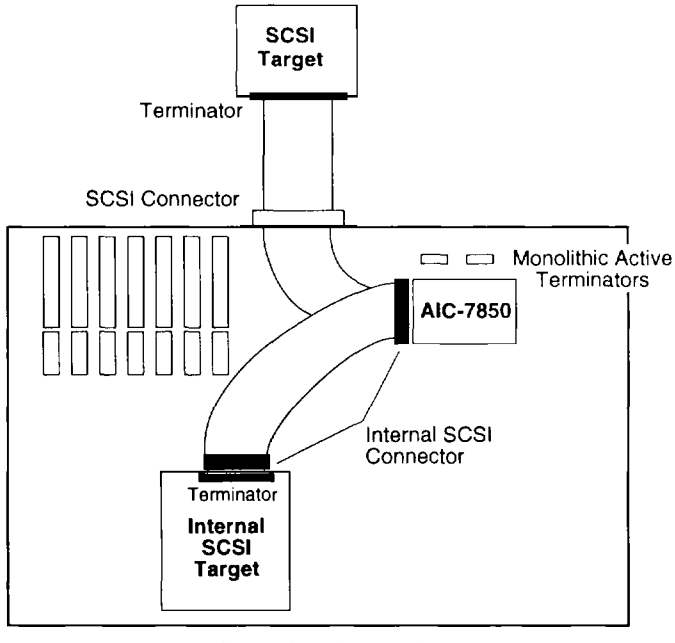
The external SCSI target and terminator will lie at the other physical end of the cable.



Front of Motherboard

Motherboard Layout With Internal SCSI Targets

The more difficult motherboard layout problem involves the situation where there are both internal and external terminators. In this system there are internal SCSI targets which would typically lie at one physical end of the SCSI cable and have to be terminated as shown. Internally, 50-conductor ribbon cable is usually used for SCSI cabling. Since the AIC-7850 may or may not be the other physical end of the SCSI cable, it needs to be easily terminated or unterminated. The simplest solution to this is to use monolithic SCSI active terminator chips with enable/disable controls. This allows the AIC-7850 to be located anywhere on the motherboard with its terminators enabled or disabled with a jumper, switch, or software control. To satisfy stub length requirements when no external targets are attached, the AIC-7850 should be within 0.1 meters of the rear SCSI connector.

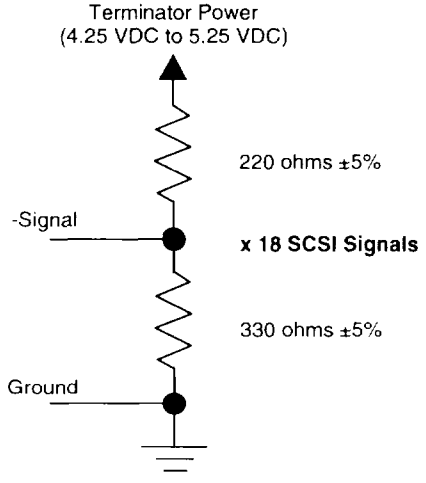


SCSI Terminators

SCSI uses open-collector drivers to implement WIRE-OR logic on the SCSI bus. This requires the use of terminators on the ends of the bus to set the logic high voltage level and match cable impedance. Two termination methods are described in the SCSI specification — passive and active.

Passive SCSI Terminators

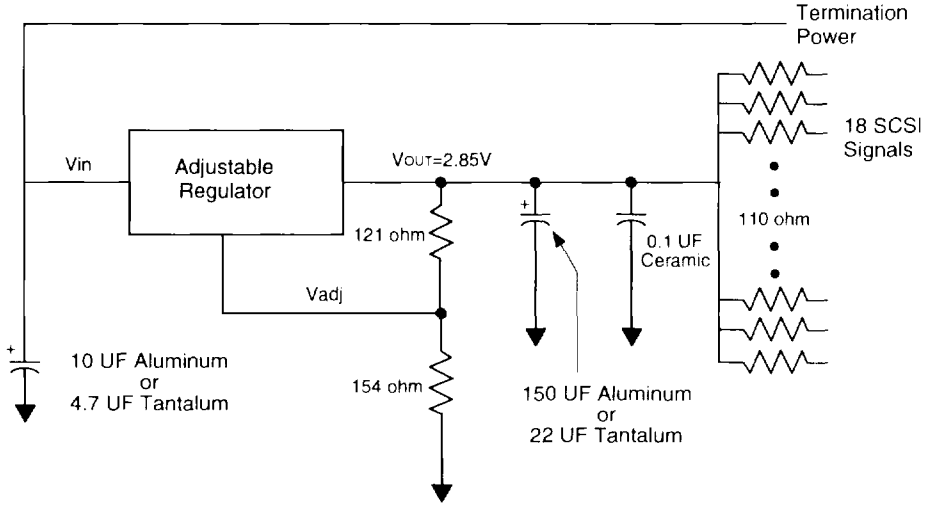
Passive termination is the original recommendation for termination and has the advantage of simplicity and availability. Its disadvantages include the very large power consumption (1636 mW) even when there is no activity on the SCSI bus and the great variation in termination voltage with changes in TERM POWER which lead to signal corruption.



132 Ohm Equivalent Impedance

Active SCSI Terminators

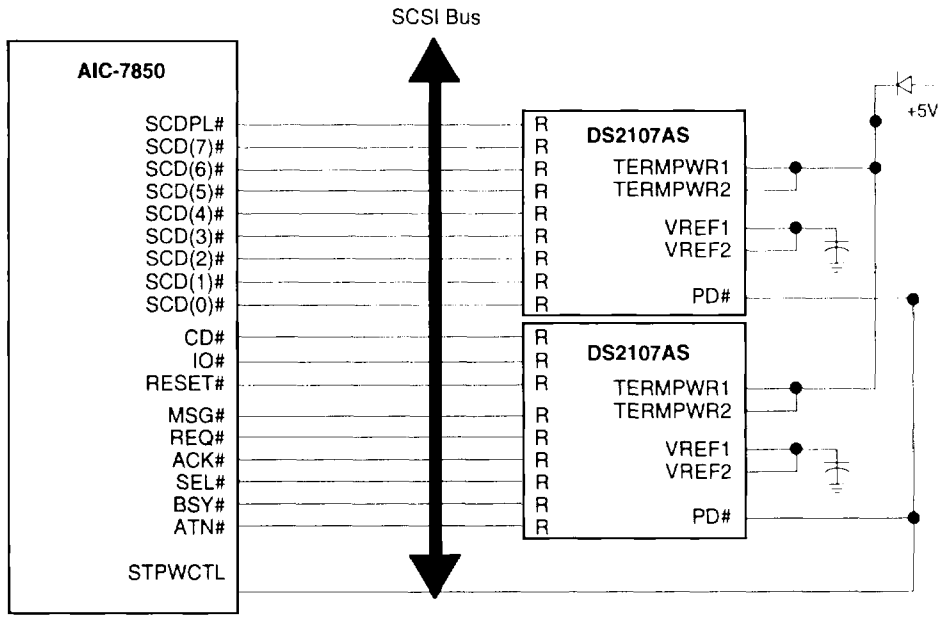
To solve the disadvantages of passive terminators, SCSI-2 defined active termination. With active termination, no quiescent power is drawn by SCSI bus signals when they are in their inactive open-collector state. Also, the voltage regulator removes any variation due to TERM POWER voltage fluctuations. The 110 ohm equivalent impedance of active termination is generally a better match for SCSI cables.



110 Ohm Equivalent Impedance

Monolithic SCSI Active Terminators

To simplify SCSI designs, SCSI active terminators are available as monolithic ICs containing the voltage regulator, voltage reference, and resistor circuits. Shown below is a SCSI bus design using the Dallas Semiconductor DS2107AS active terminator. It automatically generates the 2.85 V active termination voltage from term power and can terminate up to nine SCSI signals. A nice feature of this device is a PD# power-down control which electrically removes the device from the SCSI bus, in addition to, powering down the terminator. As shown here, the DS2107AS is enabled or disabled by the STPWCTL output control from the AIC-7850.

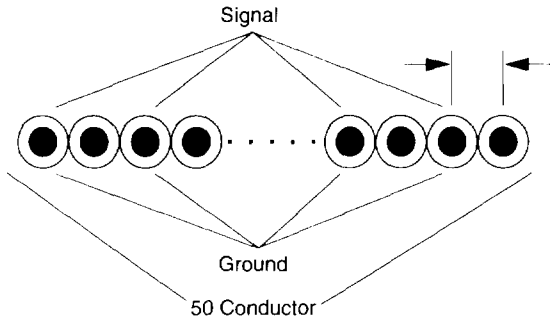


SCSI-3 Cable Signal Layout

Investigation by the SCSI committee has revised the cable impedance requirement to 72 to 96 ohms with a nominal impedance of 84 ohms. New in the cable specification is a maximum impedance difference between signals of 12 ohms. Also specified is a maximum propagation delay of 5.4 ns/m for any signal and maximum propagation delay difference of 0.15 ns/m between signals. Minimum conductor size for SCSI cable is specified as 30 AWG. Currently in wide usage are 100 ohm, 28 AWG, 50-conductor ribbon cables with 0.050-inch centers which are used with 0.100-inch internal ribbon cable connectors and 80 ohm, 30 AWG, ribbon cables with 0.025-inch centers used with the new high-density SCSI connector. Note the use of a ground between every SCSI signal to control crosstalk and maintain impedance.

Currently recommended for external cables are layered twisted pair assemblies with the critical REQ, ACK clocking signals shielded in the core. The twisted pairs are made up of 28 AWG 7/36 stranded wire. Using solid polyolefin (propylene or polyethylene), insulation impedance is about 80 ohms. Use of foamed dielectrics can raise the impedance to about 90 ohms.

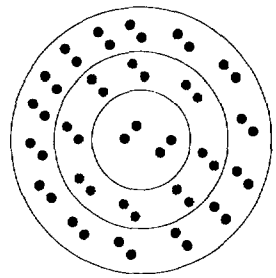
Flat Ribbon Cable



0.050-inch pitch, AWG28 PVC = 100Ω
0.050-inch pitch, AWG26 PVC = 80Ω
0.050-inch pitch, AWG30 PVC = 80Ω

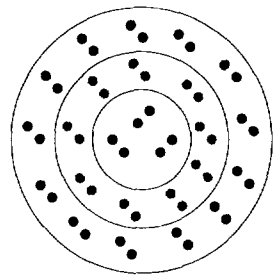
Layered Twisted Pair Cable

25 Twisted Pairs of 28 AWG 7/36 Stranded / 80Ω



Cable A: 25 Pairs

Core (2): REQ, ACK
Middle (8): RST, TermPwr, Ground, Reserved
Outer (15): DB(0)-DB(7), DB(P), CD, IO, MSG, SEL, BSY, ATN



Cable B: 25 Pairs

Core (3): REQ, ACK, Ground
Middle (9): RST, SEL, BSY, TermPwr, Ground, Reserved
Outer (13): DB(0)-DB(7), DB(P), CD, IO, MSG, ATN

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7 AIC-7850 Software

About This Chapter

Read this chapter to find out

- The layered software architecture utilized by the AIC-7850
- Driver implementation and software driver support for the AIC-7850

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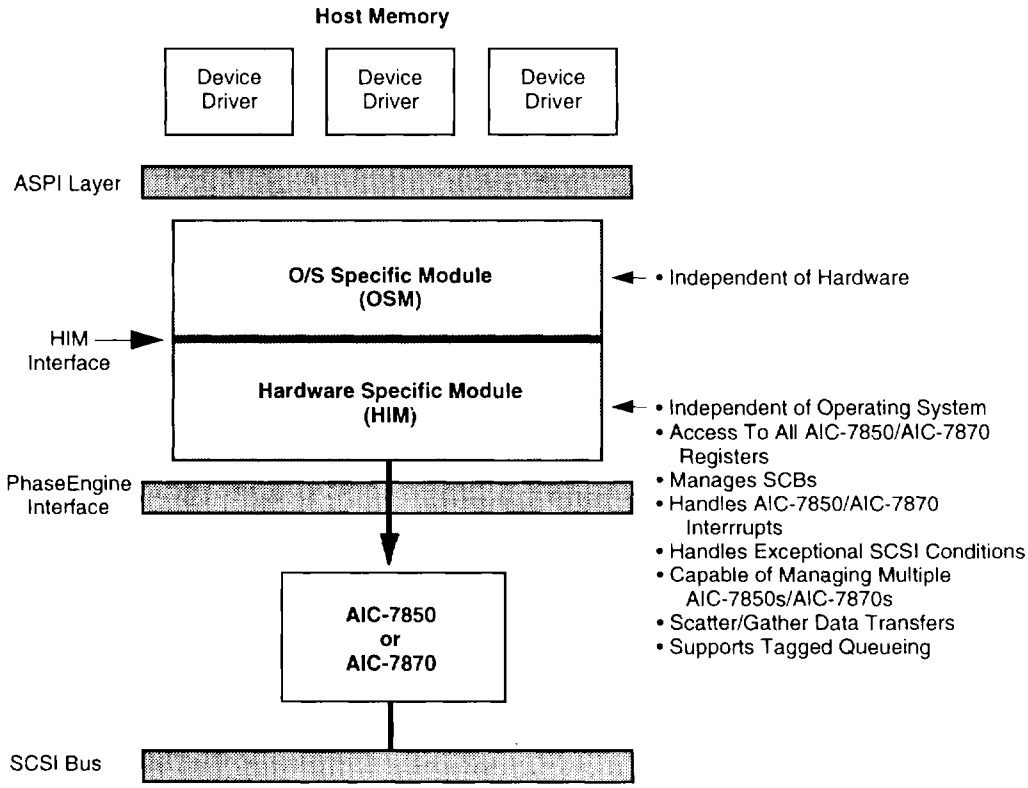
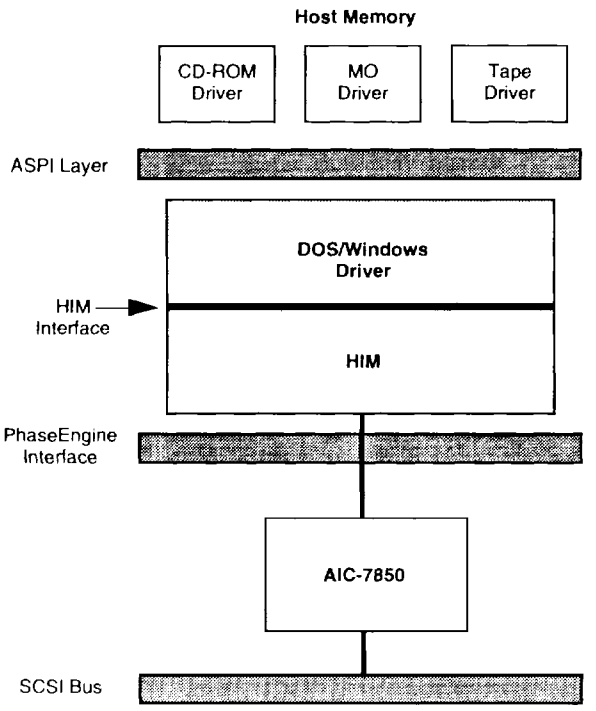
The Software Architecture

The AIC-7850 uses the same software as the AIC-7870. The AIC-7870 software utilizes a layered architecture with a standardized interface between layers. By doing this, components from each layer may be interchanged, reducing development work.

The software manager for the AIC-7850/AIC-7870 is further subdivided into two parts: an O/S Specific Module (OSM) and an AIC-7850/AIC-7870 Hardware Specific Module (HIM). Each piece insulates the other from any details which the other takes care of. Together they make up a complete AIC-7850/AIC-7870 hardware driver for a specific operating system. By replacing the O/S specific component, drivers for other operating systems may easily be created. The AIC-7850/AIC-7870 hardware specific code is available for use by software developers of specialized operating system drivers.



DOS/Windows Driver Implementation



AIC-7850/AIC-7870 Software Driver Support

- BIOS
- DOS/Windows
- Windows NT
- OS/2®
- Novell®
- SCO® UNIX
- USL UNIX®
- HIM Code Module Available for Custom Development

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