TECHNICAL MANUAL

for

SUPER NET

S-100 Single Board Computer

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INTRODUCTION

ADVANCED MICRO DIGITAL is proud to introduce the SUPER NET. The SUPER NET is a Z80 based single board computer designed to be a bus master in an S100 bus system. The SUPER NET SBC has all the hardware needed to run a single user CP/M system or 2 user MP/M system with up to 4 external floppy disk drives and an external Centronics parallel interface printer all on one board.

The SUPER NET SBC contains :

1) Z-80A cpu
2) Floppy disk controller (up to 4 drives 8 or 5 1/4 ")
3) 64 k of dynamic memory (16K bank selectible)
4) 2k or 4k of shadow eprom (2716 or 2732)
5) 2 serial ports (Z80A SIO opt.syncronous)
6) 2 12 bit parallel ports, one of which can be used for S100 vectored interrupts (Z80A PIO)
7) Real time interrupt clock (Z80A CTC)
8) S100 extended address A16 - A23

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1.1 The Floppy Disk Controller

The floppy disk controller can access up to four 8 inch or 5.25 inch floppy disk drives. It can read and write IBM 3740 single density format and double density 128,256,512,1024 sector size formats. Data transfer is done by programmed I/O with wait and interrupt syncronization.

Note : The controller cannot access both 8 inch and 5.25 inch drives simultaniously,The controller is switched from 8 inch to 5.25 inch drives by hardware jumper options.

1.2 The 64 k Dynamic ram

The 64 k ram array can be switched on and off in 16 k increments (0-16K,16K-32K,32K-48K,48K-64K) under software control. This allow- t: CPU to access bank switchable external memory on the S100 bus. The memory has an access time of 200ns. Refresh is done during Z80 M1 cycles and during wait and reset states. The memory can be accessed by an external DMA device on the S100 bus.

Note : Any external DMA device that is using continous mode DMA cycles must transfer data at an average rate of 15 us per byte or faster when holding the DMA request line for more than 1.5 ms This .s not a problem because most designers are smart enough to use byte-at-a-time or burst transfer modes when dealing with slow DMA transfer rates. The ram row address is the low order address therefor the entire ram array is refreshed by the DMA device every 128 contiguous memory cycles.

1.3 System Monitor Eprom

The system monitor eprom is switched on during reset. It can be disabled and enabled under software control. It resides when enabled at F000h to FFFFh. It has commands that allow the user to load the CP/M , MP/M or other boot loaders from floppy disk. In addition it can be used to load , examine goto and test memory. When the prom is disabled it does not use any system address space.

1.4 Serial ports

A Z80A DART is used for the two serial ports , but a Z80A SIO/0 chip can be used in it's place. This allows asyncronous and synchronous serial data communications plus a variety of interrupt modes. Modem control signals are available at each serial connector. There are two switch selectible baud rate generators for baud rates of 50 to 19.2 k baud.

Note : The serial ports are TTL and must be connected to external interface boards for RS232 communications.

(PS NET/I)

1.5 Parallel ports

A Z80A PIO is used as the parallel port. The "A" channel of this chip is connected to the parallel port connector. This port has 8 bi-directional data lines and two hand shake lines. The "B" port can be spl between the parallel port connector and the S100 bus vectored interru lines by jumper options. This allows the port to be used as an additional parallel port or interrupt controller or both.

In the output mode the parallel ports can drive one TTL load .

1.6 Real Time Interrupt clock

A Z80A CTC is used for providing a real time system clock for MP/M. Three channels of the CTC are available to the user for strapping a jumper header for synchronous baud rates or long clock times.

1.7 S100 Bus Interface

The S100 bus interface provides the signals necessary for an 8 bit bus master as described by the IEEE 696 bus specification. Vectored interrupt lines VI0 - VI7 are supported via jumper options and A16 - A23 are also supported vis an I/O port. The PAMNTON line is also implemented for the dynamic ram array.

2.0 EPROM and Monitor operation

The onboard EPROM occupies address F000H-FFFFH. The EPROM is switched on automatically during reset or power on, the EPROM contains SIO and FDC initialization code along with a simple debugger and floppy disk cold start loader. After the operating system is loaded the EPROM can be turned off so that the ram at address F000H-FFFFH can be accessed. The EPROM can be turned on and off at any time so that hardware dependent I/O routines can be called.

2.1 Eprom Enable / Disable

Switching EPROM on :

```
 F033 3E4F              MVI A,01001111B ;RESET POWER ON JUMP
                                        ; AND ENABLE MEMORY, EPROM ON
 F035 D316              OUT 16H         ;WRITE TO CONTROL PORT
```

Switching EPROM off :

```
 F033 3E4F              MVI A,01101111B ;RESET POWER ON JUMP
                                        ; AND ENABLE MEMORY, EPROM OFF
 F035 D316              OUT 16H         ;WRITE TO CONTROL PORT
```

Jumper R configures the board to accept a 2716 or 2732 EPROM.

Note : The EPROM is always addressed at F800H and can not be moved. Since the 2716 EPROM is 2K long it appears twice , F800H-FC00H and FBFFH-FFFFH.

2.2 Monitor Signon

The EPROM contains a simple debugger.
The monitor signs on with :

```
 > ADVANCED MICRO DIGITAL CORP.
   Monitor Version 1.0
   Nov - 1981
   Press "H" for help
 >
```

2.3 Monitor Commands

The monitor commands are :

Control C = Load disk boot loader

D SSSS QQQQ = Dump memory in hex from SSSS to QQQQ

F SSSS QQQQ BB = Fill memory from SSSS to QQQQ with BB

G AAAA = Go to address AAAA

L AAAA = Load memory starting at AAAA

M = Memory Test

P SSSS QQQQ = Print in ascii from SSSS to QQQQ

R = Find system ram

S SSSS QQQQ = Search for byte pattern

T = Test Memory

ESC will terminate any command

The cold boot loader will select and home drive Ø.

Track Ø sector 1 will be read into memory at location Ø.

Single density is assumed for track Ø.

If an error occures an error code will be printed.

The error code must be translated using the table

in appendex F page F-4 fig 2.

2.4 Cold Boot Program

```
                ; READ TRACK 0 SECTOR 1 INTO MEMORY

                BOOT:
F4B5 3E0D               MVI     A,ØDH           ; RESET FDC
F4B7 D30C               OUT     FDC             ; ISSUE COMMAND
F4B9 00                 NOP
                FDCW1:
F4BA DB0C               IN      FDC             ; CHECK BUSY
F4BC 0F                 RRC
F4BD DABAF4             JC      FDCW1

F4C0 00                 NOP                     ; KILL TIME
F4C1 00                 NOP
F4C2 00                 NOP
```

```
F4C3 00                 NOP

F4C4 3E03               MVI     A,3             ; GET A RESTORE
F4C6 D30C               OUT     FDC             ; ISSUE COMMAND
F4C8 00                 NOP

F4C9 DB14               IN      WAIT            ; WAIT FOR
F4CB 00                 NOP                     ; INTRQ
                TK0:
F4CC DB0C               IN      FDC
F4CE E604               ANI     4               ; CHECK TRACK 0
F4D0 CACCF4             JZ      TK0

F4D3 AF                 XRA     A
F4D4 6F                 MOV     L,A             ; POINT AT LOC 0
F4D5 67                 MOV     H,A
F4D6 3C                 INR     A
F4D7 D30E               OUT     FDCSEC          ; SET SECTOR
F4D9 3E8C               MVI     A,08CH          ; GET READ COMMAND
F4DB D30C               OUT     FDC             ; ISSUE COMMAND
F4DD 00                 NOP
                FDCRD:
F4DE DB14               IN      WAIT            ; WAIT FOR INTRQ
F4E0 B7                 ORA     A               ;  OR DRQ
F4E1 F2EBF4             JP      BOOTDN          ; EXIT IF INTRQ
F4E4 DB0F               IN      FDCDATA         ; GET DATA
F4E6 77                 MOV     M,A             ; STORE
F4E7 23                 INX     H               ; POINT NEXT
F4E8 C3DEF4             JMP     FDCRD

                BOOTDN:
F4EB DB0C               IN      FDC             ; CHECK STATUS
F4ED B7                 ORA     A               ; 0 = NO ERROR
F4EE CA0000             JZ      0               ; OK, GO
F4F1 F5                 PUSH    PSW             ; SAVE ERROR
F4F2 210FF6             LXI     H,BTERR         ; PRINT
F4F5 CDE6F0             CALL    MSG             ;  DISK ERROR
F4F8 F1                 POP     PSW             ; GET ERROR
F4F9 CD21F1             CALL    THXB            ; PRINT IT
```

3.0 INPUT / OUTPUT PORT ASSIGMENTS

Address		Function
00	Read/Write	SIO Channel A Data port
01	Read/Write	SIO Channel A Status/Control Port
02	Read/Write	SIO Channel B Data port
03	Read/Write	SIO Channel B Status/Control Port
04	Read/Write	PIO Channel A Data port
05	Write	PIO Channel A Control Port
06	Read/Write	PIO Channel B Data port
07	Write	PIO Channel B Control Port
08	Read/Write	CTC Channel 0 Control Port
09	Read/Write	CTC Channel 1 Control Portol
0A	Read/Write	CTC Channel 2 Control Port
0B	Read/Write	CTC Channel 3 Control Port
0C	Read/Write	FDC Command/States Port
0D	Read/Write	FDC Track Register
0E	Read/Write	FDC Sector Register
0F	Read/Write	FDC Data Port
10		Unused
11		Unused
12		Unused
13		Unused
14	Read/Write	FDC Syncronization/Drive/Density
15	Write	S100 Buss Extended Address A16-A24
16	Write	On-Board Memory Control Port
17		Unused
18		Unused
19		Unused
1A		Unused
1B		Unused
1C		Unused
1D		Unused
1E		Unused
1F		Unused

All address are listed in Hexidecimal.

The unused input / output ports are internally decoded and should not be used by external S100 I/O boards.

4.0 INPUT / OUTPUT PORT DISCRIPTIONS

4.1 Serial Communications Port A --- See Appendex A

00	Read/Write	SIO Channel A Data port
01	Read/Write	SIO Channel A Status/Control Port

4.2 Serial Communications Port B --- See Appendex A

02	Read/Write	SIO Channel B Data port
03	Read/Write	SIO Channel B Status/Control Port

4.3 Paralled Interface Port A --- See Appendix B

04	Read/Write	PIO Channel A Data port
05	Write	PIO Channel A Control Port

4.4 Parallel Interface Port B --- See Appendix B

This port can be jumpered via jumpers E through P to the S100 Vectored Interrupt lines or to connector J2 (see sec 6.0)

06	Read/Write	PIO Channel B Data port
07	Write	PIO Channel B Control Port

4.5 Control Timmer Interrupt circuit --- See Appendix C

08	Read/Write	CTC Channel 0 Control Port
09	Read/Write	CTC Channel 1 Control Port
0A	Read/Write	CTC Channel 2 Control Port
0B	Read/Write	CTC Channel 3 Control Port

4.6 Floppy Disk Controller --- See Appendix D

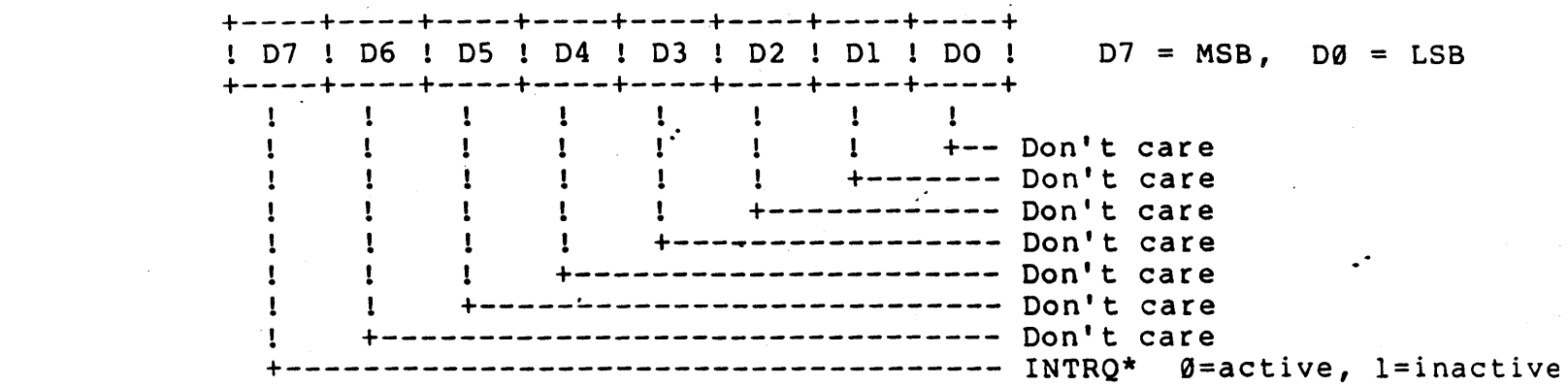
0C	Read/Write	FDC Command/States Port
0D	Read/Write	FDC Track Register
0E	Read/Write	FDC Sector Register
0F	Read/Write	FDC Data Port

4.7 Floppy Disk Control Port

14 Read/Write FDC Syncronization/Drive/Density

Port Read :

When the cpu reads this port the cpu is placed into a wait state until a data byte can be transfered to or from the floppy disk controller or untill the command complete/terminate status (INTRQ) is set by the floppy disk controller. The floppy disk controller INTRQ status bit is placed on the data bus as bit D7. This bit can be tested to determine if data is to be transfered of if the command is complete.

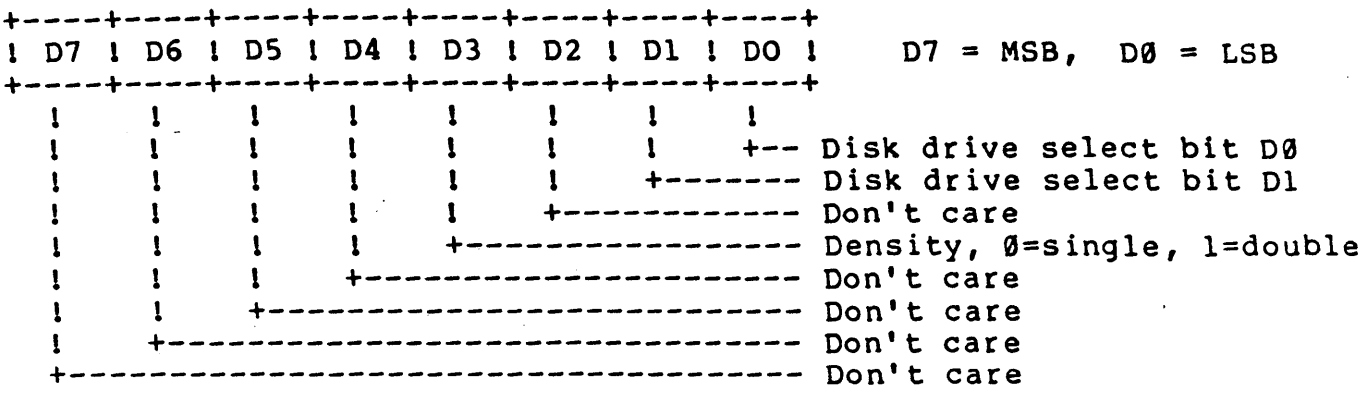


Port Write :

The low two bits DØ and D1 of this port control which drive is selected.

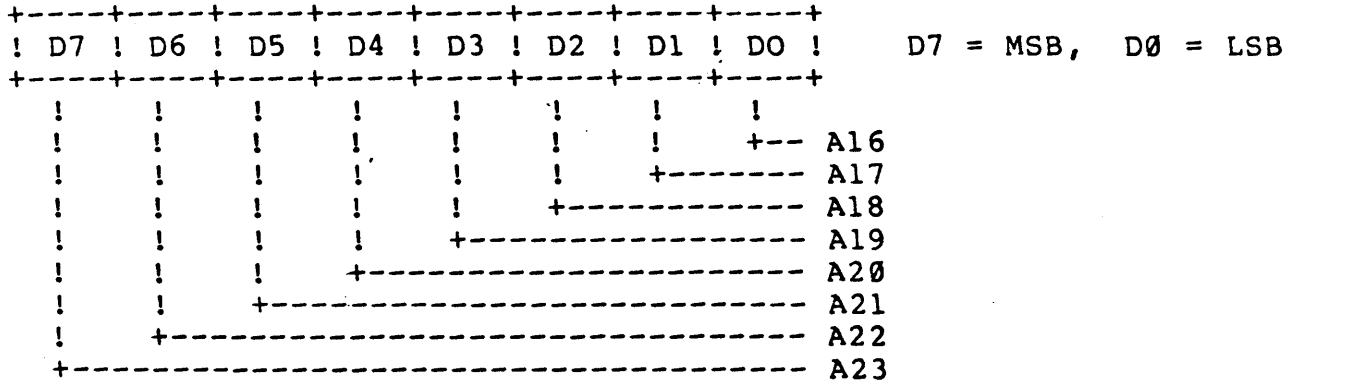
D1	DØ	
Ø	Ø	Disk drive Ø selected
Ø	1	Disk drive 1 selected
1	Ø	Disk drive 2 selected
1	1	Disk drive 3 selected

Bit D3 sets the density mode. When bit D3 = Ø, single density is selected. When bit D3 = 1, double density is selected.



4.8 Extended address port --- See Section 8.1 (buss defination)
15 Write S1ØØ Buss Extended Address A16-A23
Port Write :

This port controls the S1ØØ Extended address lines.



4.9 On-Board Memory Control Port

16 Write On-Board Memory Control Port

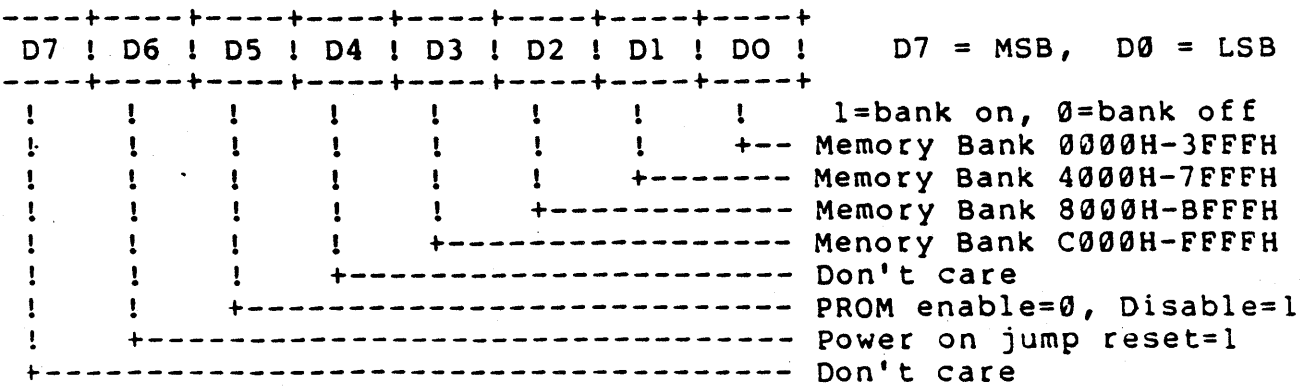
This port controls the onboard memory managment circuit, Prom enable and disable and power on jump reset circuits.

Port write :

The four low order bits D0,D1,D2 and D3 switch the on board memory in 16k banks corresponding to address 0000h-3FFFh,4000H-7FFFH, 8000H-BFFFH and C000-FFFFH on and off. When a particular bank is switched off, external S100 memory can be accessed in that banks address range. This feature allows external memory to be added to the system for multi-user operating systems.

Bit D5 of this port switches the on-board EPROM on and off. The onboard EPROM occupies address F000H-FFFFH. The EPROM is switched on automatically during reset or power on, the EPROM contains SIO and FDC initialization code along with a simple debugger and floppy disk cold start loader. After the operating system is loaded the EPROM can be turned off so that the ram at address F000H-FFFFH can be accessed.

Bit D6 reset the power on jump circuit. Bit D6 must be set high after a reset or power on situation before ram can be accessed.



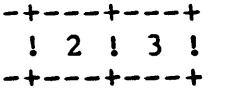
5.0 Jumper Definitions

Jumper	Function
A	CPU clock rate 2mhz/4mhz
B	External/Enternal Tx/Rx clock for SIO channel A
C	External/Enternal Tx/Rx clock for SIO channel B
D	Eight inch - five inch Drive selection
E	Select S100 interrupt vector line VI0 OR PINT.
F	Select S100 interrupt vector VIO/PINT or Parallel Port B bit D0 on J2-25.
G	Select S100 interrupt vector VI1 or Parallel Port B bit D1 on J2-27.
H	Select S100 interrupt vector VI2 or Parallel Port B bit D2 on J2-29.
J	Select S100 interrupt vector VI3 or Parallel Port B bit D3 on J2-31.
K	Select S100 interrupt vector VI4 or Parallel Port B bit D4 on J2-33.
M	Select S100 interrupt vector VI5 or Parallel Port B bit D5 on J2-35.
N	Select S100 interrupt vector VI6 or Parallel Port B bit D6 on J2-37.
P	Select S100 interrupt vector VI7 or Parallel Port B bit D7 on J2-39.
R	Select 2716 or 2732 EPROM.
S	Define floppy disk connector for eight ad five inch drives.
T	Enable / Disable S100 bus memory write signal on J1 - 68

6.0 Jumper Descriptions

6.1 A CPU clock rate 2mhz/4mhz

This jumper determines the cpu clock rate.
The jumper is located below IC U7.



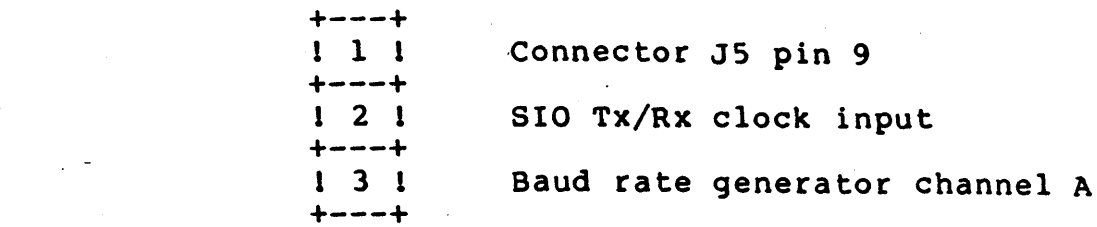
Install Plug between posts 1 & 2 for 4mhz operation.

Install Plug between posts 2 & 3 for 2mhz operation.

6.2 B External/internal Tx/Rx clock for SIO channel A

Jumper B connects the SIO channel A to either the internal baud rate generator or to the connector J4 pin 9 for use in sycronous applicati

Jumper B is located near J5.



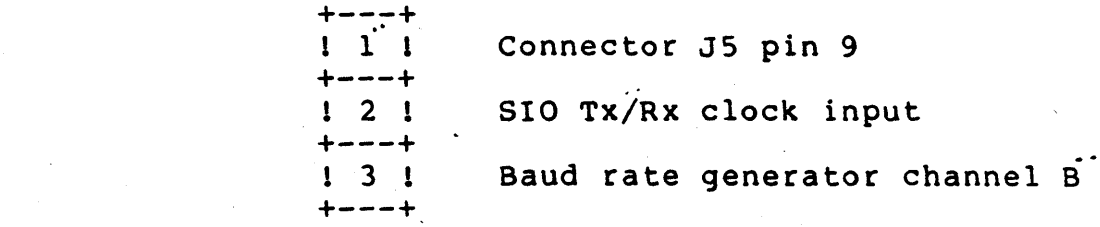
Install Plug between posts 1 & 2 for external SIO clock.

Install Plug between posts 2 & 3 for Baud rate generator.

6.3 C External/internal Tx/Rx clock for SIO channel B

Jumper C connects the SIO channel B to either the internal baud rate generator or to connector J5 pin 9 for use in sycronous applications.

Jumper C is located near J5.

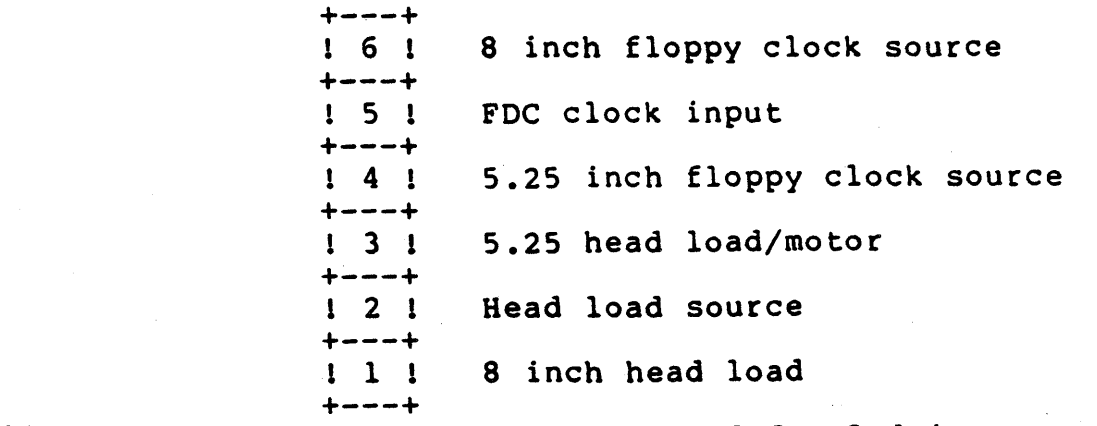


Install Plug between posts 1 & 2 for external SIO clock.

Install Plug between posts 2 & 3 for Baud rate generator.

6.4 D Eight inch - five inch Drive selection

Jumper D is located near IC U2.



Install Plug between posts 1 & 2 and 5 & 6 for 8 drives.

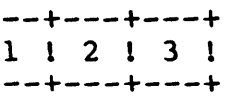
Install Plug between posts 2 & 3 and 4 & 5 for 5.25 inch drives.

Note : There are other board modifications needed to interface the FDC to a 5.25 inch drive.

6.5 E Select S100 interrupt vector line VI0 OR PINT.

Jumper E selects the interrupt line to be used when channel B bit D0 is programmed for interrupts.

Jumper E is located below IC U8.

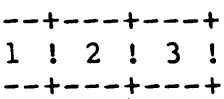


Install Plug between posts 1 & 2 for VI0 interrupt pin. (J1-4)

Install Plug between posts 2 & 3 for PINT interrupt pin. (J1-73)

6.6 F Select S100 interrupt vector VIO/PINT or Parallel Port B bit D0 on J2-25.

This jumper is located near connector J2.

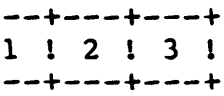


Install Plug between posts 1 & 2 to connect the PIO bit D0: to J2 pin 25 (when the PIO bit is programmed for input/output).

Install Plug between posts 2 & 3 to connect the PIO bit D0 to the jumper selector area E, VI0/PINT (when the PIO bit is programmed for interrupt mode).

6.7 G Select S100 interrupt vector VI1 or Parallel Port B bit D1 on J2-27.

This jumper is located near connector J2.

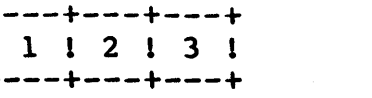


Install Plug between posts 1 & 2 to connect the PIO bit D1 to J2 pin 25 (when the PIO bit is programmed for input/output).

Install Plug between posts 2 & 3 to connect the PIO bit D1 to the vectored interrupt line VI1 (when the PIO bit is programmed for interrupt mode).

6.8 H Select S100 interrupt vector VI2 or Parallel Port B bit D2 on J2-29.

This jumper is located near connector J2.

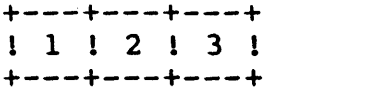


Install Plug between posts 1 & 2 to connect the PIO bit D2 to J2 pin 25 (when the PIO bit is programmed for input/output).

Install Plug between posts 2 & 3 to connect the PIO bit D2 to the vectored interrupt line VI2 (when the PIO bit is programmed for interrupt mode).

6.9 J Select S100 interrupt vector VI3 or Parallel Port B bit D3 on J2-31.

This jumper is located near connector J2.

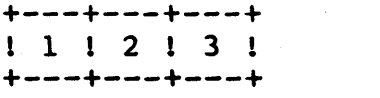


Install Plug between posts 1 & 2 to connect the PIO bit D3 to J2 pin 25 (when the PIO bit is programmed for input/output).

Install Plug between posts 2 & 3 to connect the PIO bit D3 to the vectored interrupt line VI3 (when the PIO bit is programmed for interrupt mode).

6.10 K Select S100 interrupt vector VI4 or Parallel Port B bit D4 on J2-33.

This jumper is located near connector J2.

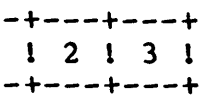


Install Plug between posts 1 & 2 to connect the PIO bit D4 to J2 pin 25 (when the PIO bit is programmed for input/output).

Install Plug between posts 2 & 3 to connect the PIO bit D4 to the vectored interrupt linr VI4 (when the PIO bit is programmed for interrupt mode).

6.11 M Select S100 interrupt vector VI5 or Parallel Port B bit D5 on J2-35.

This jumper is located near connector J2.

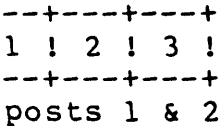


Install Plug between posts 1 & 2 to connect the PIO bit D5 to J2 pin 25 (when the PIO bit is programmed for input/output).

Install Plug between posts 2 & 3 to connect the PIO bit D5 to the vectored interrupt line VI5 (when the PIO bit is programmed for interrupt mode).

6.12 N Select S100 interrupt vector VI6 or Parallel Port B bit D6 on J2-37.

This jumper is located near connector J2.

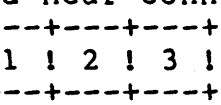


Install Plug between posts 1 & 2 to connect the PIO bit D6 to J2 pin 25 (when the PIO bit is programmed for input/output).

Install Plug between posts 2 & 3 to connect the PIO bit D6 to the vectored interrupt line VI6 (when the PIO bit is programmed for interrupt mode).

6.13 P Select S100 interrupt vector VI7 or Parallel Port B bit D7 on J2-39.

This jumper is located near connector J2.



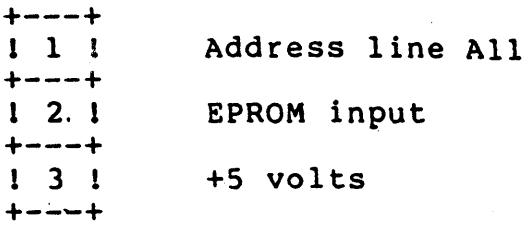
Install Plug between posts 1 & 2 to connect the PIO bit D7 to J2 pin 25 (when the PIO bit is programmed for input/output).

Install Plug between posts 2 & 3 to connect the PIO bit D7 to the vectored interrupt line VI7 (when the PIO bit is programmed for interrupt mode).

6.14 R Select 2716 or 2732 EPROM.

Jumper R configures the board to accept a 2716 or 2732 EPROM.

Jumper R is located near the Z80 chip.



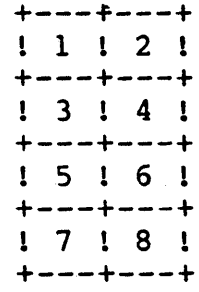
Install Plug between posts 1 & 2 for a 2732 EPROM.

Install Plug between posts 2 & 3 for a 2716 EPROM.

Note : The EPROM is always addressed at F800H and can not be moved. Since the 2716 EPROM is 2K long it appears twice , F800H-FC00H and FBFFH-FFFFH.

6.15 S Define floppy disk connector for eight , five inch drives änd FDC chip type.

This jumper is located U26.



Install Plug between posts 1 & 2 for 12 volt FDC chips (WD1793)

Remove Plug between posts 1 & 2 for 5 volt only chips (MB8877)

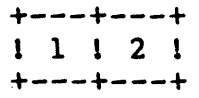
Install Plug between posts 3 & 4 to connect HEAD 2 signal to pin 2 of J3.

Install Plug between posts 5 & 6 to connect above track 43 to pin 24 of J3.

Install Plug between posts 7 & 8 to connect HEAD 2 signal to pin 14 of J3.

6.16 T Enable / Disable S100 bus memory write signal on J1 - 68

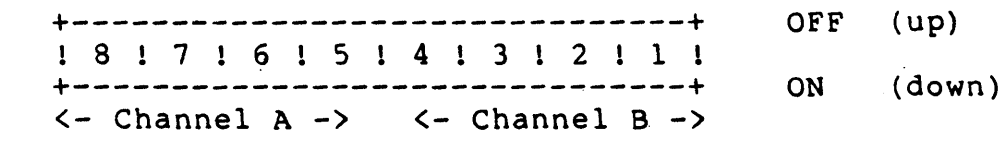
This jumper is located near U18.



Install Plug between posts 1 & 2 to connect the memory write signal (MEMWR) to the S100 bus pin 68.

7.0 Baud Rate Switch

The baud rate of the two serial channels can be select separately by setting the baud rate switch. The baud rate switch is an 8 pole switch located near U54. It is split into two sections. Switches 1,2,3,4 set the baud rate for the SIO channel B and switches 5,6,7,8 set the baud rate for the SIO channel A.



7.1 Baud rate switch setting

Switch 8 7 6 5	Channel B baud rate
Switch 4 3 2 1	Channel A baud rate
on on on on	50
off on on on	75
on off on on	110
off off on on	134.5
on on off on	150
off on off on	300
on off off on	600
off off off on	1200
on on on off	1800
off on on off	2000
on off on off	2400
off off on off	3600
on on off off	4800

off	on	off off	7200
on	off	off off	9600
off	off	off off	19,200

For exact baud rate frequencies see Appendix D

8.0 External Connector Pin definitions

8.1 Connector J1 - S100 bus connector

insert page 28 & 29 from IEEE - 696 specification

8.2 Connector J2 - Parallel port connector

	1	ARDY	PIO Channel A ready signal
	2	ARDY RET	ground
	3	ASTRB*	PIO Channel A strobe
	4	ASTRB RET	ground
	5	PA0	PIO Channel A data bit D0
	6	PA0 RET	ground
	7	PA1	PIO Channel A data bit D1
	8	PA1 RET	ground
	9	PA2	PIO Channel A data bit D2
	10	PA2 RET	ground
	11	PA3	PIO Channel A data bit D3
	12	PA3 RET	ground
	13	PA4	PIO Channel A data bit D4
	14	PA4 RET	ground
	15	PA5	PIO Channel A data bit D5
	16	PA5 RET	ground
	17	PA6	PIO Channel A data bit D6
	18	PA6 RET	ground
	19	PA7	PIO Channel A data bit D7
	20	PA7 RET	ground
	21	BRDY	PIO Channel B ready signal
	22	BRDY RET	ground
	23	BSTRB*	PIO Channel B strobe
	24	BSTRB RET	ground
*	25	PB0	PIO Channel B data bit D0
	26	PB0 RET	ground
*	27	PB1	PIO Channel B data bit D1
	28	PB1 RET	ground
*	29	PB2	PIO Channel B data bit D2
	30	PB2 RET	ground
*	31	PB3	PIO Channel B data bit D3
	32	PB3 RET	ground
*	33	PB4	PIO Channel B data bit D4
	34	PB4 RET	ground
*	35	PB5	PIO Channel B data bit D5
	36	PB5 RET	ground
*	37	PB6	PIO Channel B data bit D6

	38	PB6 RET	ground
*	39	PB7	PIO Channel B data bit D7
	40	+ 5 VOLTS	

* Note : These pins can can be jumpered to the S100 bus vectored interrupt lines.

8.3 Connector J3 Floppy disk connector

8 inch	5.25 inch	
1		ground
2		Alternate Head 2*
3		ground
4		N/C
5		ground
6		N/C
7		ground
8		N/C
9		ground
10		N/C
11		ground
12		N/C
13		ground
14		Head 2*
15		ground
16		N/C
17	1	ground
18	2	Head load*
19	3	ground
20	4	Index*
21	5	ground
22	6	Ready*
23	7	ground
24	8	Above Track 43*
25	9	ground
26	10	Drive select 0*
27	11	ground
28	12	Drive select 1*
29	13	ground
30	14	Drive select 2*
31	15	ground
32	16	Drive select 3*
33	17	ground
34	18	Direction
35	19	ground
36	20	Step*
37	21	ground
38	22	Write Data*
39	23	ground
40	24	Write gate*
41	25	ground
42	26	Track 0*

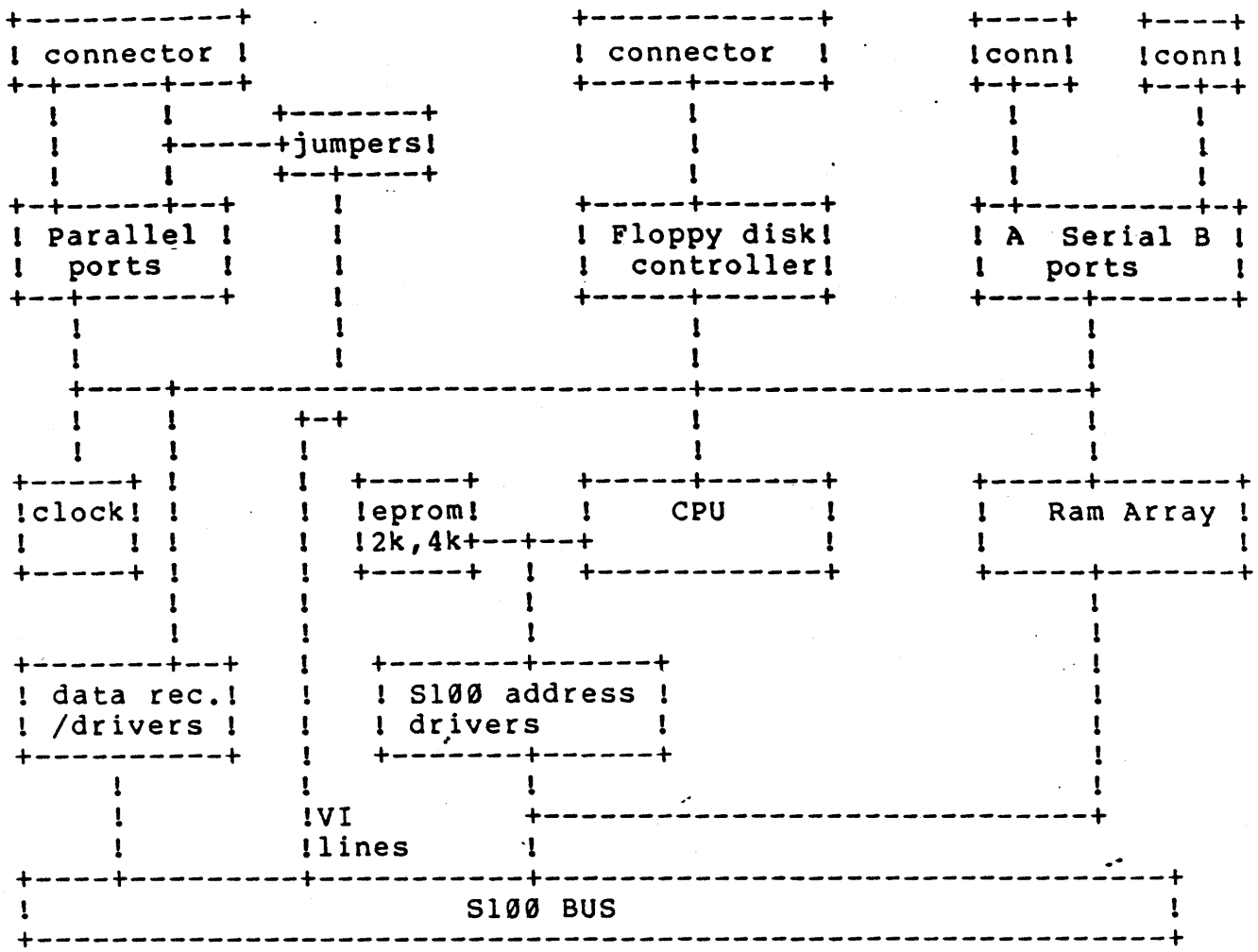
43	27	ground
44	28	Write protect*
45	29	ground
46	30	Read data*
47	31	ground
48	32	Motor on*
49	33	ground
50	34	N/C

8.4 Connector J4 - Serial port Channel A

1	N/C	
2	DCDA*	Data Carrer Detect Channel A *
3	SYNCA*	Sync Detect
4	RxDA	Receive data
5	CTSA*	Clear to send
6	TxDA	Transmit data
7	RTSA*	Request to send
8	DTRA*	Data terminal ready
9	Tx/RxCA*	Transmitt / receive clock
10	GND	
11	N/C	
12	+16 VOLTS	
13	-16 VOLTS	
14	+5 VOLTS	

8.5 Connector J5 - Serial port Channel B

1	N/C	
2	DCDA*	Data Carrer Detect Channel A *
3	SYNCA*	Sync Detect
4	RxDA	Receive data
5	CTSA*	Clear to send
6	TxDA	Transmit data
7	RTSA*	Request to send
8	DTRA*	Data terminal ready
9	Tx/RxCA*	Transmitt / receive clock
10	GND	
11	N/C	
12	+16 VOLTS	
13	-16 VOLTS	
14	+5 VOLTS	


connector
jumpers
Parallel ports
connector
Floppy disk controller
conn
conn
A Serial B ports
clock
eprom 2k,4k
CPU
Ram Array
data rec. /drivers
S100 address drivers
VI lines
S100 BUS

10.0 Factory Installed Jumpers

10.1 Factory Installed jumpers for 8 inch floppy option

Jumper		
A	2-3	CPU clock 4mhz
B	2-3	Tx/Rx clock for SIO A internal
C	2-3	Tx/Rx clock for SIO B internal
D	1-2,5-6	Eight inch Drive selection
E	1-2	Select vector line VI0
F	2-3	Parallel Port B bit D0 on J2-25.
G	2-3	Parallel Port B bit D1 on J2-27.
H	2-3	Parallel Port B bit D2 on J2-29.
J	2-3	Parallel Port B bit D3 on J2-31.
K	2-3	Parallel Port B bit D4 on J2-33.
M	2-3	Parallel Port B bit D5 on J2-35.
N	2-3	Parallel Port B bit D6 on J2-37.
P	2-3	Parallel Port B bit D7 on J2-39.
R	2-1	Select 2716
S	5-6,7-8	Define floppy disk connector
T	1-2	Enable S100 bus memory write signal

10.2 Factory Installed jumpers for 5.25 inch floppy option

Jumper		
A	2-3	CPU clock 4mhz
B	2-3	Tx/Rx clock for SIO A internal
C	2-3	Tx/Rx clock for SIO B internal
D	1-2,5-6	Eight inch Drive selection
E	1-2	Select vector line VI0
F	2-3	Parallel Port B bit D0 on J2-25.
G	2-3	Parallel Port B bit D1 on J2-27.
H	2-3	Parallel Port B bit D2 on J2-29.
J	2-3	Parallel Port B bit D3 on J2-31.
K	2-3	Parallel Port B bit D4 on J2-33.
M	2-3	Parallel Port B bit D5 on J2-35.
N	2-3	Parallel Port B bit D6 on J2-37.
P	2-3	Parallel Port B bit D7 on J2-39.
R	2-1	Select 2716
S	5-6,7-8	Define floppy disk connector
T	1-2	Enable S100 bus memory write signal

Resistor R4 is changed to 220k ohm

C22 100pf

10.3 Shugart SA 800 Jumpers

Disk drive jumpers

Remove all jumpers on the disk drive. Install jumpers as follows:

Jumper Y
Jumper D
Jumper T3,T4,T5,T6
Jumper T1
Jumper 800
Jumper X
Jumper A
Jumper B
Jumper DS
jumper DS1 or DS2

10.4 Shugart 850

Disk drive Jumpers

Jumper 2S
Jumper D
Jumper A
Jumper B
Jumper R
Jumper I
Jumper Z
Jumper 850
Jumper S2
Jumper IW
Jumper FS
Jumper RS
Jumper DS

10.8 NEC model FD1160

Disk drive Jumpers

Install jumpers as follows:

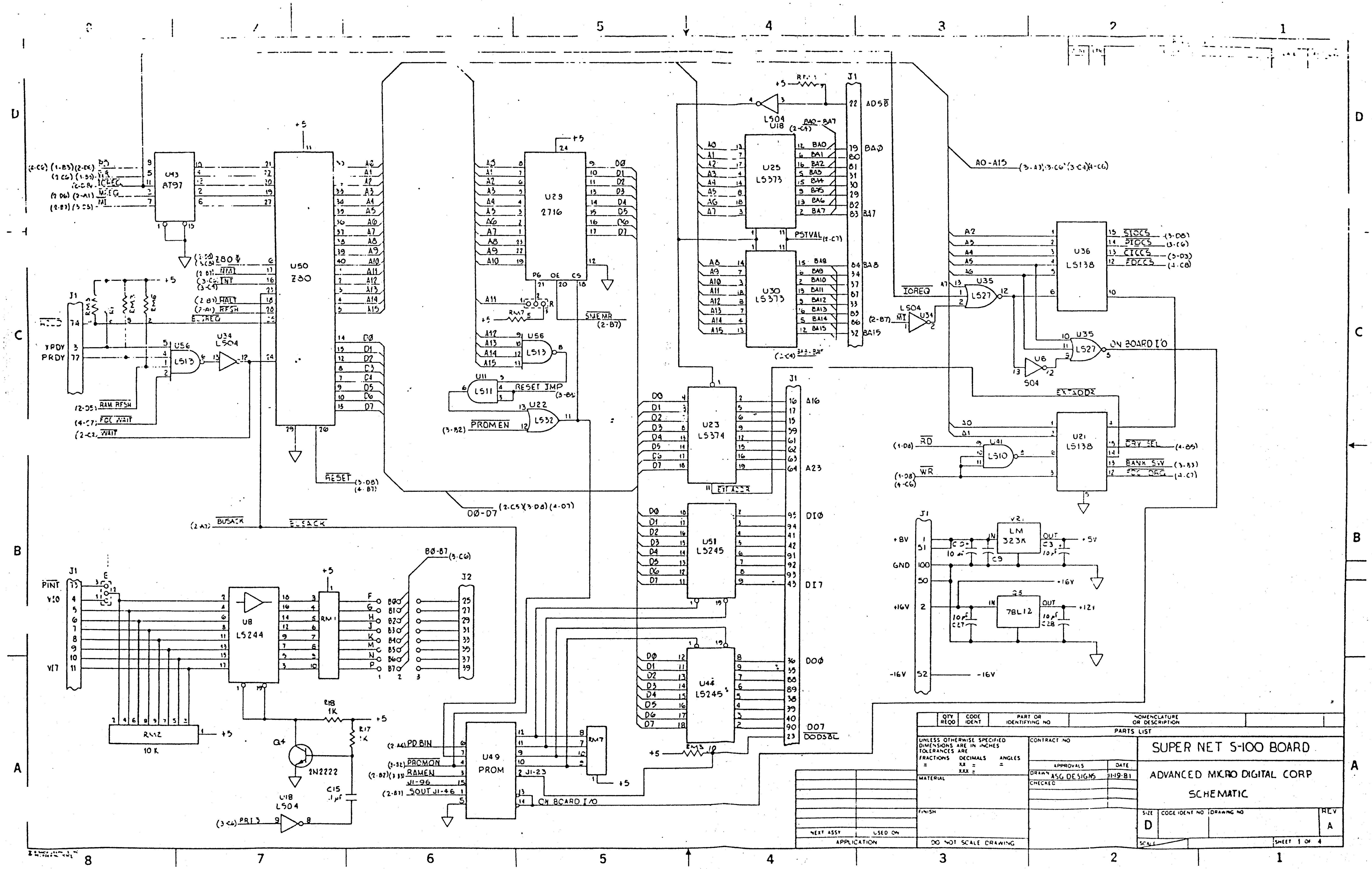
Jumper C	Jumper PRI
Jumper N	Jumper DLD
Jumper HLS	Jumper FU
Jumper M	

10.9 QUME data track 8

Disk drive jumpers

Install jumpers as follows:

DS1 OR DS2
D
C (OPTIONAL)
DC
2S


SUPER NET S-100 BOARD
ADVANCED MICRO DIGITAL CORP
SCHEMATIC
DRAWN ASG DESIGNS 11-19-81
SIZE D
REV A
SHEET 1 OF 4
DO NOT SCALE DRAWING
PARTS LIST
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
NEXT ASSY
USED ON
APPLICATION
U50 Z80
U29 2716
U25 LS373
U30 LS373
U36 LS138
U21 LS138
U23 LS374
U51 LS245
U44 LS245
U8 LS244
U49 PROM
U43 AT97
VR1 LM 323K
78L12
Q4 2N2222
A0-A15
D0-D7
B0-B7
ON BOARD I/O
EXT ADDR
PSTVAL
RESET
BUSACK
+5V
+12V
-16V
+8V
GND
+16V

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION				

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO

APPROVALS	DATE
DRAWN ASG DESIGNS	11-19-81
CHECKED	

SUPER NET S-100 BOARD

ADVANCED MICRO DIGITAL CORP.

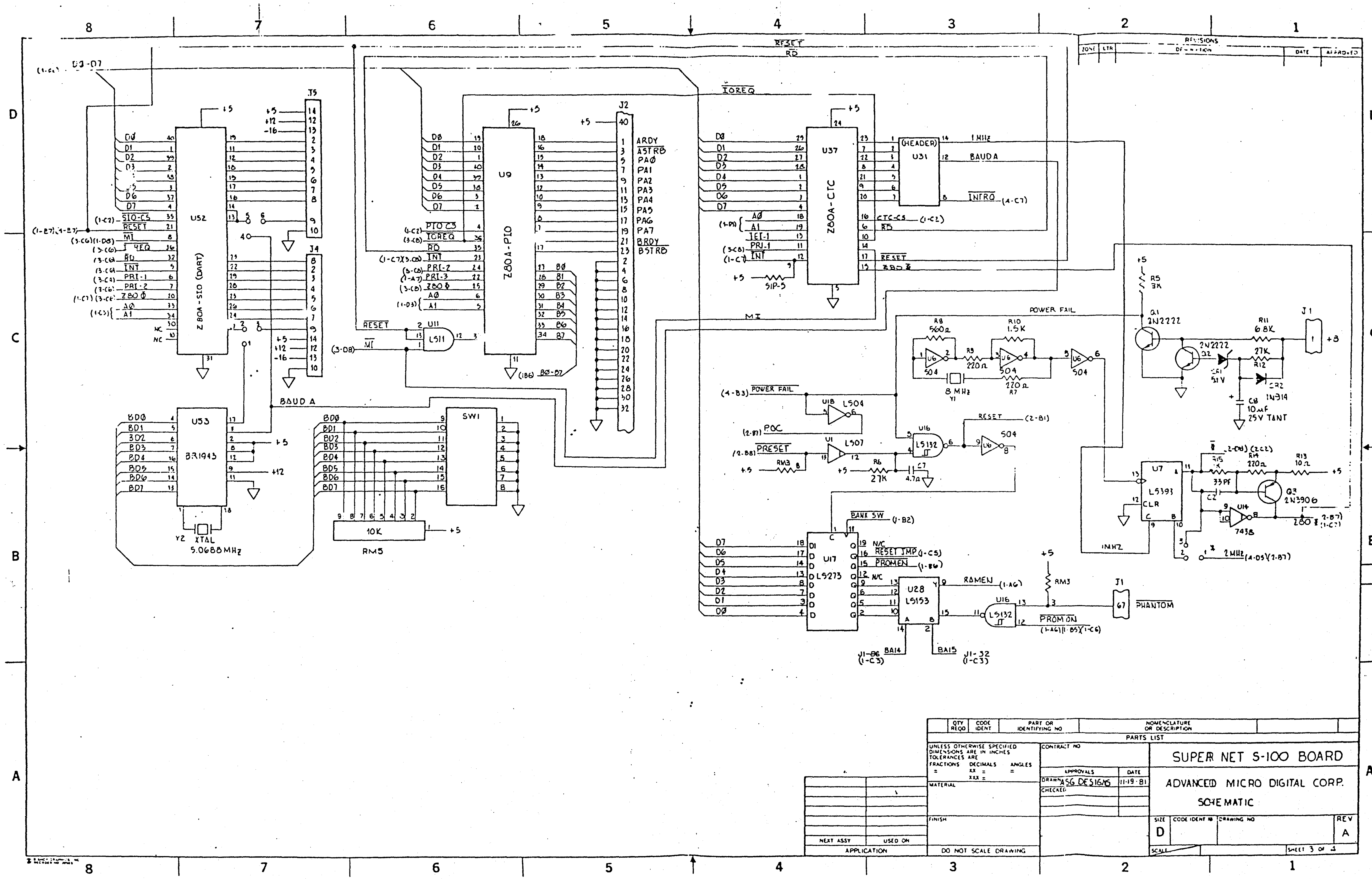
SCHEMATIC

SIZE	CODE IDENT NO	DRAWING NO	REV
D			A

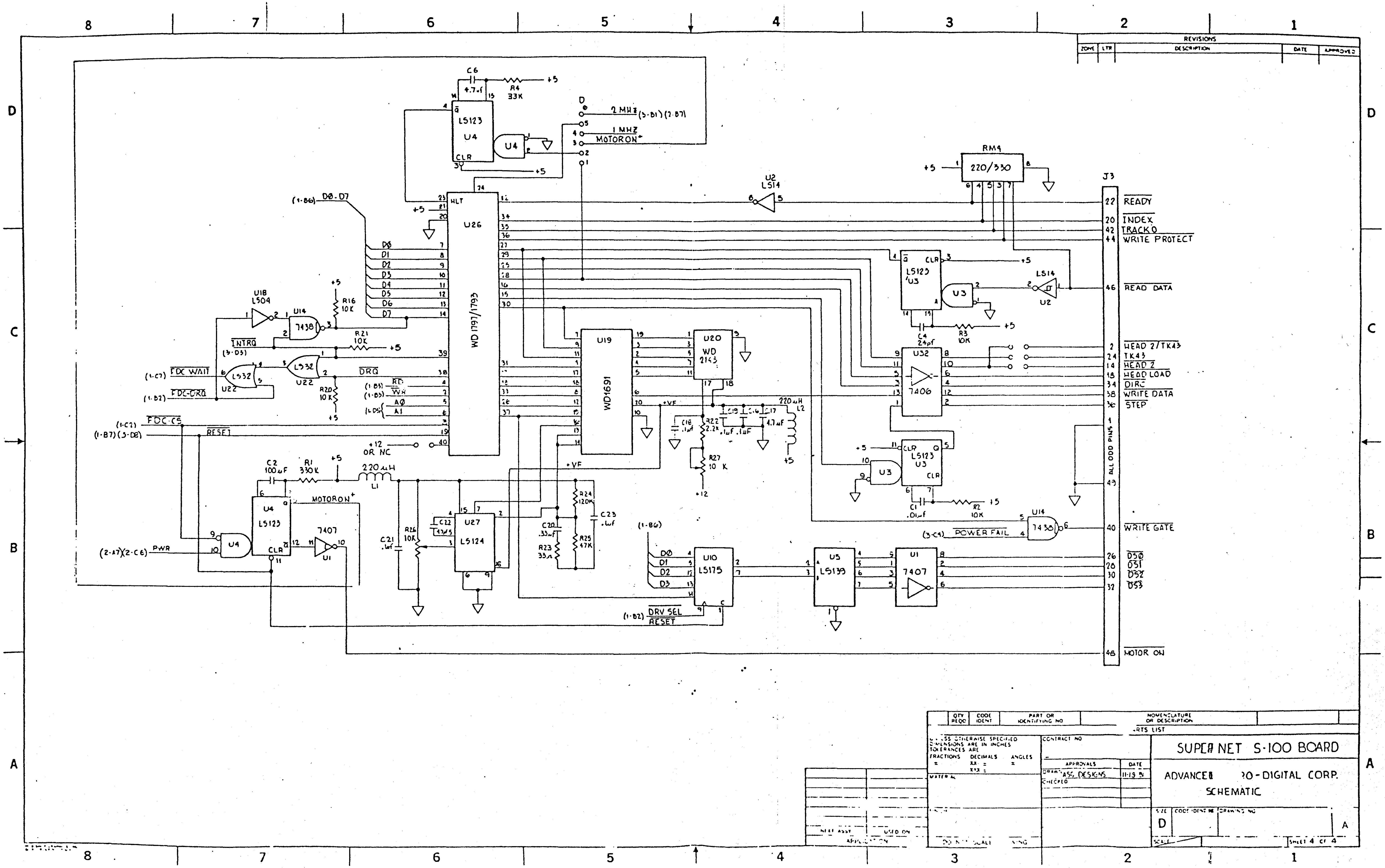
SCALE

SHEET 2 OF 4

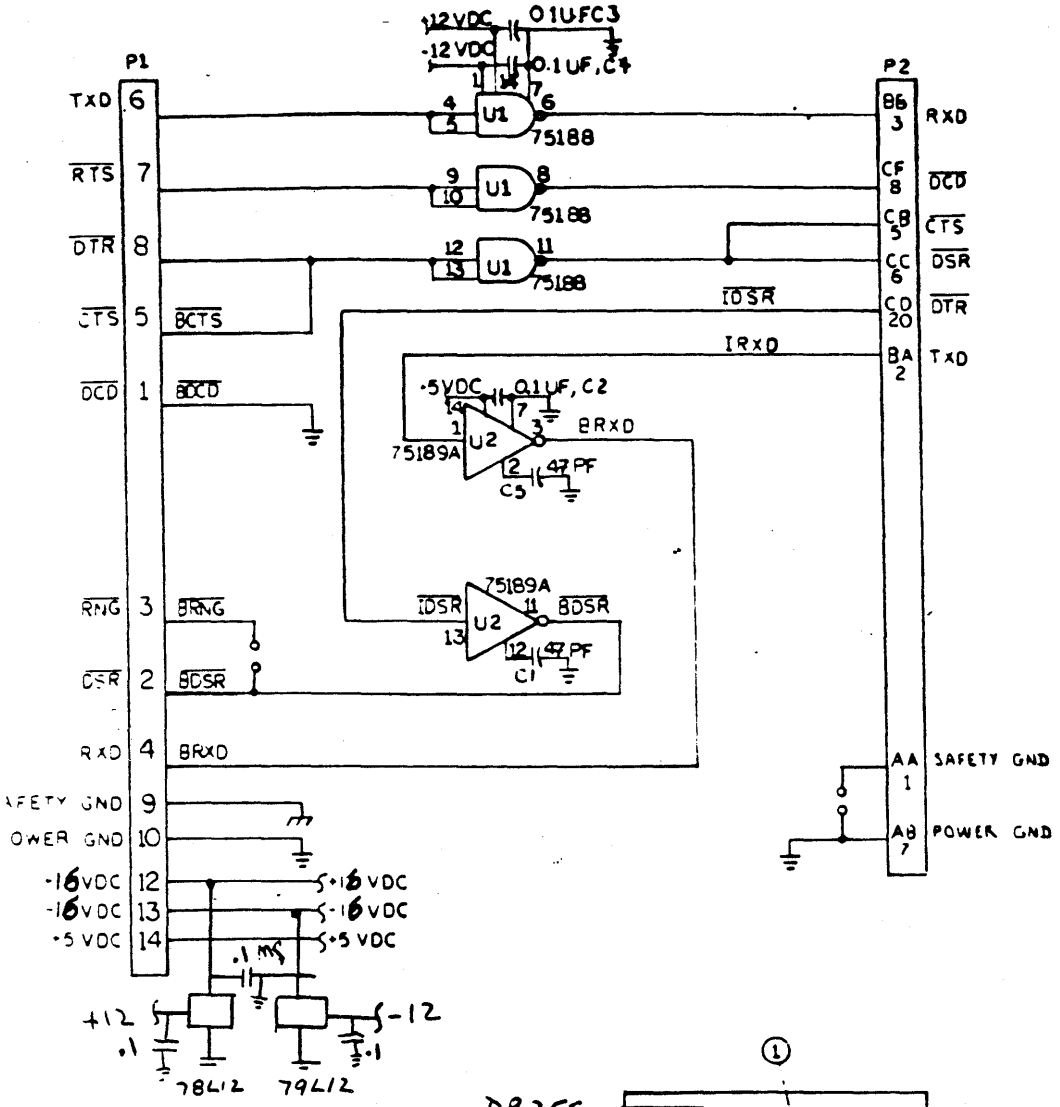
NEXT ASSY	USED ON
APPLICATION	

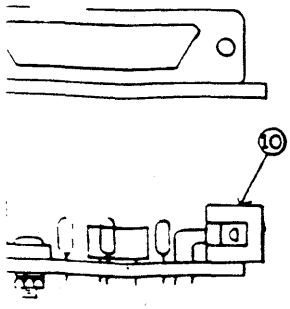


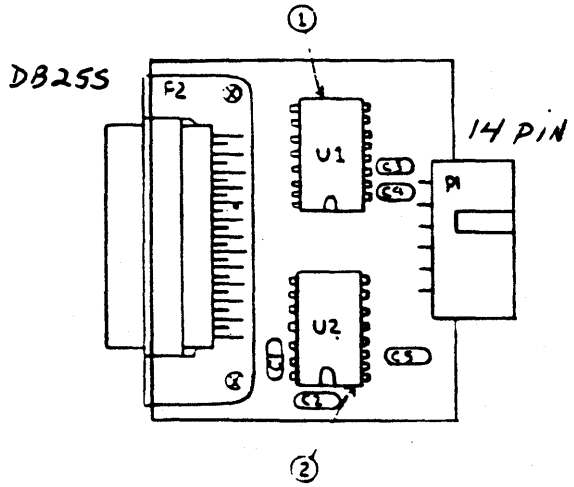
Z80A-SIO (DART)
U52
U53
BR1943
XTAL
5.0688 MHz
SW1
10K
RM5
BAUD A
U9
Z80A-PIO
J2
J3
J4
U11
LS11
U37
Z80A-CTC
U31
(HEADER)
1 MHz
BAUDA
INTRO
RESET
RD
IOREQ
M1
POWER FAIL
R5 3K
Q1 2N2222
Q2 2N2222
R11 6.8K
J1
CR1 5.1V
CR2 1N914
C8 10 µF 25V TANT
R8 560Ω
R10 1.5K
R9 220Ω
R7 220Ω
8 MHz Y1
U6 504
U18 LS04
U16 LS132
U1 LS07
POC
PRESET
U7
LS393
Q3 2N3906
U14 7438
2 MHz
INHZ
U17
LS273
BANK SW
RESET JMP
PROMEN
U28
LS153
ROMEN
RM3
PHANTOM
PROM ON
BA14
BA15
REVISIONS
PARTS LIST
SUPER NET S-100 BOARD
ADVANCED MICRO DIGITAL CORP.
SCHEMATIC
DRAWN ASG DESIGNS 11-19-81
SIZE D
REV A
SHEET 3 OF 4
DO NOT SCALE DRAWING
APPLICATION
NEXT ASSY
USED ON



REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
C6 4.7uf R4 33K +5
LS123 U4 CLR
2 MHZ (3-B1) (2-B7)
1 MHZ
MOTORON
U4
(1-B6) DØ-D7
HLT
U26
WD 1797/1793
DØ D1 D2 D3 D4 D5 D6 D7
U18 LS04
U14 7438
R16 10K
R21 10K
INTRQ (3-D3)
FDC WAIT
FDC-DRQ
U22 LS32
DRQ
RD
WR
AØ
A1
FDC-CS
RESET
+12 OR NC
U19
WD1691
U20 WD 2143
R22 2.2K
R27 10 K
+12
220uH L2
C17 4.7uF
U2 LS14
RM4 220/330
J3
READY
INDEX
TRACK0
WRITE PROTECT
LS123 U3 CLR
C4 24pf
R3 10K
READ DATA
U32 7406
HEAD 2/TK43
TK43
HEAD 2
HEAD LOAD
DIRC
WRITE DATA
STEP
ALL ODD PINS
LS123 U3
C1 .01uf
R2 10K
U14 7438
WRITE GATE
POWER FAIL
C2 100uF R1 330K
220uH L1
MOTORON
U4 LS123
7407 U1
PWR (2-A7)(2-C6)
C21 .1uF
R26 10K
C22
U27 LS124
+VF
R24 120K
C20 .33uF
R23 33Ω
R25 47K
C23 .1uF
(1-B6)
U10 LS175
DRV SEL
RESET
U5 LS139
U1 7407
DS0 DS1 DS2 DS3
MOTOR ON
PART OR IDENTIFYING NO
NOMENCLATURE OR DESCRIPTION
PARTS LIST
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE
CONTRACT NO
APPROVALS DATE
DRAWN MASS DESIGNS 11-19-81
CHECKED
SUPER NET S-100 BOARD
ADVANCE RO-DIGITAL CORP.
SCHEMATIC
SIZE D
A
SHEET 4 OF 4







ENG. H/A
10-1-81

PS NET/I

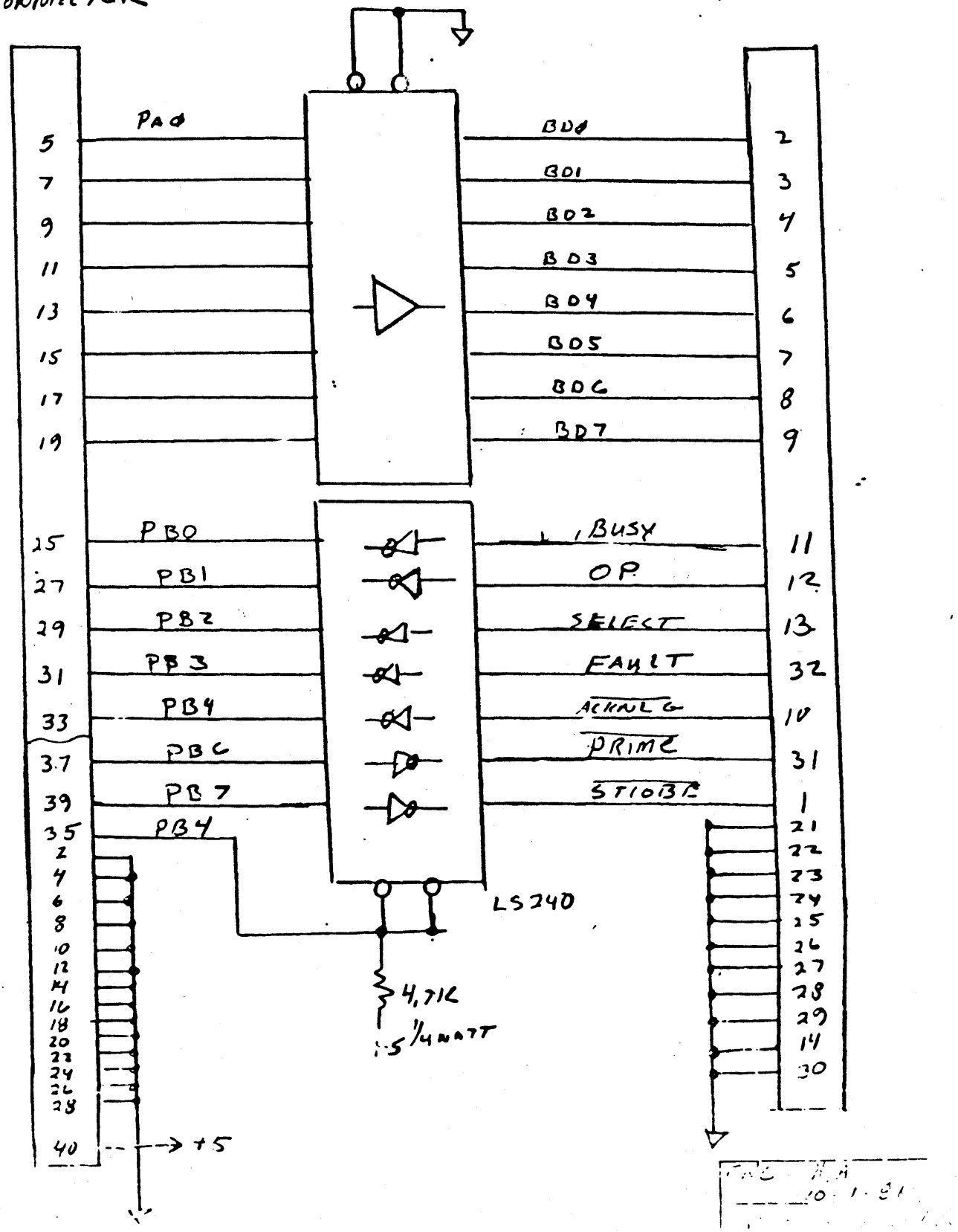
ADVANCED MICRO DE

Amphenol
57-40360

LS244

P10 CONNECTOR

TO PRINTER



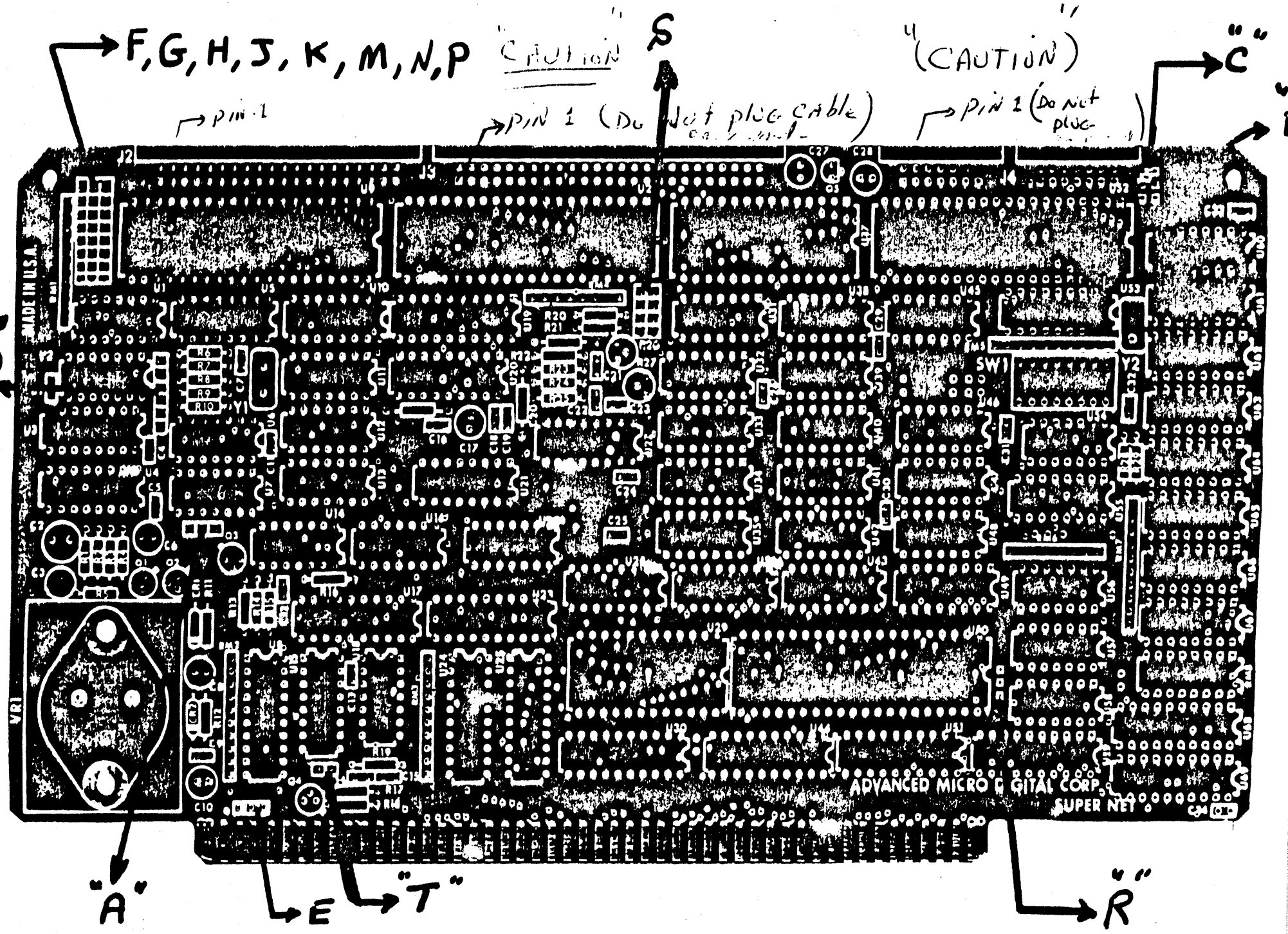
Dear Customer,

This is the board lay out of SUPER NET with jumper areas. Be sure to notice that Pin 1 of the header connector on the top of the board is on the left, do not plug disk and I/O cable in backward.

MAY CAUSE DAMAGES.

Thank you,

Advanced Micro Digital Corp.


F, G, H, J, K, M, N, P
CAUTION
pin 1
pin 1 (Do Not plug cable)
(CAUTION)
pin 1 (Do Not plug
"C"
"A"
E
"T"
"R"
MADE IN U.S.A.
ADVANCED MICRO DIGITAL CORP.
SUPER NET
SW1
Y1
Y2
VR1

Pin #	Name	Description
1	+8 VOLTS	DC power.
2	+16 VOLTS	DC power.
3	XRDY	One of two ready inputs to the current bus master. The bus is ready when both these ready signals are true. See pin 72.
4	$\overline{VI0}$	Vectored interrupt line 0.
5	$\overline{VI1}$	Vectored interrupt line 1.
6	$\overline{VI2}$	Vectored interrupt line 2.
7	$\overline{VI3}$	Vectored interrupt line 3.
8	$\overline{VI4}$	Vectored interrupt line 4.
9	$\overline{VI5}$	Vectored interrupt line 5.
10	$\overline{VI6}$	Vectored interrupt line 6.
11	$\overline{VI7}$	Vectored interrupt line 7.
12	$\overline{NMI}$	Non-maskable interrupt.
13	$\overline{PWRFAIL}$	Power fail bus signal.
14	$\overline{DMA3}$	Temporary master priority bit 3.
15	A18	Extended address bit 18.
16	A16	Extended address bit 16.
17	A17	Extended address bit 17.
18	$\overline{SDSB}$	The control signal to disable the 8 status signals.
19	$\overline{CDSB}$	The control signal to disable the 5 control output signals.
20	GND	Common with pin 100.
21	NDEF	Not to be defined. Manufacturer-specified line.
22	$\overline{ADSB}$	The control signal to disable the 16 address signals.
23	$\overline{DODSB}$	The control signal to disable the 8 data output signals.
24	ϕ	The master timing signal for the bus.
25	$\overline{pSTVAL}$	Status valid strobe.
26	pHDLA	A control signal used in conjunction with $\overline{HOLD}$ to coordinate bus master transfer operations.
27	RFU	Reserved for future use.
28	RFU	Reserved for future use.
29	A5	Address bit 5.
30	A4	Address bit 4.
31	A3	Address bit 3.
32	A15	Address bit 15.
33	A12	Address bit 12.
34	A9	Address bit 9.
35	DO1/DATA1	Data out bit 1, bidirectional bit 1.
36	DO0/DATA0	Data out bit 0, bidirectional bit 0.
37	A10	Address bit 10.
38	DO4/DATA4	Data out bit 4, bidirectional bit 4.
39	DO5/DATA5	Data out bit 5, bidirectional bit 5.

Pin #	Name	Description
40	DO6/DATA6	Data out bit 6, bidirectional bit 6.
41	DI2/DATA10	Data in bit 2, bidirectional bit 10.
42	DI3/DATA11	Data in bit 3, bidirectional bit 11.
43	DI7/DATA15	Data in bit 7, bidirectional bit 15.
44	sM1	The status signal which indicates that the current cycle is an opcode fetch.
45	sOUT	The status signal identifying the data transfer bus cycle to an output device.
46	sINP	The status signal identifying the data transfer bus cycle from an input device.
47	sMEMR	The status signal identifying bus cycles which transfer data from memory to a bus master, which are not interrupt acknowledge instruction fetch cycle(s).
48	sHTLA	The status signal which acknowledges that a HLT instruction has been executed.
49	CLOCK	2 mHz clock. Not required to be synchronous with any other bus signal.
50	GND	Common with pin 100.
51	+8 VOLTS	Common with pin 1.
52	-16 VOLTS	DC power.
53	GND	Common with pin 100.
54	$\overline{\text{SLAVE CLR}}$	A reset signal to reset bus slaves. Must be active with $\overline{\text{POC}}$ and may also be generated by external means.
55	$\overline{\text{CMA0}}$	Temporary master priority bit 0.
56	$\overline{\text{CMA1}}$	Temporary master priority bit 1.
57	$\overline{\text{CMA2}}$	Temporary master priority bit 2.
58	$\overline{\text{sXTRQ}}$	The status signal which requests 16-bit slaves to assert $\overline{\text{SIXTN}}$.
59	A19	Extended address bit 19.
60	$\overline{\text{SIXTN}}$	The signal generated by 16-bit slaves in response to the 16-bit request signal $\overline{\text{sXTRQ}}$.
61	A20	Extended address bit 20.
62	A21	Extended address bit 21.
63	A22	Extended address bit 22.
64	A23	Extended address bit 23.
65	NDEF	Not to be defined. Manufacturer-specified line.
66	NDEF	Not to be defined. Manufacturer-specified line.
67	$\overline{\text{PHANTOM}}$	A bus signal which disables normal slave devices and enables phantom slaves.
68	MWRT	$\overline{\text{sWO}}$-sOUT (logic equation).
69	RFU	Reserved for future use.

Pin #	Name	Description
70	GND	Common with pin 100.
71	RFU	Reserved for future use.
72	RDY	One of two ready inputs to the current bus master. The bus is ready when both these ready signals are true. See pin 3.
73	$\overline{INT}$	The primary interrupt request bus signal.
74	$\overline{HOLD}$	The control signal used in conjunction with pHDLA to bus master transfer operations.
75	$\overline{RESET}$	The reset signal to reset bus master devices. This signal must be active with $\overline{POC}$ and may also be generated by external means.
76	pSYNCH	The control signal identifying BS1.
77	$\overline{pWR}$	The control signal identifying the presence of valid data on DO bus or data bus.
78	pDBIN	The control signal that requests data on the DI bus or data bus from the currently addressed slave.
79	A0	Address bit 0 (least significant).
80	A1	Address bit 1.
81	A2	Address bit 2.
82	A6	Address bit 6.
83	A7	Address bit 7.
84	A8	Address bit 8.
85	A13	Address bit 13.
86	A14	Address bit 14.
87	A11	Address bit 11.
88	DO2/DATA2	Data out bit 2, bidirectional bit 2.
89	DO3/DATA3	Data out bit 3, bidirectional bit 3.
90	DO7/DATA7	Data out bit 7, bidirectional bit 7.
91	DI4/DATA12	Data in bit 4, bidirectional bit 12.
92	DI5/DATA13	Data in bit 5, bidirectional bit 13.
93	DI6/DATA14	Data in bit 6, bidirectional bit 14.
94	DI1/DATA9	Data in bit 1, bidirectional bit 9.
95	DI0/DATA8	Data in bit 0 (least significant bit for 8-bit data), bidirectional bit 8.
96	sINTA	The status signal identifying the bus input cycle(s) that may follow an accepted interrupt request presented on $\overline{INT}$.
97	$\overline{sWO}$	The status signal identifying a bus cycle which transfers data from a bus master to a slave.
98	$\overline{ERROR}$	The bus signal signifying and error condition during present bus cycle.
99	$\overline{POC}$	The power-on clear signal for all bus devices.
100	GND	System ground.