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AMC 95/1000 Series Random-Access Memory Board

User's Manual

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PREFACE

This manual provides general information, an installation and interface guide, principles of operation, and service information for the Advanced Micro Computer AMC 95/1032 32K byte and AMC 95/1016 16K byte Dynamic RAM Boards. Additional information may be obtained from the AMD Schottky and Low Power Schottky Data Book.

In this manual both active-high (positive true) and active-low (negative true) signals appear in the text. To eliminate confusion, and simplify presentation, the following convention is adhered to within this manual: whenever a signal is active-low (negative true), its mnemonic is followed by an asterisk (*) (i.e., MEMR* denotes an active-low signal). For a signal that is active-high the asterisk is omitted (i.e., IORW denotes an active-high signal).

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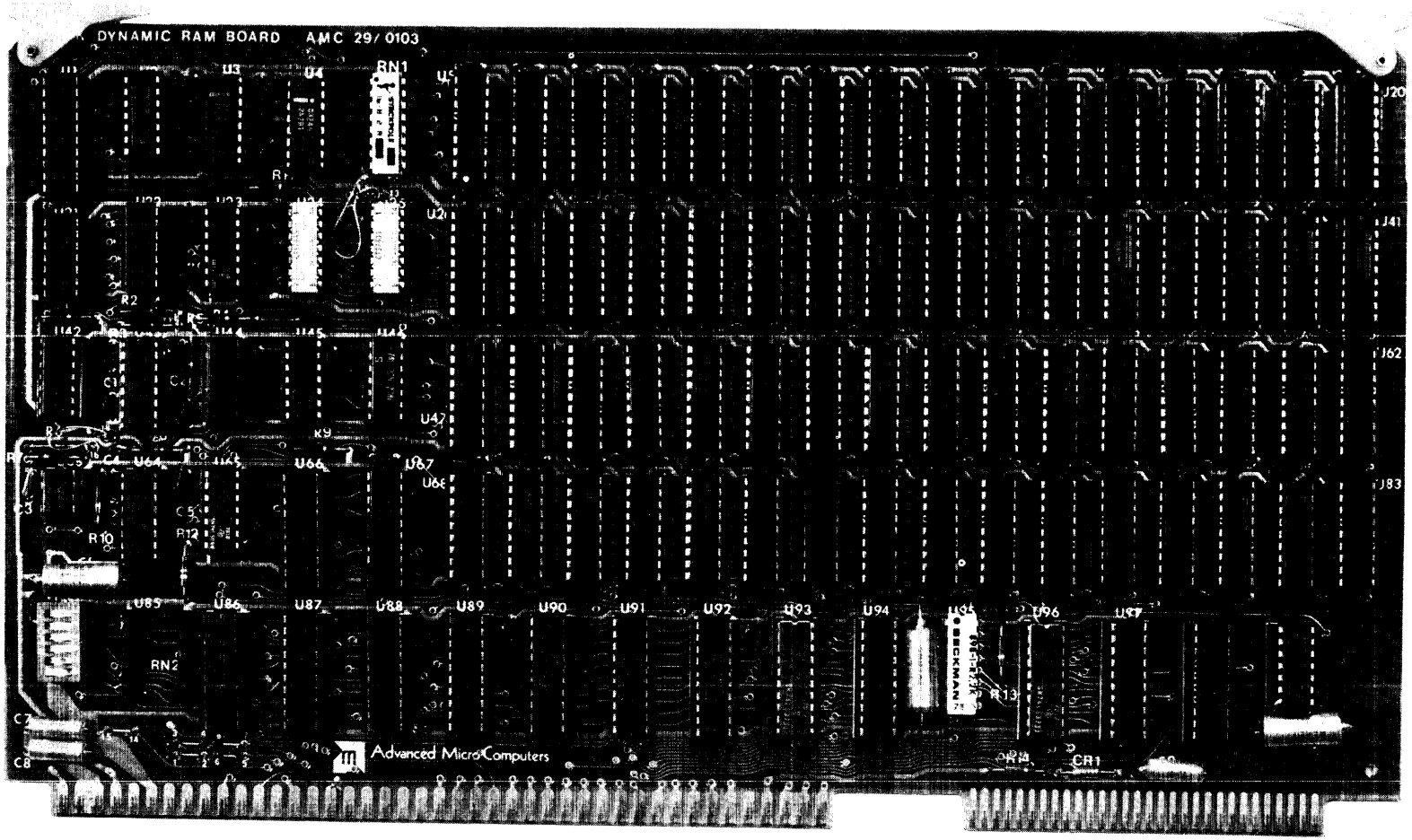
DYNAMIC RAM BOARD AMC 29/0103
RN1
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CHAPTER 1
GENERAL INFORMATION

1-1. INTRODUCTION

The AMC 95/1032 32K byte Dynamic RAM Board provides a 32K byte (8-bits) or 16K word (16-bits) memory system for System 29 Development Systems or Intel Multibus † compatible microcomputers. The AMC 95/1016 16K byte Dynamic RAM provides either a 16K byte (8-bits) or 8K word (16-bits) memory system. Interface to 16-bit computers is dependent upon the host processor activating the board's BHEN* signal. Address implementation allows the AMC 95/1032 to be placed in any 32K byte/16K word boundary and the AMC 95/1016 to be placed in any 16K byte boundary in a one megabyte address source. On-board refresh circuitry maintains the integrity of the stored data even when the support processor goes into a wait state.

1-2. PHYSICAL DESCRIPTION

The AMC 95/1032 and AMC 95/1016 Dynamic RAM Boards are built on standard SBC-80 printed circuit boards. They are designed to plug directly into a standard cardcage with an 86 pin backplane connector. Physical characteristics of the board are:

Board Dimensions

Width	30.48cm (12.00 inches)
Depth	17.15cm (6.75 inches)
Thickness	1.27cm (0.50 inches)

Environmental Requirements

Operating Temperature	0°C to 55°C
Relative Humidity	Up to 90% without condensation

†Multibus is a Trademark of Intel Corporation.

1-3. FUNCTIONAL DESCRIPTION

The AMC 95/1032 Dynamic RAM Board provides 32K bytes or 16K words of RAM memory using eight banks of eight Am9050EPC, 4K by 1-bit dynamic R/W Random Access Memories. Memory is configured into four even numbered banks and four odd numbered banks. When used with 8-bit computers, only one memory bank of eight RAMs is selected for each memory access. Even numbered banks are selected when address bit A0 is low and odd numbered banks are selected when A0 is high. Which particular bank is selected depends on address bits AD and AE. Bits AD and AE select one out of four odd or even banks. When used with 16-bit computers, two banks (one even and one odd) are selected. Two banks are selected when the byte high enable (BHEN*) is true (low). Otherwise, all operations are identical for 8-bit or 16-bit operation.

The AMC 95/1016 16KB Dynamic RAM Board provides 16K bytes or 8K words of RAM memory using four banks of eight Am9050 EPC, 4K by 1-bit dynamic R/W Random Access Memories. Memory is configured into two even numbered banks and two odd numbered banks. When used with 8-bit computers, only one memory bank of eight RAMs is selected for each memory access. Even numbered banks are selected when address bit A0 is low and odd numbered banks are selected when A0 is high. Which particular bank is selected depends on address bit AD. Bit AD selects one out of two odd or even banks. When used with 16-bit computers two banks (one even and one odd) are selected when the byte high enable (BHEN*) is true (low). Otherwise, all operations are identical for 8-bit or 16-bit operations.

There are three unique operations on the AMC 95/1032 and AMC 95/1016 memory

boards; memory read cycle, memory write cycle, and memory refresh cycle. The board only becomes active when it is addressed by the processor and not in a refresh cycle.

1-4. MEMORY READ CYCLE

When the MEMRD* signal is true (low) and an on-board memory address is placed on the address bus, a memory read cycle is initiated if the board is not inhibited by an external device or a memory refresh cycle is not in progress. When a memory read cycle is initiated, a chip enable (CE*) signal is applied to one of the memory banks after a predetermined delay has elapsed. In the case of a 16-bit operation, two CE* signals are applied to two memory banks. Data from the accessed memory location is latched into the data latch and the transfer acknowledge signal (XACK*) is forced true (low).

1-5. MEMORY WRITE CYCLE

During the memory write cycle, the MEMWR* signal is active and the appropriate address and write data is placed on each bus. The data transceiver is set to receive the data and it is written to the memory location. At the trailing edge of the CE* signal the transfer acknowledge (XACK*) is brought true (low) to let the processor know the transfer is complete.

1-6. REFRESH CYCLE

The on-board refresh timer requests a refresh cycle every 28µsec; a refresh cycle is initiated when there is not a memory read or write cycle is progress. When the refresh cycle is initiated, the refresh address generator outputs the refresh address. Once the refresh address is stable, the chip enable (CE*) signals are applied to all memory banks. At the trailing edge of the CE* signals the refresh address counter is incremented and the refresh cycle is complete. If a memory cycle is requested while the refresh cycle is in process, the memory cycle must wait for the completion of the refresh cycle before proceeding.

The reverse is also true: if a refresh cycle is requested while a memory read or write cycle is in process, the refresh cycle must wait for the completion of the memory cycle before proceeding.

1-7. SPECIFICATIONS

Specifications for the AMC 95/1032 and AMC 95/1016 Dynamic RAM Boards are listed in table 1-1.

TABLE 1-1. SPECIFICATIONS.

Memory Capactiy		
AMC 95/1032	32K by 8-bit or 16K by 16-bit	
AMC 95/1016	16K by 8 bit or 8K by 16-bit	
Data Word	8-bit or 16-bit	
Memory Addressing		
AMC 95/1032	Any 32K segment between 0 and 1024K	
AMC 95/1016	Any 16K segment between 0 and 1024K	
Cycle Times		
Read	510/610ns†	
Write	510/610ns†	
Refresh	450nsec	
Power Requirements	Typical	Maximum
+5 Volt	0.8A (Avg)	1A (Avg)
+12 Volt	130mA (Peak)	150mA (Peak)
-12 Volt	26.3mA (Avg)	32.4mA (Avg)

†Avanced Write Selected

CHAPTER 2

INSTALLATION AND INTERFACE

2-1. INTRODUCTION

This section provides information for installing and interfacing the AMC 95/1032 and AMC 95/1016 Dynamic RAM Boards. These instructions include unpacking and inspection, power requirements, cooling requirements, user selectable options, bus interface characteristics, and connector pin assignments.

2-2. UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or water-stained, request the carrier's agent to be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents are damaged, keep the carton and packing material for the agent's inspection. Shipping damages should be immediately reported to the carrier.

NOTE

Do not attempt to service the board yourself as this will void the warranty!

2-3. POWER REQUIREMENTS

The AMC Dynamic RAM Boards require +5, +12, and -12 volt power supply inputs. The current required for these supplies are listed in table 1-1. It is necessary to ensure that the system power supply has sufficient current margins to accomodate the AMC 32K Dynamic RAM Board requirements.

2-4. COOLING REQUIREMENTS

The AMC Dynamic RAM Board dissipates approximately 150 gram-calories/minute (0.6 Btu/minute) and adequate air circulation must be provided to prevent a temperature rise above 55°C (130°F).

2-5. USER SELECTABLE OPTIONS FOR THE AMC95/1032

The AMC 95/1032 32K Dynamic RAM Board is designed to operate either as a 32K by 8-bit or 16K by 16-bit memory board. Optional switch settings and jumpers are required. The following paragraphs provide instructions for optional switch and jumper configurations. Table 2-1 is a summary of the jumper requirements for each operating configuration.

2-6. BYTE HIGH ENABLE (BHEN*)

The Byte High Enable signal (BHEN*) (P1-27) is used to select two memory banks when the board is used with a 16-bit system. A jumper must be installed (jumper pins 14 and 15) to connect BHEN*, and the host computer must pull BHEN* to a logic low for 16-bit operation.

2-7. ADDRESS SELECTION

Address selection is accomplished via address bus bits A0 through A13 and the Byte High Enable (BHEN*) signal. The following are brief summaries of all address selection bits.

A0	Even/odd memory bank selection. When A0 is low, even numbered banks are selected. When A0 is high, odd numbered banks are selected.

TABLE 2-1. JUMPER CONFIGURATION SUMMARY FOR THE AMC 95/1032 BOARD.

Operation	Remove Jumper If Any	Install Jumper
32K Byte	10-11, 12-13, 14-15	9-11
16K Word	10-11, 12-13	9-11, 14-15
System 29	1-2, 3-4, 5-6, 7-8, 14-15	
Multibus Compatible Systems		1-2, 3-4, 5-6, 7-8
Normal Write Operation	17-18	16-18
Advanced Write Operation	16-18	17-18

A1 through AC	Memory location selection within each memory bank.
AD and AE	Memory bank (4K by 8 bits) selection.
AF through A13	Memory board location. The board can be placed on any 32K byte boundary up to 1M byte.
BHEN*	Used in conjunction with A0 to select two memory banks simultaneously for 16-bit data operation.

2-8. MEMORY BOARD LOCATION

Switch S1 provides the means to select the memory board location. By properly selecting the switch position, the board can be placed in any 32K byte boundary. Address bits AF through A13 define the 32K byte boundaries as shown in table 2-2. Switch S1 positions 1 through 5 must match address lines A13 through AF respectively. A zero in table 2-2 indicates that the corresponding switch must be in the OPEN position; a one indicates that the switch must be closed. Address bits AF through A13 must be 1 or 0 as shown in the table. Switch S1-6 must always be closed for a 32K byte board.

Address inputs A10 through A13 and BHEN* are provided with jumper options, jumper pins 1 through 8, 13 and 14. When the board is installed in System 29, all jumpers must be removed from these jumper pins.

2-9. MEMORY BANK SELECTION

When a jumper is installed between jumper pins 9 and 11 and the jumper is removed between jumper pins 12 and 13, address bit AE together with bits AD and A0 select the memory bank for 8-bit operation. Table 2-3 shows the memory bank selection for 8-bit configuration.

When operating with a 16-bit configuration a jumper must be installed between jumper pins 14 and 15. This configuration selects two memory banks for each address; however, address bit A0 must always be a logic low to access 16 data

TABLE 2-2. ADDRESS BITS AF THROUGH A13 DECODE.

A13	A12	A11	A10	AF	Selected
0	0	0	0	0	0 - 32K
0	0	0	0	1	32K - 64K
0	0	0	1	0	64K - 96K
0	0	0	1	1	96K - 128K
0	0	1	0	0	128K - 160K
0	0	1	0	1	160K - 192K
0	0	1	1	0	192K - 224K
0	0	1	1	1	224K - 256K
0	1	0	0	0	256K - 288K
0	1	0	0	1	288K - 320K
0	1	0	1	0	320K - 352K
0	1	0	1	1	352K - 384K
0	1	1	0	0	384K - 416K
0	1	1	0	1	416K - 448K
0	1	1	1	0	448K - 480K
0	1	1	1	1	480K - 512K
1	0	0	0	0	512K - 544K
1	0	0	0	1	544K - 576K
1	0	0	1	0	576K - 608K
1	0	0	1	1	608K - 640K
1	0	1	0	0	640K - 672K
1	0	1	0	1	672K - 704K
1	0	1	1	0	704K - 736K
1	0	1	1	1	736K - 768K
1	1	0	0	0	768K - 800K
1	1	0	0	1	800K - 832K
1	1	0	1	0	832K - 864K
1	1	0	1	1	864K - 896K
1	1	1	0	0	896K - 928K
1	1	1	0	1	928K - 960K
1	1	1	1	0	960K - 992K
1	1	1	1	1	992K - 1024K

bits simultaneously. The memory bank selection for this configuration is shown in table 2-4.

When operating with 16-bit computers, 8-bit memory reads or writes can be accomplished. Table 2-5 shows memory bank selection for 8-bit memory accesses when used as a 16-bit board.

TABLE 2-3. 8-BIT MEMORY BANK SELECTION.

Bits				Selected Bank
AE	AD	AO	BHEN*	
0	0	0	1	Bank 0
0	0	1	1	Bank 1
0	1	0	1	Band 2
0	1	1	1	Bank 3
1	0	0	1	Bank 4
1	0	1	1	Bank 5
1	1	0	1	Bank 6
1	1	1	1	Bank 7

TABLE 2-4. 16-BIT MEMORY BANK SELECTION.

Bits				Selected Bank
AE	AD	AO	BHEN*	
0	0	0	0	Bank 0, Bank 1
0	1	0	0	Bank 2, Bank 3
1	0	0	0	Bank 4, Bank 5
1	1	0	0	Bank 6, Bank 7

2-10. USER SELECTABLE OPTIONS FOR THE AMC 95/1016

The AMC 32K Dynamic RAM Board is designed to operate either a 16K by 8-bit or 8K by 16-bit memory board. Optional switch settings and jumpers are required. The following paragraphs provide instructions for optional switch and jumper configurations. Table 2-6 is a summary of the jumper requirements for each operating configuration.

2-11. BYTE HIGH ENABLE (BHEN*)

The Byte High Enable signal (BHEN*) (P1-27) is used to select two memory banks when the board is used with a 16-bit system. A jumper must be installed (jumper pins 14 and 15) to connect BHEN* and the host computer must pull BHEN* to a logic low for 16-bit operation.

TABLE 2-5. 8-BIT MEMORY SELECTION WITH 16-BIT MACHINES.

AE	AD	BHEN*	A0	Bank Selected	Notes
0	0	0	1	Bank 1	Accesses Upper Bytes
0	1	0	1	Bank 3	
1	0	0	1	Bank 5	
1	1	0	1	Bank 7	
0	0	1	0	Bank 0	Accesses Lower Bytes
0	1	1	0	Bank 2	
1	0	1	0	Bank 4	
1	1	1	0	Bank 6	
0	0	1	1	Bank 1	Not used with 8086
0	1	1	1	Bank 3	
1	0	1	1	Bank 5	
1	1	1	1	Bank 7	

TABLE 2-6. JUMPER CONFIGURATION SUMMARY FOR THE AMC 95/1016 BOARD.

Operation	Remove Jumper If Any	Install Jumper
16K Byte 8K Word	9-11, 14-15 9-11	10-11, 12-13 10-11, 12-13, 14-15
System 29	1-2, 3-4, 5-6, 7-8, 14-15	
Multibus Compatible Systems		1-2, 3-4, 5-6, 7-8
Normal Write Operation	17-18	16-18
Advanced Write Operation	16-18	17-18

2-12. ADDRESS SELECTION

Address selection is accomplished via address bus bits A0 through A13 and the Byte High Enable (BHEN*) signal. The following are brief summaries of all address selection bits.

A0 — Even/odd memory bank selection. When A0 is low, even numbered banks are selected. When A0 is high, odd numbered banks are selected.

A1 through AC — Memory location selection within each memory bank.

AD — Memory bank selection.

AE through A13 — Memory board location. The board can be placed

in any boundary up to 1M byte.

BHEN* — Used in conjunction with A0 to select two memory banks simultaneously for 16-bit data operation.

2-13. MEMORY BOARD LOCATION

Switch S1 provides the means to select the memory board location. By properly selecting the switch position, the board can be placed in any 16K byte boundries. Address bits AE to A13 define the 16K byte boundries as shown in table 2-7. Switch S1 positions 1 through 6 must match address lines A13 through AE respectively. A zero in table 2-7 indicates that the corresponding switch must be in the OPEN position; a one indicates that the switch must be closed. Address bits AE through A13 must be 1 or 0 as shown in table 2-7. Address bit A14 is used to define 16K byte boundries for the board. When the board is used in a 16K byte or 8K word configuration, jumpers must be installed at jumper pins 10 and 11, and jumper pins 12 and 13. In this configuration address bit AE defines either lower (AE=0) or upper (AE=1) 16K byte locations as shwon in table 2-7.

Address inputs A10 through A13 and BHEN* are provided with jumper options, jumper pins 1 through 8, 13 and 14. When the board is installed in System 29, all jumpers must be removed from these jumper pins.

2-14. MEMORY BANK SELECTION

Address bits AD, A0 and the BHEN* signal provide memory bank selection. As with the AMC 95/1032 board, bit A0 selects odd or even memory banks. Bit AD selects one of two odd or even banks. When a jumper is installed between jumper pins 14 and 15, the BHEN* signal selects two memory banks for 16-bit operation. Memory bank selection for 8-bit and 16-bit operation is shown in tables 2-8 and 2-9 respectively. Figure 2-1 shows the physical bank layout for the 32K board. Banks 4, 5, 6, and 7 are not populated on the 16K boards.

NOTE

When used in 16-bit configuration, bit A0 must always be low in order to access a word. This note applies to both 16K and 32K boards.

2-15. ADVANCE WRITE

If the AMC 95/1032 or AMC 95/1016 Dynamic RAM Board is used in a system which outputs the memory write (MEMWR*) signal before valid data is available, a jumper must be installed between jumper pins 17 and 18, and the jumper between jumper pins 16 and 18 must be removed. Installing a jumper between jumper pins 17 and 18 delays the chip enable (CE*) and acknowledge (XACK*) by approximately 100nsec.

2-16. BUS INTERFACE CHARACTERISTICS

Connector P1 provides the bus interface for the AMC 95/1032 and AMC 95/1016 Dynamic RAM Boards. All communication flow is via connector P1. Connector P1 is an 86-pin double sided edge connector. Table 2-10 is a pin list for connector P1. Signal descriptions of the bus interface signals are given in table 2-11.

All input signals encounter a single low power Schottky TTL load except for the data lines. The data bus transceivers used are Am8304s. Electrical characteristics for the Am8304s are shown in table 2-12.

TABLE 2-7. ADDRESS BITS AE THROUGH A13 DECODE.

A13	A12	A11	A10	AF	AE	Selected
0	0	0	0	0	0	0 - 16K
0	0	0	0	0	1	16K - 32K
0	0	0	0	1	0	32K - 48K
0	0	0	0	1	1	48K - 64K
0	0	0	1	0	0	64K - 80K
0	0	0	1	0	1	80K - 96K
0	0	0	1	1	0	96K - 112K
0	0	0	1	1	1	112K - 128K
0	0	1	0	0	0	128K - 144K
0	0	1	0	0	1	144K - 160K
0	0	1	0	1	0	160K - 176K
0	0	1	0	1	1	176K - 192K
0	0	1	1	0	0	192K - 208K
0	0	1	1	0	1	208K - 224K
0	0	1	1	1	0	224K - 240K
0	0	1	1	1	1	240K - 256K
0	1	0	0	0	0	256K - 272K
0	1	0	0	0	1	272K - 288K
0	1	0	0	1	0	288K - 304K
0	1	0	0	1	1	304K - 320K
0	1	0	1	0	0	320K - 336K
0	1	0	1	0	1	336K - 352K
0	1	0	1	1	0	352K - 368K
0	1	0	1	1	1	368K - 384K
0	1	1	0	0	0	384K - 400K
0	1	1	0	0	1	400K - 416K
0	1	1	0	1	0	416K - 432K
0	1	1	0	1	1	432K - 448K
0	1	1	1	0	0	448K - 464K
0	1	1	1	0	1	464K - 480K
0	1	1	1	1	0	480K - 496K
0	1	1	1	1	1	496K - 512K

2-17. ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am7304B T_A = -55°C to +125°C
V_{CC}MIN = 4.5V V_{CC}MAX = 5.5V

Am8304B T_A = 0°C to +70°C
V_{CC}MIN = 4.75V V_{CC}MAX = 5.25V

DC electrical characteristics over operating temperature range are shown in table 2-12.

TABLE 2-7. ADDRESS BITS AE THROUGH A13 DECODE. (Cont.)

A13	A12	A11	A10	AF	AE	Selected
1	0	0	0	0	0	512K - 528K
1	0	0	0	0	1	528K - 544K
1	0	0	0	1	0	544K - 560K
1	0	0	0	1	1	560K - 576K
1	0	0	1	0	0	576K - 592K
1	0	0	1	0	1	592K - 608K
1	0	0	1	1	0	608K - 624K
1	0	0	1	1	1	624K - 640K
1	0	1	0	0	0	640K - 656K
1	0	1	0	0	1	656K - 672K
1	0	1	0	1	0	672K - 688K
1	0	1	0	1	1	688K - 704K
1	0	1	1	0	0	704K - 720K
1	0	1	1	0	1	720K - 736K
1	0	1	1	1	0	736K - 752K
1	0	1	1	1	1	752K - 768K
1	1	0	0	0	0	768K - 784K
1	1	0	0	0	1	784K - 800K
1	1	0	0	1	0	800K - 816K
1	1	0	0	1	1	816K - 832K
1	1	0	1	0	0	832K - 848K
1	1	0	1	0	1	848K - 864K
1	1	0	1	1	0	864K - 880K
1	1	0	1	1	1	880K - 896K
1	1	1	0	0	0	896K - 912K
1	1	1	0	0	1	912K - 928K
1	1	1	0	1	0	928K - 944K
1	1	1	0	1	1	944K - 960K
1	1	1	1	0	0	960K - 976K
1	1	1	1	0	1	976K - 992K
1	1	1	1	1	0	992K - 1008K
1	1	1	1	1	1	1008K - 1024K

TABLE 2-8. 8-BIT MEMORY BANK SELECTION.

Bits			Selected Bank
AD	A0	BHEN*	
0	0	1	Bank 0
0	1	1	Bank 1
1	0	1	Bank 2
1	1	1	Bank 3

TABLE 2-9. 16-BIT MEMORY BANK SELECTION.

Bits			Selected Bank
AD	A0	BHEN*	
0	0	0	Bank 0, Bank 1
0	1	0	Bank 1
1	0	0	Bank 2, Bank 3
1	1	0	Bank 3

TABLE 2-10. CONNECTOR P1 PIN ASSIGNMENTS.

Component Side			Circuit Side		
Pin	Mnemonic	Description	Pin	Mnemonic	Description
1	GND	Ground	2	GND	Ground
3	V_{CC}	+5V	4	V_{CC}	+5V
5	V_{CC}	+5V	6	V_{CC}	+5V
7	V_{DD}	+12V	8	V_{DD}	+12V
11	GND	Ground	12	GND	Ground
19	MEMRD*	Memory Read	20	MEMWR*	Memory Write
23	XACK*	XFER Acknowledge	24	INH*	Inhibit RAM
27	BHEN*	Byte High Enable	44	A15	Address
43	A14	Address	46	A13	Address
45	A12	Address	48	A11	Address
47	A10	Address	50	A9	Address
49	A8	Address	52	A7	Address
51	A6	Address	54	A5	Address
53	A4	Address	56	A3	Address
55	A2	Address	58	A1	Address
57	A0	Address	60	DB15	Data
59	DB14	Data	62	DB13	Data
61	DB12	Data	64	DB11	Data
63	DB10	Data	66	DB9	Data

TABLE 2-10. CONNECTOR P1 PIN ASSIGNMENTS. (Cont.)

Component Side			Circuit Side		
Pin	Mnemonic	Description	Pin	Mnemonic	Description
65	DB8	Data	68	DB7	Data
67	DB6	Data	70	DB5	Data
69	DB4	Data	72	DB3	Data
71	DB2	Data	74	DB1	Data
73	DB0	Data	76	GND	Ground
75	GND	Ground	80	V_{AA}	-12V
79	V_{AA}	-12V	82	V_{CC}	+5V
81	V_{CC}	+5V	84	V_{CC}	+5V
83	V_{CC}	+5V	86	GND	Ground
85	GND	Ground			

TABLE 2-11. BUS INTERFACE SIGNAL DESCRIPTIONS.

Signal	Description
A0-A13	Address: The 20 lines transmit the Address of the memory location. A0 is the LSB.
INH*	Inhibit RAM: This signal when active prevents the board from reacting. (Refresh cycle does not depend on this signal).
BHEN*	Byte High Enable: Enables the proper data path between RAM and the data buffer.
MEMRD*	Memory Read: When activated initiates memory access from given address and places accessed data on the data buffer.
MEMWR*	Memory Write: When activated initiates write cycle with the data on data inputs at specified address.
INIT*	Initialize: Preset the Refresh enable flip-flop.
XACK*	Transfer Acknowledge: Indicates to support processor that the requested memory cycle is completed. That is, data has been placed on or accepted from the system data bus.
DB0-DB15	Data: These 16 bidirectional lines transmit and receive data to and from the specified memory location. DB0 is the LSB.

TABLE 2-12. Am8304 ELECTRICAL CHARACTERISTICS.

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
		B PORT (B_0-B_7)					
V_{IH}	Logical "1" Input Voltage	CD = V_{IL} MAX., T/$\overline{R}$ = V_{IL} MAX.		2.0			Volts
V_{IL}	Logical "0" Input Voltage	CD = V_{IL} MAX., T/$\overline{R}$ = V_{IL} MAX.	Am8304B			0.8	Volts
			Am7304B			0.7	
V_{OH}	Logical "1" Output Voltage	CD = V_{IL} MAX., T/$\overline{R}$ = 2.0V	I_{OH} = −0.4mA	V_{CC}−1.15	V_{CC}−0.8		Volts
			I_{OH} = −5mA	2.7	3.9		
			I_{OH} = −10mA	2.4	3.6		
V_{OL}	Logical "0" Output Voltage	CD = V_{IL} MAX., T/$\overline{R}$ = 2.0V	I_{OL} = 20mA		0.3	0.4	Volts
			I_{OL} = 48mA		0.4	0.5	
I_{OS}	Output Short Circuit Current	CD = V_{IL} MAX., T/$\overline{R}$ = 2.0V, V_O = 0V, V_{CC} = MAX., Note 2		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	CD = V_{IL} MAX., T/$\overline{R}$ = V_{IL} MAX., V_I = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = MAX., V_I = V_{CC} MAX.				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL} MAX., T/$\overline{R}$ = V_{IL} MAX., V_I = 0.4V			−70	−200	μA
V_C	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12mA			−0.7	−1.5	Volts
I_{OD}	Output/Input Three-State Current	CD = 2.0V	V_O = 0.4V			−200	μA
			V_O = 4.0V			200	

Notes: 1. All typical values given are for V_{CC} = 5.0V and T_A = 25°C.

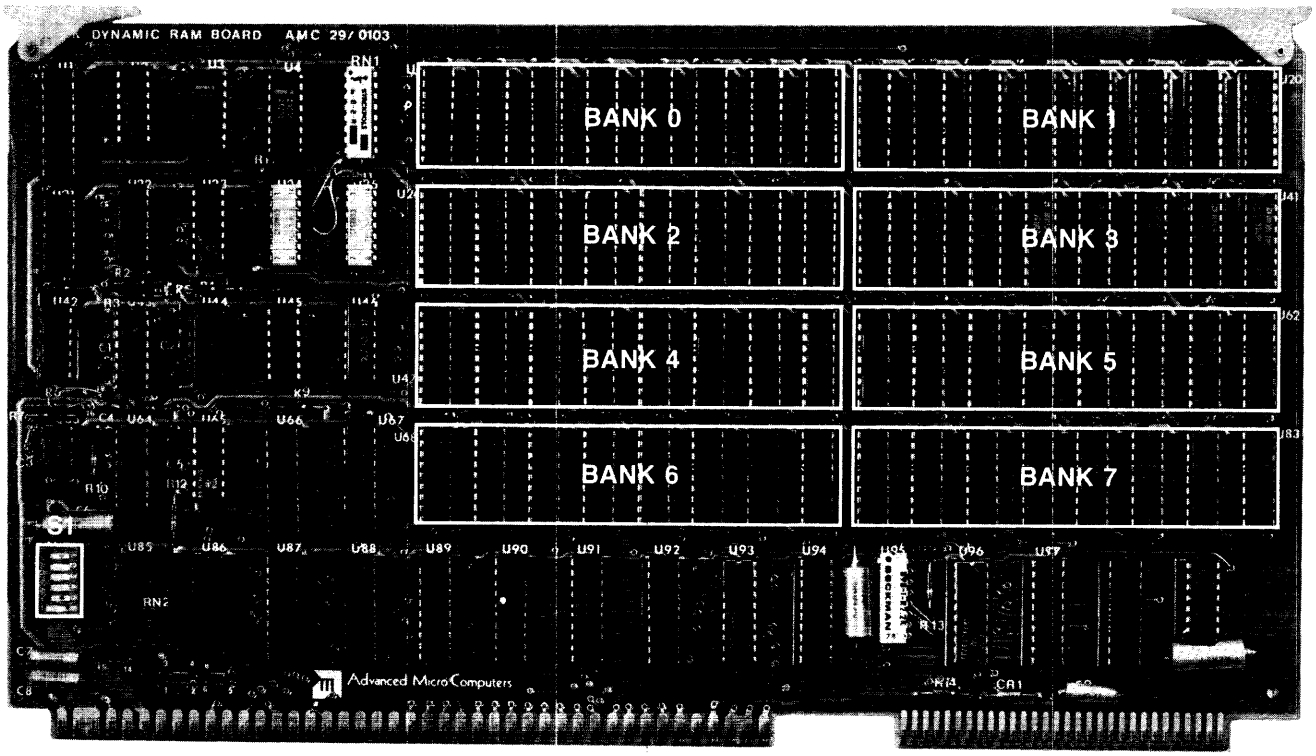


FIGURE 2-1. Physical Memory Bank Configuration.

CHAPTER 3
THEORY OF OPERATION

3-1. INTRODUCTION

The AMC 95/1032 and AMC 95/1016 Dynamic RAM Boards are functionally identical; therefore, no distinction will be made for the boards in theory of operation.

There are three unique operations that take place on the memory board. These operations are: Memory Read, Memory Write, and Memory Refresh. Figure 3-1 is a functional block diagram of the memory board.

3-2. MEMORY READ CYCLE

A memory read cycle is initiated when the MEMRD* input signal is true and a valid address is received on the address bus. The MEMRD* signal is gated with both the SEL (Board Select) and REFON* (Refresh On) signals to resolve request priorities. If a memory refresh is not in process (REFON* false), the memory read will be initiated.

A MEMON* signal is generated by the request resolver logic. The prioritized MEMON* signal triggers a 150 ns delay one-shot (U43). The output of delay one-shot (U43) and an inverted MEMON* are gated to generate the clear signal for the refresh enable flip-flop (U42, Pin 13), disabling the memory refresh logic while the memory read cycle is in progress. The direction of data flow through the data bus transceivers is controlled by inverting the MEMRD* input to the board. A high (true) on MEMRD enables data to be read from the data bus. The MEMRD signal also enables the read latches. Timing for the memory read cycle is shown in figure 3-2.

When the delay one-shot times out, the Q output triggers a 260ns one-shot (U64). The Q output (Pin 6) opens the data and triggers the OUTON flip-flop. Outputs Q and not Q of the OUTON flip-flop are gated with address bit 0 and the BHEN* signal to control communica-put (Pin 7) provides the Enable signal for the Chip Enable decoder. When the 260ns one-shot times out, the low going transition of the Q output loads memory data in the data latches and triggers an 800ns one-shot. The Q out-put (U64, Pin 10) of the 800ns one-shot is inverted through a tristate gate to provide the XACK* signal to the CPU. The 800ns one-shot is reset by either a change in the state (low to high transition) of the MEMRD* or by the 800ns time-out. When the 800ns one-shot resets, the refresh enable (REFEN) flip-flop is enabled and the read cycle is complete.

3-3. MEMORY WRITE CYCLE

A memory write cycle is initiated when the MEMWR* input signal is true and an address data and write data are received on the address bus and data bus respectively. The MEMWR* signal is gated with both the SEL and REFON* (Refresh On) signals to resolve request priorities. If a memory refresh cycle is not in progress, the MEMWR* signal provides the write enable (WE*) input to the memory chips. Timing for the memory write cycle is shown in figure 3-3.

A MEMON* signal is generated by the request resolver logic. The prioritized MEMON* signal triggers a 150ns delay one-shot (U43). The output of the delay one-shot (U43) and an inverted MEMON are gated to generate the clear signal for the refresh enable flip-flop (U42, Pin 13), disabling the memory refresh logic while the memory write cycle is

in progress. When the delay one-shot times out, the Q output triggers a 260 ns one-shot (U64). The not Q output (Pin 7) provides the Enable signal for the Chip Enabler decoder. When the 260 ns one-shot times out, the low going transition of the Q output triggers an 800ns one-shot. The Q output (U64, Pin 10) of the 800ns one-shot is inverted through a tristate gate to provide the XACK* signal to the CPU. The 800ns one-shot is reset by either a change in the state (low to high transition) of the MEMWR* or by the 800ns time-out. When the 800ns one-shot resets the refresh enable (REFEN), flip-flop is enabled and the write cycle is complete.

The direction of data flow through the data bus transceivers is controlled by inverting the MEMRD* input to the board. A low (false) MEMRD* enables data to be written to memory from the data bus.

3-4. MEMORY REFRESH CYCLE

The on-board refresh timer U63 requests a refresh cycle approximately every 28 µsec. Timing for the refresh cycle is shown in figure 3-4. The refresh timer (U63) clocks the Refresh Request (REFREQ) flip-flop (U42) on every low to high transition. When Pin 5 of U42 goes high, it is gated with the Refresh Enable output of U42 Pin 9. When there is not a memory read or write cycle in progress, the gating of U42 Pin 5 and U42 Pin 9 (REFEN F/F) triggers a 450ns refresh one-shot (43) and a 150ns delay one-shot. When REFON* (U43 Pin 9) goes low, the request resolver is forced high, which tristates the system address bus. The REFON* signal also enables the refresh counter to output the refresh address. While the REFON* signal is active, the column addresses are forced to logical low.

The REFON* signal gates off the MEMWR* and MEMRD* signals, and any memory access request will be held off until the refresh cycle is completed and the REFON* signal is deactivated. The output of gating MEMWR* and REFON* disables the Write Enable (WE*) signal to the memory chips. REFON* is also applied to the clear input of Refresh Request flip-flop U42.

On the trailing edge of the 150ns delay one-shot (U43) the Q output is ANDed with the REFON*, and the output is applied to the E4 and POL inputs to the chip enable decoder. This forces all chip enable lines true, and accomplishes the simultaneous refresh of all memory banks.

When the 450ns one-shot (U43) times out, its not Q going high increments the refresh counter by one and floats its output. The Q output of the 450ns one-shot going high concurrently enables the address bus. This places the board in an idle state waiting for a memory read or write, or for the next refresh cycle.

3-5. MEMORY BANK SELECTION

Selection of memory banks is provided by address bits A0, AD, AE, and the BHEN* input. Address bits A0, AD, and AE are applied to a one-of-eight decoder. The four least significant output bits from the decoder provide chip select for the even numbered (0, 2, 4, and 6) memory banks. The four most significant outputs from the one-of-eight decoder select the odd numbered (1, 3, 5, and 7) memory banks. When used with 16-bit computers, the BHEN* signal is gated with each of the four outputs of the decoder (Y0, Y1, Y2 and Y3) to provide dual memory chip select. In this case one even and one odd memory bank is selected.

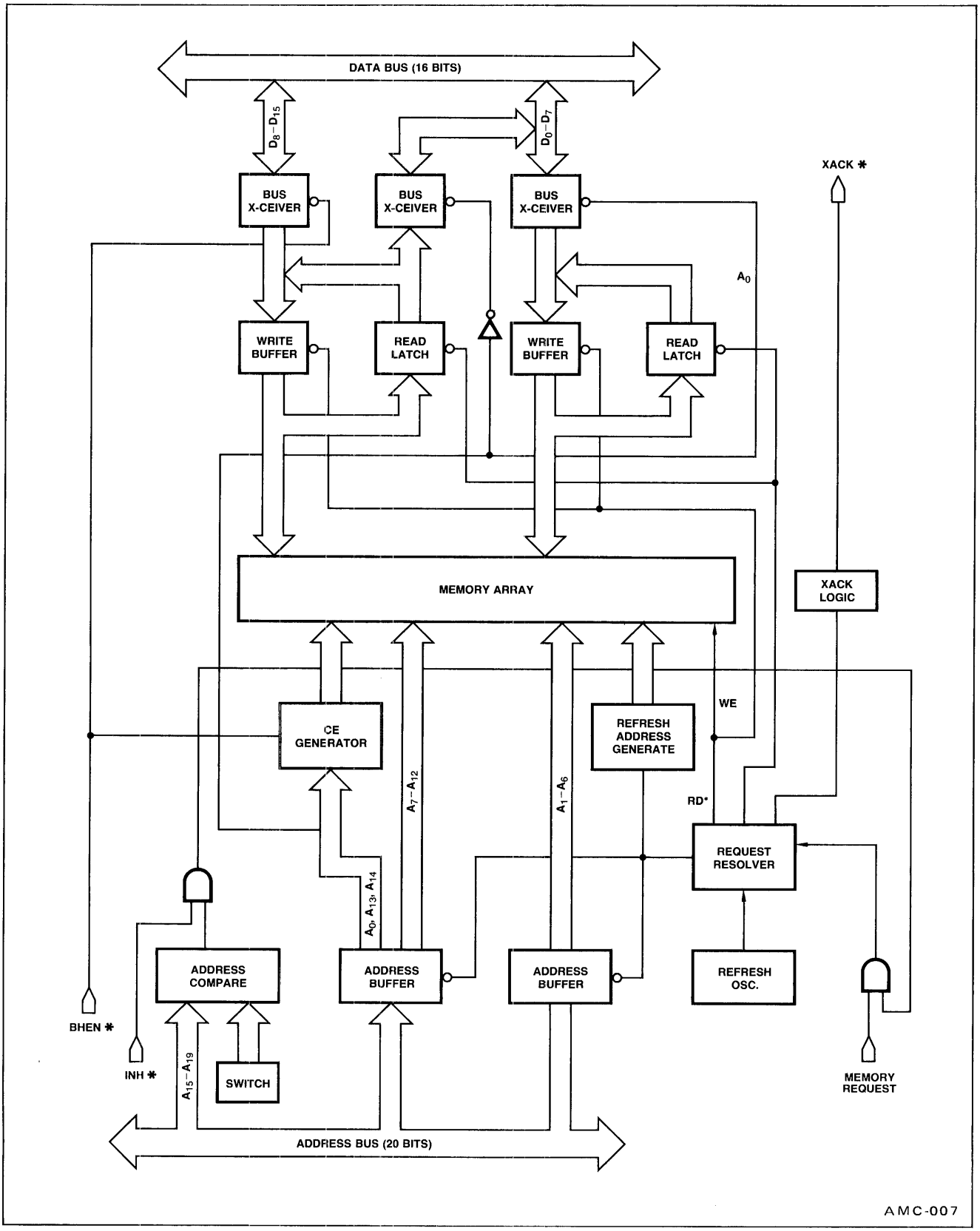


Figure 3-1. AMC 95/1032 and AMC 95/1016 Dynamic RAM Board Functional Block Diagram.

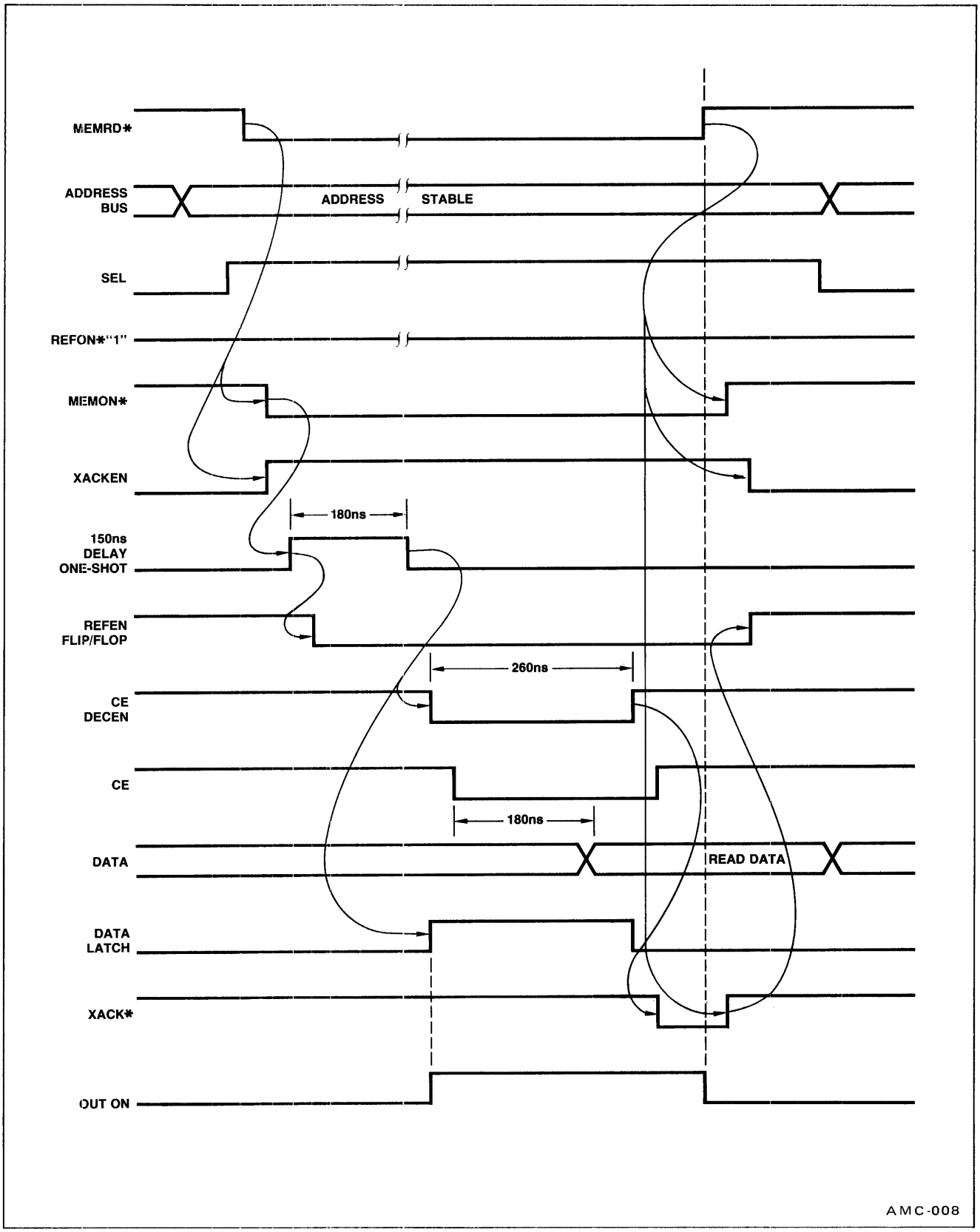


Figure 3-2. Memory Read Cycle Timing.

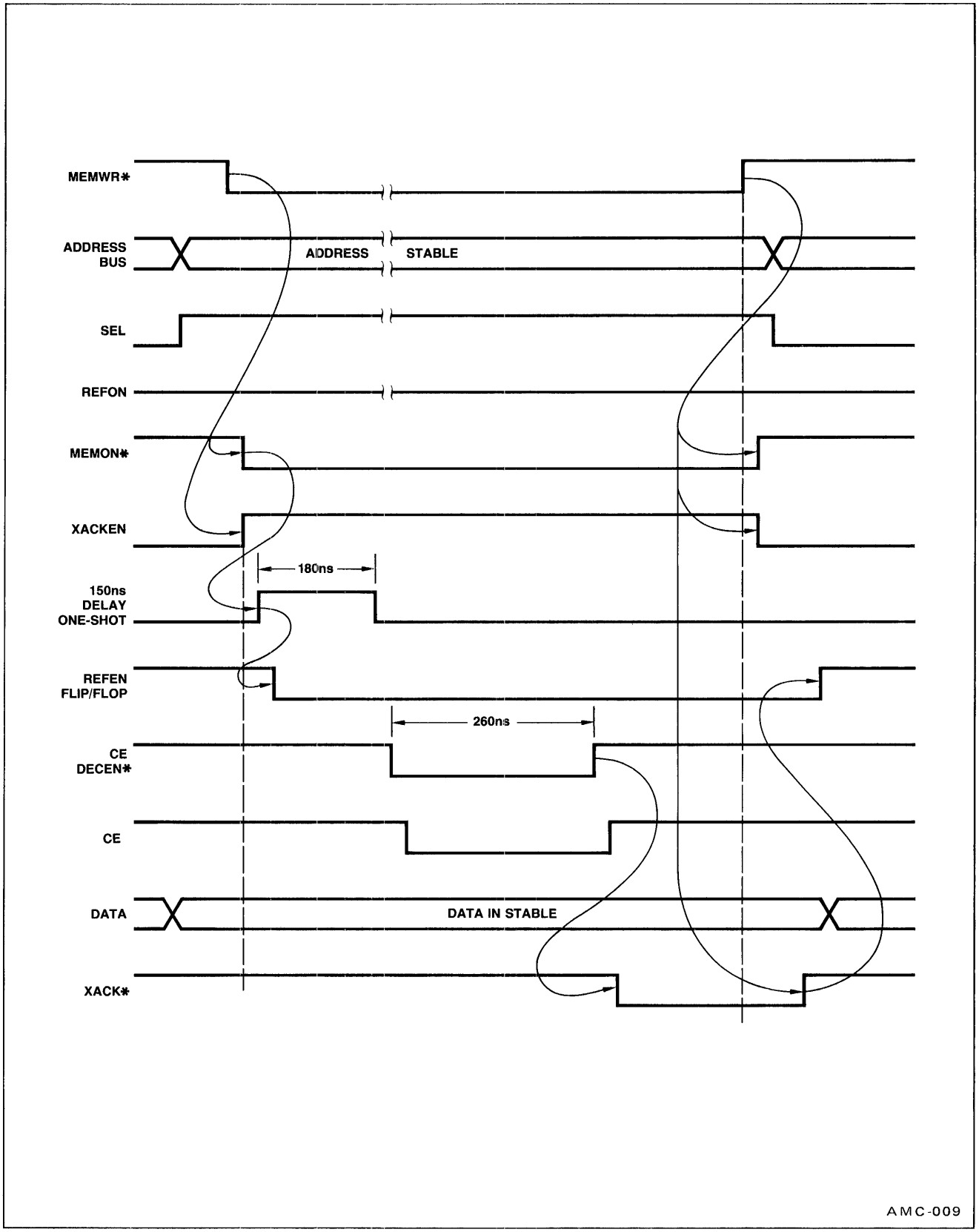
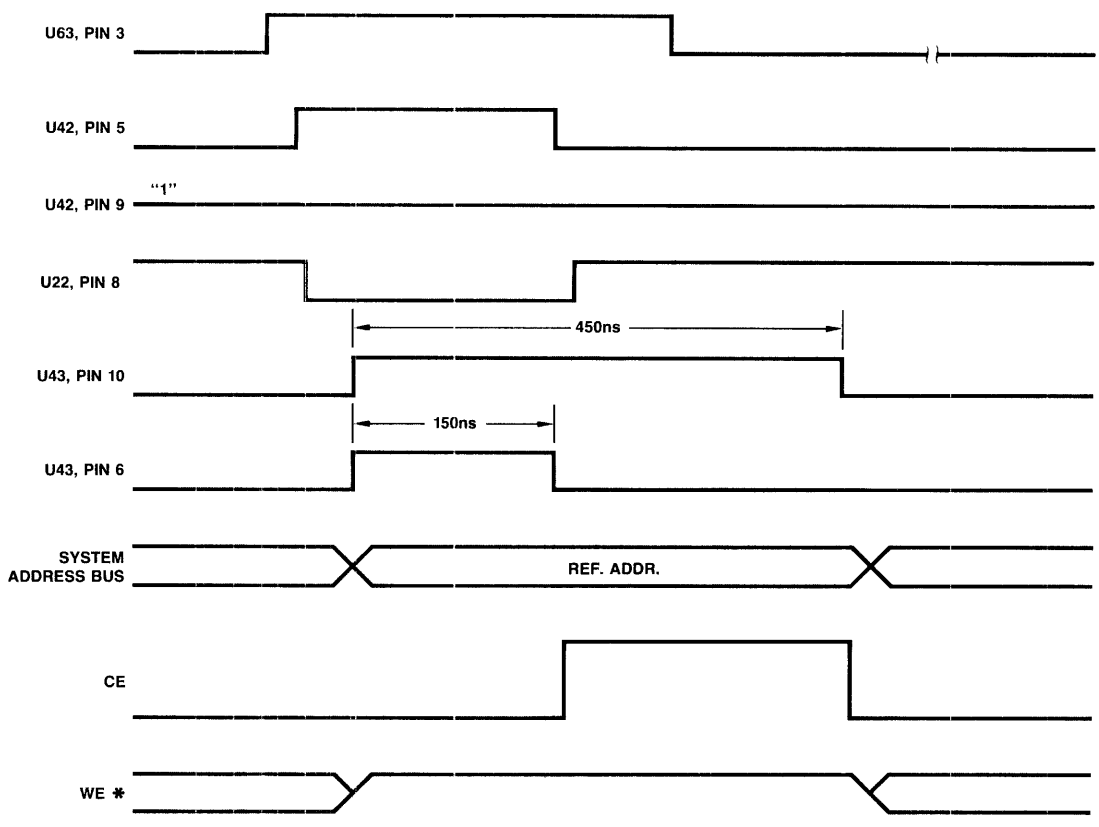


Figure 3-3. Memory Write Cycle Timing.



AMC-010

Figure 3-4. Memory Refresh Cycle Timing.

CHAPTER 4
SERVICE INFORMATION

4-1. INTRODUCTION

This chapter provides information on service and repair assistance, user replaceable parts and service diagrams for the AMC 95/1032 and AMC 95/1016 Dynamic RAM Boards.

4-2. SERVICE AND REPAIR ASSISTANCE

If it is necessary to return an AMC Dynamic RAM Board to Advanced Micro Computers for service or repair, contact the Service Manager for OEM Products at the telephone number listed below. A Return Material Authorization number must be obtained prior to shipment. When the reshipment is due to the board being damaged during shipment from AMC, or the board is out of warranty, a purchase order is required to complete the repair.

Repackage the board in the original packing material, or an equivalent substitute, and enclose in a corrugated carton suitable for shipping. Seal the shipping carton securely; mark it FRAGILE, and address to:

Advanced Micro Computers
Service Manager, OEM Products
3340 Scott Boulevard
Santa Clara, California 95051

TELEPHONE: (408) 988-7777

TOLL FREE:
California (800) 672-3548
U.S.A. (except California)
(800) 538-9791

4-3. USER REPLACEABLE PARTS

A list of all user replaceable parts for the AMC 95/1032 and AMC 95/1016 Dynamic RAM Boards is provided in table 4-1. Figure 4-1 is a component location diagram for the AMC 95/1016; figure 4-6 shows the component locations for the AMC 95/1032.

4-4. SERVICE DIAGRAMS

Schematic diagrams for the AMC 95/1016 are provided in figures 4-2 through 4-5; schematics for the AMC 95/1032 are provided in figures 4-7 through 4-12.

TABLE 4-1. USER REPLACEABLE PARTS.

AMC Part Number	Description	Location
0034-0011	Capacitor, .1µf, 50V 20%	C11 through C87
0034-0002	Capacitor, 22µf, 15V	C9
0034-0035	Capacitor, 47µf, 15V	C6, R10, C7, C8
0034-0014	Capacitor, 47pf, 500V, 5%	C4, C1
0034-0010	Capacitor, 100pf, 500V, 5%	C2
0034-0034	Capacitor, 470pf, 500V, 5%	C3, C5
0047-003	Card Extractor	
0020-0024	Decoder, one of eight 25LS2538	U1
0069-0016	DIP Switch, 6 Position	S1
0028-0008	Integrated Circuit, Type 3245	U3, U4
0020-0020	Integrated Circuit, Type Am25LS2521PC	U86
0020-0076	Integrated Circuit, Type Am25LS2569PC	U66, U67
0022-0020	Integrated Circuit, Type Am26S02PC	U43, U64
0028-0006	Integrated Circuit, Type Am8304N	U91, U92, U93
0023-0011	Integrated Circuit, Type Am9050EPC	
0028-0003	Integrated Circuit, Type NE555V	U63
0020-0045	Integrated Circuit, Type SN74LS00N	U22
0020-0033	Integrated Circuit, Type SN74LS02N	U46
0020-0032	Integrated Circuit, Type SN74LS04N	U65
0020-0001	Integrated Circuit, Type SN74LS08N	U2
0020-0002	Integrated Circuit, Type SN74LS10N	U23
0020-0003	Integrated Circuit, Type SN74LS32N	U44, U21
0020-0004	Integrated Circuit, Type SN74LS74N	U85, U42, U45
0020-0016	Integrated Circuit, Type SN74LS240N	U87, U88, U89, U90
0020-0018	Integrated Circuit, Type SN74LS244N	U95, U98
0020-0075	Integrated Circuit, Type SN74LS373N	U94, U97
0043-0010	Jumper Pin	
0063-0036	Resistor, 22Ω, DIP, 14 Pins	RN2, RN3
0063-0049	Resistor, 22Ω, DIP, 16 Pins	RN1
0063-0041	Resistor, 270Ω, 5%	R14
0063-0033	Resistor, 2.2KΩ, 5%	R11, R9, R5, R4, R1, R13
0063-0038	Resistor, 2.2KΩ, SIP, 8 Pins	RN4
0063-0035	Resistor, 2.2KΩ, DIP, 16 Pins	RN5
0063-0042	Resistor, 5.6KΩ, 5%	R3
0063-0007	Resistor, 10KΩ, 5%	R6, R12, R2, R7
0063-0037	Resistor, 10KΩ, SIP, 8 Pins	RN6
0063-0034	Resistor, 15KΩ, 5% AB	R8
0063-0051	Resistor, 39KΩ, 5%	R10
0045-0018	Solder IC Socket, 18 Pin	
0031-0001	Zener Diode, 5.1V	CR1

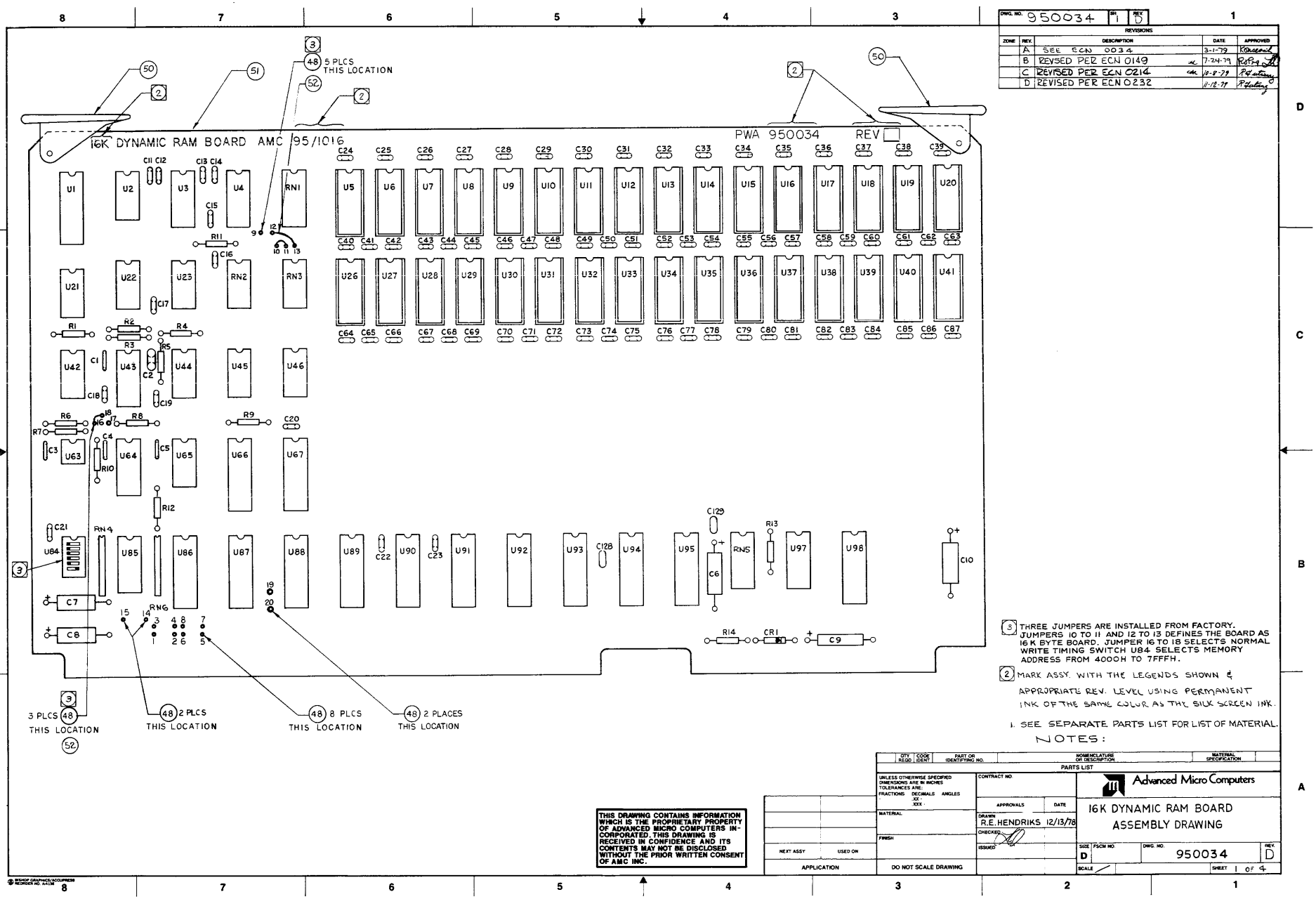


Figure 4-1. AMC 95/1016 Assembly Drawing.

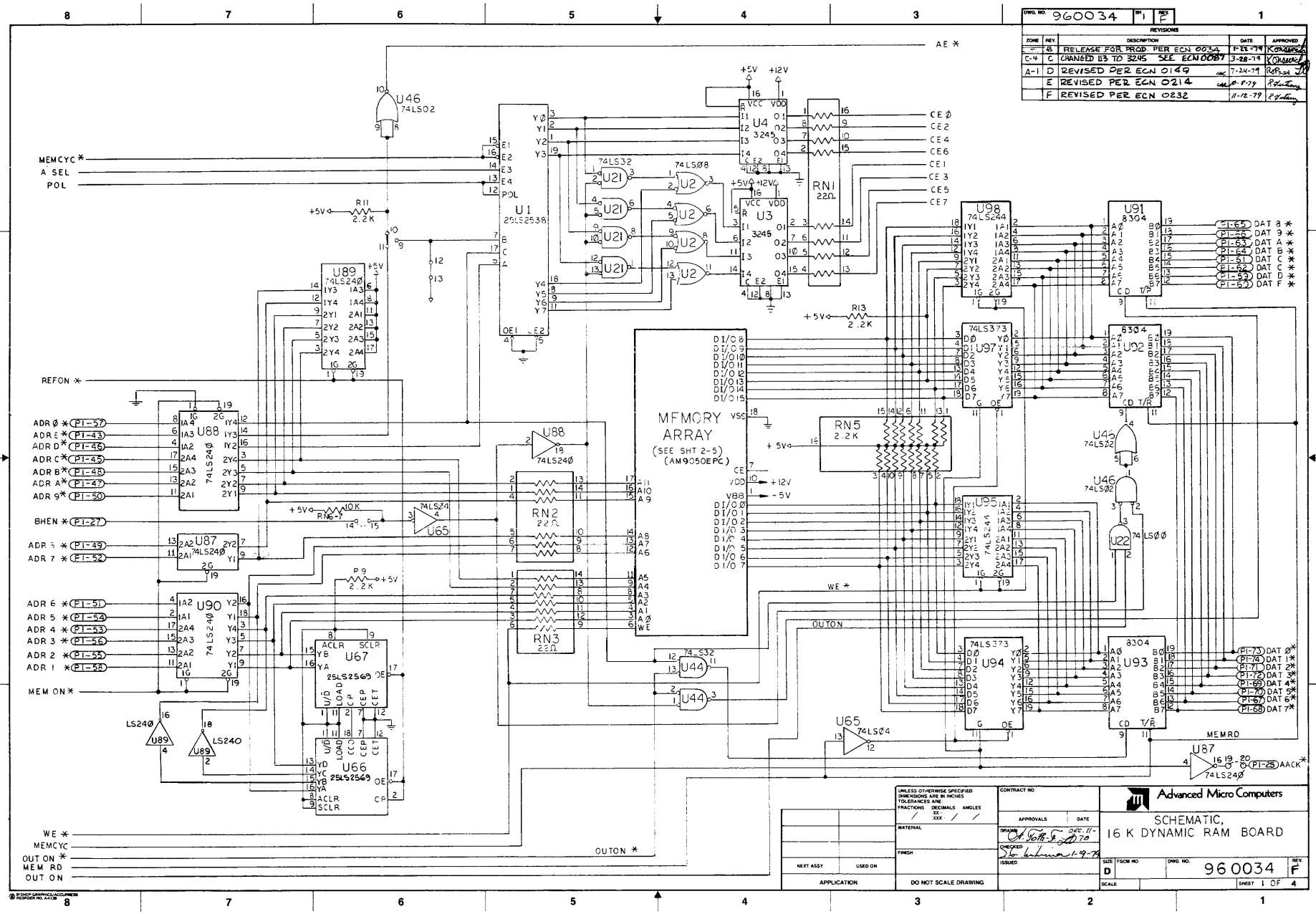


Figure 4-2. 16K Dynamic RAM Board Schematic Sheet 1.

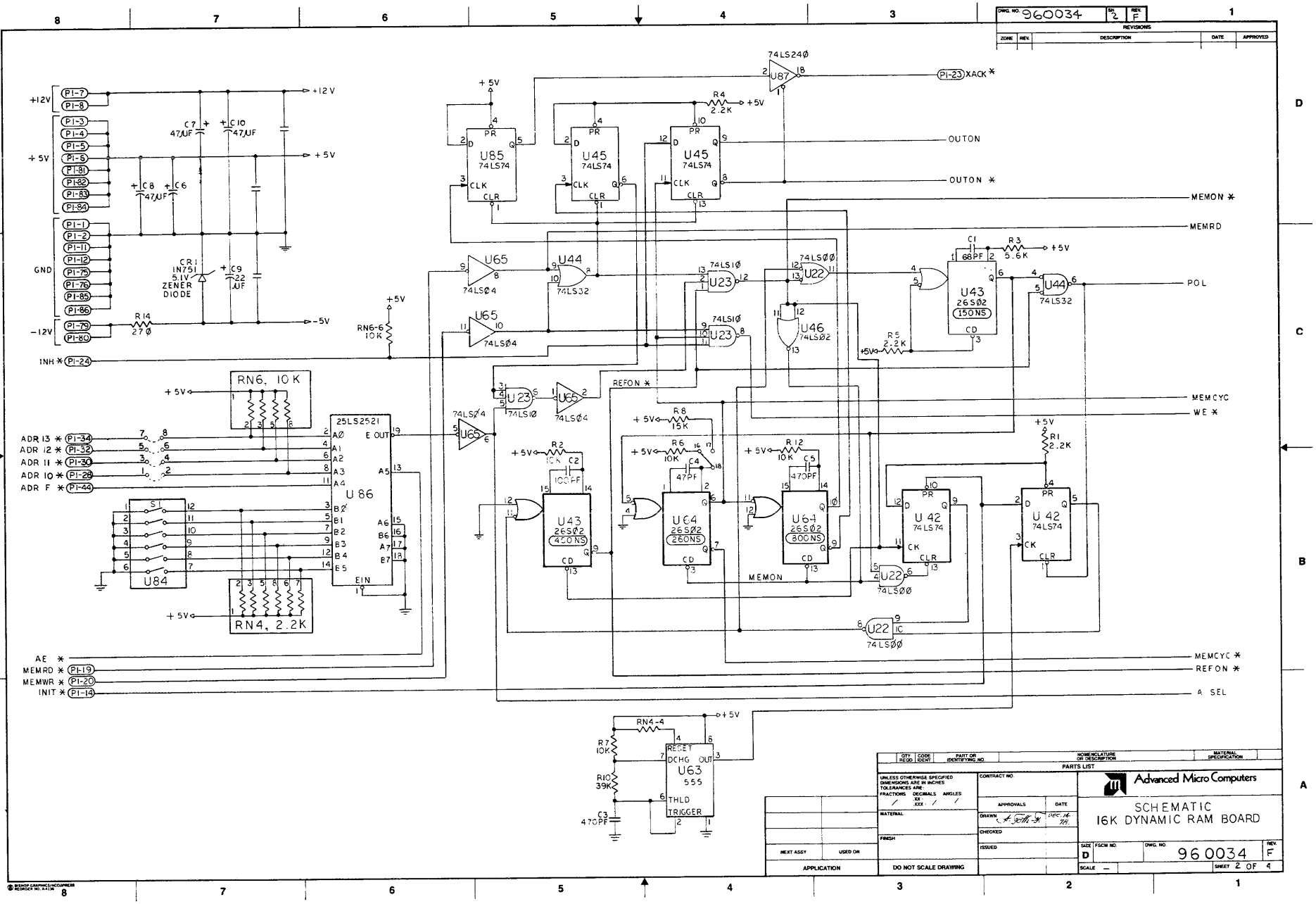


Figure 4-3. 16K Dynamic RAM Board Schematic Sheet 2.

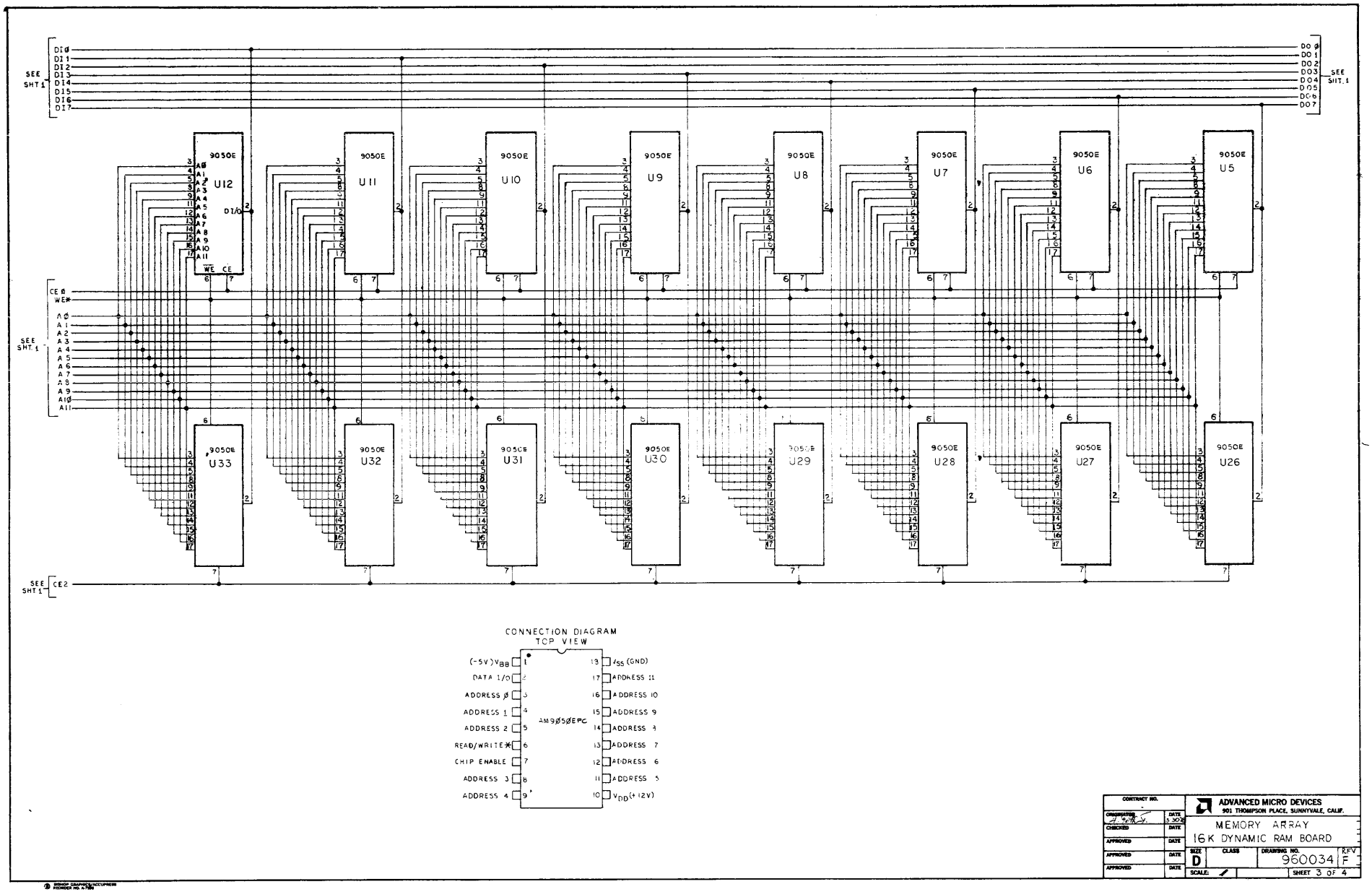


Figure 4-4. 16K Dynamic RAM Board Schematic Sheet 3.

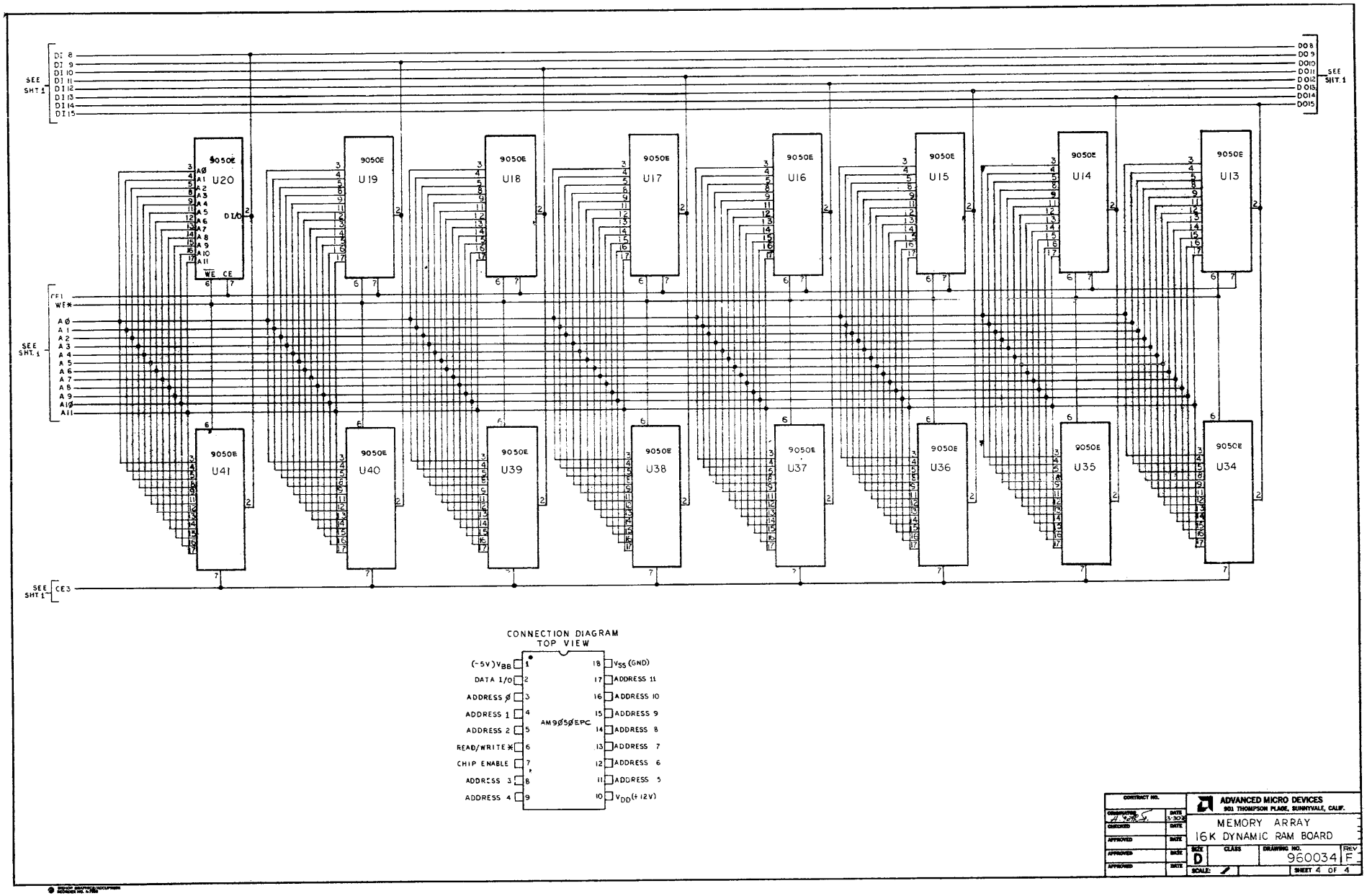


Figure 4-5. 16K Dynamic RAM Board Schematic Sheet 4.

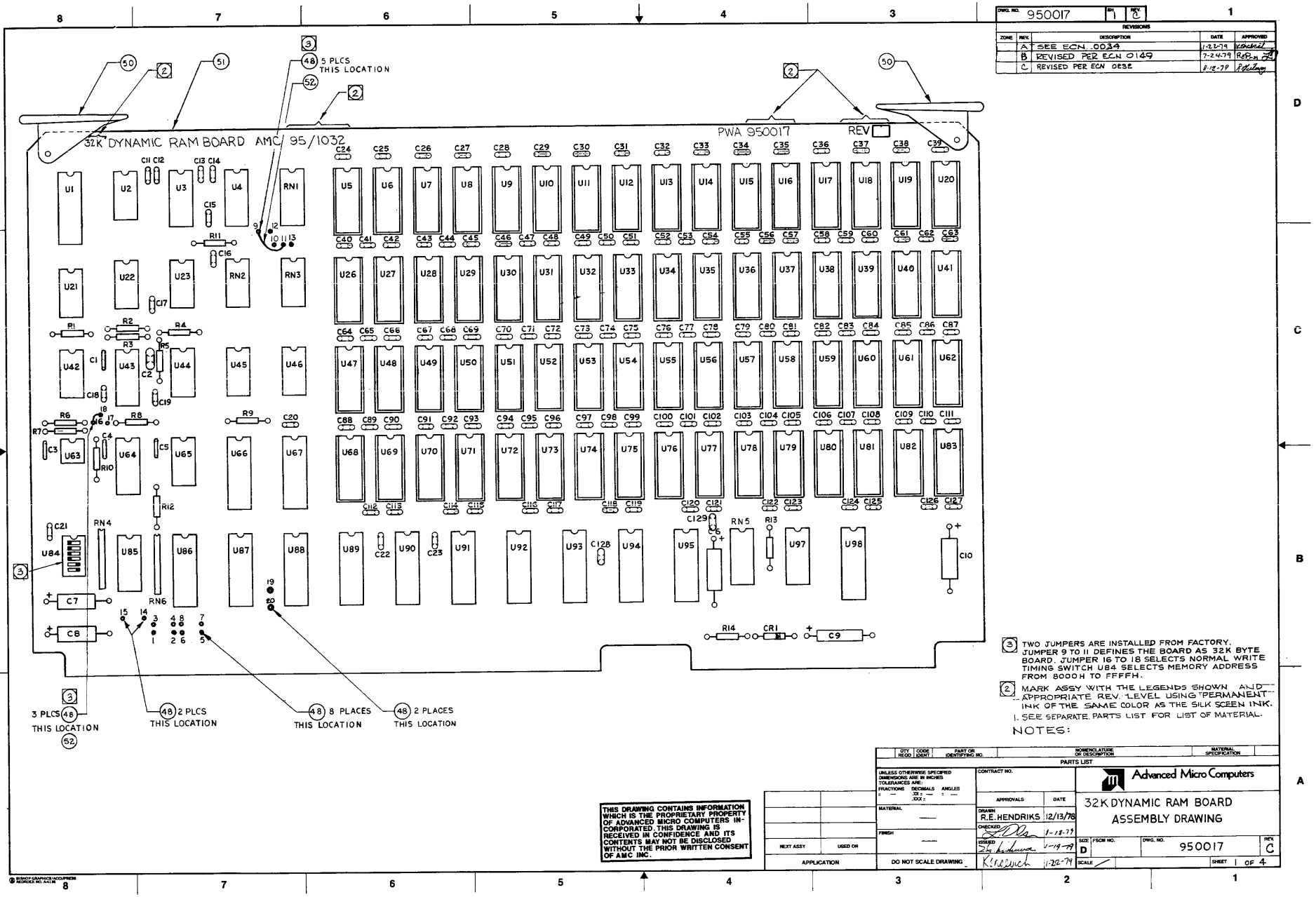


Figure 4-6. AMC 95/1032 Assembly Drawing.

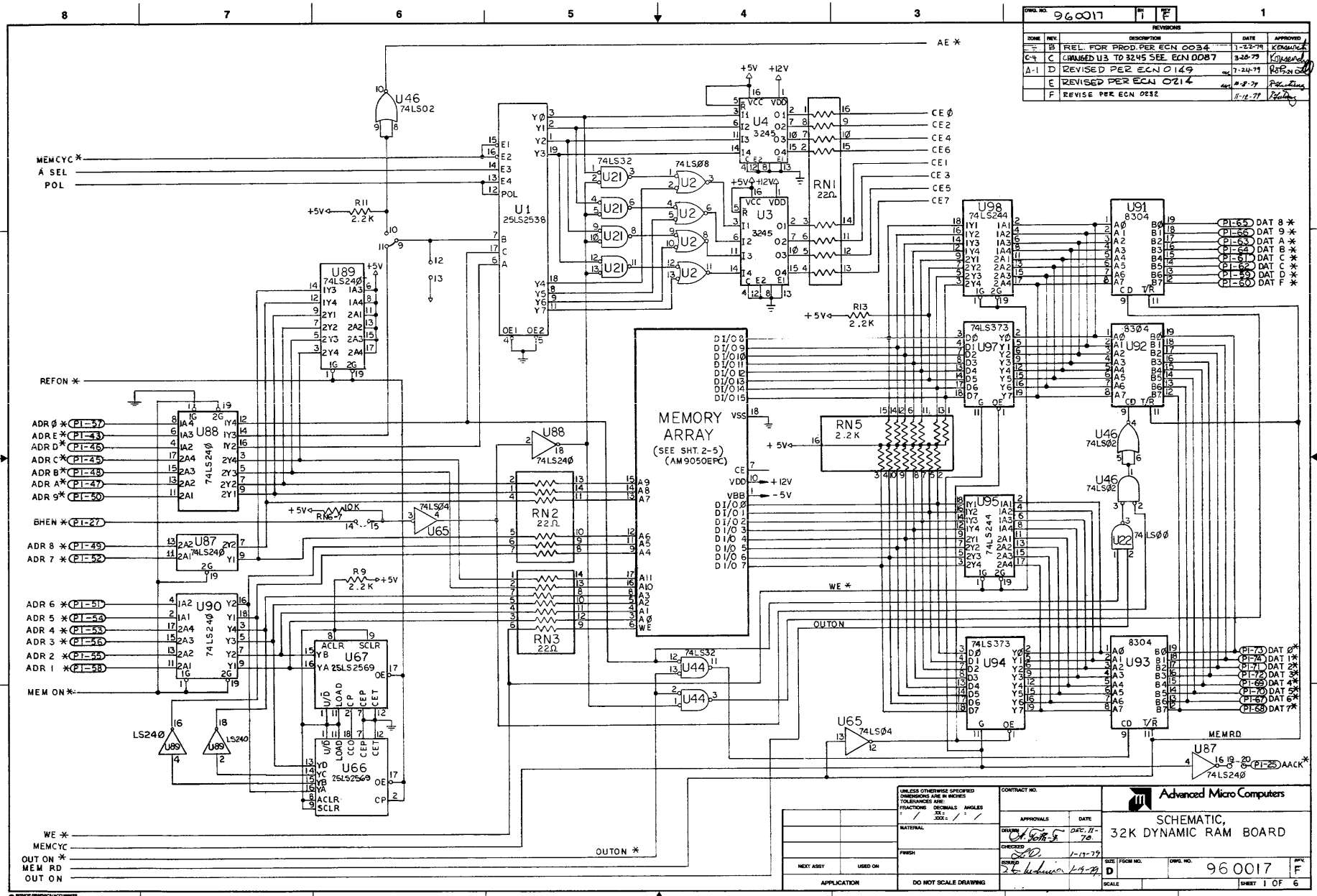


Figure 4-7. 32K Dynamic RAM Board Schematic Sheet 1.

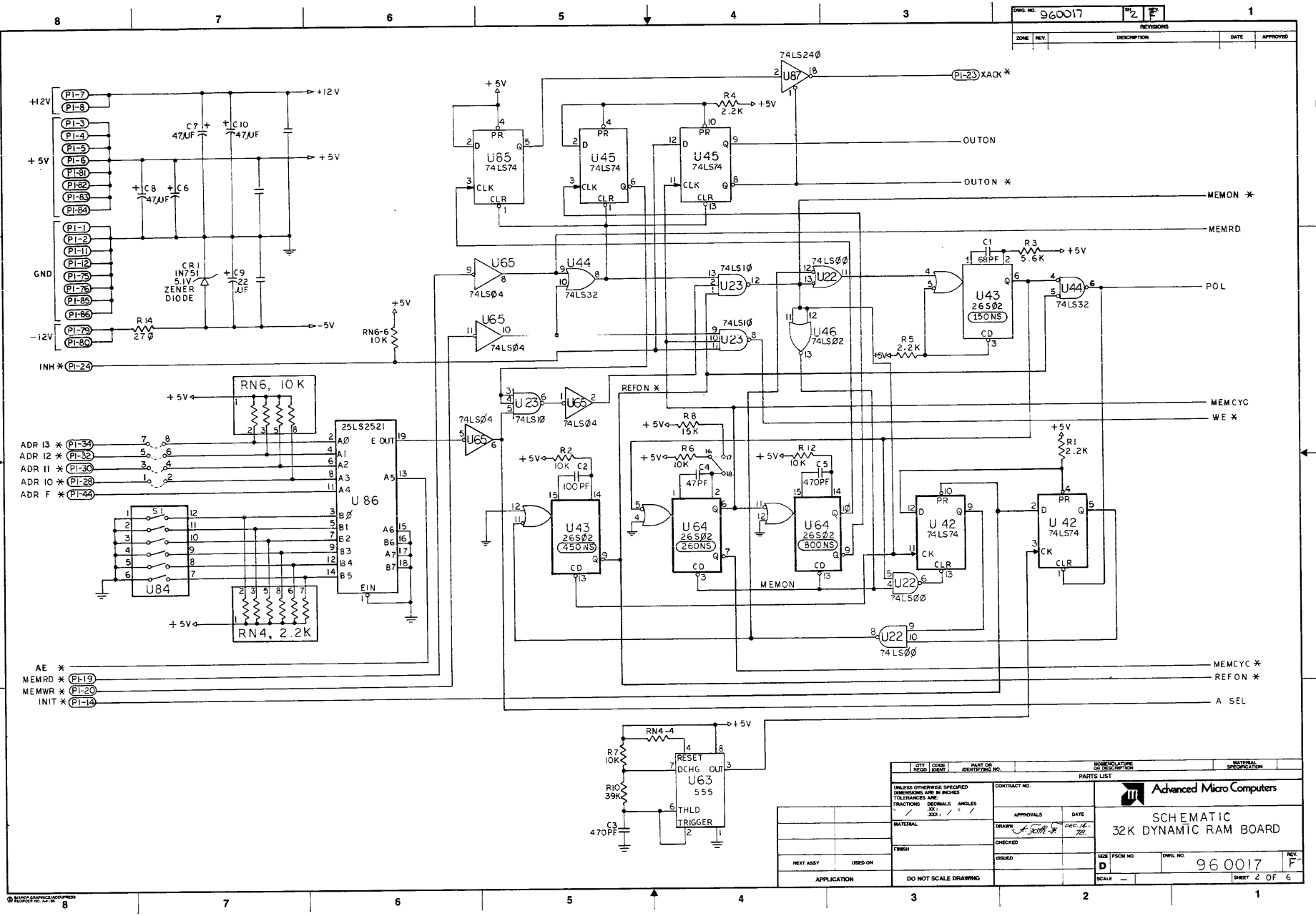


Figure 4-8. 32K Dynamic RAM Board Schematic Sheet 2.

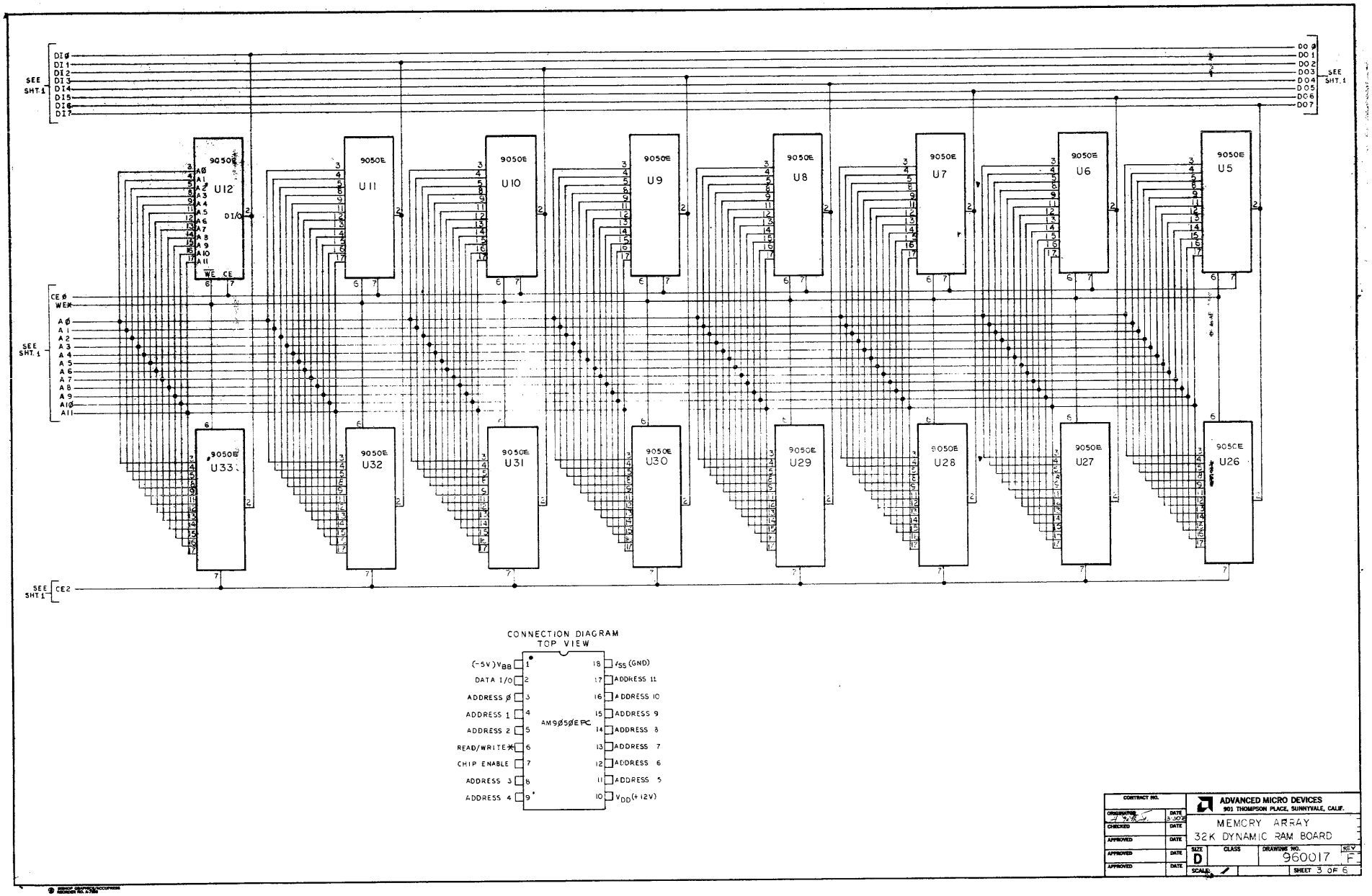


Figure 4-9. 32K Dynamic RAM Board Schematic Sheet 3.

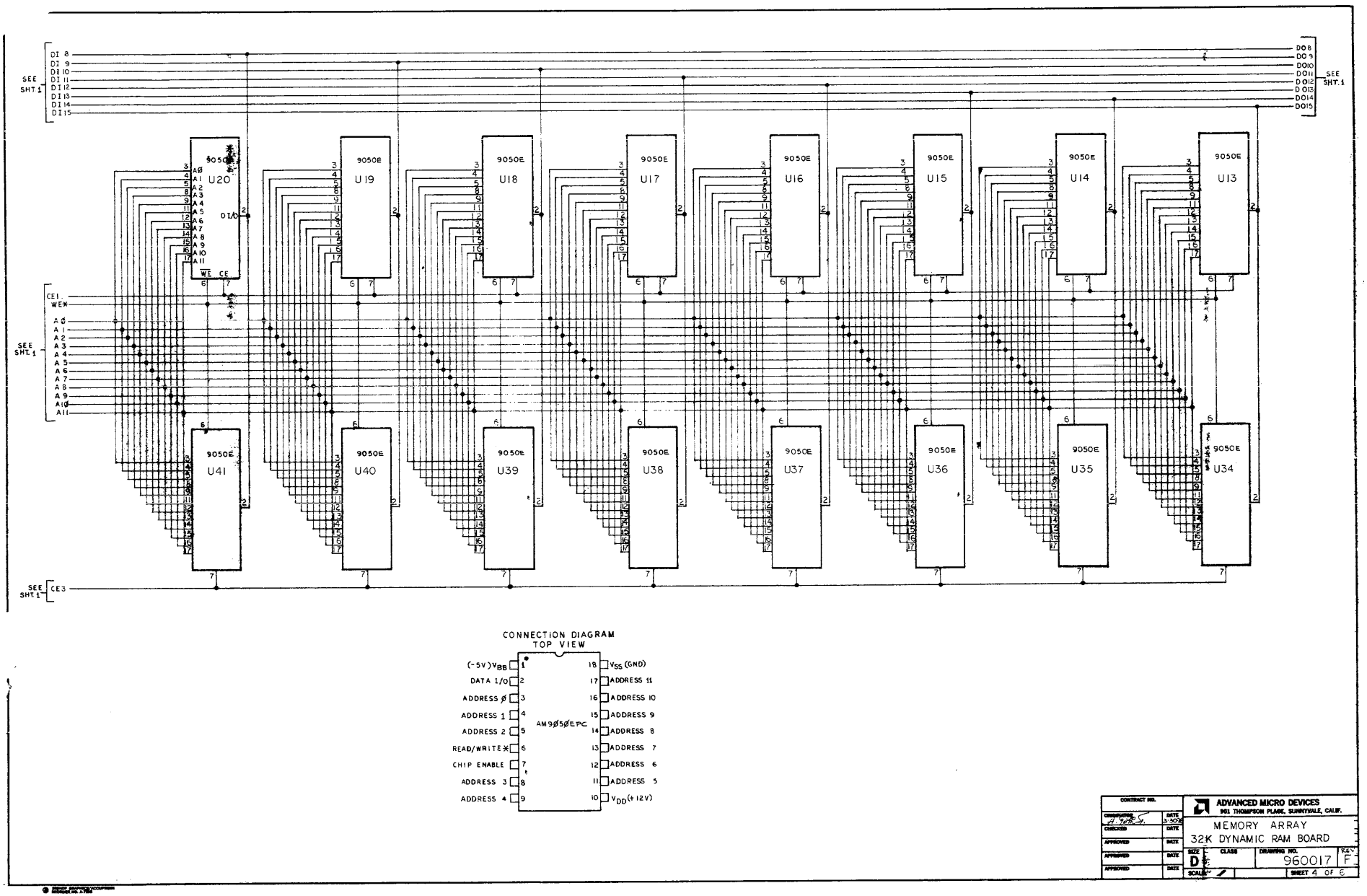


Figure 4-10. 32K Dynamic RAM Board Schematic Sheet 4.

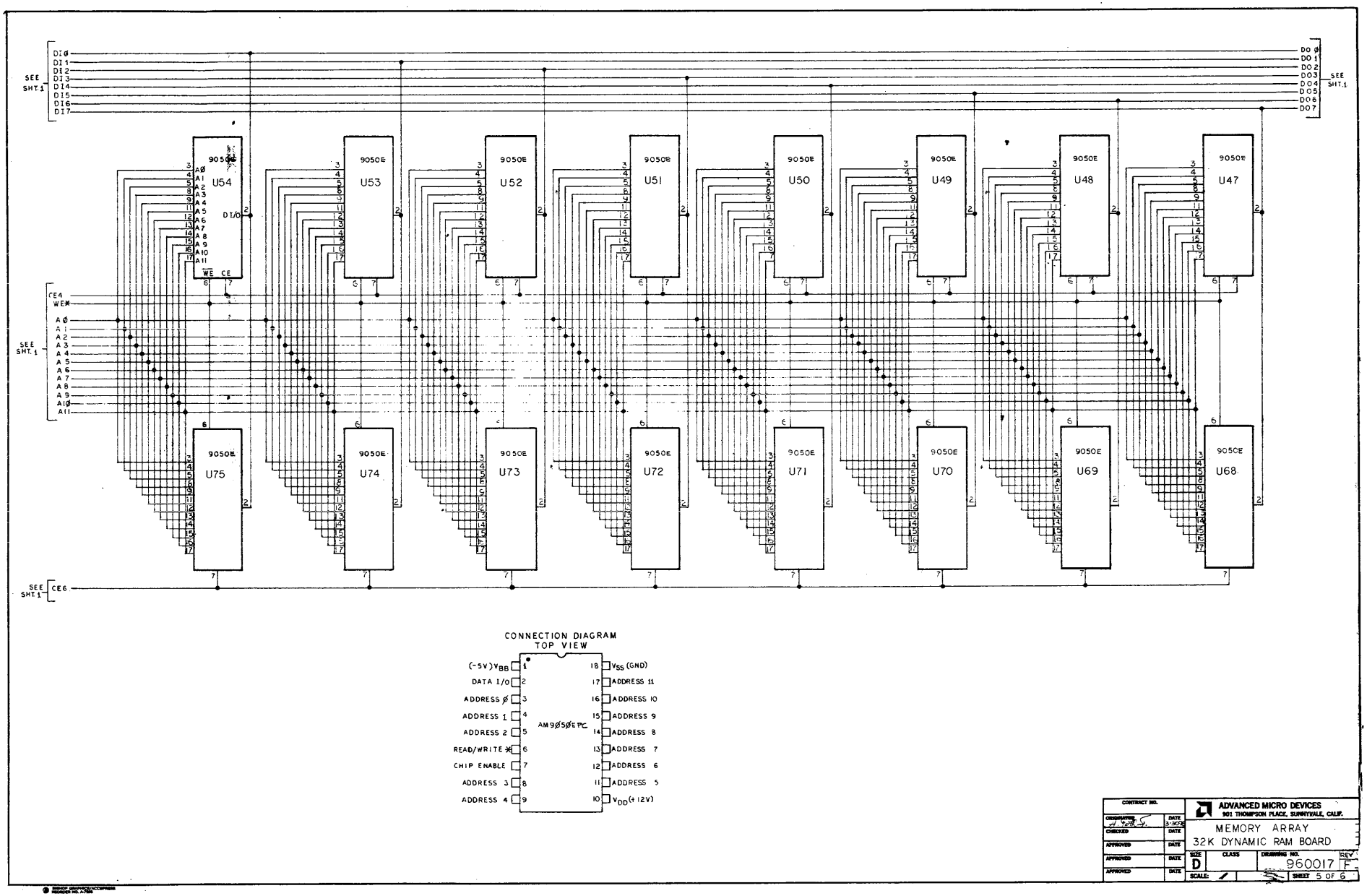


Figure 4-11. 32K Dynamic RAM Board Schematic Sheet 5.

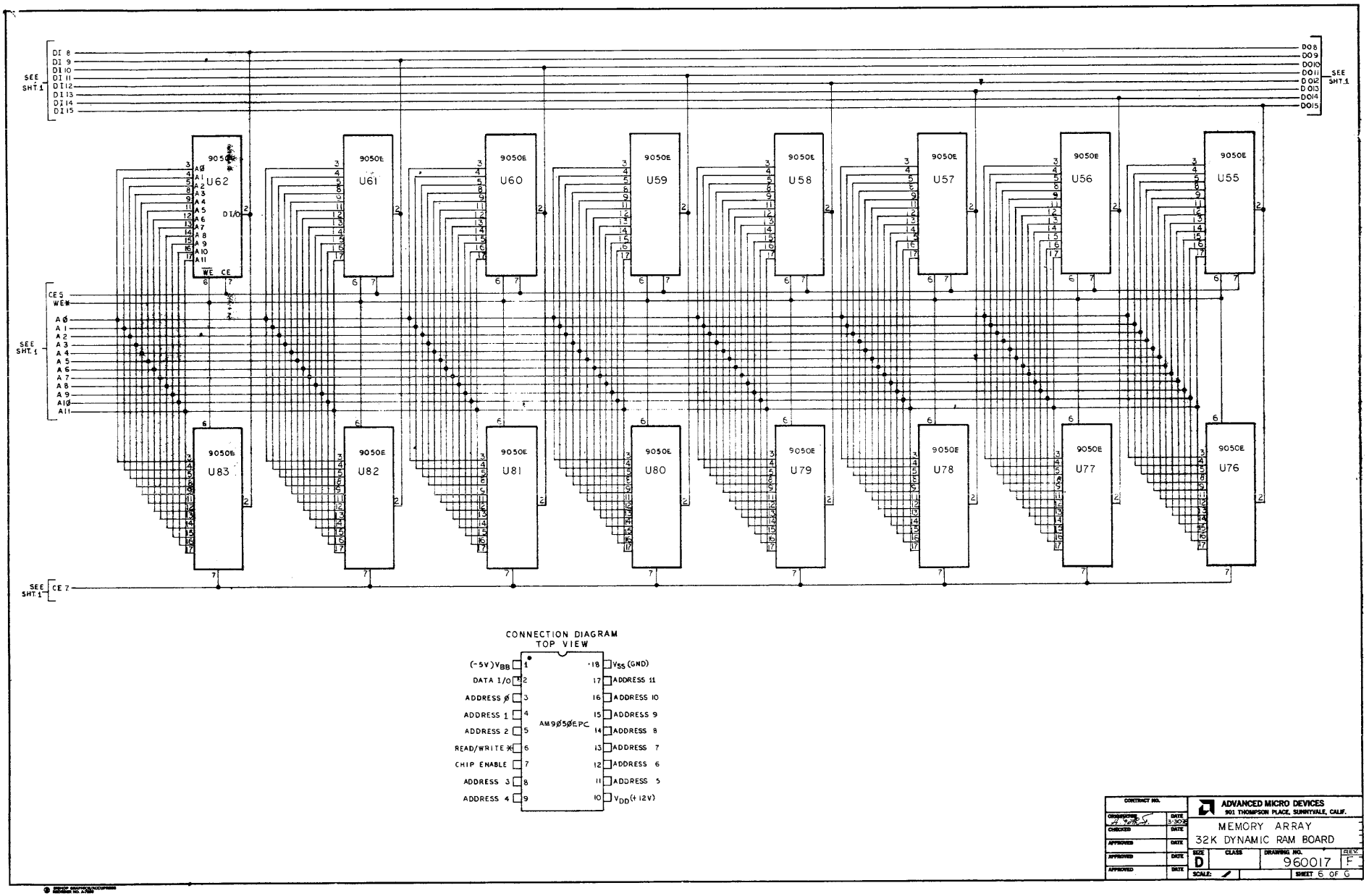


Figure 4-12. 32K Dynamic RAM Board Schematic Sheet 6.

COMMENT SHEET

TITLE: RANDOM-ACCESS MEMORY BOARD
PUBLICATION NO: 00680109C

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