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ABSTRACT

This memorandum documents the first production version of 3B* 2 Common I/O (CIO) hardware (Issue 1) - the core circuit of all 3B 2 intelligent peripherals to date. This document intends to aid test/manufacturing engineers and peripheral designers in the understanding and use of the CIO circuit. To this end, complete descriptions of the circuit's subcomponents and operation are given. In addition, the electrical issues are discussed and interfaces defined.

Issue 1 of CIO hardware is based on the requirements set forth in "3B 2 Requirements - I/O Board Hardware and Firmware Architecture and Design" (November 4, 1983).

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subject: 3B™ 2 Circuit Description: Common I/O Hardware Issue 1 (LDI LA - LD)

date: December 28, 1983

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Internal Memorandum (IM)

1. INTRODUCTION

Many 3B 2 intelligent peripherals will be based on a common realization of hardware, referred to as Common I/O (CIO). The usefulness of a common design stems from the fact that the I/O Bus interface is well defined. Although the I/O Bus interface of CIO is firm, the application interface is flexible. As shown later, CIO hardware is not in itself a general-purpose, stand-alone physical entity - rather, it needs application hardware to be operational. As such, it exists as a circuit schematic, as opposed to a Circuit Design File. This document describes Issue 1 of CIO hardware, LDI LA (with deltas LB and LD).

Section 2 of this document presents an overview of CIO hardware. Section 3 outlines the basic subcomponents of CIO where the basic operations of CIO are discussed in section 4. Hardware / software and electrical requirements are presented in Sections 5 and 6, respectively.

Closely related documents include "3B2 Requirements - I/O Board Hardware and Firmware Architecture and Design,"[1] "3B2 System Architecture and Requirements,"[2] and "3B 2 Component Requirements and Specifications: I/O Bus"[3]. More details of circuitry on the System Board side of the I/O bus will be found in "3B2 Component Requirements - System Board"[4].

2. CIO HARDWARE OVERVIEW

A primary objective of 3B 2 system architecture was to achieve a competitive cost/performance ratio. To this end, the 3B 2 supports intelligent microprocessor-based peripherals. These microprocessors can of course be programmed to access 3B 2's main memory via the I/O Bus. Likewise, it can be expected that the WE™-32000 (on the System Board) would at times wish to use the I/O Bus to access RAM, say, of a given peripheral. (Such an access is called a "passive" access.) If, however, these two operations were to occur simultaneously, a deadlock would ensue.

Conceivably, additional hardware (cost and space) could be used to detect such a situation and in turn temporarily back off the peripheral's microprocessor (or

WE-32000 for that matter) and allow the WE-32000's access complete. Alternatively, as in the case with CIO, the peripheral could provide a restricted interface to the WE-32000. In particular, the WE-32000 can only access a few registers of a CIO-based peripheral, with messages and the like being passed back and forth through queues in main memory. The few registers of a peripheral which the WE-32000 can access are used primarily to generate interrupts or cause a reset of a given peripheral.

CIO-based peripherals consist of two major functional sections: CIO hardware and application hardware.[1] Although CIO is designed to be the core circuit of any intelligent 3B 2 peripheral, the application circuit defines the peripheral's ultimate use. Four major factors influenced the design of CIO: functionality, size, cost and performance. CIO hardware, for example, primarily consists of an Intel 80186 microprocessor along with I/O Bus control and miscellaneous support logic. The 80186 is a 16-bit microprocessor with many support features (e.g. programmable interrupt controller) integrated into 1 compact VLSI package. Finally, in the interest of system performance, CIO hardware minimizes bus occupancy through the use of latched reads.

Before proceeding, the existence of two forms of CIO hardware should be noted: *basic* and *enhanced*. Basic CIO hardware, as described in this document, supports all the features discussed in [1] whereas enhanced CIO supports I/O Bus memory interlock and multiple access cycles. (CIO firmware assumes only basic CIO and therefore can run on either form.)

3. SUBCOMPONENTS

The CIO is an 80186 based intelligent peripheral to which an application circuit may be attached. The subcomponents of the CIO, as presented in the block diagram on page 2 of the attached circuit schematic, are:

1. CPU (Intel 80186)
2. I/O Bus control logic and buffers/latches
3. ID/Vector Register
4. Page Register
5. Peripheral Control and Status Register (PCSR)
6. Local RAM *support*

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1. The 3B 2 Ports and Network Interface boards are two examples of CIO-based peripherals.

7. Local ROM *support*

8. Miscellaneous support logic

These are discussed in detail below.

3.1 CPU (Intel 80186)

The Intel 80186 is a 16-bit microprocessor with many support features integrated into 1 compact (approximately 1 square inch) VLSI package. These features include,

- *Enhanced 8086-2 CPU*

  The 80186, like the 8086, uses a segmented addressing scheme (as opposed to linear) and is object code compatible with all existing iAPX 86, 88 software (10 new instruction types). It has 8 categories of addressing modes, 8 data types and 14 internal registers including: 8 16-bit general purpose registers, 4 16-bit segment registers (text, data, stack and global data) and 2 16-bit special registers (instruction pointer, status word).

- *2 independent DMA channels, 0 and 1*

  DMA channel 0 is used by CIO firmware to move data from the peripheral's on-board RAM to 3B 2 main memory, or vice-versa. DMA channel 1 is left to the application. (It could be programmed, for example, to transfer data between on-board RAM and a disk controller.)

  Data can be transferred in bytes or 16-bit words, to or from even or odd addresses. Each DMA channel maintains both a 20-bit source and destination pointer which can be optionally incremented or decremented after each data transfer (by one or two, depending on byte or word transfers). Each data transfer consumes a minimum of two bus cycles (eight clocks): one cycle to fetch data and another to deposit the data, thereby providing a maximum data transfer rate of 2 MBytes per second. DMA channel 1 may be programmed in source or destination synchronized or unsynchronized mode; channel 0 must be programmed in a synchronized mode. The two channels may be programmed in fixed or rotating priority in relation to each other.

- *Programmable interrupt controller*

  The 80186 can receive interrupts from a number of sources both internal and external. The internal interrupt controller serves to merge these requests on a priority basis for individual service by the CPU. Internal interrupt sources may be disabled by their own control registers or by mask bits within the interrupt controller. The 80186 interrupt controller has its own control registers that set the mode of operation for the controller.

  In addition to the 80186 internal interrupt sources (Timers and DMA) five external interrupts are accepted: INT0-3 and a Non-Maskable Interrupt

(NMI). Vectors will be provided internally and automatically by the 80186 interrupt controller. Of these 5 interrupts, INT0 and INT1 are reserved exclusively for CIO firmware, NMI can be shared between CIO and application firmware and INT2 and INT3 are completely application defined. Priority levels are firmware programmable.

- *3 programmable 16-bit timers*

  The 80186 provides three internal 16-bit programmable timers. Two of these are highly flexible and are connected to four external pins (2 per timer). They can be used to count external events, time external events, generate non-repetitive waveforms, etc. The third timer is not connected to any external pins and is useful for real-time coding and time delay applications. In addition, this timer may be used as a prescaler to the other two, or as a DMA request source. Each timer may interrupt the 80186.

  The timer 0 output will be buffered by CIO circuitry to generate the I/O bus "PFAIL0" signal. This can be used as a sanity timer when implemented by firmware. Timer 1 is used within the Bus Abort Feature (BAF) of CIO and timer 2 is application defined.

- *Programmable memory and peripheral chip selects and wait-state generator*

  The 80186 provides a flexible, firmware programmable address decoder. It provides chip selects for upper, middle, and lower memory, as well as seven peripheral chip selects which may be mapped into memory (20-bit address) or I/O (16-bit address) space. In addition, each chip select may be programmed for 0, 1, 2, or 3 wait states with or without external data ready control. Section 5 contains tables describing the state of the address decoding circuitry as programmed for the 3B 2 CIO environment.

- *Clock generator (8 MHz basic cycle rate)*

  The 80186 provides an external connection (X1 and X2) for a fundamental mode parallel resonant crystal for its internal crystal oscillator. Alternatively, X1 can interface to an external clock where this clock or oscillator frequency is internally divided by two to generate the 50% duty cycle clock (CLKOUT). CIO realizations will use a 16MHz oscillator, thereby providing 16MHz and 8MHz clocks to the application. All 80186 timings are referenced to this output clock signal.

- *Coprocessor support, compatible with 8282/83/86/87/88/89 bus support components*

Consult the data sheet[5] for more information.

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2. CIO firmware programs the internal interrupt controller to operate in Fully Nested Mode.

3.2 I/O Bus control

Whereas the 80186 provides overall CIO control, a distinct "controller" provides CIO's interface to the I/O Bus. This controller, a Signetics 82S105 Field Programmable Logic Sequencer (FPLS)[6], realizes a state machine which has 1 entry point (on reset) and 3 major paths:

1. 80186 read or write of main memory,

2. System Board CPU read or write of peripheral and

3. Interrupt acknowledge.

The I/O Bus controller responds to I/O Bus and 80186 control signals, selectively enabling I/O Bus signals. In addition, it can prematurely force a ready to the 80186 (Bus Abort Feature) as well as set certain Peripheral Control and Status Register (PCSR) bits. The I/O Bus interface of the CIO conforms to the I/O Bus Requirements specified in [3].

3.3 ID/Vector Register

The ID/Vector Register is a 16-bit register which initially contains a given peripheral's 16-bit Identification (ID) code and later its 8-bit interrupt vector. The ID/Vector Register can be written only by the 80186 and read only by the System Board CPU. Upon a reset (e.g. on power up), 80186 firmware writes its ID (as a 16-bit word) to the ID/Vector Register and waits. During system self-configuration, the System Board CPU will poll each I/O slot, reading byte 1 and then byte 0 of a peripheral's ID/Vector Register. The 2 bytes form a 16-bit ID code uniquely identifying the peripheral.

The action of reading byte 1 of the CIO's ID/Vector Register, sets PCSR[0] which in turn generates interrupt INT0 to the 80186. Similarly, reading byte 0 also sets PCSR[0] and generates another INT0. Some time later, the System Board CPU will access the peripheral's Control Register which will set PCSR[1] and generate interrupt INT1 to the 80186. On this interrupt (known as the "attention" interrupt) the 80186 "knows" to go out over the I/O Bus and fetch its interrupt vector (among other things) from DPDRAM. Once in hand, the 80186 will write this unique 8-bit vector to byte 1 of its ID/Vector Register, thereby overwriting half of its ID. (This implies that System Board software will have only one chance to read the peripheral's ID without resetting the board.) CIO circuitry will ensure that the contents of this register are gated out on to the I/O Bus at interrupt acknowledge time. The position of the ID/Vector Register in the respective address spectrums of the System Board and 80186 is defined in Section 5.

Each peripheral type has a unique ID, where IDs will be initially assigned by BTL and later by AT&T Western Electric. Refer to [1] for the guidelines of assigning ID codes.

3.4 Page Register

The Mid-Range Memory Chip Selects of the 80186 are gated together and programmed (by CIO firmware) to provide a 128k byte address range (17-bit address) which is mapped to 3B 2's main memory (DPDRAM). A 7-bit Page Register is used to extend this 17-bit address to a 24-bit I/O Bus address. Bits 6-0 of the 7-bit page register map to I/O Bus address lines PPA[23-17]1 while CIO (80186) physical address lines CPA[16-01]1 map to PPA[16-01]1. The Page Register is write only by the 80186 where data bits 6 and 5 must be zero,[3] effectively yielding 32 pages with 128k bytes per page. (Bit 7 is ignored.) It is the responsibility of CIO firmware to initialize the Page Register on a reset and to guarantee DMA transfers do not bridge page boundaries. The Page Register resides at the address noted in Section 5.

3.5 Peripheral Control and Status Register (PCSR)

CIO hardware contains an 8-bit PCSR on 80186 byte 0 (bits 0-7) which is byte readable by the 80186. The PCSR is addressable at the locations noted in Section 5.

PCSR[0] Clear INT0
PCSR[0] (INT0 - the SYSGEN and express queue interrupt[4]) is set on a System Board CPU access of a peripheral's ID/Vector Register (except on an interrupt acknowledge cycle). The service routine for this interrupt must clear PCSR[0] by referencing the PCSR[0] location indicated in Section 5. (Since the 80186 does not latch INT0-3 internally, these signals are latched in the PCSR.) PCSR[0] is undefined after a reset (e.g. power-up) and must be cleared by CIO firmware.

PCSR[1] Clear INT1
PCSR[1] (INT1 - the attention interrupt) is set when the System Board CPU accesses the Control Register of a peripheral. This bit must likewise be cleared within the appropriate service routine. PCSR[1] is undefined after a reset (e.g. power-up) and must be cleared by CIO firmware.

PCSR[2] Clear INT2
An application dictates how PCSR[2] (INT2) is activated; this bit must be cleared within the INT2 service routine. PCSR[2] is undefined after a reset (e.g. power-up) and must be cleared by CIO firmware.

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3. Although the current DPDRAM controller ignores the two most significant address bits, PPA[23-22]1, a peripheral must force these to zero.

4. Express queues are discussed in detail in [1].

PCSR[3] Clear INT3
An application dictates how PCSR[3] (INT3) is activated; this bit must be cleared within the INT3 service routine. PCSR[3] is undefined after a reset (e.g. power-up) and must be cleared by CIO firmware.

PCSR[4] Reserved
CIO development reserves the right to utilize PCSR[4] at any time to improve design and to supply the best product possible and consequently it is not available to the application.

PCSR[5] spare
Application defined.

PCSR[6] I/O Bus locked
PCSR[6], referred to as the BAF (Bus Abort Feature) bit, is set by hardware on an on-board bus abort (due to a heavily loaded I/O Bus preventing access by the 80186) and cleared by firmware. PCSR[6] is undefined on a reset and must be cleared by CIO firmware. During "normal" operation, PCSR[6] can be cleared by firmware only if a "dummy" read is not pending. (Refer to the "Bus Abort Feature" of the **BASIC OPERATIONS** section.) Finally, the 80186 will not be able to access DPDRAM while this bit is set.

Applications which elect to not include the BAF from their design, can redefine PCSR[6]. Note, however, CIO firmware will clear PCSR[6] on a reset, regardless.

PCSR[7] Request interrupt of System Board CPU
PCSR[7], which maps to I/O Bus signal Peripheral Interrupt request (PINTx0), is cleared (activated) by firmware and set to one by hardware when the interrupt has been acknowledged. Note: PCSR[7] equal to zero indicates the peripheral's interrupt request of the System Board CPU is pending. PCSR[7] is automatically set to 1 on a reset.

3.6 Local RAM

The CIO does not specify how much or what kind of memory is to be on a peripheral, rather, this is defined by each application. On-board RAM will be accessed via the 80186's Lower Memory Chip Select (LCS). CIO firmware will initialize the 80186 internal address decoder / wait-state generator to a known state (refer to [1]) which application firmware will optionally reprogram as required. 256 KBytes of RAM address space is reserved.

3.7 Local ROM

CIO will provide two 28-pin sockets for EPROM or ROM.[5] These may be equipped

with 8K x 8 (2764) devices or 16K x 8 (27128) devices for a total (EP)ROM space of 16k or 32k bytes respectively. These sockets will be equipped with a "read-write" signal to allow ROM emulators to be used during initial development. (See page 13 of Attachment 1: CIO Hardware circuit schematic - Issue 1.) No straps are allowed to configure memory size. Note that (EP)ROM must always end at address 0xFFFFF.

On-board ROM will be accessed via the 80186's Upper Memory Chip Select (UCS). CIO firmware will initialize the 80186 internal address decoder / wait-state generator to a known state (refer to [1]) which application firmware will optionally reprogram as required. 64 KBytes of ROM address space is reserved.

3.8 Miscellaneous

CIO hardware includes essential 80186 support logic, such as address latches to demultiplex its address/data lines. I/O Bus address and data latches[6] are also included along with tri-state and open-collector buffers. Daisy-chain logic is also provided for the I/O Bus interrupt acknowledge and bus acknowledge signals, adhering to the requirements specified in [3], namely -

- While bus master, a peripheral must not allow PBACKO0 propagate to the next device in the chain.
- A peripheral must not drive PBRQ0 if PBRQ0 is currently active. Once PBRQ0 is recognized as inactive, the peripheral must delay before asserting it.
- A peripheral may not glitch the daisy-chained output signals.
- A peripheral may not preempt another's bus mastership.
- The latency from PBACKI0 to PBACKO0 should be kept under 9 nanoseconds.

3.9 CIO Hardware on Reset

A CIO-based peripheral can be reset in 1 of 2 ways: The System Board can assert I/O Bus signal SYSRST0 (hard reset) or the System Board CPU can reference the peripheral's Status Register (soft reset). In either case, the 80186 will be reset, causing all of its internal control registers to be set to the state defined in [5]. The 80186 will then start executing CIO firmware at location 0xFFFF0. The CIO I/O Bus controller will likewise be reset and so should application circuitry (unless otherwise documented in the application's requirements and/or design document).

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5. An application may elect to alter this basic configuration of (EP)ROM.
6. An 80186-generated I/O Bus address is latched (not just buffered) in support of the Bus Abort Feature.

TABLE 1. CIO HARDWARE ON A RESET

Subcomponent	State on Reset
80186 I/O Bus Ctrler	Refer to data sheet[5] Idle - All outputs inactive and no "dummy" read pending
ID/Vector	Undefined
Page Register	Undefined
PCSR[0-6]	Undefined
PCSR[7]	1

CIO will not use the RQRST0 I/O Bus signal; the application, however, is free to use this signal to cause a complete 3B 2 system reset as described in [4].

4. BASIC OPERATIONS

This section discusses in detail the basic operations of CIO hardware.

1. 80186 Read or Write of DPDRAM
2. System Board CPU Read or Write of CIO-Based Peripheral
3. Interrupting the System Board CPU
4. Bus Abort Feature (BAF)
5. Fault Handling

The discussion uses the attached state diagrams as the central point of reference. Each state is represented as a circle enclosing a state name and corresponding bit assignment. The arrows connecting each state represent state transitions which are labeled with the notation: "inputs to current state / outputs of next state" (i.e. Mealy type of state machine).

Timing diagrams have also been attached which include most 80186 signals, certain CIO hardware signals and most I/O Bus signals. At the bottom of each timing diagram is an indication of the current state of the FPLS state machine. Finally, circuit schematic (Attachment 1) page numbers have been dispersed throughout the following discussion.

4.1 80186 Read or Write of DPDRAM

CIO hardware will support both DMA and programmed accesses of DPDRAM by the 80186. (The 80186 contains an internal DMA controller.) On a reset (e.g. power-up), CIO firmware will program the 80186 Mid-Range Memory Chip Selects (MCS0-3) to map to the range, 0x80000 - 0x9ffff (128k bytes per page). CIO firmware will also initialize the page register to select one of the 32 possible pages.

CIO firmware can alter the value of the page register at any time but must guarantee that DMA transfers do not bridge page boundaries. In addition, the 80186-internal DMA controller should operate in a "synchronized" mode; a "synchronized" mode prevents the DMA controller from locking up the 80186 CPU while the DMA job is active. Finally, to minimize the length of time the DMA controller waits to use the I/O Bus, CIO hardware will not "request" that the DMA controller start until the I/O Bus is unoccupied (I/O Bus signal PBUSY0 inactive - pg 3).

An 80186 read or write of DPDRAM begins with one of 4 80186 Mid-range Memory Chip Selects (MCS3-0) going active (LOW) and hence CMCS0 as well (pg. 3). CMCS0 is synchronized on the positive edge of CLKOUT1 (80186 8 MHz output clock) with a LS374 synchronization register[7] and input to pin 2 of the FPLS (pg 5).

The state machine realized by the FPLS also operates on the positive edge of CLKOUT1. In its inactive state, it waits in state *idle* with all outputs inactive HIGH. On detecting an active CMCS0 **and** inactive PBRQ0, it advances to state *rw1* and activates bus request CBRQ0. CBRQ0 is the output net name of the FPLS which is then routed to the bus acknowledge daisy-chain logic on pg 10. Such daisy-chain logic blocks PBACKI0 from propagating on to PBACKO0. This daisy-chain scheme, as discussed in [3], guarantees a peripheral will drive CBRQ0 LOW (blocking PBACKO0) before PBACKI0 can arrive.

The FPLS will wait in *rw1* until a bus acknowledge (PBACKI0 -> CBACK0) is received enabling it to transition to *rw2*. Other transitions from *rw1* can be back to *idle* in the case of either a System Board access of the peripheral (CSPAS0) or interrupt acknowledge (CIAK0) or to the state *rwtime0* in the case of timeout of 80186 timer 1 (TIMEOUT0). These other transitions can only occur while the FPLS is waiting for CBACK0.

If CBACK0 is detected, however, *rw2* is entered, causing FPLS output COEADD0 to be asserted. COEADD0 enables the I/O Bus address latches (pg 11), page register (pg 11) and control buffer (pg 12) and also activates CONBUS0 (pg 9).

The LS646 data transceiver latches (pg 12) are enabled with COEDAT0 which is generated from four sources (pg 6):

1. On an 80816 read, CRD0 and CONBUS0 will be active. (On a read, the 80186 will have tri-stated its address/data bus (AD[15-0]) before COEDAT0 can go active.)

---

7. All inputs (except PPA011) to the FPLS are synchronized on the rising edge of CLKOUT1 and used within the FPLS on the subsequent rising edge. (PPA001 is not synchronized because it is guaranteed to be stable whenever the FPLS *is looking at it*, which occurs only during a System Board access of the peripheral. Refer to the next section.)

2. On an 80186 write, CWR0 and COEADD0 will be active.

3. On a System Board CPU read, CSPAS0 will be active and PR1W0 will be HIGH.

4. On an interrupt acknowledge cycle, CIAK0 will be active and again PR1W0 will be HIGH.

CSR61 will normally be LOW (inactive) except during a BAF "dummy" read. CDSIX0 (a combination of I/O Bus data strobes PDS[1-0]0 - pg 5.) is used to qualify COEDAT0. (i.e. During a System Board read or interrupt acknowledge, data is gated onto the I/O Bus only when the data strobe(s) are active. Data is never gated onto the bus during a System Board write.)

Returning to our previous discussion, the FPLS will unconditionally transition from *rw2* to *rw3* and then to *rw4* and activate CSTRB0. CSTRB0 asserts I/O Bus control signals PDS[1-0], PBUSY0 and PPAS0 (pg 12). (80186 signals CBHE0 and CAD001 are translated to CDSO10 and CDSO00, respectively - pg 7 - which are then buffered to PDS[1-0]0 - pg 12.) A one cycle delay (additional 125 nanoseconds) is inserted between activation of COEADD0 and CSTRB0 to guarantee valid write data before assertion of data strobes. (Although the I/O Bus address, PPA[23-00]1, didn't require this additional cycle to be valid before assertion of PPAS0, it nevertheless got it. Refer to the TIME/TAP timing analysis report which was performed on CIO hardware[7].)

Rw5 is entered when the bus acknowledge (CBACK0) has been removed, causing bus request (CBRQ0 -> PBRQ0) to likewise be removed. (PBACK0 must be contained with PBRQ0[3]).

Rw6 is unconditionally entered where the FPLS will then wait for CARDYC1 to be HIGH. The System Board will eventually respond to the peripherals assertion of strobes by activating PDTACK0 or PFLT0. In either case, CARDYB1 (pg 8) and in turn CARDYC1 (which is synchronized version of CARDYB1) will go HIGH. *Rw7* will then be entered and CSTRB0 driven HIGH, thereby deasserting the I/O Bus strobes.[8]

Incidentally, CARDYB1 going active latches the read data off the I/O Bus into the LS646 data transceiver latches (pg 12). By latching the data, we can get off the bus without waiting for the 80186 to "accept" the data, thereby lowering bus occupancy.

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8. A delay is added between removing CBRQ0 (*rw5*) and potentially driving CSTRB0 inactive (*rw7*). Such a delay ensures that PBRQ0 will have been released at least 100 nanoseconds before strobes are driven inactive (an I/O Bus requirement). This delay, however, will most likely not hurt performance since it is doubtful the System Board can return PDTACK0 within 125 nanoseconds of data strobe assertion.

Once in *rw7*, the FPLS will either transition to idle (if CARDYC1 = 0) or stay in *rw7*. In either case, COEADD0 is driven HIGH one cycle after CSTRB0 was driven HIGH. Consequently, the I/O Bus strobes and address (and data if a write) will be tri-stated one cycle (plus gate delays and the like) after strobes are driven inactive. Also note that when the 80186 removes CMCS0, CONBUS0 will go inactive HIGH (pg 9) and in turn CARDYB1 and CARDYC1 will go inactive LOW (pg 8). As a result, *idle* will not be entered until CMCS0 has gone inactive, thereby eliminating a false transition from *idle* to *rw1* again.

There is one final comment regarding the case of a 80186 read of DPDRAM. The output enable (COEDAT0) of the data transceiver latches remains active until the 80186's RD0 line is removed, some time after we have gotten off the I/O Bus.

Issue 1, LDI LA - LD of CIO hardware does not support an I/O Bus multiple access cycle.

4.2 System Board CPU Read or Write of CIO-Based Peripheral

There are three locations which the System Board CPU can reference on a CIO-based peripheral: ID/Vector Register, Control Register and Status Register. Of these three, only the ID/Vector register actually resides on the I/O Data Bus and even this register can only be read; the other two are simply addressable locations. (For other peripheral types, particularly programmed ones, all three of these registers would be accessible from the I/O Data Bus.)

The ID/Vector Register initially contains a peripheral's ID code and later its interrupt vector. Referencing this register will generate INT0 to the 80186. By referencing the Control or Status Register, the System Board generates INT1 or causes a reset, respectively, of the peripheral.

Referring to the "SBD R/W of Periph" state diagram, the FPLS state machine transitions from *idle* to *sbd1a* or *sbd1b* on CSPAS0 (the OR of PCS0 and PPAS0 - pg 5); if PPA011 = 0 (offset = 0 or 1) *sbd1a* is entered, otherwise (offset = 2 or 3) *sbd1b* is entered. PCSR[0], which maps to the 80186's CINT01 pin, is set transitioning to *sbd1a* (pg 9) while PCSR[1] (CINT11) is set within *sbd1b*. The FPLS remains in *sbd1a/b* until the System Board asserts PDS10 and/or PDS00 (CDSIX0 - pg 5), at which time *sbd2* is entered and PDTACK0 asserted. The set input of the particular PCSR bit is also removed in *sbd2*.

Other than PDTACK0, the CIO-based peripheral need only drive PSIZE160 (which it does on PCS0 - pg 7) and data if the System Board CPU is reading the peripheral's ID/Vector register (pg 12); COEDAT0 is activated on CSPAS0 if PR1W0 is HIGH (pg 6). Also, note that the direction control on the ID/Vector Register is always HIGH (data transferred onto I/O Bus) except for 80186 reads of DPDRAM (where CDT1R0 and CONBUS0 are LOW).

Sbd3 is entered and PDTACK0 removed once CDSIX0 is seen to be removed. PDTACK0 is first released, however, asynchronously with CDSIX0 (pg 7) to meet the I/O Bus specification concerning PDTACK0 removal. Finally, the FPLS waits in *sbd3* until the System Board CPU removes PCS0 or PPAS0, indicating end of the cycle. (*Idle* can not be entered until CSPAS0 goes away; otherwise there would be a false transition from *idle* to *sbd1a/b*.)

As discussed previously, addressing the ID/Vector register (offset 0 or 1) generates INT0 while addressing the Control register generates INT1. Addressing the status register (offset 4 or 5 which is equivalent to PPA021 equal to a 1) should reset the peripheral. As shown on pg 3, when PCS0, PAS0 (CSPAS0) are active LOW and PPA021 is HIGH, CRESETI0 (reset input of 80186) is asserted as well as CFPLSPR1 (pg 5) - the preset input of the FPLS. A minimum of one-half cycle later, the 80186's reset output (CRESETO1) goes active, causing CFPLSPR1 to go inactive and hence, we have the desired effect of providing a momentary pulse on CFPLSPR1, presetting the FPLS to a known state (*reset1*).

Referring to the "Reset Sequence" state diagram, on a preset the FPLS is in *reset1* and unconditionally transitions to *reset2* and then *idle*. (*Sbd1a/b* is then entered if the preset was as a result of a System Board CPU write to the status register as opposed to a power-up reset - SYSRST0.) *Reset2* is used to activate the set input of PCSR[7] which maps to Peripheral Interrupt request (PINTx0) of the I/O Bus. Setting PCSR[7] to one causes PINTx0 to go inactive HIGH.

As a related note, on such a soft reset cycle, the state transitions from *reset1* (CRESETI0 active), to *reset2*, *idle*, *sbd1a*, and *sbd2* (where potentially CSPAS0 and if so CRESETI0 are inactive), takes 500 nanoseconds. Since CSPAS0 is active throughout, CRESETI0 of the 80186 is likewise active for at least 500 nanoseconds, as required by the 80186. (Also note that PCSR[0] will always be set on such a cycle, requiring firmware to clear this bit on reset.)

4.3 Interrupting the System Board CPU

An application (via a CIO firmware primitive/routine) may interrupt the WE-32000 on one of three allowable levels by clearing bit 7 in the PCSR. Sometime during SYStem GENeration (SYSGEN), CIO firmware will write the peripheral's unique interrupt vector to the ID/Vector register. Once set, firmware need never establish this vector again unless the peripheral has multiple vectors. (An I/O Ports board, for example, may have a different interrupt vector for each port.) The sequence CIO firmware will go through to interrupt the System Board CPU is as follows:

1. Check PCSR[7] to be equal to 1 (inactive).
2. If not, repeat check since a prior interrupt request is still pending.
3. Else, optionally write the particular interrupt vector to the ID/Vector Register before referencing[9] (read or write) the PCSR[7] location (I/O Bus PINTx0 signal is generated).
4. CIO hardware will automatically set PCSR[7] to 1 (remove PINTx0) when the System Board CPU acknowledges the interrupt.[10]

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9. Read and write data is arbitrary.

Note: In the interest of synchronization, firmware can not attempt to access the ID/Vector register while PCSR[7] is zero (PINTx0 active). PCSR[7] is set to one on a reset.

The "PIAK cycle" state diagram presents the FPLS actions during an interrupt acknowledge. As a result of PCSR[7] being cleared (PCSR70 active LOW), the I/O Bus signal PINTx0 will be eventually be asserted. The daisy-chain interrupt acknowledge circuit (pg 10) prevents assertion of PINTx0, and hence CGLIAK0, in the presence of an active PIAKOx0, thereby preventing activation of CIAK0 (i.e. the peripheral will not preempt a device further down the chain). Also, to prevent metastability the request (CSR70) and acknowledge (PIAKIx0) are synchronized on different clock edges (pg 17).

The System Board will eventually acknowledge the interrupt by asserting PIAKIx0 (PIAKIx0 -> CIAK0). As illustrated, *piak1* and then *piak2* are entered when CIAK0 is LOW. Similar to the case of a System Board CPU read of the peripheral, the FPLS waits for PDS10 (CDSIX0) to be active before asserting PDTACK0 in transitioning to *piak3*. *Piak4* is entered and PDTACK0 removed[11] when PDS10 goes away. *Piak5* is then entered (and PCSR[7] set to a logic 1) on PIAKIx0 being removed, guaranteeing PINTx0 is removed after PIAKIx0. *Idle* is then unconditionally entered and again all FPLS outputs are inactive. (Although not required, CIAK0 is double sampled via states *piak1* and *piak2*. This extra sampling can be removed in future versions since there can be no glitches on CIAK0.

4.4 Bus Abort Feature (BAF)

Due to the I/O Bus being a shared resource, each peripheral must wait an arbitrary amount of time to use the bus, while all this time the 80186 CPU is locked up. Such indetermination may be unacceptable for some peripherals (Ports for example) and for this reason, we have included the BAF.

Timer 1 of the 80186 is used as a bus timer which is reset at the start of each bus cycle - programmed or DMA, off-board or on-board. After some programmed length of time for which it hasn't been reset, the timer will fire, causing CIO hardware to force a ready to the 80186, prematurely ending the cycle. In addition, PCSR[6] is set to one and an internal timer interrupt is generated.

It is important to note that although the on-board cycle has been aborted, the I/O Bus cycle was not; the peripheral's bus request is still active. Therefore, when the bus acknowledge is finally received, CIO hardware will execute a "dummy" (read) cycle. Furthermore, in the interest of synchronization, firmware must not attempt to use the I/O Bus until the "dummy" read has completed. To this end, the forced ready is recorded in PCSR[6]; firmware can read PCSR[7-0]

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10. PCSR[0] (INT0) will **NOT** be set as a result of the interrupt acknowledge.

11. Recall PDTACK0 is also released asynchronously.

as an 8-bit quantity.

Applications which use the BAF must be prepared to handle the timer 1 interrupt (clean up stack pointer, etc.) and must set up the 80186's timer 1 control block (Mode/Control, Max Count A, Max Count B and Count Registers) as follows:

TABLE 2. SETTING 80186 TIMER 1 FOR BAF

Register	Value	Description
Mode/Control - ALT	0	Use only Max Count A
Mode/Control - CONT	0	Halt on max count
Mode/Control - EXT	0	Internal clocking of timer
Mode/Control - P	0	Do not use timer 2 as prescaler
Mode/Control - RTG	1	Retrigger timer on external event
Mode/Control - EN	1*	Enable timer
Mode/Control - INT	1	Interrupt on terminal count
Max Count A	<applic. defined>	0.5 usec x Count A = timeout value e.g. Max Count of 2000 corresponds to 1 msec.
Max Count B	x	don't care
Count Register	0	initialize count to 0

Notes:
* The BAF can be disabled simply by setting EN to 0

The Timer Interrupt Control Register should be programmed in non-iRMX 86™[12] mode with MSK = 0 (unmasked) and PR2,1,0 = 0,0,0 (highest priority). In addition, if a DMA job is to be run, firmware should set up DMA Controller 0 in destination synchronized mode. Finally, CIO hardware will ensure that this DMA controller does not start up until the I/O Bus is unoccupied (PBUSY0 inactive)[13] or if PCSR[6] is active (pg 3).

In the event of a bus timeout, PCSR[6] will be set to 1 and *held* at 1 until the "dummy" read has completed. Once this cycle has completed, PCSR[6] will continue to remain at 1 until CIO firmware clears it by referencing the PCSR[6] location indicated in Table 4. Note, therefore, that attempting to clear PCSR[6] while the "dummy" read is pending will not be successful. In addition, DMA controller 0 will be inactive while PCSR[6] is 1, assuming it has been programmed in a "synchronized" mode. This guarantees that on a bus abort, DMA controller 0 will not start up until firmware clears PCSR[6].

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12. iRMX 86 is a trademark of Intel Corp.

13. Even so, the controller may not get immediate access to the bus since other peripheral's may also be waiting to use the bus.

The sequence that firmware should perform on a timeout of a DMA job is as follows:

(PCSR[6] will be set which disables DMA controller 0.)

1. On timer 1 interrupt, allow time-critical application code execute.
2. Prepare DMA controller 0 for retry (e.g. back up source and destination pointers by 1)
3. Attempt to clear PCSR[6].
4. Check PCSR[6] to be 0; if so, I/O Bus is available and DMA job can now proceed, else attempt to clear PCSR[6] again.

Note: Firmware must never attempt to access DPDRAM while PCSR[6] equals 1.

Referring to the "186 R/W of DPDRAM" state diagram, the timer is running while the FPLS is in state *rw1*. If after the programmed time limit, we still have not gotten the bus CTMRO10 will go active causing PCSR[6] to be set (CSR60 and CSR61 activated - pg 9). CSR60 is input to the FPLS and seen as TIMEOUT0 causing a transition to *rwtime0* and activation of CFRCRDY0. In addition, CFRCRDY1 (invert of CFRCRDY0) activates the 80186 ARDY input (CARDYA1 - pgs 3, 8), prematurely ending the cycle. (Timer 1 firing also generates an internal interrupt to the 80186.)

The FPLS, however, must maintain its PBRQ0 active during and after the forced cycle which means that it could receive a bus acknowledge during this time. Since a peripheral can not hold the bus for more than (5) usec., the FPLS will go through a "dummy" read of main memory when it does receive a bus acknowledge. Moreover, since the 80186 is off doing something else, CIO hardware must not depend on the 80186 for address or control signals. Therefore, such a read is like a normal read except that CSR60 forces both PDS10 and PDS00 to be LOW (pg 7) while CSR61 forces PR1W0 (pg 12) and COEDAT0 (pg 6) to be HIGH. Also, the address used with the aborted cycle had been latched (pg 11) and held constant while waiting to perform the "dummy" read.

4.5 Fault Handling

As mentioned earlier, the 80186 contains three programmable timers, where their use is ultimately determined by a given application. Timer 1 is used within BAF and timers 0 and 2 are left exclusively to the application. This implementation of CIO routes the output of timer 0 (CTMRO00) to Peripheral Fail (PFAIL0) on the I/O Bus (pg 3) such that it can be used as a sanity timer or as a means to manipulate PFAIL0 under firmware control.

Another error handling signal, PFLT0, exists in the I/O Bus. If the DPDRAM controller returns PFLT0 instead of PDTACK0 (as in case of bus timeout or parity error on read), the CIO will end the cycle and generate a Non Maskable Interrupt (NMI) to the 80186. NMI is latched within the 80186 and not registered in the PCSR; the corresponding service routine does not have to take any action to remove the source of the NMI.

5. HARDWARE /SOFTWARE INTERFACE

Tables 3 and 4 illustrate how a CIO-based peripheral and the System Board fit in each others address spectrum. The mapping of CIO hardware to 80186 firmware/software is also shown in Table 4. These tables can be found in [1] and are repeated here for convenience.

TABLE 3. I/O PHYSICAL ADDRESS SPECTRUM (From System Board)

Offset Addr. (4)	Register	Access	Size (bytes)	Action Taken
0 (5)	*ID*	read only	1	INT0 (1)
1	*ID/Vector*	read only	1	INT0 (1)
3	*Control*	-	1	INT1 (2)
5	*Status*	-	1	Reset (3)

Notes:
(1) Reference (read or write) of this address will set PCSR[0] to one (activate hardware interrupt INT0). In the case of a read, the ID code or interrupt vector is returned. Write data is arbitrary.
(2) Reference (read or write) of this address will set PCSR[1] to one (activate hardware interrupt INT1). Undefined data is returned on a read and write data is arbitrary. (Recall the Control and Status registers are nothing more than addressable locations.)
(3) Reference (read or write) of this address will reset the peripheral and its sub-devices. Undefined data is returned on a read and write data is arbitrary. (Refer to the "CIO Hardware on Reset" section.)
(4) Each peripheral has a unique base address as defined in [2].
(5) Applicable only to 16-bit peripherals, in which case byte 0 of ID code.

TABLE 4. I/O PHYSICAL ADDRESS SPECTRUM (From 80186)

Base Address Memory	Base Address I/O	Chip Select	Description	Access	Width (bits)	Size (bytes)
0x00000	*N/A*	*LCS*	RAM (vec. tbl.)	R/W	16	128
00080	*N/A*	*LCS*	RAM (DEMON)	R/W	16	256
00180	*N/A*	*LCS*	RAM (*applic.*)	R/W	16	255.6k
40000	*N/A*	*(3)*	*application*			256k
80000	*N/A*	*MCS*	DPDRAM	R/W	16	128k per page
A0000	*N/A*	*MCS*	*application*			128k
C0000	*0x400*	*PS0*	DEMON			128
C0080	*480*	*PS1*	ID/Vector	W	16	2
C0082	*482*	*PS1*	Page Register	W	7	
C0084	*484*	*PS1*	PCSR[7-0]	R	8	1
C0086	*486*	*PS1*	*reserved*			
C0088	*488*	*PS1*	PCSR[0] (INT0)	(1)	1	
C0089	*489*	*PS1*	PCSR[1] (INT1)	(1)	1	
C008A	*48A*	*PS1*	PCSR[2] (INT2)	(1)	1	
C008B	*48B*	*PS1*	PCSR[3] (INT3)	(1)	1	
C008C	*48C*	*PS1*	PCSR[4] *applic.*		1	
C008D	*48D*	*PS1*	PCSR[5] *res.*		1	
C008E	*48E*	*PS1*	PCSR[6] (BAF)	(2)	1	
C008F	*48F*	*PS1*	PCSR[7] (PINTx0)	(1)	1	
C0100	*500*	*PS2*	*application*			128
C0180	*580*	*PS3*	*application*			128
C0200	*600*	*PS4*	*application*			128
C0280	*680*	*PS5*	*application*			128
C0300	*700*	*PS6*	*application*			128
C0400	*FF00*	*186*	80186 Control Block		16	256
C0420	*FF20*	*186*	Interrupt Ctrl.		16	32
C0450	*FF50*	*186*	Timer 0 Ctrl.		16	8
C0458	*FF58*	*186*	Timer 1 Ctrl.		16	8
C0460	*FF60*	*186*	Timer 2 Ctrl.		16	6
C04A0	*FFA0*	*186*	Chip Select Ctrl.		16	10
C04C0	*FFC0*	*186*	DMA 0 Ctrl.		16	12
C04D0	*FFD0*	*186*	DMA 1 Ctrl.		16	12
C04FE	*FFFE*	*186*	Relocation Reg.		16	2
F0000	*N/A*	*UCS*	(EP)ROM	R	16	63.9k
(4)	*N/A*	*UCS*	DEMON ROM	R	16	128

Notes:
(1) Bit is invariably cleared to zero on an 80186 access of this PCSR bit
(2) Bit is cleared to zero on an 80186 access of this PCSR bit *if "dummy" read of BAF is not pending.*
(3) External address decoding will be required to select addresses in 0x40000 to 0x7ffff range.
(4) The application will link their ROM firmware with a DEMON function that will be at most 128 bytes in size.

6. ELECTRICAL DESCRIPTION

6.1 Signals

Table 5 defines several CIO signals. These are a subset of those found in [1] with one difference: CARDY1 is referred to as CARDYA1 in this implementation.

TABLE 5. CIO SIGNALS

Signal	*#*	*Source*	*Description*
CA[19-16]1	4	CIO	Upper 186 unlatched address bits
CAD[15-00]1	16	CIO/Ap	186 multiplexed address/data
CALE1	1	CIO	186 Address latch enable
CARDYA1	1	CIO/Ap	Async. data ready
CBHE0	1	CIO	186 Bus high enable
CD[15-00]1	16	CIO/Ap	Local data
CDEN0	1	CIO	186 Data buffer output enable
CDT1R0	1	CIO	186 Data buffer direction control
CFRCRDY0/1	1	CIO	BAF forced ready
CINT[0-3]1	4	CIO/Ap	186 interrupt request
CLCS0	1	CIO	186 lower (RAM) chip select
CLKIN1	1	CIO	186 osc. input (16MHz)
CLKOUT1	1	CIO	186 8MHz clock output
CMCS0	1	CIO	186 Mid-Range (DPDRAM) chip select
CPA[19-00]1	20	CIO/Ap	Local physical addr.
CPCS[0-6]0	7	CIO	186 Periph. chip selects
CPxGRD0	1	CIO/Ap	Pull down resistor nets
CPxVCC1	1	CIO/Ap	Pull up resistor nets
CRD0	1	CIO	186 Read strobe
CRESETI0	1	CIO	186 reset input
CRESETO1	1	CIO	186 sync. reset output
CSRCLR[0-7]0	8	CIO/Ap	PCSR bit clear
CSRSET[0-7]0	8	CIO/Ap	PCSR bit set
CSR[7-0]1	8	CIO	PCSR byte
CTMRI[0-1]1	2	CIO/Ap	186 Timer inputs
CTMRO[0-1]0	2	CIO	186 Timer outputs
CUCS0	1	CIO	186 Upper (ROM) chip select
CWR0	1	CIO	186 Write strobe
SYSRST0	1	I/O Bus	System reset
V12N	1	I/O Bus	+12 v. power
V12P	1	I/O Bus	-12 v. power
VBKUP	1	I/O Bus	+3.0 v. (10 ua) backup power
VCC	3	I/O Bus	+5 v. power
GRD	15	I/O Bus	Ground

6.2 I/O Bus Loading

The following table presents the maximum current driving and loading of CIO as well as the maximum capacitive loading.

TABLE 6. I/O BUS LOADING

Signal	*#*	*char*	*Iol (mA)*	*Ioh (mA)*	*Iil (mA)*	*Iih (mA)*	*Cap[1] (pf)*
PBUSY0	1	ts	24	-15	-.4	.02	40
PBRQ0	1	oc	40	-	-.4	.02	40
PBACKI0	1	tp	-	-	-7.4[2]	.07	30
PBACKO0	1	tp	20	-1	-	-	35
PCS0	1	tp	-	-	-5.8[2]	.02	30
PD[15-00]0	16	ts	24	-15	-.4	.02	40
PDS[1-0]0	2	ts	24	-15	-.4	.02	40
PDTACK0	1	oc	40	-	-.4	.02	40
PFAIL0	1	oc	40	-	-	-	35
PFLT0	1	oc	-	-	-.4	.02	25
PINT[i]0	1	oc	40	-	-	-	35
PIAKI[i]0	1	tp	-	-	-5.4[2]	.02	25
PIAKO[i]0	1	tp	20	-1	-.4	.02	40
PLOCK0	1	ts	24	-15	-	-	35
PPA[23-03]1	21	ts	32	-15	-	-	35
PPA[02]1	1	ts	32	-15	-.4	.02	40
PPA[01]1	1	ts	32	-15	-.1	.025	40
PPA[00]1	1	ts	32	-15	-.4	.02	40
PPAS0	1	ts	24	-15	-.4	.02	40
PR1W0	1	ts	24	-15	-.4	.02	40
PSIZE160	1	oc	40	-	-	-	35
RQRST0	1	oc	-	-	-	-	-
SYSRST0	1	tp	-	-	-.4	.02	25

Notes:

1. Calculation of maximum capacitance based on:
   - Input buffer - 5.0 pf
   - Output buffer - 14.0 pf
   - Via - 0.7 pf (at most 6 vias assumed)
   - MLB routing - 2.4 pf per inch (at most 6 inches assumed)
   - Edge connector - 3.0 pf

2. Includes 5 mA through pullup resistor. See next section.

Refer to [3] for a full description of these signals.

6.3 Termination

PBACKI0 and PIAKI[i]0, daisy-chain inputs, and PCS0 are pulled up to VCC through 1k ohms. In the interest of testability, no IC control pin is connected directly to VCC or GRD, rather, a control pin is either pulled HIGH through 4.7k ohms or LOW with 100 ohms. (Several pins are pulled up/down with one resistor.)

6.4 CIO Power Dissipation

3B 2 system requirements allow each peripheral dissipate at most 10 watts (typical) of which CIO circuitry (Issue 1) with two 2764 EPROMs dissipates 7.8.

TABLE 7. CIO POWER DISSIPATION (TYPICAL)

Subcomponents	*IC #*	*Device*	*Power (watts)*	*Spare Gates*
80186	1	80186	2.8	
I/O Bus Controller	13	LS374	.135	
	14	82s105	.650	
I/O Bus Buffers	7	29843	.325	
	8	29843	.325	
	9	29843	.325	
	10	LS646	.500	
	11	LS646	.500	
	12	LS244	.130	
Misc. Control	2	LS373	.120	
	3	LS373	.120	
	4	LS373	.120	
	5	LS645	.275	
	6	LS645	.275	
	15	LS74A	.020	
	16	LS139	.034	
	17	LS138	.031	
	18	LS279	.019	
	19	LS279	.019	
	20	LS244	.130	
	21	7407	.125	1
	22	LS32	.020	
	23	LS32	.020	2
	24	LS32	.020	
	25	LS32	.020	
	26	LS32	.020	
	27	LS32	.020	
	28	LS32	.020	
	29	S32	.140	2
	30	LS32	.020	3
	31	LS04	.012	
	32	LS04	.012	1
	33	LS08	.017	
	34	LS08	.017	
	35	LS08	.017	
	36	LS02	.011	1
	37	KS-22320L1	.085	
	38	LS21	.009	1
	39	2764	.160[1]	
	40	2764	.160[1]	
	41	LS74A	.020	

Notes:
1. Calculated for 10% active, 90% inactive

6.5 Parts Placement (Typical)

Although there is no formalized placement with Issue 1 of CIO hardware, a "typical" layout has been attached (Attachment 4). In addition, Attachment 5 presents guidelines which should be followed when reviewing the net length, parallelism and crosstalk audits for each peripheral which uses Issue 1 of CIO hardware.

6.6 Power Filtering

The "typical" layout of Attachment 4 includes capacitors decoupling VCC to ground as specified in [8].

7. SUMMARY

This document described the circuit of the first implementation of CIO hardware. Section 2, **CIO HARDWARE OVERVIEW**, presented the "passive access" issue and its influence on CIO architecture. The **SUBCOMPONENTS** of CIO hardware were discussed in Section 3 - namely, the 80186, I/O Bus interface, PCSR, and miscellaneous support logic. Section 4 discussed the **BASIC OPERATIONS** of CIO hardware in detail: (1) 80186 access of DPDRAM, (2) System Board CPU access of a CIO-based peripheral, (3) interrupt acknowledge cycle, (4) BAF and (5) fault handling. The address spectrum of the WE-32000 and 80186, presented in Section 5, illustrated the **HARDWARE / SOFTWARE INTERFACE** of CIO hardware. Finally, Section 6 contained the **ELECTRICAL DESCRIPTION** of CIO, notably CIO signal definition, I/O Bus loading and CIO power dissipation.

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IW-45134-PMW-unix

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Atts.
references

Attachment 1:	CIO Hardware Schematic - Issue 1	(pages 1 - 18)
Attachment 2:	CIO Hardware FPLS State Diagrams - Issue 1	(pages 1 - 5)
Attachment 3:	CIO Hardware Timing Diagrams - Issue 1	(pages 1 - 6)
Attachment 4:	CIO Hardware Typical Layout - Issue 1	
Attachment 5:	3B™2 CIO LDI LD: Audit Review Guidelines	(pages 1 - 2)
Attachment 6:	CIO Hardware FPLS ASCII Source Code	
Attachment 7:	CIO Hardware FPLS Logic Diagram	

REFERENCES

1. G. E. Laggis, et al, "3B2 Requirements - I/O Board Hardware and Firmware Architecture and Design," November 4, 1983.

2. D. C. Bina, et al, "3B2 System Architecture and Requirements", 49343-0011, February 10, 1983.

3. P. M. Walsh, "3B 2 Component Requirements and Specifications: I/O Bus", March 7, 1983.

4. K. A. McWethy, J. M. Sullivan and L. E. Wallis, "3B2 Feature Requirements - Core System Hardware," March 7, 1983.

5. Intel Corporation, "iAPX 16 High Integration 16-bit Microprocessor", Data sheet, May 1982.

6. Signetics Corporation, "Integrated Fuse Logic Data Manual", 1983.

7. R. R. Hylka and A. D. Niemi, "3B*2 Common I/O Hardware Timing Results", October 11, 1983.

8. E. L. Hepler, D. M. Olien and P. M. Walsh, "3B2 Component Design: Review Guidelines", July 5, 1983.

ATTACHMENT 1-1

ITEM

LDI ISSUE 1A | SHEET 1/18

CODE OR DOCUMENT IDENTIFICATION

CIO HW

3B2

COMMON I/O HARDWARE SCHEMATIC - ISSUE 1

RELEASE	DATE	PAGES AFFECTED	REMARKS
LA	9/15/83	1-18	ORIGINAL RELEASE
LB	10/4/83	1, 5, 6, 7, 14, 16	SUPPORT 16-bit ID CODE (3 ADDS, 3 DELETES)
LC	10/31/83	1, 2, 5, 8, 9, 10, 16.5, 15, 16	DAISY-CHAIN (BUS ACK. & INTERRUPT ACK.) FIX (20 adds, 16 deletes)
LD	12/28/83	1, 3, 8, 15, 16, 18	BAF FIX & TIE TIMER 0 PIN PULLED HIGH (3 ADDS, 2 DELETES)

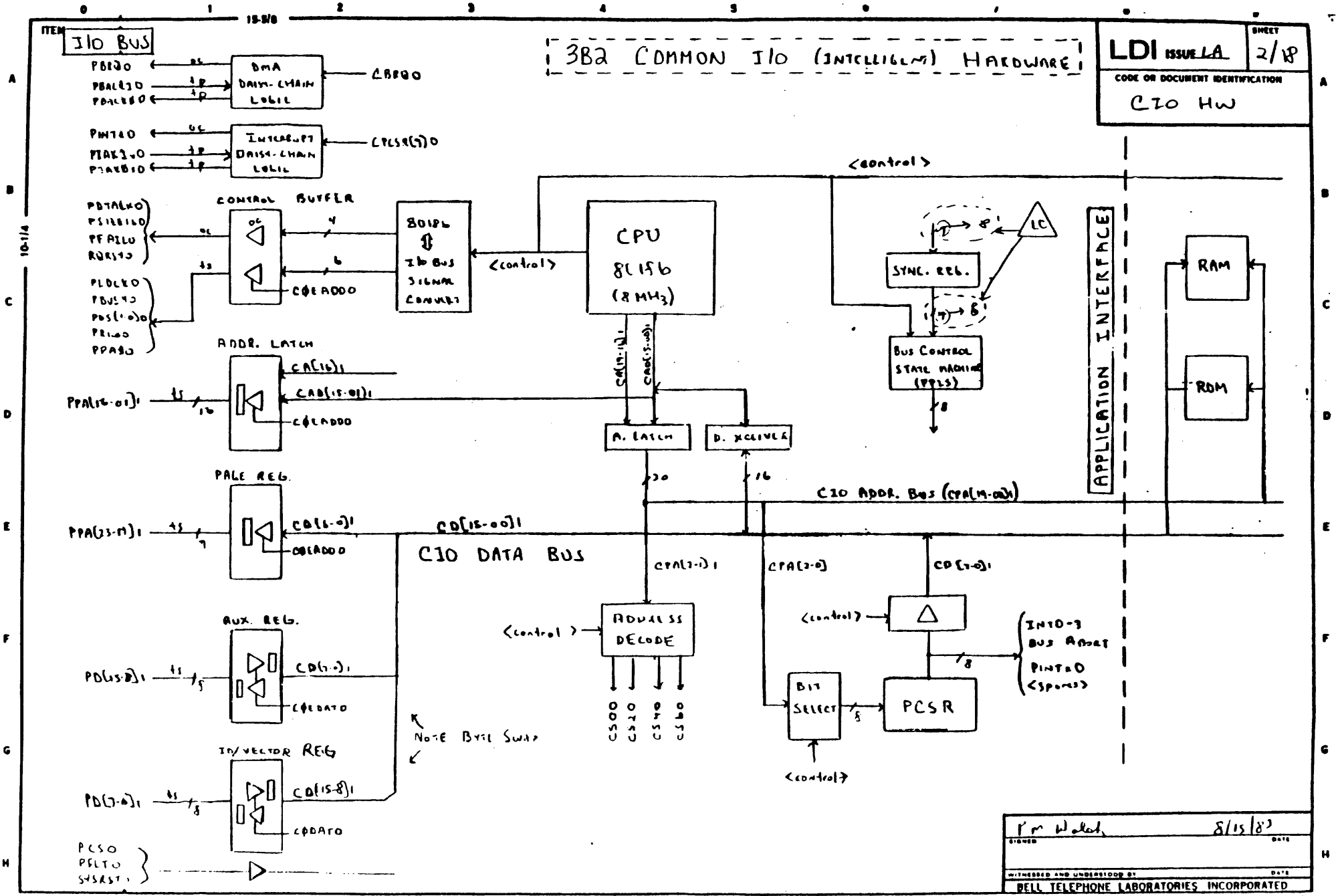
P. M. Wehl 9/12/83

SIGNED DATE

WITNESSED AND UNDERSTOOD BY DATE

BELL TELEPHONE LABORATORIES, INCORPORATED

ATT. 1-2



PRIVATE

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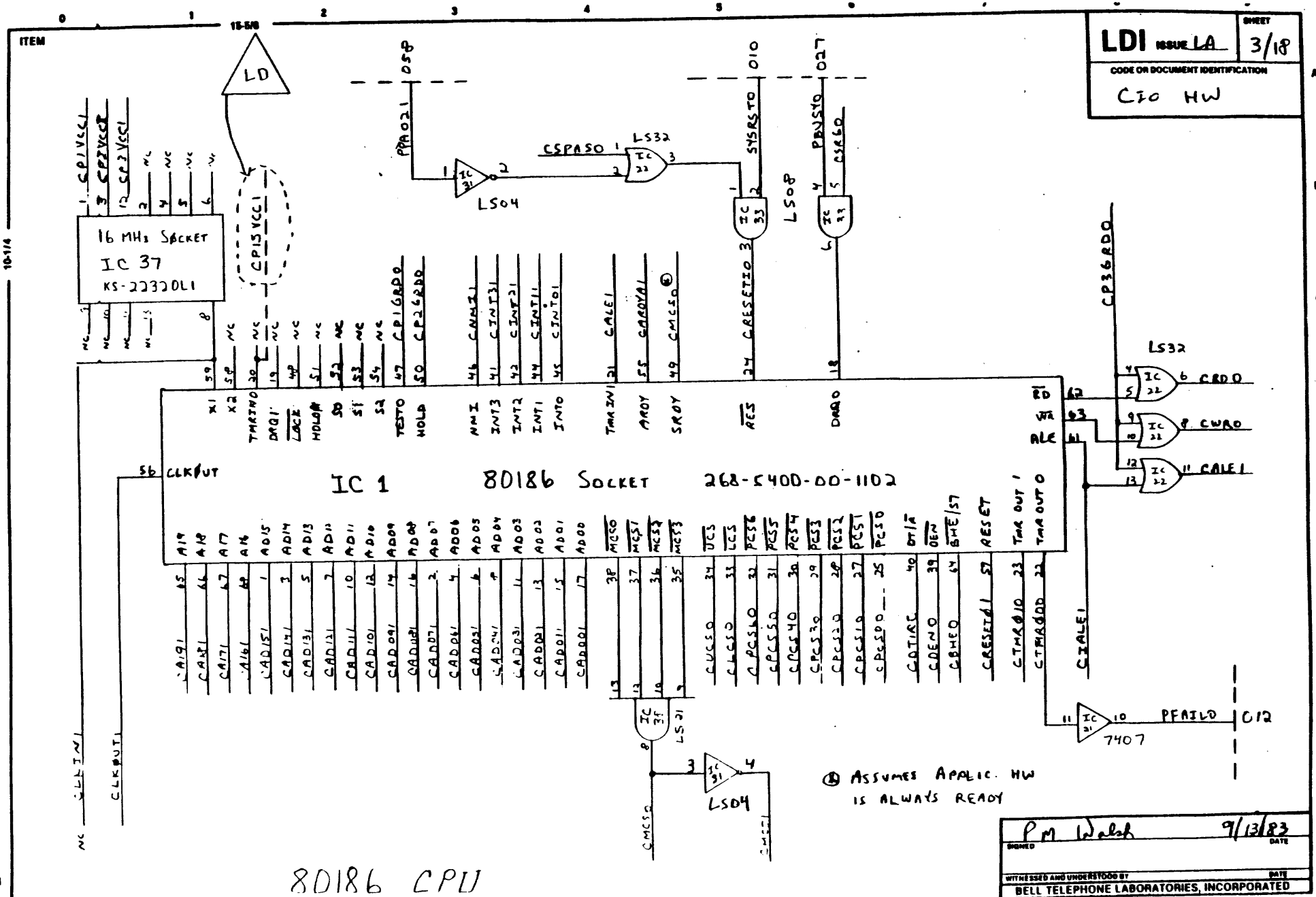
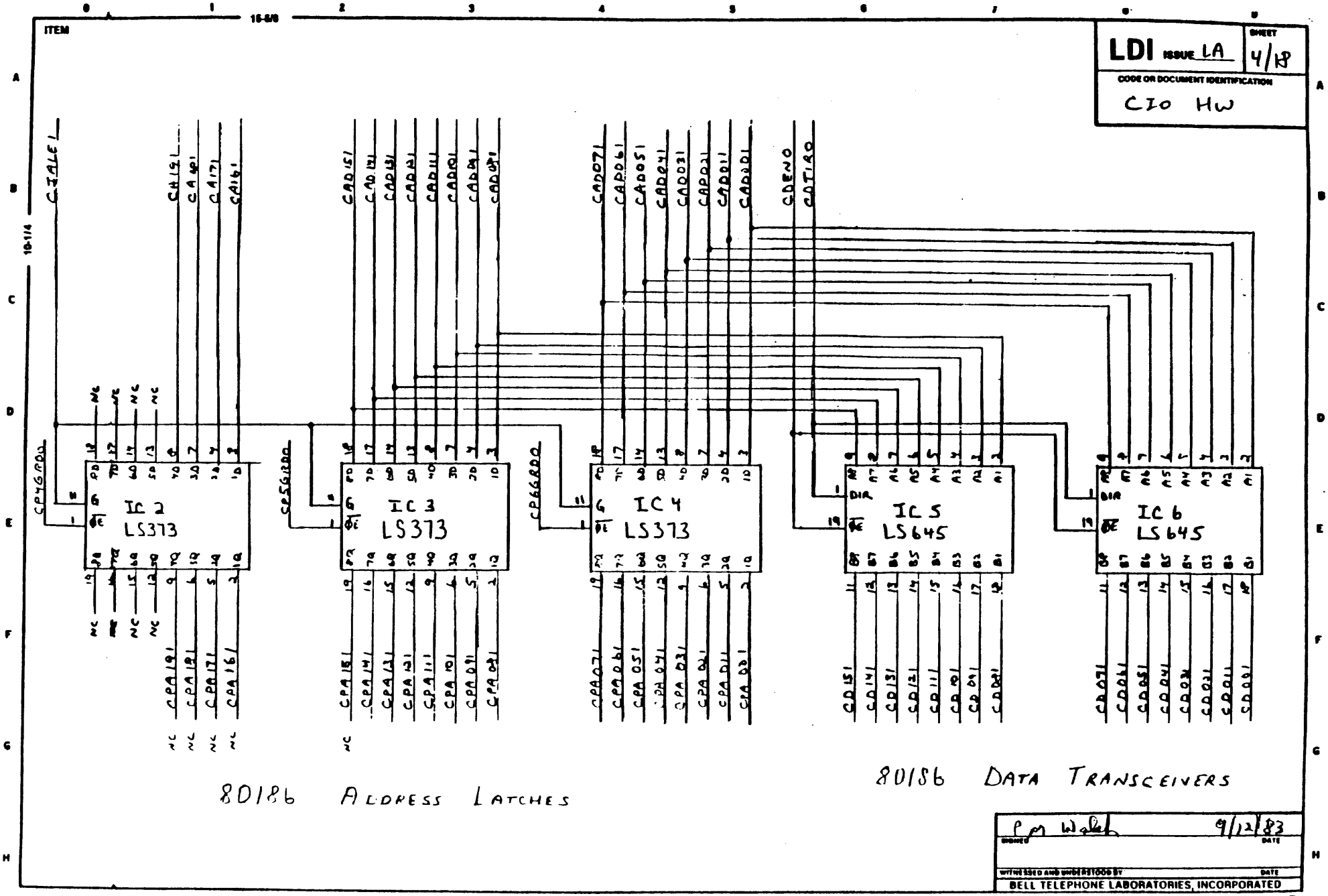
ATT 1-3

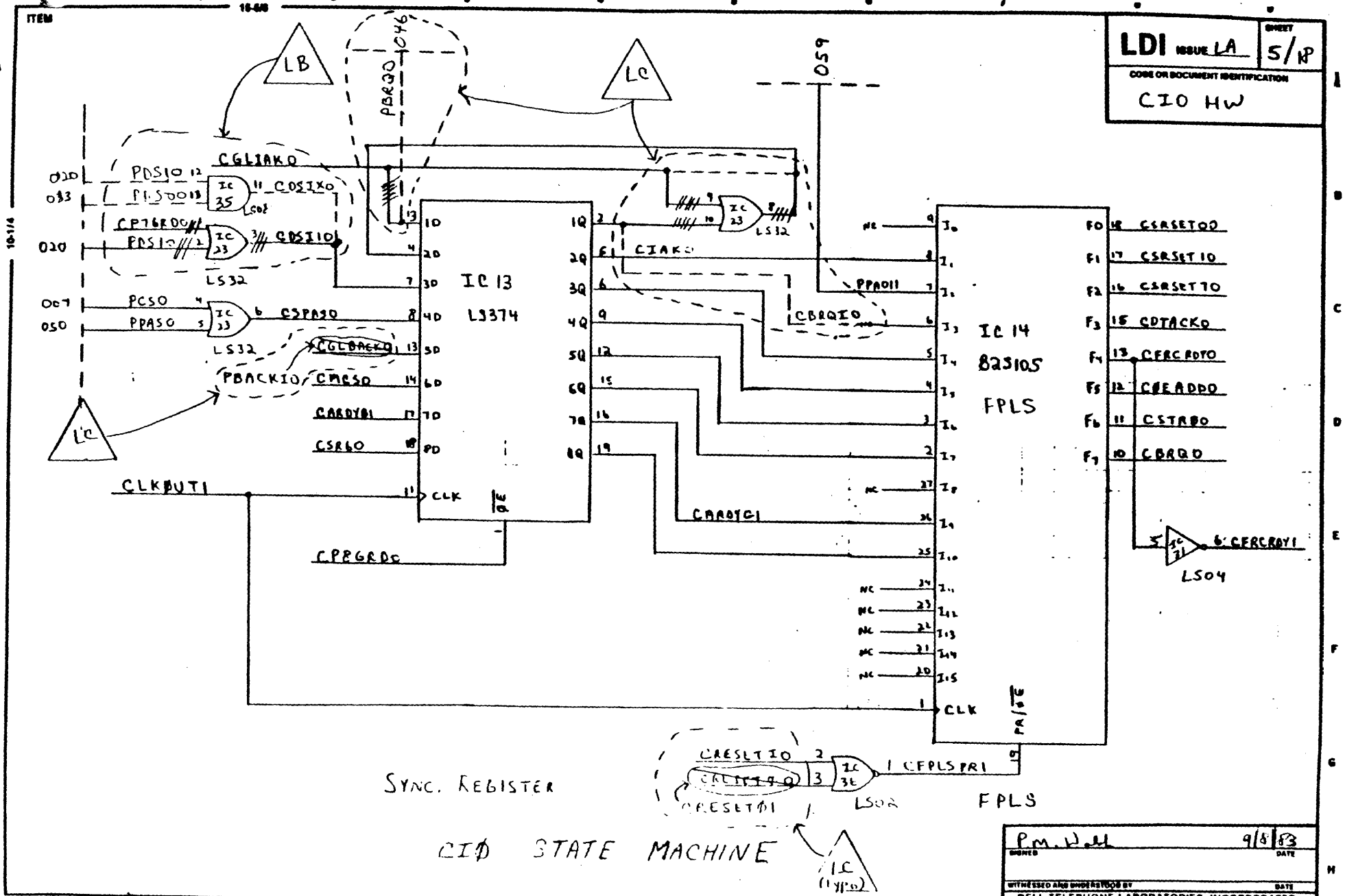


(A) ASSUMES APPLIC. HW IS ALWAYS READY

ATT. 1-4



ATT. 1-5



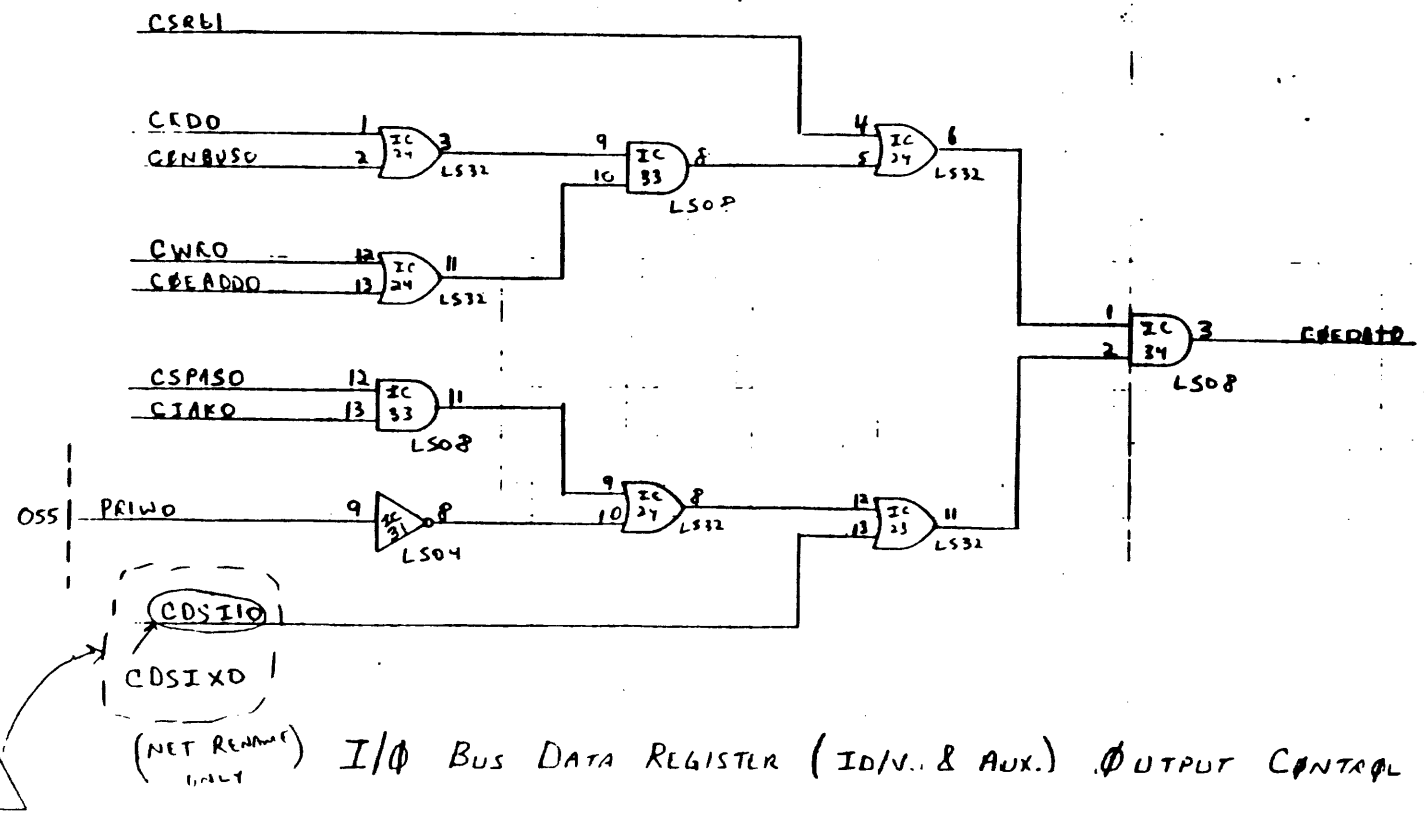
ATT 1-6

ITEM

LDI ISSUE LA SHEET 6/18

CODE OR DOCUMENT IDENTIFICATION

C30 HW



I/Ø BUS DATA REGISTER (ID/V.. & AUX.) ØUTPUT CØNTRØL

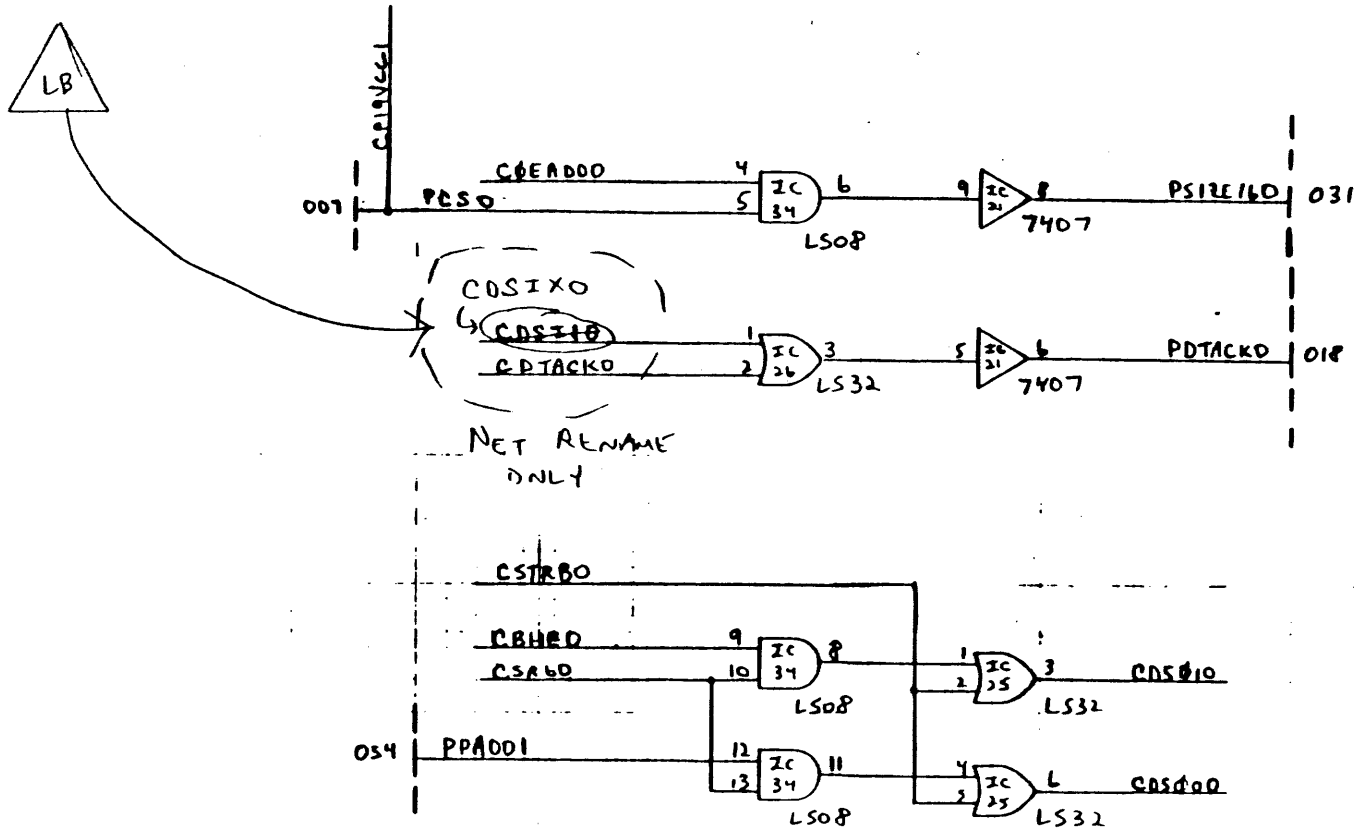
P M Wahl 9/12/83

SIGNED DATE

WITNESSED AND UNDERSTOOD BY DATE

BELL TELEPHONE LABORATORIES, INCORPORATED

ATT. 1-7



MISCELLANEOUS CONTROL

P. M. Wolf 9/12/83
SIGNED DATE

WITNESSED AND UNDERSTOOD BY DATE

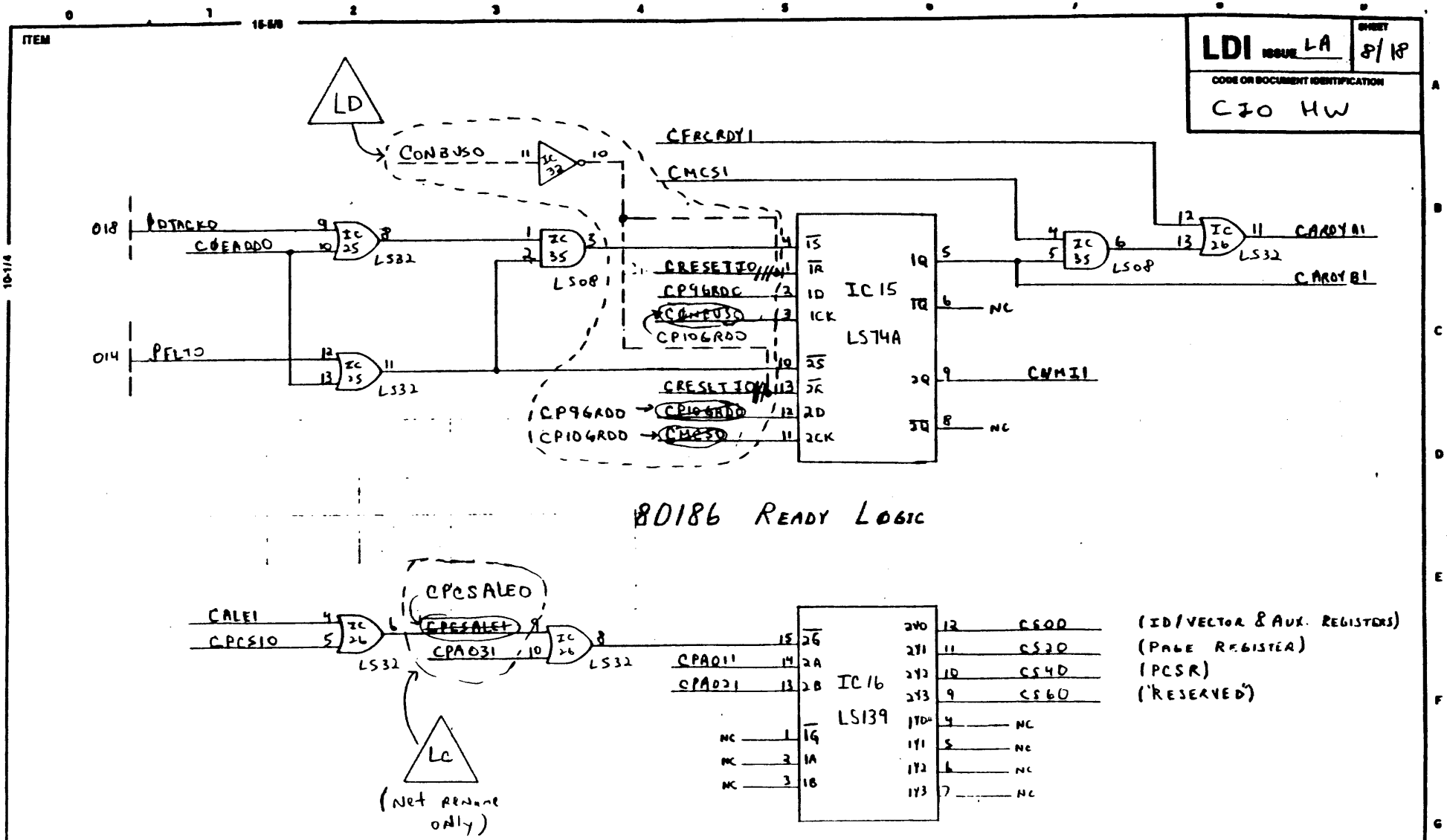
BELL TELEPHONE LABORATORIES, INCORPORATED

LDI ISSUE LA SHEET 7/18

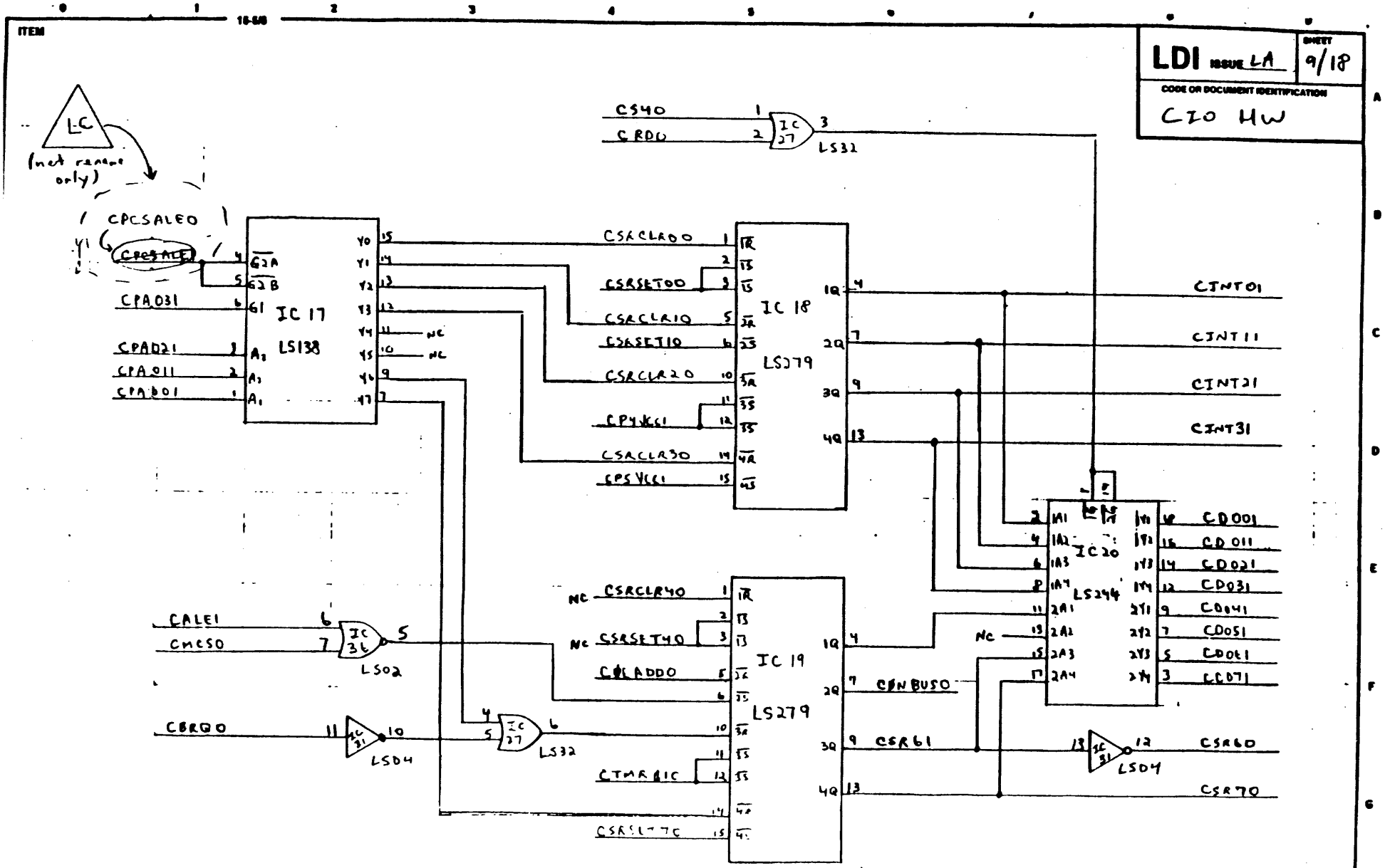
CODE OR DOCUMENT IDENTIFICATION

CIO HW

ATT 1-8

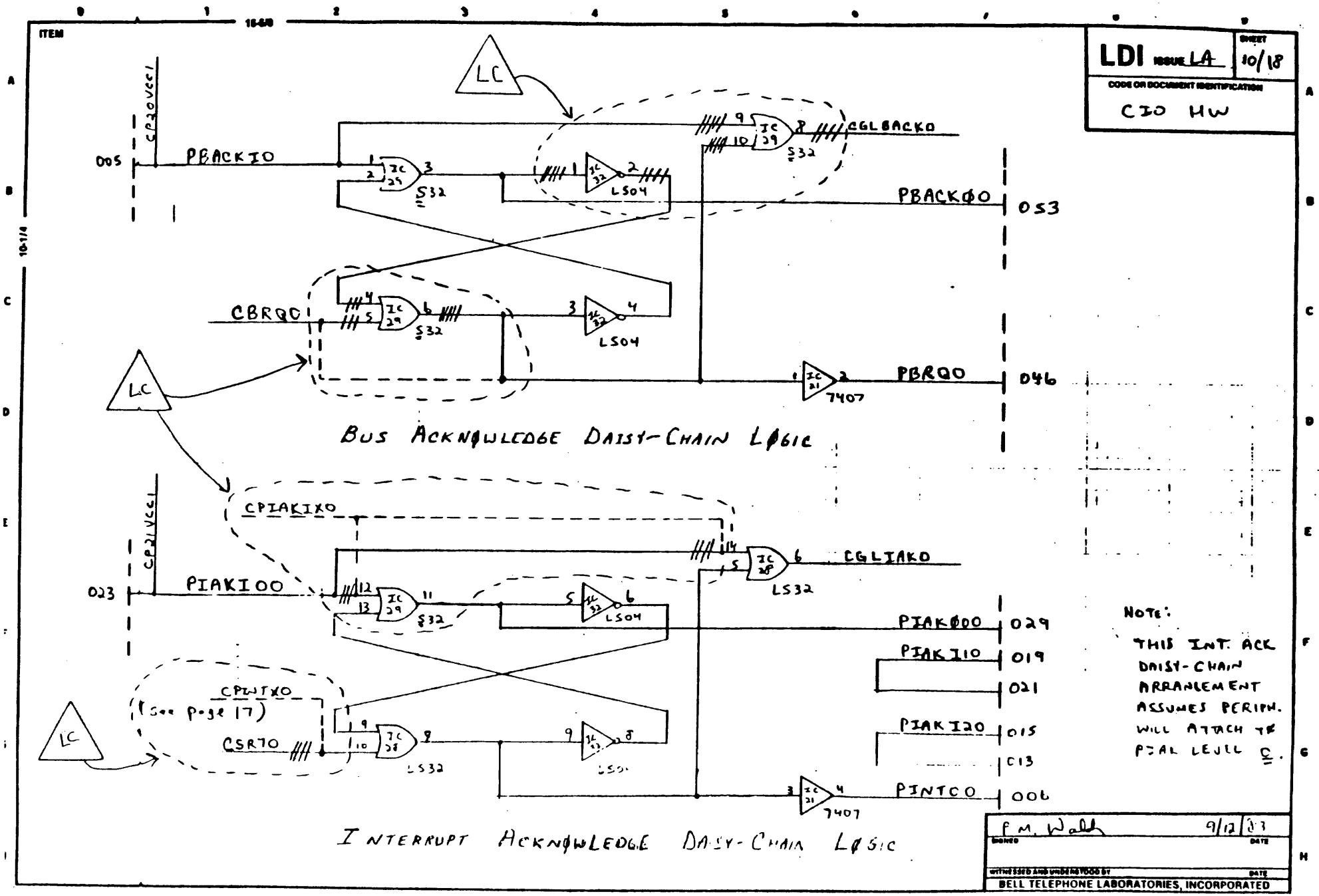


ATT. 1-9

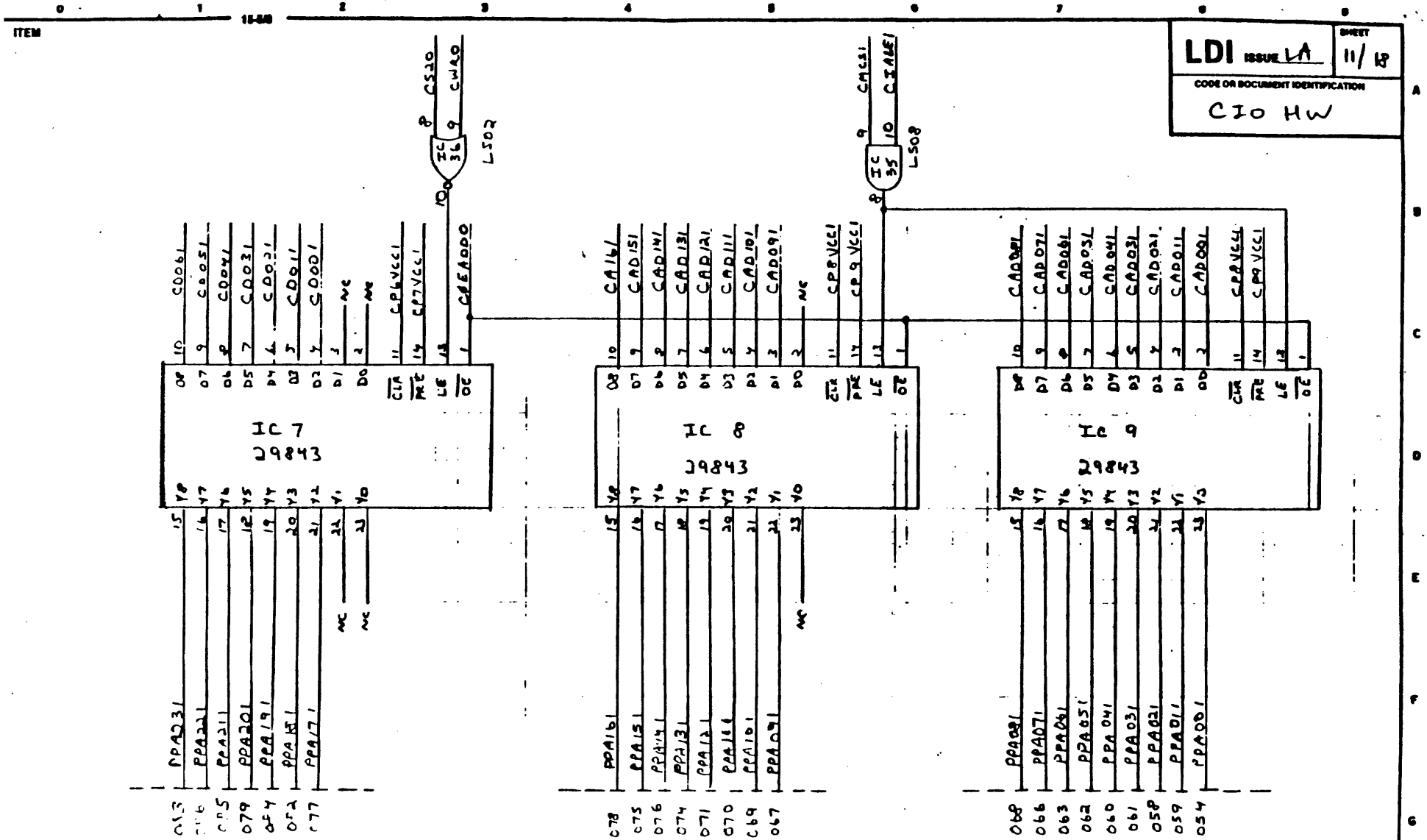


PERIPH. CONTROL & STATUS REGISTER (PCSR)

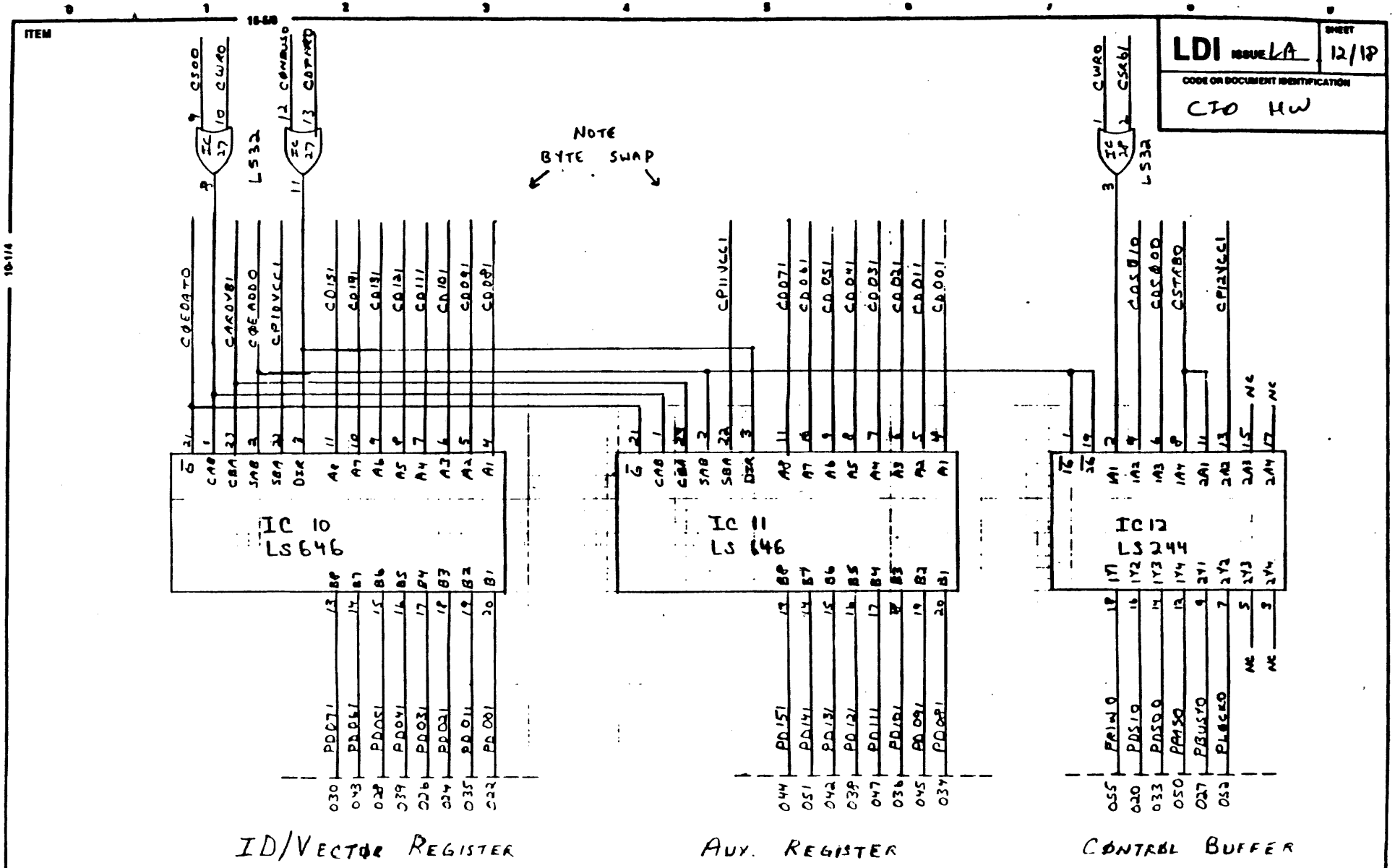
ATT. 1-10



ATT. 1-11



ATT. 1-12



PRIVATE

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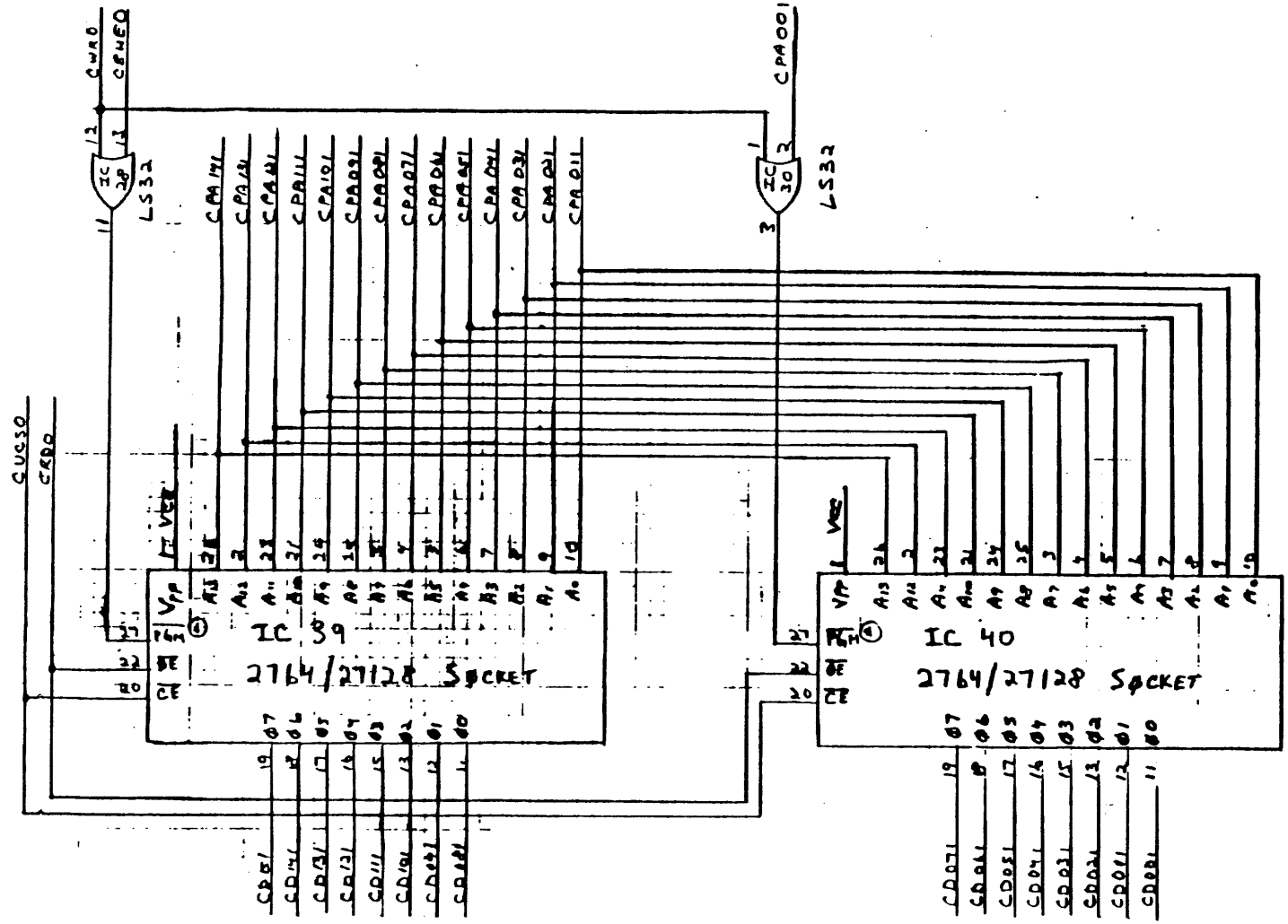
P N W261 9/12/83
SIGNED DATE

WITNESSED AND UNDERTOOD BY DATE

BELL TELEPHONE LABORATORIES, INCORPORATED

ATT. 1-13



TWO 8k/16k (EP)ROM SOCKETS

(● WITH ROM EMULATOR "WRITE" SIGNALS)

LDI ISSUE LA SHEET 13/18

CODE OR DOCUMENT IDENTIFICATION

C20 HW

P M W 9/14/83

SIGNED DATE

WITNESSED AND UNDERSTOOD BY DATE

BELL TELEPHONE LABORATORIES, INCORPORATED

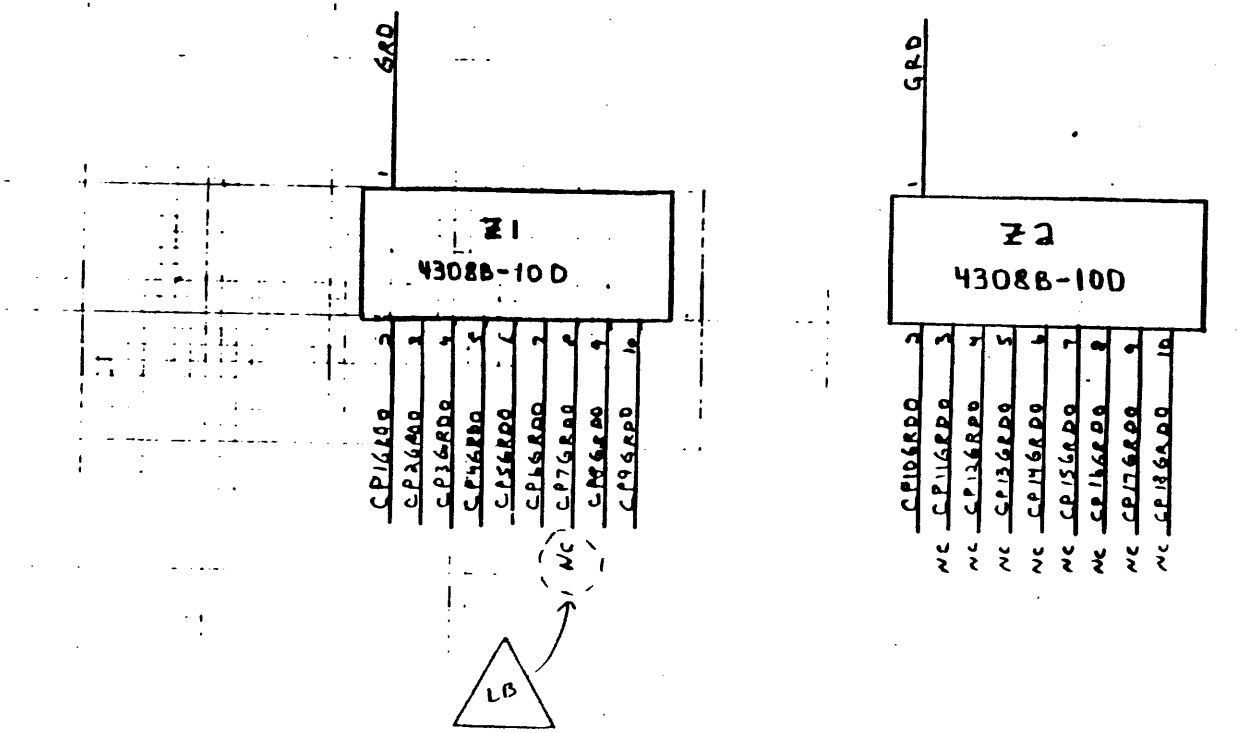
ATT. 1-14

ITEM

LDI ISSUE LA SHEET 14/18

CODE OR DOCUMENT IDENTIFICATION

C20 HW



PULL-DOWN RESISTOR SIPs

P M Walsh 9/14/83
SIGNED DATE

WITNESSED AND UNDERSTOOD BY DATE

BELL TELEPHONE LABORATORIES, INCORPORATED

25

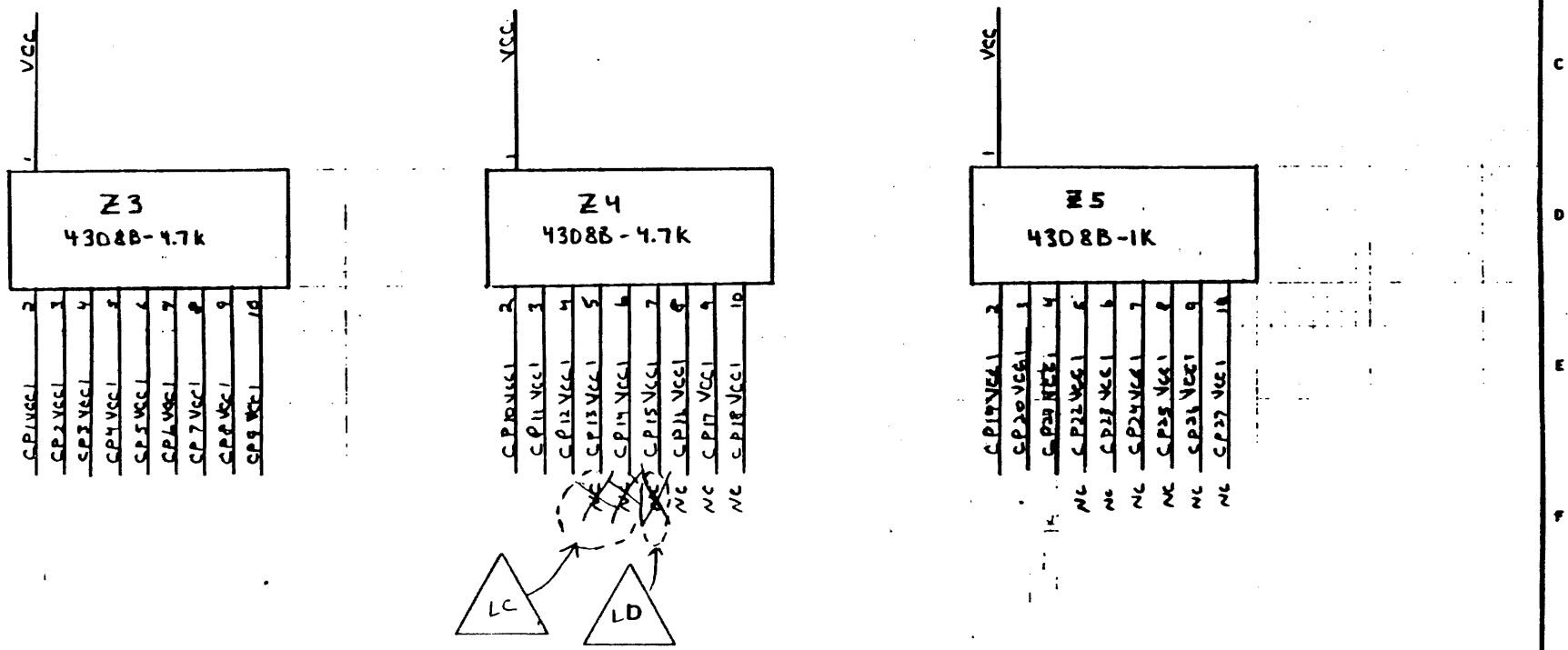
ATT 1-15

ITEM

LDI ISSUE LA SHEET 15/18

CODE OR DOCUMENT IDENTIFICATION

CJO HW



PULL-UP RESISTOR SIPS

P. Webb 9/14/83
SIGNED DATE

WITNESSED AND UNDERSTOOD BY DATE

BELL TELEPHONE LABORATORIES, INCORPORATED

ATT 1-16

15-5/8

LDI ISSUE LA | SHEET 16/18
CODE OR DOCUMENT IDENTIFICATION
CIO HW

ADDS / DELETES (CONT. ON PAGE 18)

ISOLATES

	LDI	ICNo	PIN
1.	LB	23	2
	LB	23	3
	LB	23	1
	LC	13	13
5.	LC	13	3
	LC	23	8
	LC	23	9
	LC	23	10
	LC	29	4
10.	LC	29	5
	LC	29	6
	LC	29	8
	LC	29	9
	LC	29	10
15.	LC	32	1
	LC	32	2
	LC	29	12
	LC	28	4
19.	LC	28	10

ADDS

		FROM		TO		
	LDI	ICND	PIN	ICND	PIN	NET
1.	LB	35	11	13	7	GDSIXO
	LB	BRD	020	35	12	PDS10
	LB	BRD	033	35	13	PDS00
	LC	BRD	005	13	13	PBACKIO
5.	LC	BRD	046	13	3	PBRQO
	LC	28	6	13	4	CGLIAKO
	LC	13	2	14	6	IC13.2
	LC	41	5	29	12	CPIAKIXO
	LC	41	5	28	4	CPIAKIXO
10.	LC	41	9	28	10	CPINTXO
	LC	1	56	32	1	CLKOUT1
	LC	32	2	41	11	CLKOUTO
	LC	24	5	41	1	CP13VCC1
	LC	24	5	41	13	CP13VCC1
15.	LC	24	6	41	4	CP14VCC1
	LC	24	6	41	10	CP14VCC1
	LC	BRD	023	41	2	PIAKIDO
	LC	1	56	41	3	CLKOUT1
	LC	19	13	41	12	CSR7O
20.	LC	13	2	14	6	CBRQIO
	LC	14	10	32	3	CBRQO
	LC	VCC		41	14	
	LC	GRD		41	7	
	LC	NEW MP, IC41, LS74A				

10/31/83
D M Walsh 11/4/83
SIGNED DATE
WITNESSED AND UNDERSTOOD BY DATE
BELL TELEPHONE LABORATORIES INCORPORATED

ATT. 1-17

ITEM

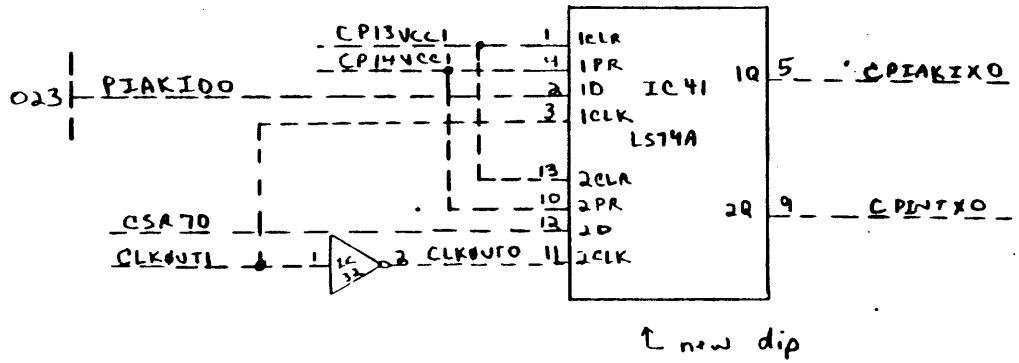
LDI ISSUE LA | SHEET 17/18

CODE OR DOCUMENT IDENTIFICATION

CIO HW

LC

THIS ENTIRE SHEET



INTERRUPT ACKNOWLEDGE DAISY-CHAIN SYNCHRONIZATION

J M WALSH 10/31/83

SIGNED DATE

WITNESSED AND UNDERSTOOD BY DATE

BELL TELEPHONE LABORATORIES INCORPORATED

ATT 1-18

ITEM

LDI ISSUE LA | SHEET 18/18

CODE OR DOCUMENT IDENTIFICATION: CIO HW

ADD / DELETES (CONT. FROM PAGE 16)

ISOLATES

	LDI	IC No.	PIN
20.	LD	15	1
	LD	15	3
	LD	15	13
	LD	15	12
24.	LD	15	11

ADDS

		FROM		TO		
	LDI	IC No.	PIN	IC No.	PIN	NET
25.	LD	24	7	1	20	CP15VCC1
	LD	19	7	32	11	CØNBUSØ
	LD	32	10	15	1	IC32.10
	LD	32	10	15	13	IC32.10
	LD	24	2	15	3	CP106RDØ
30.	LD	24	2	15	11	CP106RDØ
31.	LD	23	10	15	12	CP96RDØ

P M Walsh 12/28/83
SIGNED DATE

WITNESSED AND UNDERSTOOD BY DATE

BELL TELEPHONE LABORATORIES, INCORPORATED

ATTACHMENT 2-1

3B2

COMMON I/O BUS CONTROLLER

DEVICE CODE: 82S105A or 82S105

FUNCTION: FIELD PROGRAMMABLE LOGIC SEQ. (FPLS)

CLOCK RATE: 8 MHz

STATE MACHINE

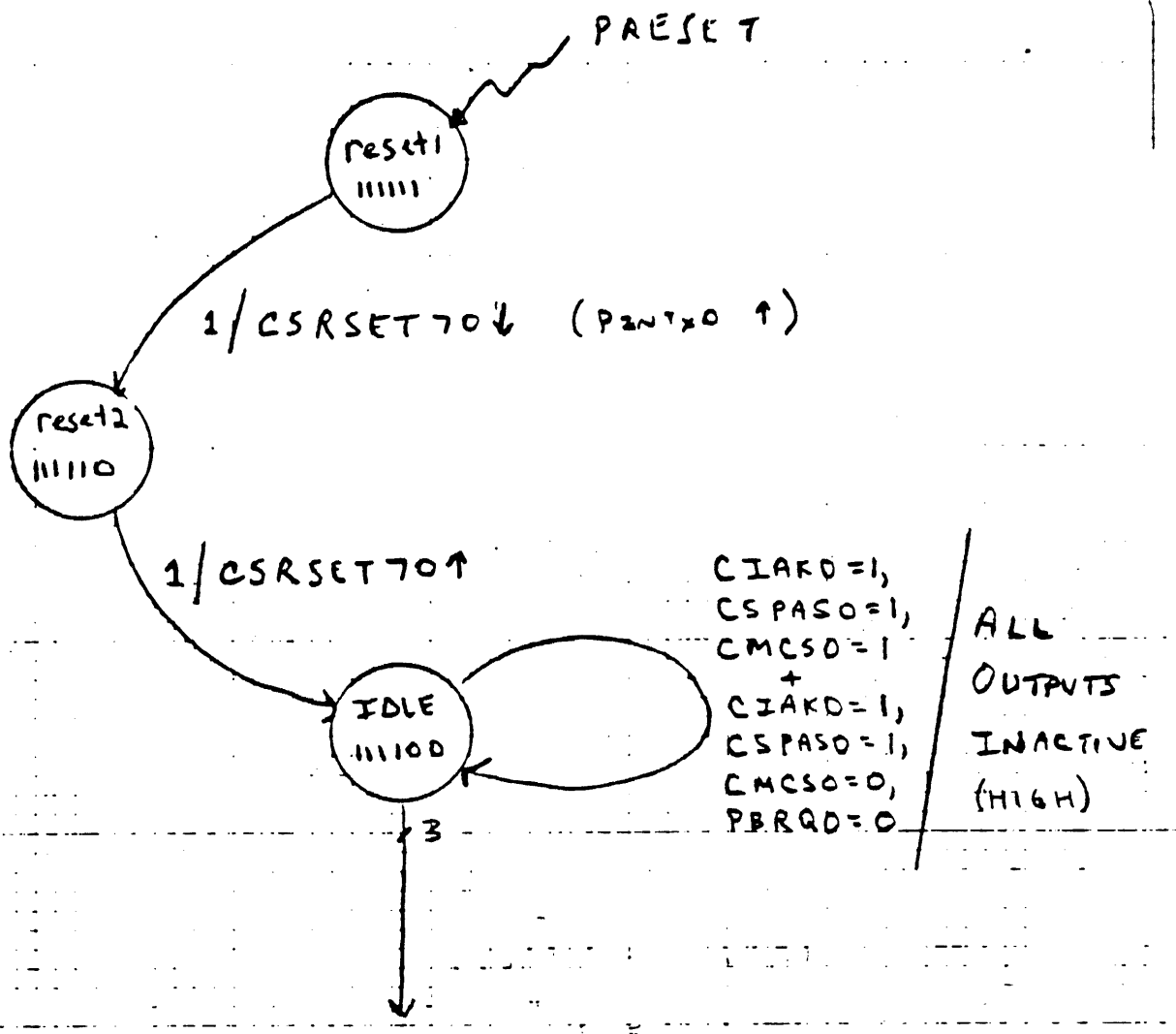
TYPE: MEALY

STATES: 20 OF POSSIBLE 64

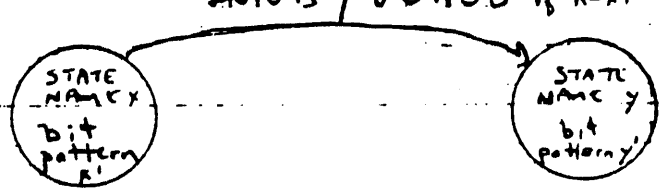
TRANSITIONS: 43 of POSSIBLE 48

NOTE:

ATTACHMENT 2-2



Legend



STATES
3

TRANSITIONS
4 (A+B counts as 2)

NOTE: A COMMA (,) SEPARATING MULTIPLE INPUTS OF A GIVEN TRANSITION TERM IS INTERPRETED AS AN "AND" FUNCTION

8MHz

ATTACHMENT 2-3

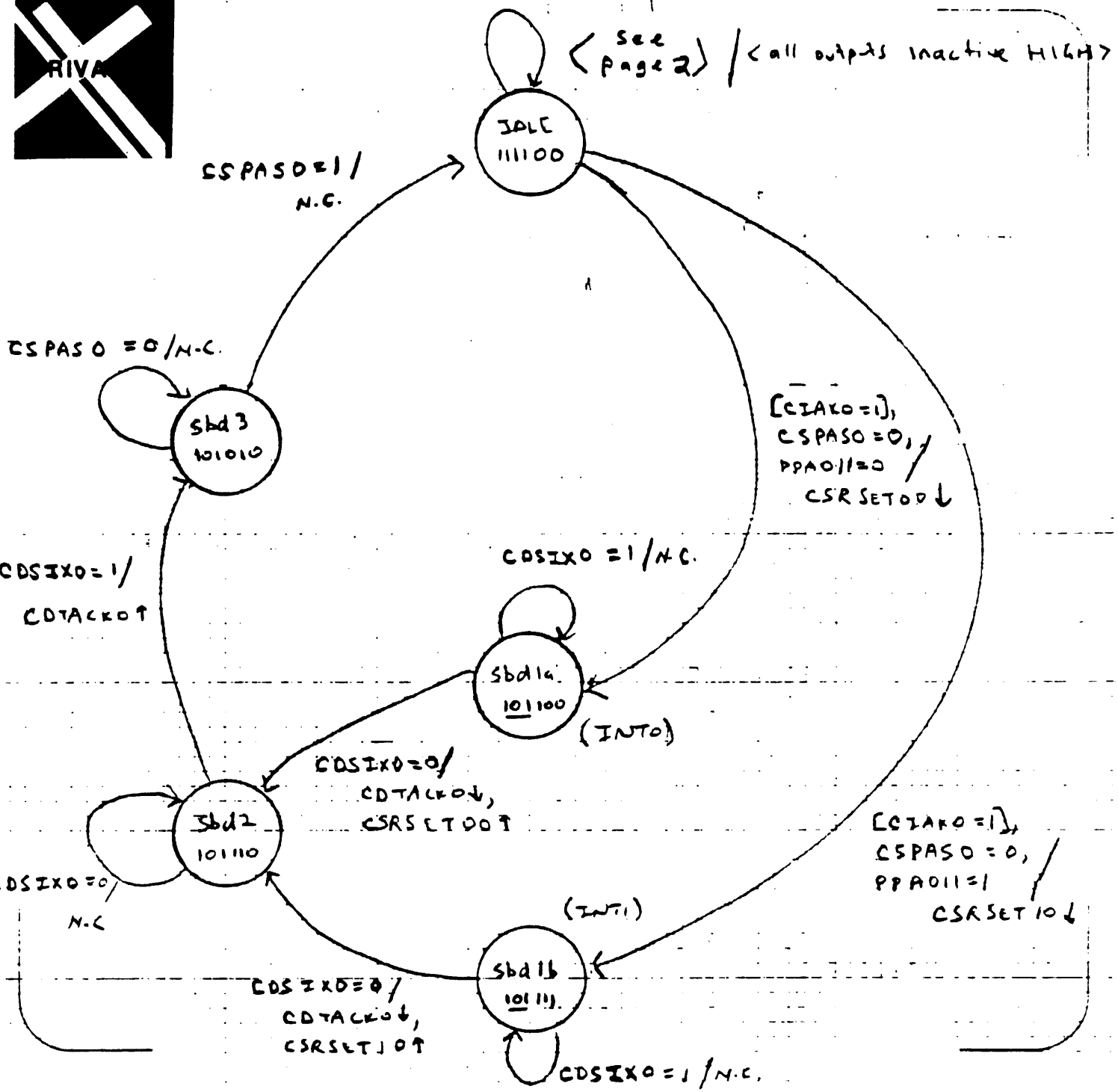
<see page 2>

<all outputs inactive HIGH>

INPUTS	OUTPUTS	# STATES	# TRANSITIONS
1. CMCSO	1. COEADDO	8	18 (A+B counts as 2)
2. CBACKO	2. CSTRBO		
3. TIMEOUTO	3. CFRCROYO		
4. CAROYCI	4. CBRQO		
5. PBRQO			

8 MH3

ATTACHMENT 2-4



INPUTS	OUTPUTS	# STATES	# TRANSITIONS
1. CSPASO	1. CSRSETOO	4	10
2. CDSIXO	2. CSRSLT10		
3. PPAO11	3. CDTACKO		

8 MHz

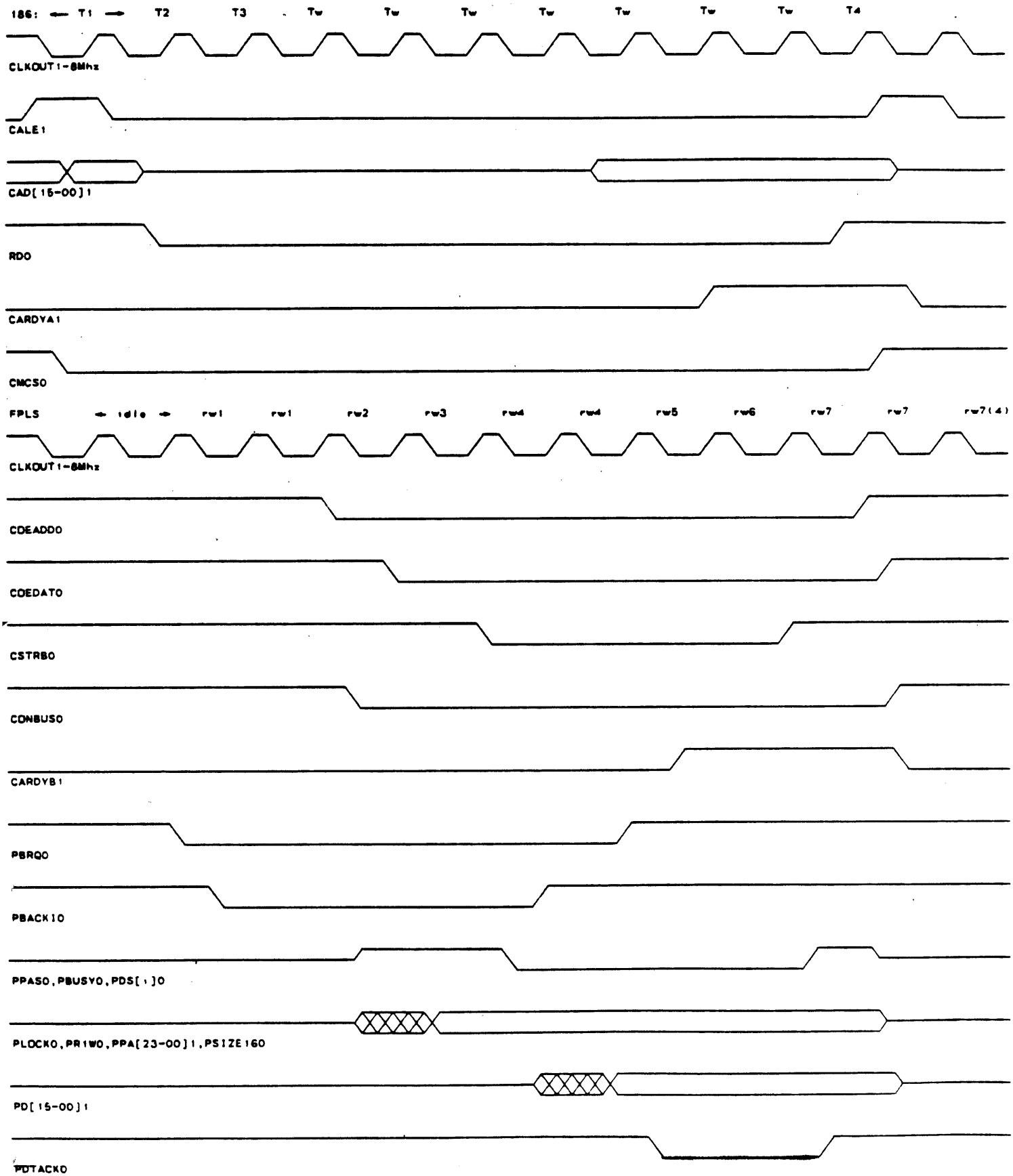
ISSUE	ENGR	TITLE	BELL TELEPHONE LABORATORIES INCORPORATED
^	PMW	CTD HARDWARE FPIC STATE	

ATTACHMENT 2-5

NOTE: Deglitching CIAKO overlapped with time for data (interrupt vector) to be valid on I/O Bus.

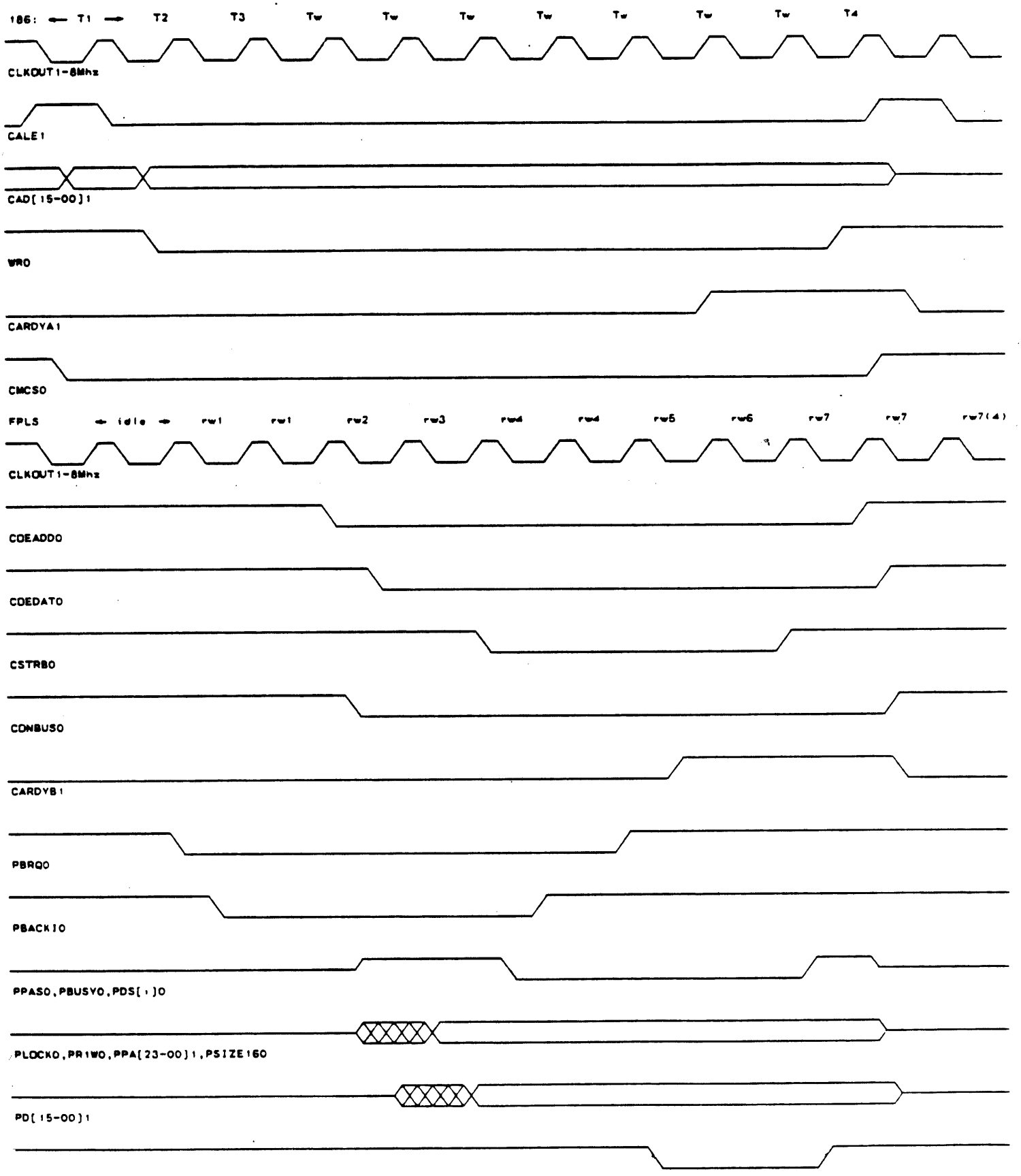
INPUTS	OUTPUTS	# STATES	# TRANSITIONS
1. CIAKO 2. CDSIXO	1. CDTACKO 2. CSRSET70 (PINTXO)	5	11

8 MHz

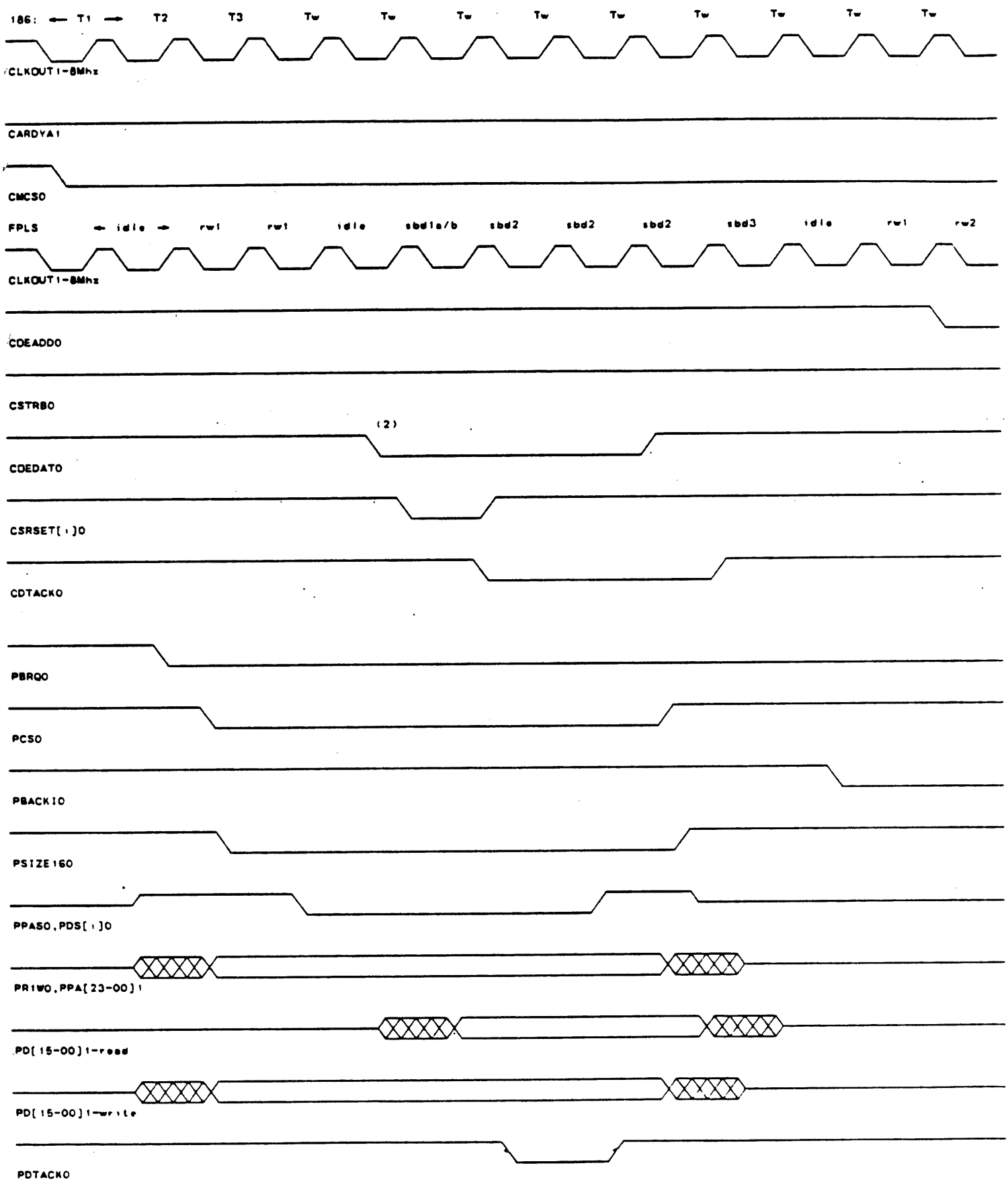


Notes:
1. Above timing diagrams assume I/O Bus is initially idle (i.e. PBRQ0 inactive).
2. PBRQ0 active to PBACK10 active will involve waiting in rw1 for at least 1 more cycle than shown.
3. PDTACK0 will typically go active later than shown, depending on performance of DPDRAM controller.
4. The FPLS will return to idle on the next rising edge of CLKOUT1.

Attachment 3-1: 80186 Read of System Board Memory



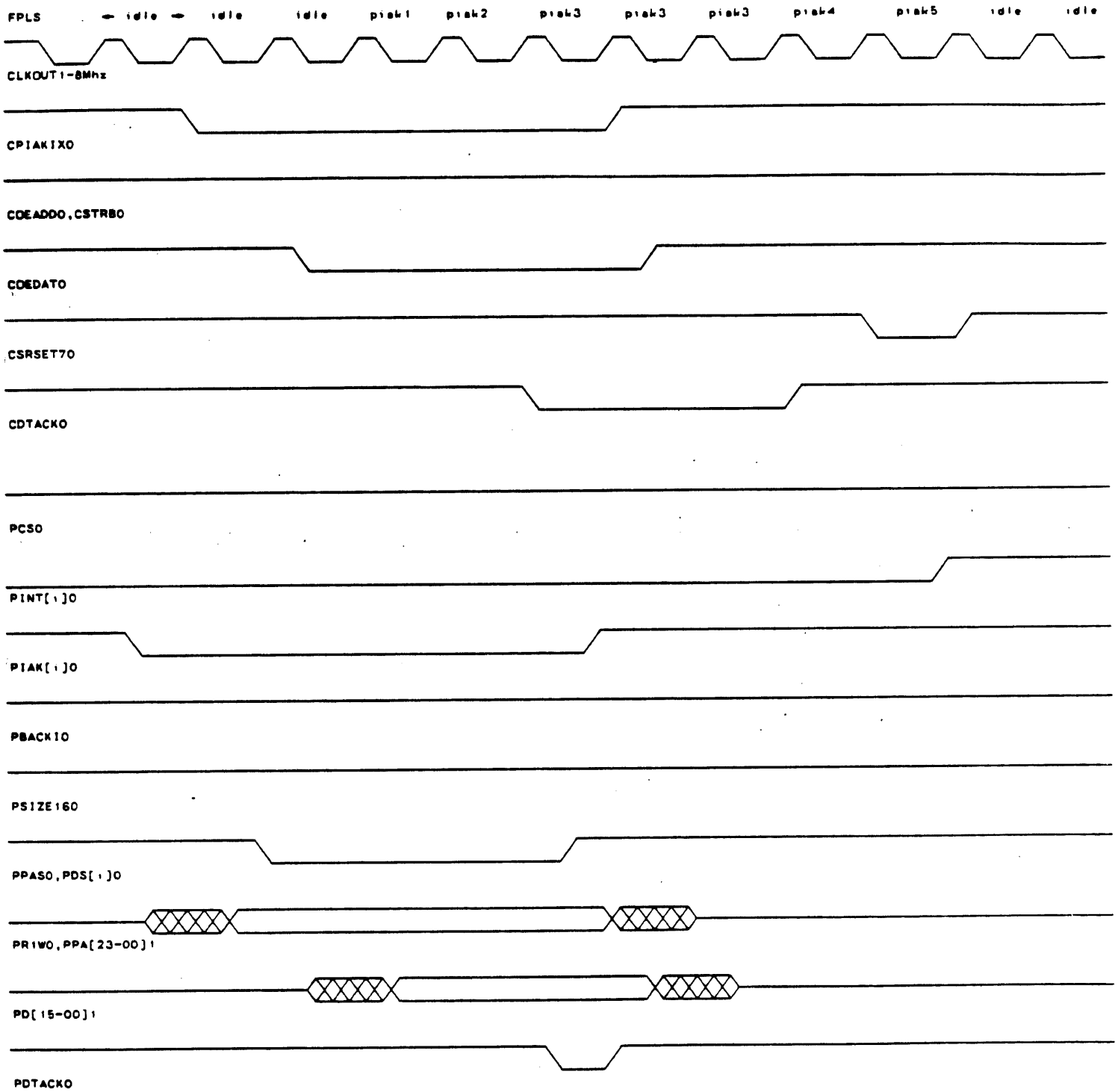
Notes:
1. Above timing diagrams assume I/O Bus is initially idle (i.e. PBRQ0 inactive).
2. PBRQ0 active to PBACK10 active will involve waiting in rw1 for at least 1 more cycle than shown.
3. PDTACK0 will typically go active later than shown, depending on performance of DPDRAM controller.
4. The FPLS will return to idle on the next rising edge of CLKOUT1.



Notes:
1. The above diagram illustrates a System Board access of a peripheral which has just started an access of System Board memory.
2. CDEDAT0 will go active (LOW) only on a read.

Attachment 3-3: System Board Read/Write of Peripheral

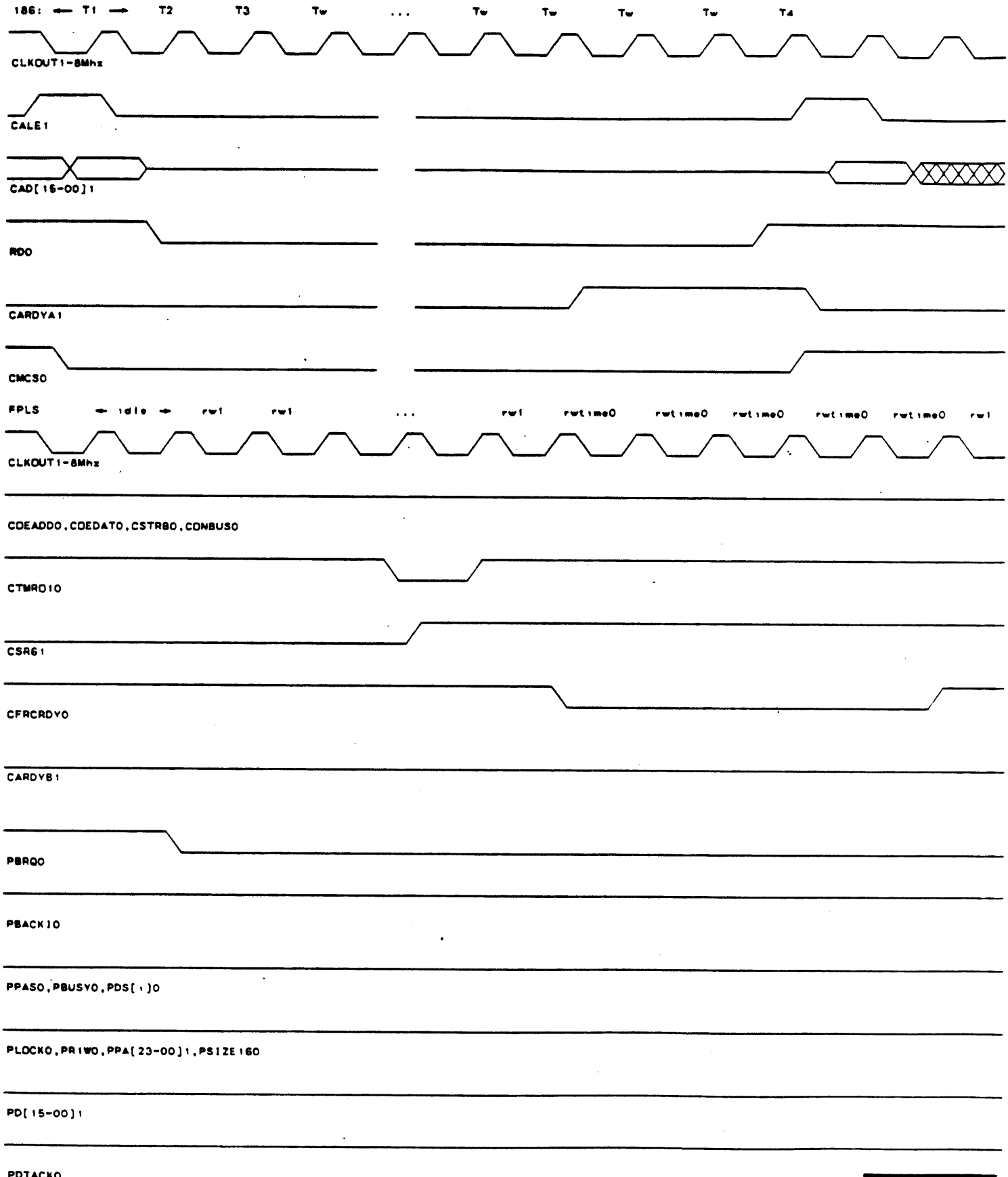
pmw



Notes:
1. PSIZE16O not asserted during PIAK cycle.
2. An interrupt acknowledge cycle is similar to a System Board read.

Attachment 3-4: Interrupt Acknowledge

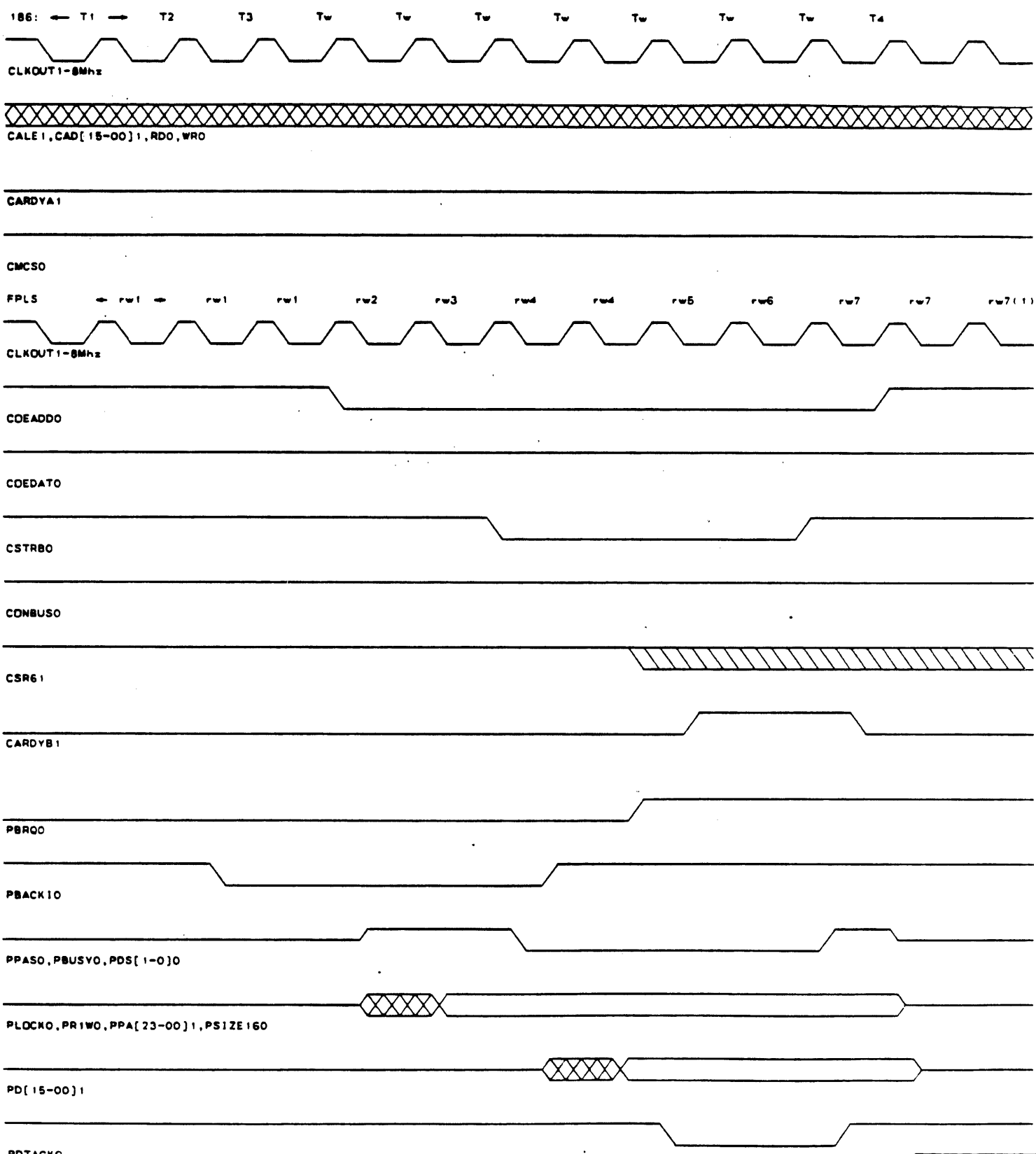
pmw



Notes:
1. Above timing diagrams illustrate an aborted 80186 read of System Board memory.

Attachment 3-5a: BAF (Forced ready)

pmw



Notes:
1. The FPLS will return to idle on the next rising edge of CLKOUT1.

Attachment 3-5b: BAF (dummy read)

3. 0 MYLIC. ALS CAN BE PLACED WITHIN CLO CHIPOUT.

1. Keep clocks (CLKOUT1, CLKOUT0 and CLKIN1) away from everything (i.e. less than 1 inch of any coupled length).

2. Keep set and reset inputs of LS279s (PCSR) away from everything

3. Keep CRESETI0, CRESETO1, IC22.3, IC36.1 (PR/OE of 82s105), CALE1, CIALE1, SYSRST0, CTMRO10 away from everything

4. Minimize potential crosstalk induced on synchronization register (LS374) and FPLS (82s105) inputs.

5. Minimize parallelism of I/O Bus nets with all other nets.

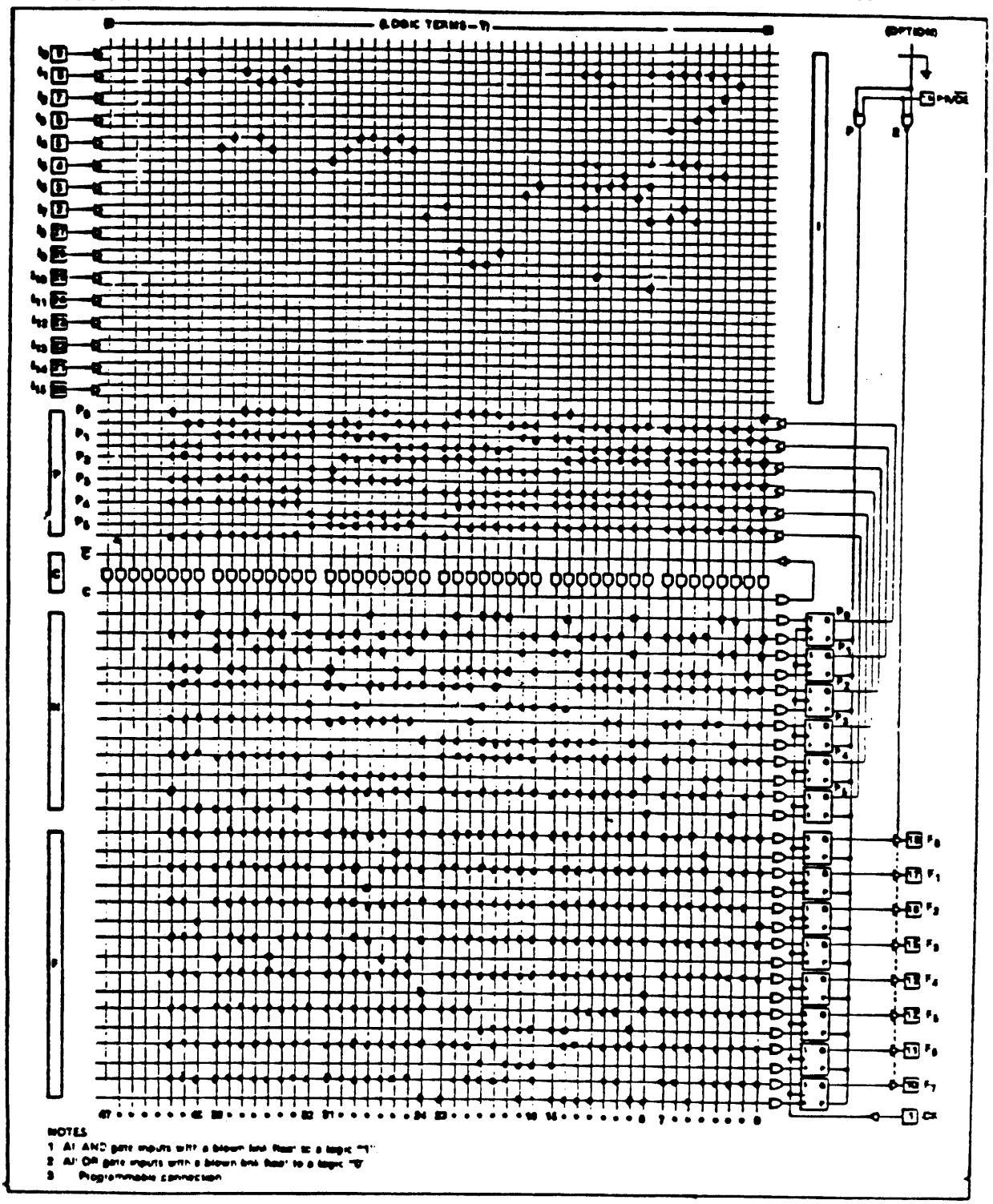
```
# File Name: fpls.lc
# Date:      10/25/83
# Purpose:   ASCII source file in Signetics format ready to be converted
             to Intel hex file (via "sigcvt") to allow DATAIO programming.
part=82s105
proe=p
#    c111111            PPPPPP NNNNNNFFFFFFFF
#    n54321098765432105432l0 54321076543210
0)   ----------------hhhhhh hhhhhlhhhhhlhh
1)   ----------------hhhhhl hhhhllhhhhhhhh
2)   --------------l-hhhhll lhlhhhhhhhhhhh
3)   ----------l--hh-hhhhll hlhhhhhhhhhhlh
4)   ----------l--lh-hhhhll hlhhllhhhhhhhl
5)   ---------l-h-h-h-hhhhll hhlhlllhhhhhhh
6)   ---------h-h---h-hhhhll hhhhllhhhhhhh
7)   ---------l-h-l-h-hhhhll hhhhllhhhhhhh
8)   ------l--lhh---h-hhlhll lllhllhhlhhhh
9)   ----------l------hhlhll hhlhhhlhlhhhh
10)  ----------hl-----hhlhll hhhhllhhhhhhh
11)  ----------h----l-hhlhll hhhhllhhhhhhh
12)  ------h---hh---h-hhlhll hhlhlllhhhhhh
13)  ---------hhh---h-hhlhll hhlhlilhhhhhh
14)  ----------------hhlhhh hhllhhlhlhhhh
15)  ----------------hhllhh hhllhllllhhhh
16)  ----------h------hhllhl hhllllhllhhhh
17)  ----------l------hhllhl hhllhllllhhhh
18)  ----------------hhllll hhlllhhllhhhh
19)  -------h--------hhllih hhlhlhhhlhhhh
20)  -------l--------hhllih hhllihhllhhhh
21)  -------l--------hhlhih hhhhllhhhhhhh
22)  -------h--------hhlhih hhlhlhhhhhhhh
23)  ---------h-------llhll hhlhlllhhhhhh
24)  ---------l-------llhll lllhlllhhlhhh
25)  ------------l----hlhhll hlhhhlhhhhlhh
26)  ------------h----hlhhll hlhhllhhhhhhl
27)  ------------l----hlhhhh hlhhhlhhhhlhh
28)  ------------h----hlhhhh hlhhhhhhhhhlh
29)  ------------h----hlhhhl hlhlhlhhhhhhh
30)  ------------l----hlhhhl hlhhhlhhhhlhh
31)  ----------h-----hlhlhl hhhhllhhhhhhh
32)  ----------l-----hlhlhl hlhlhlhhhhhhh
33)  ---------------l-lhlhhh lhhhhhhhhhhhh
34)  ---------------h-lhlhhh hhhhllhhhhhhh
35)  ------------l--l-lhhhhh lhhhhlhhhhlhh
36)  ------------h--l-lhhhhh lhhhhhhhhhhhh
37)  ---------------h-lhhhhh hhhhllhhhhhhh
38)  ------------h----lhhhhl lhhhllhhhhhhh
39)  ------------l----lhhhhl lhhhhlhhhhlhh
40)  ---------------h-lhhhll lhhhlhhhhhhlh
41)  ---------------l-lhhhll lhhhllhhhhhhh
42)  ----------------lhhhlh hhhhllhhhhhhh
43)  -lllllllllllllllllll lllllllllll
44)  -lllllllllllllllllll lllllllllll
45)  -lllllllllllllllllll lllllllllll
46)  -lllllllllllllllllll lllllllllll
47)  -lllllllllllllllllll lllllllllll
#
#              Attachment 6: CIO Hardware FPLS ASCII Source Code
```

FIELD PROGRAMMABLE LOGIC SEQUENCER (16 x 48 x 8)

82S104 (O.C.)/82S105 (T.S.)

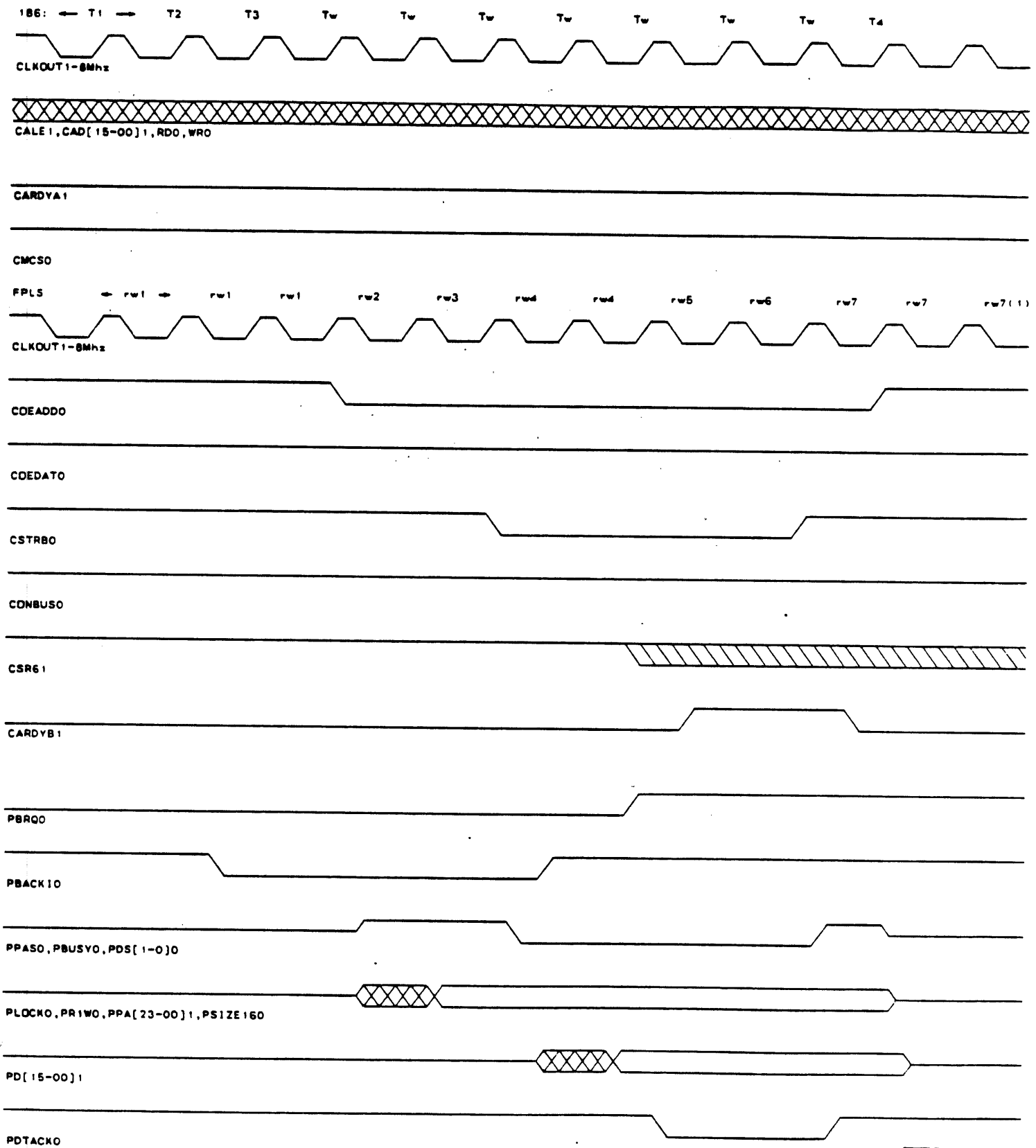
INTEGRATED FUSE LOGIC
SERIES 80

FPLS LOGIC DIAGRAM



C10 FPLS (ALD)

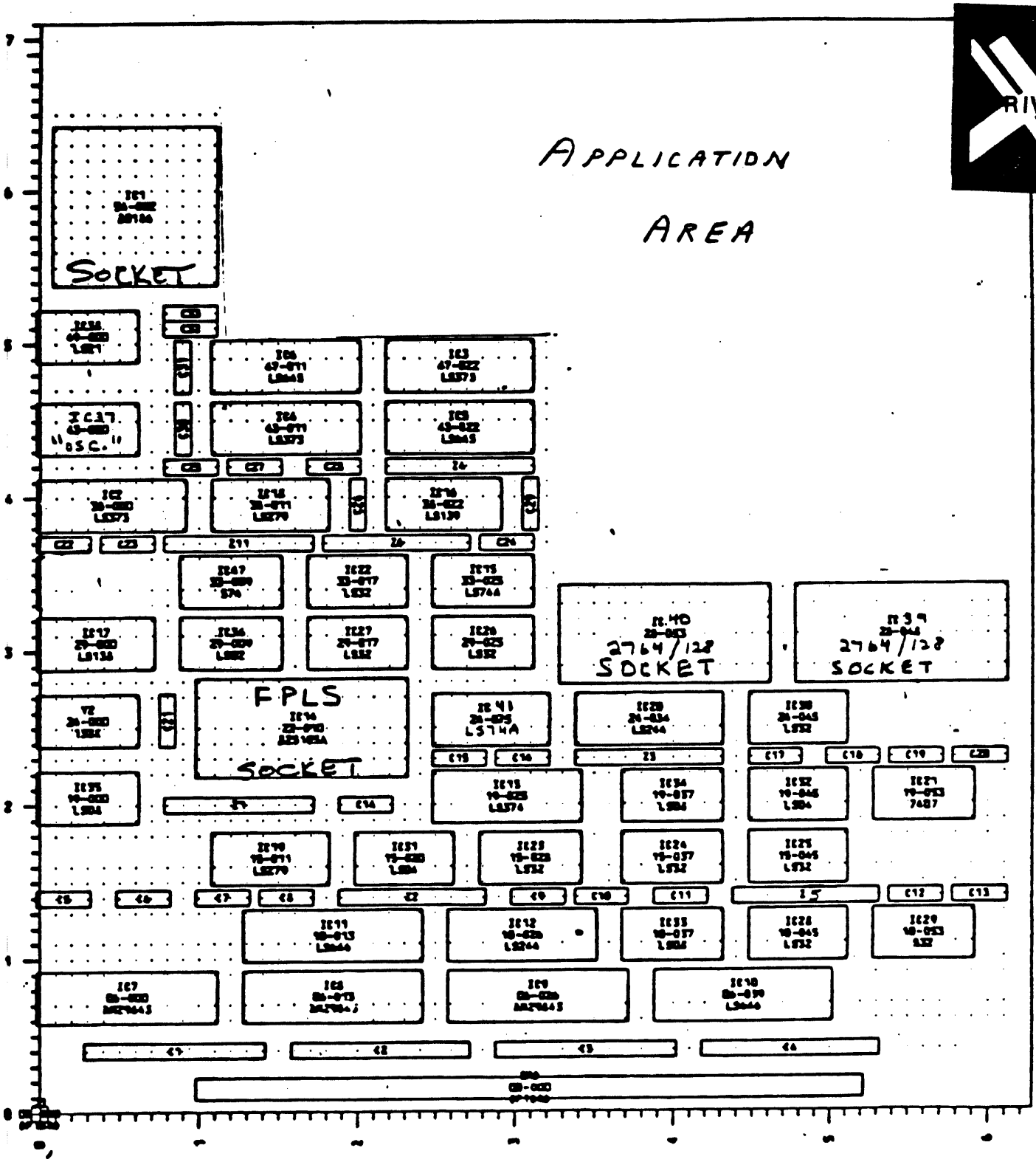
A.D.NIEMI 12/5



Notes:
1. The FPLS will return to idle on the next rising edge of CLKOUT1.

Attachment 3-5b: BAF (dummy read)

CIO HARDWARE TYPICAL LAYOUT - ISSUE 1



NOTES:

1. IC 2 (LS373), ALTHOUGH SHOWN HERE, NOT TYPICALLY NEEDED.
2. VCC DECOUPLING CAPACITORS (Cx) AND RESISTOR SIPS (Rx) INTERSPERSED THROUGHOUT LAYOUT.
3. 6 APPLIC. ICs CAN BE PLACED WITHIN CIO LAYOUT.

ATTACHMENT 5 - 3B™ 2 CIO LDI LD: AUDIT REVIEW GUIDELINES

An implementation of 3B 2 Common I/O (CIO) hardware has been developed (Issue 1, LDI LD, 12/28/83). These notes intend to assist 3B 2 peripheral designers which base their designs on this particular implementation in the way of providing guidelines for reviewing audits.

The audits in question are:

- Net length
- Crosstalk with RT1, RT2 = 2, 5 nsec. (no frequency)
- 2" Parallelism

Net Length:

For all nets, overlength should be less than 4 inches and total length less than 15 inches. (At 2.4 pf and .2 nsec per inch, 15 inches yields 36 pfs and 7.5 nsec. delay) For I/O Bus nets, overlength should be less than 1 inch and total length should be less than 6 inches. (Exceptions to this are PFAIL0, PCS0, PIAKIx0, PIAKOx0, PBACKI0, PBACKO0 and RQRST0 which can be a couple inches longer.) Note: TAP/TIME, which takes into account effects of net length, should be used to verify proper circuit timing.

Parallelism/Crosstalk:

All signals should be subject to a total of less than 300 millivolts of noise. For a voltage swing of 3 volts within 2 nsec. (RT1), (from logic LOW to logic HIGH say), 10% or less of crosstalk is required.

3 volt x 10% = 300 mvolt.

For each net, crosstalk audits list the contributors of noise due to adjacent leads and the percent of crosstalk potentially induced by each. In addition, a total sum (coherent addition) of the crosstalk of all these contributors and a statistical average (incoherent addition) of these contributors is given. If the number of contributors is small (less than 5), the total sum should be used and in which case should be less than 10%. If the number of contributors is large (greater than 10), the statistical average can be used and in which case should be less than 5%. Finally, no one single contributor should be greater than 5% and no I/O Bus net should be subject to a total sum greater than 5%.

For those totals exceeding 10% (5%), determine if the adjacent signals switch simultaneously (e.g. data bus bits). If so, no rerouting is required, assuming that a settling time of a few nanoseconds is provided. If, however, signals can potentially switch while an adjacent line is passive (e.g. a control lead or clock signal coupled with bus bits), rerouting is required.

Routing concerns specific to LDI issue LD of CIO, in decreasing order of priority, are: