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ABSTRACT

The 3B* 2 I/O Bus is an asynchronous, nonmultiplexed bus providing a simple and flexible interface for the family of the 3B 2 peripherals. It supports direct addressability up to 16 megabytes through 24-bit addresses and 8 and 16-bit data transfers. There are three priority interrupt levels and a single level of "distributed" bus arbitration. Along with having fault detection and control, the I/O Bus also supports two special transfer cycles: interlocked ready-modify-write and multiple access. A peripheral can access main memory at a rate up to two million bytes per second.

This document presents the requirements and specifications of the 3B 2 I/O Bus, allowing the design of 3B 2-compatible peripherals. Functional, electrical, and mechanical characteristics have been included.

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subject: 3B™ 2 I/O Bus: Requirements Re-release

date: December 30, 1983

from: P. M. Walsh
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This is a re-release of the document "3B2 Component Requirements and Specifications: I/O Bus", dated March 7, 1983. The major areas of change from the first release involve:

- Width of ID/Vector Register changed from 8 bits to 8 or 16 bits, depending on peripheral width.
- Autoconfiguration section updated to mention System Board assigns interrupt vectors after a reset.
- Mechanical Specifications section updated to specify two widths of I/O boards.
- Bus arbitration scheme modified and several new spec.s and figures (Figures 11a, b and c) added.
- Interrupt acknowledge scheme modified.
- Performance Objectives section added:
  1. Bus bandwidth and efficiency requirements set.
  2. Critical events of each cycle discussed.
  3. Effects of new bus arbitration scheme on performance discussed.
- Interrupt levels assigned:
  1. PINT[2]0 now reserved,
  2. PINT[1]0 explicitly slotted for high bandwidth peripherals and
  3. PINT[0]0 explicitly slotted for low bandwidth peripherals.
- Figures organized and renumbered

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- Several timing spec.s changed (e.g. bus skew increased from 30 to 40 nsec).
- Multiple access limit changed from 1024 to 64 max transfers and at most 125 usec. on bus.
- Added figures for reset timing (Figure 10) and CM195 I/O boards (Figures 16a, 16b and 16c)
- Reference to sanity failure on System Board removed.
- Discussion of IEEE 796 peripherals removed.
- Peripherals limited to 2 inputs and 1 output as opposed to 2 inputs and 2 outputs.
- Figure 12 (was Figure 13) redone based on changes in bus loading.
- Iol of all open collector nets now must meet max of 40 mA. (This change also reflected in new Figure 13.)
- System Board allowed 4 I/O loads on PD bus.
- Specify hold time on address and data as 10 (50) nsec at slave (master).
- Allow 3 input loads on PBACKI0 and PIAKIx0 and use Schottky driver for both. (Previously only PBACK0 required Schottky.)
- Change spec on deassertion of PBUSY0.

P. M. Walsh

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subject: 3B™ 2 Component Requirements and Specifications: I/O Bus

date: December 21, 1983

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Internal Memorandum (IM)

1. INTRODUCTION

Figure 1 presents a block diagram of the 3B 2 System Board. As shown, it contains a dual ported main memory; the microbus is tied to one port while the asynchronous I/O Bus is tied to the other. The microbus provides a communication path between the System Board CPU (WE*-32000) and several on-board components including main memory. On the I/O Bus side, a variable number of optional peripherals attach.[1] This document serves as the requirements and specifications of the I/O Bus.

Section 2 of this document presents a brief overview of the I/O Bus followed by a discussion of the two types of peripherals. A functional description of the I/O Bus is presented in section 3 and includes such issues as data transfers, bus exchanges, interrupts and error handling. Electrical and mechanical requirements follow in sections 4 and 5 while a discussion of performance is presented in section 6. A summary completes the document.

2. I/O ARCHITECTURE

2.1 I/O Bus Overview

The I/O Bus, which has a 16-bit data path and a 24-bit address, is designed to meet the requirements of a wide range of system configurations. Both eight and sixteen bit peripherals are supported as well as single and multiple data transfers per cycle. Various other types of operations are also possible. Although any peripheral can be a master or slave (or both), they are only

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1. A DMA subsystem, which resides on the System Board, also attaches to the I/O Bus.

allowed to access the System Board's main memory; a peripheral responds to chip selects generated on the System Board as opposed to decoding addresses.

2.2 Peripheral Types

There are two classes of 3b2-native peripherals: programmed and intelligent.[1] [2]. Any peripheral can be 8 or 16 bits wide and occupy either 1 or 2 slots in the I/O Bus backplane. While the I/O Bus does not inherently support any industry standard bus (e.g. IEEE 796 Bus), a forthcoming Commercial Bus Adapter (CBA) can be used to interface commercially available peripherals to the 3B 2.

2.2.1 *Programmed Peripherals*

Programmed peripherals are generally slave devices, responding to instructions generated by the System Board CPU. Such I/O boards have the capability of interrupting the CPU and/or becoming bus masters to access main memory (only after being "programmed" by the CPU).

A major difference between programmed peripherals and intelligent peripherals (discussed next) concerns their respective interfaces to the System Board CPU. The CPU, for example, can at times touch a programmed peripheral's internal components (i.e. a passive access). Conversely, communication between the CPU and intelligent peripherals is primarily achieved through queues in main memory.

Those programmed peripherals which can be a bus master are also responsible for preventing a deadlock resulting from the CPU attempting a passive access while the particular peripheral attempts to use the I/O Bus. (Such peripheral designs can take advantage of the fact that the peripheral can only use the I/O Bus to access main memory.)

Finally, *both* programmed and intelligent peripherals shall contain a read-only ID register defining the particular I/O board's type, size (occupying either 1 or 2 physical slots), access requirements, etc. and will be located at the same relative address on all peripherals.

• A simple telephone controller (with auto dial and a modem interface) is an example of a programmed peripheral. The System Board CPU would send it instructions such as specifying synchronous or asynchronous mode, baud, number of bits per character, etc. In addition, the peripheral would wait to be polled or use interrupts to interface with the System Board CPU. At any rate, an on-board microprocessor is not necessary.

2.2.2 *Intelligent Peripherals*

Each intelligent peripheral contains a local CPU, capable of executing locally based firmware. Communication with the System Board CPU is achieved via a unique pair of one-way queues located in main memory. (The System Board CPU loads messages for a given peripheral in a designated *request* queue while the peripheral returns messages via the corresponding *completion* queue.[2] "Attention" interrupts are used to bring a nonempty queue to the attention of the other CPU. Finally, intelligent peripherals may autonomously interact with the System Board CPU but may not directly interact with each other. (Using queues make it no longer necessary for the CPU to reach into a peripheral over the I/O Bus. Consequently, there is never a possibility for a passive access

be accessed. PPA[00]1 is the least significant bit while PPA[23-22]1 are reserved for future expansion. (Table 1 in the "Peripheral Data Path to Main Memory" section illustrates the use of the least significant address bits and data strobes.)

Data lines.

PD[15-00]1: Peripheral Data (tri-state)
These 16 bidirectional lines transmit and receive information to or from the established master and slave. PD[15]1 is the most significant bit and only lines PD[07-00] (byte 1 on I/O Bus) are valid for 8-bit peripherals.

Control lines.

PBUSY0: Peripheral Busy (tri-state)
This unidirectional signal is activated by the peripheral after receipt of bus acknowledge (PBACKI0) and held active during the entire bus cycle. The purpose of PBUSY0 is to facilitate multiple accesses by the same bus master without relinquishing control of the bus between data transfers. For example, up to 64 data transfers[2] between a peripheral and main memory may occur during 1 bus cycle[3]; PBUSY0 is held active for entire cycle.

PCS[15-01]0: Peripheral Chip Selects (totem-pole)
PCS0:

These 15 lines originate from the System Board and are fanned out to 15 unique chip selects, one for each of the 12 3B 2/400 peripheral connectors and the remaining 3 for future enhancements (e.g. accommodate a Commercial Bus Adapter, CBA). (As indicated in Table 7, each peripheral refers to its Peripheral Chip Select as PCS0.) One of these mutually exclusive lines (i.e. no broadcast addressing mode) is active when the CPU references a peripheral. Although a given PCS[i]0 is generated by the System Board's address decoder, the main memory controller/arbiter dictates its propagating onto the I/O Bus. thereby causing the appropriate PCS[i]0 (PCS0) to be activated

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2. The System Board CPU accesses main memory through its own port on the microbus side.

3. Read, write and interlock operations may be combined within the same bus cycle.

4. As discussed in the "Error Detection and Handling" section, a time limit exists on the length of an individual data transfer as well as on the entire bus cycle.

along with PPA[23-00]1, PR1W0 and PLOCK0.

PDS[1-0]0: Peripheral Data Strobes (tri-state)
These 2 bidirectional lines allow the bus master to select which bytes of the 16-bit PD bus are to be valid during the transaction; PDS[1]0 is associated with I/O Bus byte 1, PDS[0]0 is associated with byte 0. A negative transition is applied by the bus master to indicate valid write data or to cause the slave to gate read data onto the I/O Bus.

PDTACK0: Peripheral Data Acknowledge (open-collector)
Peripheral data acknowledge, a bidirectional signal, is activated by the slave to indicate receipt of valid write data or to indicate valid read data on the PD bus.

PLOCK0: Peripheral Memory Lock (tri-state)
PLOCK0 is a unidirectional signal that the bus master uses to indicate an interlock (read/modify/write) cycle. Interlocks over the I/O Bus may be established in only one direction: peripheral to main memory.

PPAS0: Peripheral Physical Address Strobe (tri-state)
This line (bidirectional, generated by master) indicates a valid physical address on the address bus. The timing requirements of several other I/O Bus signals, in addition to PPA[23-00]1, are defined in relation to PPAS0.

PR1W0: Peripheral Read-Write Signal (tri-state)
This line (bidirectional, generated by master) indicates whether a read (HIGH) or write (LOW) transfer is in progress and is recognized as valid on the activation of PPAS0.

PSIZE160: Peripheral Size (open-collector)
This signal specifies a particular peripheral's bus interface as either 8 (HIGH) or 16 (LOW) bits wide and as such is routed to the byte rotate unit on the System Board. As a 16-bit bus master, a peripheral generates PSIZE160 immediately after obtaining the bus (i.e. on receipt of PBACK10). Conversely, as a slave the peripheral will return PSIZE160 on chip select (PCS0). An 8-bit peripheral need not drive PSIZE160 inactive (HIGH) since this signal is open-collector and pulled HIGH.

RQRST0: Request System Reset (open-collector)
This line, originating from each peripheral and routed to the CPU, allows a peripheral to reset the entire system. Although the use of this capability will be necessarily limited, a typical application would be the resetting of a remote node on a computer network. (Refer to Figure 10.)

SYSRST0: System Reset (totem-pole)
System reset is activated on system power up, by a manual reset switch, via software setting the "System Reset Request" bit in

the Control and Status Register (CSR) [3], or indirectly by other devices (via RQRST0). When activated, all peripherals initialize. (Refer to Figure 10.)

Bus exchange lines.

PBRQ0: Peripheral Bus Request (open-collector)
PBRQ0 is shared by all peripherals to request I/O Bus usage on route to accessing main memory. The arbiter (on the System Board) will grant the bus to a peripheral with the bus acknowledge signal. (As discussed next, the bus acknowledge signal is daisy-chained through all peripherals.) Once bus master, a peripheral must remove PBRQ0 in "sufficient" time before the end of a cycle to ensure that the arbiter doesn't rearbitrate and possibly reassert PBACK0. Conversely, a peripheral may keep PBRQ0 active after the current *transfer* has ended to request another bus access. (See "Multiple Bus Access" section.)

PBACK0: Peripheral Bus Acknowledge (totem-pole)
PBACKI0:
PBACKO0:

The arbiter on the System Board generates PBACK0 to indicate that a peripheral may gain access to the I/O Bus and removes it when it detects the acknowledged peripheral's assertion of PBUSY0. It is daisy-chained among all peripherals and thus the priority of a given device, which is *actively* waiting for bus access, is determined by its physical position in the chain. (Refer to the "Bus Exchange" section for a further explanation of I/O Bus arbitration.) The bus acknowledge signal entering a given peripheral is referred to as PBACKI0 while the corresponding exiting signal is PBACKO0. Note: care must be taken to ensure an unbroken chain from the System Board to the last peripheral; every peripheral which does not use the bus request signal will tie its PBACKI0 and PBACKO0 signals together and no two peripherals may be separated by an empty I/O slot.

Interrupt lines.

PINT[2-0]0: Peripheral Interrupt Requests (open-collector)
PINT[2-0]0, shared by all devices on the I/O Bus, provide three dedicated system interrupt levels; PINT[2]0 is reserved and PINT[1]0 is the higher priority of the remaining two. A peripheral can use at most one of these two remaining levels. PIAK[2-0]0 are the corresponding acknowledges.

PIAK[2-0]0: Peripheral Interrupt Acknowledges (totem-pole)
PIAKI[2-0]0:
PIAKO[2-0]0:

As a result of PINT[i]0 being activated, the CPU will eventually acknowledge this specific level with PIAK[i]0. Since all

peripherals share the same three interrupt levels, the corresponding acknowledgements are daisy-chained among them. PIAKI[2-0]0 refers to the *input* acknowledgement signals while PIAKO[2-0]0 refers to the *outputs* of the chain. When a device that has requested an interrupt receives the particular PIAKI[i]0, it prevents the acknowledge from propagating any further down the chain (i.e. PIAKO[i]0 held inactive). Conversely, a noninterrupting device passes PIAKI[0] on to the next device in the chain. Finally, the System Board will remove PIAK[i]0 on receipt of the interrupting devices assertion of PDTACK0.

Error Reporting lines.

PFAIL0: Peripheral Board Fail (open-collector)
PFAIL0, shared by all peripherals, is asserted by a peripheral upon board failure such as sanity fail.

PFLT0: Peripheral Bus Fault (open-collector)
A bidirectional line, PFLT0, is asserted by the slave on detection of an erroneous operation such as parity error or bus timeout (as in case when the System Board is the slave). A peripheral must end the cycle on PFLT0 (as with PDTACK0); PFLT0 has the same timing specifications as PDTACK0.

Power and Ground.

VCC:	+5 volt power	- 1 "layer" of multilayer backplane
V12P:	+12 volt power	- 1 line
V12N:	-12 volt power	- 1 line
GRD:	system ground	- 1 "layer" of multilayer backplane
VBKUP:	+3.0 volt battery	- 1 line

During periods of no AC power, VBKUP affords 3.0 volts (at most 10 ua) to each peripheral for at least 30 days and will have a lifetime of at least 5 years.[3] During normal operation, VBKUP sustains 5 volts.

3.2 Peripheral Data Path to Main Memory

A peripheral can be 8 or 16 bits wide while main memory is 32 bits wide. Five signals combine to select which byte(s) of a 4-byte main memory word are to be accessed. Since the I/O Bus has a 16-bit data bus, a maximum of two data bytes can be transferred in a single transaction. The following discussion refers to Tables 1 and 2.

Sixteen bit peripherals drive PSIZE160 LOW and use the data strobes to indicate which byte(s) of data it is interested in. Address bit PPA[01]1 controls whether the I/O Bus is tied to main memory bytes 0 and 1 or to bytes 2 and 3. PPA[00]1 is ignored by the memory controller. Note: Table 1 implies that for the case where just one data strobes is active, only one byte is returned from

TABLE 1. Significance of Data Strobes

PSIZE160	address bits PPA[01]1	PPA[00]1	data strobes PDS[0]0	PDS[1]0	valid bytes memory	I/O
16-bit						
0	0	x	0	0	0,1	0,1
0	0	x	0	1	0	0
0	0	x	1	0	1	1
0	0	x	1	1	illegal	-
0	1	x	0	0	2,3	0,1
0	1	x	0	1	2	0
0	1	x	1	0	3	1
0	1	x	1	1	illegal	-
8-bit						
1	0	0	x	0	0	1
1	0	1	x	0	1	1
1	1	0	x	0	2	1
1	1	1	x	0	3	1
1	x	x	x	1	illegal	-

Notes:
x = don't care

TABLE 2. Relationship of Bytes and Bits

Byte		Bits
Main Memory	0	31-24
	1	23-16
	2	15-8
	3	7-0
I/O Bus	0	15-8
	1	7-0

Notes:
Bit 0 is the least significant bit.

main memory on a read. The memory controller, however, will always return a 16-bit halfword over the I/O Bus, but only check parity on the appropriate byte. Finally, not asserting either of the data strobes will result in a bus timeout failure.

Eight bit peripherals are tied to byte 1 (bits 7-0) of the I/O Bus and do NOT drive PSIZE160.* Address bits PPA[01-00]1 select the byte while the 1 data

strobe, PDS[1]0, is needed for protocol timing purposes. (PDS[0]0 is ignored by the memory controller.) Although the use of PPA[00]1 and PDS[1]0 is redundant, performance is improved; PPA[00]1 is available at the slave (memory controller) before PDS[1]0, allowing it to address main memory that much earlier in the cycle. Not asserting PDS[1]0 will yield a bus timeout failure.

3.3 Data Transfer Operations

For the discussions that follow, several timing diagrams are referenced. In all cases, each is presented from the perspective of the *slave* device. As an example, the timing for a read of main memory by a peripheral is seen at the System Board Connector (the connector which mates the backplane to the System Board, also referred to as the I/O Expansion connector.) The notation used in these timing diagrams is:

minimum time in nanoseconds / maximum time in nanoseconds.

Peripheral Read of Main Memory (Figure 3)

A read of main memory (slave) by a peripheral begins with its request of the I/O Bus (PBRQ0). On receipt of bus acknowledge (PBACK0), the peripheral (now master) asserts the bus busy signal (PBUSY0) causing the arbiter to remove PBACK0. The peripheral starts the data transfer by gating the physical address, read/write (HIGH for read), peripheral size and interlock (inactive) signals onto the bus. Once these lines are stable, the physical address strobe (PPAS0) and data strobes (PDS[1-0]0) follow.[6] PBRQ0 shall be removed after the data transfer operation has started (i.e. after PPAS0 has been asserted and PBACK0 has been removed).

Activation of the data strobes precipitates the slaves (main memory controller, in this case) gating of data onto the bus. When the data is stable, the slave asserts data transfer acknowledge (PDTACK0), allowing the peripheral to latch the data. The peripheral will subsequently drive HIGH the address and data strobes and the busy signal before tri-stating all signals it had been driving. The main memory controller will remove PDTACK0 and the data on removal of the data strobes.

Peripheral Write to Main Memory (Figure 4)

The bus request/grant syndrome is identical to that for the above read protocol. After PBACK0 and PBUSY0, the physical address, read/write (LOW), peripheral size and interlock (inactive) signals are gated onto the bus followed by PPAS0 after the required set up time. Also after PBACK0 has been received, the peripheral

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5. PSIZE16 is open-collector and pulled HIGH; an 8-bit peripheral, therefore, never need drive PSIZE16.

6. PBUSY0 can be asserted as late as when PPAS0 and PDS[1-0]0 are asserted.

gates the write data onto the bus.

After the data is stable, the peripheral asserts the appropriate combination of data strobes to indicate the valid byte(s) of data on the bus. In turn, the main memory controller "accepts" the data and activates PDTACK0. This causes the master (peripheral) to drive PBUSY0, PPAS0 and PDS[1-0]0 HIGH before tri-stating these along with the address, data and status signals. PDS[1-0]0 going HIGH causes the slave to remove PDTACK0. (Data can optionally be latched on the falling or rising edge of PDS[1-0]0,)

CPU Read/Write of a Peripheral (*Figures 5 and 6*)

These operations are very similar to those when a peripheral was bus master. The differences are:

1. The CPU's arbitration for the bus is not evident on the I/O Bus (no flopping of PBRQ0/PBACK0).

2. One of fifteen Peripheral Chip Selects (PCS[15-1]0 => PCS0) becomes active (identifying *one* peripheral) along with the address, read/write and interlock signals.

3. The CPU doesn't drive PBUSY0.

4. The addressed peripheral returns PSIZE160 on receipt of PCS0 (as opposed to generating PSIZE160 along with the address, etc. as when it was bus master).

As before, PR1W0 differentiates between a read and write operation.

Peripheral Interlock with Main Memory (*Figure 7*)

An interlock operation is the uninterruptible sequence of a read of main memory by a peripheral, modify the data read and then write it back to the same location in main memory - all within a single bus cycle. Such operations are generally used in the implementation of semaphores.

The protocol for an interlock operation is that of a read followed by a write with one exception; the PLOCK0 signal, which has the same timing specifications as PPA[23-00]1, PR1W0 and PSIZE160, is active for both the read and write. Although the same address is used for both operations, it must be valid for both the read and the write. (As a side note, an interlock operation can be easily simulated within a multiple bus access cycle if desired. Refer to the "Multiple Bus Accesses" section.)

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7. The CPU can not establish an interlock with a peripheral or vice versa.

3.4 Bus Exchange

The main memory on the System Board is dual ported; the System Board CPU (WE-32000) is tied to one port while the I/O Bus[8] is tied to the other[3]. (Refer to Figures 1 and 2.) An arbitration circuit, also on the System Board, controls accesses to main memory and is responsible for periodically refreshing main memory. In addition, since an I/O device can only access memory, the arbiter also controls I/O Bus mastership.

Any peripheral may become I/O Bus master and therefore has access to the Peripheral Bus Request (PBRQ0) and Peripheral Bus Acknowledge (PBACK0) signals. A peripheral publicly requests the bus with PBRQ0, an open-collector signal that is shared by all peripherals. The arbiter grants the bus by asserting PBACK0, which is daisy chained through all peripherals; a peripheral refers to its *input* acknowledge signal as PBACKI0 and its *output* as PBACKO0. While bus master, it must not allow PBACKO0 propagate to the next device in the chain. Furthermore, a peripheral may not glitch PBACKO0 or preempt another's bus mastership. Finally, for the case when a peripheral is not waiting for PBACK0, the latency from PBACKI0 to PBACKO0 should be kept under 9 nanoseconds; one Schottky gate delay (e.g. SN74S32) plus time of flight through two connector pins and on board wiring. (See Figure 14.)

Traditional daisy-chain circuitry allows an I/O device assert PBRQ0 at will. Given an asynchronous bus (such as the 3B 2 I/O Bus) each peripheral would drive PBRQ0 active regardless of the state of any other peripheral. Consequently, PBACKI0 and PBRQ0 of a peripheral are asynchronous events.

Conceivably PBACKI0 and PBRQ0 could be synchronized on each peripheral, thereby preventing glitches and the like from occurring when these two signals were to occur at or nearly the same time. This scheme, however, increases the latency from PBRQ0 to PBACKI0 (since PBACKI0 to PBACKO0 is delayed at each peripheral), which can be significant for peripherals near the end of the daisy-chain.

The philosophy of 3B 2 I/O Bus arbitration[9] deviates from this approach. In particular, a peripheral may not drive PBRQ0 *if PBRQ0 is currently active.* Instead, the peripheral must hold off until it sees PBRQ0 go inactive, delay momentarily (minimum of 130 nanoseconds) and then drive PBRQ0. (This delay guarantees a window large enough for all peripherals to see the inactive PBRQ0.) Once a peripheral which has been waiting to drive PBRQ0 sees PBRQ0 go inactive, it is committed to go ahead and drive PBRQ0 after the forementioned delay. Refer to Figure 11c.

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8. A DMA subsystem, located on the System Board, shares one port with the I/O Bus peripherals.

9. Patent pending.

Given the independence of the peripherals, each will sample and hence drive PBRQ0 at different times - all within a finite amount of time. The arbiter, consequently, must guarantee a delay from PBRQ0 going active to sending out PBACK0. This delay allows all interested peripherals enough time to sample and subsequently assert PBRQ0 before PBACKI0 can go active. As illustrated by Figure 11c, the time from PBRQ0 going active to the time the arbiter asserts PBACK0 is at least 185 nanoseconds. (A peripheral, therefore, has 185 nanoseconds to block PBACKI0 from propagating to PBACKO0, assuming it wishes to use the bus.)

Note that this delay is needed from PBRQ0 *going* active. PBRQ0, therefore, is delayed on the System Board before it enters the arbiter such that the arbiter doesn't "see" PBRQ0 until 1 cycle later. Obviously, then, PBACK0 will come out 1 cycle later as far as peripherals are concerned. Moreover, this delay is inserted only within the first transfer of each cluster[10] since PBRQ0 remains active throughout. Finally, delaying PBRQ0 into the arbiter effectively increases bandwidth to main memory for non I/O Bus devices (e.g. the WE-32000).

By requiring each I/O Bus device to be a "good citizen", priority is distributed over the entire bus. Within each cluster, for instance, no other peripherals can attempt to use the bus. Furthermore, once a peripheral within the given cluster finishes its cycle, it likewise may not attempt to use the bus until all other devices in the cluster have had a turn on the bus. Figure 11a presents one realization of the PBRQ0/PBACK0 daisy-chain logic followed by timing diagrams in Figures 11b and 11c.

Note: the circuit in Figure 11a uses an 8 MHz clock to meet the I/O Bus requirement "delay for a minimum of 130 nanoseconds before driving PBRQ0." Other realizations are possible. If only a slower clock were available, for example, this circuit would have to be slightly modified to guarantee the peripheral would see PBRQ0 inactive before another device could drive it active again. One straightforward alteration would have the rising edge of PBRQ0 clocking "myreq0" which would then immediately block PBACKO0. The cascaded flip flops in Figure 11a would then provide the required delay of PBRQ0 assertion.

The following protocol shall be observed:

1. A peripheral will watch for PBRQ0 to go inactive, delay momentarily, assert PBRQ0 and then wait for PBACKI0.

2. The arbiter will eventually send out PBACK0, allowing the I/O device physically closest to the CPU and with its PBRQ0 active to obtain the bus.

3. The bus master will start its bus cycle as mentioned previously: PBUSY0, PPA[23-00]1, etc. followed by PPAS0.

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10. Once PBRQ0 goes inactive, a group or cluster of peripherals will drive PBRQ0 active and wait in line for PBACK0.

4. The arbiter will remove PBACK0 on receipt of PBUSY0, with PBRQ0 still active. PBRQ0 shall be removed after PBACK0 has been removed and after PPAS0 has been asserted. (Containing PBACK0 within PBRQ0 allows a peripheral to use PBRQ0 to block PBACK0 from propagating.)

5. By the end of the cycle, the peripheral should have removed PBUSY0, allowing the arbiter to grant the next bus mastership.

The arbiter times each data transfer by measuring the width of each active PPAS0. Peripheral Bus Fault (PFLT0) is generated[11] if this time exceeds that specified in [3]. (The current value of this time is approximately 5 microseconds.)

3.5 Multiple Bus Accesses

More than one data transfer (bus access) by the same peripheral can be accomplished in one bus cycle. Such multiple accesses occur without bus arbitration overhead and are thus performance effective. (The System Board CPU is not capable of multiple accesses over the I/O Bus.)

The bus busy signal (PBUSY0) affords the multiple access feature (Figure 8). In particular, a cycle starts as a "normal" bus cycle; bus request, wait for acknowledge and then activate PBUSY0. At this point, the bus master has effectively locked out all devices from using the I/O Bus and may therefore perform several uninterrupted data transfers.[12]

The lengths of the entire bus cycle and each separate data transfer shall be constrained to limit bus occupancy and prevent bus timeout failures, respectively. Specifically there may be at most 64 transfers within a multiple access cycle and the total time on the bus must not exceed 125 microseconds.[13] (Refer to the "Performance Objectives" and "Error Detection and Handling" sections.)

3.6 Interrupt Operations

Each peripheral has the opportunity to interrupt the System Board CPU. Intelligent peripherals, for example, use interrupts to bring a nonempty *completion* queue to the attention of the System Board CPU. Three Peripheral INTerrupt request lines (PINT[2-0]0) exist in the I/O Bus, thereby dedicating

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11. PFLT0 is also generated on a parity error.

12. Transparent to the current bus master, the arbiter may *temporarily* suspend the bus cycle to force a main memory refresh. Such a preemption can only occur on an access boundary.

13. Although each transfer is expected to be on the order of 1 microsecond, the ultimate limit of a multiple access cycle is 125 microseconds.

three (of eight) system interrupt levels to I/O peripherals. Low bandwidth peripherals (e.g. terminal controllers) should attach to PINT[0]0, the lowest interrupt priority, and high bandwidth ones (e.g. disk controllers) should attach to PINT[1]0. PINT[2]0 is reserved[14].

Signals PINT[2-0]0 (open-collector) are shared by all I/O peripherals; any I/O device can attach itself to any one, and only one, of these three levels. Similar to the one bus acknowledge, three interrupt acknowledges are daisy-chained through all peripherals with the I/O device sitting closest to the CPU getting serviced first. PIAK[2-0]0 originate from the System Board, PIAKI[2-0]0 refer to the interrupt acknowledge *inputs* of a given peripheral and PIAKO[2-0]0 are the corresponding *outputs* of the chain. Unused interrupts shall have the associated input and output acknowledges tied together and no two I/O devices shall be physically separated by an empty slot.

The interrupt request/acknowledge syndrome differs that of the bus request/acknowledge in that a peripheral may assert PINT[i]0 at will. Still, PIAKO[i]0 (and consequently PIAKI[i]0) may not glitch and the scheme used for bus request/acknowledge (Figure 11a) may also be used with interrupt request/acknowledge.

A peripheral begins an interrupt operation by asserting a particular PINT[i]0. Refer to Figure 9. After generating PINT[i]0, the CPU will recognize the interrupt when the current program execution level and all pending interrupt requests are lower than the requesting interrupt level, and when execution reaches an instruction boundary. Upon recognition of an interrupt, the CPU will request to access a peripheral (i.e. use the I/O Bus), as opposed to accessing main memory. When granted the bus, the CPU will generate the appropriate interrupt acknowledgement signal which will be held up at the main memory controller until PR1W0, PLOCK0 and PPA[23-0]0 are available. The CPU will indicate a read operation (PR1W0 = 1) and place an unspecified address on the bus; the CPU's objective here is to read the interrupting device's 8-bit interrupt vector. The interrupt vector of the requesting device will consequently be read as if a normal CPU read cycle. (Note: PIAKI[i]0 differentiates an interrupt acknowledge operation from a normal read operation. In addition, since the vector is always 8 bits wide and PSIZE160 is open-collector and pulled HIGH, a 16-bit peripheral need not drive PSIZE160 during an interrupt acknowledge cycle.)

The System Board will remove PIAK[i]0 on receipt of PDTACK0 allowing the peripheral to remove PINT[i]0.[15] (Containing the acknowledge signal within the

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14. AT&T Bell Laboratories reserves the right to utilize PINT[2]0 at any time to supply the best product possible and makes no warranty, express or implied, for peripherals which use PINT[2]0 and furthermore assumes no responsibility for any such products or 3B 2 computer which uses such products.

15. PINT[i] will be removed after PIAK[i]0, automatically via hardware (i.e. "autoclear") or by software.

request signal allows a peripheral to use PINT[i]0 to block PIAKO[i]0 from propagating.)

The System Board CPU assigns unique interrupt vectors to each peripheral during system autoconfiguration on power-up. All vectors are a single byte of data, always on I/O Bus byte 1 (bits 00-07). Refer to [2] for details on the formation of the interrupt vector.

3.7 Error Detection and Handling

Two I/O Bus signals are dedicated to fault detection: PFAIL0 (Peripheral Board Fail) and PFLT0 (Peripheral Bus Fault). PFAIL0 (open-collector) is shared by all peripherals and is activated on an error (e.g. sanity failure) within an intelligent peripheral. PFAIL0 can be activated any time.

PFLT0 (bidirectional, open-collector), also common among all peripherals, is currently only activated by the System Board and has the same timing specifications as PDTACK0. A bus timeout or data parity error precipitate PFLT0 which then sets a System Board Control and Status (CSR) bit and interrupts the CPU. The bus master shall end the cycle on receipt of PFLT0.

Parity is only checked on data read from main memory and not propagated over the I/O Bus. Most faults (e.g. protocol errors), however, are expected to manifest themselves as bus timeouts. To this end, the time from PBACK0 going active to PPAS0 going inactive is measured by the arbiter; exceeding the specified limit yields a bus timeout. (For multiple access cycles, the timer is reset at the start of each transfer.) In the event of an I/O Bus request with no ensuing operation (no PPAS0), the system will hang. Finally, diagnostics afford a system integrity check other than these "normal" run time ones.

3.8 Autoconfiguration

On power up, all peripherals will be reset and 3B 2 system firmware will attempt system autoconfiguration. To this end, all "3B 2-native" peripherals shall provide an ID Register whose width corresponds to the width of the given peripheral; 8 (16) bit peripherals have 8 (16) bit ID Registers. Each peripheral type has a unique ID code as discussed in [2]. (Operator intervention is necessary with CBA-based peripherals.)

4. ELECTRICAL REQUIREMENTS

These electrical requirements are based on an I/O Bus 20 inches in length (electrical) with at most 12 peripheral taps and 1 System Board tap (i.e. the Model 400 is used as the worst case).[16] Each *peripheral* tap may have at most 2

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16. Although the CPU's address space allows up to 15 peripherals (i.e. PCS[15-01]0), only 12 will be supported due to electrical constraints.

74LSTTL input loads and 1 74LSTTL output load and present a maximum of 45 pf of capacitance such that a fully loaded bus can be expected to have up to 700 pf (Figure 12).[17] Finally, terminating resistors are used to minimize reflections and ringing.

4.1 Timing

There are five concerns with I/O Bus timing:

1. Time of flight / bus skew
2. Setup times
3. Hold Times
4. Bus cycle termination times
5. Bus cycle length - timeouts.

For a fully loaded bus, a maximum time of flight of 40 nanoseconds is possible. This number directly affects the overall timing of a bus cycle. For example, to ensure 20 nanoseconds address setup time at the slave, the bus master must guarantee a stable address at least 60 nanoseconds before activation of address strobe (PPAS0). Also, there shall be at least a hold time of 10 (50) nanoseconds at the slave (master) on the address after removal of the address strobe and on write data after removal of the data strobes.

As one bus cycle ends, another may soon be in progress; care must be taken to prevent tri-state overlap between the current and previous bus occupants. To this end, the figures also include bus cycle termination specifications. The philosophy of the cycle termination employed is: The bus master dictates when the cycle can be ended and can do so *only after the data has been received*. The action indicating end-of-cycle is removal of strobes PPAS0 and PDS[1-0]0 (and PBUSY0 if a peripheral is master). There is no more handshaking after this point. Instead, the master guarantees to drive its strobes HIGH for at least 40 nanoseconds before deactivating all its signals.[18] (PBRQ0 is a possible exception since it could have been removed as early as after PPAS0 had been asserted. At any rate, however, PBRQ0 must have risen to a HIGH state - which could take as much as 150 nanoseconds - at most 50 nanoseconds after the strobes have been driven HIGH.)

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17. As discussed later, signals PSIZE16, PDTACK0 and PFLT0 require high current drive (Schottky or standard driver) and a single I/O load and are thus exceptions to this requirement. Furthermore, limiting these taps to a single load lowers their maximum allowable tap capacitance from 45 pf to 41 pf and the maximum net capacitance from 700 pf to 600 pf (Figure 12).

18. A minimum of 40 nanoseconds guarantees that signals are inactive at the start of the next cycle. Otherwise, with a 700 pf undriven bus pulled up with 390 Ohms, the rise time to threshold would be about 150 nanoseconds.

On removal of the strobes, the slave will in turn remove PDTACK0,[19] data (if the operation was a read) and PSIZE160 (if a peripheral is the current bus slave).

As mentioned previously, the arbiter times each data transfer. In addition, the length of a bus cycle (especially for multiple accesses) is constrained.

4.2 Current Driving/Loading Requirements

The table below specifies a peripherals maximum current driving and loading requirements. (Current out of a terminal is given as a negative value.) Many commercial devices of the 74 LSTTL series (e.g. 33, 125A, 240, 244, 645 and 646) meet these specifications, except for the PSIZE160, PDTACK0 and PFLT0 specifications. Here a 74 STTL or 74 Standard TTL device may be required (e.g. 7407).

4.3 Termination Resistors

A primary objective of bus termination resistors is to eliminate signal reflections as caused when the bus length is greater than a signal's rise time. An unloaded bus with 12 nh and 3.5 pf per inch has a characteristic impedance of about 59 ohms and a propagation delay of about 2.5 nanoseconds per foot.[4] Loading a 20 inch bus with 13 taps[20] totaling 700 pf (3B 2/400), significantly lowers the characteristic impedance while increasing the time of flight to about 40 nsec. A bus length of 40 nsec. is certainly greater than the rise time of even LSTTL driven signals and thus signal reflections can be expected.

Although terminating the bus with its characteristic impedance (<< 60 ohms) will completely eliminate bus refections, driving it would be practically impossible. Some termination, however, would be helpful and, therefore, the address, data and status lines will be terminated in a network consisting of 390 ohms to VCC and 560 ohms to ground.[21] All open-collector signals of all models will be pulled to VCC[21] while daisy-chained signals will have a high impedance (1k ohms)

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19. As indicated in Tables 3 and 4, PSIZE160, PDTACK0 and PFLT0 are open-collector and require an Iol current drive of at least 40 mA and pullup resistance of 195 ohms. Such an arrangement yields a worst-case charge time to threshold of 60 nanoseconds. Recall these leads are allowed only 1 Schottky load per tap and consequently will yield a lower net capacitance (600 pf) than otherwise (700 pf if 2 input and 1 output LS loads allowed).

20. 12 peripherals and 1 System Board yield 13 taps. Note: the System Board is allowed 4 I/O loads on PD[15-00], 2 loads on PSIZE160, PDTACK0 and PFLT0 and 3 loads on the remaining signals.

21. Such an arrangement brings an undriven line to about 3 volts instead of 5, resulting in less of a voltage swing (minimize crosstalk). Both resistor arrangements - pullup versus termination network - have the same effect on reducing reflections.

TABLE 3. Peripheral Load Currents

Signal	Type	source	Iol (mA)	Ioh (mA)	Iil (mA)	Iih (mA)
PBUSY0	LS - ts	periph	24	-15	-.8	.04
PBRQ0	LS - oc	periph	40	-	-.8	.04
PBACKI0	S - tp	sys/periph	20	-1	-9?	.1
PBACKO0	S - tp	periph	20	-1	-9?	.1
PCS[	LS - tp	sys	8	-.4	-.8	.04
PD[15-00]0	LS - ts	bi-direc	24	-15	-.8	.04
PDS[1-0]0	LS - ts	bi-direc	24	-15	-.8	.04
PDTACK0	S - oc	bi-direc	40	-	-.4	.02
PFAIL0	LS - oc	periph	40	-	-.8	.04
PFLT0	S - oc	bi-direc	40	-	-.4	.02
PINT[2-0]0	LS - oc	periph	40	-	-.8	.04
PIAKI[2-0]0	S - tp	sys/periph	20	-1	-9?	.1
PIAKO[2-0]0	S - tp	periph	20	-1	-9?	.1
PLOCK0	LS - ts	periph	24	-15	-.8	.04
PPA[23-00]1	LS - ts	bi-direc	24	-15	-.8	.04
PPAS0	LS - ts	bi-direc	24	-15	-.8	.04
PR1W0	LS - ts	bi-direc	24	-15	-.8	.04
PSIZE160	S - oc	periph	40	-	-.4	.02
RQRST0	LS - oc	periph	40	-	-.8	.04
SYSRST0	LS - tp	sys	24	-1.2	-.8	.04

Notes:

1. Legend
   S => Schottky (or standard) driver
   LS => Low power Schottky driver
   ts => tri-state
   oc => open-collector
   tp => totem-pole
2. Includes 5 mA through 1k ohm pullup resistor.

pull-up resistor on the input signal physically located *on the peripheral*. Conversely, the other terminating resistors will be located at the electrical end of the I/O Bus, *on the I/O Expansion Board* (*backplane*). Table 4 presents all I/O Bus signals and associated terminations. (Coincidentally, these attempts to reduce reflections and ringing also minimize RFI.)

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22. Figure 13 uses Thevenin's theorem to compute the minimum terminating resistance for each 3B 2 model on the assumption that only LSTTL gates with a minimum Iol of 24mA or 40mA (74 series) are used. Note: in the interest of inventory management, only 1 set of resistor values will be used although the shorter bus of the 3B 2/300, for instance, could use lower values.

4.4 Lead Parallelism

The possibility of crosstalk necessitates restricting the parallelism of some signal paths.

> "Crosstalk in digital systems is the coupling of an unwanted signal onto a "passive" line (wire or net) due to the switching of adjacent "active" lines. The coupling is a result of the mutual inductance and capacitance which is a function of the closeness of the lines. For coupled lines, ..., crosstalk is significantly larger if the lines are uniformly parallel." [5]

There are essentially two coupling situations. First, adjacent signals switch simultaneously (e.g. data bus bits), generating coupled signals on each other. No rerouting is required, assuming that a settling time of a few nanoseconds is provided. Conversely, a signal may switch while an adjacent line is passive (e.g. a control lead or clock signal coupled with bus bits); such situations are prone to crosstalk.

To minimize crosstalk, routing should limit the alignment length of switching signals with passive ones and all signals will be mixed with grounds and VCCs (AC grounds). Audits should be used to flag potential coupling problems.

TABLE 4. Bus Termination (Ohms)

Signal	Type	3B 2/200 termination	3B2/300 termination	3B2/400 termination	location
PBUSY0	ts	390	390	390	backplane
PBRQ0	oc	390	390	390	backplane
PBACKI0	tp	1k	1k	1k	periph.
PBACKO0	tp	-	-	-	N/A
PCS0	tp	1k	1k	1k	periph.
PD[15-00]0	ts	*	*	*	backplane
PDS[1-0]0	ts	390	390	390	backplane
PDTACK0	oc	195	195	195	backplane
PFAIL0	oc	390	390	390	backplane
PFLT0	oc	195	195	195	backplane
PINT[2-0]0	oc	390	390	390	backplane
PIAKI[2-0]0	tp	1k	1k	1k	periph.
PIAKO[2-0]0	tp	-	-	-	N/A
PLOCK0	ts	*	*	*	backplane
PPA[23-00]1	ts	*	*	*	backplane
PPAS0	ts	390	390	390	backplane
PR1W0	ts	*	*	*	backplane
PSIZE160	oc	195	195	195	backplane
RQRST0	oc	390	390	390	backplane
SYSRST0	tp	390	390	390	backplane

Notes -

a) Legend:
   ts => tri-state
   oc => open-collector
   tp => totem-pole
   * => 390 Ohms to VCC and 560 Ohms to GRD
   - => none
   N/A => Not Applicable

b) 195 ohms = 390 ohms || 390 ohms

c) PBRQ0, PFAIL0, PINT[2-0]0 and RQRST0 may additionally be pulled up on the System Board with 4.7k ohms if so desired.

5. MECHANICAL SPECIFICATIONS

Figure 15 presents the physical structure of 3B 2 I/O. As shown, the System Board contains two connectors, A and B. Connector A[23] contains the address, data, control, power and ground for up to four peripherals (e.g. 3B 2/300). Connector B[24] contains the additional control, power and ground to support twelve peripherals (3B 2/400). Tables 5 and 6 lists the signals of connectors A and B, respectively.

At present, two distinct I/O Expansion Multilayer Boards will exist. The I/O Expansion Board of the 3B 2/300 will plug into both connectors A and B and provide only four peripheral connectors (i.e. fan out only PCS[04-01]0). The I/O Expansion Board of the 3B 2/400 will also plug into both A and B connectors, yet provide twelve peripheral connectors (PCS[12-01]0 fanned out). Both Expansion Boards will route the daisy-chained net between peripheral slots and fan out the chip selects to the appropriate slot. In addition, the terminating resistors discussed earlier will be mounted on the I/O Expansion Boards.

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23. AMP model number 1-530843-1

24. AMP model number 530843-7

TABLE 5. I/O Expansion Connector A (100 pin)

Pin Number	Signal	Pin Number	Signal
1	VCC	2	PPA[23]1
3	PPA[22]1	4	GRD
5	PPA[21]1	6	PPA[20]1
7	PPA[19]1	8	GRD
9	PPA[18]1	10	PPA[17]1
11	VCC	12	GRD
13	PPA[16]1	14	PPA[15]1
15	PPA[14]1	16	GRD
17	PPA[13]1	18	PPA[12]1
19	PPA[11]1	20	PPA[10]1
21	VCC	22	PPA[09]1
23	PPA[08]1	24	GRD
25	PPA[07]1	26	PPA[06]1
27	PPA[05]1	28	GRD
29	PPA[04]1	30	PPA[03]1
31	VCC	32	GRD
33	PPA[02]1	34	PPA[01]1
35	PPA[00]1	36	GRD
37	PLOCK0	38	PR1W0
39	PPAS0	40	GRD
41	VCC	42	PBACK0
43	PBRQ0	44	GRD
45	PD[15]1	46	PD[14]1
47	PD[13]1	48	GRD
49	PD[12]1	50	PD[11]1
51	VCC	52	GRD
53	PD[10]1	54	PD[09]1
55	PD[08]1	56	GRD
57	PD[07]1	58	PD[06]1
59	PD[05]1	60	GRD
61	VCC	62	PD[04]1
63	PD[03]1	64	GRD
65	PD[02]1	66	PD[01]1
67	PD[00]1	68	GRD
69	PDS[1]0	70	PDS[0]0
71	VCC	72	GRD
73	PDTACK0	74	PSIZE160
75	PFLT0	76	GRD
77	PFAIL0	78	PBUSY0
79	SYSRST0	80	GRD
81	VCC	82	PIAR[0]0
83	RQRST0	84	PIAR[1]0
85	PINT[0]0	86	PIAR[2]0
87	PINT[1]0	88	GRD
89	PINT[2]0	90	VBKUP
91	VCC	92	GRD
93	PCS[01]0	94	V12N
95	PCS[02]0	96	GRD
97	PCS[03]0	98	V12P
99	PCS[04]0	100	GRD

TABLE 6. I/O Expansion Connector B (60 pin)

Pin Number	Signal	Pin Number	Signal
1	VCC	2	PCS[05]0
3	VCC	4	GRD
5	PCS[06]0	6	GRD
7	VCC	8	GRD
9	VCC	10	GRD
11	PCS[07]0	12	GRD
13	VCC	14	GRD
15	VCC	16	GRD
17	PCS[08]0	18	GRD
19	VCC	20	GRD
21	VCC	22	GRD
23	PCS[09]0	24	GRD
25	VCC	26	GRD
27	VCC	28	GRD
29	PCS[10]0	30	GRD
31	VCC	32	GRD
33	VCC	34	GRD
35	PCS[11]0	36	GRD
37	VCC	38	GRD
39	VCC	40	GRD
41	PCS[12]0	42	GRD
43	VCC	44	GRD
45	VCC	46	GRD
47	PCS[13]0	48	GRD
49	VCC	50	GRD
51	VCC	52	GRD
53	PCS[14]0	54	GRD
55	VCC	56	GRD
57	VCC	58	GRD
59	PCS[15]0	60	GRD

There are two different sizes of I/O boards: about 6.5 inches by 7.4 inches (single width) and 13.4 inches by 7.4 inches (double width). Figures 16a and 16b present single width measurements and topology for the CM195 family. Figure 16c presents the pinout for a peripheral connector[25] and Table 7 lists the signals present at each of these connectors. (Double width specifics are to be determined.)

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25. AMP model number 1-530843-0

TABLE 7. Peripheral Connector (86 pin)

Pin Number	Signal	Pin Number	Signal
1	V12P	2	PINT[2]0
3	V12N	4	PINT[1]0
5	PBACKI0	6	PINT[0]0
7	PCS0	8	RQRST0
9	GRD	10	SYSRST0
11	VBKUP	12	PFAIL0
13	PIAK0[2]0	14	PFLT0
15	PIAKI[2]0	16	GRD
17	VCC	18	PDTACK0
19	PIAKI[1]0	20	PDS[1]0
21	PIAK0[1]0	22	PD[00]1
23	PIAKI[0]0	24	PD[02]1
25	GRD	26	PD[03]1
27	PBUSY0	28	PD[05]1
29	PIAK0[0]0	30	PD[07]1
31	PSIZE160	32	GRD
33	PDS[0]0	34	PD[08]1
35	PD[01]1	36	PD[10]1
37	GRD	38	PD[12]1
39	PD[04]1	40	VCC
41	GRD	42	PD[13]1
43	PD[06]1	44	PD[15]1
45	PD[09]1	46	PBRQ0
47	PD[11]1	48	GRD
49	GRD	50	PPAS0
51	PD[14]1	52	PLOCK0
53	PBACK00	54	PPA[00]1
55	PR1W0	56	GRD
57	GRD	58	PPA[02]1
59	PPA[01]1	60	PPA[04]1
61	PPA[03]1	62	PPA[05]1
63	PPA[06]1	64	VCC
65	GRD	66	PPA[07]1
67	PPA[09]1	68	PPA[08]1
69	PPA[10]1	70	PPA[11]1
71	PPA[12]1	72	GRD
73	GRD	74	PPA[13]1
75	PPA[15]1	76	PPA[14]1
77	PPA[17]1	78	PPA[16]1
79	PPA[20]1	80	GRD
81	GRD	82	PPA[18]1
83	PPA[23]1	84	PPA[19]1
85	PPA[21]1	86	PPA[22]1

6. PERFORMANCE OBJECTIVES

Two different aspects of bus performance are discussed: bus efficiency and bandwidth. Achieving efficient and fair bus utilization are the overriding concerns here. (Refer to [2] for further discussion of these issues as well as bus occupancy.)

6.1 Bus Efficiency

Within this document, bus efficiency is defined as the ratio of "time actively using bus" to "time holding bus." By actively using the bus, we mean a peripheral is progressing through an I/O Bus operation, asserting strobes for example as opposed to just sitting idle holding PBACKIO. A peripheral is considered holding the bus from the time PBACKIO is received until data strobes are driven inactive and tri-stated.

All I/O Bus peripherals must approach a bus efficiency of 100%. Translated, all peripherals must begin sequencing through the desired I/O Bus operation *immediately* after receiving PBACKIO. This requirement, however, is more likely to be applicable to multiple access cycles. As an example, the use of DMA controllers which have separate fetch and deposit operations may not be used within a multiple access cycle since doing so would severely underutilize the bus. Refer to [2] for details.

6.2 Bus Bandwidth

The amount of information (data) which can be transferred over the I/O Bus defines bus bandwidth. It is a function of the architecture of the I/O Bus as well as the *efficiency* of System Board arbiter and peripheral designs. Critical paths within each bus cycle are:

1. PBRQ0 assertion to assertion of PBACK0 (only for case of peripheral as bus master).
2. Active PBACK0 (or PCS0 if System Board CPU is master) to assertion of PDS[1-0]0.
3. Active PDS[1-0]0 to assertion of PDTACK0.
4. Active PDTACK0 to removal of PDS[1-0]0.[26]
5. Inactive PDS[1-0]0 to start of next cycle (e.g. PBACK0 asserted). Multiple accesses are performance effective in that this step is not relevant.

---

26. In the interest of system performance, a peripheral could latch read data with PDTACK0 and asynchronously remove PDS[1-0].

Preliminary designs achieve a constant I/O Bus bandwidth of 2 megabytes per second.

The above definition of bandwidth doesn't take into account the bandwidth available to each peripheral. Bus access priority does. As discussed earlier, 3B 2's I/O bus arbitration scheme dynamically distributes bus priority nearly evenly across all peripherals. Obviously then, an increase in the number of peripherals yields a corresponding decrease in bandwidth available to each peripheral. A peripheral can *typically* (i.e. no multiple access cycle in progress) expect to wait 1 to 2 microseconds for each peripheral attached to the I/O Bus. If there are 12 peripherals, for instance, each can expect to wait 12 to 24 microseconds to access the bus. (The System Board DMA subsystem, which also resides on the I/O Bus, is a "special-class citizen" in that it doesn't abide by the same fairness rules; increases in disk activity, therefore, proportionately decrease bus availability for peripherals. The current System Board disk controller can occupy the bus up to 1 millisecond.)

An analysis/estimate of overall system performance is beyond the scope of this document.

7. SUMMARY

This document started with a brief overview of the 3B 2 I/O Bus followed by a discussion of the two types of peripherals: programmed and intelligent. An in-depth functional description followed specifying signal definitions, error handling and the data transfer, bus exchange and interrupt acknowledge protocols. From here we delved into the electrical details of loading, driving and timing requirements: each tap may have at most 2 input and 1 output 74LSTTL loads (except PSIZE160, PDTACK0 and PFLT0), present no more than 45 pf (40 pf) of capacitance and allow 40 nanoseconds for time of flight. Electrical analysis also identified the need for terminating resistors on the multilayer I/O Expansion Boards. Section 5 then discussed mechanical issues of the I/O Expansion Board and associated connectors: A, B and peripheral. Finally, the target performance of the 3B 2 I/O Bus was established at 2 million bytes per second.

8. ACKNOWLEDGMENTS

Several people contributed to the formation of the I/O Bus Requirements and Specifications. Craig Miller and Cecil Deisch aided in establishing the electrical characteristics while Kevin McWethy and John Sullivan contributed significantly to the functional aspects. In addition, Ed Hepler and Mike Grinn provided several instrumental suggestions. Finally, thanks goes to the scrutinizing, yet not pedantic, reviewers of this document.

P. M. Walsh

P. M. Walsh

IW-45134-PMW-unix

Atts.

See next page

Atts.
References
Figure 1
Figure 2
Figure 3
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Figure 7
Figure 8
Figure 9
Figure 10
Figure 11 (pages 1-3)
Figure 12 (pages 1-3)
Figure 13 (pages 1-3)
Figure 14 (pages 1-2)
Figure 15
Figure 16 (pages 1-3)

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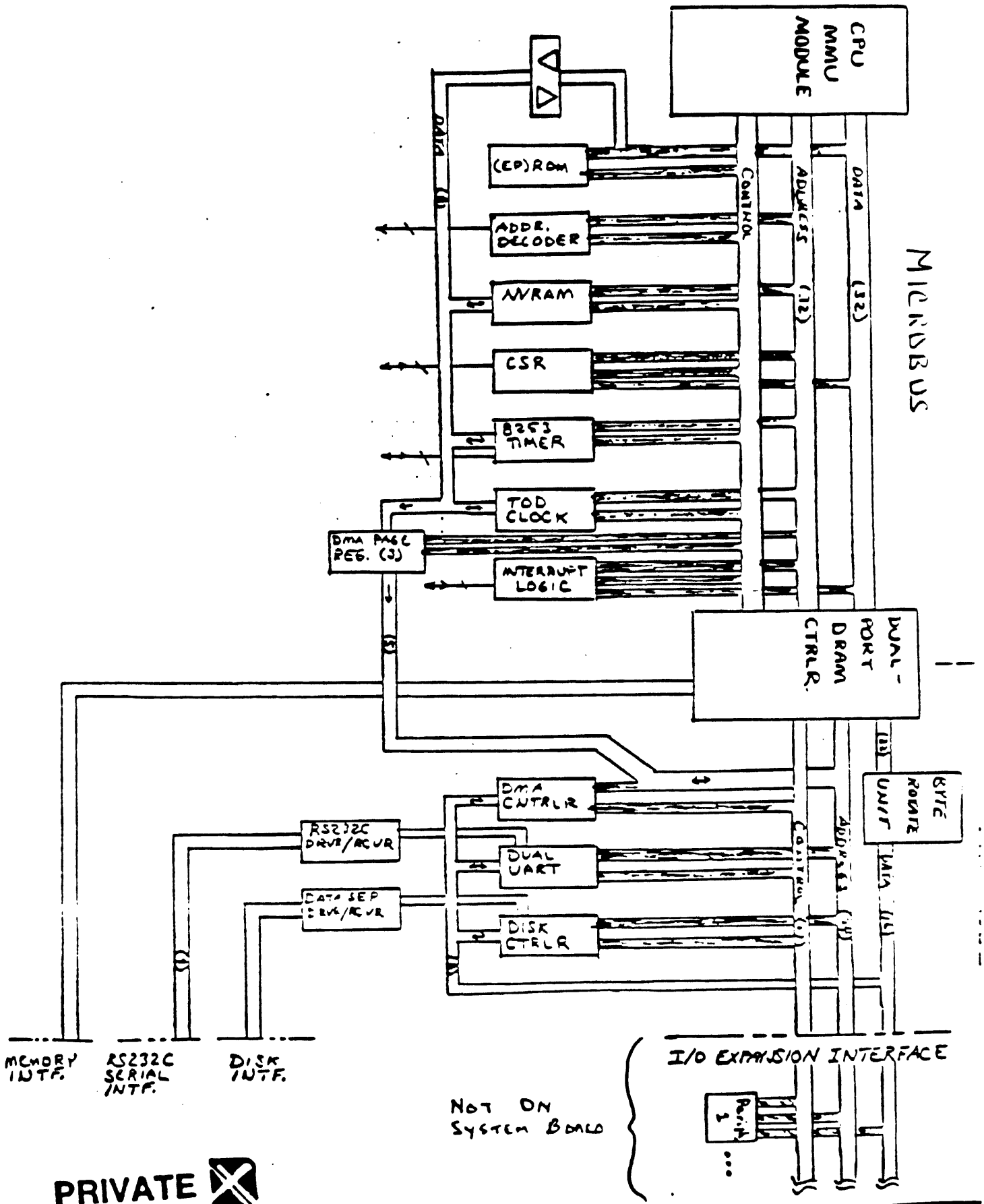
1. D. C. Bina, G. R. Guthrie, E. L. Hepler, G. E. Laggis, D. M. Olien, E. P. Schan, "3B2 System Architecture and Requirements," February 10, 1983.

2. G. E. Laggis, K. P. Sherwin, J. M. Sullivan and P. M. Walsh, "3B2 Requirements - I/O Board Hardware and Firmware Architecture and Design," November 4, 1983.

3. J. M. Sullivan, K. A. McWethy and L. E. Wallis, "3B2 Feature Requirements - Core System Hardware," March 7, 1983.

4. Cecil W. Deisch, "Electrical Design Considerations for a High-Speed Multiport Bus," 45157-820409.01TM, April 9,1982.

5. C. E. Miller, "Crosstalk Considerations for Wirewrap and Multilayer Printed Wire Circuit Packs and Backplanes for the 3B Project", 5515-780920.01MF, 40242-400, September 20, 1978.



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ISSUE	ENGR JMS	TITLE FIG 1	BELL TELEPHONE LABORATORIES INCORPORATED
	DRAWN 12-22-82	3B2 SYSTEM BOARD BLOCK DIAG.	NO. OF SHEETS PER SET

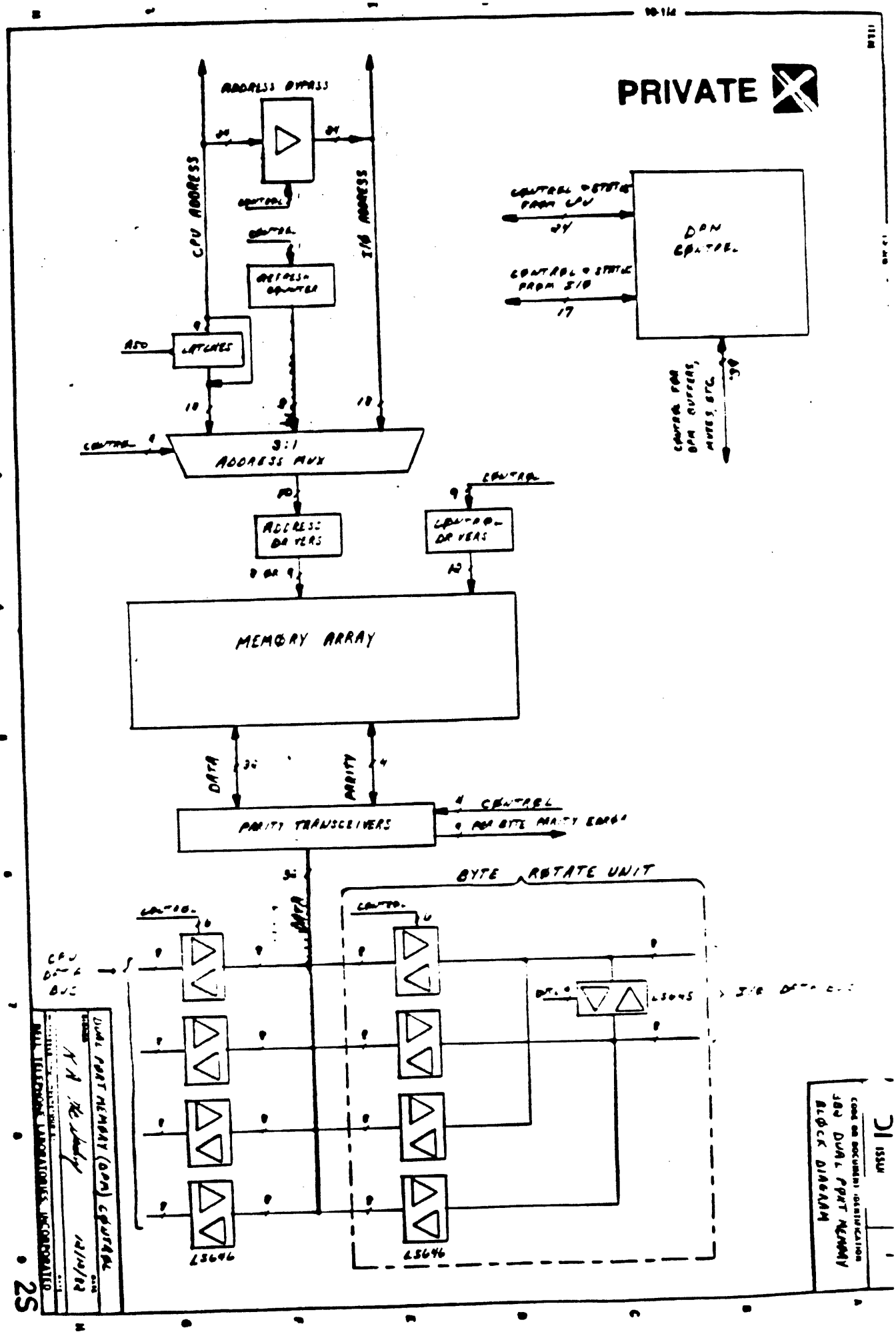
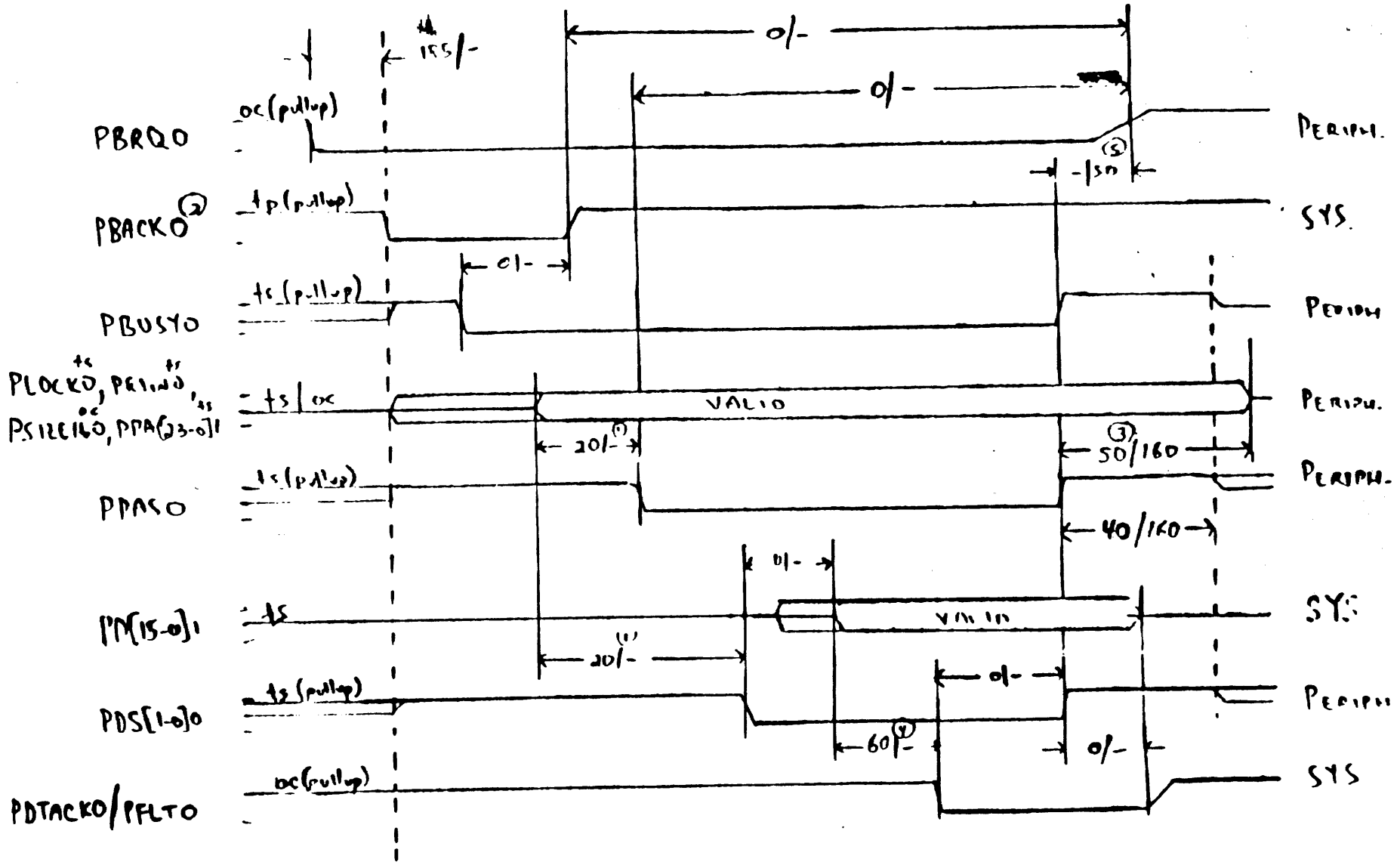

PRIVATE
ADDRESS BYPASS
CPU ADDRESS
I/O ADDRESS
DMA CONTROL
3:1 ADDRESS MUX
ADDRESS DRIVERS
CONTROL DRIVERS
MEMORY ARRAY
DATA
PARITY
PARITY TRANSCEIVERS
BYTE ROTATE UNIT
LS646
LS645
DUAL PORT MEMORY (DPM) CONTROL
BELL TELEPHONE LABORATORIES, INCORPORATED
DUAL PORT MEMORY BLOCK DIAGRAM

FIGURE 2



(1) ADD 40 nsec. to times at PERIPH. CONN. TO ACCOUNT FOR BUS SKEW

(2) PBACKO OF ACKNOWLEDGED DEVICE SHALL REMAIN BLOCKED (HIGH)

(3) 110 nsec. HOLD TIME (MIN) GUARANTEED AT SYS. BRD CONN.

(4) DATA GUARANTEED VALID FOR MIN OF 20nsec AT PERIPH CONN BEFORE PDMRQO

(5) SUFFICIENT 150 nsec. FROM TIME AT PERIPH. CONN. (MAX. PPRQO RISE TIME).

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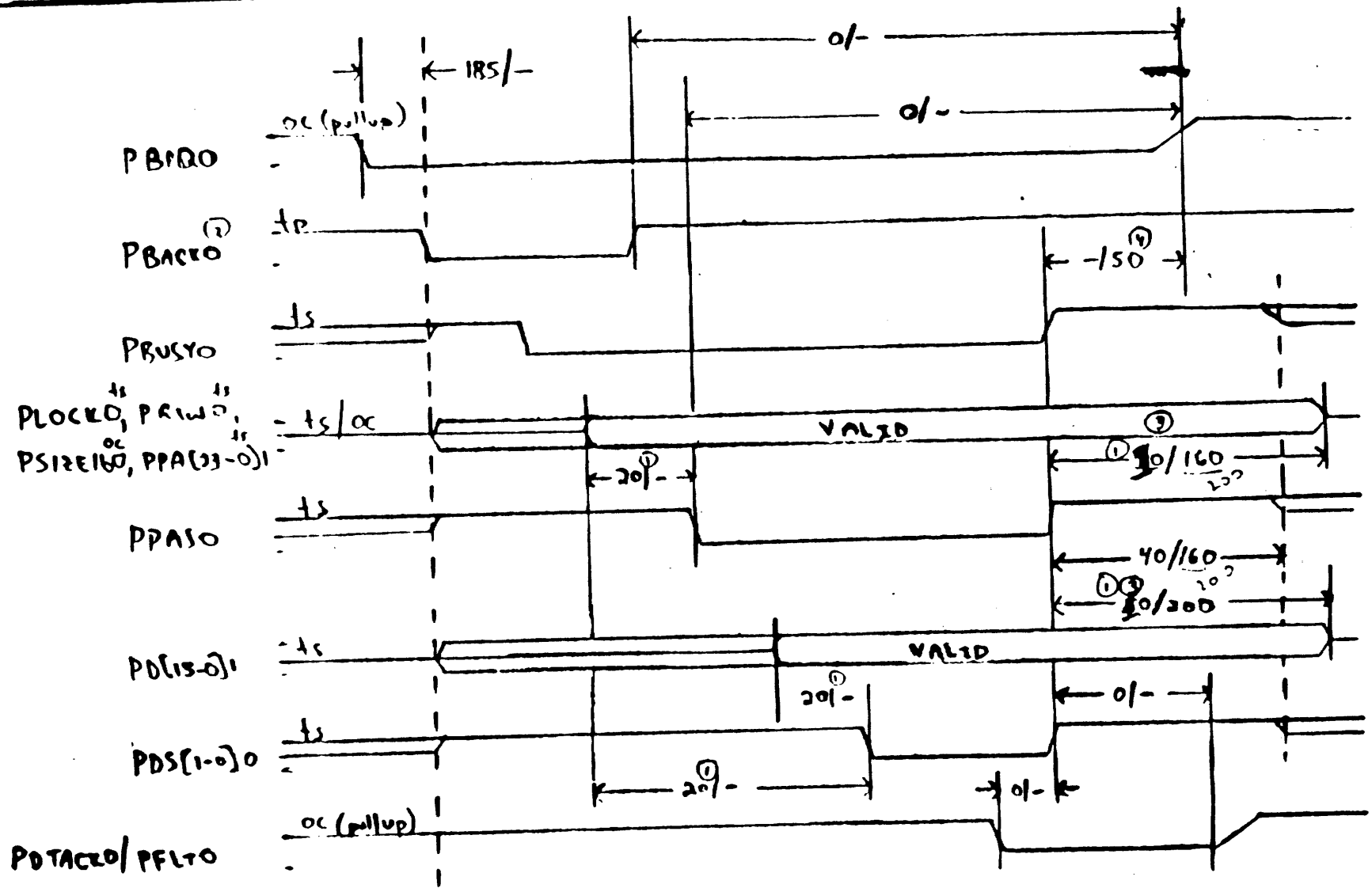
ISSUE 1
FIGURE 3
ENGR PMW
DRAWN 11/22/83
TITLE PERIPH. READ OF P... MEMORY (OS seen at SYS. ≤60, CONN.)
NO OF SHEETS/SHEET 1/1
BELL TELEPHONE LABORATORIES INCORPORATED
SHEE

FIGURE H

ISSUE | DRAWN | ERROR

TITLE
PERIPH WRITE TO MAIN MEMORY
(OS scan + SYS. BAD. conn.)

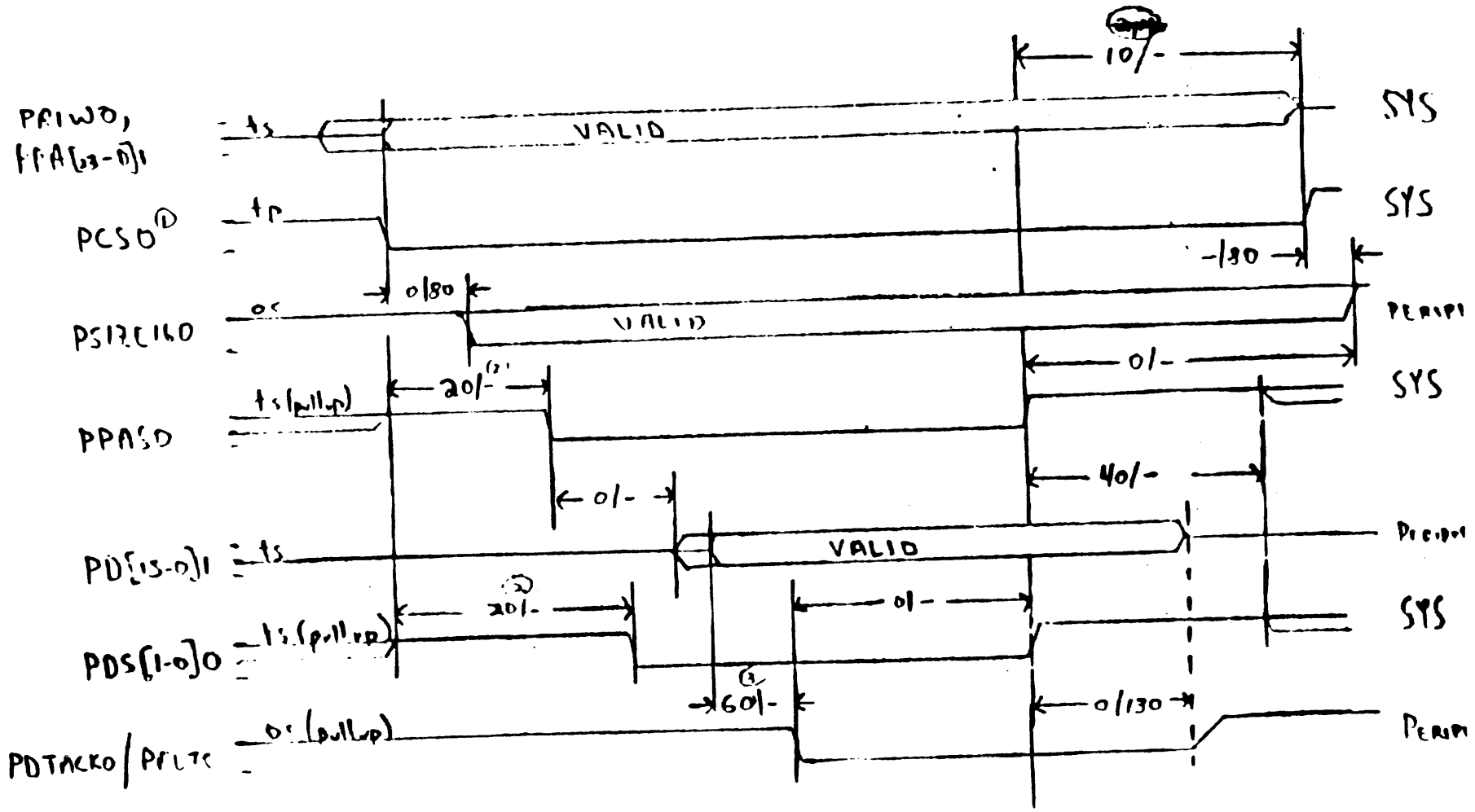


(1) ADD 40 NSEC. TO TIMES AT PERIPH CONN. TO ACCOUNT FOR BUS SKEW

(2) PBACK0 OF ACKNOWLEDGED DEVICE SHALL REMAIN BLOCKED (HIGH) FOR DURATION OF CYCLE.

(3) MIN. HOLD TIME OF 10 NSEC. GUARANTEED AT SYS. BRD. CONN ON ADDRESS & DATA AFTER PPASO↑ & PDS(1-0)↑ RESPECTIVELY

(4) MIN. FACT 150 NSEC. ON TIME AT PER. CONN. (ON PBRQ RISE TIME



① PCSO HAS SAME TIMING SPECS AS PPA[23-0]1, etc.

② ADD 40 nsec to times at SYS. BRD. CONN. TO ACCOUNT FOR BUS SKEW

③ DATA GUARANTEED TO BE VALID AT LEAST 20 nsec AT SYS. BRD. CONN BEFORE PDTACKO

④ MIN. 10 NSEC. HOLD TIME GUARANTEED AT PERIPH. CONN.

ISSUE 1 FIGURE 5

ERROR DWN

DRAWN 11/22/83

TITLE CSV READ OF PERIPHERAL (CSS SIDE of Peripheral conn.)

NO OF ENTITIES

SHEET 1/1

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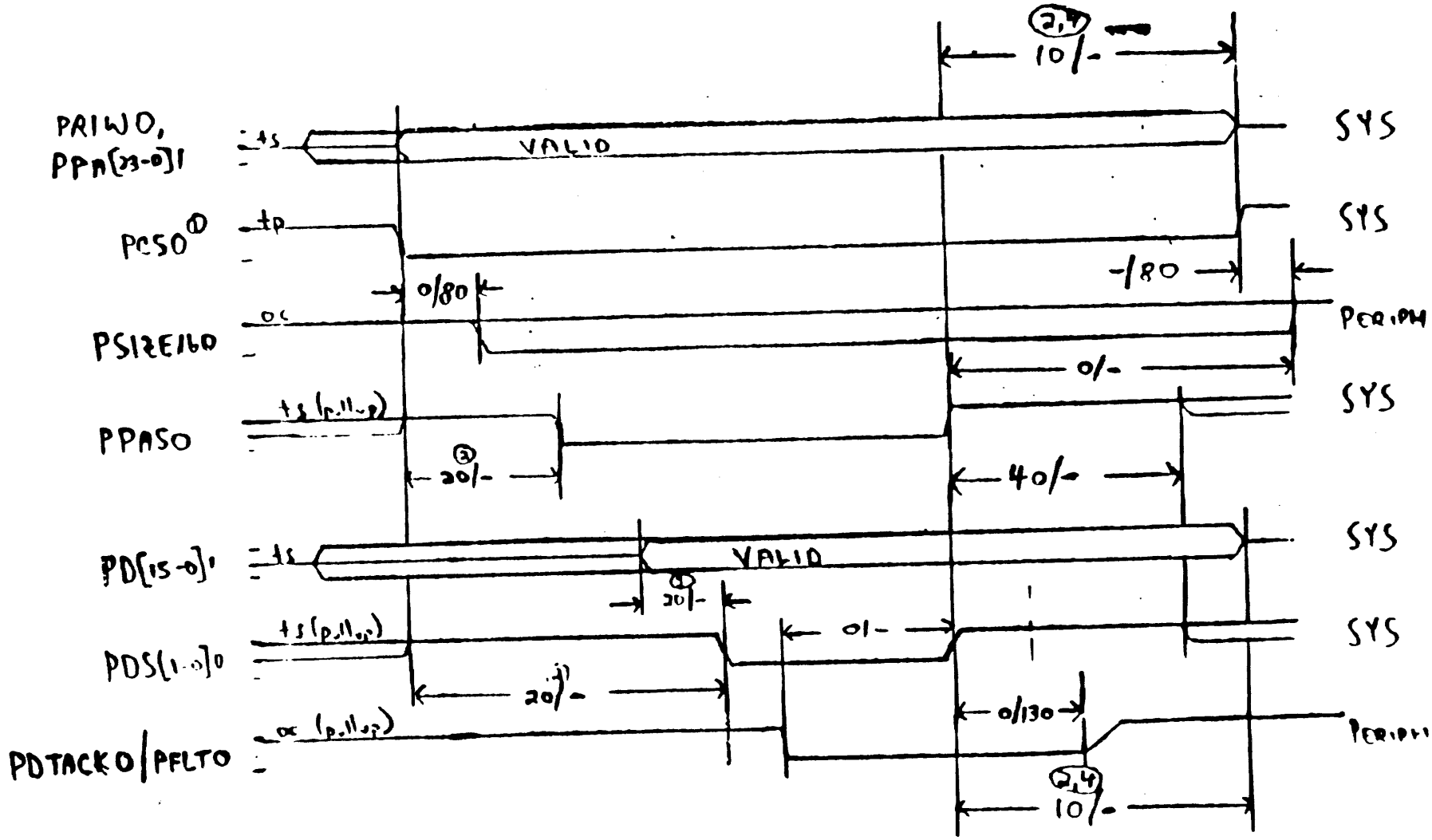
FIGURE 6

ISSUE

ENGR
DRAWN
11/22/83

TITLE
CPU WRITE TO PERIPHERAL
(DOS SYS at Peripheral conn)



① PCSO HAS SAME TIMING SPEC.S AS PPA[23-0]!, etc.

(5) ADD 40 nsec. to times AT SYS. BAD CONN. TO ACCOUNT FOR BUS SKEW

(3) PSIZE16O NEEDED AT LEAST 20nsec. BEFORE PDS[1-0]O AT SYS. BAD CONN.

(4) MIN. OF 10 NSEC. HOLD TIME GUARANTEED ON ADDRESS & DATA AFTER REMOVAL OF PPASO & PDS[1-0], RESPECTIVELY.

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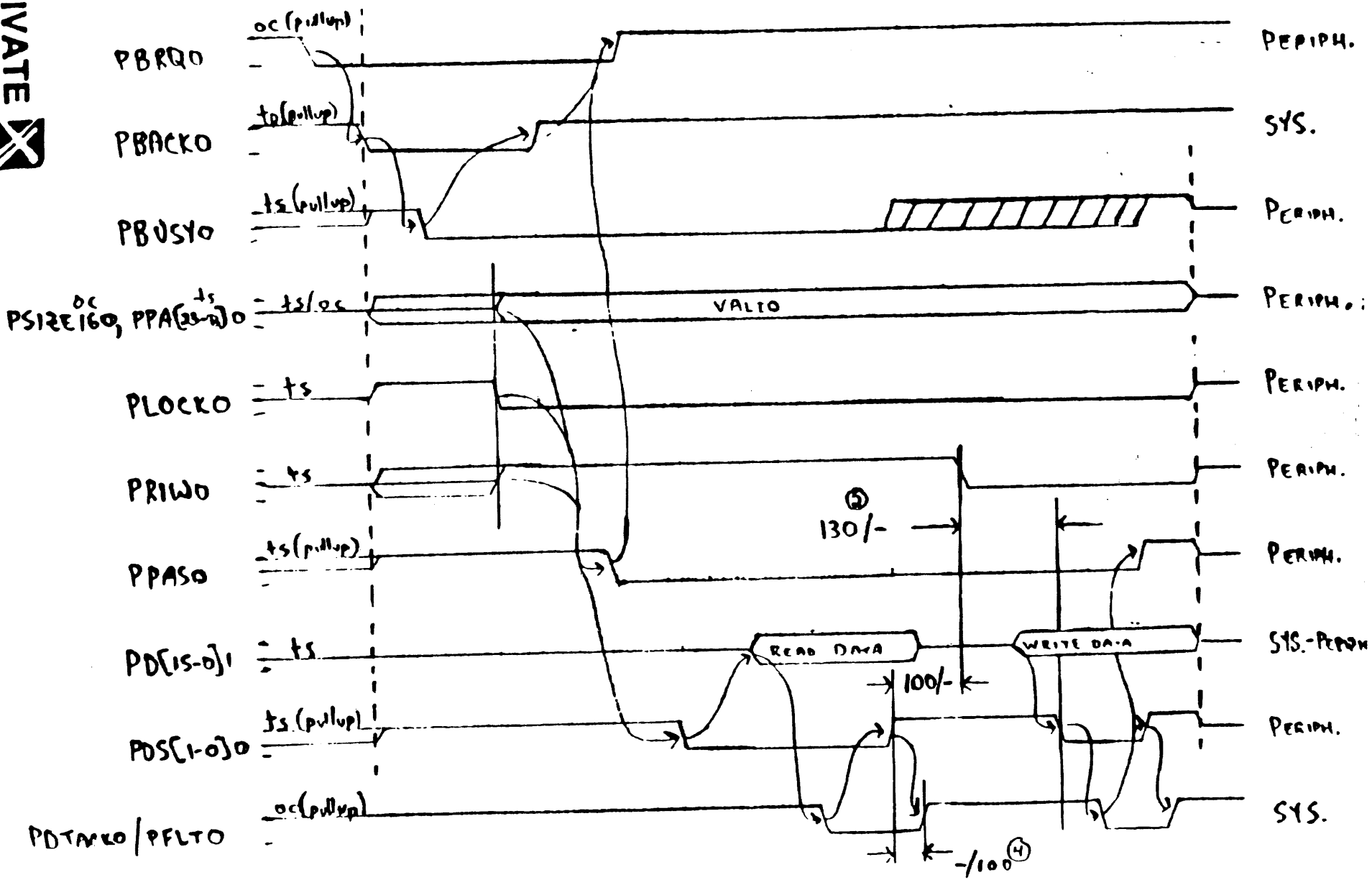
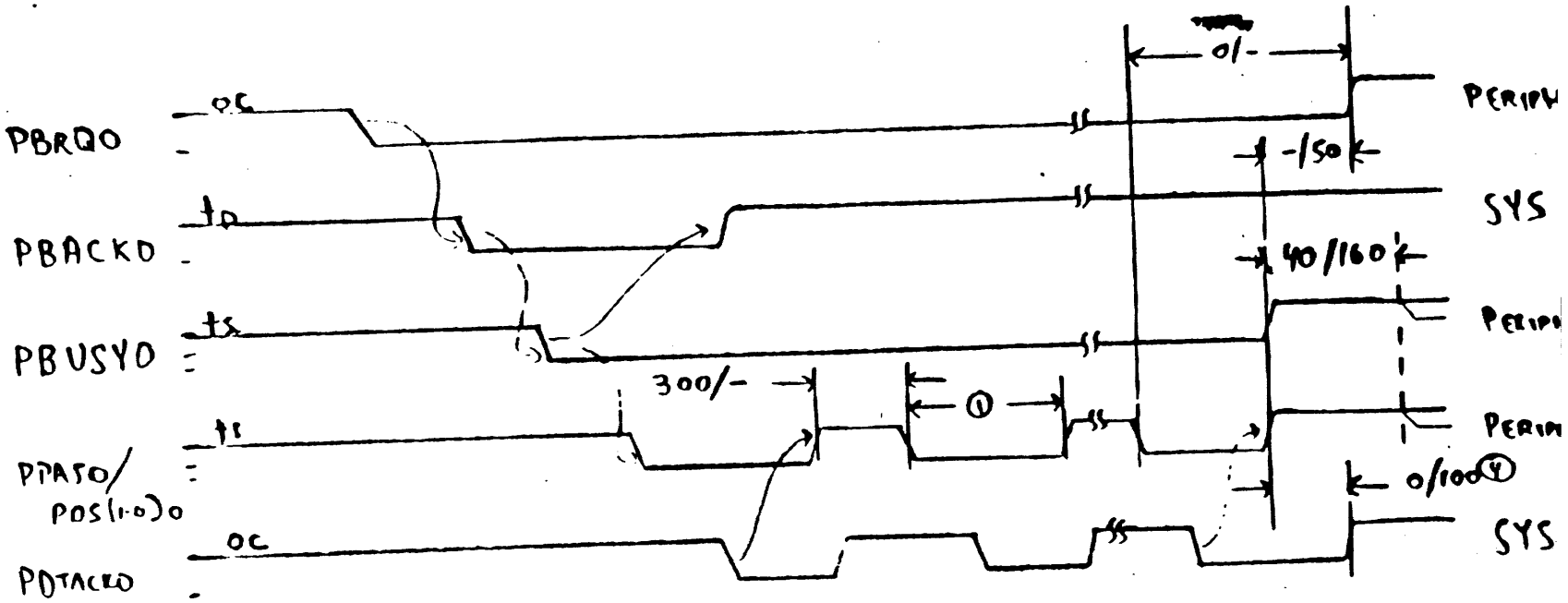
ISSUE 1
ENGR
DRAWN
TITLE PERIPHERAL INTERLOCK WITH MAIN MEMORY (as seen at SYS. BRD Conn.)
BELL TELEPHONE LABORATORIES INCORPORATED
NO OF SHEETS IN SET
SHEET 1/1

Figure 7



① TIMING NOT SHOWN IS CONSISTENT WITH FIGURES 3 AND 4
② ADD 40 NSEC. TO TIME AT PERIPH. CONN.
③ ARROWS INDICATE SEQUENCE OF EVENTS
④ DOES NOT INCLUDE 60 NSEC. RISETIME OF PDTACKO

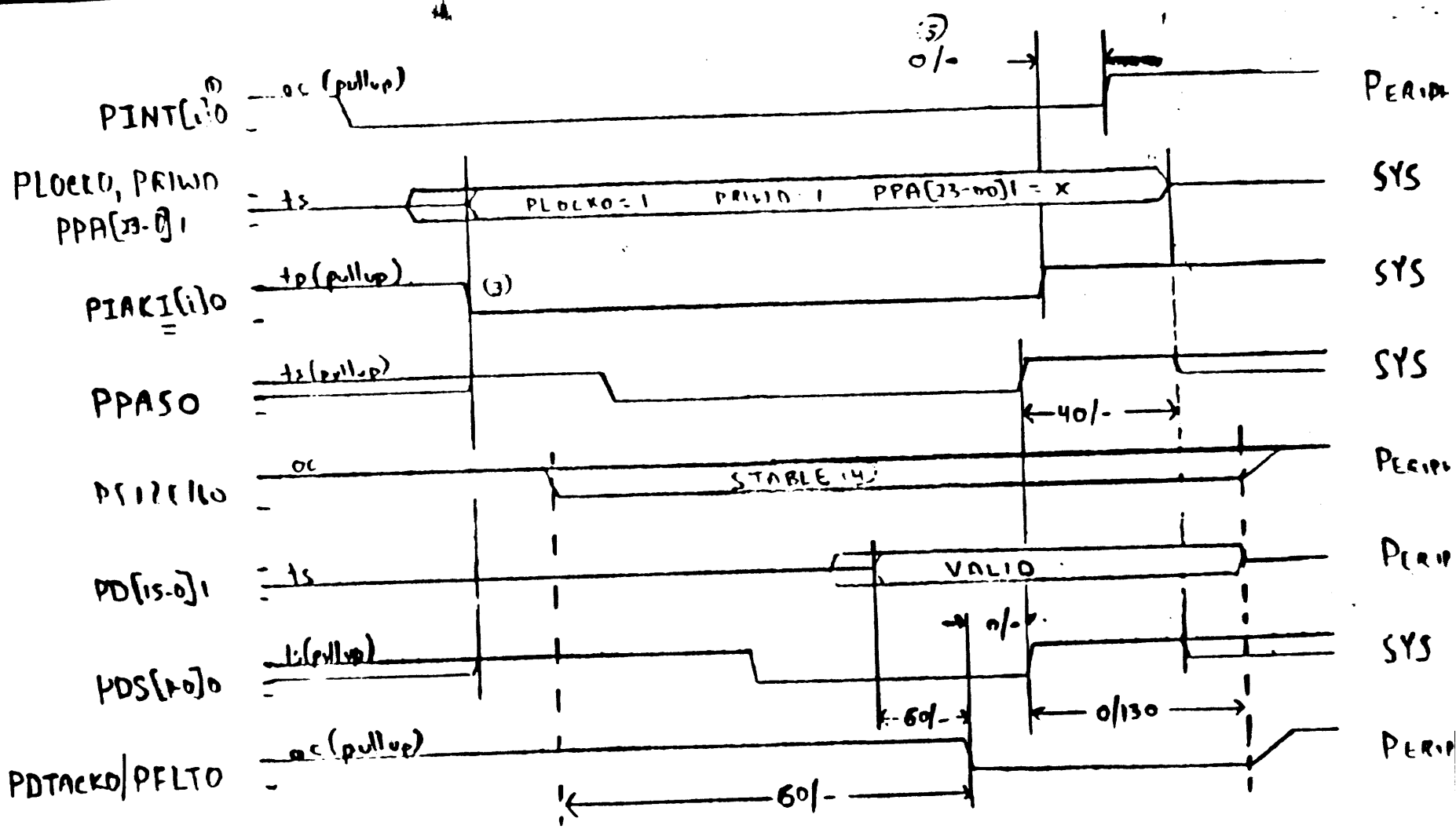


① ARBITER TIMES EACH TRANSFER.

② ARBITER USES PBUSYO TO INHIBIT FURTHER PBACKO'S.

③ ARBITER CAN TEMPORARILY PREEMPT A PERIPHERAL BUS CYCLE TO FORCE A MAIN MEMORY REFRESH. SUCH A PREEMPTION CAN ONLY OCCUR ON A TRANSACTION BOUNDARY.

④ DOES NOT INCLUDE 60 NSEC RISETIME OF PDTACKO.



① i = 0, 1 OR 2

② PIAKO[i]0 OF ACKNOWLEDGED DEVICE REMAINS BLOCKED (i.e. HIGH) FOR DURATION OF CYCLE.

③ DUE TO DAISY-CHAIN PROPAGATION DELAY, PIAKI[i]0 MAY OCCUR MUCH LATER IN CYCLE THAN SHOWN

④ PSIREIGO MAY BE 0 OR 1 DURING PIAK CYCLE, BUT MUST BE STABLE DURING PERIOD INDICATED.

⑤ PINT[i]0 MUST BE REMOVED BEFORE THE COMPLETION OF THE

FIGURE 9

I/O Bus Interrupt Cycle (as seen at Peripheral conn.)

DRAWN 11/23/83

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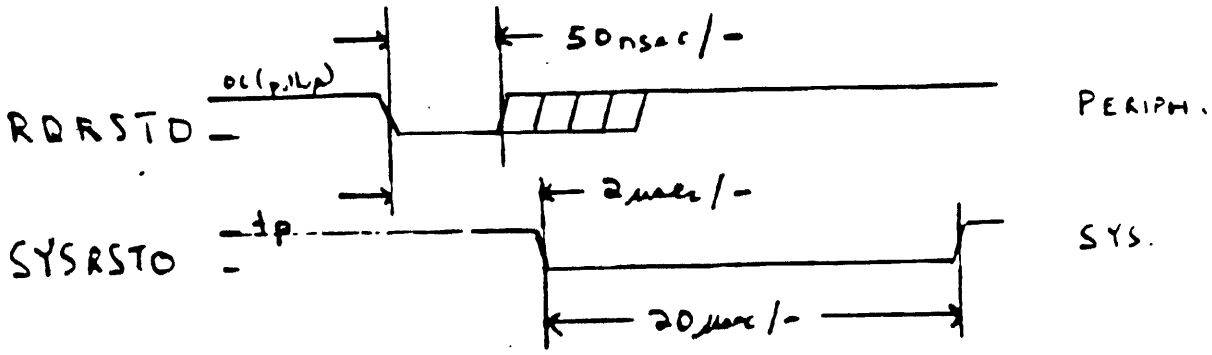

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ISSUE	ENGR	TITLE	BELL TELEPHONE LABORATORIES INCORPORATED
FIGURE 10	DRAWN 11/11/83	3B2 I/O BUS RESET	NO OF SHEETS PER SET: SHE 1/

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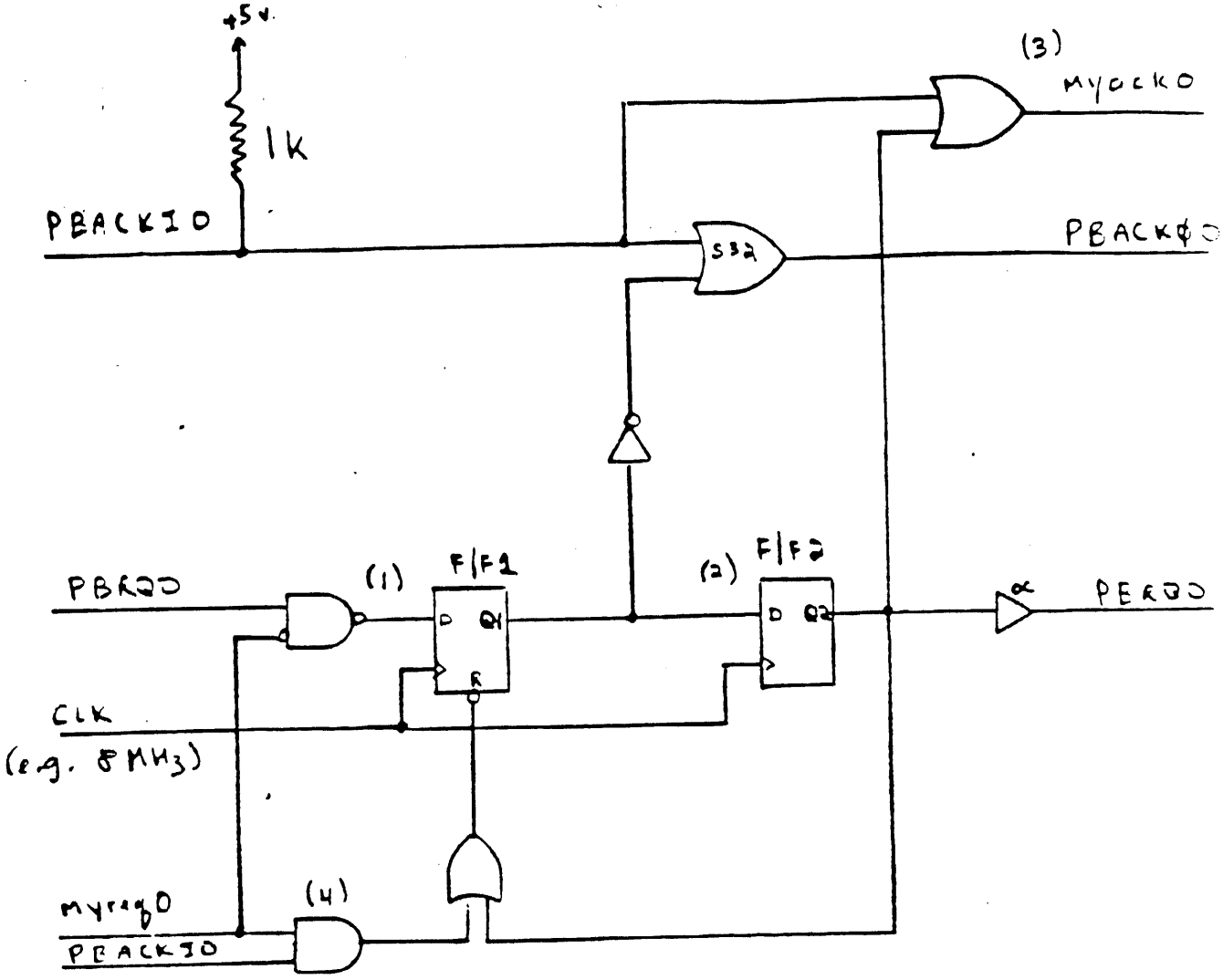
PAT. PENDING



NOTES

(1) F/F 1 CLOCKED LOW WHEN MYREQD ACTIVE & PBRQD INACTIVE, Q1 LOW FORCES PBACKØ INACTIVE (i.e. PBACKIO to PBACKØ BLOCKED)

(2) 1 CYCLE LATER, F/F2 CLOCKED LOW & PBRQD ASSERTED. ALSO, F/F1 HELD LOW VIA RESET PIN.

(3) THE NEXT PBACKIO IS INTERPRETED AS MY ACKNOWLEDGE.

(4) WHEN MYREQD & PBACKIO GO AWAY, F/F1 & THEN PBRQD ARE DEACTIVATED.

ISSUE Figure 11o	ENGR PMW / DRAWN 11/22/83	TITLE 3B2 I/O BUS DAISY-CHAIN LOGIC (typical)	BELL TELEPHONE LABORATORIES INCORPORATED

ISSUE

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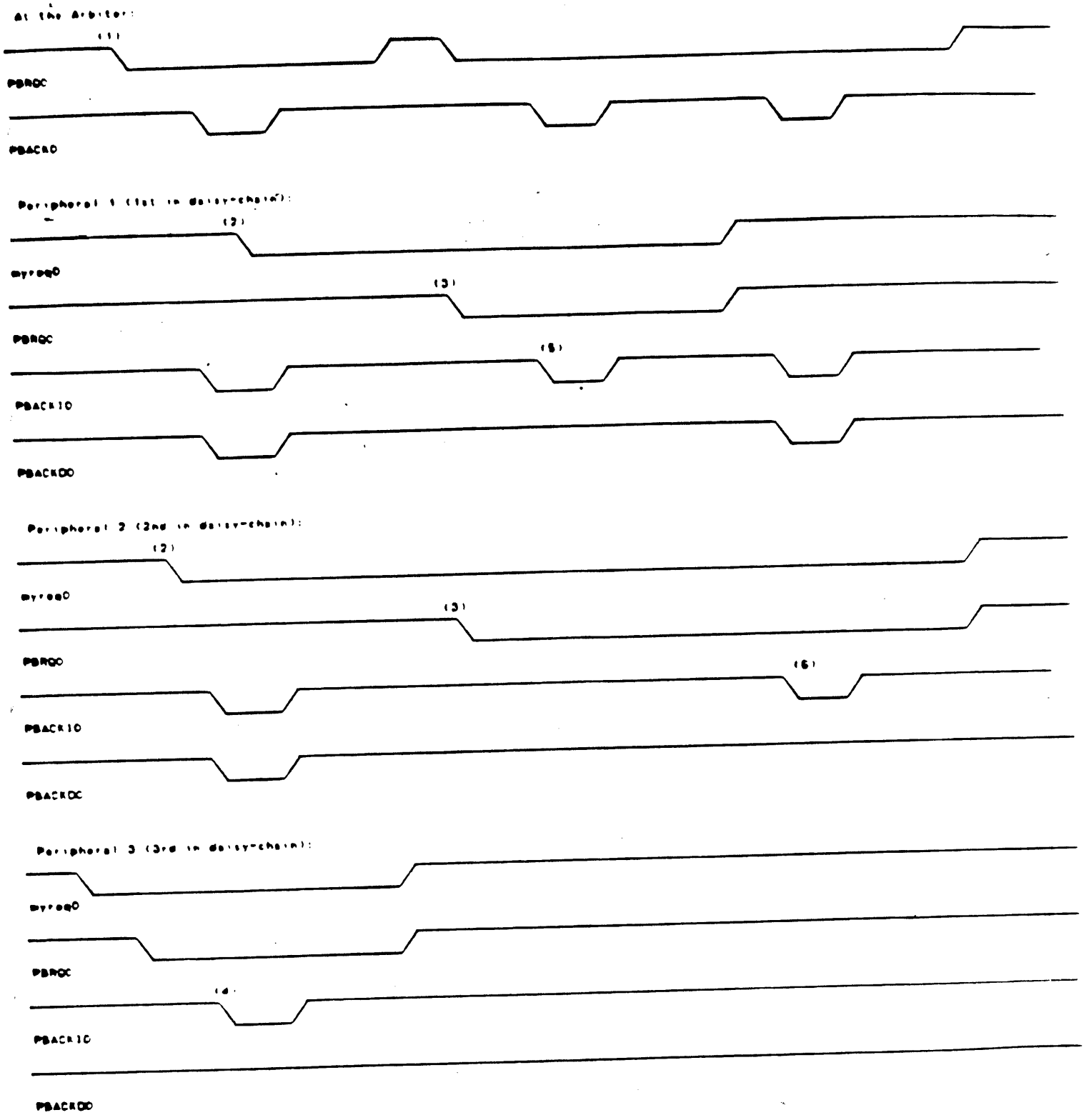

Notes:
(1) PBRQ0, at the arbiter, indicates the actual I/O Bus signal PBRQ0 as shared by all peripherals.
PBRQ0, at each peripheral, indicates how the given peripheral is driving the I/O Bus PBRQ0 signal.
(2) myreq0 indicates when a given peripheral wishes to use I/O Bus.
(3) PBRQ0 (at peripheral) not asserted, however, until shared I/O Bus signal PBRQ0 (at arbiter) detected as inactive.
(4) Peripheral 3 gets on bus. (Peripherals 1 and 2 pass PBACK0 on through.)
(5) Peripheral 1 gets on bus.
(6) Peripheral 2 gets on bus. (Peripherals 1 passes PBACK0 on through.)

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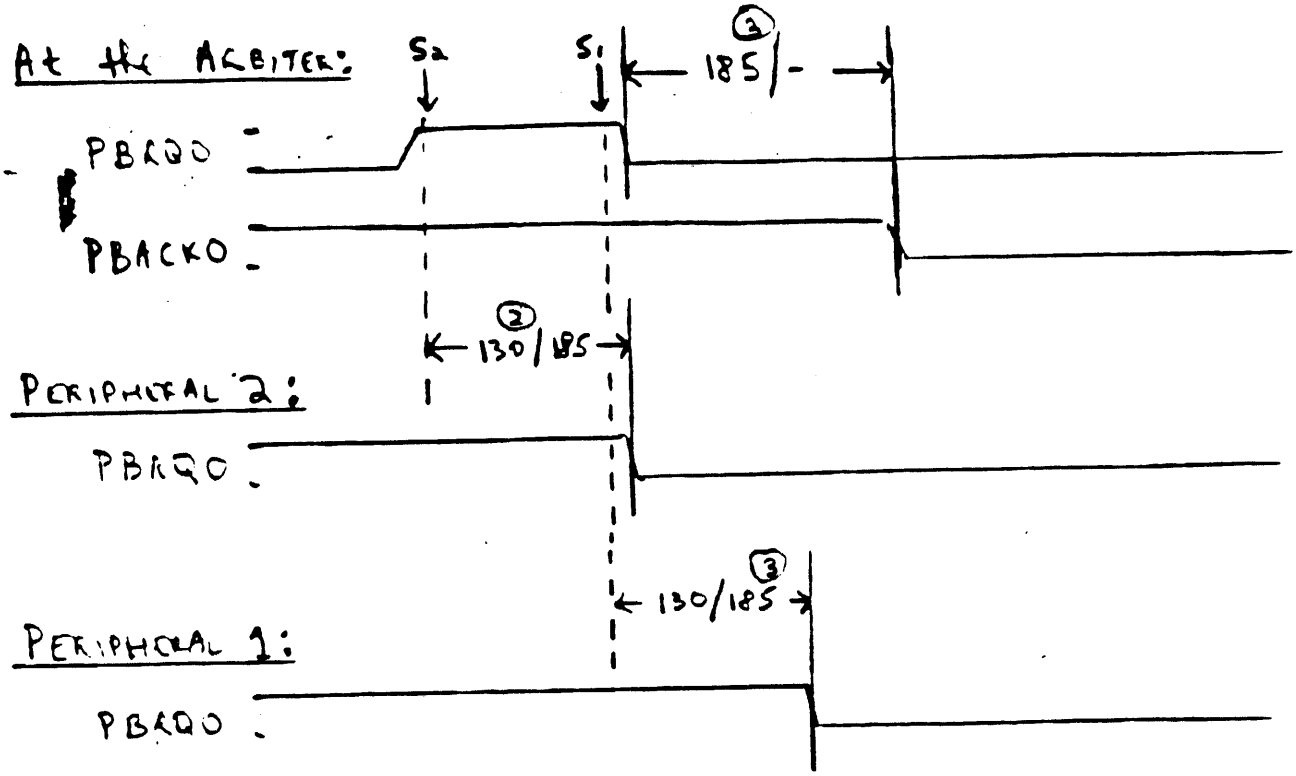
Figure 11b: TYPICAL 382 I/O BUS EXCHANGE



NOTES:

1. S_i ≙ INSTANCE WHEN PERIPHERAL i SAMPLED PBRQO INACTIVE FOR FIRST TIME.
2. PERIPHERAL MUST DELAY A MIN. OF 130 NSEC AFTER SAMPLING PBRQO TO ALLOW OTHER PERIPHERALS TIME TO SEE PBRQO INACTIVE.
3. PERIPHERAL MUST DRIVE PBRQO ACTIVE WITHIN 185 NSEC AFTER PBRQO GOES INACTIVE (i.e. BEFORE PBACKI= CAN ARRIVE.)

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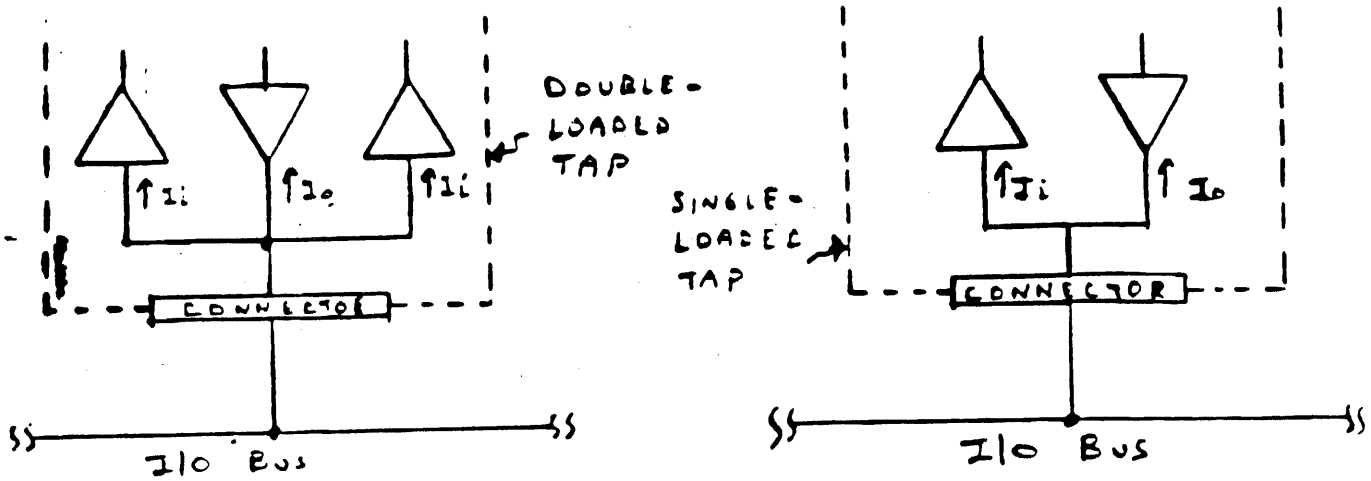
ISSUE FIGURE 11C	ENGR PMW / DRAWN 11 13/83	TITLE 3B2 I/O BUS PBRQO/PBACKO DAISY-CHAIN TIMING	BELL TELEPHONE LABORATORIES INCORPORATED / NO OF SHEETS THIS SET 3 / SHE

PERIPHERAL I/O BUS TAPS



A. CAPACITANCE PER PERIPHERAL TAP

ITEM	CAP. per ITEM (pf)	No. ITEMS	TOTAL CAP. PER TAP: SINGLE LOAD	TOTAL CAP. PER TAP: DOUBLE LOAD
INPUT BUFFER	2/5	1/2 (4)	2/5	4/10
OUTPUT (2) "	11/14	1 (4)	11/14	11/14
VIA	0.7	1/6	0.7/4.2	0.7/4.2
MLB ROUTING	2.4 per inch	1/6	2.4/14.4	2.4/14.4
EDGE CONN.	1/3	1	1/3	1/3
TOTAL			17.1/40.6	19.1/45.6

NOTES:

(1) CAPACITANCE & NO. ITEMS REPRESENTED AS MIN/MAX

(2) LS240 FAMILY USED TO SPECIFY OUTPUT CAP.

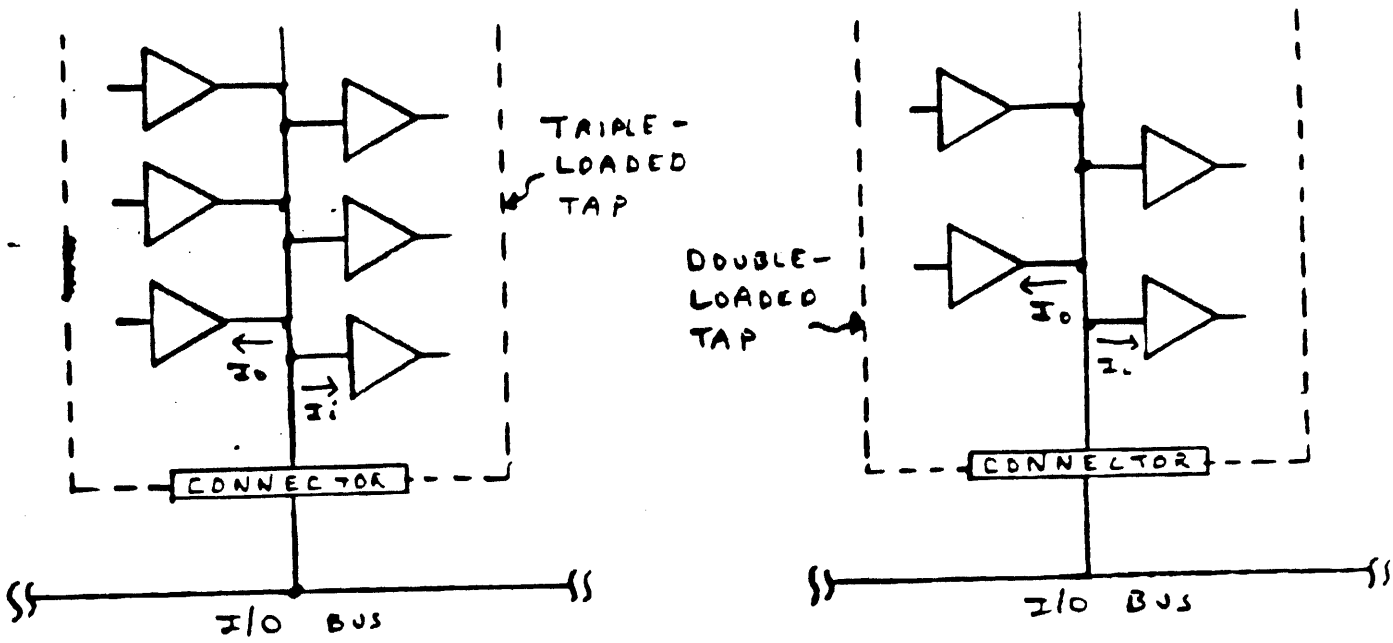
(3) CAP. VALUES ARE DESIGN WORST CASE.

(4) PERIPH. TAPS ARE ALLOWED 1 OR 2 INPUT LOADS PER TAP & ONLY 1 OUTPUT.

(cont.)

ISSUE	ERDR PMW	TITLE 3B2 I/O BUS ELECTRICAL MODEL	BELL TELEPHONE LABORATORIES INCORPORATED
FIGURE 12	DRAWN 1/10		NO OF SHEETS IN ENTRY: SHEET 1/3

SYSTEM BOARD I/O BUS TAPS



B. CAPACITANCE PER SYSTEM BOARD TAP

ITEM	CAP. PER ITEM (pf)	NO. ITEMS	TOTAL CAP. PER TAP	
			DOUBLE LOAD	TRIPLE LOAD
INPUT BUFFER	2 / 5	2 / 3 ④	4 / 10	6 / 15
OUTPUT ② "	11 / 14	2 / 3 ④	22 / 28	33 / 42
VIA	0.7	1 / 6	0.7 / 4.2	0.7 / 4.2
MLB ROUTING	2.4 pf per inch	1 / 8	2.4 / 19.2	2.4 / 19.2
EDGE CONN	1 / 3	1	1 / 3	1 / 3
TOTAL			30.1 / 644	43.1 / 83.4

NOTES:

① ~ ③ (See previous page)

④ SYSTEM BOARD TAPS ARE ALLOWED UP TO 2 OR 3 INPUT/OUTPUT LOADS PER TAP. (4 LOADS PERMITTED ON PALIS-0031)

(cont.)

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ISSUE	ENGR	TITLE	BELL TELEPHONE LABORATORIES INCORPORATED
FIGURE 12	PMW	3B2 I/O BUS ELECTRICAL MODEL	
	DRAWN 11/10/83		NO OF SHEETS PER SET 2/

ISSUE

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C. CAPACITANCE OF I/O EXPANSION BACKPLANE (3B2/40=)

ITEM	CAP. PER ITEM (pf)	NO. ITEMS	TOTAL CAP. (pf)
VIA	0.7	3 (max)	2.1
MLB ROUTING	2.4pf per inch	20" (max)	48
TOTAL			50 (max)

D. TOTAL CAPACITANCE OF FULLY LOADED BUS (3B2/4)

$C_{TOTAL} = (\#\text{ of periph. taps}) \cdot (\text{Cap/tap}) + (1\ \text{SBD tap})(\text{cap/tap}) + C_{BACKPLANE}$

a) 12 single-loaded periph w/ 1 double-loaded SBD tap.

$C_{TOTAL} = (12)(40.6) + (1)(64.4) + 50 \cong$ **600 pf**

b) 12 double-loaded periph. w/ 1 triple-loaded SBD tap

$C_{TOTAL} = (12)(45.6) + (1)(83.4) + 50 \cong$ **700 pf**

E. TIME-OF-FLIGHT (MAX.)

$T_{flight} \cong \frac{dT}{dc} \cdot C + T_{WIRE}$

a) $T_{flight} \cong (.065\ ^{①}\frac{ns}{pf})(600\,pf) + (.2\ \frac{ns}{in})(20") \cong$ **43 nsec**

b) $T_{flight} \cong (.052\ ^{②}\frac{ns}{pf})(700\,pf) + (.2\ \frac{ns}{in})(20") \cong$ **40 nsec**

① $\frac{dT}{dc}$ FOR S FAMILY = .065 ns/pf (WORST-CASE)

② $\frac{dT}{dc}$ FOR LS240 FAMILY = .052 ns/pf (WORST-CASE)

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ISSUE	ENGR	TITLE	BELL TELEPHONE LABORATORIES INCORPORATED
FIGURE 12	PMW	3B2 I/O BUS ELECTRICAL MODEL	NO OF SHEETS IN SET: 3
	DRAWN 11/10/83		

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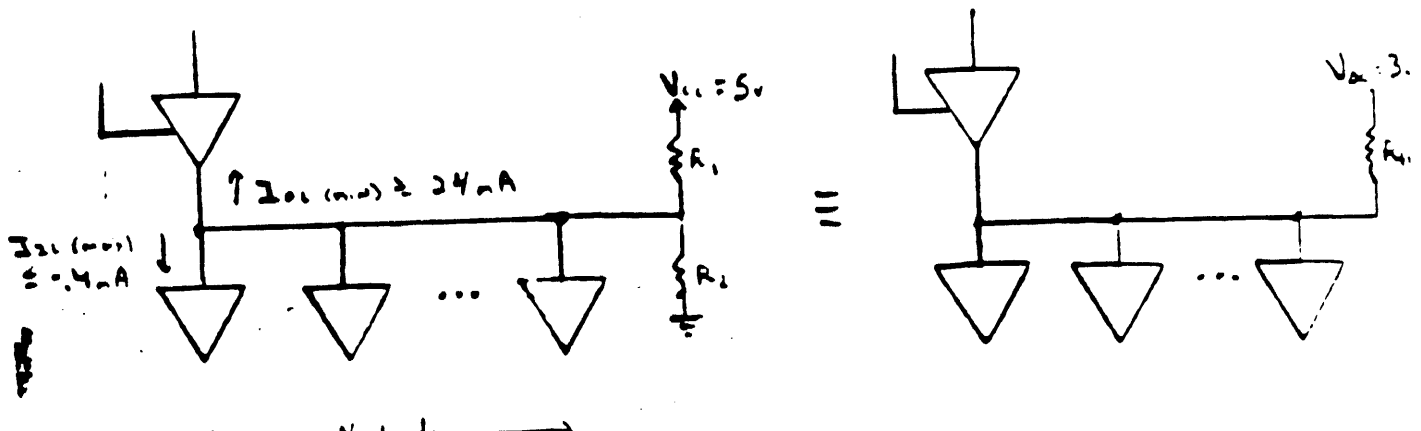

← N loads →

(1 or 2 loads per periph; 2 or 3 loads per sys. board)

1) COMPUTE R_{th}

$$R_{th} \geq \frac{V_{cc}}{I_{OL(min)} + N(.0004)} = \frac{3}{.024 - N(.0004)}$$

2) COMPUTE R_1 & R_2

a) $V_{oc} = V_{cc} \cdot \left(\frac{R_2}{R_1 + R_2}\right)$

$$3 = 5\left(\frac{R_2}{R_1 + R_2}\right)$$

b) $R_{th} = \frac{R_1 \cdot R_2}{R_1 + R_2}$

$\therefore$

$$\boxed{R_2 = \frac{5}{2} R_{th} \qquad R_1 = \frac{3}{2} R_2}$$

3) SOLVE FOR EACH 3B2 MODEL

	MODEL	N	$R_{th}(\Omega)$	$R_1(\Omega)$	$R_2(\Omega)$
4 periph →	302/300	11	153	255	383
12 periph →	302/400	27	227	379	568

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(cont.)

ISSUE	ENGR	TITLE	BELL TELEPHONE LABORATORIES INCORPORATED
FIGURE 13	PMW	CALCULATION OF TERMINATING R. (3B2 I/O BUS)	NO OF SHEETS PER SET: 1
	DRAWN 11/11/83		

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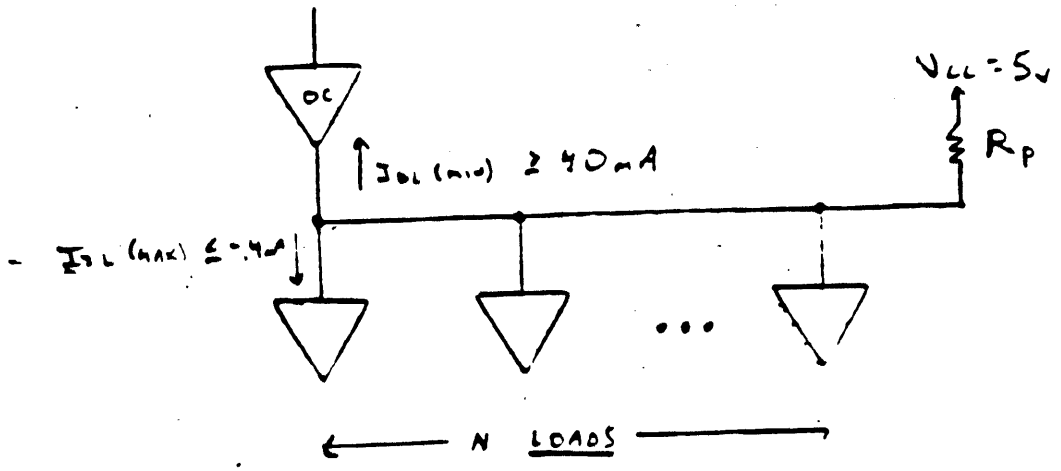
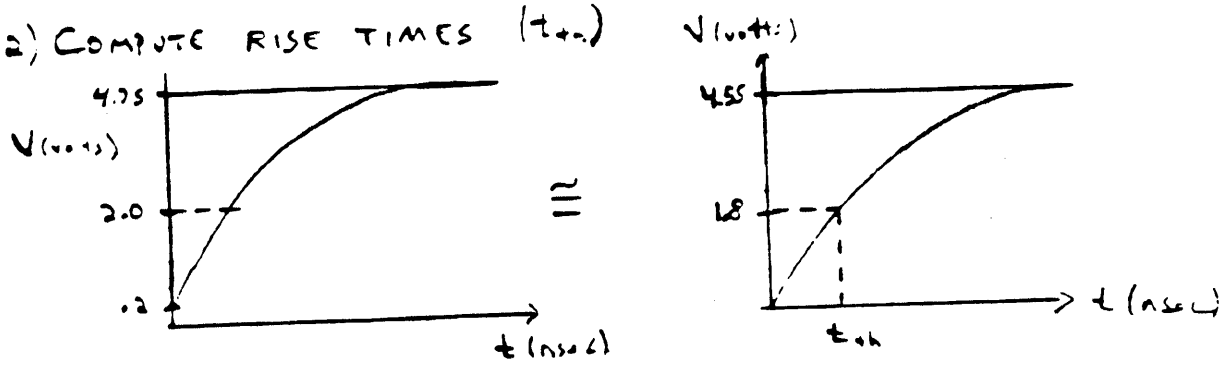
(Cont.)



1) COMPUTE R

$$R \geq \frac{VCC + 5\% \text{ of } VCC}{I_{OL(min)} + N \cdot I_{IL(max)}} = \frac{5.25}{I_{OL(min)} - N \cdot I_{IL(max)}}$$

2) COMPUTE RISE TIMES (t_{RH})



$$V_C = V_{applied(min)}\left(1 - e^{-\frac{t}{\tau}}\right)$$

$$1.8 = 4.55\left(1 - e^{-\frac{t_{RH}}{R_P C}}\right)$$

$$t_{RH} = .504 \cdot R_P C$$

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(Cont.)

ISSUE	ENGR	TITLE	BELL TELEPHONE LABORATORIES INCORPORATED
FIGURE 13	PMW	CALCULATION OF PULLUP R. (R_P) (3D2 =10 BUS)	SHEET 21
	DRAWN 11/23/83		NO OF SHEETS PER SET

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(cont.)

3) SOLVE FOR R AND t_{rk}

MODEL	MAX N_{taps}	MAX C (pf)	MIN I_{oL} (mA)	MAX I_{IL} (mA)	MIN R_p (Ω)	MAX t_{rise} (nsec)	Remarks: ①
3B2/100	N/A	N/A	N/A	N/A	N/A	N/A	–
3B2/200	N/A	N/A	N/A	N/A	N/A	N/A	–
3B2/300	11	315	40	.4	150	25	4 periph; dbl.
"	6	280	40	.4	140	20	" ; sgl.
3B2/400	27	700	40	.4	190	65	12 periph; dbl.
"	14	600	40	.4	150	45	" ; sgl.

NOTES:

① SOME OPEN COLLECTOR SIGNALS ARE LIMITED TO 1 INPUT LOAD PER PERIPH. TAP, INSTEAD OF 2. LIKEWISE, THESE SAME SIGNALS ARE LIMITED TO 2 I/O LOADS ON THE SYS. BOARD TAP, INSTEAD OF 3.

② FIGURE 12 COMPUTES CAPACITANCE PER TAP WITH THE FOLLOWING FORMULA:

$$C_{TOTAL} = (\#_{periph\ taps})(C/p.tap) + (1_{sys.tap})(C/s.$$
$$+ C_{backplane}$$

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ISSUE	ENGR	TITLE	BELL TELEPHONE LABORATORIES INCORPORATED
FIGURE 13	pmw	CALCULATION OF RISE TIMES (t_{rk}) (3B2 I/O BUS)	NO OF SHEETS PER SET
	DRAWN 11/23/83		

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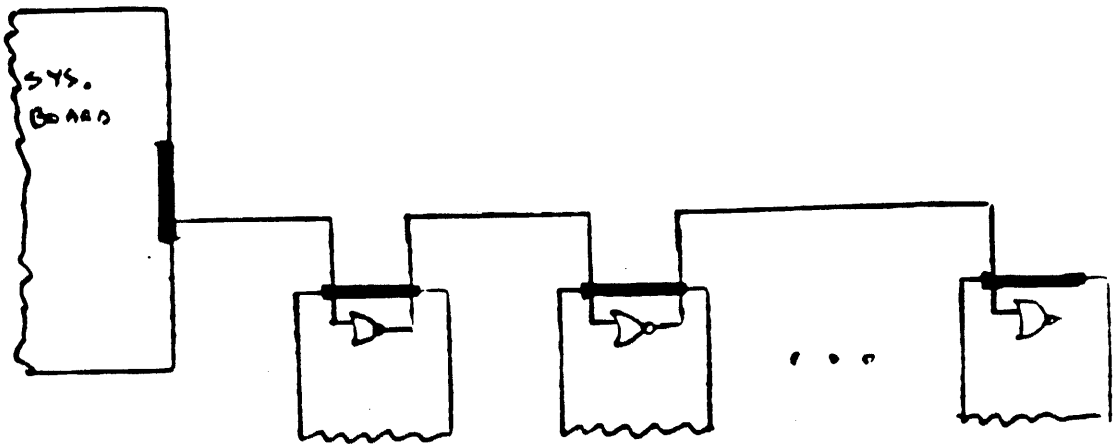

A. CAPACITANCE (max)

1. SYS. BOARD TO 1ST PERIPH. IN CHAIN

ITEM	pf (each)	pf (total)
• EDGE CONN.	3	6
• MLB ROUTING	2.4/in.	9.6
• MLB VIAS	.7	2.1
• PERIPH. INPUT BUFF	5	10
TOTAL		27.7

2. PERIPH. TO PERIPH.

27.7

B. SIGNAL PROPAGATION DELAY (MAX)

1. SYS BOARD TO 1ST PERIPH.

$$T_{SYS-Pi} = \frac{dT}{dC} \cdot C + T_{WIRE}$$

$$= (0.1)(27.7) + (.2\tfrac{ns}{in})\cdot(4'') \cong \underline{3.6 nsec}$$

2. PERIPH. TO PERIPH.

$$T_{Pi-Pj} = T_{INT(max)} + \frac{dT}{dC} \cdot C + T_{WIRE}$$

$$= [T_{spec(max)} \cdot 1.2 - 1.2] + \frac{dT}{dC} \cdot C + T_{WIRE}$$

$$= (5.5)(1.2) - 1.2 + (.09)(27.7) + (.2\tfrac{ns}{in})(4) \cong \underline{8.7}$$

PRIVATE

ISSUE	ENGR	TITLE	BELL TELEPHONE LABORATORIES INCORPORATED
FIGURE 14	PMW	DAISY-CHAIN PROPAGATION DELAY (3B2 310 BUS)	SHEET 11
	DRAWN 11/11/83		NO OF SHEETS PER SET

ISSUE

10

C. TOTAL DAISY-CHAIN PROPAGATION DELAY

$T_{DELAY} = T_{SYS-PI} + (N-1) \cdot T_{PI-PJ} = 3.6 + (N-1) \cdot 8.7$

where

N = # OF PERIPHERALS IN CHAIN

3B2 MODEL	N (MAX)	T_{DELAY} (nsec) (MAX)
300	4	30
400	12	100

NOTES:

1. CALCULATIONS WERE BASED ON:
   a) LS240 TYPE DRIVER ON SYSTEM BOARD
      $\frac{dt}{dc}$ = 0.1 nsec/pf for cap. < 50 pf
   b) 74S32 OR GATE ON EACH PERIPH.
      $\frac{dt}{dc}$ = .09 nsec/pf for cap. < 100pf

PRIVATE

ISSUE	ENGR	TITLE	BELL TELEPHONE LABORATORIES INCORPORATED
FIGURE 14	pmw	DAISY-CHAIN PROPAGATION DELAY (3B2 IIO BUS)	SHE
	DRAWN 11/11/83		NO. OF SHEETS PER SET 21

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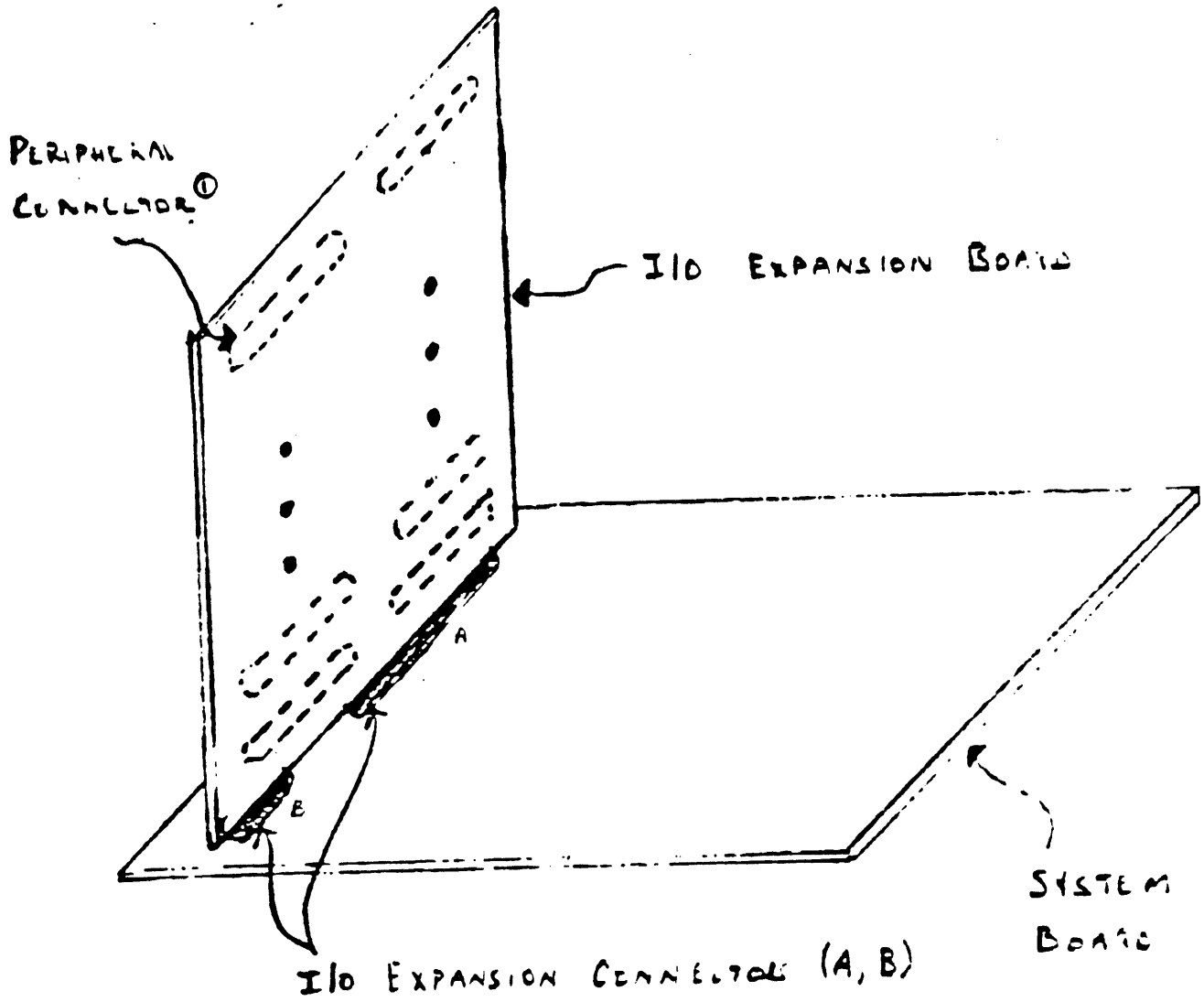
NOT DRAWN TO SCALE



① Number of PERIPHERAL CONNECTORS VARIES ACCORDING TO 382 MODEL:

MODEL	No. P-CONN.'s
100	N/A
200	N/A
300	4
400	12

PRIVATE

ISSUE	ENGR	TITLE	BELL TELEPHONE LABORATORIES INCORPORATED
FIGURE 15	PNW	382 I/O EXPANSION	NO OF SHEETS PER SET
	DRAWN 11/11/83		

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CM195 FAMILY

OPTION BOARD

10/31/89

HOLE CHART			
LETTER	SIZE	QTY	PLATE
UNMARKED	.038		P
A	.128	1	P
B	.156	3	N

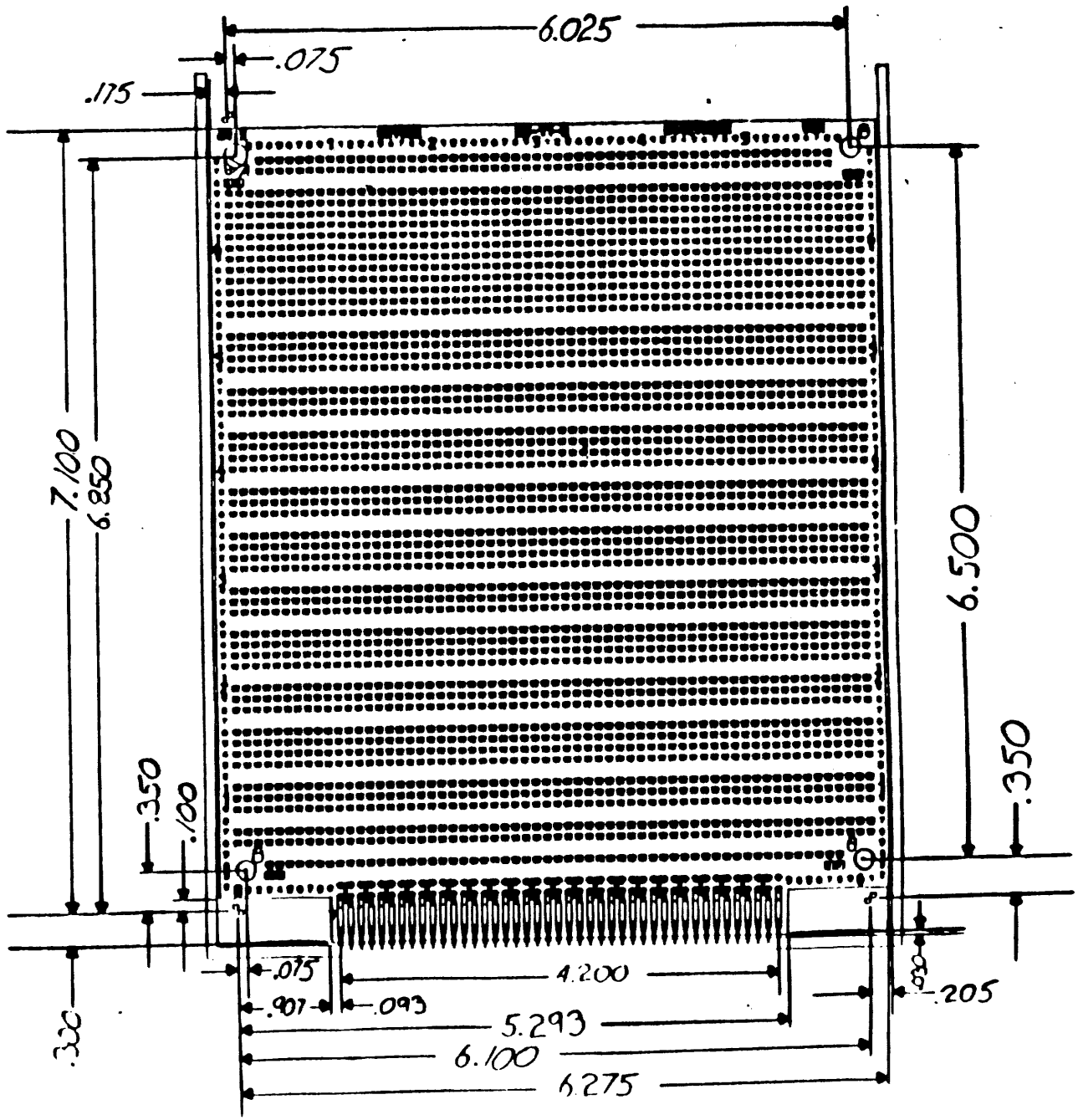
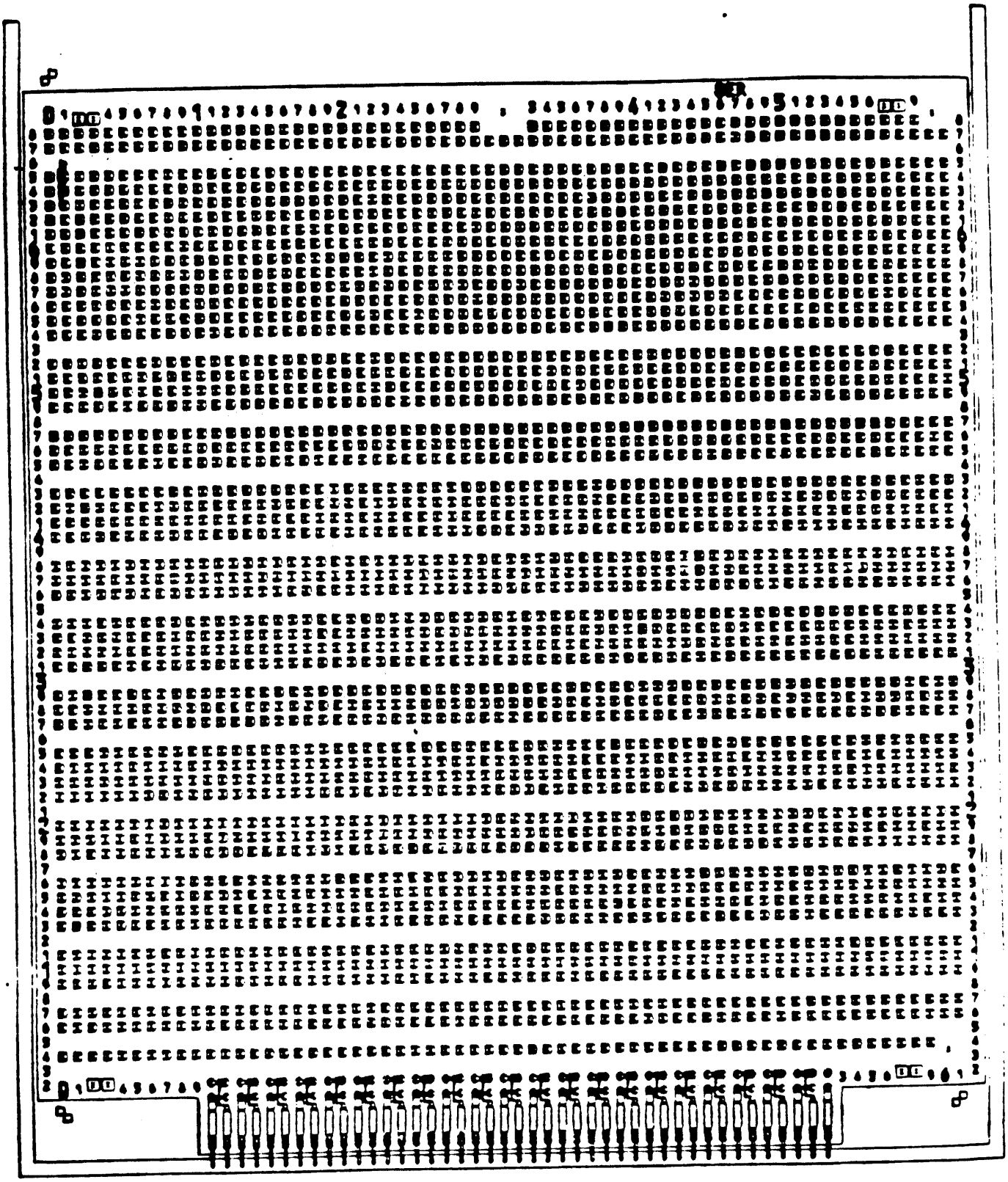


Figure 16e

195 FAMILY TOPOLOGY

6/29/83



COMPONENT SIDE VIEW

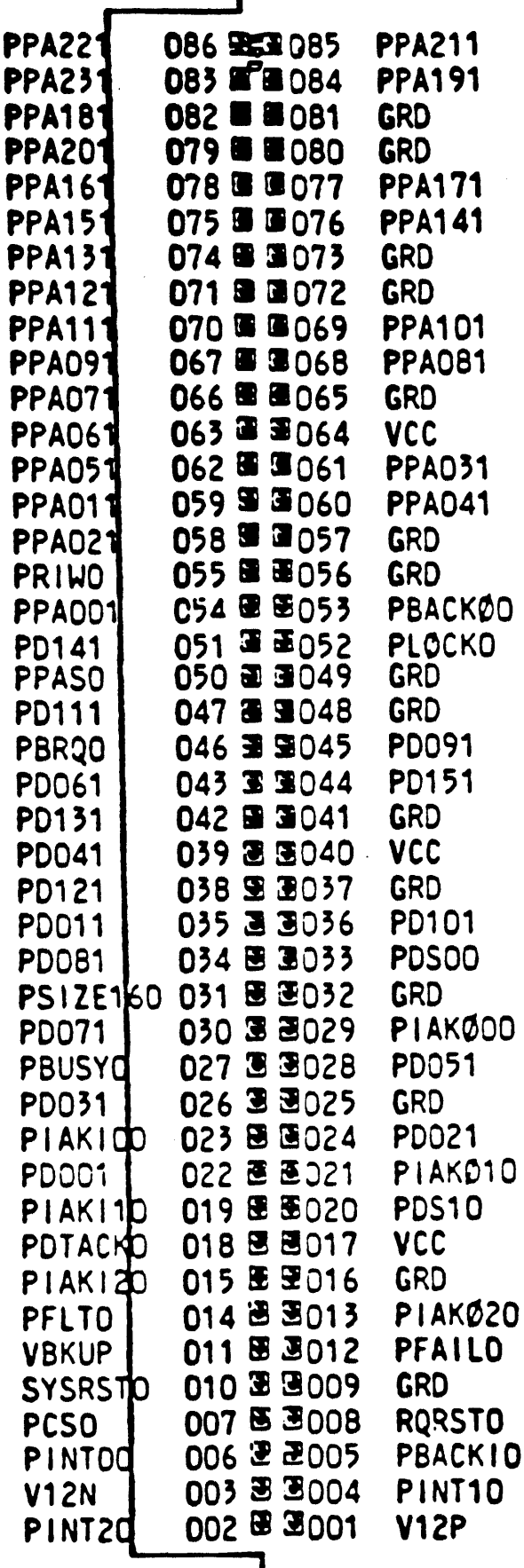
PRIVATE

FIGURE 166 21

FOR 195 FAMILY CODES

MRD
4-28-83

PRIVATE



COMPONENT SIDE VIEW
OF BOARD

NOTE: O=ZERO
O=OH