APPLICATION		A	REVISION		
NEXT ASSEMBLY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
		A	Release Per ECO #5730		

A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A													
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38

RECORD OF REVISION STATUS OF EACH SHEET

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES ANGLES ±

FRACTIONS ±

3 PLACE DECIMALS ±

2 PLACE DECIMALS ±

1 PLACE DECIMALS ±

MATERIAL:

CONTR NO.

DR	J. Aborn	1 30 89
CHK	Michalski	4 3 89
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APPROVED

BY DIRECTION OF

BBN Manufacturing Corporation

Billerica, MA

Drawing Title

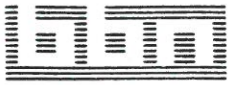
B2VME TCS Slave Functional Specification

Size		Drawing No.
A	63942	FS15022(

Scale

Sh 1 of 25

B2VME TCS Slave Processor Firmware Specification



1.1 Introduction

The B2VME is a Butterfly 2 processor card; it is also called a function card. The B2VME is equipped with a Butterfly 2 Test and Control System (TCS) Slave Processor, a Motorola 68HC11 single chip microcomputer. This programmed device implements master/slave communication and circuit board control defined in the *Butterfly 2 Technical Reference Guide*.

This document describes the commands defined for a B2VME slave Processor, BBN programmed part number 4615022G01.

1.2 TCS Messages

There are four types of TCS message:

- Register Access Request
- TBUS Memory Access Set-Up Request
- TBUS Memory Read Request
- TBUS Memory Write Request

1.2.1 Slave Addressing

The B2VME slave is initialized to broadcast group 0x04. The slave will carry out requests broadcast to this group, but will not respond. An EEPROM register defines the slave's group, so it may be modified during operation.

1.3 Register Access Messages

There are four types of register access message:

Action Registers — Action registers perform a sequence of actions on the target circuit card thus hiding board specific and 68HC11 details.

EEPROM Registers — EEPROM registers store board specific information in slave processor non-volatile memory.

Gate Array Registers — The gate array register messages access registers within the card's Switch Interface Gate Array (SIGA) and Level Converter Array (LCON).

Hardware Registers — Hardware write registers load board control registers. Hardware read registers monitor board status signals and data bits.

1.4 TBUS Messages

There are three types of memory message. All of them manipulate the SIGA to interface with the function card's Transaction bus (TBUS). See the SIGA functional specification and the TBUS functional specification for an explanation of all the registers involved.

Memory Access Set-Up — The memory set-up message initializes information to be used by a subsequent memory access message. It initializes the beginning address, and TBUS commands.

Memory Read — The memory read message returns the long word of data found in the memory location specified by the previous set-up message. The address may be optionally incremented for a subsequent memory access.

Memory Write — The memory write message loads a long word of data into the memory location specified by a previous set-up message. The address may be optionally incremented for a subsequent memory access.

1.4.1 TBUS Memory Set-Up Request

The TBUS Memory Setup Request initializes the SIGA for a memory access. ("P" in the diagrams below is message parity. Parity is the XNOR of the entire message.)

Memory Set-Up Request

bit: 8	7	6	5	4	3	2	1	0
1	P	MS_SLOT_ID						
0	LS_SLOT_ID							
0	CMD MOD				0	0	1	0
0	TBUS Command							
0	TBUS Command Modifier 1							
0	TBUS Command Modifier 0							
0	TBUS Addr<31..24>							
0	TBUS Addr<23..16>							
0	TBUS Addr<15..8>							
0	TBUS Addr<7..0>							

Positive Reply

1	MASTER ADDRESS	
0	P	0x05

Negative Reply

1	MASTER ADDRESS
0	NACK CODE

Memory Set-Up Message Format
Figure 1-1

1.4.2 TBUS Read Request

The TBUS Read Request returns data from a memory location specified by a previous set-up request.

The TBUS Read Request command modifier field contains an increment bit. If it is set, the Slave prepares for the next access when the current one completes.It increments the current TBUS address, then loads it into the SIGA. (See section 1.5 for the decoding of the message's command fields.)

TBUS Read Request

bit:	8	7	6	5	4	3	2	1	0
1	P	MS_SLOT_ID							
0	LS_SLOT_ID								
0	CMD MOD				0	0	0	0	

Positive Reply

1	MASTER ADDRESS	
0	P	0x07
0	TBUS Response	
0	TBUS Data<31..24>	
0	TBUS Data<23..16>	
0	TBUS Data<15..8>	
0	TBUS Data<7..0>	

Negative Reply

1	MASTER ADDRESS
0	NACK CODE

TBUS Read Message Format
Figure 1-2

1.4.3 TBUS Write Request

The TBUS Write Request loads its data into a destination specified by a preceding set-up request.

The TBUS Memory Write Request command modifier field includes an increment bit. If it is set, the address is incremented and loaded into the SIGA after the memory access completes. (See section 1.5 for the decoding of the message's command fields.)

TBUS Write Request

bit: 8	7	6	5	4	3	2	1	0
1	P	MS_SLOT_ID						
0	LS_SLOT_ID							
0	CMD MOD				0	0	0	1
0	TBUS Data<31..24>							
0	TBUS Data<23..16>							
0	TBUS Data<15..8>							
0	TBUS Data<7..0>							

Positive Reply

1	MASTER ADDRESS	
0	P	0x09
0	TBUS Response	

Negative Reply

1	MASTER ADDRESS
0	NACK CODE

TBUS Write Message Format
Figure 1-3

1.5 Command Byte Decoding

Cmd Type Value	Cmd Mod Value	Description
Memory Messages		
0	0	Maintain the same TBUS address
	8	Increment TBUS address after the read
1	0	Maintain the same TBUS address
	8	Increment TBUS address after the write
	1-7, 9-15	Illegal Commands
Memory Set-Up Message		
2,3	2	Use SIGA A for subsequent TBUS accesses
	3	Use SIGA B for subsequent TBUS accesses
	0, 1, 4-15	Illegal Commands
Register Access Messages		
Action Registers		
4	Don't Care	Action Register Read (See List of Action Registers)
5	Don't Care	Action Registers Write (See List of Action Registers)
EEPROM Registers		
6	Don't Care	EEPROM Register Read (See EEPROM Register List)
7	Don't Care	EEPROM Register Write (See EEPROM Register List)
Gate Array Registers		
8	0	Read LCON A Registers
	1	Read LCON B Registers
	2	Read SIGA A Registers
	3	Read SIGA B Registers
	4-15	Illegal Commands
9	0	Write LCON A Registers
	1	Write LCON B Registers
	2	Write SIGA A Registers
	3	Write SIGA B Registers
	4-15	Illegal Commands
Hardware Registers		
10	0	Read Hardware Register 0
	1	Read Hardware Register 1
	2	Read Hardware Register 2
	3	Read Hardware Register 3
	4-15	Illegal Commands
11	0	Write Hardware Register 0
	1	Write Hardware Register 1
	2-15	Illegal Commands

1.6 Action Register List

The TCS message's address byte selects which register is accessed.

The TCS message's data byte is unused in the read message, and conveys write data in the write message.

Reg. Number		Description	Read/Write
0	(0x00)	Board Status Register	(read only)
1	(0x01)	Card Control Register	(write only)
2	(0x02)	Power Control Register	(write only)
3	(0x03)	Previous ACK/NACK	(read only)
4	(0x04)	Clock Activity Check Register	(read only)
5	(0x05)	EEPROM Write Enable	(write only)
6	(0x06)	Board Ambient Temperature	(read only)
7	(0x07)	Test RAM	(read/write)
8	(0x08)	Slave Address Re-Read Command	(write only)
9	(0x09)	TCS +5 VDC Voltage Level	(read only)
10	(0x0A)	+5 VDC Voltage Level (Vcc)	(read only)
11	(0x0B)	-5.2 VDC Voltage Level (Vee)	(read only)
12	(0x0C)	Illegal Command	(n/a)
13	(0x0D)	LED Control	(write only)
14	(0x10)	Switch Signal Duty Cycle Detect	(read/write)
15	(0x0F)	Last TBUS Response	(read only)

1.7 EEPROM Register List

Reg. Number		Description	Read/Write
0	(0x00)	Card Type	(read/write)
1-16	(0x01-10)	Serial Number	(read/write)
17,18	(0x11,12)	Artwork Revision Level	(read/write)
19,20	(0x13,14)	Electrical Revision Level	(read/write)
21,22	(0x15,16)	TCS Slave Code Revision Level	(read/write)
23	(0x17)	Temperature Alarm Setpoint	(read/write)
24	(0x18)	TBUS Timeout MSB	(read/write)
25	(0x19)	TBUS Timeout LSB	(read/write)
26	(0x1A)	+5 VDC A/D Nominal Reading	(read/write)
27	(0x1B)	+5 VDC Alarm Magnitude	(read/write)
28	(0x1C)	TCS +5 VDC Nominal Reading	(read/write)
29	(0x1D)	TCS +5 VDC Alarm Magnitude	(read/write)
30	(0x1E)	-5.2 VDC A/D Nominal Reading	(read/write)
31	(0x1F)	-5.2 VDC Alarm Magnitude	(read/write)
32	(0x20)	Board Broadcast Group ID	(read/write)

1.8 Hardware Register List

Hardware registers are selected with the TCS message command modifier field. The message's address byte is not used.

Reg. Number		Description	Read/Write
Write Registers			
0	(0x00)	Power Control	(write only)
1	(0x01)	Reset Control and LED	(write only)
Read Hardware Registers			
0	(0x00)	Rack ID<3> and Status	(read only)
1	(0x01)	Rack ID<2..0> and Panel ID<1>	(read only)
2	(0x02)	Slot ID<2..0> and Panel ID<0>	(read only)
3	(0x03)	Card Type	(read only)

1.9 Gate Array Register List and Definitions

Registers within the SIGAs and LCONs are accessed using gate array register messages.

The gate array access message defines the TCS message fields as follows:

Command Type:	Specifies a read or a write
Command Modifier:	Specifies which gate array to access
Address Byte:	Specifies which register within the gate array to access
Data Byte:	Ignored

The decoding of the command type and modifier is as follows:

Command Type 8, Gate Array Read

Command Modifiers:		
	0	Read LCON A Registers
	1	Read LCON B Registers
	2	Read SIGA A Registers
	3	Read SIGA B Registers
	4-15	Illegal Commands

Command Type 9, Gate Array Write

Command Modifiers:		
	0	Write LCON A Registers
	1	Write LCON B Registers
	2	Write SIGA A Registers
	3	Write SIGA B Registers
	4-15	Illegal Commands

1.9.1 SIGA Internal Registers

The SIGA registers are presented to the master processor in the following registers. For complete descriptions of their operation see the *Butterfly 2 Technical Reference Guide* TBUS Chapter and the *SIGA Functional Specification*.

Address	Register Definition
0X0	R W Data bits <7..0>
0X1	R W Data bits <15..8>
0X2	R W Data bits <23..16>
0X3	R W Data bits <31..24>
0X4	TBUS Address <7..0>
0X5	TBUS Address <15..8>
0X6	TBUS Address <23..16>
0X7	TBUS Address <31..24>
0X8	TBUS Response
0X9	TBUS Command
0XA	TBUS Command Modifier 0
0XB	TBUS Command Modifier 1
0XC	CSL Address <7..0>
0XD	CSL Address <8>
0XE	Unused
0XF	Unused

TBUS Response Register

NDONE	Drive_AD	T_Driven	M_Par_ Err	Read Data<32> (Stolen)	T_RR <2>	T_RR <1>	T_RR <0>

TBUS Command Register

Addr <33>	Addr <32>	T_Size <2>	T_Size <1>	T_Size <0>	T_RR <2>	T_RR <1>	T_RR <0>

TBUS Command Modifier 0 Register

Spare	Spare	Spare	Spare	Write Data<32> (Stolen)	T_Path <2>	T_Path <1>	T_Path <0>

TBUS Command Modifier 1 Register

T_Sync	T_Priority <1>	T_Priority <0>	T_Lockop <1>	T_Lockop <0>	T_Source <2>	T_Source <1>	T_Source <0>

CSU Low Address Register

CSU Address <7..0>

CSU High Address Register

Spare	Spare	Spare	Spare	Spare	Spare	Spare	CSU Addr <8>

1.9.2 LCON Internal Registers

There are three classes of LCON internal register. Those that control the state of the LCON, those that assert LCON signals, and those that monitor LCON pins.

LCON Control Registers (Write Only)

The LCON is enabled and reset with a series of registers. The register address determines the action taken. The actions enumerated in the bit definitions below can be combined in the address byte as desired (except for reset). For example, to enable the requester, server and tri-state clock with a single register access, write the register: 00xx1110.To disable all three write the register: 00xx0000. To enable just the requester portion of the LCON, write the register: 00xx0010. To issue a reset, write the register: 00xx0001.

Note: It is forbidden to issue a reset in conjunction with any of the enable signals. These controls are mutually exclusive.

LCON Control Register Address Byte

Always Zero	Always Zero	Don't Care	Don't Care	Tri-State Enable	Server Enable	Requestor Enable	Reset

LCON Signal Monitoring Register Addresses (Read Only)

The following registers read the state of the indicated signals and return a one bit value in Data<0> of the response message.

These registers are primarily meant to read the state of static signals. Some of the signals enumerated below constantly change during normal Butterfly 2 operation. A read of their "static" value yields a probabalistic result.

Address	Description
0x40	Read tri-state clock enable
0x41	Read requester clock divided by 64 (625 kHz)
0x42	Read server clock divided by 64 (625 kHz)
0x43	Read 65 ms pulse divided by 2 (7.69 Hz)
0x44-4F	Unused
0x50-57	Read server ECL data bits 0-7
0x58	Read requester reverse
0x59	Read server frame
0x5A	Read system net-time
0x5B	Read function board net-time
0x5C	Read revision level bit <0>
0x5D	Read revision level bit <1>
0x5E	Read requester enable
0x5F	Read server enable

LCON Signal Assertion Registers Addresses (write only)

Address	Description
0x60	Assert Requester ECL data bit <0>
0x61	Assert Requester ECL data bit <1>
0x62	Assert Requester ECL data bit <2>
0x63	Assert Requester ECL data bit <3>
0x64	Assert Requester ECL data bit <4>
0x65	Assert Requester ECL data bit <5>
0x66	Assert Requester ECL data bit <6>
0x67	Assert Requester ECL data bit <7>
0x68	Assert Requester Frame
0x69	Assert Server Reverse
0x6A-6F	Unused

1.10 Action Register Definitions

Action Register 0, Board Status (read only)

Temp Okay	Spare	Power Okay	Spare	Broad-cast Error	Dead CPU	Serial Comm. Error	Slave Proc. Error

Temp Okay
: Temperature okay. Indicates that the board's temperature is below the value set in the slaves EEPROM temperature alarm register. Note: The slave turns board power off if the temperature ever exceeds the alarm setpoint. If the slave detects an over temperature state, this register must be read to set "temp okay" back to one.

Power Okay
: Indicates that the board's power supplies are generating voltages within the range specified in the slave's EEPROM registers. If Vcc ever strays out of the specified range for more than a second or so, the slave shuts off the board power. This is primarily intended to turn off the board's power control circuitry in the event that bulk power to the circuit card turns off. This prevents a large power supply surge current if bulk power is reapplied. If this bit is cleared by the slave, the status register must be read to clear the error condition.

Broadcast Error
: Indicates that a broadcast message to this slave has resulted in a negative acknowledgement since the last time the status register was read. This bit is cleared by reading the status register.

Dead CPU
: A zero in this bit indicates that the B2VME's CPU has taken an interrupt since the last read of the status register.

Serial Comm. Error
: Indicates that a receiver serial communications error was detected by the slave's serial communication hardware since the last read of the status register. Note: The slave does not execute the command requested by a TCS message with a serial communications error. This bit is cleared by a read of the status register.

Slave Processor Error
: Indicates that the slave processor software entered an illegal state since the last time the status register was read. If this bit is set, either the slave processor must be replaced, or there is a bug in the slave software.

Action Register 1, Control Register (write only)

Spare	Spare	Spare	Spare	Select TCS Bus B	Spare	CPU Reset	Card Reset

Select TCS Bus B
Writing a one to this bit selects TCS bus B for TCS communication. Writing a zero selects bus A.

CPU Reset
Writing a one to this bit holds the B2VME's CPU reset.

Card Reset
Writing a one to this bit holds the SIGAs' and the board's reset wires asserted.

Action Register 2, Power Control Register (write only)

Spare	Spare	Spare	Spare	Power Margin Level<1>	Power Margin Level<0>	Power Margin Enable	Power On

NOTE: The B2VME slave monitors the board's Vcc levels. If the voltage ever deviates from the range defined by the slave's EEPROM registers for more than a second or so, the slave turns the board power off and signals "power not okay" in the board status register.

Power Margin Level<1..0>
Selects the voltage level that the board's power supplies are set to when margining is enabled.

00 = -10%
01 = -5%
10 = +5%
11 = +10%

Power Margin Enable
Sets the board's power supplies to the voltage level selected by the power margin level bits.

Power On
Turns the board power supplies on. Note: The slave will only turn power on in response to an individually addressed message, never a broadcast message.

Action Register 3. Previous Message Ack/Nack (read only)

This register always contains the Ack Nack byte of the previous TCS message. Reading this register clears it.

Spare	Ack Nack Code<5>	Ack Nack Code<4>	Ack Nack Code<3>	Ack Nack Code<2>	Ack Nack Code<1>	Ack Nack Code<0>	Ack Bit

Ack/Nack Code<5..0>
This is an acknowledgment code for TCS messages. It is either a positive or negative acknowledgment depending on the sense of the Ack bit in this register.

Nack codes
0 - Null Description
1 - Timeout
2 - Parity Error
3 - Serial Communication Error
4 - Spare
5 - TCS Message Format Error

Ack Codes
0 - Action Register Acknowledge
1 - EEPROM Register Acknowledge
2 - Setup Message Acknowledge
3 - Memory Read Message Acknowledge
4 - Memory Write Message Acknowledge
5 - Gate Array Register Acknowledge
6 - Hardware Register Acknowledge

Ack Bit
A one in this bit indicates that the code is an acknowledgment.

Action Register 4. Clock Check (read only)

A one in this register indicates that low to high transitions were detected on corresponding clock signals.

Each clock checked by this register is monitored for a fixed period of time looking for low to high transitions. The monitoring periods are the following:

Server Clock	1 msec
Requestor Clock	1 msec
System Net Time	1 msec
My Net Time	1 msec
65 Msec Clock	150 msec

These add up to 154 msec. The master must take into account the time that the slave takes to respond to this action register.

Note: Reading this register uses the LCON to monitor clock signals. Any preceding LCON signal assertion commands (writes to the LCON signal assertion registers) are nullified by a read of this register.

Spare	Spare	Server Clock	Requestor Clock	System Net Time	My Net Time	Spare	65 msec
		1	1		1	1	1

Action Register 5. EEPROM Access Enable (write only)

Writing this register with any data enables an EEPROM register write on the next access. This register must be written before each EEPROM write, otherwise a format nack is returned in response to the write request.

Action Register 6. Board Ambient Temperature (read only)

This register returns the board's ambient temperature at 0.977 °F per tick.

Action Register 7. RAM Test Register (read write)

This register is one byte of slave processor read write RAM for testing communication with the TCS Master; anything may be written into it.

Action Register 8. Re-Read Slave Address (write only)

Writing this register with any data requests the slave to re-read its rack and midplane number, and to re-initialize its TCS bus address.

Action Register 9. TCS Vcc Voltage Sensor (read only)

This register returns the voltage detected on the TCS Vcc power supply at 24.4 mv per tick. Voltage is calculated with the following formula:

Millivolts = (register value)*(24.4 mv/tick)

Action Register 10. Vcc Voltage Sensor (read only)

This register returns the voltage detected on the board's Vcc power supply at 24.4 mv per tick. Voltage is calculated with the following formula:

Millivolts = (register value)*(24.4 mv/tick)

Action Register 11. Vee Voltage Sensor (read only)

This register returns the voltage detected at the board's -5.2 VDC supply. The value is calculated with the following formula:

Millivolts = (register value)*(34.8 mV per tick) - 6400 mv

Action Register 12. Illegal Register (n/a)

This registers returns a message format negative acknowledgement.

Action Register 13. LED Control (write only)

This register controls the board's indicator LED. Note: The LED is turned on by the board's power on reset. It is left on until instructed otherwise by the master processor.

Writing the following values to the LED control register results in the described LED state:

0 - LED off
1 - LED flash at 1 Hz
2 - LED flash at 3 Hz
3 - LED constant on
4-255 - Not Defined

Action Register 14, Switch Signal Duty Cycle Monitor (read/write)

This register measures the fraction of time that selected switch signals are in the high state. The LCON is used to monitor one of the signals and present it to the slave processor. The slave samples the signal's state 1020 times over an 11 millisecond monitoring period and averages the results to normalize them into an eight bit number. E.g. an action register 14 value of 0x0 indicates the signal was low for the entire 11 ms, a value of 0x7F indicates the signal was high for half the time, and a value of 0xFF indicates the signal was high the entire time.

The averaging calculation does not obscure a single high sample. The averaging consists of a divide by 4. The sample count is initialized to 3, so a single high sample results is an answer of 1.

The register is written with a data value that indicates which of the signals accessible to the LCON the register monitors. These values are the LCON monitoring register addresses:

Address	Description
0x40	Read tri-state clock enable
0x41	Read requester clock divided by 64 (≈25 kHz)
0x42	Read server clock divided by 64 (≈25 kHz)
0x43	Read 65 ms pulse divided by 2 (≈7.69 Hz)
0x44-4F	Unused
0x50-57	Read server ECL data bits 0-7
0x58	Read requester reverse
0x59	Read server frame
0x5A	Read system net-time
0x5B	Read function board net-time
0x5C	Read revision level bit <0>
0x5D	Read revision level bit <1>
0x5E	Read requester enable
0x5F	Read server enable

Writes to this register initiate signal monitoring and return a result, reads cause no monitoring, but return (again) the result from the previous write. This is intended to allow broadcast writes, which send no response to the master, to simultaneously monitor selected signals. Results of the broadcast write can be read back later one by one.

Note: Accessing this register nullifies any bit assertion commands previously sent to the LCON via a gate array access message. LCON A is used to monitor the signals. LCON B can optionally be used by writing the register with a one in the command modifier field of the message.

Action Register 15. Last TBUS Response (read only)

This register returns the value of the TBUS response register for the last TBUS access made.

1.11 EEPROM Register Definitions

Slave EEPROM writes take about 20 ms to complete. The Master processor must take into account the long time it takes for the Slave to acknowledge these messages.

The TCS message address byte is the EEPROM register number. The data byte is unused in the read message, and conveys data to be written in the write message.

All EEPROM registers are read/write.

EEPROM Register 0. Card Type

A one byte register allocated for storing the card type. The card type is an ASCII character.

EEPROM Registers 1-16. Board Serial Number

Board serial number registers. This is a block of 16 bytes allocated for storing the BBN board serial number in ASCII format. The least significant character is in register 1.

EEPROM Registers 17 and 18. Artwork Revision Level

Revision level of the printed circuit board part of the board assembly. These registers hold two ASCII characters that represent the revision level of the circuit card. The least significant character is in register 17.

EEPROM Registers 19 and 20. Electrical Revision Level

The revision level of the circuitry of the circuit board. This is used to keep track of the implementation of Engineering Change Orders (ECOs) on the circuit card. These registers hold two ASCII characters that represent the electrical revision level of the circuit card. The least significant character is in register 19.

EEPROM Registers 21 and 22. Slave Software Revision Level

Revision level of the firmware in the 68HC11. This is a two character alphanumeric value. The least significant character is in register 21.

EEPROM Register 23. Temperature Alarm Setpoint

This register contains the analog to digital converter reading at which the slave considers the board too hot. At this value the slave shuts off board power and flags temperature error in the board status register. The units of this register are the same as for the temperature sensor action register: 0.977 °F per tick.

EEPROM Register 24. TBUS Access Timeout Value Most Significant Byte

This register is the most significant byte of the 16 bit timeout value for TBUS accesses. If the SIGA's "done" bit is not asserted in response to a TBUS access within this time, a timeout nack is returned to the master. This register has units of 1.024 milliseconds per tick.

EEPROM Register 25. TBUS Access Timeout Value Least Significant Byte

This register is the least significant byte of the 16 bit timeout value for TBUS accesses. This register has units of 4 microseconds per tick.

EEPROM Register 26. Vcc A D Converter Nominal Reading

This register stores the analog to digital converter reading that results when Vcc power supply is at 5.00 VDC. This register is programmed at the factory, and is referenced by the TCS master processor when reading the TCS Vcc voltage sensing register to calibrate the results for analog component tolerances. The register's units are the same as those of the Vcc voltage sensing action register, 24.4 mV per tick.

EEPROM Register 27. Vcc Alarm magnitude

This register contains the Vcc deviation from nominal that signals a voltage error in the status register. The register's units are the same as those of the Vcc voltage sensing action register, 24.4 mV per tick. Note: Vcc deviation from specified range results in board shut down.

EEPROM Register 28. TCS Vcc A/D Converter Nominal Reading

This register stores the analog to digital converter reading that results when TCS Vcc power supply is at 5.00 VDC. This register is programmed at the factory, and is referenced by the TCS master processor when reading the TCS Vcc voltage sensing register to calibrate the results for analog component tolerances. The register's units are the same as those of the Vcc voltage sensing action register, 24.4 mV per tick.

EEPROM Register 29. TCS Vcc Alarm magnitude

This register contains the Vcc deviation from nominal that signals a voltage error in the status register. The register's units are the same as those of the Vcc voltage sensing action register, 24.4 mV per tick.

EEPROM Register 30. Vee A/D Converter Nominal Reading

This register stores the analog to digital converter reading that results when Vee power supply is at -5.2 VDC. The register's units are the same as those of the Vee voltage sensing action register, 34.8 mV per tick.

EEPROM Register 31. Vee Alarm magnitude

This register contains the Vee deviation from nominal that signals a voltage error in the status register. The register's units are the same as those of the Vcc voltage sensing action register, 34.8 mV per tick.

EEPROM Register 32. Board Broadcast Group ID

This register is the group identifier for broadcast message. The message processing code compares the least significant address byte of broadcast TCS messages to this register. If the address matches, the message is executed by the slave.

1.12 Hardware Register Definitions

The hardware registers are the raw board registers the slave controls. All hardware registers are either write only or read only.

TCS messages select between hardware registers with the command modifier field of the command byte.

The address byte is unused.

The data byte specifies any write data.

Write Register 0. Power Control Register (write only)

Spare	Power Enable	Spare	Spare	Spare	Voltage marg<1>	Voltage marg<0>	Voltage Margin Disable

Power Enable
Turns on the board's power supply.

Voltage Margin <1..0>
These bits select the margin level that power supplies go to when margining is enabled.

Voltage Margin Disable
Clearing this bit connects voltage trimming resistors to the board's power supply voltage trimming circuitry via an analog multiplexor.

Write Register 1, Reset and LED Control (write only)

SIGA A Reset	SIGA B Reset	Small Machine	Preset Dead CPU*	CPU Reset	Board Reset	Oscillator Select*	LED Off

SIGA A Reset
Writing a one to this bit asserts and holds the A SIGA reset line.

SIGA B Reset
Writing a one to this bit asserts and holds the B SIGA reset line.

Small Machine
Writing a one to this bit tells the boards address decoding logic that this board is in a machine with 64 slots or fewer.

Preset Dead CPU
This bit is connected to the preset line of a flip flop. Writing a zero to this bit sets the flip flop. This flip flop is cleared whenever the processor takes an interrupt, it thus can be used to detect that the processor is running. This bit is used by the status action register.

CPU Reset
Writing a one to this bit holds the processor reset; a zero releases it.

Board Reset
Writing a one to this bit holds the board reset; a zero releases it.

Oscillator Select*
Writing a zero to this bit selects an on board oscillator to run the board; a one selects an LCON buffered version of requestor clock.

LED Off
This bit controls the board's indicator LED. A zero turns it on. Note: This bit is meant to be controlled by the slave, not the master.

1.12.1 Read Register Definitions

Read Register 0 (read only)

No Connect	No Connect	No Connect	No Connect	Spare, Reads One	Spare, Reads One	Spare, Reads One	Rack ID<3>

No Connect
Undefined.

Spares
These are pulled up to a logical one.

Rack ID<3>
This is the most significant bit of the 4 bit rack number for this slave. This bit is read off of the midplane where it is set with DIP switches.

Read Register 1 (read only)

No Connect	No Connect	No Connect	No Connect	Rack ID<2>	Rack ID<1>	Rack ID<0>	Mid-plane ID<1>

No Connect
Undefined.

Rack ID<2..0>
These are the three least significant bits of the 4 bit rack number for this slave. These bits are read off of the midplane where they are set with DIP switches.

Midplane ID<1>
This is the most significant bit of the two bit midplane number. This bit is read off of the midplane where it is set with DIP switches.

Read Register 2 (read only)

No Connect	No Connect	No Connect	No Connect	Mid-plane ID<0>	Spare. Reads One	Spare. Reads One	Spare. Reads One

Midplane ID<0>
This is the least significant bit of the two bit midplane number. This bit is read off of the midplane where it is set with DIP switches.

Spares
These are pulled up to a logical one.

Read Register 3 (read only)

No Connect	No Connect	No Connect	No Connect	Card Type<3>	Card Type<2>	Card Type<1>	Card Type<0>

Card Type <3..0>
This is the board card type set with pull ups and pull downs on the board. For the B2VME this register reads "4"