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ABSTRACT and CONTENTS

This document specifies the special functions and branch conditions in the standard microprocessors.

Branch Conditions

Ø	Never branch
1	Always branch
2	X= Ø
3	X≠ Ø
4	X<Ø
5	X≥Ø
6	X>Ø
7	Y≥ Ø
1Ø	Y<Ø
11	RØ<Ø
12	RØ≥Ø
13	X≤Ø
14	X'∧777777B = Ø (X(6) - X(23) = 777777B)
15	X'∧777777B ≠ Ø (X(6) - X(23) ≠ 777777B)
16	Z≥Ø
17	Z<Ø
2Ø	Always branch
21	Y∧7≠Ø (Y(23)∨Y(22)∨Y(21)= 1)
22	BL=Ø
23	BL≠Ø
24	Y(23) = Ø
25	Y(23) ≠ Ø

Branch Conditions - 2

26	Attention latch 1 = Ø (also resets the latch)
27	(RSLAT 1 = Ø)∨(RSLAT2 = Ø)
3Ø	Protect ≠ X
31	RSLAT2 = Ø
32	Special flag A = Ø
33	Special flag A ≠ Ø
34	Attention latch 2 = Ø
35	Attention latch 3 = Ø
36	Attention latch 1 ≠ Ø
37	Undecoded
4Ø	undefined
41	undefined
42	Local memory parity error = 1 (resets the latch)
43	undefined
44	Central memory parity error = 1 (resets the latch)
45	breakpoint ≠ Ø

Rows 34–36: Also resets the latch

Special Conditions

Ø	No activity
1	LCY 1
2	LCY 2
3	LCY 3
4	LCY 4
5	LCY 8
6	LCY 12
7	LCY 16
1Ø	LCY 2Ø
11	LCL Z (CCFZA)
12	LCH Z (CCFZB)
13	SKZ - Reference scratchpad with address in Z (SPFZ)
14	ALERT
15	POT
16	PIN
17	Request Strobe #1
2Ø	Unprotect
21	Unusable
22	Load memory request priority field (LPF)
23	Reset Request Strobe latch #1 (Occurs at end of instruction)
24	Reset Central Memory Request (Local & Central Memory)
25	Request Protect

Special Conditions - 2

26	Reset T.U. (or other device attached to I/O connector)	
27	undecoded	
3Ø	Set special flag A	Occurs at end of instruction
31	Reset special flag A	
32	Reset Request Strobe Latch #2	
33	Request Strobe #2	
34	undefined	
35	undecoded	
36	undecoded	
37	undecoded	
4Ø	Release	Memory Reference
41	Prestore	
42	Store	
43	Store & Hold	
44	Fetch	
45	Fetch & Hold	
47	Prefetch	
6Ø	Set Bank B	
61	Set Bank A	
62	Clear all CPU Maps	
64	Fetch	ODDWORD FETCH
65	Fetch & Hold	

Undefined means that the signal is brought off the card in the low true sense to be used as a special function if needed or, in the case of branch conditions, an input to the branch condition gate is brought to a pin for use if needed.

Undecoded means that the condition is presently not wired on the board.

Unusable means to avoid conflict with the TP's, this function is not used in the Model 1.

There exist two Always Branch conditions to reduce the number of diodes in the MC5 bit in the ROM.

Attention Latches operate as follows: They are set at the end of the global cycle with K2. They are cleared at the end of the interval in which branch is tested, unless the set exists simultaneously, in which case the latch is set. This means if the latch was set, the branch was unsuccessful and attention was sent, the latch will still be set at the end of the branch instruction.

Protect is discussed in MPMBM/S-12.

Special Flag A is set and cleared with special function at the end of state A or state B depending on whether or not VCY is set.

Parity error latches are set upon receipt of an error and cleared upon branching, like the attention latches. More information on this is in MPPC/S-14, "Microprocessor Parity Checking Logic."

ALERT, POT, and PIN are discussed in MPPI/S-16, "Microprocessor Pot/Pin Interface."

The request strobe latches work as follows: the correct 8 low order X bits are made = 1 to select the proper microprocessor(s) and the request strobe #1 or #2 is sent out for 100 ns during State A if VCY is false, or State B if it is true, to set the appropriate latch.

A special function clears the request strobe latch #1 and another clears the request strobe latch #2. The branch conditions associated with the request strobe latches are 1) both latches are not set and 2) request strobe latch #2 not set.

RSLAT #1 is used for normal communication between microprocessors and RSLAT #2 is used for failure notices to the microprocessors. Hence, using the first branch condition, it is determined if a request strobe of either type has been sent and the second branch condition allows one to determine which type request strobe was sent.