

Nov. 7, 1961

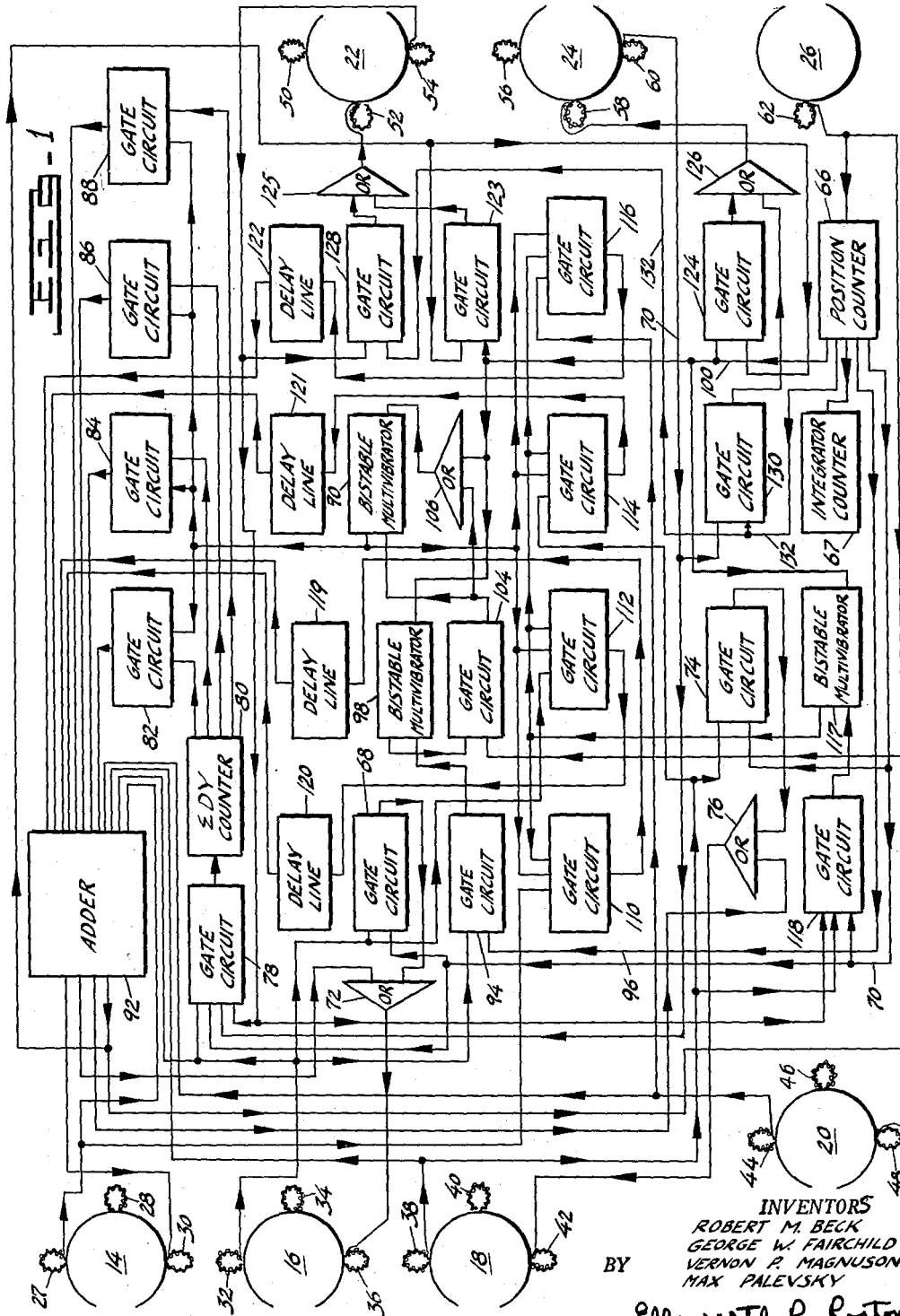
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3,007,640

DIGITAL DIFFERENTIAL ANALYZERS

Filed Jan. 6, 1954

11 Sheets-Sheet 1



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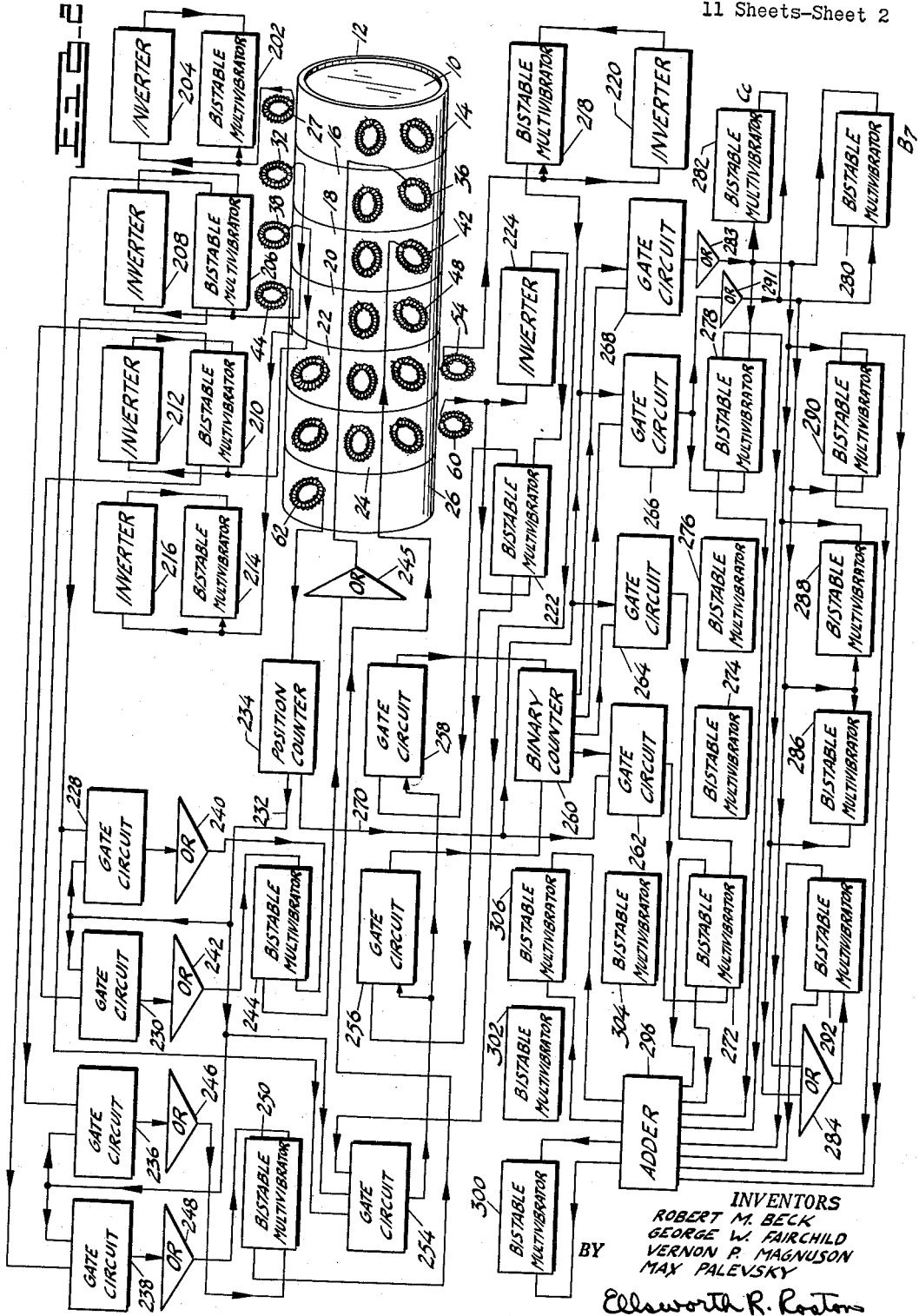
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11 Sheets-Sheet 2



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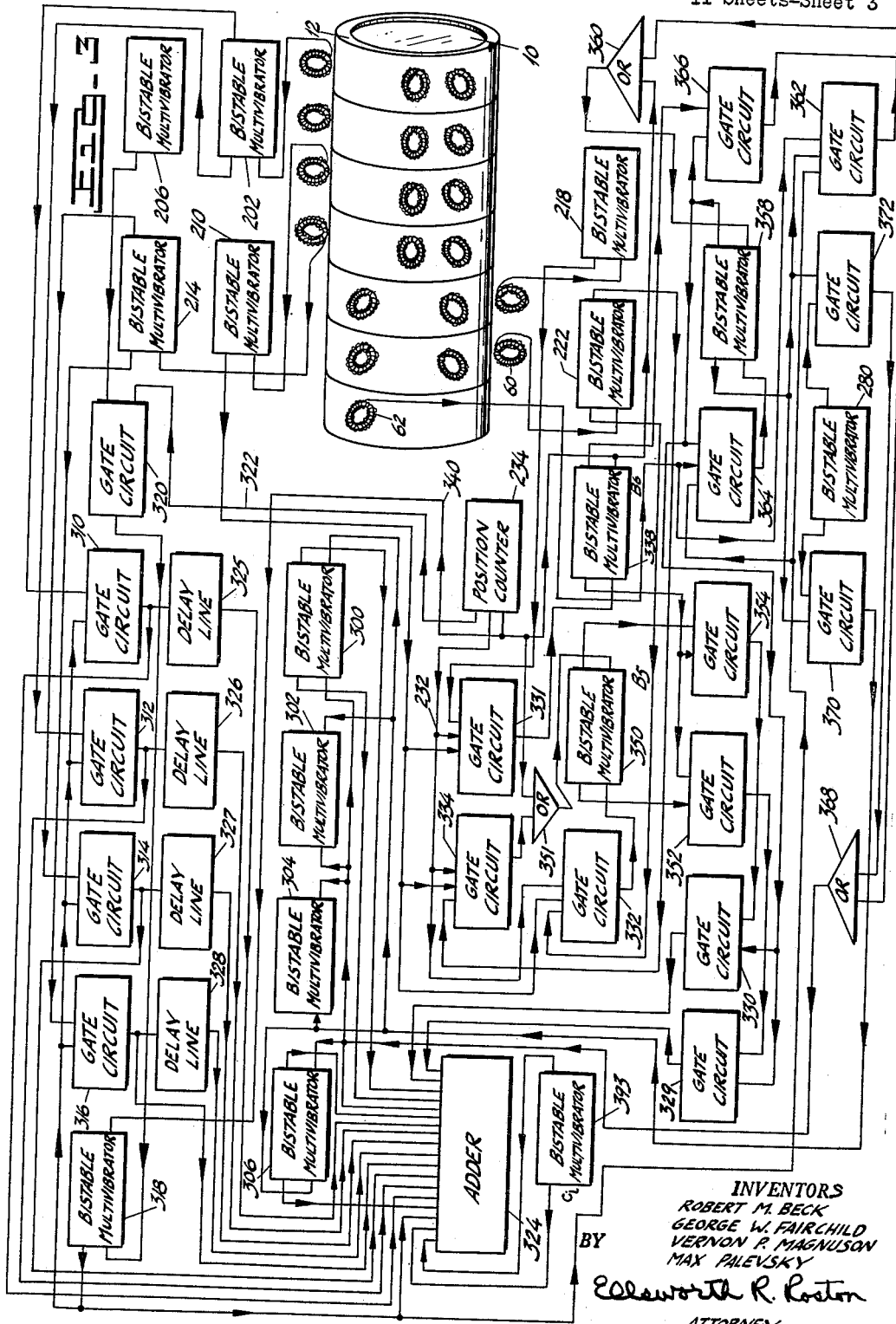
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DIGITAL DIFFERENTIAL ANALYZERS

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11 Sheets-Sheet 3



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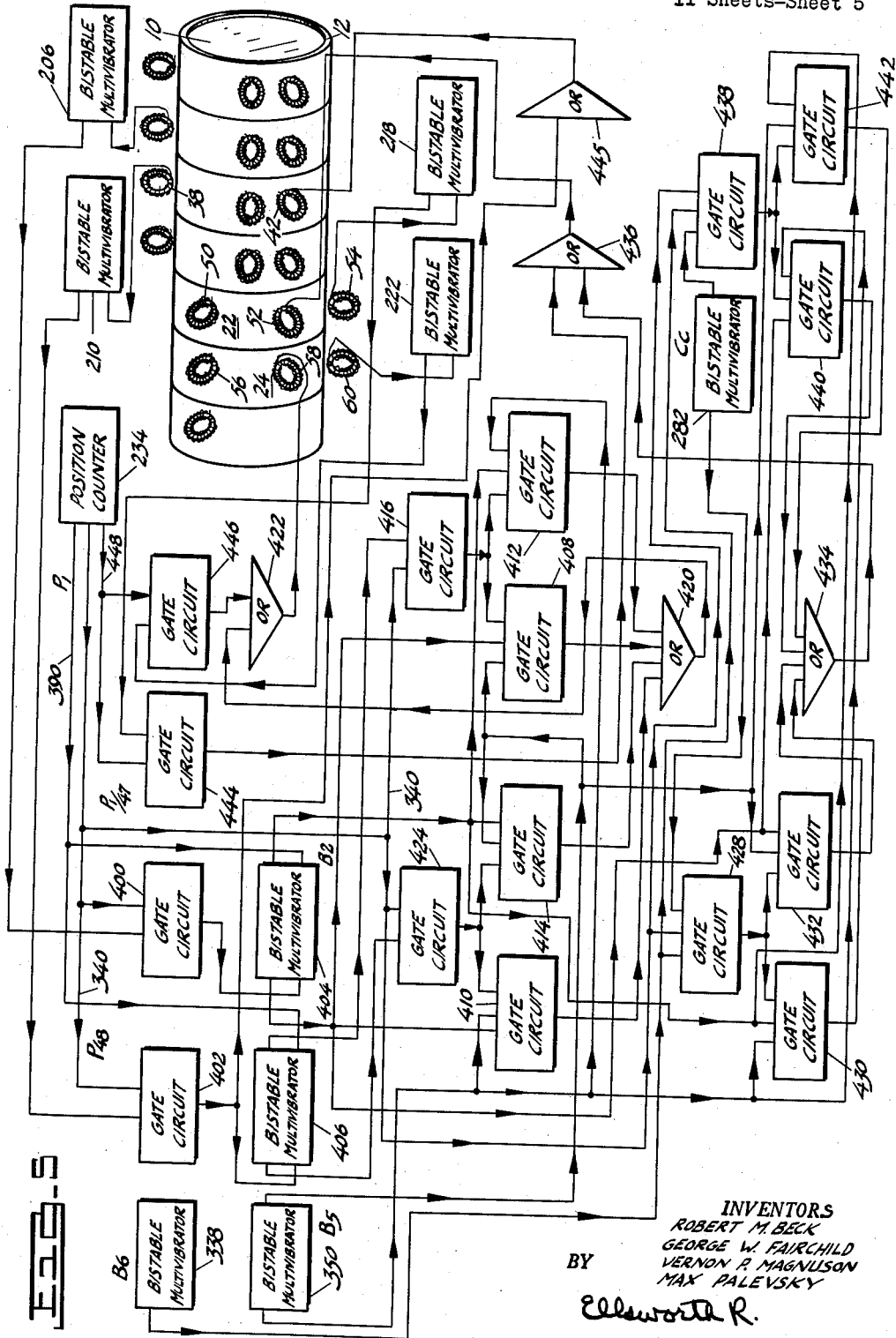
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DIGITAL DIFFERENTIAL ANALYZERS

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11 Sheets-Sheet 5



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DIGITAL DIFFERENTIAL ANALYZERS

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11 Sheets-Sheet 6

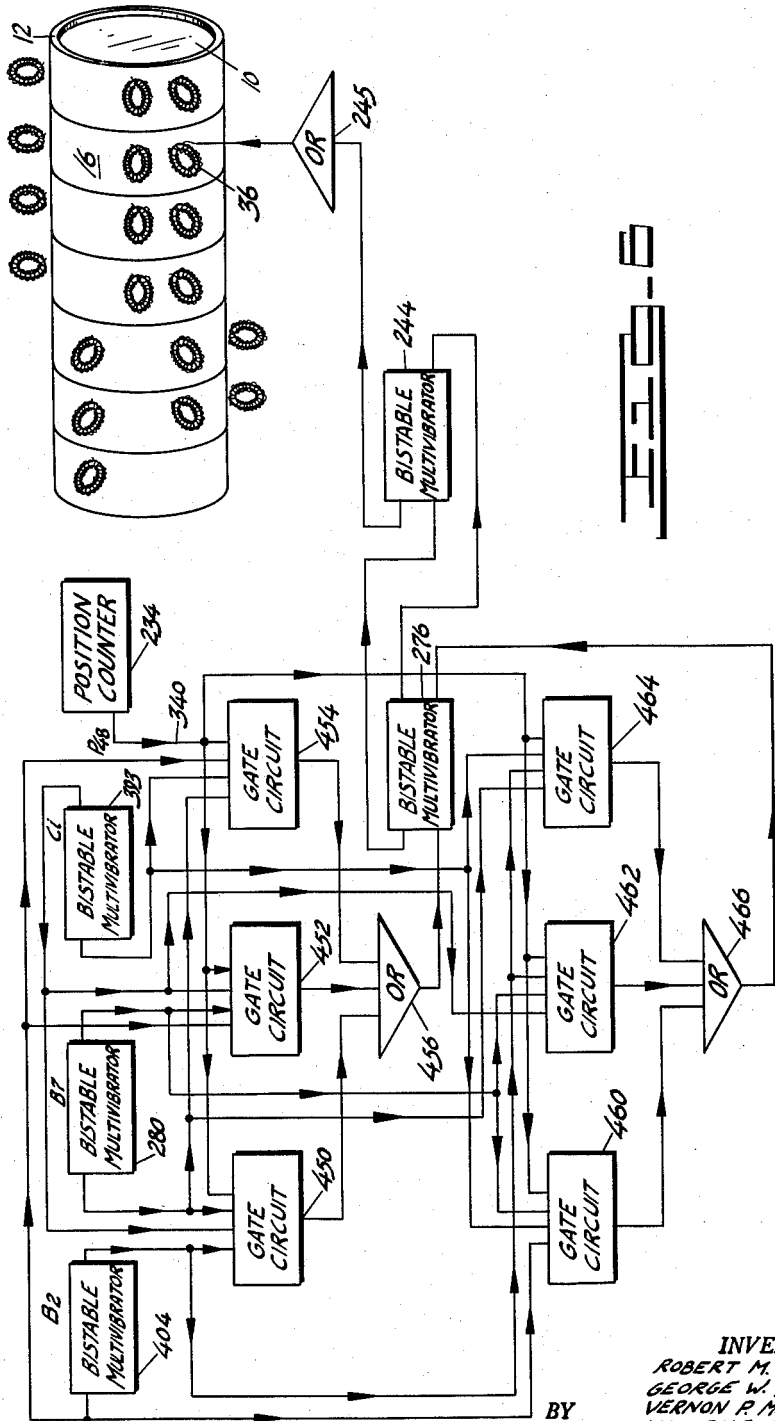


FIG. 6

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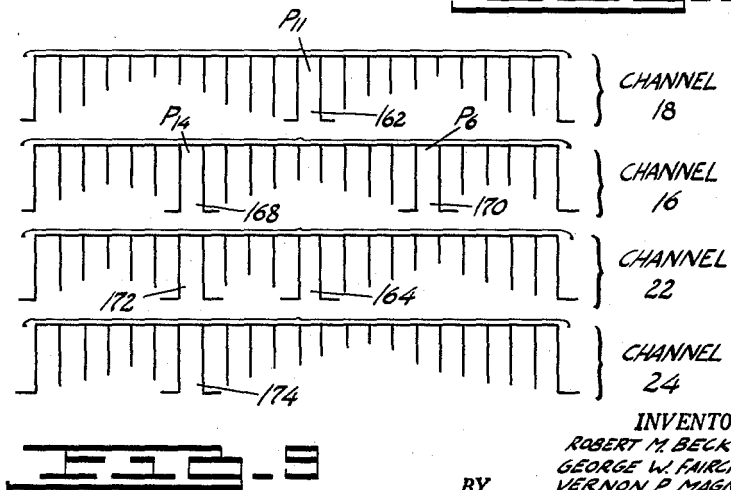
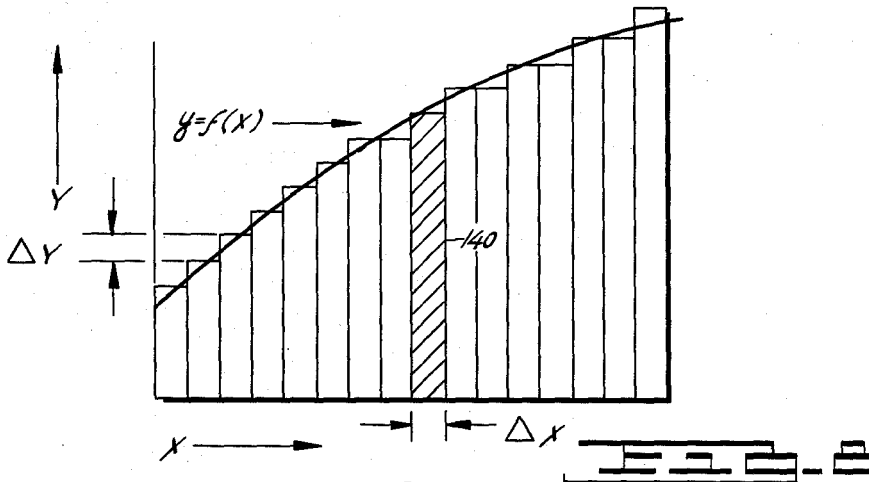
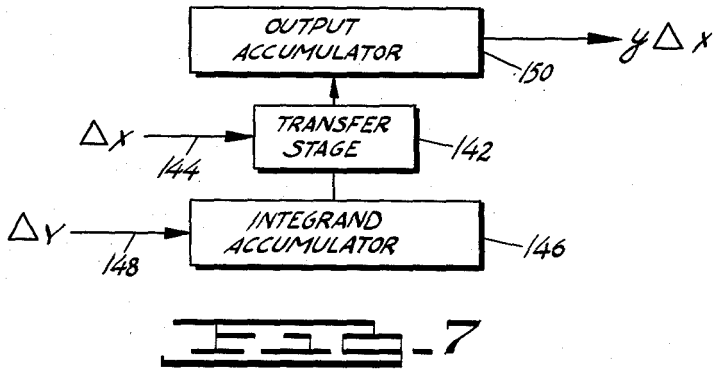
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11 Sheets-Sheet 7



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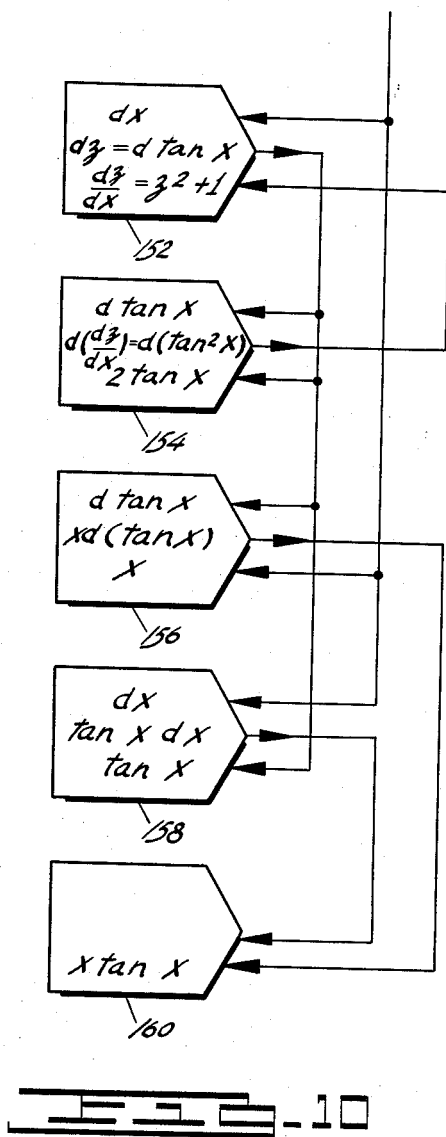
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11 Sheets-Sheet 8



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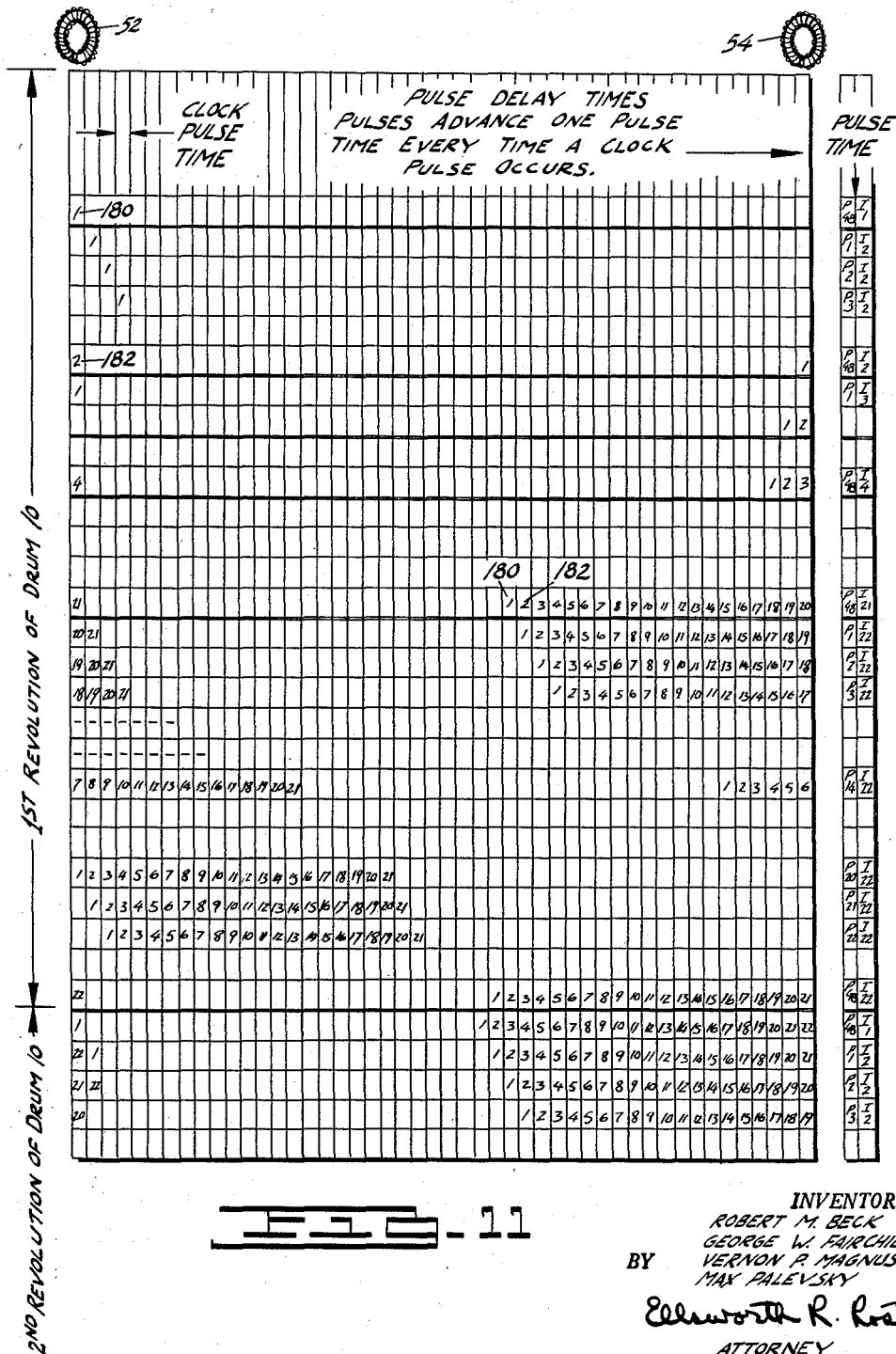
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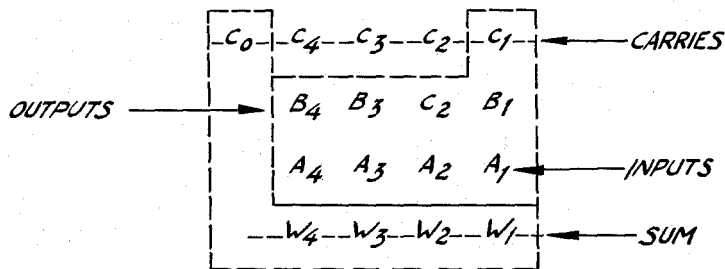
DIGITAL DIFFERENTIAL ANALYZERS

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4	3	2	1	YORR
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1	0	1	1	+8
1	0	1	0	+7
1	0	0	1	+6
1	0	0	0	+5
0	1	1	1	+4
0	1	1	0	+3
0	1	0	1	+2
0	1	0	0	+1
0	0	1	1	+0
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1	0	1	1	-2
1	0	1	0	-3
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0	1	1	0	-7
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4	3	2	1	YORR
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1	0	0	0	+8
0	1	1	1	+7
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1	0	1	0	-6
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1	0	0	0	-8
0	1	1	1	-9



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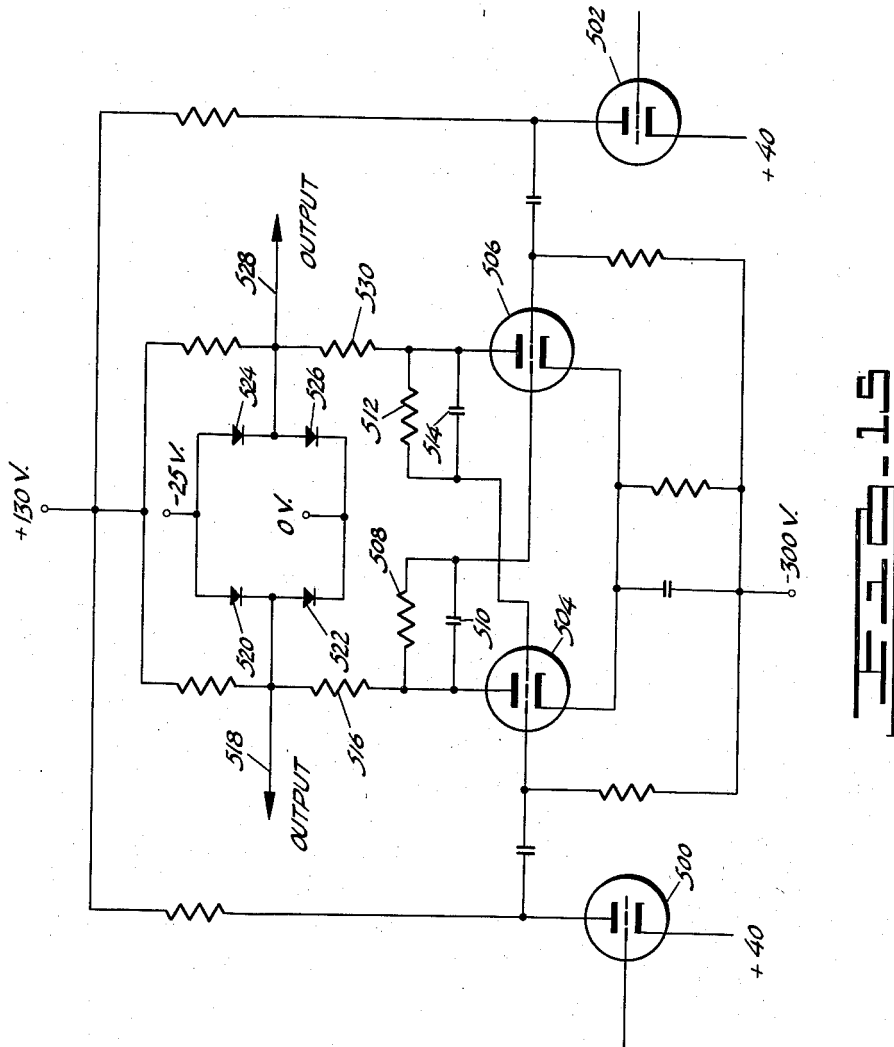
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DIGITAL DIFFERENTIAL ANALYZERS

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11 Sheets-Sheet 11



11-15

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DIGITAL DIFFERENTIAL ANALYZERS

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3 Claims. (Cl. 235—152)

This invention relates to digital differential analyzers, and more particularly to an analyzer for utilizing decimal digits to facilitate its ease of operation.

In co-pending application, Serial No. 217,478, filed March 26, 1951, and now Patent No. 2,900,134, by Floyd G. Steele and William S. Collison, a digital differential analyzer is disclosed for solving complex differential problems by digital steps. The analyzer has the advantages of both digital computers and differential analyzers. The analyzer obtains the advantages of differential analyzers in that it is relatively simple in construction. The analyzer also has the advantage of digital computers in its speed and accuracy of operation. By combining these advantages, a computer is obtained which is able to solve complex differential equations even though it is housed in a cabinet smaller than a desk.

The digital differential analyzers now in use operate in the binary system to obtain the solution of digital problems. These systems have been entirely satisfactory from the standpoint of operation. However, operators of the machine have expressed some desire for an analyzer which will operate on a decimal basis. It has been the opinion of these people that a machine operating on a decimal basis can be initially coded relatively easily and that the results obtained during and after the solution of a problem can also be read and digested easily.

This invention provides a digital differential analyzer for converting binary information into decimal information and for solving differential problems on the basis of the decimal information. The analyzer operates on a decimal basis by combining bits of binary information into parallel combinations of signals such that each parallel combination represents a different decimal digit in a multi-digital number. The analyzer operates to simultaneously present the signals in each combination for computation. By utilizing parallel combinations of signals, not only the advantage of operating on a decimal basis but also the advantages of increased capacity and speed of operation are obtained.

An object of this invention is to provide a digital differential analyzer which operates in digital steps to obtain a solution of complex differential problems.

Another object is to provide an analyzer of the above character which is capable of being coded and of operating on a decimal basis to solve differential problems.

A further object is to provide an analyzer of the above character for converting binary bits of information into parallel combinations of signals representing decimal digits and for utilizing the parallel combinations of signals to obtain speedy and accurate solutions of problems.

Still another object is to provide an analyzer of the above character which has a relatively large capacity for information and a relatively high speed of operation.

A still further object is to provide a method of solving differential problems in digital steps and on a decimal basis.

Other objects and advantages will be apparent from a detailed description of the information and from the appended drawings and claims.

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In the drawings:

FIGURE 1 is a simplified block diagram which schematically illustrates a digital differential analyzer forming one embodiment of this invention;

FIGURES 2, 3, 4, 5 and 6 are schematic diagrams, partly in block form and partly in perspective, illustrating in some detail an operating system of the digital differential analyzer shown in FIGURE 1;

FIGURE 7 is a block diagram illustrating the operation of one of the integrators forming part of the digital differential analyzer shown in FIGURES 2 to 6, inclusive;

FIGURE 8 is a curve illustrating the operation of an integrator such as the integrator shown in FIGURE 7;

FIGURE 9 is a chart which illustrates how different parts of an integrator such as that shown in FIGURE 7 are coded to control the operation of the integrator;

FIGURE 10 is a schematic diagram illustrating the relationship between different integrators forming the digital differential analyzer shown in FIGURES 2 to 6, inclusive, when the analyzer is solving a particular problem;

FIGURE 11 is a chart illustrating the operation of certain of the components forming a part of the analyzer shown in FIGURE 1 and in FIGURES 2 to 6, inclusive;

FIGURE 12 is a chart which illustrates the operation of certain of the components shown in FIGURES 2 to 6, inclusive;

FIGURE 13 is a chart illustrating the operation of certain of the components in analyzers now in use to provide a comparison with the chart shown in FIGURE 12.

FIGURE 14 is a chart which illustrates the operation of certain of the components shown in FIGURES 2 to 6, inclusive; and

FIGURE 15 is a diagram of a flip-flop unit which forms a basic stage of the analyzer shown in FIGURE 1 and of the analyzer shown in FIGURES 2 to 6, inclusive.

A simplified operation-illustrating block diagram is shown in FIGURE 1 of an analyzer for solving differential problems by digital steps. The analyzer includes a drum (similar to drum 10 schematically shown in FIGURES 2 to 6, inclusive) adapted to be rotated by a suitable motor (not shown). A thin coating 12 (FIGURE 2) of magnetic material is applied to the periphery of the drum. The coating 12 can be considered as being divided into a plurality of annular channels 14, 16, 18, 20, 22, 24 and 26. These channels are shown schematically in FIGURE 1 in separated relationship for purposes of convenience. Each of the channels is separated by a sufficient distance from its adjacent channel so as to be substantially unaffected by the magnetic information provided in the adjacent channel.

The circumferential distance of each channel may be considered as being divided into a plurality of positions. Each of the positions is sufficiently separated from its adjacent positions to receive a different magnetization than that provided on the adjacent positions. For example, approximately 1160 equally spaced pulse positions may be provided in each channel when the drum has a radius of approximately four inches.

A plurality of toroidal coils are positioned adjacent to each of the channels 14, 16, 18, 20, 22, 24 and 26. For example, coils 27, 28 and 30 are provided in contiguous relationship to the channel 14. These coils are shown schematically in FIGURE 1. Similarly, coils 32, 34 and 36; coils 38, 40 and 42; coils 44, 46 and 48; coils 50, 52 and 54; and coils 56, 58 and 60 are associated with the channels 16, 18, 20, 22 and 24, respectively. A single coil 62 is disposed adjacent the channel 26.

The coils 27 and 30 are effectively separated from each other by approximately 104 pulse positions, and the coil

28 is disposed at an intermediate position between the coils 27 and 30. The coil 30 is adapted to provide signals in a pattern dependent on the operation of the digital differential analyzer and to induce the corresponding magnetic pattern on the drum 10 as the drum rotates. The pattern induced on the drum 10 by the coil 30 is of the binary form in which a magnetization in one circumferential direction indicates one value and a magnetization in the other direction indicates a second value.

The coil 27 is adapted to pick up the changes in the direction of magnetization in the channel 14 as the drum rotates. The coil 28 is adapted to produce a substantially constant signal for returning the direction of magnetization on the drum to that representing a value of "0" after the magnetic pattern on the drum has been converted into a corresponding electrical pattern by the coil 27.

The coils 32, 34 and 36 are separated from one another by distances corresponding to the distances between the coils 27, 28 and 30 and are adapted to perform functions similar to those performed by the coils 27, 28 and 30, respectively. The coils 38, 40 and 42 and the coils 44, 46 and 48 are also separated in the channels 18 and 20 in a similar manner to the separation of the coils in the channel 14 and are adapted to perform functions corresponding to those performed by the coils 27, 28 and 30, respectively.

The coils 52 and 58 are adapted to operate in a manner similar to the coil 30 to provide a magnetic pattern in the channels 22 and 24, respectively, in a pattern dependent upon the problem to be solved. The coils 52 and 58 are effectively separated from the coils 54 and 60, respectively, by approximately 49 pulse positions during the operation of the analyzer to obtain the solution of a mathematical problem.

The coils 54 and 60 are adapted to produce signals in accordance with the magnetic pattern provided in their respective channels by the coils 52 and 58. The coils 50 and 56 are adapted to operate in a manner similar to the coil 28 to produce a "zero" direction of magnetization in the channels 22 and 24, respectively, after the patterns provided by the coils 52 and 58 have been utilized by the coils 54 and 60, respectively.

The coil 62 is adapted to produce a cycle of a signal approximating a sine wave as each pulse position in the channel 26 moves past the coil. The coil 62 produces sinusoidal signals because of the magnetic pattern permanently provided in the channel 26. This pattern remains constant regardless of the problem to be solved.

A counter 66 is connected to the coil 62 to count the cycles of the sine waves in the channel 26 as the drum rotates. The counter 66 is formed from a plurality of multivibrators connected in cascade arrangement and is adapted to count successive sine signals in a numerical range from "1" to "48." Upon each count of "48," the counter 66 is adapted to return to its initial state for the commencement of a new count. As will be disclosed in detail hereinafter, a new integrator i.e. integrator storage section is presented for computation upon the completion of each count of "48."

Similarly, a counter 67 is formed from a plurality of multivibrators in cascade arrangement. The counter 67 is connected to the counter 66 to count the number of times that a full count is obtained in the counter 66. For example, the counter 67 may count up to 22 full counts in the counter 66 before returning to its initial state for the initiation of a new count. In this way, the counters 66 and 67 divide the drum 10 into 22 integrators each having 48 pulse positions.

As schematically shown in FIGURE 1, the output signals induced in the coil 32 are introduced to a gate circuit 68, which also has signals applied to it through a line 70 from the counter 66. The output signals from the gate circuit 68 are in turn applied through an "or" network 72 to the coil 36. Similarly, a gate circuit 74 re-

ceives signals from the coil 38 and through the line 70 from the counter 66. The output terminal of the gate circuit 74 is connected to an input terminal of an "or" network 76 having its output terminal connected to the coil 42.

The coil 32 is not only connected to the gate circuit 68 but also to an input terminal of a gate circuit 78 having other input terminals connected to the coils 54 and 60 and through the line 70 to the counter 66. The output from the gate circuit 78 passes to a counter 80 formed from a plurality of multivibrators in cascade arrangement. The output from the counter 80 is in turn applied to input terminals of gate circuits 82, 84, 86 and 88 having other input terminals connected to the plate of the left tube in a multivibrator 90. The output terminals of the gate circuits 82, 84, 86 and 88 are connected to input terminals of an adder 92. The adder 92 comprises a system for additively combining various quantities represented by electrical signals in a manner to be explained. The structure of the adder 92 is not given since the system of FIGURE 1 is merely a simplified illustrative system, and the structure of an operating system will be subsequently described in detail.

The signals from the coil 32 are also introduced to an input terminal of a gate circuit 94 having another input terminal connected through a line 96 to the counter 66. The output from the gate circuit 94 is applied to the grid of the left tube in a bistable multivibrator 98, the grid of the right tube in the multivibrator being connected through a line 100 to the counter 66. The plate of the left tube in the multivibrator 98 is connected to an input terminal of a gate circuit 104, another input terminal of which is connected to the coil 62. The signals passing through the gate circuit 104 are introduced directly to the grid of the left tube in the multivibrator 90 and through an "or" network 106 to the grid of the right tube in the multivibrator to change the state of the multivibrator 90 with each signal. Signals also pass from the counter 66 through the line 100 and the "or" network 106 to the grid of the right tube in the multivibrator 90.

In addition to receiving the signals from the gate circuits 82, 84, 86 and 88, the adder 92 also receives signals from the coils 27, 32, 38 and 44. The signals from the gate circuits 82, 84, 86 and 88 are arithmetically combined with the signals from the coils 27, 32, 38 and 44. The results obtained are applied directly to the coil 30, through the "or" network 72 to the coil 36, through the "or" network 76 to the coil 42, and directly to the coil 48.

The pulses induced in the coils 27, 32, 38 and 44 are also applied to input terminals of gate circuits 110, 112, 114, and 116, respectively. Connections are also made to input terminals of the gate circuits 110, 112, 114 and 116 from the plate of the left tube in the multivibrator 90 and from the plate of the left tube in a multivibrator 117. Connections are respectively made to the grids of the left and right tubes in the multivibrator 117 from a gate circuit 118 and through the line 100 from the counter 66. The gate circuit 118 in turn receives signals from the coils 38 and 54 and through the line 70 from the counter 66.

The output signals from the gate circuits 110, 112, 114 and 116 are introduced through suitable delay lines 119, 120, 121 and 122, respectively, to the adder 92 for combination with the signals from the coils 27, 32, 38 and 44. The delay lines 119, 120, 121 and 122 may be bistable multivibrators to delay by one pulse position the information from the gate circuits 110, 112, 114 and 116. The output signals obtained by the adder 92 are applied to the coils 30, 36, 42 and 48.

The output signals passing from the adder 92 to the coil 48 are also applied to gate circuits 123 and 124 having other input terminals connected through the line 100

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to the counter 66. The output signals from the gate circuits 123 and 124 respectively pass through "or" networks 125 and 126 for introduction to the coils 52 and 58. The "or" networks 125 and 126 also respectively receive signals from gate circuits 128 and 130. Connections are made to input terminals of the gate circuit 123 from the coil 54 and through a line 132 from the counter 66. Similarly, input terminals of the gate circuit 130 are connected to the coil 60 and the line 132.

The digital differential analyzer as illustratively described above in simplified form is adapted to provide the solution of differential equations. For example, it may provide the solution of the problem of evaluating the integral of a general equation $y=f(x)$ so as to obtain a function $\int ydx = \int f(x)dx$, where $f(x)$ represents a function of x and $\int f(x)dx$ represents the integral of the function. If a curve $y=f(x)$ is plotted with x as the abscissa and y as the ordinate, the analyzer obtains the relationship $\int ydx = \int f(x)dx$ by computing the area under the curve $y=f(x)$. By determining the area under the curve $y=f(x)$, the analyzer performs electronically operations that may sometimes be performed mentally by a skilled mathematician when the problem to be solved is relatively simple.

The analyzer obtains the value of the function

$$\int ydx = \int f(x)dx$$

by producing small increments of x . These increments may be represented by the symbol Δx . For each Δx increment, the analyzer determines the value of y and obtains the product $y\Delta x$. This product $y\Delta x$ approximates the area under the curve $y=f(x)$ for each Δx increment, as indicated in FIGURE 8 by the shaded area 140 for a particular Δx increment. If the product $y\Delta x$ is obtained for successive Δx increments and if all of the $y\Delta x$ increments are added together, the area under the interval of the curve representing $f(x)$ from x_0 to x may be approximated. A relatively accurate approximation may be obtained by decreasing the value of each Δx increment.

An integrator for determining the $y\Delta x$ increments and for storing the cumulative values of these increments is shown in FIGURE 7. The integrator includes a transfer stage 142 for obtaining Δx increments at periodic intervals through a line 144. The integrator also has an integrand accumulator 146 for storing the value of the dependent quantity y and for receiving Δy increments through a line 148 from its own and from other integrators so as to vary the value of y in accordance with the function $y=f(x)$. An output accumulator 150 is provided to receive $y\Delta x$ increments, to combine each $y\Delta x$ increment with the previous increments and to deliver the cumulative value obtained to another integral accumulator or transfer stage while holding the remainder in store. A detailed explanation of this will be given hereafter.

The interrelationship between different integrators is illustrated in FIGURE 10 for a particular problem. This problem starts with a differential equation represented by

$$\frac{dy}{dx} = y^2 + 1$$

As is mathematically known, the differential solution of this problem indicates that $y = \tan x$. The interrelationship illustrated in FIGURE 10 utilizes this solution to generate the function $\tan x$ which is accumulated in the register of an output integrator. The integrators involved in the generation of the function $\tan x$ are indicated in FIGURE 10 by blocks 152, 154, 156, 158 and 160. In each integrator, the introduction of the Δx increments constituting changes in the independent variable quantity for the integrator is indicated by a line extending into the upper right position in the block. The Δy increments are introduced into the integrator through a line or a plurality of lines extending into the lower right portion of the block representing the integrator. The output of the integrator is obtained from a line extending from

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an intermediate position at the right side of the appropriate block.

As will be seen in FIGURE 10, Δx increments of the independent variable for a particular integrator may be obtained from the output of another integrator. For example, in FIGURE 10, the Δx increments for the integrators 154 and 156 are obtained from the output of the integrator 152. Similarly, Δy increments for a particular integrator may be obtained from the output of other integrators as well as from the output of the integrator itself. For example, Δy increments for the integrators 154 and 158 are obtained from the output of the integrator 152.

The Δy and Δx increments for each integrator are actually determined from a coded pattern provided in the channels 16 and 18, respectively. As previously disclosed, the pulse positions in each channel are subdivided into 22 integrators each having 48 pulse positions. The first 22 positions in each integrator in the channel 18 are coded to indicate a Δx increment. Since the first 22 positions in the channel 18 for each integrator correspond in number to the 22 integrators in the analyzer, each integrator can receive a Δx increment from the output of any of the other integrators. This can be effectuated by providing a pulse in the channel 18 in a particular one of the first 22 positions for the integrator.

For example, the Δx increments for the integrator 154 in FIGURE 10 would be coded in a particular one of the 22 positions in the channel 18. As will be disclosed in detail hereinafter, the particular position corresponds to the time at which the output from the integrator 152 appears on the coils 54 and 60. In FIGURE 9, a pulse 162 is shown as being recorded in the channel 18 in the 11th pulse position for a particular integrator.

A pulse in the channel 18 in one of the first 22 positions for a particular integrator indicates that a Δx increment may be made for the integrator. However, such a pulse does not indicate whether an increment will actually be made and, if so, whether the polarity of such increment will be positive or negative. The actual occurrence of a Δx increment for the integrator is indicated by the presence or absence of a coincidental pulse in the channel 22. If a positive pulse is picked up from the channel 22 by the coil 54 at the same time as the pulse representing a possible Δx increment for a particular integrator is picked up by the coil 38, a Δx increment for the integrator actually occurs. For example, the pulse 162 in FIGURE 10 indicates an actual Δx increment for a particular integrator since it coincides in time with a pulse 164 in the channel 22. A Δx increment is not obtained for the integrator if a pulse does not appear in the channel 22 at the same time as the pulse in the channel 18.

The polarity of each Δx increment is determined by the presence or absence of a coincidental pulse in the channel 24. If a pulse is picked up from the channel 24 by the coil 60 at the same time that pulses indicating an actual Δx increment for a particular integrator are picked up by the coils 38 and 54, the Δx increment for the integrator is positive. The Δx increment is negative if a pulse does not appear in the channel 24 at the same time as the pulses in the channels 18 and 22. For example, the pulse 162 in FIGURE 9 indicates a negative Δx increment since a pulse does not appear in the channel 24 simultaneously with the occurrence of the pulses 162 and 164 in the channels 18 and 22, respectively.

The first 22 positions in the channel 16 for each integrator are coded to indicate Δy increments in a manner similar to the coding of corresponding positions in the channel 18 to indicate Δx increments. Since the first 22 positions in each integrator correspond to the 22 integrators in the digital differential analyzer, each integrator is coded in particular ones of the first 22 positions in the channel 16 so as to receive the outputs from certain other integrators in accordance with the problem to be solved. For example, a pulse would be coded in

the channel 16 in a particular one of the first 22 positions for the integrator 158 in FIGURE 10 so as to coincide with the time at which the output from the integrator 152 is made available to the coils 54 and 60 in the channels 22 and 24, respectively. Although only one Δx increment can be obtained for an integrator upon each revolution of the drum, several Δy increments can be obtained. This may be seen by the pulses 168 and 170 in the channel 16 in FIGURE 9.

Each pulse in the first 22 positions in the channel 16 for each integrator represents the possibility of a Δy increment but does not indicate the actual occurrence of such an increment or the polarity of the increment. The actual occurrence of the increment is indicated by the presence or absence of a pulse in the channel 22 at the same time that the pulse in the channel 16 is made available to the coil 32. For example, the pulse 168 in FIGURE 9 indicates an actual Δy increment for a particular integrator since it coincides in time with a pulse 172 in the channel 22. However, no Δy increment is obtained when the pulse 170 is picked up by the coil 32 since there is no coincidental pulse in the channel 22.

The sign of each actual Δy increment is indicated by the presence or absence of a pulse in the channel 24 at the time that pulses in the channels 16 and 22 are simultaneously made available to the coils 32 and 54. For example, the pulse 168 in FIGURE 9 indicates a positive Δy increment for a particular integrator since a pulse 174 appears in the channel 24 at the time that the pulses 168 and 172 are picked up by the coils 32 and 54, respectively.

Since the interrelationship between the different integrators remains constant during the solution of a particular problem, the coding pulses in the channels 16 and 18 for the first 12 positions of the integrator must be retained during the computation. Retention of the pulses in the channel 16 is effectuated by the gate circuit 68, which remains open during the first 22 positions in each integrator to pass the coded information in these positions. The gate circuit 68 opens during these pulse positions because of the introduction of a relatively high voltage through the line 70 from the counter 66. The signals then pass through the "or" network 72 for recordation by the coil 36 in the channel 16. Similarly, the gate circuit 74 opens during the first 22 positions for each integrator so that the coding information can pass through the "or" network 76 for recordation by the coil 42 in the channel 18.

It should be appreciated that the gate circuits similar to the circuit 68 operate to pass information only when positive pulses are simultaneously introduced to all of the input terminals of the circuit. In computer terminology such circuits have been designated as "and" networks. The term "or" networks is also common in computer terminology. Such circuits operate to pass such information when any one of their input terminals receives a relatively high voltage. Such "or" networks are shown in the drawings as triangles and are exemplified by the networks 72 and 76.

During the first 22 positions of each integrator, the gate circuit 78 operates to determine the occurrence of Δy increments for the integrator and the polarity of each such increment. The gate circuit 78 makes such determinations by comparing the pulses from the coil 32 with the pulses from the coils 54 and 60. Each pulse induced in the coil 32 in the first 22 positions for an integrator indicates that a Δy increment can be obtained. As previously disclosed, the particular position in which a pulse occurs determines for an integrator which of the other integrators in the analyzer provides Δy increments for the integrator. The simultaneous production of a pulse by the coil 54 indicates that a Δy increment has actually occurred. When the coil 60 also produces

a simultaneous pulse, the gate circuit 78 indicates that the Δy increment has a positive polarity.

At the same time that the gate circuit 78 operates to determine the occurrence of Δy increments for an integrator and the polarity of each such increment, the counter 80 arithmetically combines each such Δy increment. For example, a signal passing to the counter 80 from the gate circuit 78 may cause the circuit to provide a numerical indication of +4 when an indication of +3 was previously provided by the counter. Similarly, the indications in the counter 80 may change from a value of -3 to a value of -4 upon the introduction of a negative signal from the gate circuit 78.

The counter 80 retains in binary form the numerical information relating to the cumulative value of the Δy increments for an integrator. The counter 80 retains the information in binary form since it comprises a plurality of multivibrators arranged in cascade relationship. In this embodiment, four multivibrators in cascade arrangement are provided. For example, with a resultant count of +5 for the Δy increments for a particular integrator, the first and third multivibrators in the cascade arrangement may be operated to indicate a binary pattern of 0101, where the least significant digit is at the right. In binary form, a pattern of 0101 indicates that $(0)(2^3) + (1)(2^2) + (0)(2^1) + (1)(2^0) = 5$. Similarly, a value of +3 is indicated by a pattern of 0011, where the least significant digit is at the right.

As previously disclosed, the information controlling increments in the dependent quantity for each integrator is provided in the channel 16 in the first 22 pulse positions for each integrator. The information relating to the dependent quantity y itself occurs in the channels 14, 16, 18 and 20 after the 22nd pulse position for each integrator. As will be disclosed in detail hereinafter, a group of pulse indications simultaneously appearing in the channels 14, 16, 18 and 20 provides an indication as to the value of a decimal digit.

The information relating to the dependent quantity y for each integrator is preceded by a pulse in the channel 16 to indicate that the information which follows relates to the dependent quantity y . For example, a pulse may occur in pulse position 28 for an integrator to indicate that the subsequent information in the channels 14, 16, 18 and 20 relates in part to the dependent quantity y for the integrator. This pulse has been designated in co-pending application Serial No. 217,478 as the "start" pulse.

The "start" pulse in the channel 16 is introduced to the gate circuit 94, which also receives signals through the line 96 from the counter 66. Since a relatively high voltage appears on the line 96 only after the 22nd pulse position for each integrator, the "start" pulse is the first pulse which is able to pass through the gate circuit 94. This pulse passes to the grid of the left tube in the multivibrator 98 and cuts off the tube. The resultant relatively high voltage on the plate of the left tube in the multivibrator 98 is introduced to the gate circuit 104.

Because of its connection to the coil 62, the gate circuit 104 passes each clock signal in the channel 26 after a relatively high voltage is introduced to it from the multivibrator 98. The signals from the gate circuit 104 are introduced directly to the grid of the left tube in the multivibrator 90 and through the "or" network 106 to the grid of the right tube in the multivibrator. The first signal from the gate circuit 104 causes the left tube in the multivibrator 90 to become cut off for reasons which will be disclosed in detail hereafter. Upon the passage of a second signal through the gate circuit 104, the grid of the right tube in the multivibrator 90 becomes cut off and the left tube starts to conduct.

Similarly, the left tube in the multivibrator 90 becomes alternately cut off upon the introduction of odd signals from the gate circuit 104 and the right multivibrator tube

becomes cut off upon the introduction of even signals. At the 48th pulse position for each integrator, a signal is introduced from the counter 66 through the line 100 and the "or" network 106 to the grid of the right tube of the multivibrator 90 so as to cut off the tube. In this way, the multivibrator 90 is prepared to have its left tube cut off upon the passage of the first signal through the gate circuit 104 for the next integrator.

As previously disclosed, the plate of the left tube in the multivibrator 90 becomes cut off upon the passage of the first signal through the gate circuit 104. When the left tube in the multivibrator 90 becomes cut off, a relatively high voltage is introduced through the plate of the tube to the gate circuits 82, 84, 86 and 88 to open the gate circuits for the introduction of information from the counter 80. Information relating to the least significant binary unit is introduced from the counter 80 to the gate circuit 82 and information relating to binary digits of increasing significance are simultaneously introduced to the gate circuits 84, 86, 88. It has already been disclosed that the information introduced to the gate circuits from the counter 80 relates to increments in the dependent quantity y for each integrator.

The information from the counter 80 passes through the gate circuits 82, 84, 86 and 88 to the adder 92 for combination with the signals induced in the coils 27, 32, 38 and 44, respectively at alternate pulse positions, when the signals induced in the coils 27, 32, 38 and 44 relate to the dependent quantity y for the integrator undergoing computation. For example, when the start pulse for an integrator occurs at pulse position 27 for the integrator, pulse position 28 constitutes the first information pulse. Information relating to the value of the dependent quantity y for the integrator is accordingly provided in the channels 14, 16, 18 and 20 in pulse position 28 for the integrator and subsequently in alternate pulse positions such as pulse positions 30, 32, 34 etc.

The information relating to the dependent quantity y for each integrator is provided in the channels 14, 16, 18 and 20 on a decimal basis. For example, when the start pulse occurs in pulse position 27, the information in the channels 14, 16, 18, and 20 for pulse position 28 provides an indication of a decimal number between "0" and "9" inclusive. Similarly, the information in the channels 14, 16, 18 and 20 for pulse position 30 provides an indication of the "tens" digit such as "10," "20," "30" etc. The exact manner in which the signals in the channels 14, 16, 18 and 20 provide such decimal information will be disclosed in detail hereafter.

Since the information in the channels 14, 16, 18 and 20 relate to decimal indications in a particular decimal code and since the signals passing through the gate circuits 82, 84, 86 and 88 relate to binary information, the signals passing through the gate circuits 82, 84, 86 and 88 are first converted to a decimal basis of the particular code before they are combined with the signals induced in the coils 27, 32, 38 and 44. The correction required to produce this conversion to a decimal base and the circuitry required for such conversion will be described in detail subsequently in connection with the detailed system shown in FIGURES 2 to 6 inclusive. The resultant signals produced by the adder 92 provide an indication in decimal form of the new value of the dependent quantity for the integrator undergoing computation. These signals are introduced to the coils 30, 36, 42 and 48 for recordation in the channels 14, 16, 18 and 20, respectively.

The pulses induced in the coils 27, 32, 38 and 44 are not only introduced to the adder 92 but also to gate circuits 110, 112, 114 and 116, respectively. Since the gate circuits 110, 112, 114 and 116 are also connected to the plate of the left tube in the multivibrator 90, the gate circuits become prepared for opening at alternate pulse positions after the start pulse. In these pulse positions, in-

formation relating to the dependent quantity y for each integrator is presented in the channels 14, 16, 18 and 20.

The gate circuits 110, 112, 114 and 116 become opened for the passage of information to the adder 92 only when a relatively high voltage is introduced to them from the plate of the left tube in the multivibrator 117. Such a high voltage is produced on the plate of the left tube in the multivibrator 117 when a signal passes to the grid of the tube from the gate circuit 118 and since the gate circuit is connected through the line 70 to the counter 66, it is prepared for opening only during the first 22 pulse positions of each integrator. During these pulse positions, a signal passes through the gate circuit 118 when pulses of relatively high voltage are simultaneously induced in the coils 38 and 54. The pulse of relatively high voltage induced in the coil 38 indicates the possibility of a Δx increment for an integrator undergoing computation. When a pulse simultaneously is induced in the coil 54, an indication is provided that a Δx increment has actually occurred for the integrator.

Since the signal passing through the gate circuit 118 provides an indication that a Δx increment has actually occurred for an integrator, the voltage on the plate of the left tube in the multivibrator 117 becomes relatively high only upon the actual occurrence of such an increment. When the voltage on the plate of the left tube in the multivibrator 117 becomes high, it remains high during the time that the remaining pulse positions in the integrator are presented for computation. At pulse position 48 for the integrator, a signal is introduced to the grid of the right tube in the multivibrator 117 through the line 100 from the counter 66 so as to cut off the right tube in the multivibrator and make the left tube conductive. In this way, the left tube in the multivibrator 117 is prepared to become triggered into a state of non-conductivity upon the occurrence of a Δx increment for the next integrator.

Because of the connection between the plate of the left tube in the multivibrator 117 and the gate circuits 110, 112, 114 and 116, information is able to pass through the gate circuits only when a Δx increment has actually occurred for an integrator. As previously disclosed, this information relates to the new value of the dependent quantity y for the integrator. The information in the channels 14, 16, 18 and 20 relating to the value of the dependent quantity y for an integrator is delayed by one pulse position and is then differentially combined in the adder 92 with the signals in the channels 14, 16, 18 and 20 relating to the cumulative value of the differential combination $y\Delta x$ for the integrator. The new information relating to the cumulative value of the differential combination for each integrator is recorded in alternate pulse positions in the channels 14, 16, 18 and 20.

Sometimes, as the $y\Delta x$ increments for an integrator are added to the cumulative value of the differential combination for the integrator, an over-flow is obtained in the information stored in the channels 14, 16, 18 and 20. When an over-flow occurs in the cumulative value of the differential combination for an integrator, the indications representing the cumulative value return to an intermediate value so that they can build up again to a relatively high value. At the same time, an over-flow pulse is produced by the adder 92 at pulse position 48 for the integrator. This pulse passes through the gate circuit 123 since the gate circuit opens at the last pulse position for each integrator because of its connection through the line 100 to the counter 66. The pulse then passes through the "or" network 125 for recordation by the coil 52 in the channel 22.

For example, a first pulse of relatively high voltage may be provided in the channel 22 at the 48th position of integrator "1." This pulse indicates that an over-flow has occurred in the cumulative $y\Delta x$ value stored in the channel 18 for the integrator but the pulse does not indicate whether the overflow is positive or negative. The

pulse is indicated at 180 in the chart shown at FIGURE 11.

In all of the vertical columns in the chart shown in FIGURE 11, except for the two at the extreme right, numbers between "1" and "22" are shown corresponding to the 22 integrators in the digital differential analyzer. In the two columns at the extreme right, numbers are shown prefaced by the letters "I" and "P." The letter "I" followed by a number indicates the particular integrator that is moving past the coil 52 at any instant. For example, "I₃" indicates that a pulse position in the third integrator is moving past the coil 52 in the channel 22. Similarly, a designation such as "P₁₃" indicates that the 13th pulse position in the particular integrator is moving past the coil 52.

After the pulse 180 is recorded by the coil 52 in the channel 22, it advances from the coil 52 towards the coil 54. During this time, the first 47 positions of integrator "2" are passing under the coil 52. At the P₄₈I₂ position—or, in other words, the last position of integrator "2"—an indication is recorded by the coil 52 in the channel 22, as indicated at 182 in FIGURE 11. At the P₁I₃ position, the indication 180 passes through the gate circuit 128 and the "or" network 124 to the coil 52. The pulse passes through the gate circuit 128 since the gate circuit opens in the first 47 pulse positions of each integrator. After passing through the gate circuit 128 and the "or" network 125, the pulse 180 is again recorded by the coil 52 in the channel 22, this time at the pulse position adjacent to the indication 182.

Similarly, indications are provided in adjacent pulse positions to show whether or not an over-flow has occurred in the cumulative $\gamma\Delta x$ value for each of the other integrators in the analyzer. These indications are recirculated by the gate circuit 128, which remains open during the first 47 pulse positions of each integrator. At the 48th position for each integrator, the gate circuit 128 closes and prevents any recirculation of old information for the integrator.

At the same time that the gate circuit 128 closes, the gate circuit 123 opens. When the gate circuit 123 opens, the overflow information for the integrator moving past the coil 52 is recorded in the channel 22. In this way, old over-flow information for an integrator is replaced by new over-flow information for the integrator every time that the integrator is presented for computation.

After the indications have been provided in the channel 22 for the 48th pulse position of each integrator, integrator "1" is presented for computation a second time. As the drum 10 rotates through the first 22 positions for the integrator, the output indications for the 22 integrators move in sequence past the coil 54. This causes the output indications in the channel 22 to become available for determining whether or not a Δx increment and Δy increments are actually obtained for the integrator during the second computation. The determination of the occurrence of an actual Δx increment and of actual Δy increments is made by respectively comparing the coding pulses in the channels 16 and 18 with the over-flow pulses in the channel 22. The operation of the digital differential analyzer to obtain such a determination has been disclosed previously.

In FIGURE 1, several bi-stable multivibrators, such as the multivibrator 90, are shown. Furthermore, the construction and operation of these multivibrators have been disclosed above on a general basis. A specific circuit for use as such multivibrators is shown in FIGURE 15. The multivibrator includes a pair of tubes 500 and 502. The grid of each tube is connected to an appropriate output stage. For example, if the circuit shown in FIGURE 15 serves as the multivibrator 90 in FIGURE 1, the grid of the tube 500 would be connected to the output terminal of the gate circuit 104 and the grid of the tube 502 would be connected to the output terminal of the "or" network 106. The cathodes of the

tubes are connected to the coil 62 and to a suitable source of positive biasing voltage.

Connections are respectively made from the plates of the tubes 500 and 502 through suitable coupling capacitances to the grids of tubes 504 and 506. The cathodes of the tubes 504 and 506 are both connected through a suitable resistance and capacitance to a source of negative voltage. The plate of the tube 504 is coupled to the grid of the tube 506 by a suitable resistance 508 and capacitance 510 connected in parallel. Similarly, the plate of the tube 506 is coupled to the grid of the tube 504 through a resistance 512 and a capacitance 514 connected in parallel.

The plate of the tube 504 is also connected to one terminal of a resistance 516, the other terminal of which is connected to an output line 518. Connections are made from the output line 518 to the cathode of a diode 520 and to the plate of a diode 522. The plate of the diode 520 biased at approximately -25 v. and the cathode of the diode 522 is biased at approximately 0 v. The plate of the diode 520 and the cathode of the diode 522 also have common terminals with the plate of a diode 524 and the cathode of a diode 526, respectively. The cathode of the diode 524 and the plate of the diode 526 are connected to an output line 528 and to one terminal of a resistance 530 having its other terminal connected to the plate of the tube 506.

Clock pulses are introduced to the cathodes of the tubes 500 and 502 from the coil 62 to reduce the voltages on these tubes from a positive voltage to approximately 0 volt. Upon the simultaneous introduction of a positive pulse to the grid of one of the tubes, the tube conducts. For example, the tube 500 conducts when a positive pulse of voltage is introduced to it from the gate circuit 104. When the tube 500 conducts, the voltage on the plate of the tube falls and causes the tube 504 to become cut off. Since the tube 504 is no longer conductive, the voltage on the plate of this tube rises. This voltage is introduced through the resistance 508 and capacitance 510 to the grid of the tube 506 to make the tube 506 conductive.

Similarly, the tube 506 becomes conductive when a pulse is introduced to the grid of the tube from the "or" network 106 at the same time that a "clock" pulse is introduced to the cathode of the tube from the coil 62. This causes the tube 506 to become cut off and a relatively high voltage to be produced on the plate of the tube. Upon the production of this high voltage, the tube 504 starts to conduct. In this way, either the tube 504 or the tube 506 conducts at any one time and the other tube is cut off.

The diodes 520, 522, 524 and 526 serve as a clamping network to maintain the voltages on the output lines 518 and 528 at either 0 volt or -25 volts. For example, when a potential of -25 volts is to be produced at the output line 518, current flows through the diode 520 to maintain this potential in case of any tendency of the voltage to become more negative than -25 volts. Similarly, the diode 522 passes a current when a potential of 0 volt is to be produced at the output line 518 and the potential on the line tends to rise above 0 volt.

An operative embodiment of the system illustratively shown in FIGURE 1 and disclosed above is shown in some detail in FIGURES 2 through 6, inclusive. The system includes the channels 14, 16, 18, 20, 22, 24 and 26 and the coils respectively associated with the different channels. For example, the coils 27, 28 and 30 are associated with the channel 14. The coil 27 is connected to the grid of the left tube in a bistable multivibrator 202 (FIGURE 2) and to the input terminal of an inverter 204, the output from which is introduced to the grid of the right tube in the multivibrator 202. In like manner, a multivibrator 206 and an inverter 208; a multivibrator 210 and an inverter 212; a multivibrator 214 and an inverter 216; a multivibrator 218 and an inverter 220; and

a multivibrator 222 and an inverter 224 are respectively associated with the coils 32, 38, 44, 54 and 60.

Connections are made from the plates of the left and right tubes in the multivibrator 206 to input terminals of gate circuits 228 and 230, respectively. Other input terminals of the gate circuits 228 and 230 are connected through a line 232 to a counter 234 corresponding to the counter 66 shown in FIGURE 1. Similarly, the voltages on the plates of the left and right tubes in the multivibrator 210 are respectively introduced to input terminals of gate circuits 236 and 238 having other input terminals connected through the line 232 to the counter 234.

The output signals from the gate circuits 228 and 230 respectively pass through "or" networks 240 and 242 to the grids of the left and right tubes in a bistable multivibrator 244. The voltage on the plate of the left tube in the multivibrator 244 is in turn introduced through an "or" network 245 to the coil 36 for recordation in the channel 16. In like manner, the signals from the gate circuits 236 and 238 respectively pass through "or" networks 246 and 248 to the grids of the left and right tubes in a bistable multivibrator 250. A connection is made from the plate of the left tube in the multivibrator 250 to the coil 42 for the recordation of information in the channel 18. It shall be understood that the bistable multivibrators 244 and 250 each contain circuitry for creating a delay of one pulse position.

The voltage on the plate of the left tube in the multivibrator 206 is not only introduced to the gate circuit 228 but also to a gate circuit 254 having other input terminals connected to the line 232 and to the plate of the left tube in the multivibrator 218. The output signals from the gate circuit 254 pass to input terminals of gate circuits 256 and 258, other input terminals of which are respectively connected to the plates of the left and right tubes in the multivibrator 222. The output terminals of the gate circuit 256 and 258 are connected to a counter 260 corresponding to the counter 80 shown in FIGURE 1 for summing the Δy elements of the dependent variable.

The output terminals of the counter 260 are connected to input terminals of gate circuits such as circuits 262, 264, 266 and 268 having other input terminals connected through a line 270 to the counter 234. Only certain of the gate circuits are shown in FIGURE 2 for purposes of simplicity. The output terminals of the gate circuits such as the circuits 262, 264, 266 and 268 are in turn connected to the grids of the left and right tubes in bistable multivibrators 272, 274, 276 and 278, respectively.

In addition to being connected to the grid of the left tube in the multivibrator 278, the output terminal of the gate circuit 266 is also connected to the grid of the left tube in a bistable multivibrator 280 and to the grid of the right tube in a bistable multivibrator 282. Similarly, the output from the gate circuit 268 is introduced to the grid of the right tube in the multivibrator 280 and the grid of the left tube in the multivibrator 282.

Connections are made from the output terminal of the gate circuit 268 through an "or" network 283 to an "or" network 284, to the grid of the left tube in a bistable multivibrator 292, directly to the grid of the left tube in the bistable multivibrator 286, and to the grids of the right tubes in bistable multivibrator 288 and 290. The output terminal in the gate circuit 266 is connected through an "or" network 291 to the "or" network 284, to the grid of the left tube in the multivibrator 292, directly to the grid of the right tube in the multivibrator 286, and to the grids of the left tubes in the multivibrators 288 and 290.

The plates of the two tubes in each of the multivibrators 292, 286, 288 and 290 are connected to an adder 296. Only certain of these connections are shown for purposes of convenience. The adder 296 also receives the signals from the plates of the two tubes in the multivibrators 272, 274, 276 and 278 and arithmetically combines this information with the signals from the multivibrators 292,

286, 288 and 290. The adder 296 is a four-digit parallel binary adder. One form of such an adder is shown and described on page 41 of a book entitled "Automatic Digital Calculators" by Booth and Booth, published in 1953 by Butterworth Scientific Publications, London. The adder shown therein functions to combine in a parallel manner, binary-coded values registered in two registers. Similarly, the adder 296 functions to additively combine (in a parallel manner), the value registered in the multivibrators 292, 286, 288 and 290 with the value registered in the multivibrators 272, 274, 276 and 278. The results obtained are introduced to the appropriate grids of the two tubes in each of bistable multivibrators 300, 302, 304 and 306. Only certain of the connections to the multivibrators 300, 302, 304 and 306 are shown for purposes of convenience.

As shown in FIGURE 3, the voltages on the plates of both tubes in the multivibrators 202, 206, 210 and 214 are connected to input terminals of gate circuits such as gate circuits 310, 312, 314 and 316. For purposes of simplicity, only the gate circuits 310, 312, 314 and 316 are shown in FIGURE 3. Other terminals of the gate circuits such as the circuits 310, 312, 314 and 316 are connected to the plate of the left tube in a multivibrator 318 corresponding to the multivibrator 98 shown in FIGURE 1 to receive the start pulses. The grid of the left tube in the multivibrator 318 receives its voltage from the output terminal of a gate circuit 320 corresponding to the gate circuit 94 shown in FIGURE 1. Input terminals of the gate circuit 320 are connected to the plate of the left tube in the multivibrator 206 and through a line 322 to the counter 234.

The output signals from the gate circuits such as the gate circuits 310, 312, 314 and 316 are introduced to delay lines such as the delay lines 325, 326, 327 and 328 for a delay of one pulse position. These delay lines may be bistable multivibrators similar to those disclosed above. The output signals from the gate circuits such as the circuits 310, 312, 314 and 316 and from the delay lines such as the lines 325, 326, 327 and 328 are introduced to an adder 324. The operation of the adder 324 is controlled by the voltage on the plate of the left tube in the multivibrator 318 and by signals passing through gate circuits 329 and 330.

In addition to being connected to one of the gate circuits corresponding to the circuits 310, 312, 314 and 316, the plate of the left tube in the multivibrator 210 is connected to input terminals of gate circuits 331, 332 and 334. Connections are made to other input terminals of the gate circuit 331 from the plate of the left tube in the multivibrator 218 and through the line 232 from the counter 234. The signals passing through the gate circuit 331 are applied to the grid of the left tube in a multivibrator 338, the grid of the right tube in the multivibrator being connected through a line 340 to the counter 234.

Like the gate circuit 331, the gate circuits 332 and 334 receive voltages through the line 232 from the counter 234. Voltages are also respectively applied to input terminals of the gate circuits 332 and 334 from the plates of the left and right tubes in the multivibrator 222. The output signals from the gate circuit 332 pass to the grid of the left tube in a bistable multivibrator 350, and the output signals from the gate circuit 334 pass through an "or" network 351 to the grid of the right tube in the multivibrator. Signals from the counter 234 also pass through the line 340 and the "or" network 351 to the grid of the right tube in the multivibrator 350. The voltages on the plates of the left and right tubes in the multivibrator 350 are in turn respectively applied to gate circuits 352 and 354 having other input terminals connected to the plate of the left tube in the multivibrator 338.

The output signals from the gate circuits 352 and 354 are respectively connected to input terminals of the gate circuits 329 and 330, other input terminals of which are connected to the plate of the right tube in a multivibrator

358. The grid of the right tube in the multivibrator 358 is connected to an output terminal of an "or" network 360, input terminals of which are connected to a gate circuit 362 and through the line 340 to the counter 234. Connections are made to input terminals of the gate circuit 362 from the coil 62 in the channel 26 and from the plates of the left tubes in the multivibrators 318 and 358.

The voltage on the plate of the right tube in the multivibrator 358 is also applied to an input terminal of a gate circuit 364. Other input terminals of the gate circuit 364 are connected to the coil 62 and to the plate of the left tube in the multivibrator 318, and the output terminal is connected to the grid of the left tube in the multivibrator 358. In addition, the voltage on the plate of the right tube in the multivibrator 358 is applied to an input terminal of a gate circuit 366, another input terminal of which is connected to the plate of the right tube in the multivibrator 338. The signals passing through the gate circuit 366 are introduced to an "or" network 368 having its output terminal connected to the grids of the left tubes in the multivibrators 300 and 302 and to the grids of the right tubes in the multivibrators 304 and 306.

Connections are made from the plate of the left tube in the multivibrator 358 to input terminals of gate circuits 370 and 372. The gate circuit 370 has a second input terminal connected to the plate of the left tube in the multivibrator 280 and the gate circuit 372 has a second input terminal connected to the plate of the right tube in the multivibrator. The output from the gate circuit 372 is applied to the "or" network 368, and the output from the gate circuit 370 is introduced to the grids of the right tubes in the multivibrators 300 and 302 and to the grids of the left tubes in the multivibrators 304 and 306.

The output from the adder 324 shown in FIGURE 3 is applied to the grids of both tubes in each of the multivibrators 272, 274, 276 and 278 shown in FIGURES 2 and 4. Only certain of these connections are shown for purposes of convenience. The output from the adder 324 is also applied to gate circuits 376 (FIGURE 4) and 378 having other input terminals connected to the plate of the left tube in the multivibrator 318. The output signals from the gate circuits 376 and 378 are in turn respectively introduced to the "or" networks 283 and 291 also shown in FIGURE 2. As previously disclosed, the signals passing through the "or" network 283 and 291 control the operation of the multivibrators 292, 286, 288 and 290.

The output signals passing through the gate circuits 376 and 378 are also respectively introduced to the grids of the left and right tubes in the bistable multivibrator 282 also shown in FIGURE 2. Connections are respectively made from the plates of the left and right tubes in the multivibrator 282 to input terminals of gate circuits 382 and 384, each of which has another input terminal connected to the plate of the left tube in a multivibrator 386.

The grid of the left tube in the multivibrator 386 receives signals from an output terminal of a gate circuit 388 having input terminals connected to the coil 62 in the channel 26 and to the plate of the left tube in the multivibrator 318. The grid of the right tube in the multivibrator 386 has a voltage introduced to it through a line 390 from the counter 234, and the plate of the right tube in the multivibrator has its voltage applied to a gate circuit 392. Other input terminals of the gate circuit 392 are connected to the coil 62 and to the plate of the left tube in the multivibrator 318. The output from the gate circuit 392 passes to the coil 36 through the "or" network 245 also shown in FIGURE 2.

The output signals from the gate circuits 382 and 384 are respectively introduced to the grids of the left and right tubes in a multivibrator 393. As shown in FIGURES 3 and 4, the voltages on the plates of the left and right tubes in the multivibrator 393 are introduced to the

adder 324 for combination with the signals from the multivibrators 300, 302, 304 and 306 and the signals from the gate circuits corresponding to the circuits 312, 314, 316 and 318. As will be disclosed in detail hereinafter, the voltages on the plates of the two tubes in the multivibrator 393 control the carry to one pulse position of the results obtained by the addition in the adder 324 of information provided for a previous pulse position.

As shown in FIGURE 2 and disclosed previously, the output from the multivibrators 272, 274, 276 and 278 is combined in the adder 296 with the output from the multivibrators 292, 286, 288 and 290. The particular pattern of voltages introduced to the adder 296 from the multivibrators 292, 286, 288 and 290 is controlled by the voltages from the gate circuits 266 and 268. The connections to obtain the particular patterns of voltages in the multivibrators 292, 286, 288 and 290 for a high voltage on the output terminals of either the gate circuit 266 or the gate circuit 268 are shown in FIGURE 2 and have been disclosed previously.

The output signals from the adder 296 are applied to gate circuits such as the circuits 394, 395, 396 and 397 in FIGURE 4. Other input terminals of the gate circuits corresponding to the circuits 394, 395, 396 and 397 are connected to the plate of the left tube in the multivibrator 386, and the output terminals of the gate circuits are connected to the grid of one of the tubes in the multivibrators 244 and 250 and in multivibrators 398 and 399.

As shown in FIGURE 5, the voltages on the plates of the left tubes in the multivibrators 206 and 210 are respectively introduced to input terminals of gate circuits 400 and 402. The gate circuits 400 and 402 also receive signals through the line 340 from the counter 234 and introduce their output signals to the grids of the left tubes in bistable multivibrators 404 and 406. The grids of the right tubes in the multivibrators 404 and 406 are connected through the line 390 to the counter 234.

Connections are made from the plate of the left tube in the multivibrator 404 to input terminals of gate circuits 408 and 410 and from the plate of the right tube in the multivibrator 404 to input terminals of gate circuits 412 and 414. The gate circuits 408 and 412 also receive the output signals from a gate circuit 416 having its input terminals connected to the plate of the right tube in the multivibrator 406 and through the line 340 to the counter 234. Other input terminals of the gate circuits 408 and 412 are respectively connected to the plates of the right and left tubes in the multivibrator 350, which is also shown in FIGURE 3. The output signals from the gate circuits 408 and 412 pass through "or" networks 420 and 422 to the coil 58 for recordation in the channel 24.

Other input terminals of the gate circuits 410 and 414 have voltages applied to them from a gate circuit 424, which in turn has input terminals connected to the plate of the left tube in the multivibrator 406 and through the line 340 to the counter 234. The gate circuits 410 and 414 also have input terminals respectively connected to the plates of the left and right tubes in the multivibrator 350. The output signals from the gate circuits 410 and 414 pass through the "or" networks 420 and 422 to the coil 58 for recordation in the channel 24.

Connections are made to a gate circuit 428 from the plates of the left tubes in the multivibrators 282 and 338 and through the line 340 from the counter 234. The output signals from the gate circuit 428 are applied to input terminals of gate circuits 430 and 432. Other input terminals of the gate circuit 430 are connected to the plate of the left tube in the multivibrator 350 and to the plate of the right tube in the multivibrator 404. In like manner, other input terminals of the gate circuit 432 are connected to the plate of the right tube in the multivibrator 350 and the plate of the left tube in the multivibrator 404. The output signals from the gate circuits

430 and 432 pass through "or" networks 434 and 436 to the coil 52 for recordation in the channel 22.

Signals are applied to a gate circuit 438 from the plate of the left tube in the multivibrator 338, from the plate of the right tube in the multivibrator 282 and through the line 340 from the counter 234. The output signals from the gate circuit 438 pass to input terminals of gate circuits 440 and 442. Other input terminals of the gate circuit 440 are connected to the plates of the left tubes in the multivibrators 350 and 404. Connections are also made to other input terminals of the gate circuit 442 from the plates of the right tubes in the multivibrators 350 and 404. The output signals from the gate circuits 440 and 442 pass through the "or" networks 434 and 436 to the coil 52 for recordation in the channel 22.

The signals from a pair of gate circuits 444 and 446 also pass through the "or" networks 436 and 422 for recordation by the coils 52 and 58 in the channels 22 and 24, respectively. Input terminals of the gate circuit 444 are connected to the plate of the left tube in the multivibrator 218 and through a line 448 to the counter 234. Similarly, connections are made to input terminals of the gate circuit 446 from the plate of the left tube in the multivibrator 222 and through the line 448 from the counter 234.

In FIGURE 6, a plurality of gate circuits 450, 452 and 454 are connected in various arrangements to the multivibrators 280, 393 and 404. Connections are made to input terminals of the gate circuit 450 from the plate of the left tube in the multivibrator 280, from the plates of the right tubes in the multivibrators 393 and 404 and through the line 340 from the counter 234. Voltages are applied to input terminals of the gate circuit 452 from the line 340, the plate of the left tube in the multivibrator 404 and the plates of the right tubes in the multivibrators 280 and 393. Similarly, signals pass to input terminals of the gate circuit 454 from the line 340 and the plates of the left tubes in the multivibrators 280, 393 and 404. The output signals from the gate circuits 450, 452 and 454 pass through an "or" network 456 to the grid of the left tube in the multivibrator 276, which is also shown in FIGURE 2.

Signals from the multivibrators 280, 393 and 404 are also applied to gate circuits 460, 462 and 464 in particular arrangements. The gate circuit 460 receives signals from the plates of the left tubes in the multivibrators 393 and 404, from the plate of the right tube in the multivibrator 280 and through the line 340 from the counter 234. Voltages are applied to input terminals of the gate circuit 462 from the line 340 and the plates of the right tubes in the multivibrators 280, 393 and 404. Connections are made to input terminals of the gate circuit 464 from the line 340, from the plates of the left tubes in the multivibrators 280 and 393 and from the plate of the right tube in the multivibrator 404. The output signals from the gate circuits 460, 462, and 464 pass through an "or" network 466 to the grid of the right tube in the multivibrator 276.

As previously disclosed, a pulse is provided in the channel 18 in one of the first 22 positions for each integrator to control the occurrence of a Δx increment for the integrator every time that the integrator is presented for computation. The particular position in which the coding pulse is recorded for the integrator undergoing computation is dependent upon which of the other integrators feeds Δx increments into the integrator undergoing computation. Since the connections between integrators remains constant during the solution of a problem, the coding pulse in the channel 18 in one of the first 22 positions for each integrator remains constant during the solution of the problem. As a result, these pulses have to be retained during the solution of a problem.

Retention of the pulses in the channel 18 is provided by the multivibrator 210 (FIGURE 2), the gate circuits

236 and 238 and stages associated with these gate circuits. The pulses in the channel 18 having a first polarity of magnetization are converted by the coil 38 to pulses of relatively high voltage. These voltage pulses are then introduced to the grid of the left tube in the multivibrator 210 so as to cut off the tube. When the left tube in the multivibrator 210 becomes cut off, a high voltage is produced on the plate of the tube and is introduced to the gate circuit 236.

The gate circuit 236 is opened by a signal from the counter 234 when the first pulse in each integrator is picked up by the coil 62. The gate circuit 236 remains open so that information in the channel 18 up to and including the 22nd pulse position for each integrator can pass through the gate circuit. During the time that the gate circuit 236 remains open, the positive pulses from the plate of the left tube in the multivibrator 210 pass through the gate circuit to the "or" network 246. The network 246 in turn passes to the grid of the left tube in the multivibrator 250 any positive pulses introduced to it. These signals cause the left tube in the multivibrator 250 to become cut off and a positive pulse of voltage to be produced on the plate. The positive voltage pulse passes to the coil 42 for recordation in the channel 18. In this way, the coil 42 operates to produce a magnetic field in the channel 18 similar to the pattern of the electrical signals induced in the coil 38.

In like manner, a pulse of low voltage is induced in the coil 38 to indicate the integer "0" for a pulse position. This voltage pulse is inverted by the inverter 212 and introduced as a positive pulse to the grid of the right tube in the multivibrator 210 to cut off the tube and to produce a positive pulse on the plate of the tube. When such a pulse is produced in one of the first 22 positions for an integrator, the gate circuit 238 opens and the pulse passes through the gate circuit and the "or" network 248 to the grid of the right tube in the multivibrator 250. Since the right tube in the multivibrator becomes cut off upon the introduction of such a pulse, the left tube becomes conductive. This causes a pulse of low voltage to pass to the coil 42 for recordation in the channel 18.

Similarly, the multivibrator 206, the gate circuit 228, the "or" network 240 and the multivibrator 244 in FIGURE 2 operate to recirculate in the channel 16 the positive coding information provided in the first 22 positions of each integrator. As previously disclosed, positive pulses may be provided in the channel 16 in the first 22 positions for each integrator to indicate whether any variations in the value of the dependent quantity y will be made for the integrator.

The gate circuit 254 operates to determine whether or not an actual Δy increment is made for an integrator at the time that a coding pulse appears in the channel 16 in one of the first 22 positions for the integrator. The gate circuit 254 receives the coding pulses in the channel 16 because of its connection to the plate of the left tube in the multivibrator 206. The connection from the counter 234 through the line 232 to the gate circuit 254 causes the gate circuit to become open during the first 22 positions of each integrator. The operation of the counter 234 to provide a relatively high voltage during the first 22 positions of each integrator is fully disclosed in co-pending application Serial No. 217,478, filed March 26, 1951, by Steele and Collison.

Since the gate circuit 254 is also connected to the plate of the left tube in the multivibrator 218, it can open for the passage of a signal only when high voltages are simultaneously produced on the plates of the left tubes in the multivibrators 206 and 218. A relatively high voltage is produced on the plate of the left tube in the multivibrator 218 only when a relatively high voltage is induced in the coil 54. As previously disclosed, the coil 54 indicates in adjacent pulse positions any overflow in the value of the cumulative $y\Delta x$ increments which are obtained for each of the 22 integrators in the analyzer.

The passage of a pulse through the gate circuit 254 indicates only the occurrence of a Δy increment for an integrator, but it does not indicate whether such increment is positive or negative. The polarity of each pulse passing through the gate circuit 254 is indicated by the gate circuits 256 and 258, both of which receive the signals from the gate circuit 254. Since the gate circuit 256 is connected to the plate of the left tube in the multivibrator 222, it receives a relatively high voltage when a relatively high voltage is induced in the coil 60. As previously disclosed, a high voltage from the coil 60 indicates a positive increment. Since the gate circuit 256 passes a signal only when relatively high voltages are simultaneously introduced to it from the gate circuit 254 and from the plate of the left tube in the multivibrator 222, the gate circuit 256 passes a signal only when a Δy increment of positive polarity has occurred.

Each signal passing through the gate circuit 256 for an integrator causes the numerical indications provided by the counter 260 to increase by an integer in a positive direction. For example, a signal passing to the counter 260 from the gate circuit 256 may cause the counter to provide a numerical indication of +3 when an indication of +2 was previously provided by the counter. Similarly, the indications in the counter 260 may change from -3 to -2 upon the introduction of a signal from the gate circuit 256.

As previously disclosed, a positive increment in the cumulative $y\Delta x$ value for an integrator is indicated by the simultaneous occurrence of pulses in the channels 22 and 24. Similarly, a negative increment in the cumulative $y\Delta x$ value for the integrator is indicated by the absence of a pulse in the channel 24 at the time that a pulse is produced in the channel 22. Because of the absence of a pulse in the channel 24, a relatively low voltage is induced in the coil 60. This voltage is inverted by the inverter 224 and is introduced as a relatively high voltage to the grid of the right tube in the multivibrator 222. The high voltage introduced to the grid of the right tube in the multivibrator 222 causes the tube to become cut off and a high voltage to be produced on the plate of the tube.

When a high voltage is produced on the plate of the right tube in the multivibrator 222 at the same time that a positive pulse passes through the gate circuit 254, the gate circuit 258 opens and passes a signal to the counter 260. This signal provides an indication of a negative Δy increment. Since the counter 260 is adapted to provide a negative count as well as a positive count of the Δy increments, it operates upon the introduction of signals from the gate circuit 260 to subtract an integer from the resultant value of the counter. For example, the indications in the counter 260 are changed from +4 to +3 when a signal is introduced to the counter from the gate circuit 258. The operation of the counter 260 in providing a positive and negative count of digital increments is fully disclosed in co-pending application Serial No. 217,478.

As previously disclosed, the counter 260 is formed from a plurality of multivibrators arranged in cascade arrangement. Specifically, four multivibrators are disclosed in co-pending application Serial No. 217,470, now Patent No. 2,654,590. The operation of these multivibrators for a positive or a negative count is controlled by a plurality of gate circuits operative in accordance with logical equations disclosed in the specification and in FIGURE 29 of the co-pending application.

The information in the counter 260 is introduced to the gate circuits such as the circuits 262, 264, 266 and 268 such that each of the gate circuits receives information relating to a binary digit of increasing significance. Because of their connection through the line 270 to the counter 234, the gate circuits such as the circuits 262, 264, 266 and 268 open at pulse position 23 of each integrator to pass to the multivibrators 272, 274, 276 and 278 the information relating to the cumulative value of the Δy increments for each integrator.

The information passing to the multivibrators 272, 274, 276 and 278 from the gate circuits such as the circuits 262, 264, 266 and 268 causes the multivibrators to be triggered in a pattern dependent upon the indications in the counter 260. This causes a corresponding pattern of voltages to be produced on the plates of the multivibrator tubes for introduction to the adder 296. Since the indications provided by the multivibrators 272, 274, 276 and 278 relate to a binary number and since the digital differential analyzer constituting this invention operates on a decimal basis, the adder 296 converts the information from the multivibrators into a decimal form.

The digital differential analyzer constituting this information operates in particular decimal code known as the "excess three" code. In this code, the value "0" is indicated in binary form by 0011 for successive pulse positions, where the least significant digit is at the right. Since an indication of 0011 would ordinarily constitute an indication of the integer "3," the "excess three" code constitutes the normal binary code with a value of +3 added when the number is positive. This may be seen by a comparison of the charts shown in FIGURES 12 and 13, which respectively indicate the "excess three" code and the normal binary code.

As will be seen in the chart shown in FIGURE 12, an indication of "0" for a count in a negative integer is indicated by 1101 where the least significant digit is at the right. This is obtained by inverting the indications of 0011 representing the value of "0" for a positive count so as to obtain a value of 1100 and by adding the binary indication "1" to the least significant digit. The inversion of the indications representing a positive digit and the addition of the indication "1" to the least significant digit of the inverted number constitutes the standard way of indicating a negative number in binary form. Since each of the positive numbers is represented in binary form by indications having a value of 3 added to the indications normally representing the number, the inversion of the number causes negative numbers to be represented by indications which are more negative by a value of "3" than the normal binary indications obtained by the counter 260. For example, as shown in FIGURE 12, the value of -4 is represented in "excess 3" code by 1001. In the normal binary code shown in FIGURE 13, an indication of 1001 will represent a value of -7.

In order to convert the binary number from the counter 260 into a decimal number in the "excess three" code, the polarity of the number must first be determined. As disclosed in detail in co-pending application Serial No. 217,478, each integrator can receive increments from a maximum of only 7 integrators when the integrator is presented for computation. This causes the cumulative value of the Δy increments for each integrator to lie within a range of -7 to +7 every time that the integrator is presented for computation. For positive values up to +7, the counter 260 produces a voltage indicative of the binary value "0" in the binary position of highest significance. This is indicated in the chart shown in FIGURE 13. This signal passes through the gate circuit 268 shown in FIGURE 2. For negative values up to -7, the counter 260 produces a voltage indicative of the binary value "1" in the pulse position of highest significance. This signal passes through the gate circuit 266 in FIGURE 2.

The signals from the gate circuit 268 pass to the grid of the left tube in the multivibrator 282 and cause the tube to be triggered into a state of non-conductivity such that a high voltage is produced on the plate of the tube. The signal from the gate circuit 268 also passes to the grid of the left tubes in the multivibrators 292 and 286 and to the grids of the right tubes in the multivibrators 288 and 290, so as to trigger these multivibrators into states of operation representing the indications 0011, where the least significant digit is at the right.

The multivibrators 292, 286, 288 and 290 are triggered

into operation by a signal from the gate circuit 268 since a signal is also introduced to the multivibrators from the coil 62 through suitable lines (not shown). As shown in FIGURE 13, the indications 0011 represent a value of +3 in binary form. These indications are combined in the adder 296 with the indications from the counter 260 to obtain output indications representing the cumulative value of the Δy increments for an integrator in the "excess three" code.

Similarly, a signal passing through the gate circuit 266 causes the right tube in the multivibrator 282 to be triggered into a state of non-conductivity. Since this signal represents a negative value in the Δy increments for an integrator, a relatively high voltage is produced on the plate of the right tube in the multivibrator 282 to represent such a polarity. The signal passing through the gate circuit 266 also causes the left tubes in the multivibrators 292, 288 and 290 and the right tube in the multivibrator 286 to be triggered into non-conductivity in a pattern represented by 1101 where the least significant digit is at the right. These indications represent a value of -3 in binary form. Since the adder 296 combines these indications with the indications from the counter 260, the adder 296 provides output indications representing the cumulative value of the Δy increments for each integrator in the "excess three" code.

The output indications from the adder 296 are introduced to the multivibrators 300, 302, 304 and 306 (FIGURES 2 and 3) and are in turn applied to the adder 324 (FIGURE 3). Since the adder 324 is connected to the plate of the left tube in the multivibrator 318, it becomes operative only when a relatively high voltage is produced on the tube plate. As previously disclosed, the multivibrator 318 corresponds to the multivibrator 98 shown in FIGURE 1. During the first 22 positions for each integrator, the left tube in the multivibrator 318 is conductive. Upon the occurrence of the first pulse in the channel 16 after the first 22 positions for each integrator, a pulse passes through the gate circuit 320 to trigger the left tube in the multivibrator 318 into a state of non-conductivity. A pulse passes through the gate circuit 320 after the first 22 positions for each integrator because of the introduction of a relatively high voltage to the gate circuit through the line 322 from the counter 234 to prepare the gate circuit for opening.

When the left tube in the multivibrator 318 becomes cut off upon the appearance of the "start" pulse in the channel 16, a relatively high voltage is introduced from the plate of the tube to the gate circuit 388 (FIGURE 4). This voltage passes through the gate circuit during the pulse position following the start pulse because of the connection from the coil 62 to the input terminal of the gate circuit. The signal passing through the gate circuit 388 causes the left tube in the multivibrator 386 to become triggered into a state of conductivity in the pulse position following the start pulse. For example, when the start pulse occurs in the channel 16 in pulse position 27 for an integrator, the left tube in the multivibrator 318 becomes triggered into a state of non-conductivity at pulse position 27 and the left tube in the multivibrator 386 becomes triggered into a state of non-conductivity at pulse position 28.

When the left tube in the multivibrator 318 becomes cut off, it remains cut off until pulse position 48 for the integrator, at which time a signal is introduced to the grid of the right tube in the multivibrator 318 through the line 340 (FIGURE 3) from the counter 234 to cut off the tube. Similarly, when the left tube in the multivibrator 386 becomes cut off for an integrator, it remains cut off until pulse position 1 of the following integrator. At the first pulse position of the following integrator, a signal passes from the counter 234 through the line 390 (FIGURE 4) to the grid of the right tube in the multivibrator 386 to cut off the tube.

When the left tube in the multivibrator 318 becomes

cut off, the signals from the multivibrators 300, 302, 304 and 306 (FIGURE 3) are combined by the adder 324 with the signals passing through the gate circuits corresponding to the circuits 310, 312, 314 and 316. The gate circuits corresponding to the circuits 310, 312, 314 and 316 become opened after the appearance of the "start" pulse because of their connection to the plate of the left tube in the multivibrator 318. When the gate circuits become opened, they pass to the adder 324 the signals appearing in the channels 14, 16, 18 and 20.

In the first pulse position after the start pulse, the signals in the channels 14, 16, 18 and 20 indicate in the "excess 3" code the least significant digit of the value of the dependent quantity y for the integrator undergoing computation. These signals are combined in the adder 324 with the signals representing the cumulative value of the Δy increments for the integrator, as indicated in the multivibrators 300, 302, 304 and 306. The resultant signals produced by the adder 324 provide an indication of the new value of y for the least significant decimal digit of the integrator. This new value of y is uncorrected and therefore must be applied to the adder 296 with correction signals from the multivibrators 292, 286, 288, and 290, to be corrected, as is necessary after an excess 3 code addition. While this correction-addition is taking place in the adder 296, the old value of y is added to the cumulative $y\Delta x$ value in the adder 324. During the next pulse position, which will be even, the next significant digit value of y will be added to the value Δy , in the adder 324 to form an uncorrected new value which is the next significant digit of y . Simultaneously with this addition, the uncorrected sum of y and $y\Delta x$ for the least significant digit will be corrected in the adder 296. It may therefore be seen that the adder 324 performs additions which are corrected by the addition of correction factors in the adder 296.

The combination of the signals in the channels 14, 16, 18 and 20 and the indications in the multivibrators 300, 302, 304 and 306 occurs during the time that the integrator is being advanced from one pulse position to the next. For example, the combination of the information in the channels 14, 16, 18 and 20 in pulse position 27 with the information in the multivibrators 300, 302, 304 and 306 occurs before the end of pulse position 28 for the integrator. This combination occurs in one pulse position even through the indications in four channels must be combined and carry indications must be transferred from one channel to the next.

The operation of the adder 324 in obtaining a new value of y can be given by the following logical equations:

$$\begin{aligned} C_2' &= (C_1' + A_1'B_1')(A_1' + B_1') \\ C_3 &= (C_2 + A_2B_2)(A_2 + B_2) \\ C_4' &= (C_3' + A_3'B_3')(A_3' + B_3') \\ C_0 &= (C_4 + A_4B_4)(A_4 + B_4) \\ W_1' &= (C_2 + A_1'B_1C_1')(A_1'B_1' + C_1') \\ W_2 &= (C_3' + A_2B_2C_2)(A_2 + B_2 + C_2) \\ W_3' &= (C_4 + A_3'B_3C_3')(A_3' + B_3' + C_3') \\ W_4 &= (C_0 + A_4B_4C_4)(A_4 + B_4 + C_4) \end{aligned}$$

In the above equations, B_1 = a relatively high voltage on the plate of the left tube in the multivibrator 202 to represent an indication of "1" in the channel 14 for a pulse position;

B_2, B_3 and B_4 = high voltages on the plates of the left tubes in the multivibrators 206, 210 and 214, respectively, to represent indication of "1" in the channels 16, 18 and 20 for a pulse position;

A_1 = a relatively high voltage on the plate of the left tube in the multivibrator 300 to represent the integer "1" for the least significant digit of the Δy increments;

A_2, A_3 and A_4 = relatively high voltages on the plates of the left tubes in the multivibrators 302, 304 and 306;

C_1 = a relatively high voltage on the plate of the left tube in the multivibrator 393 shown in FIGURES 3 and 4 to indicate a carry from a pulse position of lesser significance to a pulse position of increased significance;

C_2 =a carry resulting from the binary addition of C_1 , B_1 and A_1 ;

C_3 =a carry resulting from the binary addition of A_2 , B_2 and C_2 ;

C_4 =a carry resulting from the addition of A_3 , B_3 and C_3 ; and

C_0 =the output carry resulting from addition of A_4 , B_4 and C_4 ;

W_1 =the result obtained by the addition of A_1 , B_1 and C_1 and represents a relatively high voltage indicative of the integer "1";

W_2 , W_3 and W_4 =the results obtained by the addition of the different values in the pulse positions corresponding to the channels 16, 18 and 20, respectively;

A_1' =the complement of A_1 to represent a relatively high voltage on the plate of the right tube in the multivibrator 300; and

A_2' , A_3' , A_4' , B_1' , B_2' , B_3' , B_4' , C_1' , C_2' , C_3' , C_4' , C_0' , W_1' , W_2' , W_3' , and W_4' represent the complements of the corresponding indications having no prime representations. In the above equations C_2 , C_3 and C_4 represent components which are not specifically shown, but which are included in the box representing the adder 324. Although these components are not specifically shown, it is believed that their construction and operation will be understood by persons skilled in the art from the logical equations listed above and from the chart shown in FIGURE 14.

A carry indication is obtained when the addition of different values causes a full binary indication of +2 to be obtained for a pulse position. In binary form, an indication of "+2" is equivalent to a value of "0" for the pulse position and a carry of "+1" to the next highest digit. For example, when a binary indication of "1" for y in the 26th position of the channel 14 for an integrator is added to a binary indication of "1" for Δy in the multivibrator 300, the resultant value may be "0" in the channel 14 and a carry of "1" into the channel 16. This carry would be provided by a multivibrator representing C_2 in the above equations.

A carry may also be provided from a first pulse position to the next position when a carry from the position immediately preceding the first position is added to the integer "1" indicating the value of either y or Δy for the first position. For example, a carry may be provided from the channel 14 to the channel 16 as disclosed in the previous paragraph. The addition of this carry indication with an indication of "1" representing the value of the dependent quantity y for pulse position 26 in the channel 16 causes a carry to be made into the channel 18. This carry would be indicated by a multivibrator corresponding to C_3 in the above equation.

It should be further appreciated that the logical equations disclosed above are general equations which control the operation of the adder 324 in the different pulse positions. Since no carry is to be retained for use in a subsequent pulse position upon the addition of the dependent quantity y and the incremental quantity Δy in the least significant digit, the multivibrator 393 does not become operative until after this position. The multivibrator 393 is made inoperative at this pulse position because of the operation of the gate circuits 382 (FIGURE 4) and 384, which have a voltage applied to them from the plate of the left tube in the multivibrator 386. Since the left tube in the multivibrator 386 is triggered into a state of non-conductivity one pulse position after the triggering of the left tube in the multivibrator 318, signals cannot pass through the gate circuits 382 and 384 until after the addition of y and Δy in the least significant digit.

The new value of the dependent quantity y in the least significant digit is introduced by the adder 324 to the multivibrators 272, 274, 276 and 278. Sometimes, upon the addition of signals representing the values of y and Δy , a carry is obtained from the last digit. For example,

when a value of +7 in the "excess 3" decimal code is added to a value of +5 in the same code, a carry is produced in the last position corresponding to the information in the channel 20. This carry is represented by the term C_0 in the logical equations disclosed above and in the chart shown in FIGURE 14 and is indicated by a high voltage which is introduced to the grid of the left tube in the multivibrator 282. This voltage causes the left tube in the multivibrator 282 to become cut off and a relatively high voltage to be produced on the plate of the tube.

At the next pulse position, the high voltage on the plate of the left tube in the multivibrator 282 passes through the gate circuit 382 and causes the left tube in the multivibrator 393 to become cut off. Since the voltage from the multivibrator 393 is introduced to the adder 324, the carry indications produced by the adder 324 are reintroduced to the adder after a delay of one pulse position. At this time, information relating to the values of y and Δy in the decimal digit of next highest significance are being combined by the adder 324. In this way, a carry is obtained from one decimal digit to the next so that a proper addition can be obtained.

As discussed in connection with the simplified embodiment shown in FIGURE 1, indications relating to the dependent quantity y and to the differential combination $y\Delta x$ for each integrator are alternately presented in successive pulse positions in the channels 14, 16, 18 and 20. For example, indications relating to the value of y for decimal digits of increasing significance may be successively presented in pulse positions 26, 28, 30, etc. in the channels 14, 16, 18 and 20. Similarly, indications relating to the cumulative value of the differential combination $y\Delta x$ for an integrator may be successively presented in pulse positions 27, 29, 31, etc. in the channels 14, 16, 18 and 20.

Since the adder 324 alternately operates to obtain new values for y and $y\Delta x$ for each integrator, some control must be provided to insure that the values of y and $y\Delta x$ do not become mixed. This control is provided by the operation of the multivibrator 358 shown in FIGURE 3. This multivibrator corresponds to the multivibrator 90 shown in FIGURE 1. The operation of the multivibrator 358 is in turn controlled by the gate circuits 362 and 364. Because of the connection to input terminals of the gate circuits 362 and 364 from the plate of the left tube in the multivibrator 318, the multivibrator 358 does not become operative until after the appearance of the "start" pulse in the channel 16.

When the "start" pulse appears in the channel 16, the first clock signal induced in the coil 62 after the "start" pulse passes through the gate circuit 364 and causes the left tube in the multivibrator 358 to become cut off. The resultant high voltage on the plate of the left tube in the multivibrator 358 is introduced to the gate circuit 362 to prepare the gate circuit for the passage of a signal upon the production of the next clock signal by the coil 62. This clock signal passes through the gate circuit 362 and the "or" network 360 to the grid of the right tube in the multivibrator 358 and causes the tube to become cut off.

Since the voltage on the plate of the right tube in the multivibrator 358 is introduced to the gate circuit 364, the gate circuit becomes prepared to pass the next clock signal from the coil 62. In this way, the left and right tubes in the multivibrator 358 become alternately triggered into states of non-conductivity upon the introduction of successive clock signals from the coil 62. At pulse position 48 for each integrator, a signal passes from the counter 234 through the line 340 and the "or" network 360 to the grid of the right tube in the multivibrator 358. This signal causes the right tube in the multivibrator 358 to become cut off if it happens to be conductive at that time.

In this way, the left tube in the multivibrator 358 becomes prepared for an initial triggering after the ap-

pearance of the "start" pulse in the next integrator. By insuring that the left tube in the multivibrator 358 becomes initially triggered for each integrator, coordination is provided between the operation of the multivibrator 358 and the introduction of information to the adder 324. This results from the fact that information relating to the dependent quantity y appears in the channels 14, 16, 18 and 20 in the first pulse position after the "start" pulse for each integrator.

The relatively high voltage produced in alternate pulse positions on the plate of the left tube in the multivibrator 358 is introduced to the gate circuits 370 and 372. Since the gate circuits 370 and 372 are also respectively connected to the plate of the left and right tubes in the multivibrator 280, either the gate circuit 370 or the gate circuit 372 is prepared for opening at all times in alternate positions.

As shown in FIGURE 2, the grids of the left and right tubes in the multivibrator 280 respectively receive the signals passing through the gate circuits 266 and 268. The signals through these gate circuits respectively represent Δy increments of negative and positive polarity. Because of this, a relatively high voltage on the plate of the left tube in the multivibrator 280 indicates that the cumulative value of the Δy increments for an integrator are negative. Similarly, a relatively high voltage is produced on the plate of the right tube in the multivibrator 280 when the cumulative value of the Δy increments is positive. As a result of the operation of the gate circuits 266 and 268, the multivibrator 280 becomes triggered into one state of operation or the other at pulse position 23 for each integrator. The multivibrator then remains in this state during the remaining pulse positions for the integrator.

As disclosed in co-pending application Serial No. 217,478 the value of the Δy increments for each integrator appears only in the first pulse positions for the integrator. In the remaining pulse positions the indication as to the sign of the Δy increments is repeated. Since the analyzer disclosed in the co-pending application Serial No. 217,478 operates on a binary basis, a binary indication of "0" is added to the value of y in successive pulse positions when the cumulative value of the Δy increments is positive. In like manner, a binary value of "1" is added in successive pulse positions when the cumulative value of the Δy increments for an integrator is negative.

For reasons which will be disclosed in detail hereinafter, indications of 0011 are added to the value of y after the first decimal digit for an integrator in the analyzer constituting this invention to represent that the cumulative value of the Δy increments for the integrator is positive. Such indications are introduced to the adder 324 by the multivibrators 300, 302, 304 and 306 (FIGURE 3) when a signal passes through the gate circuit 372. Similarly, indications of 1100 are added to the value of y after the first decimal digit to indicate that the cumulative value of the Δy increments for an integrator is negative. This pattern is produced in the multivibrators 300, 302, 304 and 306 when a signal passes through the gate circuit 370.

It has already been disclosed that indications relating to the cumulative value of $y\Delta x$ for each integrator are presented in alternate pulse positions in the channels 14, 16, 18 and 20. These indications are presented to the adder 324, which combines them with the signals representing the $y\Delta x$ increment. However, in order to have a $y\Delta x$ increment, a Δx increment must be obtained. The gate circuits 331, 332 and 334 and the multivibrators 338 and 350 operate to determine the occurrence of each Δx increment and the polarity of each such increment.

Since the pulse controlling the occurrence of each Δx increment for an integrator occurs in one of the first 22 pulse positions for the integrator, the gate circuit 331 is prepared for opening during these positions. The gate circuit is so prepared by the introduction of a relatively

high voltage through the line 232 from the counter 234. The voltage on the plate of the left tube in the multivibrator 210 is also introduced to the gate circuit 331 since the coding pulse occurs in the channel 18. When a relatively high voltage is simultaneously produced on the plate of the left tube in the multivibrator 218, a signal passes through the gate circuit 331 to indicate that a Δx increment has actually occurred for the integrator undergoing computation.

The signal passing through the gate circuit 331 causes the left tube in the multivibrator 338 to become cut off and a relatively high voltage to be produced on the tube plate. This high voltage continues during the remaining pulse positions of the integrator. At pulse position 48 of each integrator, the multivibrator 338 becomes cut off as a result of the introduction of a signal through the line 340 from the counter 234. In this way, the multivibrator 338 indicates the actual occurrence of a Δx increment during the time that the information relating to the cumulative value of $y\Delta x$ for the integrator is presented to the adder 324.

The voltages on the plate of the left tube in the multivibrator 210 and on the line 232 are introduced to the gate circuits 332 and 334 as well as to the gate circuit 331. This causes the gate circuits 332 and 334 to be prepared for opening at a particular one of the first 22 positions for each integrator corresponding to the position in which the Δx coding pulse appears in the channel 18. When a relatively high voltage is produced on the plate of the left tube in the multivibrator 222 at the same time as the introduction of the coding pulse to the gate circuit 332, a signal passes through the circuit to indicate that any Δx increment is positive.

The signal from the gate circuit 332 passes to the grid of the left tube in the multivibrator 350 and cuts off the tube. The left tube in the multivibrator 350 then remains cut off during the remaining pulse positions for the integrator. At pulse position 48 for the integrator, a signal is introduced to the grid of the right tube in the multivibrator 350 through the line 340 and the "or" network 351 to cut off the tube and make the left tube in the multivibrator conductive. In this way, the left tube in the multivibrator 350 remains cut off for a positive Δx increment for an integrator during all of the time that the information relating to the cumulative value of the $y\Delta x$ increments for the integrator appears in the channels 14, 16, 18 and 20.

The induction of a relatively low voltage in the coil 60 causes the right tube in the multivibrator 222 to become cut off. When the right tube in the multivibrator 222 becomes cut off at the same time that a coding pulse appears in the channel 18 in one of the first 22 positions for an integrator, a signal passes through the gate circuit 334 and the "or" network 351. This signal provides an indication that any Δx increment for the integrator undergoing computation is negative. The signal passes to the grid of the right tube in the multivibrator 350 and causes the tube to become cut off. The right tube in the multivibrator 350 then remains cut off during the remaining pulse positions for the integrator.

Upon the simultaneous production of relatively high voltages on the plates of the left tubes in the multivibrators 338 and 350, a signal passes through the gate circuit 352. This signal provides an indication that a Δx increment has actually occurred and that the increment has a positive polarity. The signal from the gate circuit 352 is introduced to the gate circuit 329.

Because of its connection to the plate of the right tube in the multivibrator 358, the gate circuit 329 opens at alternate pulse positions to provide for the passage of a signal to the adder 324. The adder 324 then combines the signals from the gate circuits such as the circuits 310, 312, 314 and 316 with the signals from the delay lines 325, 326, 327 and 328 to produce new indications representing the cumulative value of the $y\Delta x$ increments.

As previously disclosed, the delay lines 325, 326, 327 and 328 delay by one pulse position the value of the dependent quantity y in the channels 14, 16, 18 and 20 so that they will coincide with the signals relating to the cumulative value of the $y\Delta x$ increments in the channels 14, 16, 18 and 20. The combination of a particular $y\Delta x$ increment with the cumulative value of the $y\Delta x$ increments upon the occurrence of a positive Δx increment is fully disclosed in co-pending application Serial No. 217,478 and in co-pending Serial No. 362,584, filed June 18, 1953, and now Patent No. 2,900,135, by Reno V. Benaglio et al.

In like manner, a signal passes through the gate circuit 354 when relatively high voltages simultaneously occur on the plate of the left tube in the multivibrator 338 and on the plate of the right tube in the multivibrator 350. This signal indicates that a Δx increment has actually occurred and that the polarity of the increment is negative. In alternate pulse positions, the signal from the gate circuit 354 passes through the gate circuit 330 to the adder 324. The signal operates on the adder to cause the indications from the delay lines 325, 326, 327 and 328 to be inverted. Inversion of these indications upon the occurrence of a negative Δx increment results from the fact that $(y)(-\Delta x) = (-y)(\Delta x)$. The inversion of the indications relating to y for a negative Δx increment is fully disclosed in co-pending application Serial No. 217,478 disclosed above and in co-pending application Serial No. 362,584, filed June 18, 1953, by Reno V. Benaglio et al. Since it is fully disclosed in the co-pending applications it is not fully disclosed in this application and fully shown in the drawings in the interest of simplification.

The indications obtained by the adder 324 in successive pulse positions are introduced to the multivibrators 272, 274, 276 and 278. The resultant indications produced in the multivibrators 272, 274, 276 and 278 then pass to the adder 296 (FIGURE 4) for combination with the signals from the multivibrators 292, 286, 288 and 290. As will be disclosed in detail hereafter these multivibrators provide a corrective factor which is necessary to obtain proper decimal indications when the analyzer operates in the "excess three" decimal code.

The corrective factor provided by the multivibrators 292, 286, 288 and 290 is dependent upon a carry or lack of carry from the addition of information in the adder 324. For example, when the combination of signals in the adder 324 causes a carry C_0 to be introduced from the adder to the multivibrator 282 (FIGURE 4), a corrective factor of 0011 is provided by the multivibrators 292, 286, 288 and 290. Thus, the multivibrators 292 (FIGURE 2) and 286 provide indications of the integer "1" and the multivibrators 288 and 290 provide indications of the binary value "0."

Sometimes a carry is not obtained from the adder 324 when signals are combined in the adder. A lack of a carry from the adder 324 is indicated by a relatively high voltage on the plate of the right tube in the multivibrator 282. When this occurs, the multivibrators 292, 286, 288 and 290 introduce a corrective factor of 1101 to the adder 296, where the least significant digit is at the right.

Since the analyzer constituting this invention operates in the "excess three" decimal code, each number has a corrective value of 3 applied to it. Thus, when the adder 324 adds two positive numbers, each number has a corrective factor of +3 added to it. The resultant number obtained by the adder 324 has a corrective factor of +6. Although the adder 324 combines two numbers in the "excess three" code, each number is still formed from a plurality of binary indications. In the binary code, a carry cannot be obtained until a binary number equivalent to a decimal indication of "16" has been obtained. Since an indication of "16" is greater by a value of "6" than a value of "10" required to obtain a carry in normal decimal operation, the excess factor of +6 obtained by

the adder 324 makes up this difference. However, the new number obtained by the adder 324 now has to have a value of +3 added to it to return it to the "excess three" code. Such a corrective factor of +3 is represented in binary form by 0011 and is added in the adder 296 to the indications from the adder 324 to return these indications to the proper value.

When an output carry does not occur upon the addition of two numbers in the adder 324, a value having a corrective factor of +6 is obtained. Since only a corrective factor of +3 is required to convert a binary number into the "excess three" code, a value of 3 must be subtracted from the number obtained by the adder 324. This value is obtained by inverting the indications of 0011 representing +3 into indications of 1100 and adding 1 to the least significant digit. The resultant indications of 1101 represent a value of -3 in binary form. The indications of 1101 is added in the adder 296 to the indications from the adder 324 to return these indications to their proper value.

The operation of the multivibrators 292, 286, 288 and 290 to produce indications of 0011 and indications of 1101 have been previously disclosed in detail. As previously disclosed and shown in FIGURE 2, the operation of the multivibrators 292, 286, 288 and 290 to obtain these indications is controlled by the signals from the "or" networks 283 and 291. As shown in FIGURES 2, and 4, a signal passes through the gate circuit 376 and the "or" network 283 to produce a pattern of 0011 in the multivibrators 292, 286, 288 and 290 when a carry indication is obtained by the adder 324. Similarly, a signal passes through the gate circuit 378 and the "or" network 291 to produce a pattern of 1101 in the multivibrators 292, 286, 288 and 290 when no carry is obtained in the adder 324.

The resultant indications obtained by the adder 296 in combining the indications in the multivibrators 272, 274, 276 and 278 and in the multivibrators 292, 286, 288 and 290 represent in alternate positions the new value of the dependent quantity y for each integrator. These indications pass from the adder 296 through the gate circuits such as the circuits 394, 395, 396 and 397 (FIGURE 4) to the multivibrators 398, 244, 250 and 399. The indications then pass from the multivibrators 398, 244, 250 and 399 to the coils 30, 36, 42 and 48 for the recordation of the information in the channels 14, 16, 18 and 20, respectively.

The information passing through the gate circuits such as the circuits 310, 312, 314 and 316 to represent the value of y for each integrator is delayed by one pulse position. The information is delayed by the delay lines 325, 326, 327 and 328, which may be bistable multivibrators. The information then passes to the adder 324 (FIGURE 3) for combination with the signals provided in the channels 14, 16, 18 and 20 to represent the cumulative value of the $y\Delta x$ increments for the integrator. The indications produced by the adder 324 to represent the new cumulative value of the $y\Delta x$ increments are then corrected in the adder 296 by a factor of +3 or -3. The resultant indications are introduced to the multivibrators 398, 244, 250 and 399 (FIGURE 4) for recordation in the channels 14, 16, 18 and 20, respectively.

When a Δx increment does not occur for an integrator, neither the gate circuit 329 (FIGURE 3) nor the gate circuit 330 is able to open in alternate pulse positions. This prevents the value of y from being either added to or subtracted from the cumulative value of the $y\Delta x$ increments for the integrator. However, since a Δx increment has not occurred, the voltage on the plate of the right tube in the multivibrator 338 is relatively high. This causes the gate circuit 366 to open in the alternate pulse positions in which a relatively high voltage is introduced to the gate circuit from the plate of the right tube in the multivibrator 358. As previously disclosed,

a relatively high voltage is produced on the plate of the right tube in the multivibrator 358 at the alternate pulse positions corresponding to the presentation of the $y\Delta x$ increments for computation.

Upon the passage of a signal through the gate circuit 366 and the "or" network 363, the left tubes in the multivibrators 300 and 302 and the right tubes in the multivibrator 304 and 306 become triggered into states of non-conductivity. This causes the multivibrators 300, 302, 304 and 306 to produce a pattern of indications representing 0011, where the least significant digit is at the right. This corresponds to an indication of the integer "3" in binary form. These indications are then combined in the adder 324 with the indications representing the cumulative value of the $y\Delta x$ increments in the channels 14, 16, 18 and 20.

As will be seen in the chart shown in FIGURE 12, no carry indication is obtained when indications of 0011 are combined with any positive number between 0 and 9 or with any negative number between 0 and -9. Since no carry indication is obtained in the adder 324 by the addition of 0011, the multivibrators 292, 286, 288 and 290 are triggered into a pattern representing 1101 by a signal passing through the gate circuit 378 and the "or" network 291. This corresponds to an indication of -3. In this way, the adder 296 subtracts the value of 3 that is added to the $y\Delta x$ increments in the adder 324. The resultant indications obtained by the adder 296 correspond to the indications introduced to the adder 324 from the channels 14, 16, 18 and 20. As a result, the indications representing the cumulative value of the $y\Delta x$ increments for each integrator are circulated in the channels 14, 16, 18 and 20 when a Δx increment is not obtained for the integrator.

Sometimes an overflow occurs in the cumulative value of the $y\Delta x$ increments stored in the channels 14, 16, 18 and 20. For example, if a decimal value of "1,000" is the maximum value that can be stored in the channels 14, 16, 18 and 20 for an integrator, an overflow occurs in the channel 20 when a decimal value of "6" representing a $y\Delta x$ increment for the integrator is added to a decimal value of "996" previously stored in the channel for the integrator.

An overflow in the cumulative value of the $y\Delta x$ increments stored in the channels 14, 16, 18 and 20 for an integrator can occur only upon a combination of the indications in pulse position 47 for the integrator. The overflow can occur only upon such a combination since the information relating to the digit of highest significance for the $y\Delta x$ increments occurs in pulse position 47. When an overflow occurs in pulse position 47, it is carried into pulse position 48.

Since an overflow from the channel 20 can occur only from pulse position 47 to pulse position 48 for each integrator, the gate circuits 428 and 438 (FIGURE 5) open only at position 48. This results from the connection made from the counter 234 through the line 340 to the gate circuits 428 and 438. As disclosed above, an overflow can occur only when a $y\Delta x$ increment is added to the cumulative value of the $y\Delta x$ increments previously obtained for the integrator. Since a $y\Delta x$ increment for an integrator can be obtained only upon the actual occurrence of a Δx increment, a connection is made from the plate of the left tube in the multivibrator 338 to input terminals of the gate circuits 428 and 438. This prevents the gate circuits 428 and 438 from opening except upon the actual occurrence of a Δx increment.

The gate circuit 428 is able to open only when a relatively high voltage is introduced to it from the plate of the left tube in the multivibrator 282 to indicate a positive carry from the adder 324. A positive carry is produced by the adder 324 to represent an overflow when a positive increment of $y\Delta x$ is added to indications having a positive polarity and representing the cumulative value of $y\Delta x$. A positive $y\Delta x$ increment is

obtained when both y and Δx are positive and when both y and Δx are negative. This results from the fact that $(y)(\Delta x) = (-y)(-\Delta x)$.

The gate circuit 430 passes a signal when a carry is produced by the adder 324 in pulse position 48 and y and Δx are both positive. The gate circuit passes a signal for such a set of conditions because a relatively high voltage on the plate of the left tube in the multivibrator 350 indicates a positive Δx increment and a relatively high voltage on the plate of the right tube in the multivibrator 404 indicates a positive value of y . The operation of the multivibrator 404 to provide such an indication will be disclosed in detail hereafter. The signal passing through the gate circuit 430 also passes through the "or" networks 434 and 436 to the coil 52 for recordation in the channel 22. As previously disclosed, successive pulse positions in the channel 22 are utilized to indicate whether or not an overflow has occurred in the cumulative value of the $y\Delta x$ increments for the different integrators.

Similarly, the gate circuit 432 opens when a carry is made by the adder 324 into pulse position 48 for an integrator and the values of y and Δx are both negative. The simultaneous occurrence of such conditions is indicated by relatively high voltages on the output terminals of the gate circuit 428, the plate of the right tube in the multivibrator 350 and the plate of the left tube in the multivibrator 404. Since such a simultaneous occurrence of conditions indicates that an overflow has actually occurred in the indications provided in the channels 14, 16, 18 and 20, a signal passes from the gate circuit 432 through the "or" networks 434 and 436 to the coil 52 for recordation in the channel 22.

As will be seen in the chart shown in FIGURE 12, negative numbers between -6 and -9 are represented in the "excess three" code by an indication of "0" in the last pulse position. It will be further seen that a negative count occurs by substituting the indication "0" for the indication "1" in pulse positions of increasing significance. This results from the fact that a negative number can be indicated by an inversion of the corresponding positive indications and the addition of a binary indication "1" to the pulse position of least significance.

For the above reasons, a negative overflow can occur when no output carry is produced by the adder 324. Since such an overflow can occur only for negative numbers, a negative increment of $y\Delta x$ must be added to a negative number representing the cumulative value of the $y\Delta x$ increments in the channels 14, 16, 18 and 20. A negative increment of $y\Delta x$ can be obtained by having either y negative and Δx positive, or by having y positive and Δx negative. In other words,

$$(-y)(\Delta x) = (y)(-\Delta x)$$

The gate circuits 438, 440 and 442 provide a determination as to whether an overflow in the negative value of the $y\Delta x$ increments has occurred when such increments are negative. Since the gate circuit 438 is connected through the line 340 to the counter 234, it can open only in pulse position 48 for each integrator. As previously disclosed an overflow in the cumulative value of $y\Delta x$ for each integrator can occur only in this pulse position. Because of its connection to the plate of the left tube in the multivibrator 338, the gate circuit becomes opened only when a Δx increment has actually occurred for an integrator. In addition, the gate circuit 438 can become opened only when an output carry indication is not provided by the multivibrator 282. This results from the connection between the gate circuit and the plate of the right tube in the multivibrator 282.

The signals passing through the gate circuit 438 are introduced to the gate circuits 440 and 442. The gate circuit 440 passes a signal when a negative $y\Delta x$ increment is produced by a negative value of y and a positive value of Δx . This results from the connections respec-

tively made to input terminals of the gate circuit from the multivibrators 404 and 350. Similarly, the gate circuit 442 becomes opened only when y is positive and Δx is negative. The signals from the gate circuit 440 and 442 pass through the "or" networks 434 and 436 to the coil 52 for the recordation of a positive signal in the channel 22.

The operation of the gate circuits 428, 430 and 432 and the gate circuits 438, 440 and 442 in producing an overflow indication in the channel 22 for an integrator can be given by the following logical equation:

$$Z_t = P_{43} B_6 [(B_2' B_5 + B_2 B_5') C_c + (B_2 B_5 + B_2' B_5') C_c']$$

In the above equation,

Z_t = a pulse of relatively high voltage introduced to the coil 52 to indicate an overflow in the cumulative value of the $y\Delta x$ increments for an integrator;

B_6 = a relatively high voltage on the plate of the left tube in the multivibrator 338 to indicate that a Δx increment has actually occurred for the integrator;

B_2 = a relatively high voltage on the plate of the left tube in the multivibrator 404 to indicate that the value of y for the integrator is negative;

B_5 = a relatively high voltage on the plate of the left tube in the multivibrator 350 to indicate that any Δx increment for the integrator is positive;

C_c = a relatively high voltage on the plate of the left tube in the multivibrator 282 to indicate that a positive carry has been obtained from the adder 324; and

B_2', B_5', B_5', C_c' = relatively high voltages on the plates of the right tubes in their respective multivibrators to indicate an inverse of that provided by high voltages on the plates of the left tubes in the multivibrators.

The signals passing to the coil 52 for recordation in the channel 22 indicate only that an overflow has occurred in the cumulative value of the $y\Delta x$ increments for an integrator. Such a signal does not indicate whether the increments are positive or negative. The polarity of each such overflow is indicated by the passage of signals to the coil 58 for recordation in the channel 24. When a positive signal passes to the coil 58, an indication is provided that a positive overflow in the $y\Delta x$ increments has occurred. The absence of such a positive signal indicates that a negative overflow in the cumulative value of the $y\Delta x$ increments has occurred.

In co-pending application, Serial Number 217,478, a coding pulse is provided in pulse position 48 of the channel containing the $y\Delta x$ information for each integrator. Since this channel corresponds to the channel 18 in the analyzer constituting this invention, coding information is inserted in the channel 18 at pulse position 48 for each integrator. This coding information provides an indication as to whether or not the polarity of the overflow indications for the $y\Delta x$ increments have to be inverted. The appearance of a positive pulse in pulse position 48 for an integrator indicates that the polarity of the cumulative value of the $y\Delta x$ increments for the integrator has to be inverted. Similarly, the absence of a pulse in the channel 18 in position 48 for an integrator indicates that the polarity of the cumulative value of $y\Delta x$ does not have to be inverted.

Since the coding information in the channel 18 in pulse position 48 for each integrator must be retained during computation, a circuit is provided for recirculation of this information in the channel 18. This circuit includes the coil 38, the multivibrator 210, the gate circuit 402, the "or" network 445, and the coil 42. The gate circuit 402 opens at pulse position 48 for each integrator to pass a positive coding signal in the channel 18 since the gate circuit is connected through the line 340 to the counter 234.

The passage through the gate circuit 402 of a positive coding pulse at pulse position 48 for an integrator causes the left tube in the multivibrator 406 to become triggered

into a state of non-conductivity. The left tube in the multivibrator 406 then remains cut off for one pulse position. At pulse position 1 of the following integrator, a signal is introduced to the grid of the right tube in the multivibrator 406 through the line 390 from the counter 234. This signal causes the right tube in the multivibrator 406 to become cut off. In this way, the left tube in the multivibrator 406 can become cut off for a duration of only one pulse position in each integrator.

The voltage on the plate of the right tube in the multivibrator 406 is introduced to the gate circuit 416. Since the right tube in the multivibrator 406 remains cut off at pulse position 48 for an integrator only when the cumulative value of the $y\Delta x$ increments for the integrator is positive, the gate circuit 416 becomes open only when the polarity of the $y\Delta x$ increments does not have to be inverted. The gate circuit 416 can become open only at pulse position 48 for each integrator because of its connection through the line 340 to the counter 234.

When the gate circuit 416 opens, a signal passes to the gate circuits 408 and 412. A signal then passes through gate circuit 412 when the values of y and Δx are both positive in the $y\Delta x$ increment just obtained for the integrator. This results from the connection to input terminals of the gate circuit from the plate of the right tube in the multivibrator 404 and the plate of the left tube in the multivibrator 350. When the gate circuit 412 opens, the signal passes through the gate circuit and the "or" networks 420 and 422 to the coil 58 for recordation in the channel 24. This signal provides an indication that a positive overflow has occurred in the cumulative value of the $y\Delta x$ increments stored in the channels 14, 16, 18 and 20.

Similarly, the gate circuit 408 opens when both y and Δx are negative for the $y\Delta x$ increment just obtained for the integrator undergoing computation. Since both y and Δx are negative, a positive $y\Delta x$ increment is produced. This causes the overflow in the cumulative value of the $y\Delta x$ increments for the integrator to be positive. Such a positive overflow is indicated by the passage of a signal through the gate circuit 408 and the "or" networks 420 and 422 to the coil 58 for recordation in the channel 24.

It has previously been disclosed that a negative overflow in the cumulative value of the $y\Delta x$ increments can occur. Such a negative overflow can occur only when a negative $y\Delta x$ increment is added to negative indications in the channels 14, 16, 18 and 20. A negative $y\Delta x$ increment for an integrator can result when either y is positive and Δx is negative or when y is negative and Δx is positive.

The gate circuit 414 is connected to the multivibrators 350 and 404 to become prepared for opening when y is positive and Δx is negative. Similarly, the gate circuit 410 receives voltages from the multivibrators 350 and 404 to become prepared for the passage of a signal when y is negative and Δx is positive. Signals are able to pass through the gate circuits 410 and 414 only upon the introduction of a relatively high voltage from the gate circuit 424.

The gate circuit 424 is able to open only at pulse position 48 for each integrator because of its connection through the line 340 to the counter 324. Since the gate circuit is also connected to the plate of the left tube in the multivibrator 406, a signal passes through the gate circuit only when the polarity of the indications in the channels 14, 16, 18 and 20 have to be inverted. Because of this requirement for inversion, a signal passing through the gate circuit 424 causes a negative overflow to be inverted into a positive overflow. In this way, the signals passing through the gate circuits 410 and 414 provide an indication of a positive overflow in the cumulative value of the $y\Delta x$ increments for an integrator. These signals pass through the "or" networks 420 and 422 to the coil 58 for recordation in the channel 24.

The operation of the gate circuits 416, 408 and 412 and

of the gate circuits 424, 410 and 414 to provide indications of positive overflows in the cumulative $y\Delta x$ increments can be given by the following logical equation:

$$Z_s = P_{43}[(B_2'B_5 + B_2B_5')B_3' + (B_2B_5 + B_2'B_5')B_3]$$

In the above equation,

Z_s = a pulse of relatively high voltage introduced to the coil 58 to indicate a positive overflow in the cumulative value of the $y\Delta x$ increments for an integrator;

B_3 = a relatively high voltage on the plate of the left tube in the multivibrator 406 to indicate an inversion in the polarity of the cumulative $y\Delta x$ increments for the integrator;

And B_2 and B_5 have previously been defined.

In co-pending application Serial No. 217,478 the 48th pulse position for each integrator in the channel containing the y information is utilized to indicate the sign of y . This channel corresponds to the channel 16 in the analyzer constituting this invention. In accordance with the operation of the analyzer disclosed in co-pending application 217,478 a positive pulse is provided in the channel 16 in pulse position 48 for each integrator when the value of y for the integrator is negative. Correspondingly, no positive pulse is provided in this pulse position when the value of y is positive.

The components shown in FIGURE 6 are included to determine whether the value of y for each integrator is positive or negative at any instant. This determination is necessary since Δy increments are being combined with the value of y for each integrator every time that the integrator is presented for computation. For example, negative Δy increments representing a value of -3 may be added to a value of y representing a value of $+2$. This causes the new value of y to be -1 and requires that the coding pulse representing the sign of y be changed.

The components shown in FIGURE 6 are included to determine the sign of the y information for each integrator. The components include the gate circuits 450, 452 and 454, which are utilized to determine negative values of y . The gate circuit 454 opens for the passage of a signal upon the simultaneous introduction of signals from the plates of the left tubes in the multivibrators 280, 393 and 404. Because of its connections, the gate circuit 454 passes a signal when the values of y and Δy are both negative and there is a carry. As has previously been disclosed, indications of 1100 are added to the value of y when the cumulative value of the Δy increments for an integrator are negative. The gate circuit 454 opens only when a positive carry occurs since the addition of 1100 to any of the negative numbers shown in the chart in FIGURE 12 causes a carry to be obtained. For example, the addition of 1100 to an indication of 1100 representing -1 or to an indication of 0100 representing -9 causes a carry to be obtained.

The signal passing through the gate circuit 454 is introduced through the "or" network 456 to the grid of the left tube in the multivibrator 276. This signal causes the left tube in the multivibrator 276 to become cut off and a high voltage to be produced on the tube plate. The high voltage from the multivibrator 276 in turn causes the left tube in the multivibrator 244 to become cut off. The resultant high voltage on the plate of the left tube in the multivibrator 244 passes through the "or" network 245 for recordation by the coil 36 in the channel 16. In this way, an indication is provided in the channel 16 that the value of y for the integrator is negative.

Because of its connections to the multivibrators 280, 393 and 404, the gate circuit 450 passes a signal when the value of y for an integrator is positive, the cumulative value of the Δy increments for the integrator is negative and there is no carry. Since the cumulative value of the Δy increments is negative, an indication of 1100 is added to the value of y for each pulse position after the position of least significance. The addition of 1100 to any positive number between 1 and 9 causes a carry to be produced

by the adder 324. These positive numbers are shown in the chart shown in FIGURE 12. For example, the addition of 1100 to an indication of 0100 representing $+1$ causes a carry indication to be obtained.

Since the addition disclosed in the previous paragraph occurs in the pulse positions holding the value of y after the first information position for y , a positive number indicative of y represents a value of "10" or more. As has been disclosed, the maximum value of Δy increments for an integrator can never be greater than -7 . The addition of -7 to a positive value exceeding 10 still produces a positive number. Under such circumstances, the production of a carry indication indicates that the value of y is still positive.

As will be seen, the addition of 1100 representing negative Δy increments to indications of 0011 representing a "0" value of y produces a resultant indication of 1111 in a particular pulse position but no carry. If a carry is obtained from the addition of y and Δy in a previous pulse position, this indication of "1" in the least significant position when added to the indication of "1111" causes a carry to be obtained in the particular pulse position. Because of this carry from a previous pulse position, a carry indication can be provided in the position of highest significance as to a positive value of y even though a value of y less than "10" is added to negative Δy increments.

When the value of y undergoing computation is less than "10," a carry is obtained in the pulse position of least significance for positive values of y greater in absolute magnitude than the negative value of the Δy increments. For example, a carry indication is produced when an indication of 1000 representing a value of y equal to $+5$ is added to an indication of 1001 representing a value of the Δy increments equal to -4 . But a carry indication is not obtained for an addition of 1000 representing a value of y equal to $+5$ and an indication of 0111 representing a value of the Δy increments equal to -6 . As disclosed in the previous paragraph, a carry from the pulse position of least significance causes a carry to be obtained for the pulse position of highest significance even though the value of y in the pulse position of highest significance is represented by an indication of 0011 equal to 0.

In the previous four paragraphs, various possibilities have been discussed to show that a carry is produced when a positive value of y for an integrator is added to a negative value of Δy having a magnitude less than the value of y . Similarly, no carry is produced when the absolute value of Δy for the integrator is greater than the positive value of y . In this way, a signal passes through the gate circuit 450 only when the new value of y is negative.

The gate circuit 452 passes a signal to indicate a negative value of y for an integrator when the value of y undergoing computation is negative, the cumulative value of the Δy increments is positive and there is no carry from a previous pulse position. For positive Δy increments, an indication of 0011 is added to the value of y for the pulse positions after the position of least significance. For additions of 0011 to any negative number between "1" and "9," no carry is obtained. This may be seen by the arithmetical combination of 0011 with any of the negative numbers shown in the chart in FIGURE 12.

In case the negative value of y undergoing computation is less than 10, the addition of this number to a positive number having a greater magnitude and representing the Δy increments produces no carry. For example, if a value of 0110 representing a value of Δy equal to $+3$ is added to any of the indications in FIGURE 12 representing negative values of y equal to 4, 5, 6, or 7, no carry is obtained. In this way, no carry can be transferred from one position to a position of increased significance to cause an output carry to be obtained at the position of increased significance. Because of this, a signal passes through the gate circuit 452 even for negative values of y

less than 10, provided that the cumulative value of the Δy increments has a positive polarity and an absolute magnitude less than the value of y . This signal passes through the multivibrators 276 and 244 and the "or" network 245 for recordation by the coil 36 as a positive indication in the channel 16.

The operation of the gate circuits 450, 452 and 454 can be given by the following logical equation:

$$Y_{sn} = P_{48}(B_2'B_7C_1' + B_2B_7'C_1' + B_2B_7C_1)$$

In the above equation,

Y_{sn} = a pulse of relatively high voltage recorded by the coil 36 in the channel 16 at pulse position 48 for an integrator to indicate that the value of y for the integrator is negative; and

B_2 , B_7 and C_1 have previously been defined.

The gate circuits 460, 462 and 464 pass signals to indicate positive values of y . Because of its connections to the multivibrators 280, 293 and 404, the gate circuit 462 passes signals when the values of y and the Δy increments are both positive and there is no carry. As previously disclosed, a positive value of the cumulative $y\Delta x$ increments is represented by an indication of 0011. When this indication is added to any positive value of y between 0 and 9, no carry is obtained.

The signals passing through the gate circuit 462 are introduced through the "or" network 466 to the grid of the right tube in the multivibrator 276. This signal causes the right tube in the multivibrator 276 to become cut off and a relatively high voltage to be produced on the tube plate. The high voltage on the plate of the right tube in the multivibrator 276 is introduced to the grid of the right tube in the multivibrator 244 to cut off the tube. The resultant low voltage on the plate of the left tube in the multivibrator 244 causes a pulse of relatively low voltage to be recorded by the coil 36 in the channel 16 as an indication that the value of y for the particular integrator is positive.

The gate circuit 460 passes a signal when the value of y for an integrator is negative, the cumulative value of the Δy increments for the integrator is positive and a carry occurs. Since the cumulative value of the Δy increments for the integrator is positive, an indication of 0011 is added to the value of y . As has previously been disclosed, the value of y is negative when no carry is obtained by the addition of a negative value of y and a positive value of the Δy increments. Inversely, the value of y becomes positive when a carry is obtained.

The new value of y is also positive when a positive value of y is added to a negative value of the cumulative $y\Delta x$ increments and a carry is obtained. The new value of y is positive for a positive carry since the value of y is negative when no carry occurs. Upon the occurrence of a positive value of y under such a set of conditions, a signal passes through the gate circuit 462 and the "or" network 466 to the grid of the right tube in the multivibrator 276.

This signal causes a pulse of relatively low voltage to be recorded by the coil 36 in the channel 16.

The operation of the gate circuits 460, 462 and 464 can be given by the following logical equation:

$$Y_{sn}' = P_{48}(B_2B_7'C_1 + B_2'B_7C_1' + B_2'B_7C_1)$$

In the above equation,

Y_{sn}' = a pulse of relatively low voltage recorded by the coil 36 in the channel 16 at pulse position 48 for an integrator to indicate that the value of y for the integrator is positive; and

B_2 , B_7 and C_1 have previously been defined.

The system disclosed above has several important advantages. Since the values of y and the cumulative value of $y\Delta x$ for each integrator are recorded in decimal form, these values can be easily determined for each integrator. Furthermore, the recordation of y and $y\Delta x$ for each integrator in the channels 14, 16, 18 and 20 on a decimal

basis causes the capacity of the analyzer to be increased with no material increase in the time required for the analyzer to solve a mathematical problem.

In co-pending application Serial No. 324,726, filed December 8, 1953, now Patent No. 2,923,470 by Robert E. Beck et al., a system is disclosed for determining the initial value of y for different integrators. This system requires that certain values be varied by the arithmetical combination of incremental values. Furthermore, in co-pending application Serial No. 390,506, filed November 6, 1953, by Glenn E. Hagen et al., a system is disclosed for providing a correction to the value of y for each integrator over the range of each Δx increment. This correction is produced by obtaining a particular function of the cumulative $y\Delta x$ increments during the time that a Δx increment is being produced.

It should be appreciated that the particular systems disclosed in the two co-pending applications mentioned in the previous paragraph can be also included in the system disclosed and claimed in this application. Instead of recording the value of y for each integrator in alternate pulse positions in the channels 14, 16, 18 and 20, the value of y can be recorded in every 4th position in the channels. Similarly, the value of $y\Delta x$, the initial value of y and the correction in the value of y can be recorded in every 4th position on a recurring basis. These values can be presented on a sequential basis to the adders 324 in a manner similar to that in which the values of y and $y\Delta x$ are alternately presented as disclosed above. In such a system, the advantages of parallel decimal operation would be even greater than in the simplified analyzer disclosed above.

It should be further appreciated that a system of parallel decimal operation similar to that disclosed above can be included in other digital differential analyzers than that disclosed in co-pending application Serial No. 217,478. For example, the system disclosed above can be easily adapted for use with the digital differential analyzer disclosed in co-pending application Serial No. 263,152, filed December 26, 1951, now Patent No. 2,850,232, by Glenn E. Hagen et al.

Although this invention has been disclosed and illustrated with reference to particular applications, the principles involved are susceptible of numerous other applications which will be apparent to persons skilled in the art. The invention is, therefore, to be limited only as indicated by the scope of the appended claims.

What is claimed is:

1. A differential analyzer for manipulating digital signals representing quantities of mathematical functions, comprising:

a signal register means including at least four channels, each for registering sequences of binary bits; means for providing said sequences of binary bits in integrator storage sections whereby said signal register includes a plurality of integrator storage sections; selective means for simultaneously providing binary signals from each of said channels representing first alternate binary bits from said channels, said simultaneous binary signals representing a decimal digit of a dependent quantity of a mathematical function from an integrator storage section; process means for processing said signals representative of a dependent quantity, connected to receive signals representative of variations in a dependent quantity for altering said signals representative of a dependent quantity in accordance with said signals representative of variations in a dependent quantity; means for recording signals from said altering means back in said signal register means as said first alternate bits in each of said channels; transfer means connected to receive said signals representative of a dependent quantity and signals representing variations in an independent quantity of a mathematical function, for forming product signals representative of the product of the values rep-

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resented by the received signals upon each occurrence of said signals representing a variation in an independent quantity while signals representative of an independent quantity are in process; and means for accumulating said product signals representing binary-coded decimal digits as second alternate bits in each of said channels.

2. Apparatus according to claim 1 wherein said accumulating means comprises means for providing signals representing second alternate bits from each of said channels; means for adding said signals representing second alternate bits to said product signals to form accumulated signals; and means for recording said accumulated signals as said second alternate bits in said register means.

3. Apparatus according to claim 1 further including means for sensing the accumulation of a predetermined value of said product signals to provide an overflow signal from an integrator storage section; and means for applying said overflow signals within said analyzer as representative of variations in a dependent quantity and variations in an independent quantity.

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