B 1870/B 1860 CENTRAL SYSTEMS

TECHNICAL MANUAL VOLUME 1:

OPERATION and MAINTENANCE

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LIST OF EFFECTIVE PAGES

Page	Issue	Page	Issue
Title	Original	1-53 thru 1-61	Original
ii thru iii	Original	1-62	Blank
iv	Blank	1-63 thru 1-65	Original
v thru xii	Original	1-66	Blank
1-1 thru 1-5	Original	1-67 thru 1-86	Original
1-6	Blank	2-1 thru 2-7	Original
1-7	Original	2-8	Blank
1-8	Blank	3-1 thru 3-18	Original
1-9 thru 1-51	Original	4-1 thru 4-24	Original
1-52	Blank	5-1 thru 5-26	Original

TABLE OF CONTENTS

TABLE OF CONTENTS (Cont)

TABLE OF CONTENTS (Cont)

TABLE OF CONTENTS (Cont)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Cont)

LIST OF ILLUSTRATIONS (Cont)

LIST OF TABLES

LIST OF TABLES (Cont)

SECTION 1
FUNCTION AND OPERATION

INTRODUCTION

The Function and Operation Section provides a basic description of the B 1870/B 1860 Central System and its operation. Included are separate discussions of M-Processor-3, Cache Memory, S-Memory Base-3, I/O Base-3, Port Interchange-3 and the power supply and distribution system. Also provided is a basic description of the manner in which the system is programmed, including the microinstruction set and the implementation of higher level programming languages.

System General Description

The B 1870/B 1860 series consists of a microprogrammed processor with a local high-speed micro memory (Cache), a dynamic main memory (S-Memory), and a low-speed I/O subsystem. With the exception of a few circuits which contain discrete (transistor) elements, the entire system circuitry is composed of CTL (complementary transistor micro logic) and TTL (transistor-transistor logic) integrated circuit elements. A typical B 1870/B 1860 system is shown in figure 1-1.

Significant changes from previous practice include the following:

a. Use of a hardware-managed Cache memory for local (in-processor) storage of microinstructions.

b. Incorporation of a 3-phase micro execution structure in which the functions of fetching, decoding, and executing microinstructions are performed separately (and concurrently).

c. Incorporation of stored logic in the form of preprogrammed read-only memories.

d. The use of a nano register to store control signals for the processor execute structure.

e. Incorporation of 4K storage elements in S-memory, allowing the maximum permissible storage to be contained on one memory base.

f. Increased usage of error-detection techniques in data storage and manipulation, and the addition of an error-correction capability to S-memory.

g. Physical and electrical partitioning of the internal circuits along common boundaries, enhancing system maintainability.

h. Memory Base compatibility with the B 1720 series system. This means that the processors of both systems may be used interchangeably with the Memory Base Unit-3.

A block diagram of the B 1870/B 1860 system is shown in figure 1-2.

Features and Capabilities

Features and options of the B 1870/B 1860 system include the following:

a. A variable micrologic design, which allows the processing environment to be optimized (by way of software) for a variety of programming languages.

b. A hardware-managed Cache memory for in-processor storage of microinstructions. The management scheme employed in the use of Cache ensures that the need for accessing main memory to fetch micros is minimized.

c. A modular, integrated-circuit main (S) memory which utilizes error detection and correction techniques. The S-memory is expandable in 64 KB increments from 64KB to 512KB, and is bit-addressable.

d. An optional port interchange which may be employed to allow independent S-memory access by devices other than the processor (such as a multiline control).

e. An independent, expandable I/O subsystem which employs fully buffered control logic. Peripheral devices available for use in the B 1870/B 1860 I/O subsystem include the following types:

1. 96-column punched card equipment.
2. 80-column punched card equipment.
3. Line printers.
4. Disk cartridge memory.
5. Disk pack memory.
6. Head-per-track disk memory (B 1870 only).
7. Magnetic tape equipment.
8. Reader/sorter equipment.
9. Data communications equipment.

Microprogramming

The B 1870/B 1860 Central System performs operations by executing a set of low-level microinstructions which are fetched and executed from the main memory of the system. There are 38 microinstructions for performing the various necessary machine functions. The micros are decoded within the processor, and the outputs thereby produced activate the appropriate registers, pseudo registers, logic and arithmetic sections for performing a specific activity.

Micro programming has several definite advantages. One advantage which is most obvious is ease in modification of machine operations. That is, an operation can be changed through software rather than requiring a modification of the logic. Another obvious advantage is that microprogramming allows the manner in which the hardware is exercised to be "tailored" to the requirements of a particular programming language such as COBOL, FORTRAN, etc.

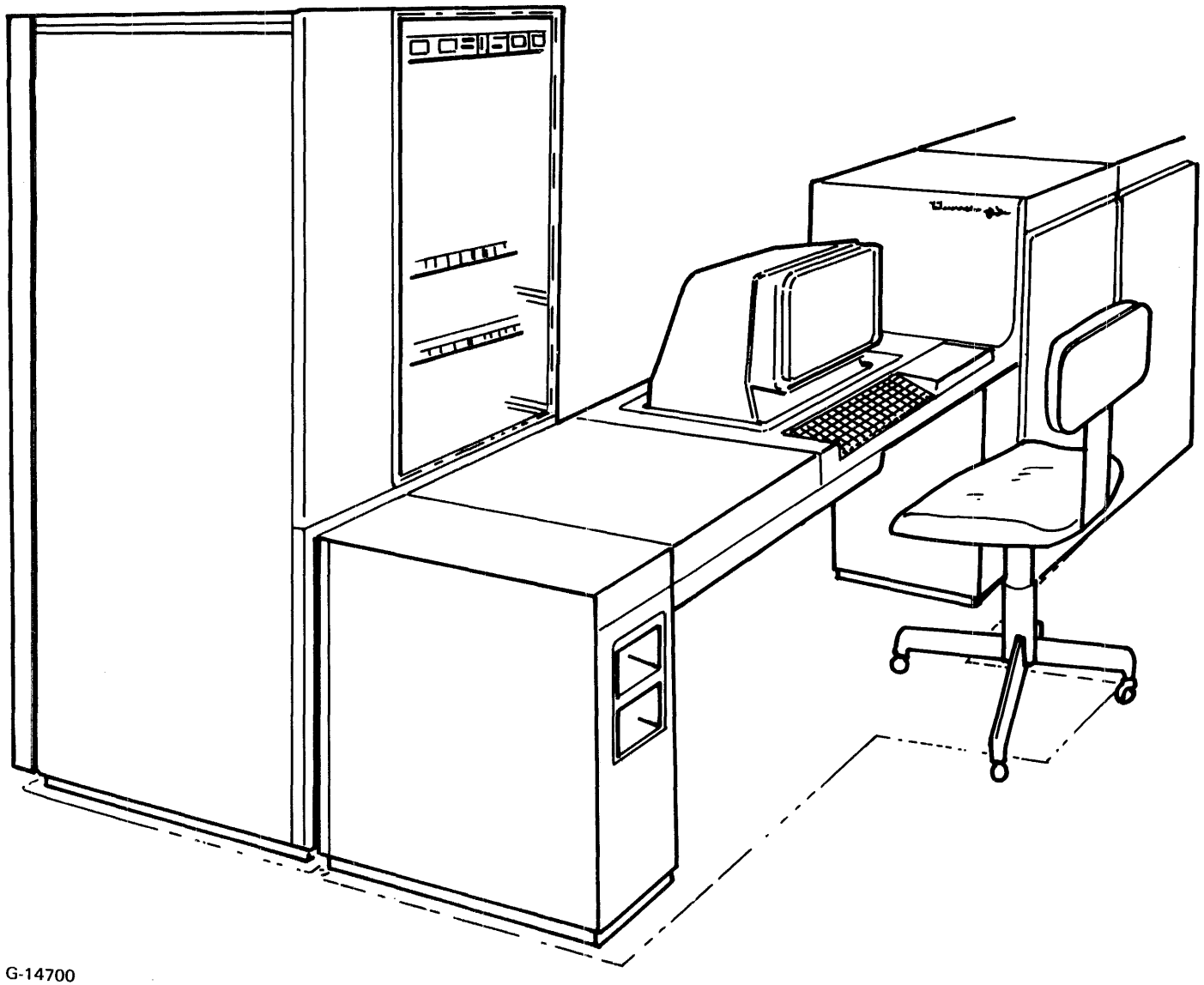

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Figure 1-1. B 1870/B 1860 Central System

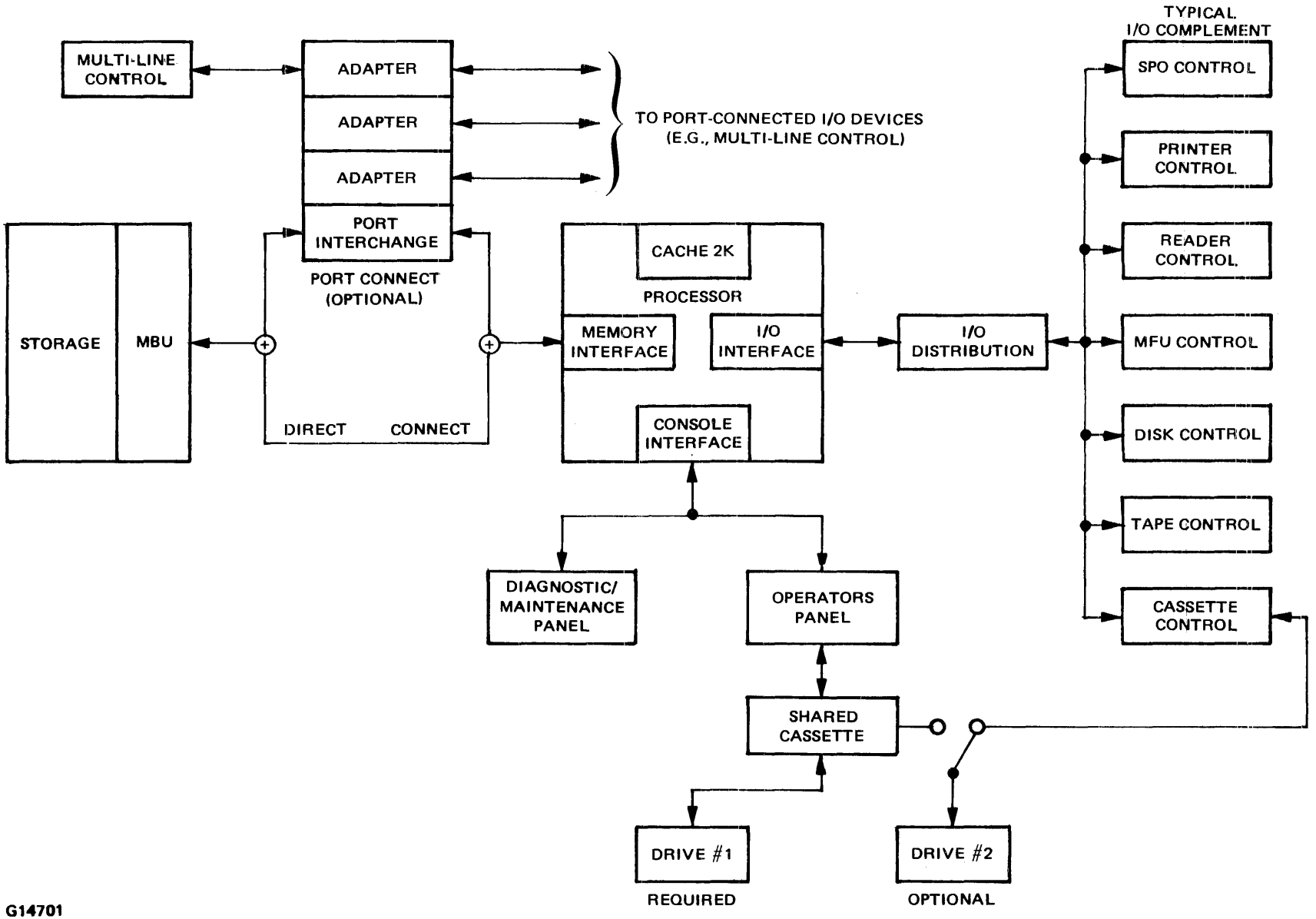

Figure 1-2. B 1860 Series Central System Block Diagram

Program Products

Program products available for use with the B 1870/B 1860 Central Systems include the following:

a. A Master Control Program (MCP) which provides management of the system's resources.

b. A variety of program products, including compilers for COBOL, FORTRAN, RPG, BASIC, SDL, MIL, NDL, and UPL.

c. Special emulator and translator programs which allow direct execution or machine translation of programs written in code for certain other systems.

In addition to having a structure which is adaptable to the execution of a variety of computer languages, the B 1870/B 1860 systems have the following capabilities:

a. Multiprogramming under MCP control.

b. Virtual memory.

c. Bit-addressability for storage purposes, allowing code compaction of variable-length operands.

Physical Configuration

The B 1870/B 1860 Central System is contained within a single-bay cabinet measuring 28" (71 cm) wide, 72" (183 cm) high, and 35" (89 cm) deep. An additional bay can be added (expansion cabinet). Figures 1-1 and 1-3 show 1-bay cabinets.

The B 1870/B 1860 Central System cabinet is equipped with a control panel (equivalent to the similar panel on B 1700 series systems) which is reserved for diagnostic and maintenance purposes. This panel, recessed behind a smoke-tinted plastic cover, is not intended to be used during normal system operation. Operational control is provided by a separate operator's control panel, which is part of the sit-down console table.

All essential elements of the central system are contained within the main cabinet, including the processor, S-memory, the I/O base and I/O controls, the port interchange (if used), AC power distribution facilities, DC power supplies and ventilation equipment. For ease of access to the interior, the side and rear cabinet panels are removable. Internally, the central system cabinet consists of a 19" (48 cm) RETMA rack mounting fixture. All internal circuit elements, except the console controls and the AC distribution assembly are located within the rack, which forms a vertical air column for cooling purposes. Logic circuitry is constructed on pluggable 11-3/4" x 14-1/4" (30 x 36 cm) circuit cards. Connections between the cards are made by point-to-point wrapped wires on the backplane and by multipair flat cables on the frontplane. DC power is distributed to the circuits by a network of bus bars.

M-PROCESSOR-3

The M-processor-3 consists of 13 logic cards plus a clock card and an I/O distribution card. Also considered part of the processor are the console controls (both operator's controls and diagnostic/maintenance controls) and the cassette tape reader. The processor contains the necessary circuitry to perform the arithmetic, logical and data movement/storage functions required of a central processing unit, plus the means to interface with its I/O subsystem, the port interchange, and the memory.

Functional Layout

To carry out its designed function, the processor consists of a number of distinct sections:

a. Working Registers: For storage of operands, addresses, literals and control signals having significance to the operations being performed.

b. 24-Bit arithmetic/logic unit (ALU): For performing arithmetic, logical, and data repositioning functions on selected fields of data. The ALU is that part of the system where actual "data processing" occurs. The ALU is also referred to as the 24-Bit function/rotator.

c. A, M and A-stack registers: For controlling the source of microinstructions, and providing a pathway to the decoding and execution logic.

d. Cache Memory: For local in-processor storage of microinstructions, providing a rapid access location for the program material in current use.

e. S-Memory Interface: For providing communication with the central system main storage unit.

f. I/O Interface: For providing communication with the system peripheral devices.

The above-listed operational sections are related to each other as illustrated in figure 1-4. Not shown as an operational section is the microinstruction decoding and execution control logic. However, the control elements, of equal importance with the functional logic sections, are discussed in the following subsections.

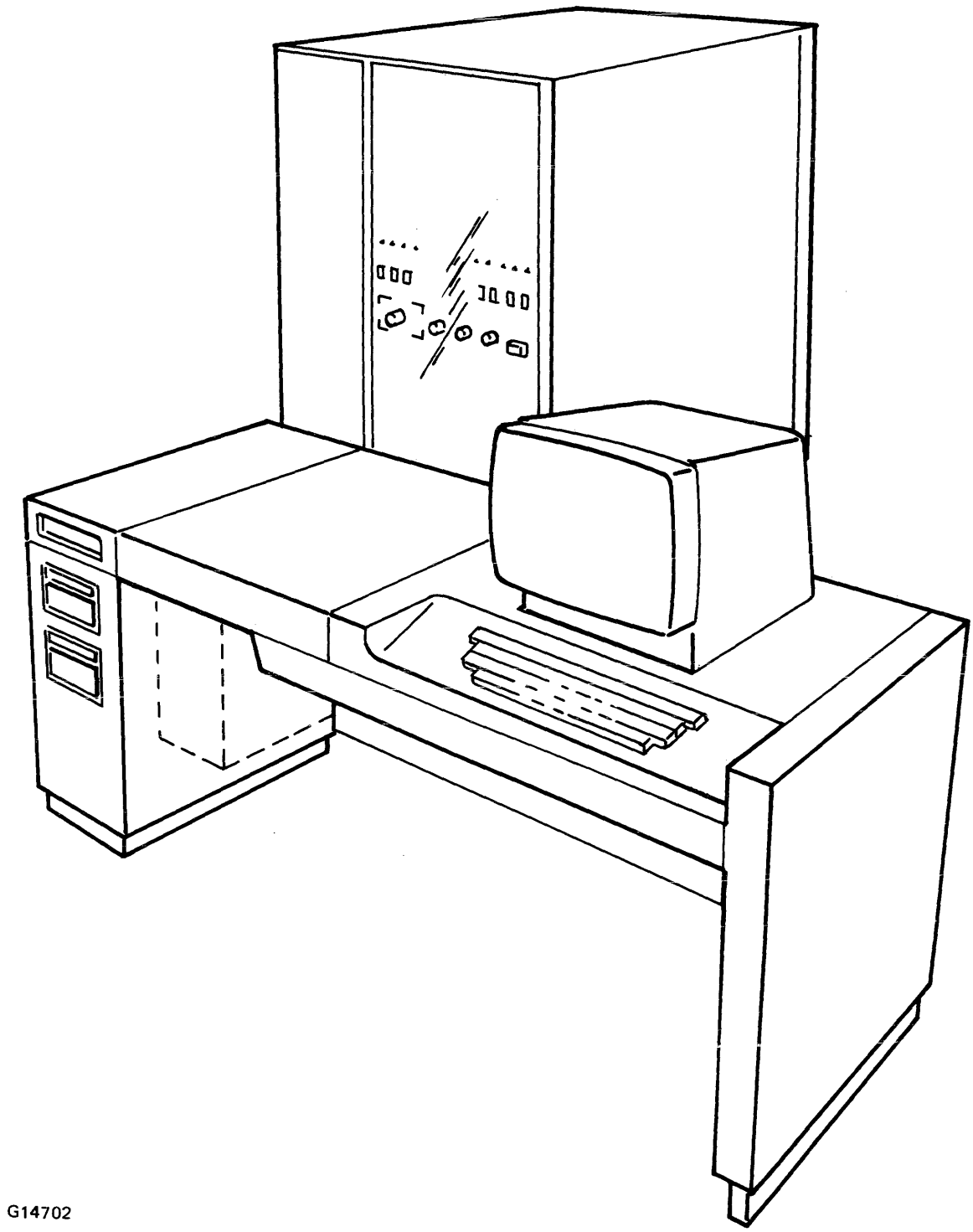

Figure 1-3. B 1870/B 1860 Physical Configuration

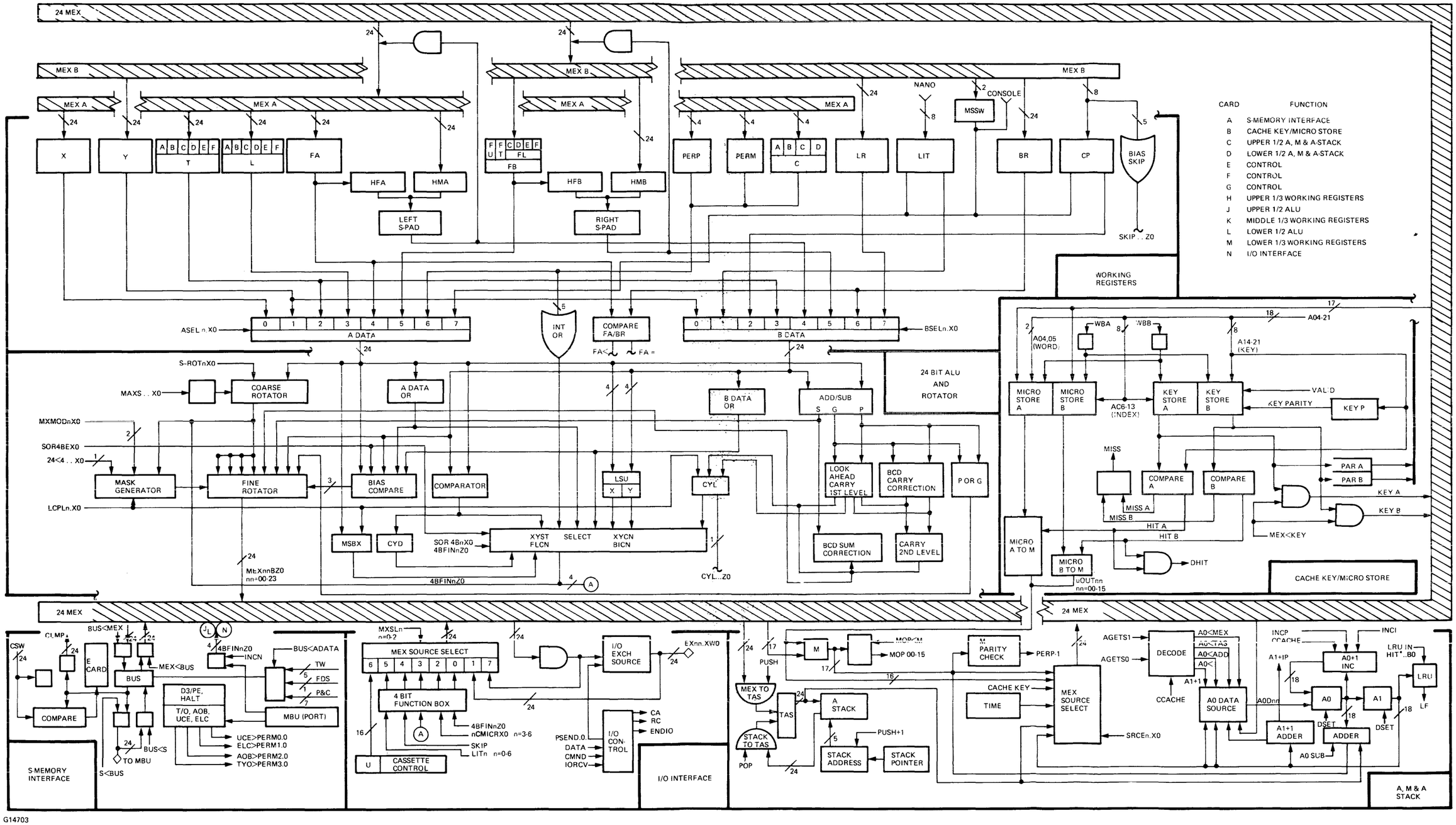

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Figure 1-4. M-Processor-3 Functional Layout

Data Paths

Data movement within the M-processor-3 is handled primarily by the 24-bit main exchange, and by its subdivisions MEXA and MEXB. These data paths are described separately.

24-Bit Main Exchange

The 24-bit main exchange (MEX) is in actuality simply the common input and output connections of a number of logic elements. In general the MEX receives the output of the 24-bit function/rotator, and feeds the working register inputs by way of MEXA and MEXB. The outputs of the working registers in turn feed the function/rotator inputs, through which their contents must pass to reach the exchange. Additional inputs and outputs to/from the exchange are the memory interface, the I/O interface, the A and M registers and A-stack, and Cache memory. All of the above are bidirectional, although the dedicated function of the A register is to address Cache, that of Cache is to feed the M register, and that of M is to feed the microinstruction decoding logic.

MEXA and MEXB

Because certain microinstructions involve the simultaneous movement of data to/from two of the working registers (FA and FB), the working register inputs are divided into two sections which are electrically isolated from one another. MEXA feeds X, T, L, FA, HMA, PERP, PERM, and C and MEXB feeds Y, FB, HMB, LR, BR, MSSW, and CP. The isolation is significant only to the simultaneous move operation; both sections receive the contents of the MEX without enabling signals.

Working Registers

The storage elements provided to contain data significant to current processor operations (other than micro addresses or microinstructions themselves) are termed working registers. The working registers are divided into two groups corresponding to the division of inputs between MEXA and MEXB. The register outputs are similarly divided into two groups feeding the A-data and B-data inputs to the 24-bit function/rotator, but the groupings do not necessarily follow the pattern of the inputs (see figure 1-4). In fact, several registers have both A-data and B-data outputs. The A and B data designations have significance only to ALU operations. The working registers are discussed individually in the following subsections.

X Register

The X register is a 24-bit general purpose register which can serve as either a source or a destination. X is used primarily to store one of the operands for the 24-bit ALU operations. X may be addressed only in its entirety. Other functions of X are as follows:

a. X is one of four registers (X, Y, T, and L) which may serve as a source or destination for data on S-memory Read/Write operations.

b. X may also be used as a source or destination for data on Cache Diagnostic Read/Write operations.

c. X may be shifted or rotated, and also may be normalized (shifted left in 1-bit increments until the most-significant bit referenced by the CPL register contents equals 1 or until the FL register equals 0).

d. X may be concatenated with the Y register to effectively form a 48-bit register. When this is done, X occupies the 24 most-significant bit positions.

Y Register

The Y register is a 24-bit general-purpose register which can serve as either a source or a destination. Y is used primarily to store the second of two operands for the 24-bit ALU (X stores the other). Like X, Y may be addressed in its entirety only. Other functions of Y are as follows:

a. Y is one of four registers (X, Y, T, and L) which may serve as a source or destination for data on S-memory Read/Write operations.

b. Y may be used as a source for data on Cache Diagnostic Write operations.

c. Y is the destination for data on the Diagnostic Read/Write Memory operation. The data received may be the write data, the address, or the contents of the Error Log register.

d. Y may be concatenated with X to form a 48-bit register. When this is done, Y occupies the 24 least-significant bit positions.

T Register

The T register is a 24-bit general purpose register which is addressable as a whole and in 4-bit subgroups designated TA, TB, TC, TD, TE, and TF (see figure 1-5). T (and its subregisters) may be used as either sources or destinations. The input of T is from MEXA, and it is one of two registers (Y is the other) which has outputs to both the A Data and B Data gates. T is one of four registers (X, Y, T, and L) which may be used as a source or destination for S-memory Read/Write operations.

TA	TB	TC	TD	TE	TF	
23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0	BIT

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Figure 1-5. T Register

EXAMPLE 1 – ROTATE LEFT BY 5 BITS

T-REGISTER CONTENTS

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	BIT
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	CONTENTS

OUTPUT TO MEX

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	BIT
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	CONTENTS

EXAMPLE 2 – ROTATE RIGHT BY 11 BITS

T-REGISTER CONTENTS

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	BIT
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	CONTENTS

OUTPUT TO MEX

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	BIT
0	0	0	1	0	0	1	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	CONTENTS

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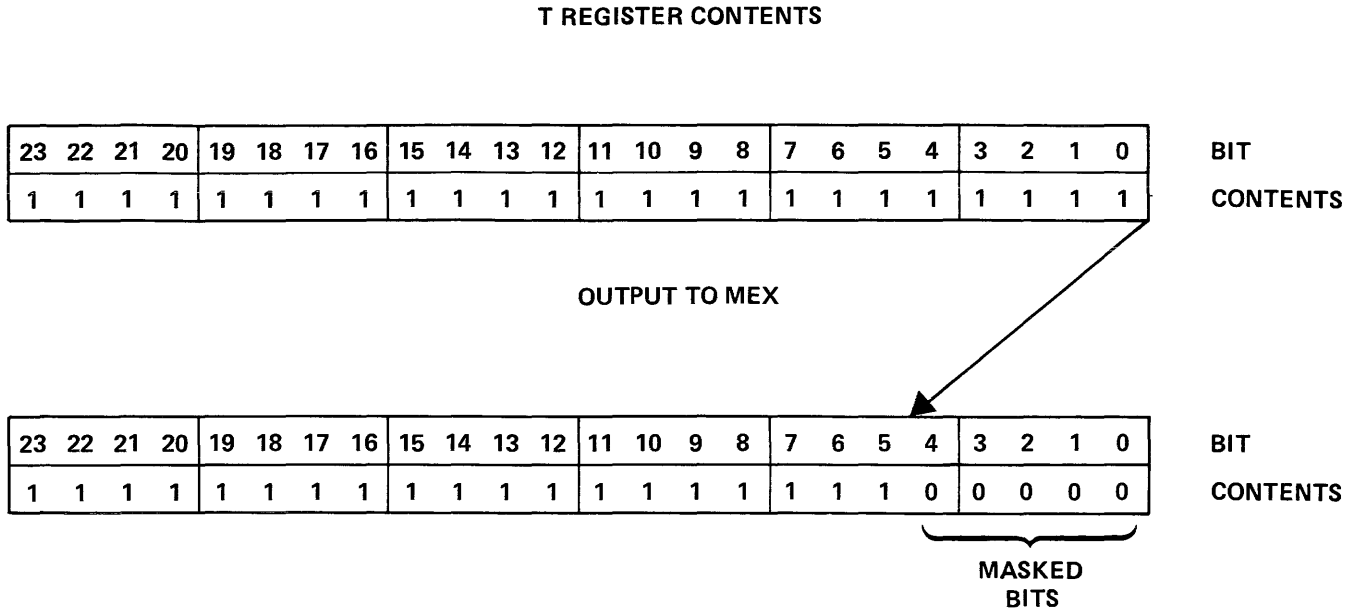
Figure 1-6. Rotation Function of T Register

In addition to its normal storage functions, the contents of T may be rotated, shifted or extracted. These functions, performed during execution of the 10C and 11C micros, are defined as follows.

Rotation is the simultaneous lateral movement of all data contained within a specified field, with wrap-around provided (data departs the field at one end and simultaneously reappears at the opposite end). Rotation is illustrated in figure 1-6.

Shifting is the simultaneous lateral movement of all data contained within a specified field, without wrap around (data departing the field is lost; zero fill occurs at the opposite end). Shifting is illustrated in figure 1-7.

EXAMPLE 1 – SHIFT LEFT BY 5 BITS



EXAMPLE 2 – SHIFT RIGHT BY 7 BITS

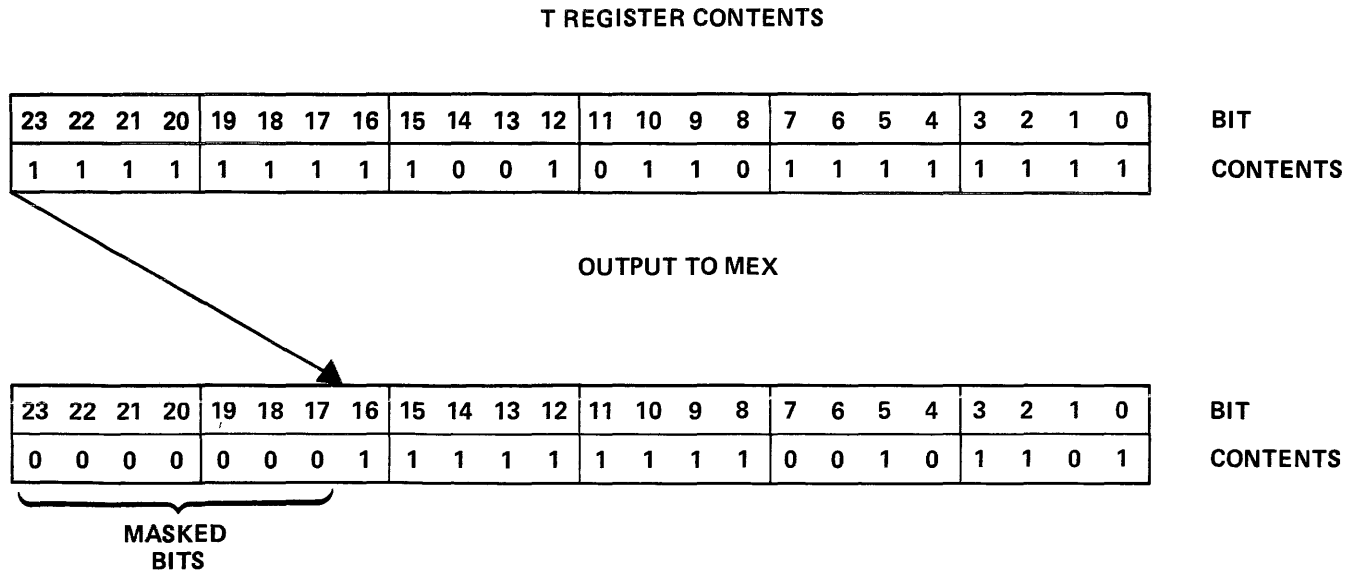


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Figure 1-7. Shift Function of T Register

EXAMPLE: EXTRACT FROM T THE DATA FIELD CONSISTING OF BITS 8 – 12.
THIS INVOLVES RIGHT ROTATION BY 8 BITS, AND MASKING OF THE 19 MOST SIGNIFICANT ROTATOR OUTPUT BITS.

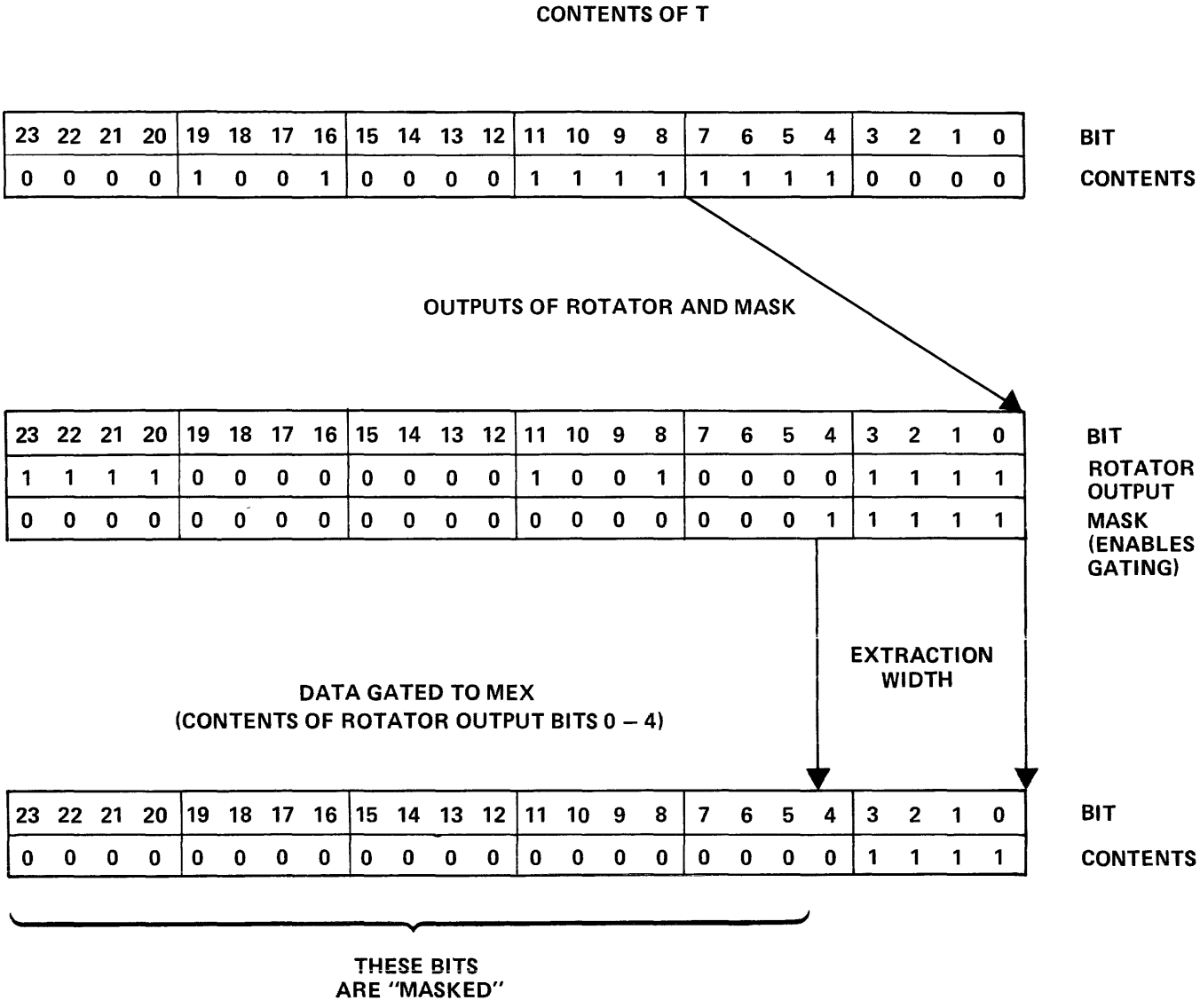

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Figure 1-8. Extract from T Function

Extraction is the separation of a defined subfield from a larger field. In the context of the T register, this means rotation to right-justify the desired subfield with respect to the output lines, then application of a mask to limit the output to the specified number of bit positions. Extraction is illustrated in figure 1-8.

Unlike the earlier B 1700 processors, M-Processor-3 does not have a separate rotator and mask logic associated with the T register. The shift/rotate and extract functions are now assumed by the main rotator and mask, which are parts of the 24-bit ALU.

L Register

The L register is a 24-bit general-purpose register which like the T register, is addressable as a whole or in 4-bit groups designated LA, LB, LC, LD, LE, and LF. L and its subregisters may be used as either sources or destinations. Input to L is from MEXA, and its output goes to the A Data gates. L is one of four registers (X, Y, T, and L) which can be used as a source or destination for S-memory Read/Write operations and Cache Diagnostic Write operations. Additional functions utilizing L are the Dispatch operation, which uses L as the source or destination for a 24-bit message, and the Bind operation, which uses L as the source of a 24-bit value to be added to the contents of T.

Base and Limit Registers

The Base (BR) and Limit (LR) registers are both 24-bit registers which can be addressed as either a source or destination. These registers are used programmatically for storage of memory addresses. The addresses contained therein are customarily used for protection of memory (against overlaying) and for base-relative addressing. For a given program, writing in memory is generally allowed within the bounds specified by the contents of BR and LR. If the address does not fall within the Base and Limit, a software function determines if the cycle is to be allowed.

FA Register

The FA (Field Address) register is a 24-bit register which is used primarily to hold the address currently being accessed in S-memory (for data access only and not for fetching microinstructions). The address contained in FA is an absolute bit address; the significance of the various bit positions are as illustrated in figure 1-9. FA may be used as either a source or destination, and in addition may be incremented or decremented by the literal value contained in a 7C Read/Write Memory micro or by the value in CPL if the literal is equal to 0. Neither overflow nor underflow of FA is detected; therefore the count may wrap around in either direction.

Additional micro functions involving the FA register are as follows:

a. The Scratchpad Relate FA micro (8D) provides increments/decrements of FA by the value contained in a selected word of left scratchpad.

b. The Exchange Doublepad Word micro (7D) provides swapping the contents of both FA and FB with the contents of a double (left and right) scratchpad word.

c. The load F From Doublepad Word micro (5E) provides loading both FA and FB with the contents of a double scratchpad word.

d. The Store F Into Doublepad Word micro (4E) provides storing the contents of both FA and FB into a double scratchpad word.

e. The Count FA/FL micro (6D) provides incrementing or decrementing of FA by the literal value contained in the microinstruction.

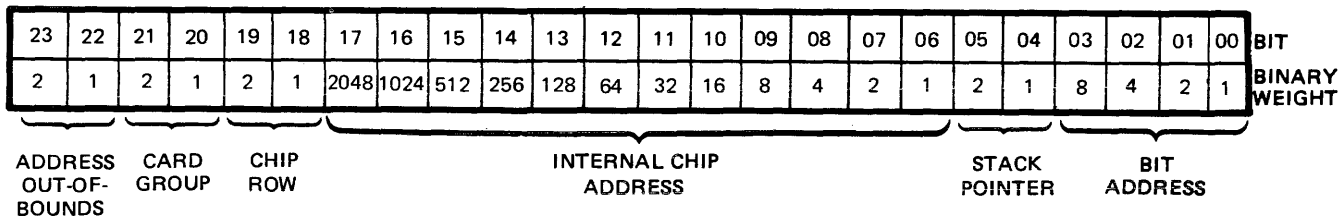


Figure 1-9. FA Register Showing Memory Addressing Significance

FB Register

The FB register is a 24-bit special purpose register which is used to hold information pertaining to current S-memory accesses. FB is functionally divided into the 4-bit FU and FT portions, plus the 16-bit FL portion. (See figure 1-10.) The FL portion is further subdivided into the 4-bit FLC, FLD, FLE, and FLF registers. The entire FB register is addressable as a whole, as is the 16-bit FL portion. In addition, all 4-bit portions are addressable separately as either sources or destinations.

The contents of FB have significance with respect to the subregister portions rather than for FB as a whole. The subregister portions are described in the following subsections.

FU

The FU (field unit) register is used to hold the length of the unit which makes up a field of data in S-memory. The FU register can describe fields up to 15 bits in length. FU is used primarily as a bias source for the CP register. Refer to the Bias (3E) micro description for more information.

FT

The FT (field type) register holds a field type designator which has specific meaning only to software, and can therefore vary depending on the program in use. The FT register is not used by the hardware unless specifically accessed on command of the executing micro.

FL

The FL (field length) register holds a value which describes the total length of a field of S-memory data. The value in FL is binarily weighted, and can describe fields up to 65,536 bits in length. FL may be incremented or decremented by the literal value in a microinstruction or by the value in the CPL register. Overflow and underflow of FL can occur, but overflow is not detected and will cause the register to wrap around to 0. Underflow is detected and will not cause wraparound (a value of 0 is left in the register). FL is used as a bias source for the CP register and for a state compare with the first word of right scratchpad. The static compare results are available when the pseudo register FLCN (field length conditions) is sourced.

Special functions provided for FB are the means for being stored in, loaded from, or swapped (along with FA) with a specified word of scratchpad. These three functions are provided by the 4E, 5E, and 7D micros, respectively.

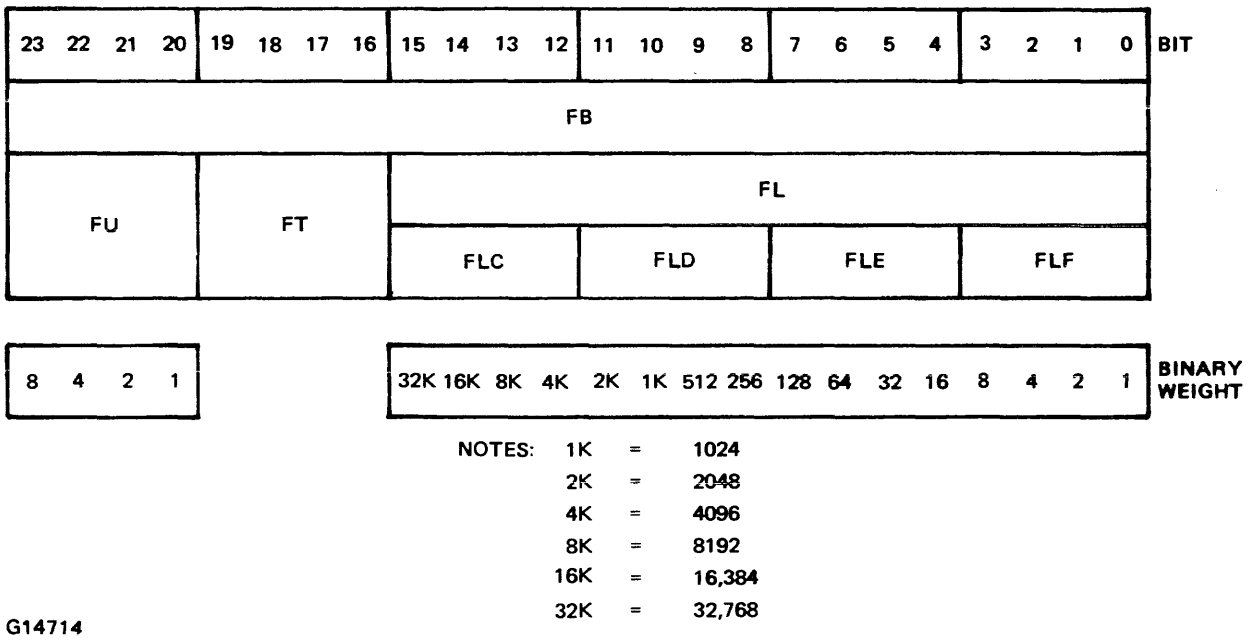


Figure 1-10. FB Register

Scratchpad Memory

Scratchpad memory is a 16x48 bit random-access memory provided for general purpose in-processor storage. Scratchpad is functionally divided into left and right halves consisting of the 24 most-significant and 24 least-significant bit positions of each of the sixteen 48-bit words. Refer to figure 1-11. Each 48-bit word is addressable as an entity or may be considered as two 24-bit words, each of which can be addressed. All storage locations within scratchpad may be addressed as sources or destinations. Unlike earlier systems, scratchpad is directly accessible from the console in the M-Processor-3 system. This means of access is provided at the Diagnostic/Maintenance console, and is incorporated into the console register selection switches.

Associated with scratchpad are four special latch registers which receive the inputs from the F register (FA and FB) and the MEX. These are identified as HFA (receives the contents of FA), HMA (receives the contents of MEXA), HFB (receives the contents of FB), and HMB (receives the contents of MEXB). The latches are shown in figure 1-4.

Word 0 of right scratchpad is reserved for storage of parameters known as SFU and SFL. These are binary values which correspond to the FU and FL portions of the FB register, and are used for reference purposes. Special monitoring logic (external to scratchpad) performs a constant comparison between SFL and FL, and sets certain bits in the FLCN pseudo register based on the results. SFU and SFL are not addressable separately, but may be accessed together by addressing word 0 of right scratchpad. Scratchpad may be accessed by way of the following micros:

Micro	Action
Scratchpad Move (2C)	May address any 24-bit word of left or right scratchpad as either source or destination.
Exchange Doublepad Word (8D)	May address any 48-bit word of scratchpad, exchanging the contents thereof with the contents of the FA and FB registers.
Scratchpad Relate FA (8D)	May address any 24-bit word of left scratchpad as a source
Store F in Doublepad Word (4E)	May address any 48-bit word of scratchpad as a destination for the contents of the FA and FB registers.
Load F from Doublepad Word (5E)	May address any 48-bit word of scratchpad as a source for the contents of the FA and FB registers.

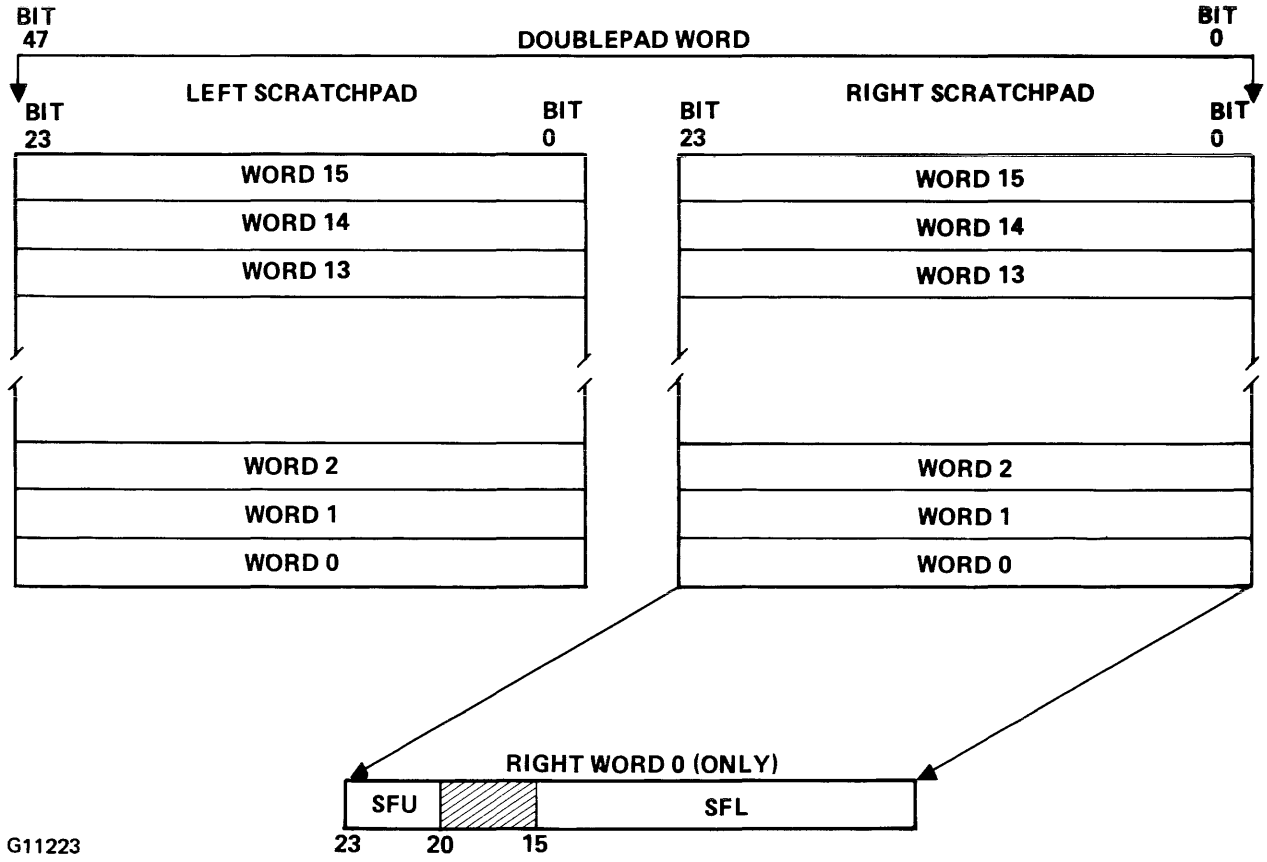


Figure 1-11. Scratchpad

PERP Register

The PERP (Parity Error-Processor) register is a 4-bit register which is used to store error conditions generated in the processor. The errors thus reported are the result of a Cache double bit, a Cache key parity error, an M-register parity error, or a Cassette Tape Read parity error. The format of PERP is illustrated in figure 1-12, and the specific meaning of the individual bit positions is explained in the following subsections.

PERP3 (CACHE DOUBLE HIT)

This bit is set whenever there is a hit from both blocks A and B of Cache. This event results in a double read, with both micros being ORed. When Cache is being used as a source of microinstructions, a double hit is interpreted as a hardware malfunction and will cause the processor to halt. When Cache is not being used as a source of micros (as when S-memory is selected on the MICRO SOURCE switch on the D/M panel), the double hit is ignored, but CD3 and PERP3 are set.

PERP2 (CACHE KEY PARITY ERROR)

PERP2 is set whenever there is a parity error on reading the key store. The error indicated may be detected on either key A or key B, since the two are read together. The parity check determines if there is an odd sum of the key (8 bits), the validity bit (1 bit) and the parity bit (1 bit). When a Cache key parity error occurs during a fetch the processor is halted and PERP2 is set. When Cache is disabled (MICRO SOURCE = S), a Cache key parity error causes CD3 and PERP2 to be set, but the processor does not halt.

PERP1 (M-REGISTER PARITY ERROR)

PERP1 is set whenever there is a data parity error on a microinstruction in the M-register. Such an error can occur on a micro fetch from Cache or directly from S-memory, and causes the processor to halt concurrent with setting PERP1. Parity error reporting on the M-register is disabled on non-fetch data moves to the M-register and when loading M from the cassette tape reader, since no parity generation is provided for these functions.

PERP0 (CASSETTE PARITY ERROR)

PERP0 is set whenever a non-recoverable cassette read error occurs. When such an error occurs in the TAPE mode the processor is halted.

The PERP register is reset to 0 whenever the processor is started (from the halt state) or, during the halt state, when the LOAD button (OP panel) is pressed with REGISTER SELECT (D/M panel) at MEMORY MODE.

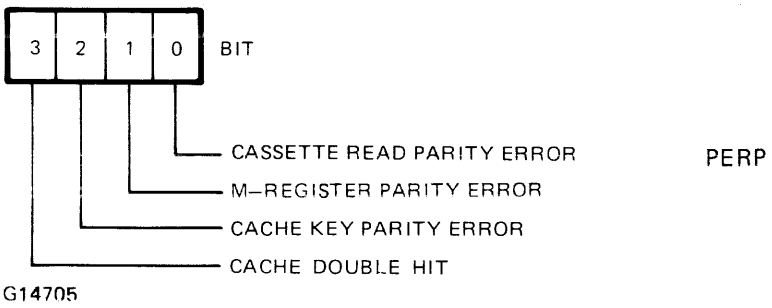


Figure 1-12. PERP Register

PERM Register

The PERM (Parity Error-Memory) register is a 4-bit register which is used to store error conditions occurring in connection with the processor's use of S-memory. The errors thus reported are the result of a memory access micro timeout, a memory access outside the administrative bounds of memory, a change in the S-memory Error Log register, or an uncorrectable S-memory error during a processor operation. The format of PERM is illustrated in figure 1-13. The specific meaning of the individual bit positions is explained below.

PERM3 (S-MEMORY MICRO TIMEOUT)

This bit is set whenever a predetermined time has elapsed during the execution of a memory access micro. The time check is made for all memory micros, including 7C, 2D, 11D, and 1E.

PERM2 (OUT-OF-BOUNDS MEMORY ACCESS)

This bit is set whenever the administrative bounds of memory are exceeded, as determined by either MAXS or the physical memory present. The executing micro may be either a read or write operation.

PERM1 (CHANGE IN ERROR LOG REGISTER)

This bit is set whenever there has been a change in the Error Log register. Such a change indicates either logging an initial error (since the Error Log was last cleared), or a higher priority error, information on which replaces the previous contents. Three possible levels of errors may be reported:

a. A single-bit error which was corrected (lowest priority).

b. An uncorrectable error from a non-processor memory access (middle priority).

c. An uncorrectable error from a processor memory access (highest priority).

Generally, the first error detected is logged. Then, if a higher priority error occurs, this information replaces the previous contents. The Error Log register is cleared when read by the processor.

PERM0 (UNCORRECTABLE ERROR ON PROCESSOR MEMORY ACCESS)

This bit is set whenever an uncorrectable error is detected during a processor memory read cycle.

Setting any bit of PERM causes the error flag bit CD3 to be set (assuming the processor is running). Processor actions thereafter are determined by software.

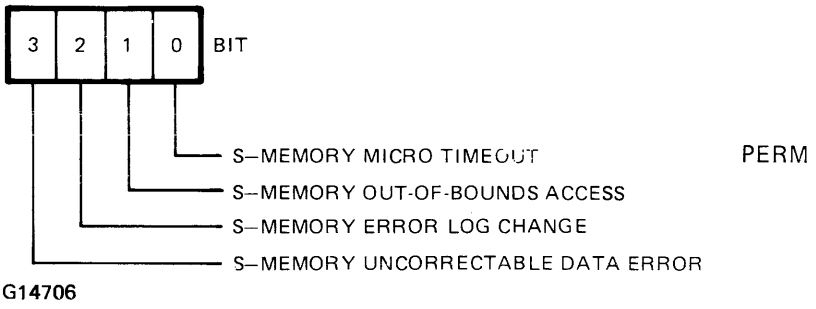


Figure 1-13. PERM Register

C Register

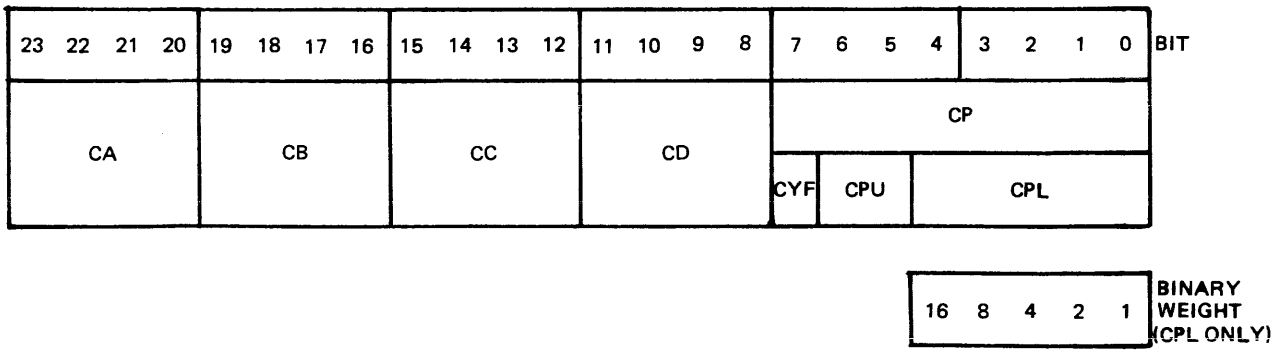
The C register is a 24-bit register not addressable as an entity but functionally divided into one 8-bit section and four 4-bit sections. These subdivisions of C are identified as CA, CB, CC, CD, and CP. Refer to figure 1-14. CP is further divided into the 5-bit CPL portion, the 2-bit CPU portion, and the 1-bit CYF. The functions of the various portions of C are explained in the following paragraphs.

CA AND CB REGISTERS

The 4-bit CA and CB registers have no special function, and are available for general-purpose storage.

CC AND CD REGISTERS

The 4-bit CC and CD registers are used for storage of various processor states and conditions. The various flag bits are set by the processor when the corresponding state or condition exists, this occurring regardless of what has been previously stored in the register. Refer to figure 1-15. CC and CD may also be addressed as normal storage registers.



NOTES:
1. CA,CB,CC,CD AND CP ARE ADDRESSABLE AS SOURCE OR SINK
2. CPU IS ALSO ADDRESSABLE AS SOURCE OR SINK. IT IS TREATED AS A 4-BIT REGISTER WITH THE LEFTMOST 2 BITS ALWAYS EQUAL TO ZERO

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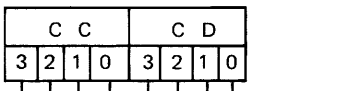
Figure 1-14. C Register



SIGNIFICANCE WHEN REGISTER BIT = 1

CD0 — WRITE/SWAP ADDRESS-OUT-OF-BOUNDS FLAG. FA <BR OR FA>. MEMORY WRITE/SWAP CYCLE OCCURS ONLY IF CD2 IS TRUE.

CD1 — READ ADDRESS-OUT-OF-BOUNDS FLAG. FA <BR OR FA>LR.MEMORY.

CD2 — WRITE/SWAP ADDRESS-OUT-OF-BOUND OVERRIDE FLAG. MEMORY WRITE/SWAP OCCURS REGARDLESS OF OUT-OF-BOUNDS CONDITION.

CD3 — MEMORY ERROR FLAG. ANY PERM OR PERP BIT IS SET.

CC0 — CONSOLE FLAG. THE INTERRUPT LIGHTS ON THE D/M AND OP PANELS ARE ON.

CC1 — I/O BUS FLAG. ONE OR MORE I/O CONTROL REQUIRES SERVICING.

CC2 — TIMER FLAG. SET EVERY 100 MILLISECONDS BY THE REAL TIME CLOCK.

CC3 — STATE. SET VIA SOFTWARE TO INDICATE VIA D/M PANEL STATE LAMP THAT THE SYSTEM IS IN THE CONTROL STATE (MCP IS IN CONTROL). WHEN THIS LAMP IS OFF, THE SYSTEM IS IN THE NORMAL STATE (USER'S PROGRAM IS EXECUTING).

NOTE: WITH THE EXCEPTION OF CD0, CD2, AND CD3, THE CC AND CD BIT STATES HAVE NO HARDWARE SIGNIFICANCE BUT ARE EXAMINED BY SOFTWARE AND USED ACCORDINGLY.

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Figure 1-15. CC and CD Registers

CP REGISTER

The 8-bit CP register consists of three subregisters (CYF, CPU, and CPL), each of which has its own special function. CP is addressable as either a source or destination, using the eight least-significant bits of the MEX. The subregister functions are as follows.

CYF

The Carry Flip-flop (CYF) consists of bit 7 only (most significant bit of CP). This flip-flop is used to store a carry level on add operations or a borrow level on subtract operations. CYF is not addressable separately, but may be set or reset as part of CP.

CPU

The Control Parallelism Unit (CPU) register consists of bits 5 and 6 of CP. CPU is used to designate the type of arithmetic operation the processor is to perform. If CPU=00 or 10, the operand data and result are handled as binary values. If CPU=01 or 11, 4-bit binary coded decimal (BCD) values are specified.

The contents of CPU are used to determine the least significant unit of Y (LSUY) and least significant unit of X (LSUX) functions which are obtained when the BICn are XYST pseudo registers (respectively) are sourced. CPU is addressable separately as a source or sink, and is handled as if it were a 4-bit register. The two most-significant bits are non-existant and, therefore, return zeros whenever CPU is sourced.

CPL

The Control Parallelism Length (CPL) register consists of bits 0 through 4 of CP. CPL is used to designate the field length of data (1 to 24 bits) to be handled on arithmetic operations. In addition, CPL designates the data field length of S-memory Read/Write operations when the value in the FL register is 0. CPL is not addressable separately, but must be sourced or sinked as part of the 8-bit CP register. CPL values of 25-31 are treated as being equal to a value of 24.

LIT Register

The LIT (literal) register is an 8-bit register not addressable as such. The function of LIT is to receive and store eight literal bits contained in the 8C or 9C micro, pending a move of this data to another register (which move completes the 8C/9C micro execution). LIT is entirely hardware-controlled, and therefore invisible to the programmer. LIT is not accessible from the console.

MSSW Register

The Microinstruction Source Switch (MSSW) register is a 4-bit special purpose register which is used to determine the source of microinstructions for machine execution. MSSW is unusual in that the outputs of the D/M panel's MICRO SOURCE switch are ORed with the register output. MSSW may be loaded in the same manner as any other 4-bit hardware register.

The format of MSSW is shown in figure 1-16. MSSW can be sourced or sinked as a 4-bit register. However, the upper two bits are always equal to 0. The S0 and S1 bit configurations are defined as follows:

S0	S1	Micro Source	Name
0	0	Cache, but micro is fetched from S-memory on a Miss.	NORMAL
0	1	S-memory only; Cache is disabled.	S
1	0	Cache only; processor halts on a Miss.	C
1	1	M-register only; micro in the M-register repeats continuously.	FROZENM

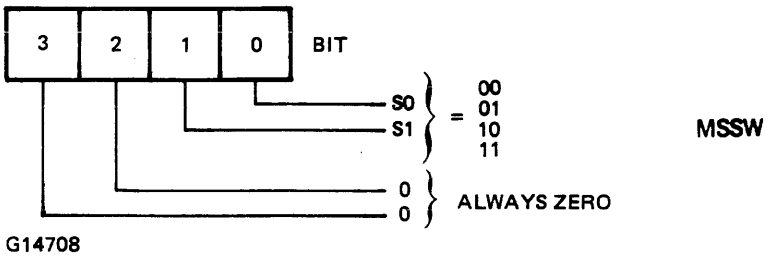

Figure 1-16. MSSW Register

U Register

The U register is a 16-bit register used exclusively as a means of entry for data from the cassette tape reader on the console. Since the data on cassette tapes is stored in serial fashion, conversion to parallel format is necessary. The U register performs the conversion by accumulating the incoming data bits until full, then gating them simultaneously to the MEX (on command). The U register is addressable only as a 16-bit source.

Associated with the U register is error correction logic which is capable of correcting errors in up to three sequential data bits. This correction logic makes use of the Forward Error Correcting Character (FECC) which is part of the tape data format. Error correction is discussed further in Volume 3, Theory of Operation, form number 1095551.

The U register functions somewhat differently in each mode of operation, (cassette tape, run). Therefore, each is described separately.

CASSETTE TAPE MODE

Selecting tape (MTR) mode causes generation of a 1C (Move U to M) pseudo micro, resulting in execution of micros directly from the cassette tape. This process is altered only if specified by a micro being executed. An example of such a deviation would be a 1C (Register Move) micro designating the U register as the source and some register other than M as the destination.

RUN MODE

In run (NORMAL) mode, U is sourced only when so directed by an executing micro. Since the accumulation of 16 bits in U is a relatively slow process compared with processor operation, completion of a micro that is using U as a source is delayed if U is not yet full at the time of execution. The cassette drive itself is controlled in the run mode by the 2E micro.

MAXS Register

MAXS (Maximum size of S-memory) is a 24-bit register which is set to indicate the amount of administrative memory. MAXS is a wired constant and is therefore addressable as a source only. The value in MAXS is binarily weighted, and adjustable by the field engineer. Refer to figure 1-17.

CSW Register

CSW (Console Switches) is a 24-bit pseudo register representing the data set on the 24 console switches, and can act as a source only. When addressed as a source, the console switch data is supplied to the destination.

TIME Register

TIME is a 24-bit register which is continuously incremented at the rate of one count for every three system clock pulses. The TIME register may serve as a source only; however, attempting to move data into it causes TIME to be reset to 0. TIME also wraps around to 0 when the count reaches the maximum value (all bits true). Only the 1C (Register Move) micro can access the TIME register. TIME may be reset only by the 8C, 9C, and 10C micros.

NULL Register

NULL is a 24-bit pseudo register representing all zeros. In actuality there are five NULL registers in the M-processor-3: NULLA, NULLB, NULLC, NULLD, and NULLE. The five registers have different register selection codes, but serve identical functions. Any of the NULL registers may serve as a source or sink, but the results obtained by accessing them depend on whether or not the processor is running.

When the processor is halted, a hardware-forced 1C micro (Move Register to Null) is constantly executing. The data gated to the main exchange consists of the contents of the register designated by the REGISTER GROUP and REGISTER SELECT switches (D/M panel). The main exchange data is displayed on the console lamps.

When the LOAD button is pressed (processor halted), the hardware forced 1C micro is changed to specify Move Null to Register. This causes the contents of the 24 console switches to be gated to and loaded into the register specified by the switches.

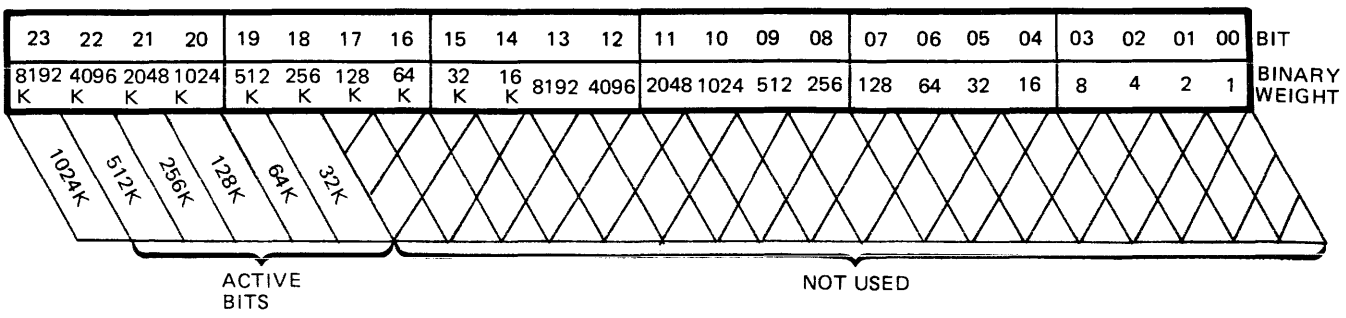

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Figure 1-17. MAXS Register

When the processor is running (or when START is pressed in the SINGLE MIC mode), execution of a micro designating NULL as sink causes the data to be gated to "nowhere." No registers are changed. If TAS is moved to NULL, the stack pointer is decremented by 1. On execution of a micro designating NULL as source when running (or when START is pressed in the SINGLE MIC mode), all zeros are moved to the designated sink, effectively clearing it. If NULL is moved to TAS, TAS is cleared and the stack pointer is incremented by 1.

NOTE

In the B 1720 processor a special feature known as "Halt on A = console switches" was provided. A similar function (which is now expanded to include "Halt on FA = CSW") is implemented in the B 1870/B 1860 processor, but it no longer involves the use of NULL. Refer to the Central System Operation discussion for further information.

CMND Register

CMND (Command) is a 24-bit pseudo register which is used exclusively for I/O operations. Designating CMND as sink on a Register Move or Scratchpad Move operation serves to enable gating from the main exchange to the I/O bus, and causes the Command Active (CA) signal to be generated. CA signals the I/O devices that information is present on the I/O bus for one of them, and indicates the first part of the two part I/O cycle. Since CMND enables output gating, it may serve as a sink only. The information transferred to the I/O system when CMND is sink may be operators, variants, channel number, reference addresses, file addresses, or write data. The 1C, 2C, and 10C micros can use CMND as a destination.

DATA Register

DATA is a 24-bit pseudo register whose function is complementary to that of CMND. DATA may serve as a source or destination, and is used to transfer data to and from the I/O bus. When used as a source, the processor generates the Response Complete (RC) signal to the interface and accepts 24 bits of data from the bus. RC is also generated when DATA is used as a destination, but data flow is in the opposite direction. DATA can be used as a source by the 1C and 2C micros, and as a destination by the 1C, 2C, and 10C micros.

INCN Register

INCN (interrupt conditions) is a 4-bit pseudo register which indicates interrupt conditions pertaining to dispatch operations. As such it is significant only in systems having a port interchange (port connect configuration). The meanings of INCN bits are shown in figure 1-18. INCN may serve as a source only.

Other Registers

Other pseudoregisters are outputs from the 24-bit Function/Rotator. These include SUM, DIFF, XANY, XORY, XEOX, MSKX, MSKY, XYST, XYCN, FLCN, and BICN. They are discussed within the 24-bit Function/Rotator description that follows.

24-BIT FUNCTION/ROTATOR (ALU)

The 24-Bit Function/Rotator, also called the (24-bit Arithmetic/Logic Unit or ALU, is the main logic element for processing numerical data within the system, and is used for most operations which require arithmetic or logical manipulation of two operands. The ALU has an input capacity of two operands, each a maximum of 24 bits in length. The ALU includes a function section, a rotator section, and masking capabilities. The function and rotator sections are essentially parallel devices, sharing the same inputs and active at different times. However, the ALU output passes through the rotator second stage en route to the MEX. Since the two sections (function,rotator) have distinctly different purposes, each is discussed separately.

Inputs (Shared)

Inputs to the function section are from the A-data and B-data gates. The rotator, on the other hand, receives the A-data inputs only. A-data and B-data sources are defined as follows:

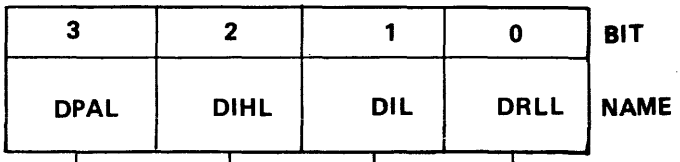
A Data:
- X Register
- Y register (also B data)
- T Register (also B data)
- L register
- FA register
- FB register
- LIT register
- CP register
- PERP register
- PERM register
- C register

B Data:
- Y register (also A data)
- LIT register
- CP register
- T register (also A data)
- Left scratchpad
- Right scratchpad
- BR register
- LR register

NOTE

The rotator has a separate input from the MAXS register; this is not a part of A data or B data.

In the above list, note that the Y and T registers are both A-data and B-data inputs. This variation occurs because both registers serve as B-data inputs to the ALU as well as having rotation functions in the microinstruction set.



DESTINATION PORT ABSENT LEVEL –
WHEN TRUE, IT INDICATES THAT A DISPATCH HAS BEEN SENT TO A PORT DEVICE WHICH IS NOT PRESENT

DISPATCH INTERRUPT HIGH LEVEL –
WHEN TRUE, IT INDICATES THAT A HIGH PRIORITY DISPATCH IS PRESENT. USED ONLY IN CONJUNCTION WITH DIL (BELOW)

DISPATCH INTERRUPT LEVEL –
WHEN TRUE, IT INDICATES THAT A DISPATCH IS PRESENT FOR THE PROCESSOR

DISPATCH REGISTER LOCK LEVEL –
WHEN TRUE, IT INDICATES THAT THE DISPATCH REGISTER (LOCATED IN THE PORT INTERCHANGE) IS IN USE

NOTE: ALL INCN BITS REFLECT CONDITIONS EXISTING IN THE DISPATCH REGISTER, WHICH IS LOCATED IN THE PORT INTERCHANGE. REFER TO THE PORT INTERCHANGE SECTION FOR FURTHER DETAILS.

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Figure 1-18. INCN (Interrupt Conditions) 4-Bit Pseudoregister

Actual input to the ALU for the operations it performs is received from the X and Y registers (except for the 4F (Bind) micro, in which it adds together the contents of the L and T registers). All the other A-data and B-data inputs pass through the rotator en route to the MEX. Rotation and masking are implemented for some of these sources, as defined by the microinstruction set.

ALU Function Sections

The ALU includes a binary adder/subtractor that performs the actual arithmetic functions between two operands. Both the input and output of this stage are in binary form. Generation of carry and borrow outputs is automatic.

The BCD decoding logic is used to convert the arithmetic output to binary-coded decimal (BCD) form. This is generally done for data which is destined for transmission to an I/O device. Translation to BCD is necessary for I/O operations which involve a printout because numerical values between 10 and 15 require generation of two characters, whereas only one is used in hexadecimal.

The status and condition result logic provides outputs which reflect the logical relationships existing between the 24-bit operands stored in the X and Y registers. The outputs of this logic include both logical combinations of the X and Y data, as well as indicators of conditions existing in and between the two registers. These outputs are discussed in the following paragraphs.

24-Bit Results

In operation the ALU may be regarded as a group of nine pseudoregisters which correspond to the actions it can perform. Obtaining a desired function is accomplished by placing the operands in X and Y, then executing a Register Move micro with the appropriate pseudo register as the source. The nine 24-bit pseudo registers are composed of the adder/subtractor and logical function outputs previously mentioned.

SUM

This pseudoregister produces a value equal to the sum of the X and Y register contents, plus the Carry flip-flop (CYF). The value in CPL specifies the length of both operands and the sum. If the sum occupies more bit positions than the length specified by CPL, the carry level (CYF) is generated. The value in CPU determines whether a direct binary or BCD sum is produced.

DIFF

This pseudoregister produces a value equal to the difference between the X register (minuend) and Y register (subtrahend) contents. The value of CYF (binary weight twice that of the most-significant bit of X/Y is also subtracted from X if set. When X = Y or X < Y and CYF is true, the borrow level (CYD) is generated. As with SUM, CPL determines the operand length, and CPU specifies binary or BCD output.

XANY

This pseudoregister produces the logical AND function of the values in X and Y. The AND function is defined as follows: Corresponding bits of the X and Y registers must both be true (binary 1) to produce a 1-bit in the same output bit position. CPL determines the length of the operand field.

XORY

This pseudoregister produces the logical OR function of the values in X and Y. The OR function is defined as follows: A true level in (binary 1) in a given bit position of either the X or Y register (or both) will produce a 1-bit in the corresponding bit position of the output. CPL determines the length of the operand field.

XEOY

This pseudoregister produces the logical Exclusive-OR function of the values in X and Y. The Exclusive-OR function is defined as follows. A true level in a given bit position of either the X or Y register (but not both) will produce a 1-bit in the corresponding bit position of the output. CPL determines the length of the operand field.

CMPX, CMPY

These pseudoregisters form the complement of X (Y) and hold the result.

MSKX, MSKY

These pseudoregisters produce the contents of those bit positions of X (Y) beginning with the least significant bit, referenced by the value in CPL. As an example, sourcing MSKX with a value of 6 in CPL will cause the six least significant bits of X to be gated to the output. The masking function is actually produced by the mask logic, which is a portion of the ALU output.

4-Bit Results

Use of the ALU involves, in many cases, programmatic decision making to determine what processor action would be appropriate following the one in progress. To accommodate these needs, special logic has been provided to monitor relational conditions existing in and between the X and Y registers, and the status of the logic. The condition/state indicator bits are arranged in 4-bit groups known as XYST, XYCN, FLCN, and BICN. These are pseudoregisters which can serve as a source only. These registers are described in the following subsections.

XYST

XYST (X-Y States) is a 4-bit pseudoregister representing states existing in the X and Y registers, and the processor interrupt state. Refer to figure 1-19.

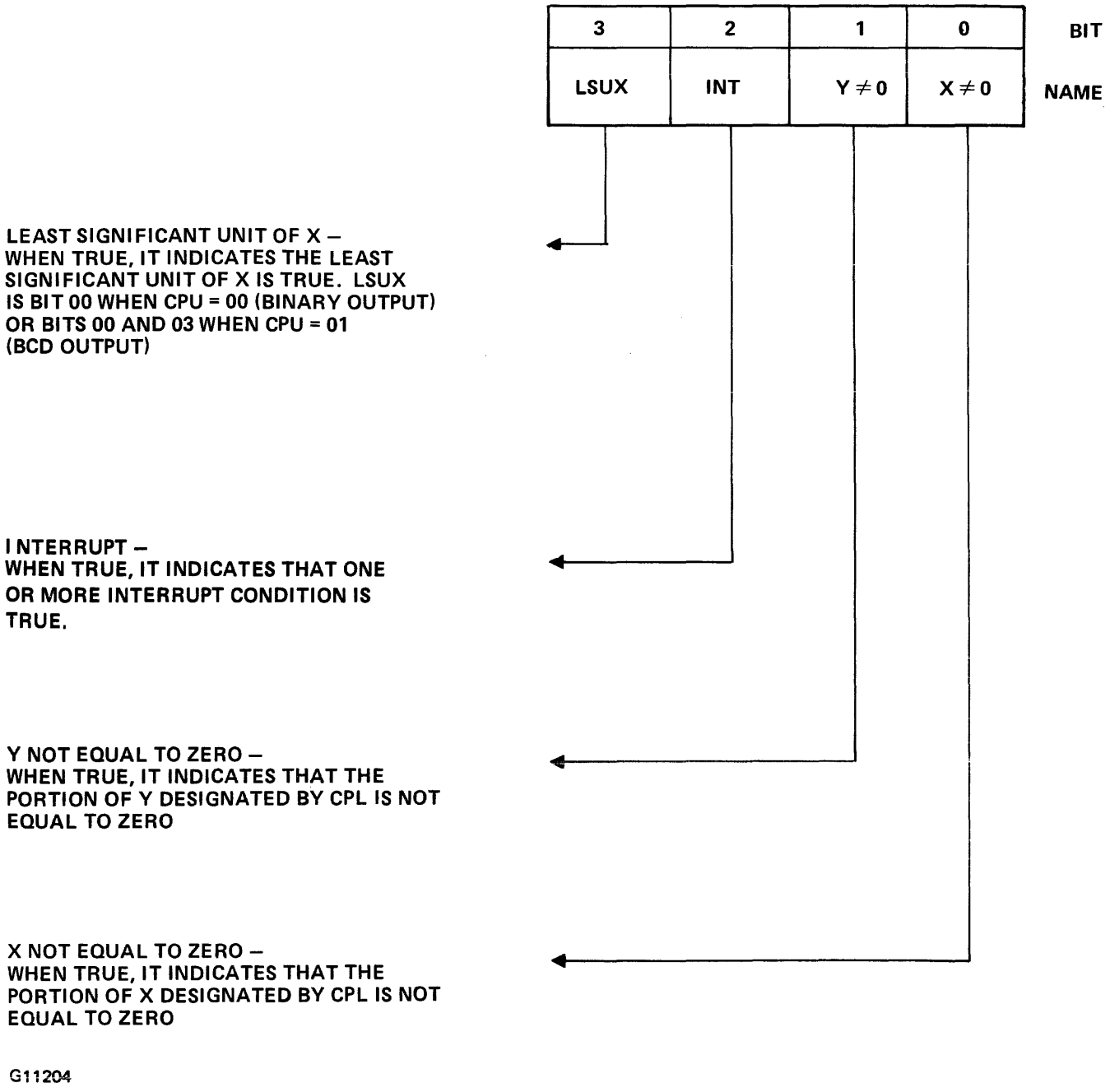


Figure 1-19. XYST 4-Bit Pseudoregister

XYCN

XYCN (X-Y Conditions) is a 4-bit pseudo register representing relational conditions of the X and Y registers. Refer to figure 1-20.

FLCN

FLCN (Field Length Conditions) is a 4-bit pseudo-register which indicates comparison conditions between the FL portion of the FB register and the corresponding portion of the first word of right scratchpad (referred to as SFL). Refer to figure 1-21.

BICN

BICN (Binary Conditions) is a 4-bit pseudoregister representing conditions present at the output of the 24-bit function box, and a state existing in the Y register. Refer to figure 1-22.

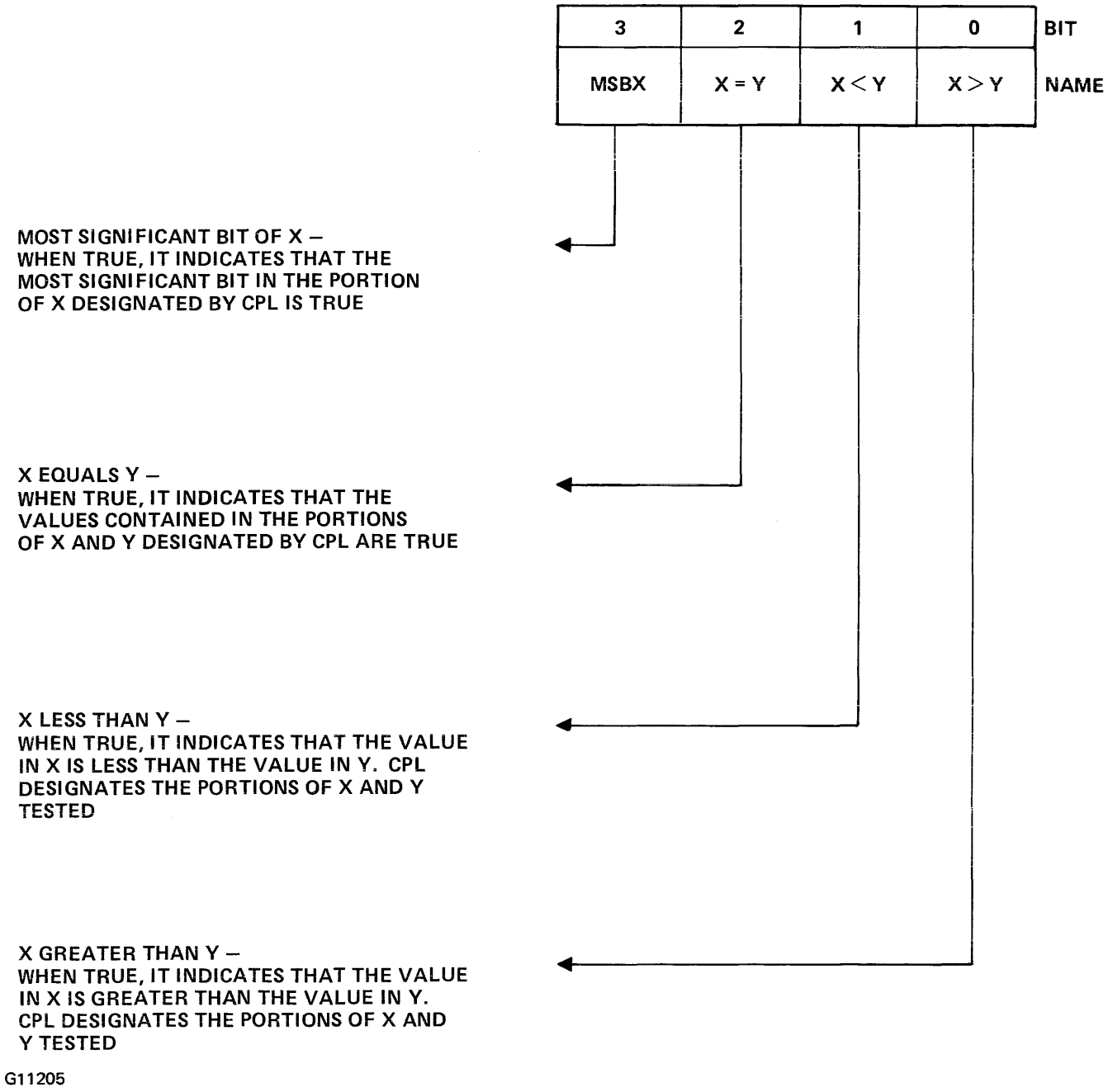
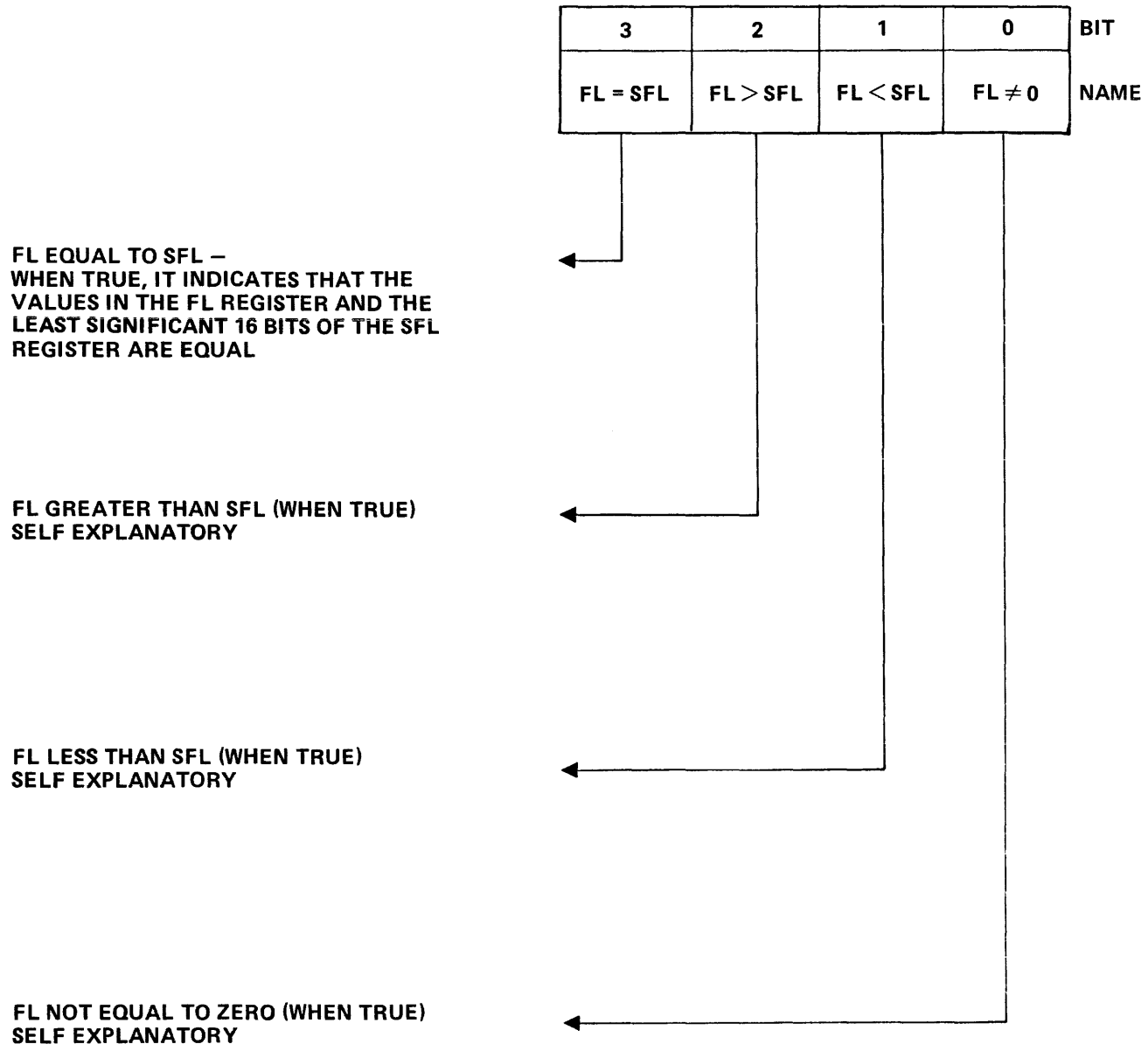


Figure 1-20. XYCN 4-Bit Pseudoregister



NOTE: FL IS THE LEAST SIGNIFICANT 16 BITS OF THE FB REGISTER
SFL IS A DISCRETE 24-BIT REGISTER WHICH ALWAYS CONTAINS THE SAME VALUE AS THE FIRST WORD (WORD 0) OF RIGHT SCRATCHPAD. ONLY BITS 00 THRU 15 OF SFL ARE CONSIDERED FOR THIS FUNCTION.

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Figure 1-21. FLCN 4-Bit Pseudoregister

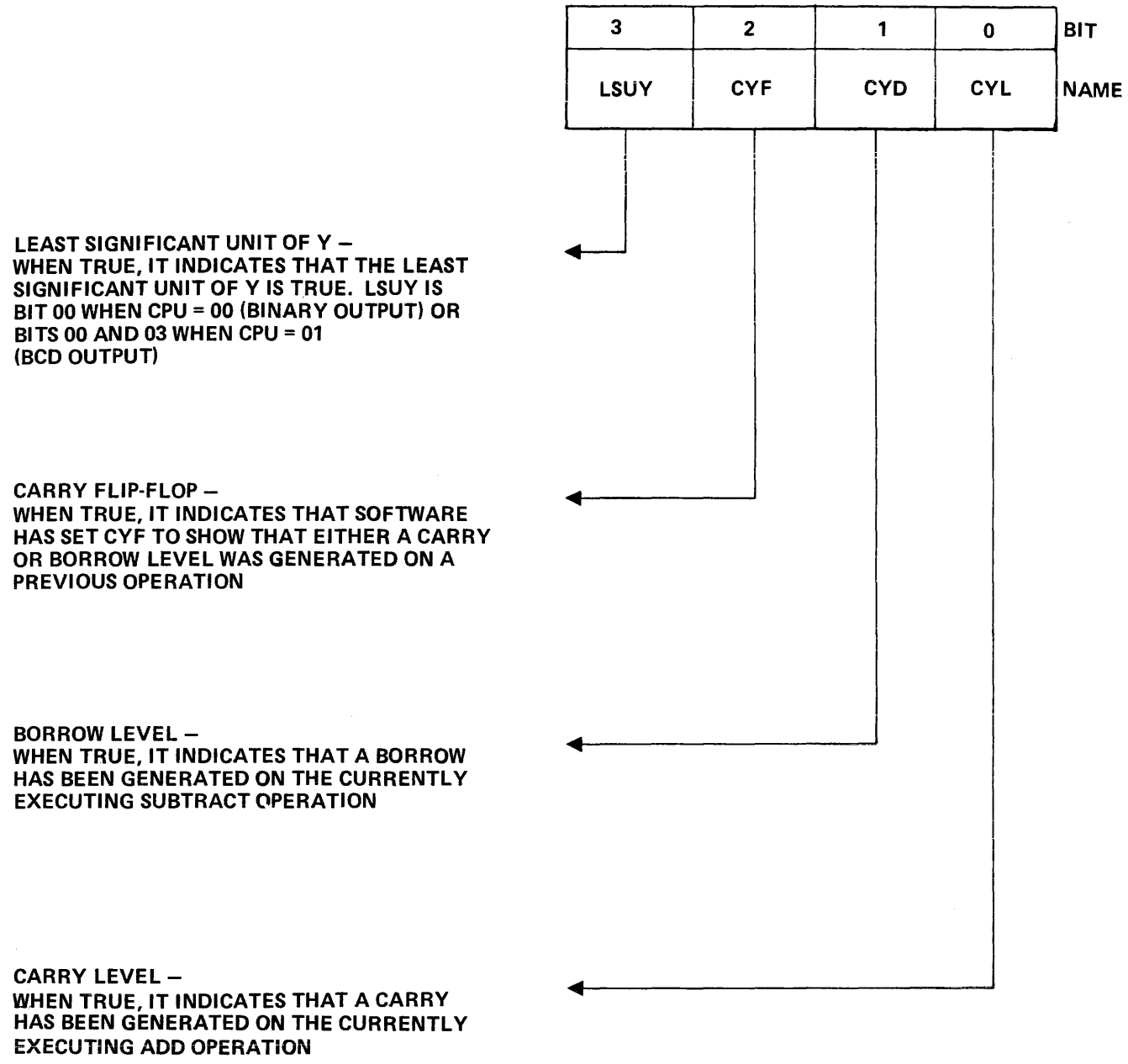


Figure 1-22. BICN 4-Bit Pseudoregister

ALU Rotator Sections

The rotator is a two-stage multiplexing device having a data rotation capability of from 0 to 23 bits. It is accompanied by a mask generator and mask logic, and therefore has rotation, shifting and masking capabilities. These functions are defined as follows:

a. Rotation Function: Simultaneous lateral movement of the contents of a given data field, with wrap around provided (data departing the field at one end simultaneously reappears at the opposite end).

b. Shifting Function: Simultaneous lateral movement of the contents of a given data field without wrap around (data departing the field is lost; zero fill occurs at the opposite end).

c. Masking Function: Selective out-gating of a portion of a given data field, generally a specified number of the least-significant bits.

The rotator includes "coarse" and "fine" rotation stages. The coarse stage rotates 0, 4, 8, 12, 16, 20, or 24 bit positions and the fine stage rotates 0 through 3 bit positions. The coarse stage has as inputs the A-data bus contents only, whereas the fine rotator accepts outputs of the course rotator as well as the ALU function section. Function outputs are not rotated; they are only multiplexed by the fine rotator. (See Volume 3, Form No. 1095551.)

Micro Access and Execution Logic

A microinstruction fetch is accomplished as follows: the micro is obtained from the location specified by the contents of the A register and gated to the M-register for decoding and execution. The location of the microinstruction is specified by an S-memory address, even though the micro is usually obtained from Cache memory. Cache essentially duplicates a portion of S-memory within the processor, providing rapid access to microinstructions. The hardware-management aspect of Cache operations comes from the automatic loading feature which is implemented when the desired micro cannot be found in Cache. The operation of Cache is further discussed below.

M-Register

The M (micro) register is a 17-bit register which is used to hold the microinstruction to be executed. The contents of M feed the micro decoding logic, and are used to produce the various enabling signals for causing the specified operation to occur. The contents of M are divided into four fields for decoding, which in the M-processor-3 amounts to addressing "stored" logic contained in a group of programmable read-only memories (PROMs). Refer to figure 1-23.

The normal input to the M register is from Cache memory, from which a direct path is provided. The M register can also receive input from the main exchange; this means is used when micros are entered from main (S) Memory, the console, or the cassette tape drive (by means of U register). The M register may also serve as a source or sink for Register Move operations. When used as a sink, the input data is bit-ORed with the incoming micro.

The M register incorporates parity checking on the microinstruction. The 17th bit (most significant) of M contains the odd parity bit, which is generated in the memory base in conjunction with the micro fetching process. The parity check is performed on the contents of M after each fetch, provided the micro comes from Cache or S-memory. The check is not made after a load from the console switches or the cassette tape or after a Register Move to the M register.

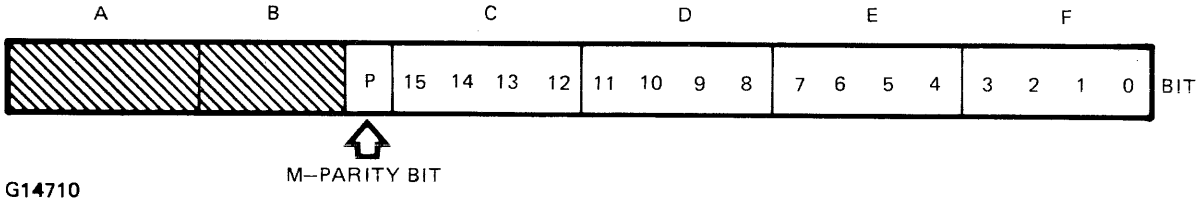


Figure 1-23. M-Register as Viewed on Console Lamps

A-Register

The A register is an 18-bit microprogram address register which is used to hold the address of the microinstruction currently being accessed (fetched) for execution. The address contained in A defines a location in S memory where the desired micro is to be found. However, actual micro fetching, in most instances, will be performed from Cache memory, which duplicates a portion of S memory. That is to say, the A address specifies a location in Cache where the desired micro is to be found, provided it was previously placed there by the hardware function for doing so. If the desired micro is not present in Cache, the same A address will be used to fetch it from S-memory. Concurrent with a fetch from S-memory, a hardware-controlled Load Cache routine is performed which results in writing the addressed micro plus the three succeeding micros into Cache. Micro execution with fetches from Cache then continues until another Miss is encountered or an exception condition arises. Finding the desired micro in Cache during the course of a fetch is termed a "Hit"; not finding it is a "Miss."

The A register (figure 1-24) is a two-stage register composed of sections known as A0 and A1. Two stages are required to hold the microaddress during the first two phases of the "fetch-decode-execute" procedure which is performed for each micro. Since there are succeeding micros in each phase of the "pipeline" at any given time, separate address storage facilities are needed to retain the contents of the A register in case they are needed (for reference purposes) when the micro is decoded. Therefore, the contents of A0 are known as the fetch address, and those of A1 the decode address. Transfer of the contents of A0 to A1 occurs concurrently with the move of the fetched micro to M.

The contents of the A0 register may be modified either by incrementing by 1 or adding/subtracting the contents of a 12 or 24-bit field. Incrementing by 1 occurs automatically with each fetch in the run, continuous or step mode. A0 is not automatically incremented in the MTR mode. Adding or subtracting some externally-originated value is part of a Skip or Branch operation. Wrap-around of A can occur and is permitted.

The A register can be addressed as either source or sink. The A0 register receives the main exchange, but does not drive it. Conversely, A1 drives the main exchange but does not receive it. When A is a source, the rightmost four bits received from A are always equal to 0; when A is a sink, the rightmost four bits of the source are lost.

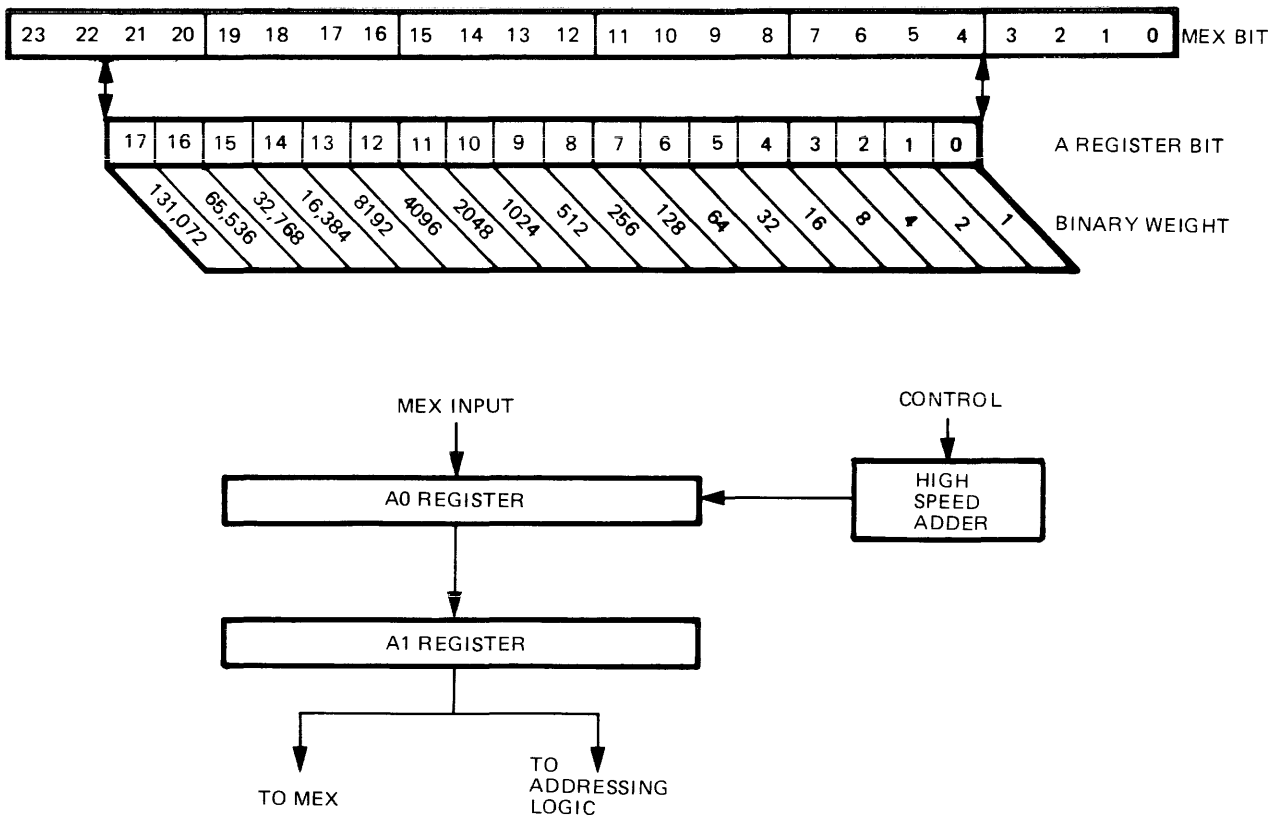


Figure 1-24. A-Register Block Diagram and Relationship to Main Exchange

A Stack

The A Stack is a 33-word deep, 24-bit wide memory with automatic addressing keyed to the entry or retrieval of data. The A Stack operates as a pushdown stack with a last in/first out structure. As such, the stack is generally used for storage of microaddresses in normal call/return programming where it is desired to perform a subroutine, then return control to the program when the subroutine is completed. The function of the A Stack in this is to store the program exit address while the subroutine is executing. The depth of A Stack makes 33 levels of nesting within subroutines possible.

The A Stack is addressed by a stack pointer which is upcounted or down counted by moves into or out of the stack. The position indicated by the stack pointer is known as the top of the A Stack (TAS). As such, it is a relative position within the stack, and its actual location is dependent on previous usage. New to A Stack (in M-processor-3) is the incorporation of an external latch register which serves as a buffer for data going to or from A Stack. This register effectively is the top of the A Stack, and extends the depth of the stack by one position (33 versus 32 words). A move to TAS results in retention of the write data in the TAS register. An actual write of this data in A Stack memory does not occur until another move to TAS is performed.

The time at which upcounting and downcounting of the stack pointer occurs is significant, since this determines the operational structure of the device. Moves into TAS cause the stack pointer to be upcounted before the write occurs. Moves from TAS cause the read to be performed before downcounting is allowed. The actual location within the stack indicated by TAS is dependent upon previous usage, and is invisible to the user. The stack pointer may wrap around in either direction.

Cache Memory

Cache is a high-speed memory located within the M3 processor and analagous to M-string memory in the M-1 and M-2 processors. Cache, like M-string, is used to hold microinstructions for fetching and execution, with the primary difference between the two being the manner in which micros are loaded and stored. Unlike M-string, Cache is hardware managed, with loading depending entirely on usage within the program being executed (M-string is loaded by software). The essential mode of Cache operation is delivery of microinstructions as specified by the contents of the A register, with automatic loading from S-memory when the desired micro is not present. Furthermore, each such load operation involves the desired micro plus the three succeeding micros (as stored in S-memory). This "load four" (stream mode) provision is sufficient to ensure loading the core of any given program within a short time after beginning execution. In fact, the reentrant nature of most programs allows a 98 percent success rate in accessing micros from Cache once stabilized operation is attained.

Cache memory is organized for the exclusive purpose of storing microinstructions, and has the capacity to store 2,048 (2K) micros. Cache storage is divided into words, blocks and classes as shown in figure 1-25. Each micro location is considered one word, with the "width" of Cache (the block) being four words. The length of Cache is expressed in classes, there being 256 classes of two blocks each (block A and block B). Cache addressing is index associative; this means that the physical location occupied by a given micro is only partially determined by the contents of the A register. In this scheme the least-significant 10 bits of the A address are used to determine the word and index at which the micro is to be stored. The eight most-significant bits of A (known as the key) are stored along with the micro (actually four micros, corresponding to the same storage configuration in main memory) as a means of identity. Note that there are two blocks per class. This feature provides the facility for storing two groups of four micros having the same index but different keys.

Fetching micros from cache involves comparison of the key portion of the A register contents with the keys stored at the cache location specified by the index portion of A. On a match of the two values (Hit), the desired micro (as specified by the word portion of A) is gated to the M register for execution. The absence of a match (Miss) causes initiation of the 4-micro load routine previously described. The incoming four micros are loaded into the block (of 2 at the addressed index) determined to be the "Least Recently Used" (LRU) by special logic provided for the purpose.

Various other capabilities provided for normal Cache operations and for diagnostic purposes are as follows:

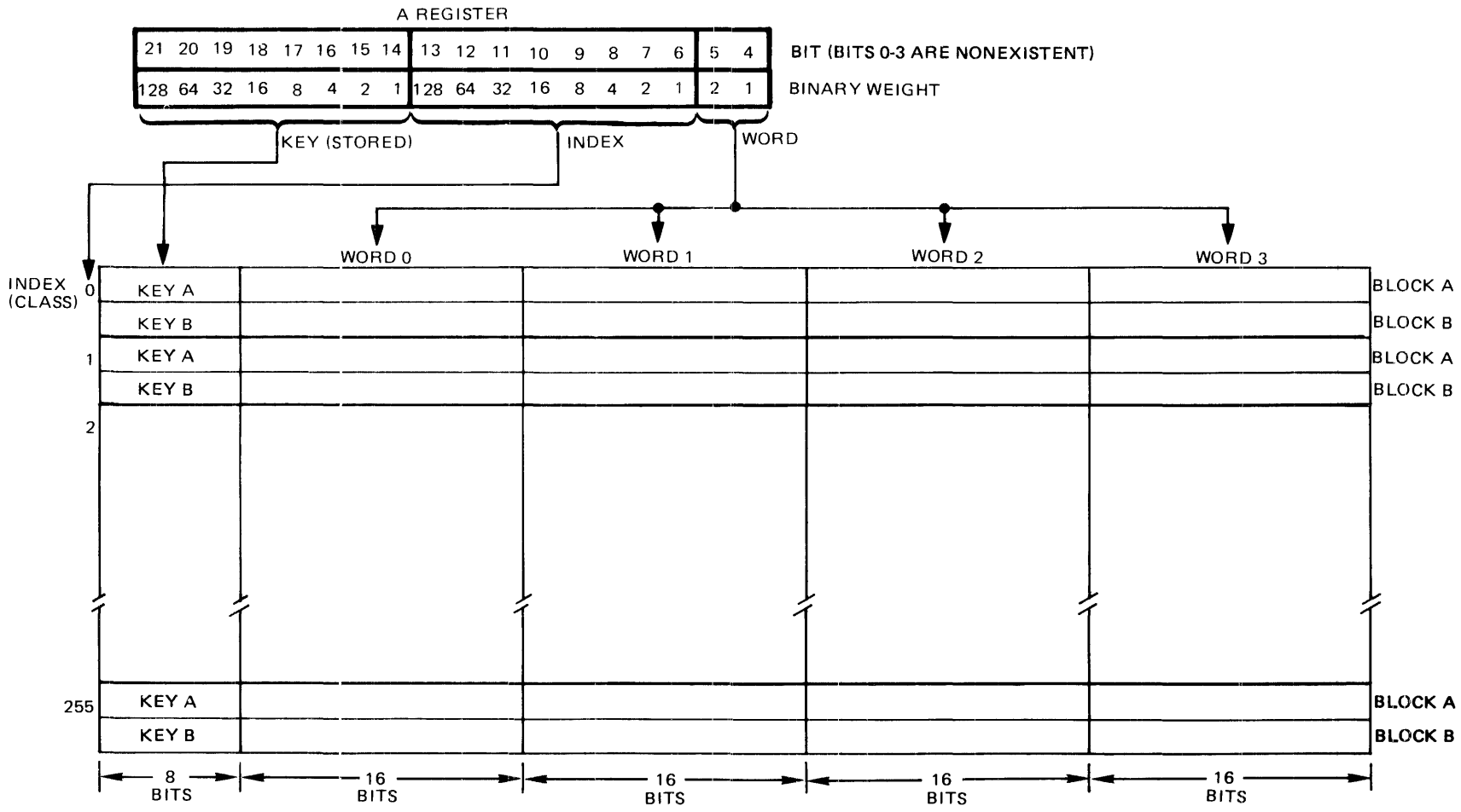
a. Read/Write Cache (7E) and Clear Cache (5F) micros are available. These are used primarily for diagnostic purposes.

NOTE

Reading Cache keys may be performed only by way of the Read Cache micro.

b. A validity bit accompanies each stored block, indicating whether or not that block contains any information (a false validity bit indicates good data). The validity bit is normally reset when the four micros are loaded from S-memory. However, validity bits may also be manipulated by writing in Cache from the console (resets validity bit), by executing the Clear Cache (5F) micro, or by pressing the CLEAR button. (Both Clear operations set the validity bit).

c. Parity generation and checking are provided for both the Cache word and Cache key storage. Micro parity is generated in the memory base and checked at the M-register. Cache key parity is both generated and checked within the Cache logic. Parity errors of both types are reported by way of the PERP register.



NOTE:

KEY STORAGE IS ACTUALLY 10 BITS IN WIDTH: 8 BITS ADDRESS, 1 VALIDITY BIT AND 1 PARITY BIT. LIKEWISE, MICRO STORAGE IS ACTUALLY 17 BITS WIDE: 16 DATA AND 1 PARITY.

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Figure 1-25. Cache Memory Layout and Addressing

NOTE

Cache key parity covers the eight key bits as well as the validity bit. In all, 10 bits are stored for each key.

4-BIT FUNCTION BOX

The 4-Bit Function Box is an arithmetic and combinatorial unit which is used to analyze and alter the contents of the four-bit processor registers, subregisters and pseudoregisters. Operations which utilize the 4-Bit Function Box involve manipulation of the contents of a single register, with the result being either returned to the source or the source being cleared (except for pseudoregisters, which may not be altered or cleared unless the conditions creating the states existing therein are changed). For operations requiring two operand inputs, one input comes from the source register, and the other from a literal or mask in the controlling micro. The 4-Bit Function Box is used primarily to generate and manipulate control signals within the processor, and is therefore, for the most part, a programmatic tool.

Inputs

In addition to a 4-bit literal or mask from the controlling microinstruction, any of the 4-bit processor registers or pseudoregisters may serve as inputs to the 4-Bit Function Box. The possible inputs are listed in table 1-1.

Table 1-1. Four-Bit Function Box Inputs

TA	LA	FU	CA	BICN
TB	LB	FT	CB	XYCN
TC	LC	FLC	CC	XYST
TD	LD	FLD	CD	FLCN
TE	LE	FLE	MSSW	INCN
TF	LF	FLF	NULL	PERM
				PERP

Operations and Functions

Operation of the 4-Bit Function Box is best explained in terms of the microinstructions which exercise it. A listing of these micros and the actions available is provided below. Note that the functions listed are those concerning the 4-Bit Function Box only; the microinstructions themselves may have additional variants affecting other logic.

1C (REGISTER MOVE), 2C (SCRATCHPAD MOVE)

These micros cause the contents of a 4-bit register to be moved to a 4-bit or 24-bit register. No manipulation or altering of the original sourced data is provided. Input (to the 4-Bit Function Box) is by means of the auxiliary 4-bit bus, and output is by means of the least-significant four bits of the main exchange. If a 24-bit register is selected as a sink, the four bits are moved to the least-significant four positions, and the remaining 20 bits are zero filled. Note that scratchpad may be a sink only.

3C (4-BIT MANIPULATE)

This micro executes the designated logical function, using the contents of the sourced 4-bit register and the least-significant four bits (literal) of the 3C microinstruction as operands. The functions include:

Function	Result
SET	Moves the literal to the designated 4-bit register. This value is also placed on the 4-bit result bus.
AND	Performs the logical AND function between the 4-bit register contents and the literal. (Both corresponding bits must be true for a true result bit.) The result is placed on the 4-bit result exchange.
OR	Performs the logical OR function between the 4-bit register contents and literal (either or both corresponding bits being true produces a true result bit). The result is placed on the 4-bit result bus.
EOR	Performs the logical exclusive-OR function between the 4-bit register contents and the literal; (either one, but not both, of the corresponding bits being true produces a true result bit). The result is placed on the 4-bit result bus.
INC	Binarily adds the 4-bit register contents and the literal. The result is placed on the 4-bit result bus. Overflow (carry) is not detected.
INC and TEST	Binarily adds the 4-bit register contents to the literal and monitors the result for overflow. Overflow causes the skip function to be initiated. The arithmetic result is not used.
DEC	Binarily subtracts the literal from the contents of the 4-bit register. The result is placed on the 4-bit result bus. Underflow (borrow) is not detected.
DEC and TEST	Binarily subtract the literal from the contents of the 4-bit register and monitor the result for underflow. Underflow (borrow) causes the skip function to be initiated. The arithmetic result is not used.

4C (BIT TEST RELATIVE BRANCH FALSE), 5C (BIT TEST RELATIVE BRANCH TRUE)

These micros test the specified bit of the selected 4-bit register, and branch on the results of the test. The branch is taken if the tested bit is 0 (false) for a 4C micro or if the bit is 1 (true) for a 5C micro. The relative displacement of the branch (number of micros skipped) is contained in the literal, and may be a maximum of 15 instructions for a positive branch of 13 for a negative branch. Negative branching results in looping back to a microinstruction in lower sequential order. No output is provided, as the source data is not altered.

6C (SKIP WHEN)

Input register (See table 1-1) bits that correspond with 1 bits in the mask are tested. Action depends on the variant:

Variant	Action
0	If any mask-referenced bit is 1, skip the next-in-line microinstruction. If the mask = 0000, do not skip.
1	If all the mask-referenced bits are 1's, skip the next-in-line microinstruction.
2	If mask=register, skip.
3	If all mask-referenced bits are 1's, or if the mask = 0000, skip. Also, clear (reset to 0) all mask-referenced 1 bits in the register.*
4	If any mask-referenced bit is 1, do not skip. If the mask = 0000, skip.
5	If all mask-referenced bits are 1's, or if the mask = 0000, do not skip.
6	If mask=register, do not skip.
7	If any mask-referenced bit is 1, or if the mask = 0000, do not skip. Also clear (reset to 0) all mask-referenced 1 bits in the register.*

* BICN, FLCN, XYCN, XYST cannot be cleared.

Outputs

The processed output of the 4-Bit Function Box is returned to the source register (excepting pseudoregisters) unless a variant which specifies clearing as a possible result is selected. When the "clear" condition arises, all zeros are returned to the source. Other outputs from the Function Box are the branch and skip signals which initiate those actions when the test conditions are met.

Processor/Memory Interface Logic

The memory interface within M-processor-3 consists of gating and control logic for causing the bidirectional gating of control signals and data to and from the memory. Functions provided by this logic are as follows:

a. Multiplexing of address information and data over a common bidirectional bus to memory.

b. Generating the necessary control signals to properly sequence the memory access operations.

c. Transmitting (to memory) user-originated control signals concerning the memory cycles. (Examples: transfer width, field direction sign.)

d. Executing a timing function which monitors the time allowed for completion of memory cycles.

NOTE

The port interchange is optional, since independent access to main-memory by devices other than the processor is not needed in many installations.

The following discussion deals with the processor/memory interface only; the Port Interchange and Memory Base Unit are described elsewhere in this section.

Memory Access

Access to S-memory, other than for loading micros into Cache memory, is gained through execution of any of several microinstructions (the 7C, 2D, 11D, and 1E micros). Causing the memory access to occur involves generation of appropriate control signals and sequencing the transfer of information. This function is performed by the S-memory interface section of the processor. This procedure is described in the discussion of the memory base unit (MBU).

Memory Interface Logic

Because in some configurations the S-memory serves devices other than the processor, the memory is not considered to be an integral part of the processor logic. To permit tailoring to individual user requirements, the memory and its interface logic were designed as discrete, modular elements which must be assembled and connected to form a usable system. The physical divisions of the memory access logic are as follows:

a. That portion which generates S-memory requests and controls gating memory data into and out of the processor (the processor/memory interface).

b. That portion which controls memory access by user devices (the port interchange).

c. That portion which performs the actual access operations to the storage elements (the memory base unit).

d. The reception and storage of indicator bits pertaining to memory operations (inputs to the PERM and INCN registers).

Memory interfacing in the B 1870/B 1860 system is considerably simplified from previous designs, due to the major revision of memory structure and the means by which micros are obtained for execution. Specifically eliminated in the processor memory interface are the need for different adapters for direct connect and port connect operations, the necessity for modifying the furnished address, comparison of the furnished address with reference values, storage of read data, and control of memory refresh operations.

I/O Interface

Communication between the processor and the peripheral devices connected to the system is provided by the I/O (input/output) subsystem. The I/O subsystem is comprised of a processor-to-I/O interface, an I/O base, and I/O controls. These devices are defined as follows:

Processor-to-I/O Interface	Provides communication between the processor and the I/O subsystem.
I/O Base	Distributes the I/O bus and provides physical facilities for the installation of I/O controls.
I/O Controls	Interface peripheral devices with the I/O system. Each control is a unique device which serves to control the operation of a specific type of I/O equipment.

I/O Operations

The overall purpose of the I/O subsystem is for communication between the processor and external devices which aid in its operation. I/O operations consist of conversions of data from one means of transmission or storage to another. This is a two-stage process involving a standard intermediate format common to all I/O devices. From the point of view of the processor, this arrangement means that

data transmitted to or received from an I/O device is always handled in the same way. Manipulations necessary for the proper operation of a peripheral device are the function of the I/O control associated with that device.

I/O Interface Logic

Processor interface with the I/O subsystem consists of control of gating functions, since the I/O Bus is simply an extension of the processor main exchange. Communication with the I/O subsystem consists of executing microinstructions which cause the gating functions controlling access to the I/O bus to occur. The I/O bus gates are controlled by register source/sink functions actuated by Register Move micros. These functions are known within the processor as the Command (CMND) and Data (DATA) pseudoregisters. Since CMND and DATA have different purposes, each is discussed separately as follows.

CMND

The CMND function serves as a 24-bit pseudoregister that can act as a destination only. The CMND function is used to transfer operation commands to devices on the I/O Bus. When CMND is sinked, the CA (Command Active) signal is generated, signalling the I/O subsystem that an I/O operation has been initiated.

DATA FUNCTION

The DATA function serves as a 24-bit pseudoregister that can act as either a source or destination. DATA is used for transfer of data to and from the devices on the I/O bus. When DATA is sourced or sinked the processor generates the RC (response complete) signal, informing the I/O system that the two-part I/O operation is completed.

Cassette Tape Drive and Cassette Control

Like its predecessors, the B 1870/B 1860 Central System is equipped with a cassette tape drive. The dedicated function of this tape drive is direct entry of microprograms to the processor. However, in the B 1870/B 1860, the option of using this tape drive in the additional role of an I/O device (with both read and write capabilities) is available. Also available is a second cassette drive, for which space is provided on the operator's panel. This second drive functions as an I/O device only. To use either or both drives in the I/O mode requires that a cassette I/O control be installed in the I/O base.

Operation of the primary cassette tape drive in the "System" mode (for direct entry of microprograms) is controlled by the processor cassette control, a device separate and distinct from the cassette I/O control. The processor cassette control operates the primary tape drive in the read-only configuration, with the output from the tape being assembled for the processor's use in the U register. Functions performed by the cassette control include conversion of the serial tape data to parallel form for processor use, error correction on the tape data (using the forward error correcting code which is part of the tape data format), control of tape movement and signalling.

Control of the cassette tape operating mode is provided by two switches, one on each control panel. Selection between the System and I/O modes is made at the CASSETTE SELECT switch on the diagnostic/maintenance panel. Selecting the I/O mode causes control of the primary cassette tape drive to be transferred to the cassette I/O control. The functions of the drive are determined by system software. Selecting the SYSTEM mode causes control of the primary drive to revert to the processor cassette control, and enables the secondary MODE switch on the operator's panel. This switch selects between the NORMAL and MTR submodes (described as follows):

Submode	Meaning
NORMAL	The cassette drive serves as a source for data during normal program execution. Control of the cassette drive is exercised through execution of 2E (Cassette Control) micros, and cassette tape data is utilized by executing Register Move micros with the U register as source.
MTR	Micro execution directly from the cassette is implemented by a hardware-forced "Move U to M" micro fetch routine. The cassette drive is started by way of the START button (operator's panel) when in MTR. Stopping is usually accomplished by the Cassette Control micro. The MTR mode is used for maintenance operations and for certain system functions such as the Clear/Start initialization.

Console Interface

Operator controls for the B 1870/B 1860 Central System are provided on two control panels. These panels are known as the Operator's Panel (op panel) and the Diagnostic/Maintenance Panel (D/M panel). This division of control means was made to simplify and separate the controls customarily used by a computer operator in day-to-day functions, yet retain a full diagnostic capability for use when needed.

Console Control Implementation

Console control functions, in most cases, duplicate functions that can be performed by microinstructions. Therefore, the outputs of the console controls are compatible with and integrated into the micro decoding and execution logic. Many of the console control functions are effected by generating "pseudo" micros or portions of micros. Others actuate logic elements directly. The controls and their functions are discussed individually in the following subsections.

Operator's Panel

The operator's panel contains the basic controls necessary for operation of the system under normal conditions. The panel also contains the shared cassette drive, and has space for installation of a second cassette drive for I/O use only. The operator's panel

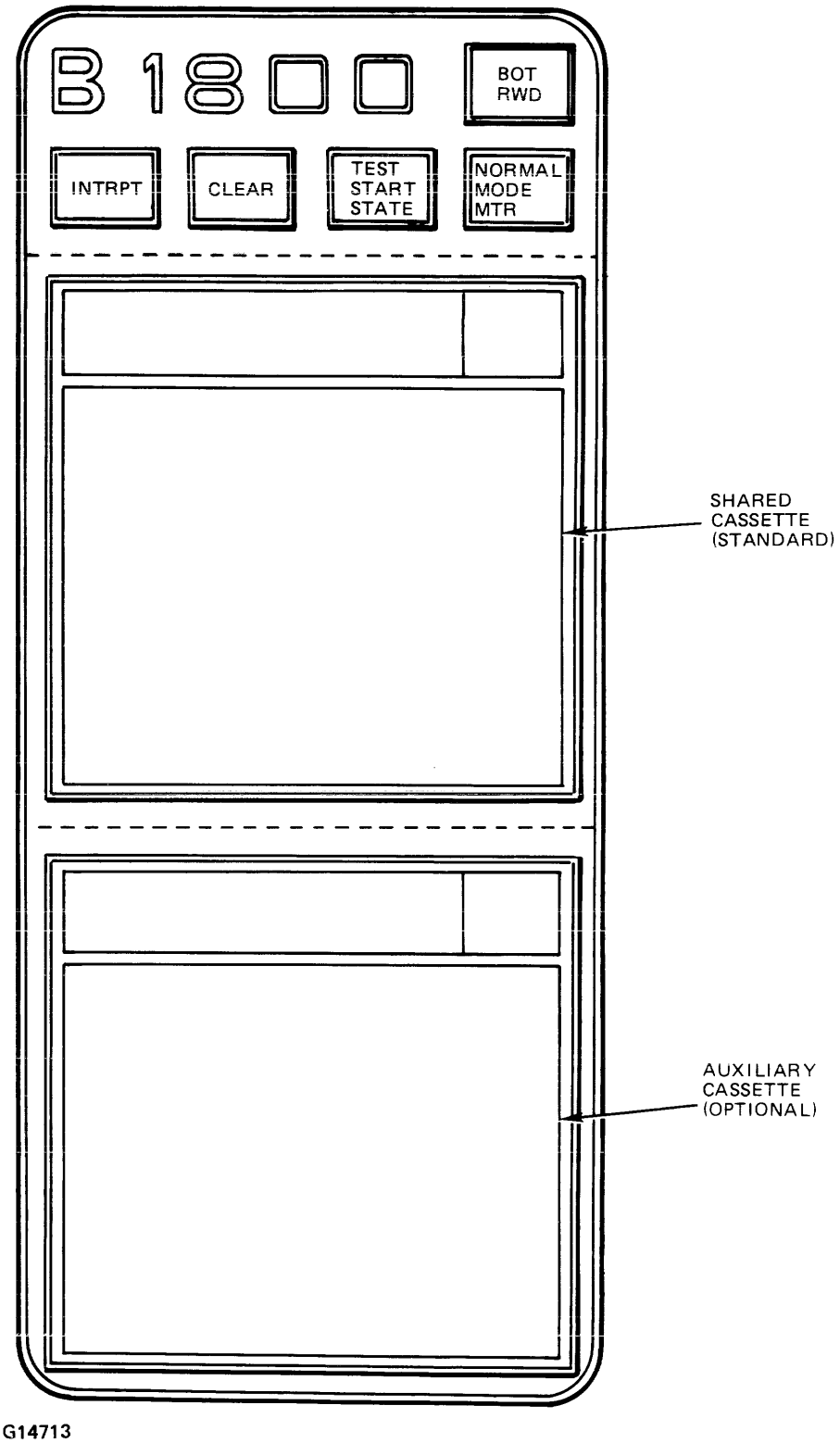

Figure 1-26. Operator Panel

and their functions are described below. Refer to figure 1-26.

INTERRUPT SWITCH AND INDICATOR

The INTRPT (Interrupt) switch is a two-position (latching) pushbutton with an internal indicator lamp. This switch is used to set the console interrupt bit in the CC register (bit CCO). This bit is interrogated by software, with actions following detection being determined by the executing program. The INTRPT lamp is lit when CCO is set. CCO cannot be reset by way of the INTRPT switch. The INTERRUPT switch on the D/M panel is identical in function to INTRPT on the Op panel.

CLEAR BUTTON

The CLEAR button is used for placing significant system registers and control flip-flops in the deferred clear state. This button is normally used only when the processor is halted. However, if the processor cannot be halted by ordinary means, the halt may be effected by simultaneously pressing the HALT and CLEAR buttons. The CLEAR button is duplicated on the Diagnostic/Maintenance panel.

START BUTTON AND TEST STATE INDICATOR

START, TEST STATE is a dual-purpose control. The START button is used to initiate processor operation from the halt state. The TEST STATE lamp, contained within the START button, is used to indicate that any of several conditions defined as abnormal exist within the processor. Conditions which cause the lamp to be lit are as follows:

a. Interrupt bit (CCO) set.

b. SINGLE/CONT switch (on D/M panel) in SINGLE position.

c. MICRO SOURCE switch (on D/M panel) in any position other than NORMAL.

MODE SWITCH AND INDICATOR

The MODE switch is a two-position (latching) pushbutton with an internal two-state indicator lamp. This control is used to select between the Normal and Maintenance Test Routine (MTR) modes of processor operation, and to indicate which mode has been selected. The meaning of the two modes is as follows:

Mode	Definition
NORMAL	Micros are fetched and executed in the manner intended for regular system operation. The source of micros is determined by the MICRO SOURCE switch (D/M panel) or the MSSW register.
MTR	Micros are obtained and executed directly from the cassette tape. Fetching consists of a hardware-controlled move of the contents of the U register to the M register. MTR is used for maintenance and diagnostic testing, and for limited entry of normal program material.

REWIND BUTTON AND BOT INDICATOR

BOT/RWD is a combined control and indicator used to initiate cassette tape rewind, and to indicate that the rewind has been completed. Rewind may be initiated only when the cassette drive is halted. The BOT lamp illuminates whenever the clear leader at the beginning of tape is detected. This control affects only the shared (top) cassette drive.

Diagnostic/Maintenance Panel

The Diagnostic/Maintenance panel provides controls and indicators necessary for repair and servicing operations. This console is equivalent to the main console on B 1700 series systems, but is less prominently located. The control and display functions provided are essentially the same as in earlier systems, with such changes as reflect the altered internal structure of the central system. Significant improvements in the capabilities provided include direct console access to scratchpad, micro (fetch) source selection, and shared system and I/O use of the cassette drive.

The Diagnostic/Maintenance panel controls and their functions are described below. Refer to figure 1-27.

24 CONSOLE LAMPS

The 24 console lamps provide a visual display of the contents of the 24-bit main exchange (MEX). This means is used for visually inspecting the contents of any desired register or a selected location in memory (when the processor is halted). When the processor is running, the lamp display indicates data flow through the main exchange, although useful information is probably not discernable due to the speed of operation.

24 CONSOLE SWITCHES

The 24 console switches are used for manual entry of data or addresses when the processor is halted. Access may be gained to any desired register or memory location in the same manner as viewing on the 24 console lamps. In practice the switches are manipulated to the desired bit pattern. Up is binary 1 (true); down is 0 (false).

HALT BUTTON

The HALT button is used to cause the processor to cease micro execution. Pressing HALT stops the processor at the end of the currently executing micro. The next micro to be executed is fetched and stored in M (except in MTR mode, in which the last micro executed remains in M).

CLEAR BUTTON

The CLEAR button duplicates the function of the operator's CLEAR button. This control is used for placing significant system registers and control flip-flops in the defined Clear state. Normally used only when the processor is halted.

START BUTTON

The START button duplicates the function of the operator's START button. This control is used to initiate processor operation from the halt state.

INTERRUPT SWITCH

The INTERRUPT switch duplicates the function of the operator's INTRPT switch. Raising this switch sets the console interrupt bit in the CC register (bit CCO), and lights the INTRPT indicator on the operator's console.

NOTE

Unlike the operator's INTRPT switch, this control is not combined with an indicator of its own.

STATE INDICATOR

The STATE lamp indicates, when lit, that bit 3 of

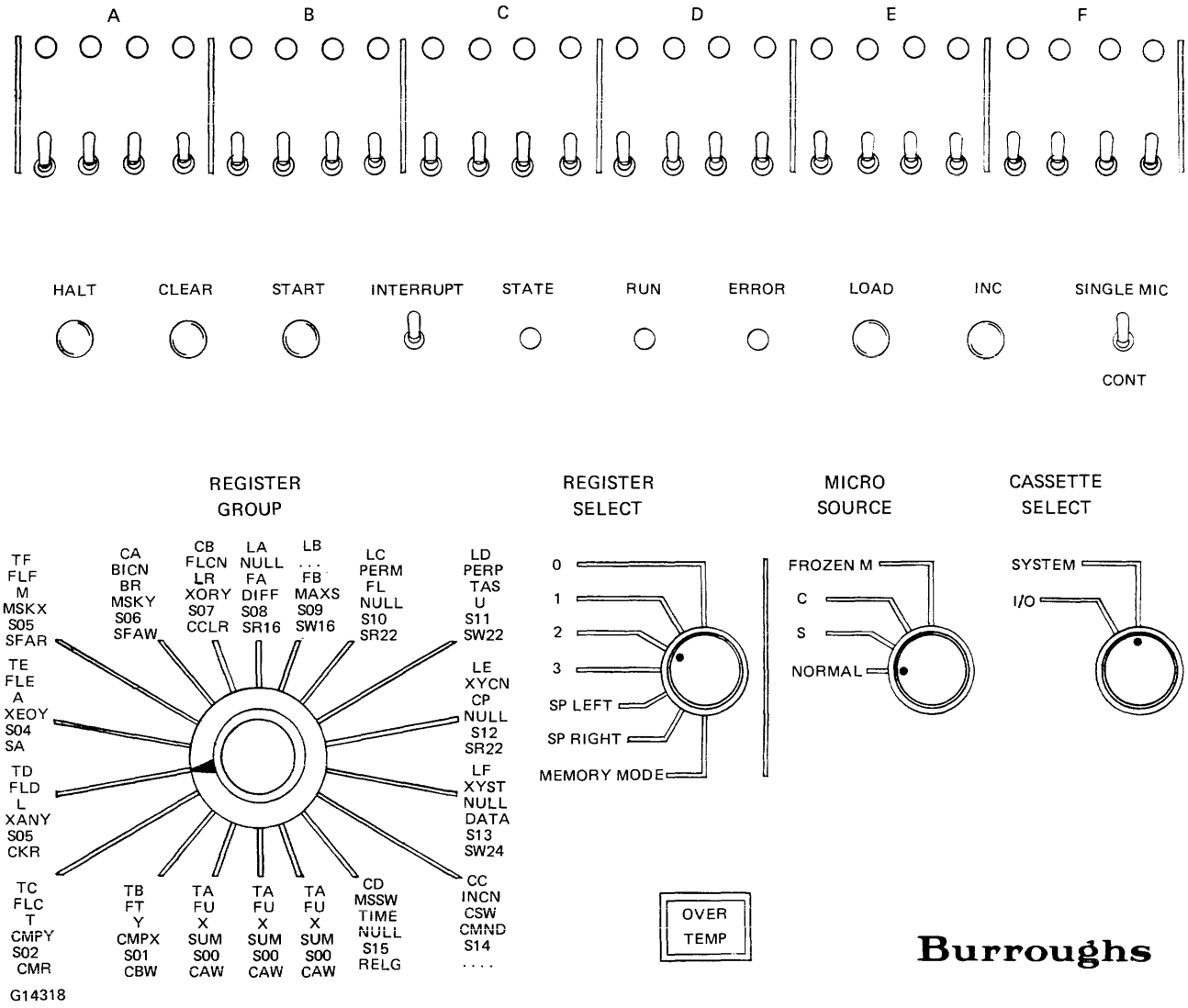

Figure 1-27. Diagnostic/Maintenance Panel

the CC register is set. This bit is set programmatically, and is used to provide the operator with a visual indication that selected events are occurring. (STATE has specific meaning only as defined by the executing program.)

RUN INDICATOR

The RUN lamp, when lit, indicates that the processor is running (executing micros).

ERROR INDICATOR

The ERROR lamp, when lit, indicates that a parity error has occurred. The ERROR lamp is lit whenever any condition occurs which sets the parity bit in the C register (bit CD3). In practice any condition which sets any bit in the PERM or PERP register also sets CD3, and causes the processor to halt (excluding PERM1). When this occurs, PERM and PERP may be examined to determine the exact nature of the error.

The ERROR lamp is automatically extinguished when the processor is started. The lamp may also be extinguished manually by placing the REGISTER SELECT switch in the MEMORY MODE position and pressing the LOAD button; the REGISTER GROUP switch may be in any position when this is done.

LOAD BUTTON

The LOAD button is used to actuate manual entry of data from the console. Pressing LOAD causes the contents of the 24 console switches to be gated to the register or memory element designated by the REGISTER SELECT and REGISTER GROUP switches. LOAD may be used only when the processor is halted.

NOTE

The procedures for accessing registers and memory locations from the console are discussed in the Processor Operation portion of this section.

INC BUTTON

The INC button is used to increment the address in the A-register (for accessing Cache memory) or the FA-register (for accessing S-memory). The amount these registers are incremented by is determined by the setting of the REGISTER GROUP switch. Refer to the processor operation discussion for further information.

SINGLE MIC/CONT SWITCH

The SINGLE MIC/CONT switch is used to select between single micro and continuous micro execution. In the SINGLE MIC mode (formerly known as "step" mode), the processor executes one micro and halts each time the START button is pressed. This ability is used primarily for diagnostic purposes. The CONT mode is the normal machine operating environment, with micro fetching and execution proceeding in a continuous manner.

CASSETTE SELECT SWITCH

The CASSETTE SELECT switch is used to place the primary cassette tape drive (on the operator's panel) in either the SYSTEM or I/O mode. These modes are defined as follows:

Mode	Definition
SYSTEM	The cassette serves as a read-only device for entry of microprogram material directly to the processor. The cassette output is assembled in the processor U register. Also, the cassette may be controlled directly through execution of certain micros.
I/O	The cassette serves as a data storage facility with both read and write capabilities. Control of the cassette's operation is assumed by the Cassette Tape Control, which must be included in the I/O Base for that purpose.

MICRO SOURCE SWITCH

The MICRO SOURCE switch is used to manually select the source of microinstructions for execution. The output of this switch is ORed with the MSSW register output, with the result that either may be used to choose the source of micros. The four switch positions and their meanings are as follows:

Switch	Definition
NORMAL	Micros may be fetched from either Cache or S-memory. This is the normal operational configuration.
C (Cache)	Micros may be fetched from Cache memory only.
S (S-Memory)	Micros may be fetched from S-Memory only.
FROZEN M	The micro presently in the M register is locked in place and repeatedly executed.

REGISTER GROUP and REGISTER SELECT SWITCHES

The REGISTER GROUP and REGISTER SELECT rotary switches are used to access any desired register or memory location for examination and/or alteration by way of the 24 console lamps and 24 console switches. The B 1870/B 1860 Registers (and "pseudo register" functions that are accessed as registers) are divided into groups of six which are selected by the REGISTER GROUP switch. An individual register or pseudo register within the group is then selected by moving the REGISTER SELECT switch to that register's relative position. Refer to figure 1-28.

Note that the B 1870/B 1860 system features full console access to scratchpad, and a variety of memory access operations not found on earlier systems. This has been accomplished by increasing the number of Register Select columns from four to seven. Columns 0, 1, 2, and 3 are essentially the same as in the B 1700 series systems, differing only with respect to certain register additions and deletions. Columns 4 and 5 are used for left and right scratchpad access respectively, with the scratchpad word address coming directly from the register group selection. Column 6 is used for memory access functions and several special halt functions. These memory mode functions are explained in the following table.

Register Group	Function
0	Console write to Cache block A and increment A by 16.
1	Console write to Cache block B and increment A by 16
2	Console read from Cache micro store and increment A by 16.
3	Console read from Cache Key store and increment A by 16.
4	Halt when the value set on the console switches equals the contents of the A register.
5	Halt when the value set on the console switches equals the contents of the FA register (on a memory read operation only.)
6	Halt when the value set on the console switches equals the contents of the FA register (on a memory write operation only.)
7	Clear Cache. The entire Cache memory (key store and micro store) is cleared when LOAD is pressed in this position. All validity bits are set to 1.
8	Console read of 16 bits (of data) from S-memory at the address specified by FA, and increment FA by 16.
9	Console write of 16 bits (of data) into S-memory at the address specified by FA, and increment FA by 16.

Register Group Switch	Register Select Switch						
	000	001	010	011	100	101	110
0 0 0 0(11)	TA	FU	X	SUM(1)	S00A	S00B	CAW(5)
0 0 0 1	TB	FT	Y	CMPX(1)	S01A	S02B	CBW(5)
0 0 1 0	TC	FLC	T	CMPY(1)	S02A	S02B	CMR(5)
0 0 1 1	TD	FLD	L	XANY(1)	S03A	S03B	CKR(5)
0 1 0 0	TE	FLE	A	XEOY(1)	S04A	S04B	SA
0 1 0 1	TF	FLF	M	MSKX(1)	S05A	S05B	SFAR
0 1 1 0	CA	BICN(1)	BR	MSKY(1)	S06A	S06B	SFAW
0 1 1 1	CB	FLCN(1)	LR	XORY(1)	S07A	S07B	CACLR(8)
1 0 0 0	LA	NULL	FA	D1FF(1)	S08A	S08B	READ16(6)
1 0 0 1	LB	. . .	FB	MAXS(1)	S09A	S09B	WRITE16(6)
1 0 1 0	LC	PERM	FL	NULL	S10A	S10B	READ22(6)
1 0 1 1	LD	PERP	TAS(2)	U(3)	S11A	S11B	WRITE22(6)
1 1 0 0	LE	XYCN(1)	CP	NULL	S12A	S12B	READ24(7)
1 1 0 1	LF	XYST(1)	NULL	DATA(4)	S13A	S13B	WRITE24(7)
1 1 1 0	CC	INCN(1)	CSW(1)	CMND(4)	S14A	S14B	. . . .
1 1 1 1	CD	MSSW	TIME(10)	NULL	S15A	S15B	RELOG(9)

NOTES:

1 SOURCE ONLY.

2 SOURCE ONLY. PUSH OR POP OF POINTER INHIBITED IS WRITE INHIBITED.

3 NOT AVAILABLE AS SINK OR SOURCE FROM CONSOLE.

4 LOAD WILL GENERATE CA FOR DATA, RC FROM CMND. RC INHIBITED WHEN LOAD NOT USED.

5 INC WILL CAUSE A TO INCREMENT BY ONE 16-BIT WORD, LOAD WILL CAUSE CACHE READ OR WRITE.

6 INC WILL CAUSE FA TO INCREMENT BY 16, LOAD WILL CAUSE S-MEMORY READ OR WRITE.

7 INC WILL CAUSE FA TO INCREMENT BY 24, LOAD WILL CAUSE S-MEMORY READ OR WRITE.

8 LOAD WILL CAUSE A CACHE CLEAR.

9 LOAD WILL CAUSE S-MEMORY ELOG TO BE READ AND DISPLAYED.

10 SOURCE ONLY. USING TIME AS SINK WILL CAUSE TIMER TO RESET TO ZERO.

11 REGISTER GROUP HAS 18 POSITIONS. POSITION 17 AND 18 ARE THE SAME AS POSITION 1.

G14715

Figure 1-28. Register Group and Register Select Coordinates

Register Group	Function
10	Console read of 22 bits (of data and error correction bits) from S-memory at the address specified by FA, and increment FA by 16.
11	Console write of 22 bits (of data and error correction bits) into S-memory at the address specified by FA, and increment FA by 16.
12	Console read of 24 bits (of data) from S-memory at the address specified by FA, and increment FA by 24.
13	Console write of 24 bits (of data) into S-memory at the address specified by FA, and increment FA by 24.
14	Not defined.
15	Read the contents of the Error Log Register.

OVER TEMP INDICATOR

The OVER TEMP lamp is used to indicate that one or more of the fans in the central system cabinet ventilation system has failed (this condition is detected by airflow switches). Ventilation failure causes automatic removal of power from the Logic Power Supply. The OVER TEMP indication may be reset by switching the main system power off, then on again. The ventilation problem must be corrected before again supplying power or the automatic power-down will be repeated.

S-MEMORY AND MEMORY ACCESS

S-memory is the primary data storage element within the B 1870/B 1860 central system. The memory is constructed as an independent, random access storage medium which may be accessed in a variety of ways. In operation the memory may be accessed by the processor or by other devices (such as a multiline control) which are part of the system. The memory, its operation, and the means of access thereto are discussed in the following subsections.

S-Memory Composition

The S-memory is made up of random access integrated circuit memory chips, and is dynamic in nature (stores data only when power is applied). S-memory as incorporated in the B 1870/B 1860 system is word oriented (16 bits per word) and utilizes error correction techniques; these provisions represent a radical departure from past designs. As viewed by the processor the memory is an electrically continuous field of bit locations which can be randomly accessed beginning at any selected bit. Memory accesses can involve from 0 to 24 bits per cycle. The bit addressability feature is provided by special logic included for this purpose.

Within each chip any single bit location may be accessed at a given time. Addressing these locations is accomplished by way of six binarily weighted address lines, with the required 12 address bits being entered sequentially in two increments. In this context the storage medium may be viewed as an array of 64 rows and 64 columns of bit locations, with one 6-bit address increment specifying a row coordinate and the other a column coordinate. Refer to figure 1-29. Decoding of the multiplexed address is internal to the chip.

Since each memory chip can access only one bit position at a time, storage and access for multiple bit data fields is by an array of memory chips which are addressed in parallel. The number of such chips is determined by the basic unit of data handled by the using system. This memory "width" is equal to 16 bits in the B 1870/B 1860 system, corresponding to the standard length of microinstructions.

NOTE

Do not confuse the 16-bit "basic unit of memory" with the maximum data transfer per operation, which is 24 bits. The "basic unit" refers to the physical structure of the memory components.

Added to the 16 bits of data storage in the basic unit of memory are six error correction bits, which are stored and accessed in parallel with the associated data. Therefore the actual physical width of the basic unit is 22 bits, although only 16 bits are visible to the user.

In physical terms the memory is composed of rows of 22 memory chips installed on logic cards, with each card containing four such rows. The capacity of a storage card is 4096 (bits per chip) x 4 (chip rows), or 16,384 (16K) words of memory. This corresponds to 32K bytes. Half populated (two rows of chips) memory cards are also available. A memory storage card is illustrated in figure 1-30.

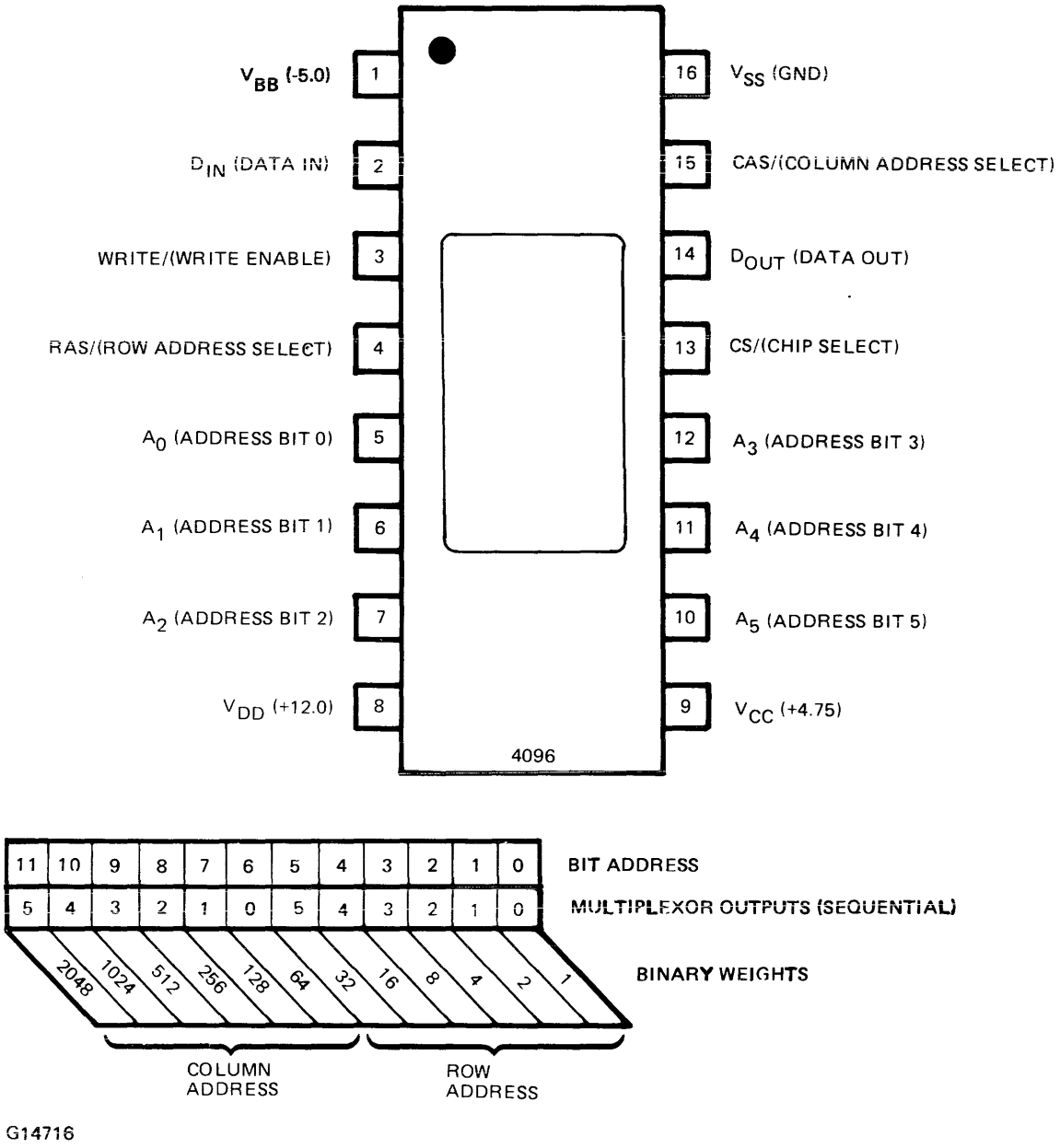

Figure 1-29. 4K Memory Chip

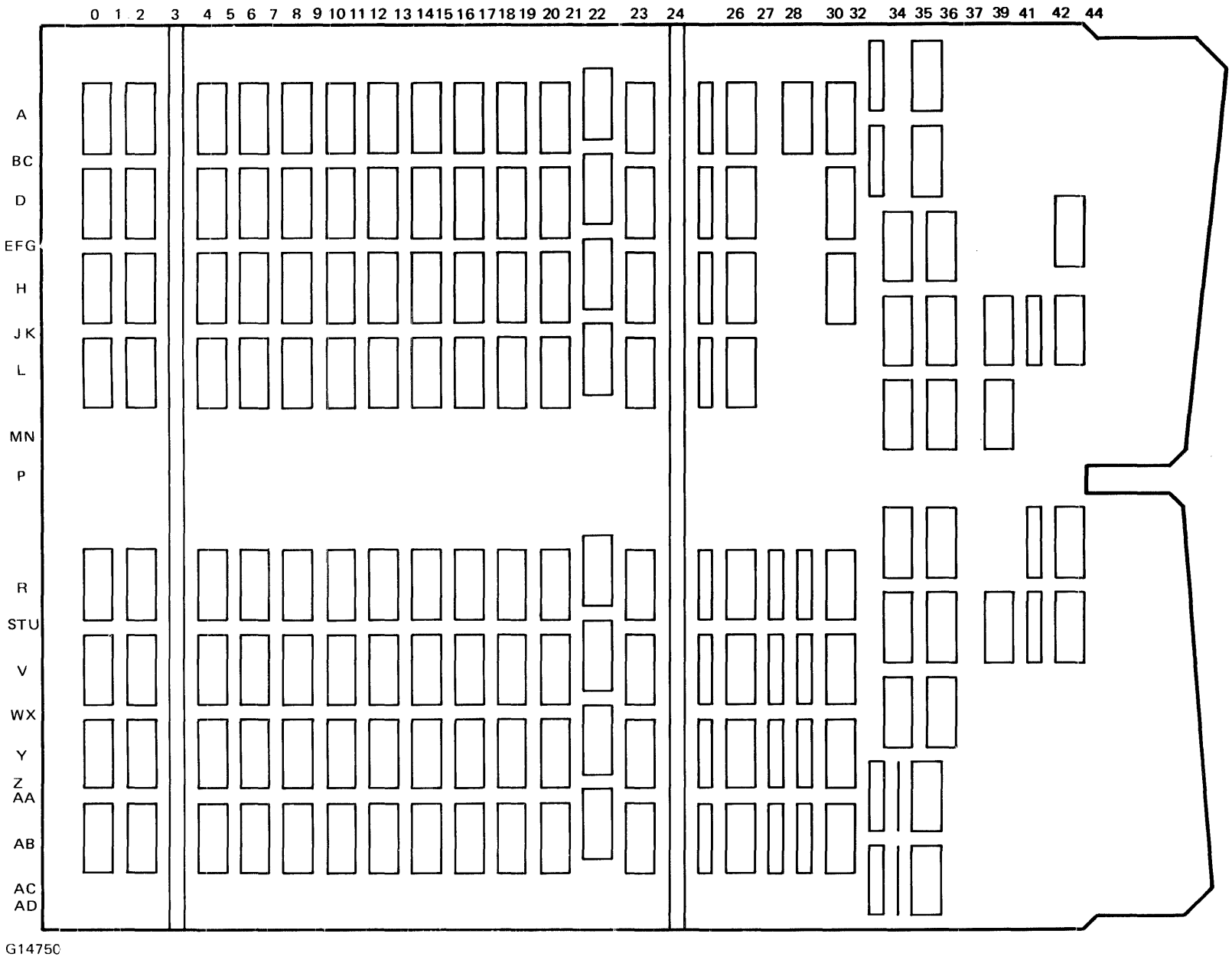

Figure 1-30. S-Memory Storage Card

Memory Access

Gaining access to memory for the purpose of reading or writing is a three-stage process which involves the following actions:

a. Accessing the correct storage elements and bit locations therein.

b. Left or right lateral movement of the data being transferred into or out of storage to provide the correct alignment between the input/output lines and the selected storage locations.

c. Limiting the number of bits transferred into or out of storage to the amount specified for the operation.

All memory access operations are accomplished by supplying the interface logic with a set of parameters describing the desired access. These parameters (see figure 1-31) include the following:

a. A 24-bit "memory address" which is equal to the absolute binarily-weighted number assigned the bit location (starting bit) where the access is to begin. (All bit locations in memory are numbered sequentially.)

b. A five-bit "Data Field Length" which specifies the field length of the data to be stored or read from memory. The maximum field length for each operation is 24.

NOTE

Data Field Length is also known as "Transfer Width."

c. A 1-bit "field direction sign" which specifies that the operation is to involve either the higher numbered or lower numbered bit locations adjoining the starting bit (in addition to the starting bit itself).

After obtaining the necessary information, the interface logic performs the three stages of the access cycle as described in the following subsections.

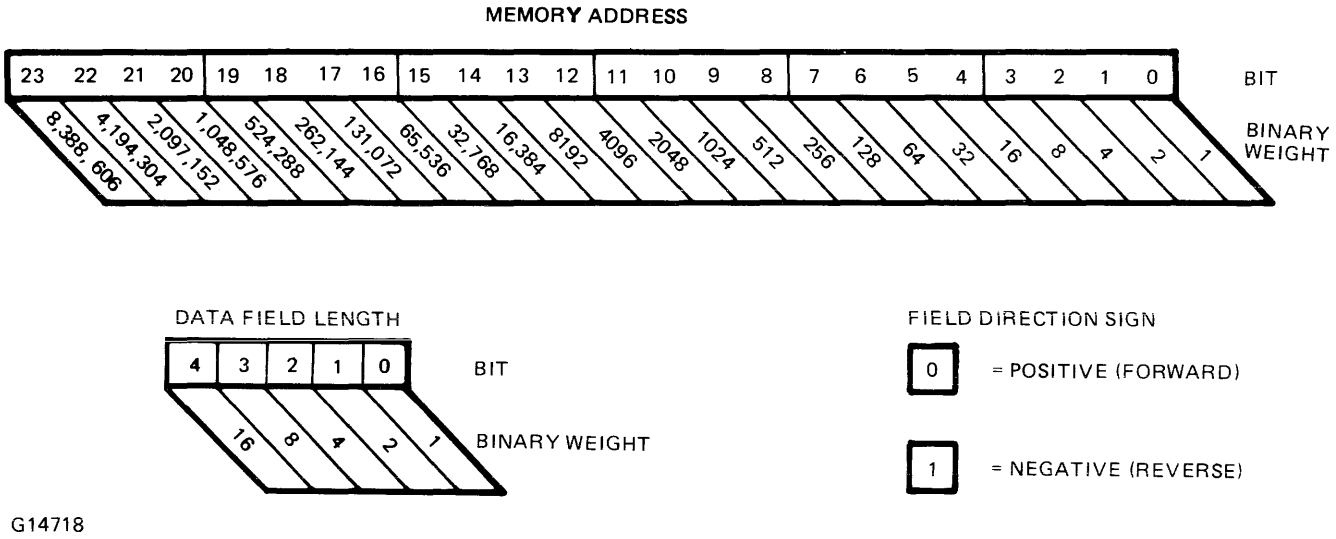

Figure 1-31. Memory Access Parameters

Storage Element Access

Functional memories in the B 1870/B 1860 series systems are assembled of groups of four memory cards, with the minimum configuration being four cards and the maximum consisting of 16 cards. The storage elements are configured electrically as shown in figure 1-32, having an effective "width" of 64 bits of data storage (this being the manner of assignment of addresses).

A combined physical/electrical representation of the memory is shown in figure 1-33, which also illustrates the significance of the various memory address bits. Each rectangle in the illustration represents one memory card, with the horizontal rows of cards being known as card groups, and the vertical columns as stacks. The memory shown is the maximum configuration of 16 cards. A minimum configuration memory would consist of one card group (four cards).

Access to the cards is one at a time, with the card group select and stack pointer portions of the address specifying the card within the 4 x 4 matrix to be accessed. The internal address within the storage card is specified by the chip row and chip address select portions of the address. Bit addressing, where the desired data field does not reside within even 16-bit boundaries, is performed externally.

As mentioned previously, memory accesses may involve data fields of up to 24 bits in length, and may begin at any desired bit location. Such requirements are met by causing memory access cycles to be multi-phase events in which the necessary stack (storage card) accesses are performed sequentially. For selection of succeeding memory locations, the memory control modifies the initial address supplied by the user device. Since the desired storage locations may occupy as many as three stacks, one address modification is necessary in some cases.

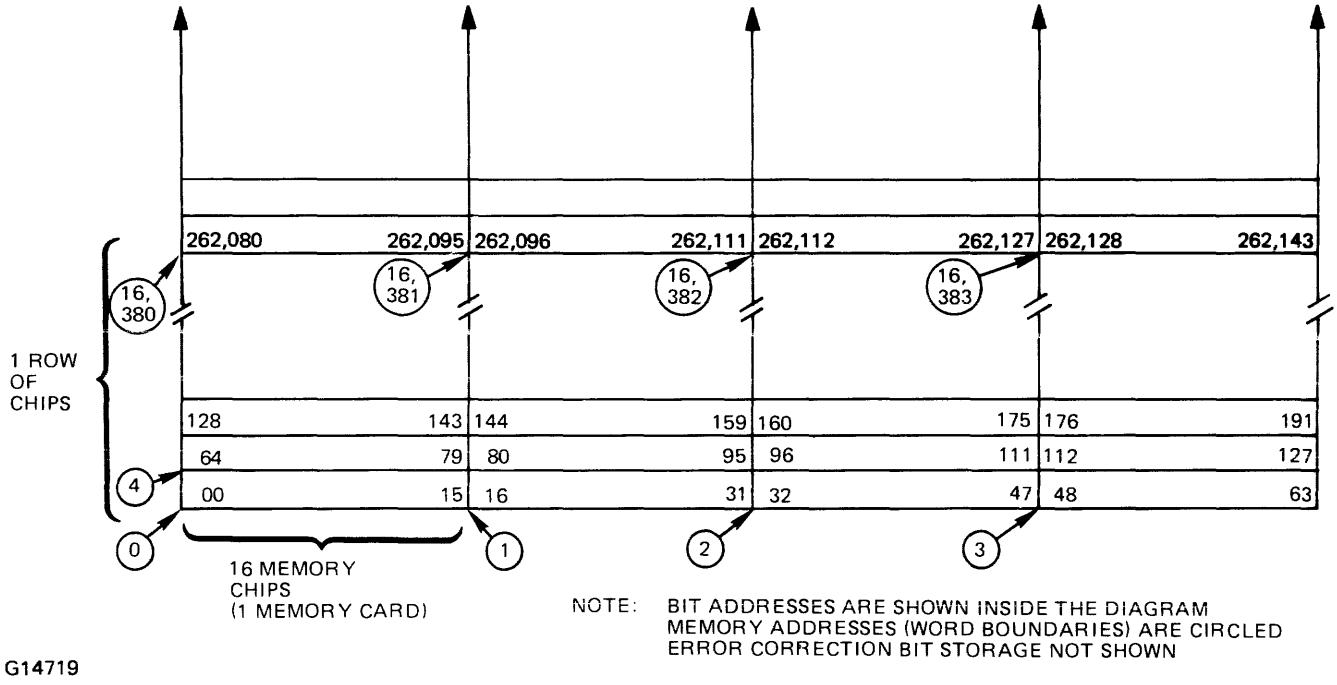

Figure 1-32. S-Memory Layout

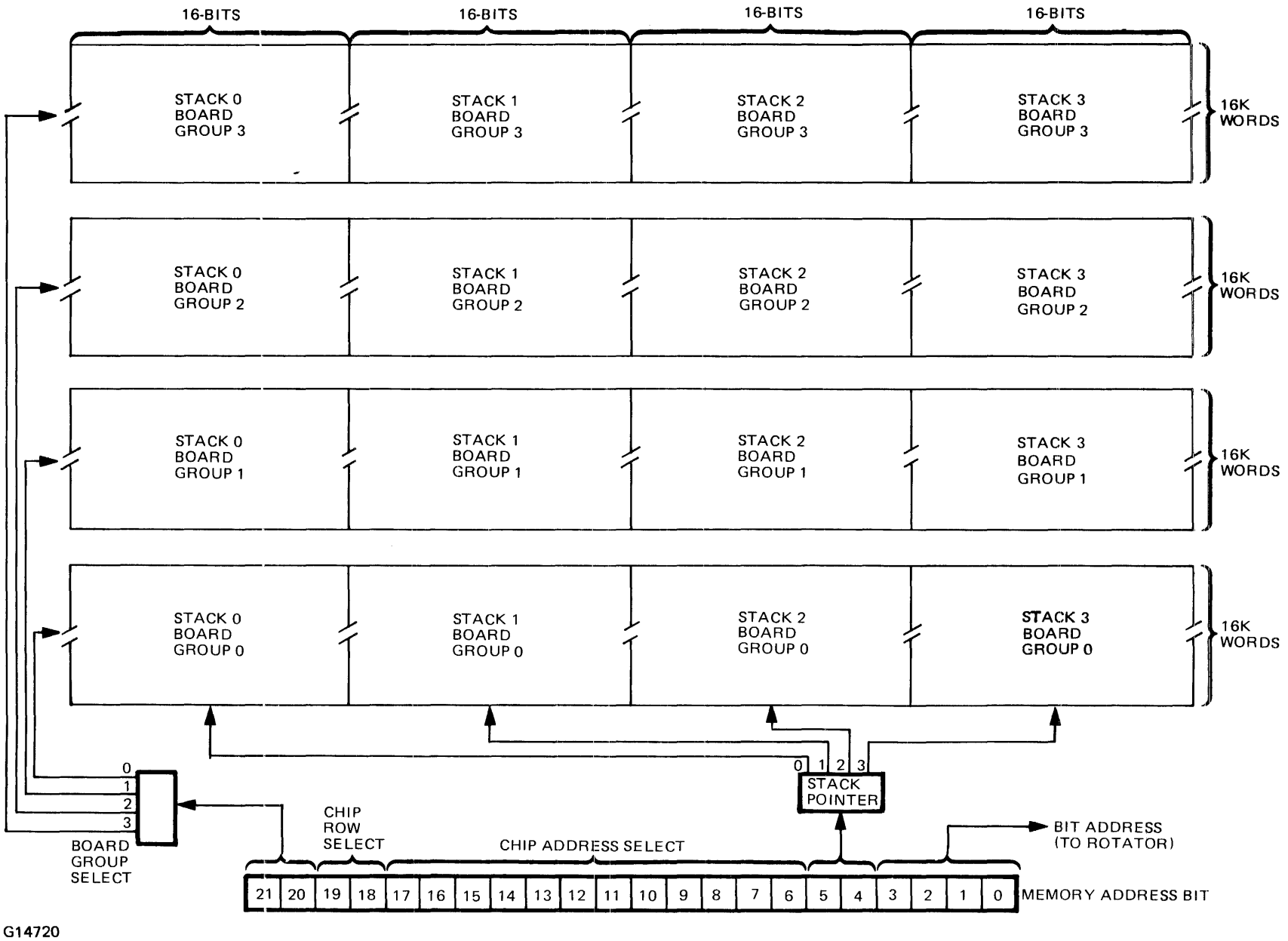

Figure 1-33. B 1820 Memory Addressing

Memory Cycles

To understand the functioning of the memory access logic a knowledge of the types of memory cycles that may be performed is needed. There are eight basic types, and within these a number of individual variants. The memory cycle types are as follows:

Micro or Pseudomicro	Result
7C READ (Micro)	Accesses the contents of a specified field in S-memory and gates this data to the MEX for use within the processor. The access operation may involve from 1 to 24 bits of data, and may address any bit location within memory.
7C WRITE (Micro)	Moves a field of data from a source in the processor to S-memory, storing it at a specified location. The data previously stored at the accessed location is overlaid. The access may involve from 1 to 24 bits, beginning at any bit address within memory.
2D SWAP (Micro)	Exchanges a field of data from a source within the processor with the contents of a similar field in S-memory. The operation may involve fields from 1 to 24 bits in length, and may access any bit address in memory.
1E DISPATCH (Micro)	Writes or reads a dispatch message (to or from another port device) at address 0 in S-memory, and/or alters the contents of the dispatch register. Dispatch operations are not implemented where the processor is the sole user device of memory. However, certain dispatch-related functions are performed regardless of the system configuration to satisfy programming requirements.
CONSOLE READ (Pseudomicro)	Accesses the contents of a specified address in S-memory and moves this data to the console lamps for viewing. This operation is executed from a hardware-forced micro instruction created in part by the console register selection switches. Data field length and direction are preset. Console reads may be performed only when the processor is halted.
CONSOLE WRITE (Pseudomicro)	Moves the contents of the console switches to S-memory, writing this data into a specified address. This operation is also executed from a hardware-forced microinstruction created in part by the console register selection switches. Data field length and direction are present. Console writes may be performed only when the processor is halted.
FETCH (Pseudomicro)	Accesses the contents of a 16-bit word (at even stack boundaries) and moves the contents to the processor. Single micro or 4-micro fetches may be performed, depending on conditions existing in the processor. Fetching is a hardware-forced means of accessing micro operators in S-memory. The destination within the processor depends on the subcategory of fetch being performed:

Subcategory	Destination
Single Micro S-Fetch	M Register.
C-Micro S-Fetch	M Register and Cache Memory.
9C Literal Fetch	As specified by previous micro.
M-Sink Fetch	M Register (OR-ed with data loaded in M by previous micro).

NOTE

The 4-micro stream-mode fetch is the normal operating activity within the system, occurring when a miss is encountered when fetching micros from Cache memory.

Port Interchange

The port interchange is an optional interfacing device for controlling memory access when more than one user device is present. The interchange has the basic function of determining which user device is to be granted memory access, then directing the flow of addresses, control signals and write data to memory and read data from memory. In addition to the processor interface, the port interchange provides facilities for connection of up to three synchronous or asynchronous port devices. Examples of such user devices are as follows:

a. Multiline Control (synchronous). Provides input and output to a number of remote data terminals.

b. Bus Interface Control (asynchronous). Provides interfacing with a B 6700 system, for which the B 1870/B 1860 central system serves as a "Reader/Sorter processor."

Specific functions provided by the port interchange (in addition to address and data gating) are as follows:

a. Priority resolution for control of access requests by user devices.

b. Generation of Clear signals for initializing purposes.

c. Control of dispatch operations, including the dispatch register and associated logic.

d. Temporary storage of memory read data.

e. Internal sequencing of its own operations to satisfy control requirements of the memory and the user devices as well.

The port interchange assembly consists of a four-card backplane containing the interface and control

logic (on one card), and spaces for three port adapter cards. The processor connects directly to the port interchange, and is accordingly known as a close-coupled port. Each synchronous/asynchronous port device used requires an accompanying port adapter.

Memory Base Unit

The memory base unit is the basic element of assembled S-memory, and includes both memory storage cards and control logic. The memory base has the basic function of controlling the distribution of addresses to the memory cards, plus control of write data entry and read data departure from storage. To implement these general requirements a number of specific functions are provided. These are as follows:

a. Control of all addressing activities, including direction of the basic address and the modified address to the storage card addressing logic as appropriate. Provisions are also included to determine if the address furnished by the user device is contained within the memory base.

b. Rotation of read data for correct alignment with the output data lines, and rotation of write data for correct alignment with the appropriate bit positions in memory.

c. Merging read and write data for the purpose of inserting new data in a selected storage area, and masking of read data to prevent unwanted information from being gated to the output.

d. Generation of error-correction code bits for write data and checking of same for read data including correction of errors where appropriate.

NOTE

The error-correcting code employed is capable of correcting single-bit errors in a given data word (16 bits), and detecting multiple-bit errors.

e. Generation of necessary control signals to properly sequence its own operations.

The memory base is physically composed of a 22-card backplane, of which five logic cards contain the control and interface circuits of the base itself. Sixteen of the remaining card positions are reserved for the installation of memory storage cards (which may be added in groups of four), and one position is left as a spare. Since each memory card contains 16,384 (16K) 16-bit words, a card group represents 65,536 (64K) words of storage. A full memory base consists of 262,144 (256K) words, or the equivalent of 524,288 (512K) 8-bit bytes. Operation of the memory base is described in Volume 3 (FETM 1095551) of this manual.

I/O SUBSYSTEM

The B 1870/B 1860 I/O Subsystem is comprised of an I/O base and I/O device controls. Each control serves as an interface between the I/O bus and one (or more) peripheral device(s). The controls are located close to the processor to minimize the length of the I/O bus which, in turn, minimizes propagation time.

I/O Bus

The I/O bus is a 24-bit wide bidirectional bus which is used to carry either data or commands between the I/O subsystem and the processor. This bus is shared by all I/O controls attached to the processor. In conjunction with the 24-bit bus are control lines which define the operation as to phase (command active or response complete) and also as to the presence of data or commands on the bus.

I/O Base

The I/O controls are installed in modules known as the I/O base and I/O base extension(s). These are packaged in a manner similar to the processor logic. Each control is constructed on one or more logic cards; one to eight of these controls may be installed in the I/O base and one to five controls in the I/O base extension. A maximum of 15 I/O controls may be employed within the system (channel 16 is reserved). This would entail the installation of at least one I/O base and three extensions, depending on the number of card positions occupied by the individual controls.

The I/O base and extension(s) each contain a distribution card which interfaces it with the main I/O bus. The primary function of these cards is buffering, with line receivers and drivers, to minimize loading and reflection on the main I/O bus. The I/O base distribution card also processes and distributes the system clock and generates a distributes the slow clocks to its own controls (by way of the backplane) and to the distribution cards of the extensions (by way of coaxial cables).

The I/O bus is connected between the processor and I/O base distribution card by way of a strip cable. From this card, it is further connected to the distribution cards in the base extensions by other strip cables. Refer to the B 1700 I/O Base Technical Manual, form number 1053352, for further information.

I/O Controls

The B 1870/B 1860 I/O Controls are special-purpose controls, and each is unique. The controls, along with the devices with which they interface, are listed in figure 1-34. In most cases, a single control handles a single device. Each control is described in detail in its own I/O technical manual.

I/O Control Name	M&E Top Unit Number	Type	Control Cards	Backplane Sizes (if independent)	Peripheral Devices/Comments
I/O Base Extension 2	2211 1330		1	10	Control card is subdistribution card.
I/O Base Extension 3	2212 8680		1	6	Control card is subdistribution card.
Operator Display Console Control 2	2212 2139	(SPO-2)	1	-	B 9348-31
Card Reader Control 1	2200 5656	80 Column	1	-	B 9115, B 9116, B 9117
Card Reader Control 2	2205 7202	80 Column	1	-	B 9111, B 9112
Card Punch Control 1	1861 6391	80 Column	1	-	B 9212, B 9213
Card Reader/Card Punch Control 1	1862 5228	80 Column	2	-	B 9418-2
Card Read/Punch/Print Control (MFCU-2)	2209 7802	96 Column	2	-	B 9119-1, 2; B 9419-2, -6
Printer Control 4	2205 7244	Chain	1	-	B 9249-1, -2, -3
Printer Control 5	2211 1306	Train	2	-	B 9247-12, -13, -14, -15
Magnetic Tape Control 3	2212 2154	NRZ	2	-	B 9491-2, B 9495-2; B 9496-2, -4
Magnetic Tape Control 5	2212 8920	PE	2	-	B 9495-2; B 9496-2, -4
Magnetic Tape Cassette Control 1	2208 2838	NRZ	2	-	B 9490-25
Disk Cartridge Control 3	2212 8805	32/64 Sector	3	-	B 9480-12, B 9481-12, B 9482-32
Disk Pack Control 2	2212 8912	–	2	-	B 9499-7, -8, -25, -55 (MEC/One Drive); B 9486-4, -5 (Drives)
Industry Compatible Mini-Disk Control 1	2212 8896	(Flexible Disk)	2	-	B 9489-16, -17,
Disk File Control (B 1870 Systems only)	2212 0234	(5N Subsystem)	4	4	B 9470-2
Reader/Sorter Control 2	2205 7251	MICR/OCR	2	-	B 9134-1; B 9135-2, -3; B 9137-1
Single-Line Control 1	2200 5771		2*	4	Any line adapter and optionally on Auto Call Adapter.
Dual-Line Control Base	2212 8995	–	0**	6	Any line adapter except Auto Call for each set of control cards.
Multi-Line Control 1	2200 9765	–	4*	12	Any combination of one to eight line adapters.
Multi-Line Extension 1	2201 2314	–	1*	10	Any combination of one to eight line adapters.
96 Column Read/Punch/Print	–	300/60/60/CPM	2	-	B 9319-2

* Does not include the line adapter(s).

** Each set (two control cards) must be ordered separately: Single-Line Control-2 M & E (top unit) number 2212 8979.

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Figure 1-34. B 1820 I/O Devices and Controls

SYSTEM CLOCK

The system clock is used to provide synchronization of all logic activity within the processor. The raw clock signal is generated by a (quartz) crystal-controlled oscillator operating at a frequency of 6 MHz. Following the oscillator are shaping circuits (to produce an approximate square wave) and several delay lines. From the delay line taps are derived several signals which are buffered, then distributed to the system logic by way of coaxial cables and a backplane wiring. The timing relationship between the various clock module outputs is illustrated in figure 1-35.

POWER

Power for the B 1870/B 1860 Central System is supplied by a minimum of one and a maximum of four power supplies, all of which are contained within the central system cabinet. The main power source for the system logic is the logic power supply. One such logic supply is always present in single-bay cabinet configurations, with two being employed (in master/slave operation) in large installations where a two-bay cabinet is necessary. Also available are booster supplies which are added as necessary to tailor the current delivery capacity to the system requirements (in most single-bay installations the current demand exceeds the capacity of the logic power supply). Significant changes from previous practice include the elimination of memory power supplies (the memory now operates from the standard logic voltages), and reversal of the two 12-volt logic supply outputs for increased current on the +12-volt side. Figure 1-36 illustrates the physical locations of the supplies within the central system cabinet.

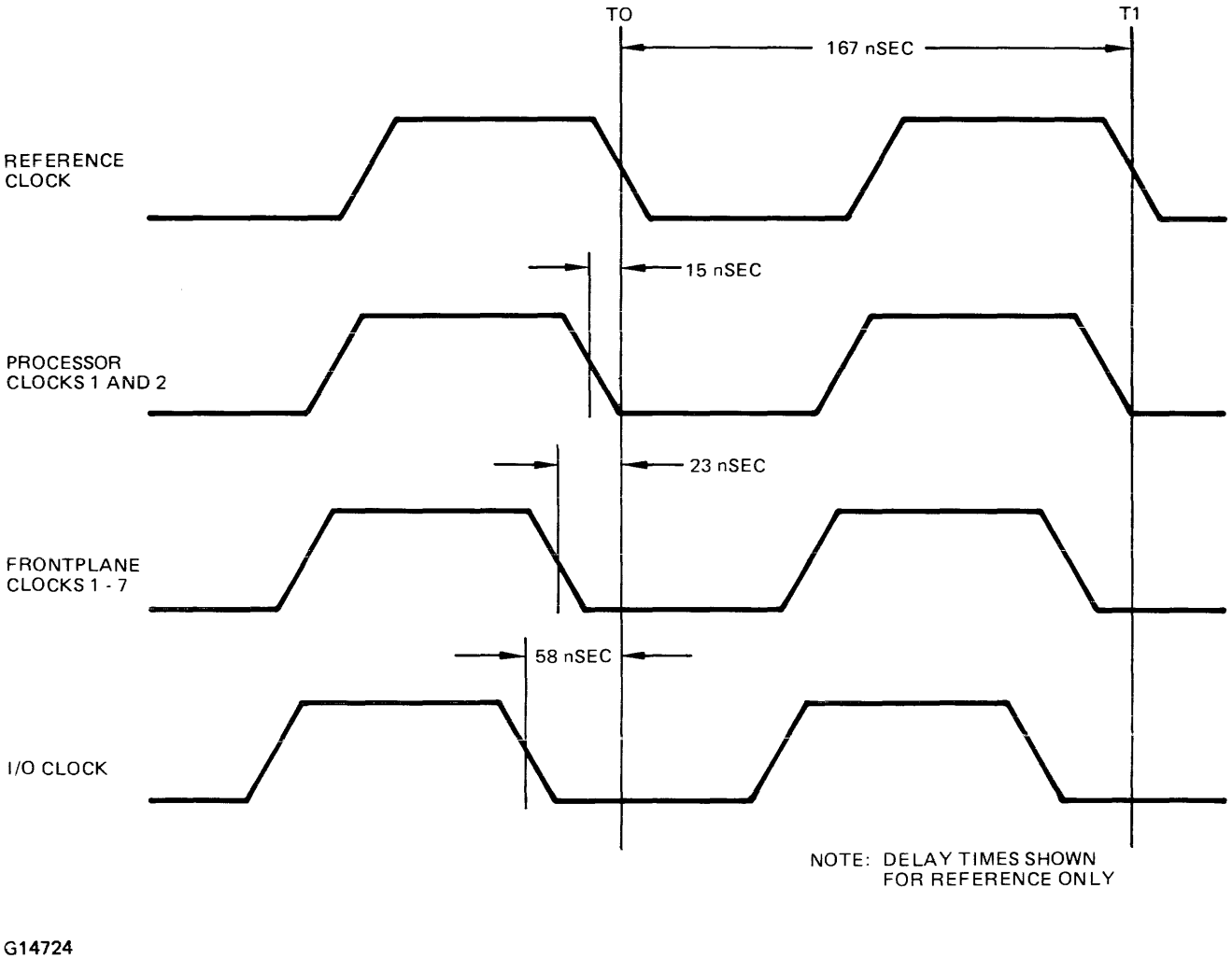


Figure 1-35. B 1870/B 1870 Clock Timing

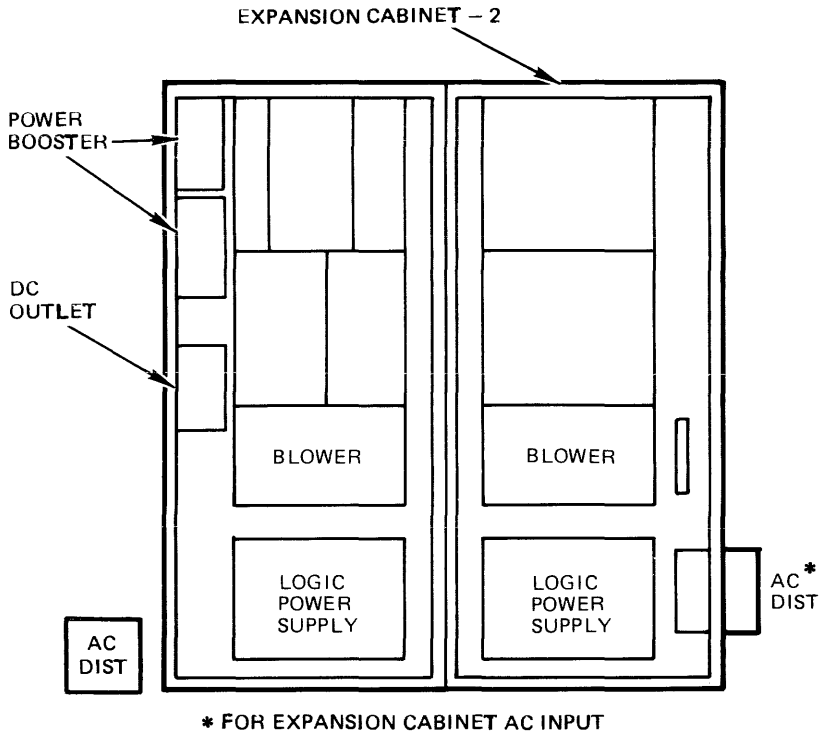


Figure 1-36. B 1870/B 1860 Central System Power Subassemblies

Power Distribution

The B 1870/B 1860 Central System is intended to operate from single phase, 188 to 253 volts, 50/60 Hz, ac power. However, use of the system with other supply voltages in a three-phase configuration is also possible. Refer to section 6 of this volume for further details. AC power is distributed within the central system as illustrated in figure 1-37. Note that power for several peripheral devices is provided through the central system ac control.

Logic Power Supply

The logic power supplies convert the ac input power to four output voltages used throughout the central system to operate the logic, the S-memory, and line drivers and receivers. The four output voltages and current levels are defined as follows:

a. +4.75 Volts; Used as the Vcc (collector voltage) of CTL logic, with a nominal output current of 200 amperes.

b. –2.0 Volts: Used as the Vee (emitter voltage) of CTL logic, with a nominal output current of 200 amperes.

c. +12.0 Volts: Used mainly as a supply voltage to the memory storage elements and to line drivers, with a nominal output current of 18 amperes.

d. –12.0 Volts: Used mainly as a supply voltage to line drivers and receivers, with a nominal output current of 6 amperes.

The logic power supply is physically constructed in a 19-inch RETMA rack cabinet which may be extended from the central system frame, for ease of access, when being serviced. When extended, the supply may also be rotated upwards 90 degrees for access to the underside. Refer to the B 1870/B 1860/ B 1700 Power Supplies, FETM 1070281, for further details.

Auxiliary Power Supplies

For applications where the current draw of the main central system logic exceeds the capacity of the Logic Power Supply, one or two additional booster supplies are employed to meet the expanded load requirements. The booster supply produces +4.75 Volts and –2.0 Volts at a maximum output current of 80 amperes. (See FETM 1070281.)

BASIC SOFTWARE OVERVIEW

The B 1870/B 1860 System has previously been described as one that conducts its operations through the execution of microinstructions. Because of the vast numbers of micros necessary to compose a workable program, it is usually not practical for programmers to write microprograms. Therefore, various higher level languages (from which microprograms are generated) have been developed for use with the system. It is beyond the scope of this manual to describe these higher level languages, but a

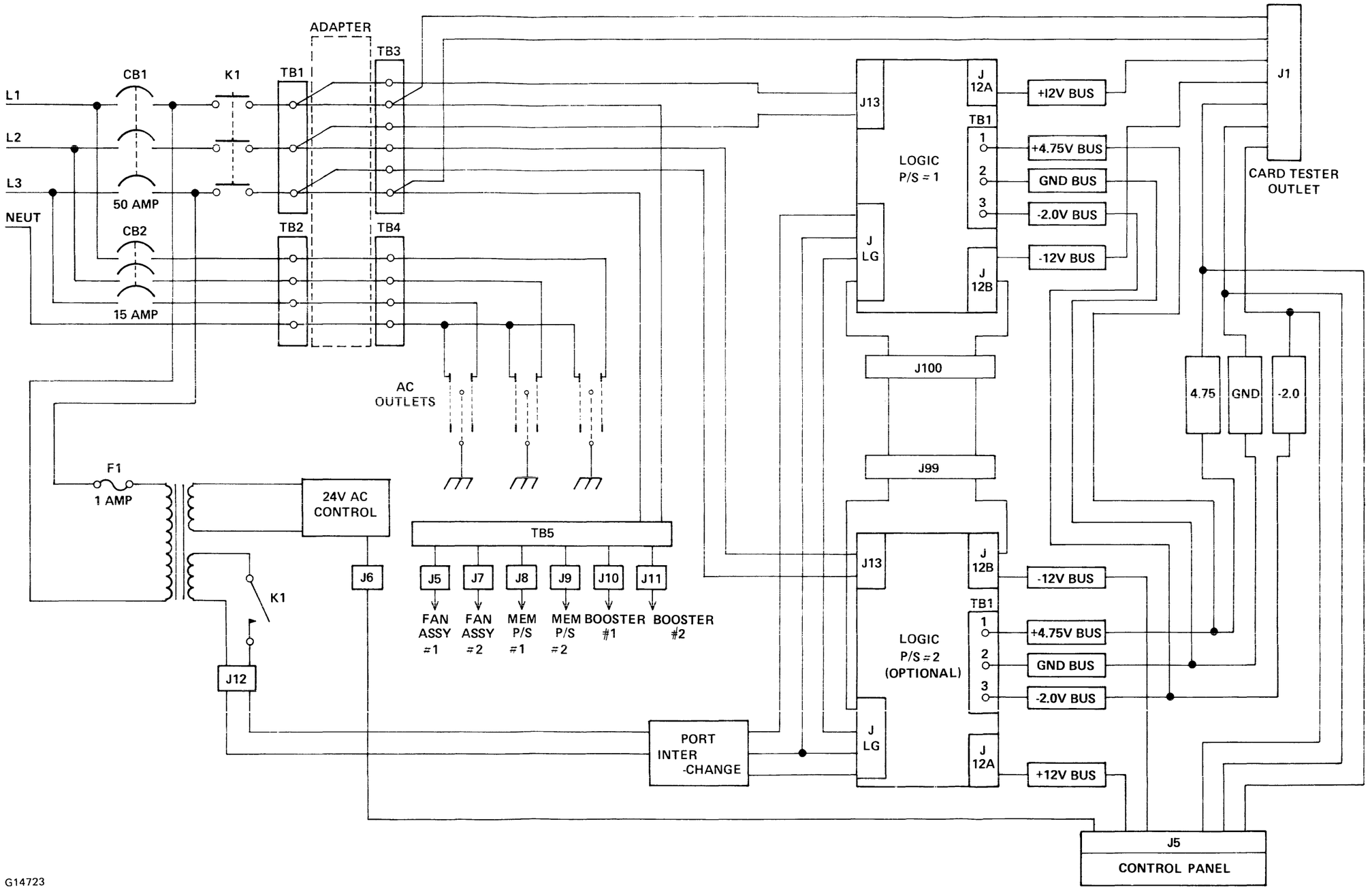


Figure 1-37. B 1870/B 1860 Power Distribution

discussion of the relationship that exists beteen the microprogram and the higher level languages is provided.

Programming Languages

To enable the programmer to develop programs suited to specific categories of data processing applications, procedure-oriented languages and problem-oriented languages are used. These are high level languages which allow the programmer to express the job requirements in a form easily convertible to operations that may be performed by a computer. COBOL (Common Business Oriented Language), FORTRAN (Formula Translator) and SDL (Software Development Language) are some of the standard high level procedure-oriented languages. RPG (Report Program Generator) and NDL (Network Definition Language) are other examples of problem-oriented languages which serve as an interface between actual performance requirements and machine capabilities.

After the program has been written in a procedure-oriented or problem-oriented language, it is compiled (machine translated) into what is known as S-language. This is an intermediate binary-coded language which is used only for handling (encoding and storage) of functional programs. S-language instructions are similar to the machine language instructions used in earlier types of equipment, in that each such instruction describes a complete machine operation (such as an ADD) that requires a string of microinstructions for execution in the B 1870/B 1860.

The S-language program is stored in S-memory, from which it is fetched and executed. It must be remembered that S-instructions are not executed directly, but rather are used to specify strings of microinstructions which cause the desired actions to take place. In addition to specifying a micro string, the S-instruction may also contain variants which affect the execution of that string.

Interpreters

The derivation of micro strings from S-language instructions is not an automatic hardware function, but rather requires the action of another program which is referred to as an interpreter. Essentially, the interpreter consists of a basic micro subroutine for decoding the S-instuctions, plus additional subroutines which execute the actions specified by the S-ops. The program loop in which the interpreter works is shown in figure 1-38, and is common to all interpreters. Interpreters have been developed for each of the high-level S-languages (such as COBOL, FORTRAN and SDL). Figure 1-39 illustrates the manner in which an S-language Add instruction could be executed through use of an interpreter subroutine.

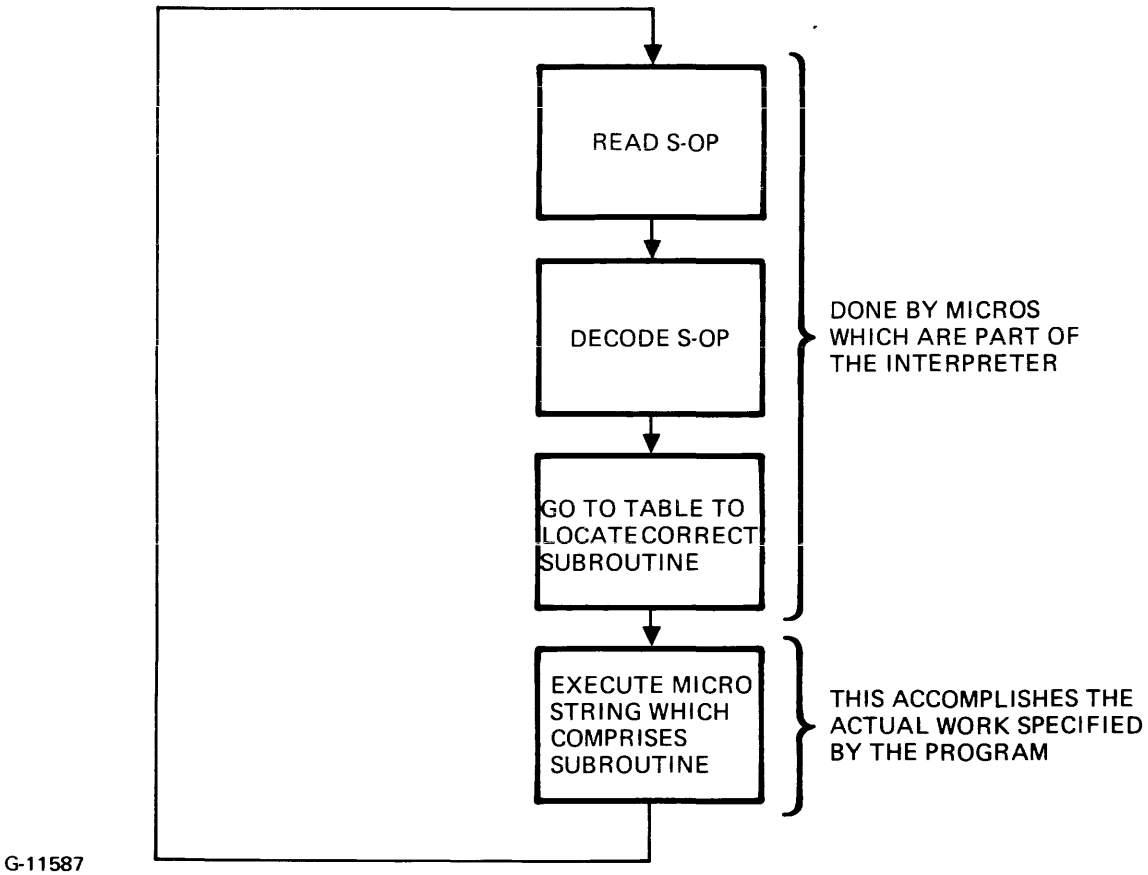


Figure 1-38. S-Language/Interpreter Relationship

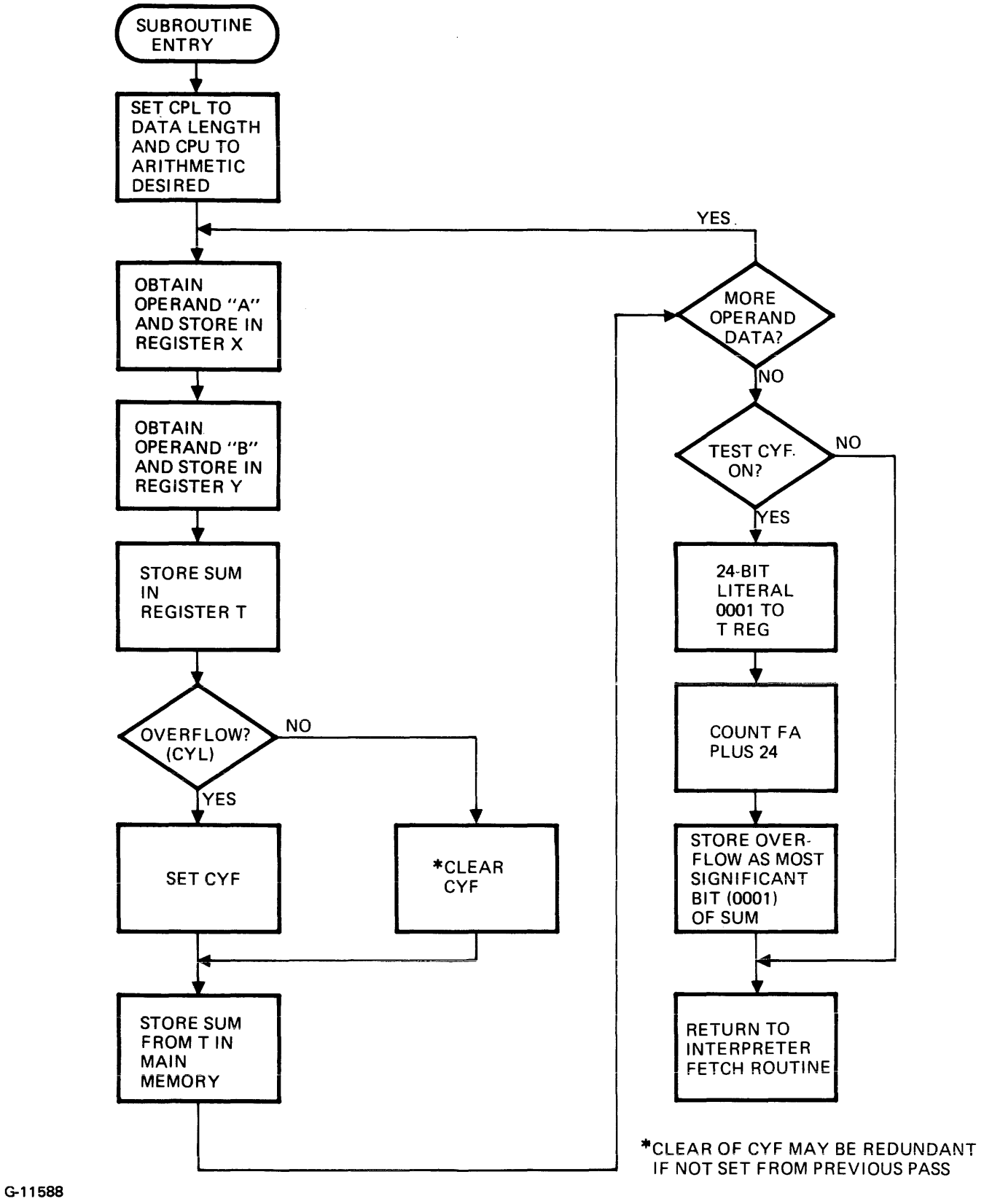


Figure 1-39. Subroutine Flow for 4-Bit BCD Sum (Resulting from S-Language Sum Instruction)

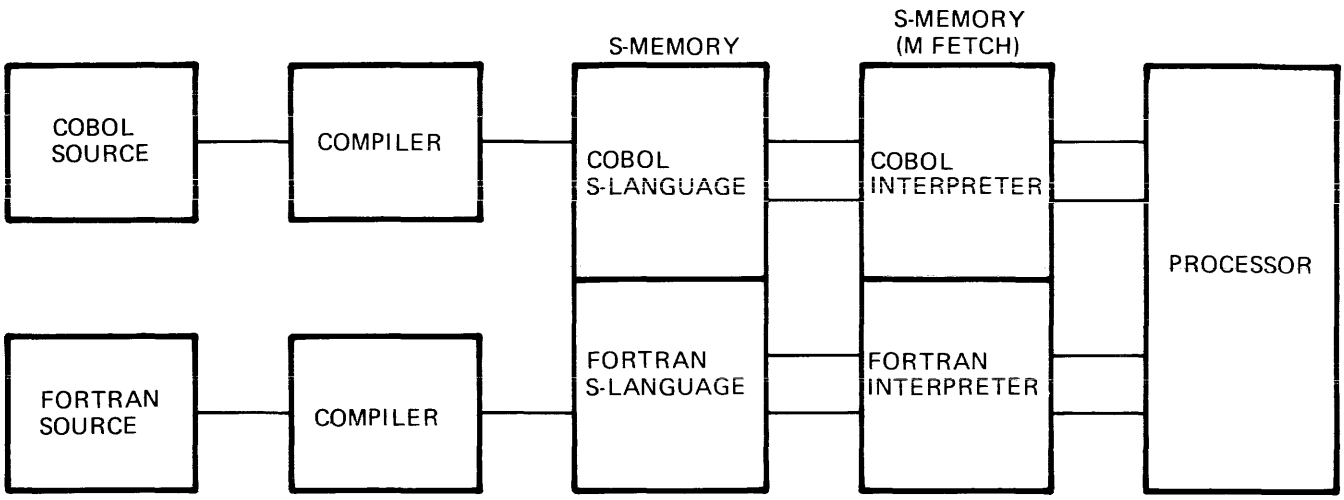


Figure 1-40. Software/Hardware Relationship

Program Storage and Execution

The S-language programs and required interpreters are customarily stored on disk until needed. Location and loading into memory for use is handled under the control of the Master Control Program (MCP). The MCP is a housekeeping program which maintains control over all system acrtivities, acting as an interface between all other operational programs. The MCP is written in SDL, and therefore the SDL interpreter is always present in the system. Figure 1-40 illustrates the relationship between the various stages of software and the hardware micro processor.

CENTRAL SYSTEM OPERATION

The B 1870/B 1860 Central System may be operated in either an on-line or off-line manner. On-line operation implies that control of the system activities has been assumed by a program, with actions proceeding at normal machine speed. In this condition the operator communicates with the system by way of the operator's display console (a video display and entry keyboard which replaces the teletype machine used in earlier systems). Off-line operation, on the other hand, involves manual control by way of the Diagnostic/Maintenance console, usually with the processor halted. Describing on-line operating procedures is beyond the scope of this manual, but such information is fully documented in the applicable software publications. In particular, reference should be made to the B 1800 Systems Software Operational Guide, form number 1068731.

The B 1870/B 1860 system offers, as did its predecessors, a variety of control and access functions which may be employed by the user. These include controls and indicators needed during normal system operations, and other special-purpose controls and indicators which are used primarily for troubleshooting purposes. The operational and maintenance controls have been separated, and are now installed on different control panels. These two panels are known as the Operator's panel and the Diagnostic/Maintenance panel respectively. The functions of the controls provided and the capabilities available to the operator are described in the following subsections.

Console Operations

The console of the B 1870/B 1860 Central System (considering both control panels) represents a physical interface with the micro decoding logic, the operational status control logic, and the main 24-bit exchange. The controls allow the normal on/off, start/stop and operational mode selection functions, and, in addition, include provisions for examining the contents of manually entered data into the various registers and storage elements within the machine. Note that there is some duplication of functions between the two control panels.

Operator's Panel Functions

The operator's console is used primarily for control of system activities in the on-line condition. The functions provided are therefore restricted to actions concerning initiating and terminating operations, selecting operational modes, and controlling the cassette tape drive.

SELECTION OF OPERATIONAL MODE

Selection of the system operational mode is accomplished by way of the MODE pushbutton. This control is a two-position switch which changes state each time it is pressed. A self-contained indicator shows the state selected. The two operational modes may be defined as follows:

NORMAL — System operation is conducted in the customary manner, with fetching and execution of micros from Cache and S-memory proceeding at full machine speed.

MTR — Micros are entered (and executed) from the cassette tape drive, with fetching consisting of moving the contents of the U register (which assembles the cassette output) to M.

NOTE

Machine functions within either of the two modes is dependent on the setting of several switches on the Diagnostic/ Maintenance panel. These include the SINGLE MICRO/CONTINUOUS switch, the CASSETTE SELECT switch and the MICRO SOURCE switch. Refer to the descriptions of these control functions for further information.

CLEARING

The system may be cleared (initialized to the defined clear state) in preparation for operations by pressing the CLEAR button. This is normally done only when the machine is halted. The CLEAR button is duplicated on the Diagnostic/Maintenance panel.

STARTING

The execution of micros is initiated (from the Halt state) by pressing START. The START button has an internal indicator lamp (TEST STATE) which is lit whenever an abnormal run condition exists. The following conditions cause TEST STATE to be lit:

a. The Interrupt bit (CCO) is set.

b. The single micro mode is selected (SINGLE MIC).

c. The MICRO SOURCE selection is other than NORMAL.

NOTE

The latter two conditions are controlled from the Diagnostic/Maintenance panel.

The START button is duplicated on the Diagnostic/Maintenance console.

INTERRUPT

The INTRPT button is used to set the interrupt bit (CCO). The state of this bit is tested by the executing program, with actions following detection of either a true or false condition being determined by the programmer. The usual function provided is to cause the processor to halt at an orderly break off point when the interrupt bit is set. The Interrupt bit may only be set (not reset) by way of the INTERRUPT button. This control is duplicated on the Diagnostic/Maintenance panel (INTERRUPT).

CASSETTE REWIND

Cassette rewind may be effected by pressing the RWD (Rewind) button. This may be done with the processor running or halted. The RWD button has a self-contained indicator lamp (BOT) which signals that the beginning of tape is being sensed. Illumination of BOT indicates that the tape is rewound, and is ready for use or removal.

Diagnostic/Maintenance Panel Operations

The Diagnostic/Maintenance panel, as its name implies, contains controls which are most often used for troubleshooting purposes. Such troubleshooting may be occasioned by either hardware malfunction or by the need to investigate unsatisfactory program results. The functions provided are essentially the same as those of the main console in B 1700 systems, but feature extended capabilities in several respects.

REGISTER SELECTION

Selection of registers for viewing the contents thereof on the console lamps or loading data by way of the control switches is accomplished with the REGISTER GROUP and REGISTER SELECT switches. To select a register, the REGISTER GROUP switch must first be rotated to the position corresponding to the group of six registers in which the desired one is located. When this has been done, the REGISTER SELECT switch is then rotated to the number (0 through 3) indicating the relative position of that register within the group.

The act of selection causes a hardware-forced 1C (Register Move) micro to be executed, with the source being the desired register, and the destination being Null (the console lamps). Viewing and altering the contents of registers is possible only when the processor is halted. Reading and writing in Cache memory, S-memory, and scratchpad memory are accomplished in the same manner as register access. Specific procedures for accessing registers and for reading and writing in memory are described in the following subsections.

USING THE CONSOLE LAMPS AND CONSOLE SWITCHES

The console lamps are provided to monitor the contents of the main exchange. As such they serve as both a visual indication of processor operation (when it is running), and allow the contents of any register or memory location to be examined when the processor is halted. The 24 console switches allow manual selection of a 24-bit data field configuration which can then be moved to any selected data storage location register, S-memory, or Cache memory.

The significance of the various bit positions depends on the unit addressed. All registers are right-justified when displayed individually, and will occupy the appropriate number of bit positions. Memory Read/Write data, on the other hand, may occupy any of several positions, depending on the memory access mode selected. In all cases, however, each individual console switch corresponds to the console lamp directly above it, and will, when raised, cause

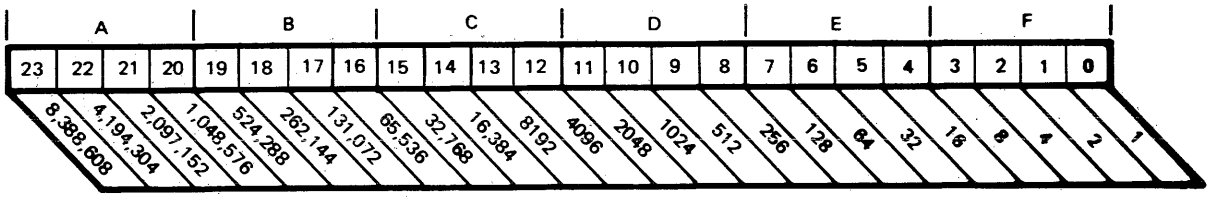


Figure 1-41. Console Switch/Lamp Binary Weights

a 1-bit to be set in that position. Note, however, that 1-bits thus selected are not gated to the designated register or memory location until this is specifically effected by initiating a load or write cycle. The binary weight of each of the 24 console switch/lamp positions is shown in figure 1-41. These binary weights are valid only as regards the 24-bit field taken as a whole. Quite often, smaller fields within the 24 bits are assigned individual meanings with accompanying (smaller) binary weights. Refer to the register and micro descriptions for detail on these specialized meanings.

READING THE CONTENTS OF A REGISTER

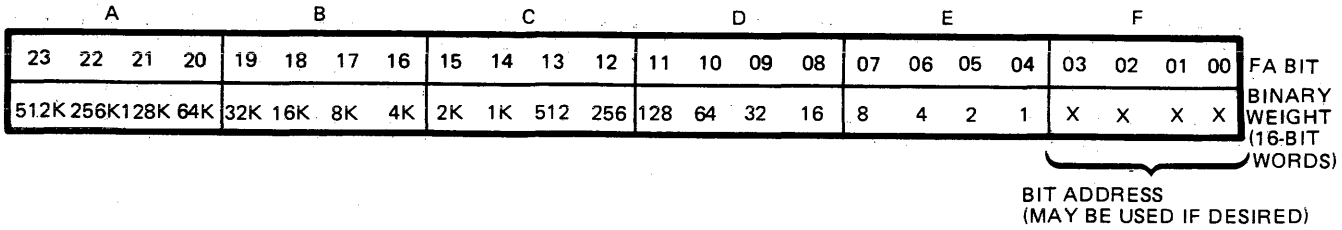
To read a register's contents, simply select the desired register by way of the REGISTER GROUP and REGISTER SELECT switches (with the processor halted.) The act of selection causes a hardware-forced 1C register move micro to be executed, moving the contents of the selected register to the main exchange, and then be latched into the console lamp register. The contents of this register are continuously displayed when the processor is halted. Refer to the register descriptions for the specific meaning of individual register contents.

LOADING A REGISTER

To load a register, the selection procedure described in Reading the Contents of a Register (above) must first be performed. When this has been done, the desired bit pattern should be selected on the console switches. Pressing the LOAD pushbutton causes a hardware-forced 1C (Register Move) micro to be executed, gating the contents of the switches to the register. Note that the entire contents of the register are affected by the loading process. If it is desired to save any portion, these bits must be re-inserted by use of the console switches.

READING IN S-MEMORY

To read, or cause the data stored at a specific location in S-memory to be displayed on the console lamps, the bit address desired must first be loaded into the FA (Field Address) register. The binary weight of this code is illustrated in figure 1-42. Following loading the address, MEMORY MODE is selected on the REGISTER SELECT switch, and the desired memory read mode is selected on the REGISTER GROUP switch. It is important to note at this point that there are three S-memory read options which may be exercised. These options are as follows (refer to figure 1-43):



NOTES: 1. FA ADDRESSES ABOVE 512 ARE AS FOLLOWS:
- 1K = 1024
- 2K = 2048
- 4K = 4096
- 8K = 8192
- 16K = 16,384
- 32K = 32,768
- 64K = 65,536
- 128K = 131,072
- 256K = 262,144
- 512K = 524,288

2. BIT ADDRESS (IF ANY) IS IGNORED ON 22-BIT READ/WRITE OPERATIONS

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Figure 1-42. S-Memory Addressing

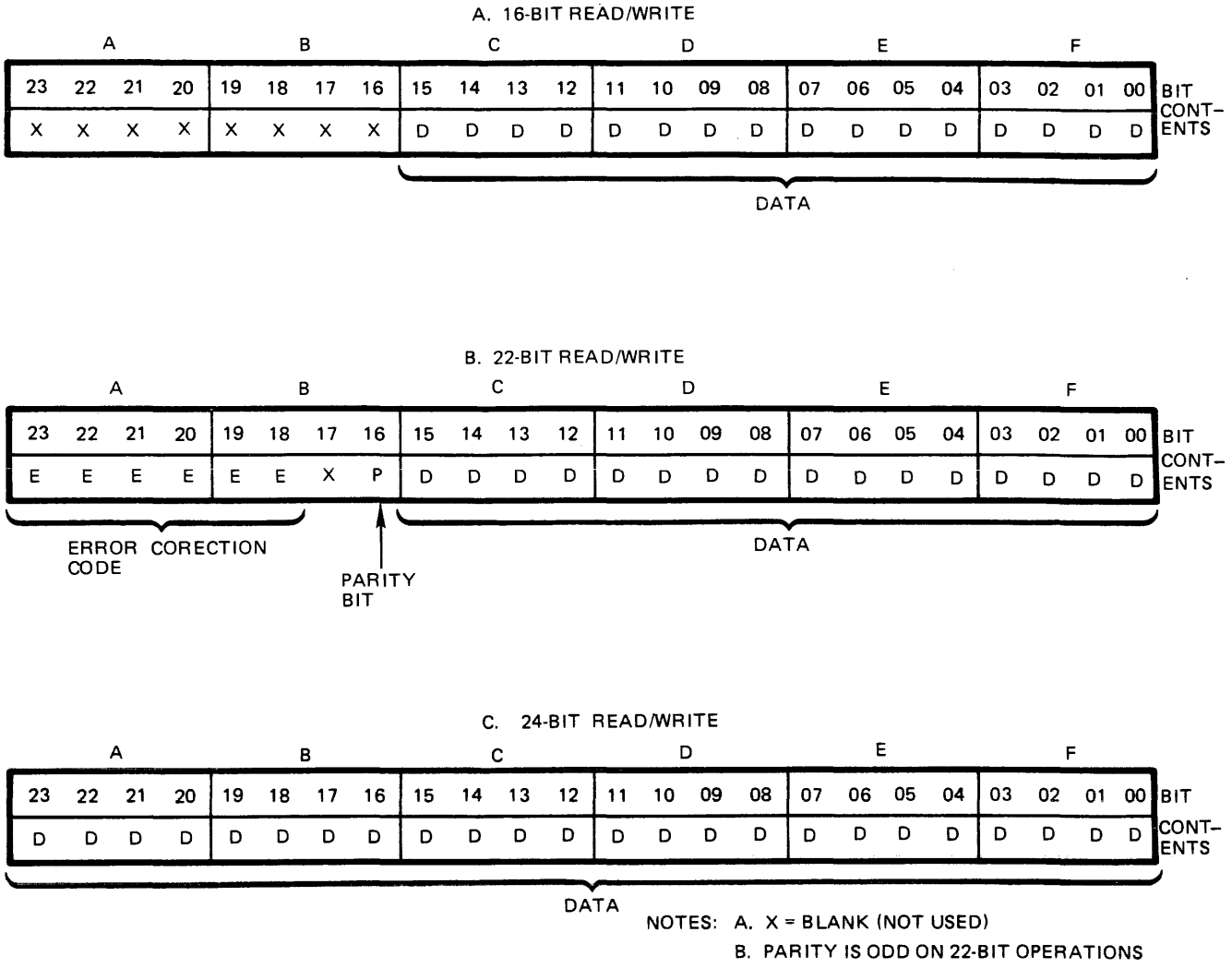


Figure 1-43. S-Memory Read/Write Variants

a. Read 16 bits: Read 16 bits of stored data, beginning at any desired bit location in memory. The data is right justified on the console lamps.

b. Read 22 bits: Read 16 bits of stored data, beginning at any even 16-bit boundary in memory, plus the corresponding six syndrome (error corrrection code) bits. The data is right justified, with the error-correction code bits and parity bit on the left. Refer to figure 1-43. For 22-bit reads, the contents of the least-significant four bits of FA are ignored (forcing the use of 16-bit boundaries).

NOTE

Refer to volume 3, Theory of Operation, form number 1095551, for information on the error correction code.

c. Read 24 bits: Read 24 bits of stored data, beginning at any desired bit location in memory. The data occupies all 24 console lamps.

After selecting the desired memory read mode, the read operation is initiated by pressing the LOAD button. After the read, pressing INC (Increment) causes the address in FA to be incremented by an amount appropriate to the read mode selected. FA is incremented by binary 16 (for 16-and 22-bit reads), and by binary 24 (for 24-bit reads). Note that the 16-bit increment for 22-bit reads is correct, since only 16 data bits are involved (the error correction bit storage is invisible to the addressing logic).

Note that performing a read does not destroy the data stored at the addressed location. The address being accessed may be monitored by selecting FA on the register selection switches. However, once the switches have been moved, it is necessary to again press LOAD when returning to the S-memory read mode.

WRITING IN S-MEMORY

To write (that is to cause the bit configuration selected on the console switches to be gated to S-memory), the desired address must first be loaded into the FA register. This procedure is identical to that performed before a memory read. Once the ad-

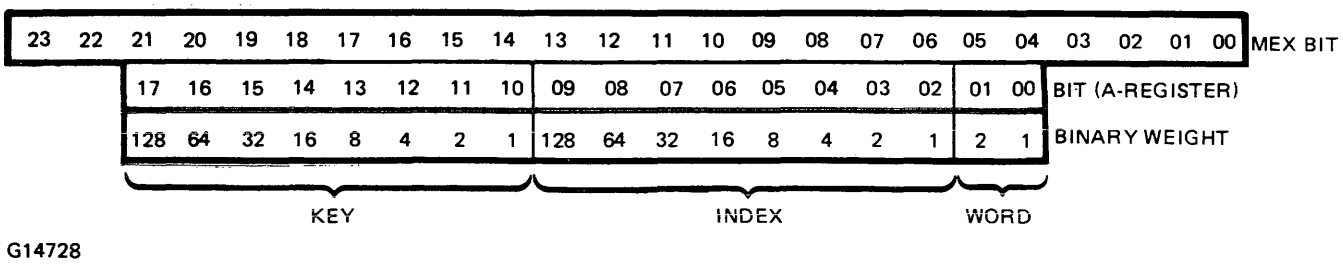


Figure 1-44. Cache Addressing (A-Register Values)

dress has been entered, MEMORY MODE is selected on the REGISTER SELECT switch, and the desired memory write mode is selected on the REGISTER GROUP switch.

The memory write mode variants are similar to the memory read operations, with 16-, 22-and 24-bit field lengths possible. The operations (see figure 1-43) may be defined as follows:

a. Write 16 bits: Move 16 bits of data from the console switches to a specified location in memory, overlaying the data previously stored there. The selected data field may begin at any desired bit location in memory. The data is right justified on the console switches as shown in figure 1-43.

b. Write 22 bits: Move 16 bits of write data plus six error correction bits from the console switches to a specified word address (within even 16-bit boundaries) in memory. The error correction bits are stored in memory elements reserved for this purpose (and correspond directly to the associated data storage locations) which are essentially invisible to the addressing logic. Note that a parity bit is not used, this being a function of 22-bit memory read operations only.

NOTE

It is not practical to create the proper error-correcting code (for a given data field) by manual means. Therefore, use of the 22-bit write operation is limited to verifying proper functioning of the ECC storage locations.

c. Write 24 bits: Move 24 bits of data from the console switches to a specified location in memory, overlaying the data previously stored there. The selected data field may begin at any desired bit location in memory. The data occupies all 24 console switch locations.

As with the S-memory read operation, a memory write is initiated by pressing the LOAD button. Pressing INC (Increment) after the write causes the address in the FA register to be incremented by a value appropriate to the write mode selected. This value is equal to binary 16 (for 16-and 22-bit writes), or binary 24 (for 24-bit writes).

Note that console write operations are fixed-field length functions. Therefore, if it is desired to replace only a portion of a given 16-or 24-bit field with new data, the existing data which is to be saved must be rewritten by manipulation of the appropriate data selection switches (just as if the entire data field were new).

READING IN CACHE

To read, or cause the data stored at a specific location in Cache Memory to be displayed on the console lamps, the Cache address desired must first be loaded into the A (address) register. The binary weight of this code is illustrated in figure 1-44. Following loading the address, MEMORY MODE is selected on the REGISTER SELECT switch, and CMR (Cache Memory Read) is selected on the REGISTER GROUP switch. The read operation is initiated by pressing LOAD. For the operation to be a success, there must be a HIT (match of a stored micro key with the key portion of the A register) and a good validity bit. If there is no associative match (MISS), then all zeros will be returned to the console lamps. The read data format is illustrated in figure 1-45.

Parity is not checked on the Cache read data, since the data bypasses the M register. However, a parity check is performed on both keys A and B. Also, performing the read operation causes the LRU (least recently used) bit to be inverted, indicating the block which was not selected.

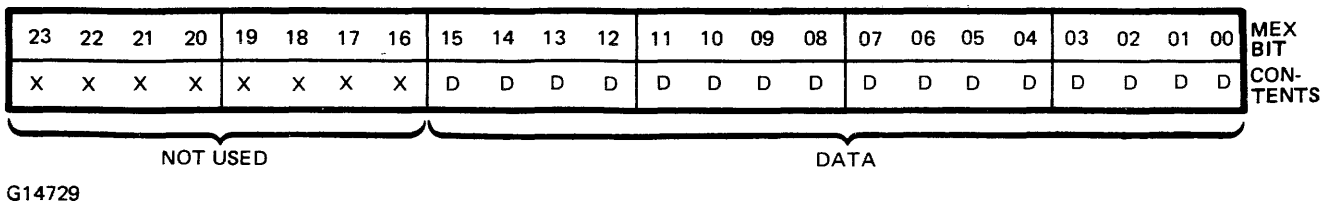


Figure 1-45. Cache Micro Read/Write Data Format

The A register is not automatically incremented by the read operation. Incrementing A by binary 16 (1 in bit position 4) may be effected by pressing the INC (increment) button on the D/M panel. A read at the new address may then be performed by again pressing LOAD.

NOTE

It is not possible to determine which block (A or B) was accessed without performing a Cache Key Read using the same address. The procedure for doing a Cache Key Read is described below.

Also provided as an option in Cache read operations is the ability to view the contents of the Cache key storage. To perform a Cache key read, the index portion of A (bits 06-13) must first be loaded with the desired index address. (The other bits of A may also contain address bits at this time, but these are not used except to provide a Hit/Miss indication.) Following loading the index address, MEMORY MODE is selected on the REGISTER SELECT switch and CKR (Cache Key Read) is selected on the REGISTER GROUP switch. The read operation is initiated by pressing LOAD. The data format presented on the console lamps is illustrated in figure 1-46. This is a non-associative read, so data is always returned. However, a Hit/Miss indication is provided for both keys, which signals that a match has or has not been made with the key portion of A. This indication is of significance only if an address was placed in the key portion of A prior to the operation.

Reading the Cache key contents does not change the stored addresses or other existing conditions (LRU, validity bits, and parity bits). Parity checks are made on both key fields displayed. If a parity error is detected, it will be reported by setting PERP2 and CD3 and illuminating the PARITY lamp on the D/M panel.

NOTE

The parity bits displayed on the console lamps (along with the keys and other data) do not indicate parity errors directly, but rather represent the parity information stored along with the adjoining keys.

WRITING IN CACHE

To write in Cache, the Cache address desired must first be loaded into the A (address) register. This procedure is the same as for reading from Cache, and is illustrated in figure 1-44. Following loading the address, MEMORY MODE is selected on the REGISTER SELECT switch and CAW (Cache Write Block A) or CBW (Cache Write Block B) is selected on the REGISTER GROUP switch. The desired data is then set on the console switches, using the 16 least-significant bit positions as shown in figure 1-45. For proper parity to be written bit 16 must also be set to reflect an ODD sum of the 16 data bits plus the parity bit itself. (Parity is not automatically generated on console Cache write operations.) The write operation is then initiated by pressing LOAD.

The A register is not automatically incremented by the write operation, but may be incremented by pressing the INC button. Also, the write operation overrides the LRU logic, writing into the specified block.

NOTE

Writing into the Cache key storage elements is not possible from the console.

CASSETTE OPERATION

Primary control of the cassette tape drive is maintained by way of the operator's panel. However, selection of the cassette operating mode is performed by way of the CASSETTE SELECT switch on the D/M panel. The two possible modes are described as follows:

SYSTEM: The cassette tape drive serves the sole purpose of entering microprograms and data into the processor by way of the U register. Control of the cassette is maintained by the console controls and the processor cassette logic.

I/O: The cassette tape drive serves as a read and write device for the storage and entry of data, interfacing with the processor by way of the I/O system. Control of cassette operations in the I/O mode is maintained by an optional cassette I/O control, which must be present in the I/O base for this purpose.

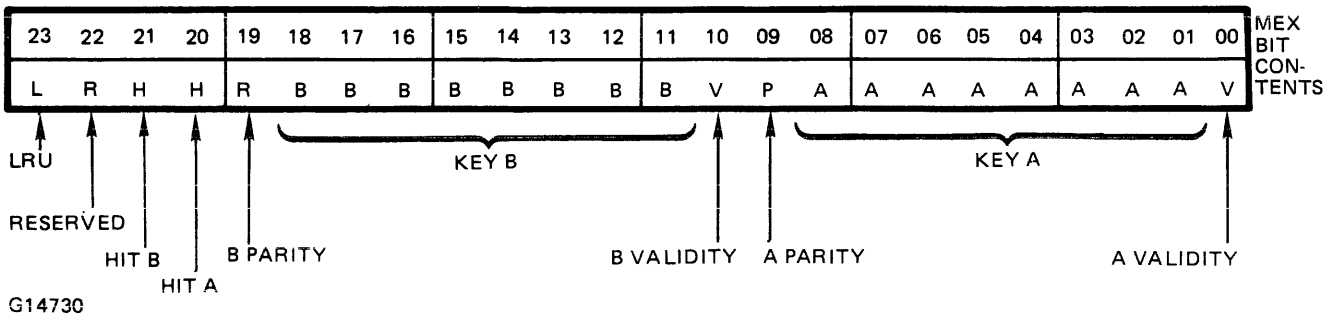


Figure 1-46. Cache Key Read Data Format

Microinstructions

The B 1870/B 1860 processor is capable of executing 39 different microinstructions, an increase of six micros over the B 1720 series instruction set. Each microinstruction causes a specific hardware activity to occur, such as "move the contents of register A to register B." The micros implemented were chosen to satisfy both hardware and software design concepts of the system. While the B 1870/B 1860 instructions set comprises only 39 micro types, many individual micros have a number of variant options which may be selected. Exercising variant options extends the useful range of the instruction set to include many hundreds of separate and distinct functions. The micros and their functions are listed in figure 1-47.

As a system design convention, microinstructions are defined as consisting of a 16-bit binary field. Each micro is named in accordance with the binary weight in its most significant 4-bit subfield (characteristic) which contains some value other than 0. The subfields are identified in the same manner as the 4-bit subregisters in the processor (suffix A,B,C,D,E, or F). Therefore, the micro which has a binary weight of 1 in the C subfield is known as the 1C micro. A micro having a value of 0 in the C subfield and 4 in the D subfield is known as the 4D, etc. The A and B subfield designations are not used, since micros always occupy the 16 least-significant bits of any medium in which they are stored (exclusive of memory). Variants and literal data within microinstructions are always contained in those bit positions to the right of the characteristic subfield. Refer to the individual microinstruction descriptions which follow.

	MICRO NAME	MC 15	14	13	12	MD 11	10	9	8	ME 7	6	5	4	MF 3	2	1	0	VARIANTS	0 00 000	1 01 001	10 010	11 011	100	101	110	111
1C	REGISTER MOVE	0	0	0	1	REG 1 GROUP SOURCE REGISTER				REG 1 SELECT		REG 2 SELECT		REG 2 GROUP SINK REGISTER												
2C	SCRATCHPAD MOVE	0	0	1	0	REGISTER GROUP SOURCE OR SINK				REG SELECT		MOV DIR	DPW 1/2	DOUBLE PAD WORD ADDRESS				MOV DIR:	P ←R LEFT	R ←P RIGHT						
																		1/2 DPW:								
3C	4-BIT MANIPULATE	0	0	1	1	REGISTER GROUP 4-BIT SOR & SNK				REG SEL	MANIPULATE VARIANTS			4-BIT MANIP LITERAL				MANIP VARIANTS	SET	AND	OR	EOR	INC	INC TEST	DEC	DEC TEST
4C	BIT TEST REL BRANCH FALSE	0	1	0	0	REGISTER GROUP 4-BIT SOURCE				REG SEL	TEST BIT NUMBER		DSP SGN	RELATIVE BRANCH DISPLACEMENT MAG				DSP SIGN:	+	-						
5C	BIT TEST REL BRANCH TRUE	0	1	0	1	REGISTER GROUP 4-BIT SOURCE				REG SEL	TEST BIT NUMBER		DSP SGN	RELATIVE BRANCH DISPLACEMENT MAG				DSP SIGN:	+	-						
6C	SKIP WHEN	0	1	1	0	REGISTER GROUP 4-BIT SOR & SNK				REG SEL	SKIP TEST VARIANTS			4-BIT TEST MASK				SKIP TEST VARIANTS	ANY CLR/	ALL CLR/	EOL CLR/	ALL CLR	ANY/ CLR/	ALL/ CLR/	EOL/ CLR/	ALL/ CLR
7C	READ/WRITE MEMORY	0	1	1	1	R/W VAR	COUNT FA/FL VARIANTS			DATA REG CODE		DSP SIGN		DATA TRANSFER WIDTH MAGNITUDE				READ/WRITE: DISPLACEMENT SIGN:	R LEFT	W RIGHT						
																		REG. CODE:	X	Y	T	L				
																		COUNT FA/FL:	NOP	FA↑	FL↑	FA↑ FL↓	FA↓ FL↑	FA↓	FL↓	FA↓ FL↓
8C	MOVE 8-BIT LITERAL	1	0	0	0	REGISTER GROUP REG SEL IS 2				ENTIRE 8 BITS OF 8-BIT LITERAL																
9C	MOVE 24-BIT LITERAL	1	0	0	1	REGISTER GROUP REG SEL IS 2				8 MOST SIGNIFICANT BITS OF FULL 24-BIT LITERAL																
10C	SHIFT/ROTATE T-REG	1	0	1	0	SINK REGISTER GROUP				SNK REG SELECT		S/R VAR		LEFT SHIFT/ROTATE & COUNT				S/R VAR:	SHFT	ROT						
11C	EXTRACT FROM T-REG	1	0	1	1	RIGHT BIT POINTER FOR EXTRACTION FLD				SINK REG CODE				EXTRACTION FIELD WIDTH				SINK REG CODE:	X	Y	T	L				
12C	BRANCH RELATIVE FORWARD	1	1	0	0	RELATIVE DISPLACEMENT MAGNITUDE																				
13C	BRANCH RELATIVE REVERSE	1	1	0	1	RELATIVE DISPLACEMENT MAGNITUDE																				
14C	CALL RELATIVE FORWARD	1	1	1	0	RELATIVE CALL ADDRESS MAGNITUDE																				
15C	CALL RELATIVE REVERSE	1	1	1	1	RELATIVE CALL ADDRESS MAGNITUDE																				
2D	SWAP MEMORY	0	0	0	0	0	0	1	0	DATA REG CODE		TW SGN		DATA TRANSFER WIDTH MAGNITUDE				TW SIGN: REG CODE:	+ X	- Y	T	L				
3D	CLEAR REGISTERS	0	0	0	0	0	0	1	1	L-REG	T-REG	Y-REG	X-REG	FA REG	FL REG	FU REG	CP REG									
4D	SHIFT/ROTATE X OR Y	0	0	0	0	0	1	0	0	S/R DIR VARIANT		X/Y VAR		LEFT OR RIGHT X OR Y SHIFT/ROTATE COUNT				X/Y VAR:	X	Y						
5D	SHIFT/ROTATE X AND Y	0	0	0	0	0	1	0	1	S/R DIR VARIANT		LEFT OR RIGHT, X AND Y SHIFT/ROTATE COUNT						S/R DIR VARIANTS	SFT←	4D AND 5D SFT→	ROT←	ROT→				

G14731/SHEET 1 OF 3

Figure 1-47. B 1860 System Micro Chart (Sheet 1 of 3)

	MICRO NAME	MC 15	14	13	12	MD 11	10	9	8	ME 7	6	5	4	MF 3	2	1	0
6D	COUNT FA/FL	0	0	0	0	0	1	1	0	COUNT FA/FL VARIANTS				COUNT SCALAR MAGNITUDE			
7D	EXCHANGE DPW	0	0	0	0	0	1	1	1	SINK DPW ADDRESS				SOURCE DPW ADDRESS			
8D	SCRATCHPAD RELATE FA	0	0	0	0	1	0	0	0	0	0	0	SPD SGN	LEFT HALF PAD WORD ADDRESS			
9D	MONITOR	0	0	0	0	1	0	0	1	LITERAL OCCURRENCE IDENTIFIER							
10D	NANO MOVE	0	0	0	0	1	0	1	0	C/A VAR	STOPPING SEQUENCE NUMBER				NANO REGISTER WORD PORTION		
11D	DIAGNOSTIC READ/WRITE MEMORY	0	0	0	0	1	0	1	1	SOURCE REGISTER		FDS OR P.I. R/E	MBU/ P.I.	MEM/ ECHO	MEM R/W	ECHO VAR	
										X	X	0	0	0	0	0	0
										r	r	0	0	0	1	0	0
										r	r	0	0	1	0	0	1
										X	X	0	0	1	0	1	0
										X	X	1	0	1	0	1	0
										X	X	0	0	1	0	1	1
										X	X	0	1	1	0	0	0
										r	r	1	1	1	0	0	0
										r	r	1	1	1	0	0	1
										r	r	1	1	1	0	1	0
										r	r	1	1	1	0	1	1
										r	r						
										X	X						

VARIANTS	0 00 000	1 01 001	10 010	11 011	100	101	110	111
COUNT FA/ FL VAR:	NOP	FA↑	FL↑	FA↑ FL↓	FA↓ FL↑	FA↓	FL↓	FA↓ FL↓
SPAD SIGN:	+	-						
CONTINUE/ABORT:	C	A						
STOPPING SEQ. NUMBER:	0/8	1/9	2/10	3/11	4/12	5/13	6/14	7/15
WORD PORTION:	0	1	2	3	4	5	6	7
SIGNIFICANCE	(ALL OTHER BIT PATTERNS ARE UNDEFINED)							
READ 22-BIT WORD (16 DATA + 6 ECC) TO Y.								
WRITE 22-BIT WORD FROM X, Y, T, OR L.								
ECHO WRITE DATA TO Y FROM X, Y, T, OR L.								
ECHO WRITE DATA TO Y FROM X, Y, T, OR L.								
ECHO MODIFIED ADDRESS FORWARD, FA TO Y.								
ECHO MODIFIED ADDRESS BACKWARD, FA TO Y.								
READ AND CLEAR ERROR LOG (READ TO Y).								
READ PORT DATA LATCH TO Y.								
ECHO THRU P.I. TO Y FROM X, Y, T, OR L.								
ECHO THRU P.A. 1 TO Y FROM X, Y, T OR L.								
ECHO THRU P.A. 2 TO Y FROM X, Y, T, OR L.								
ECHO THRU P.A. 3 TO Y FROM X, Y, T, OR L.								
SOURCE REGISTER: X Y T L								
IGNORE								

G14731/SHEET 2 OF 3

Figure 1-47. B 1860 System Micro Chart (Sheet 2 of 3)

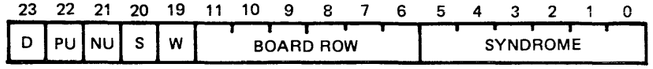
	MICRO NAME	MC 15	14	13	12	MD 11	10	9	8	ME 7	6	5	4	MF 3	2	1	0
1E	DISPATCH	0	0	0	0	0	0	0	0	0	0	0	1	DISPATCH VARIANTS			SKP FLG
2E	CASSETTE CONTROL	0	0	0	0	0	0	0	0	0	0	1	0	CASSETTE MANIP. VARIANTS			HLT=0 SKP=1
3E	BIAS	0	0	0	0	0	0	0	0	0	0	1	1	BIAS VARIANTS			TEST FLAG
4E	STORE F INTO DPW	0	0	0	0	0	0	0	0	0	1	0	0	SINK DPW ADDRESS			
5E	LOAD F FROM DPW	0	0	0	0	0	0	0	0	0	1	0	1	SOURCE DPW ADDRESS			
6E	CARY FF MANIPULATE	0	0	0	0	0	0	0	0	0	1	1	0	CYF ← CYD	CYF ← CYL	CYF ← 1	CYF ← 0
7E	READ/WRITE CACHE	0	0	0	0	0	0	0	0	0	1	1	1	PAR-ITY	READ/WRITE VARIANTS		
1F	HALT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
3F	NORMALIZE X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4F	BIND	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
5F	CLEAR CACHE	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
6F	INC A	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
7F	LOAD LAMPS	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
ZERO	NO OPERATION	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VARIANTS	0 000	1 001	10 010	11 011	100	101	110	111
SKP FLAG: DISP VAR:	FAIL LOCK	SUCC WRTLC	READ	R&C	WRTHI	ABSNT	UNDEF	UNDEF
CASSETTE MANIPULATE:	START TAPE	STOP AT GAP	STOP OR SKIP ON X ≠ Y	STOP OR SKIP ON FA≠BR	UNDEF	UNDEF	STOP OR SKIP ON X = Y	STOP OR SKIP ON FA≠BR
TEST FLAG: BIAS:	TEST/ UNIT	TEST F	S	FS	NO-OP	FCP	NO-OP	NO-OP
PARITY: READ/WRITE:	GOOD R	BAD E S E	R V E	D	DIAG BLKA	WRITE BLKB	READ MICRO	READ KEYS

PERP	CACHE DOUBLE HIT	CACHE KEY PARITY ERROR ON KEY A OR KEY B	PARITY ERROR OF FETCHED MICRO IN M-REGISTER	CASSETTE ERROR NOT CORRECTABLE
PERM	S-MEMORY MICRO INSTRUCTION TIME-OUT	S-MEMORY FIELDS OUT OF ADMINIS-TRATIVE BOUNDS	S-MEMORY E-LOG REGISTER LOGGED	UNCORRECTABLE S-MEMORY ERROR IN PROC. OPS
MSSW	NULL BIT	NULL BIT	S1: MICRO SOURCE FROM CACHE OR FRO-ZEN IN M-REGISTER	S0: MICRO SOURCE FROM S-MEM OR FRO-ZEN IN M-REGISTER

INT. = ANY ONE OR MORE OF: CC0, CC1, CC2, CD0, CD3, INCN1, INCN3.

THE ERROR LOG REGISTER HAS MEANINGS AS FOLLOWS:



PU: UNCORRECTABLE ERROR ON CPU ACCESS
NU: UNCORRECTABLE ERROR ON NON-CPU ACCESS
S: SINGLE BIT ERROR (CORRECTED IN DATA OR CHECK-BIT)
D: DUPLICATE ERROR OCCURRENCE (LOGGING DATA LOST)
W: BOARD/ROW/SYNDROME LOADED ON WRITE OPERATION

NOTE: REGISTER BITS AS WELL AS MICRO INSTRUCTION BITS ARE NUMBERED ACCORDING TO HARDWARE CONVENTION. MSB IS HIGHEST-ORDER (AND LEFTMOST) BIT.

G14731/SHEET 3 OF 3

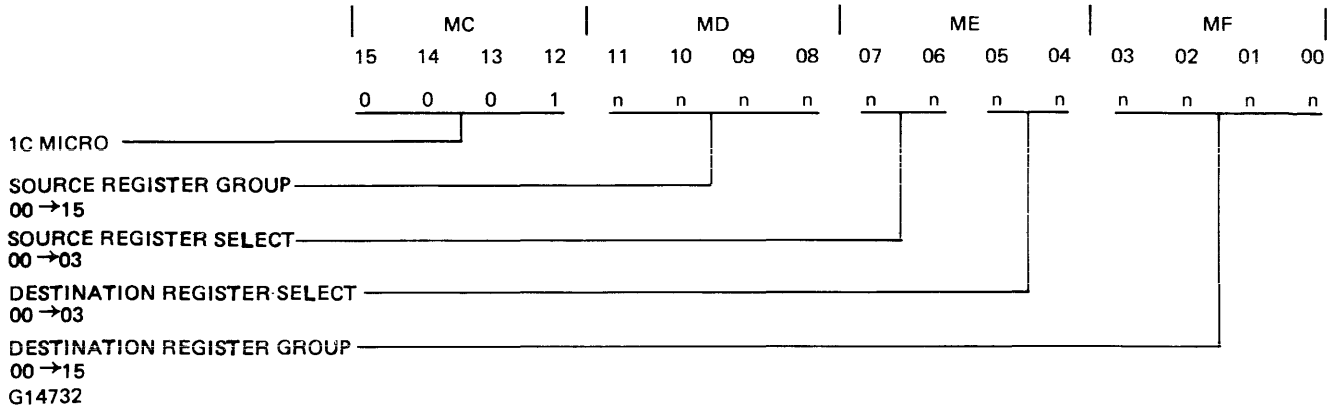
REGISTER GROUP	REGISTER SELECT 0	1	2	3
0	TA	FU	X	SUM
1	TB	FT	Y	CMPX
2	TC	FLC	T	CMPY
3	TD	FLD	L	XANY
4	TE	FLE	A	XEQY
5	TF	FLF	M	MSKX
6	CA	BICN	BR	MSKY
7	CB	FLCN	LR	XORY
8	LA	NULL-A	FA	DIFF
9	LB	RESV	FB	MAXS
10	LC	PERM	FL	NULL-C
11	LD	PERP	TAS	U
12	LE	XYCN	CP	NULL-D
13	LF	XYST	NULL-B	DATA
14	CC	INCN	CSW	CMND
15	CD	MSSW	TIMR	NULL

INDIVIDUAL BITS OF SOME 4-BIT REGISTERS HAVE SPECIAL MEANINGS AS NOTED BELOW:

	3	2	1	0
BICN	LSUY	CYF	CYD	CYL
XYCN	MSBX	X = Y	X < Y	X > Y
XYST	LSUX	INT	Y NEQ 0	X NEQ 0
FLCN	FL = SFL	FL > SFL	FL < SFL	FL NEQ 0
INCN	PORT DEV. MISSING	PORT HI PRIORITY	PORT INTERRUPT	PORT LOCKOUT
CC	CONT. PANEL STATE LAMP FLIP-FLOP	REAL TIME CLOCK INTERRUPT	I/O BUS SERV. RQST INTERRUPT	CONTROL PANEL INTERRUPT
CD	MEM. READ ERROR INTERRUPT	MEM. WRITE/SWAP (LR/BR CHK) OUT OF BDS OVERRIDE	MEM. READ ADDR. (LR/BR CHK) OUT OF BDS	MEM. WRITE/SWAP (LR/BR CHK) OUT OF BDS INTERRUPT

Figure 1-47. B 1860 System Micro Chart (Sheet 3 of 3)

1C Register Move



The contents of the source register are moved to the destination register. If the move is from a smaller register to a larger one, the data is right-justified with left (most significant) zero bits supplied. Moves from larger registers to smaller ones are also right-justified, but with the excess most-significant bits truncated.

The contents of the source register are unchanged unless it is also the destination register.

Exceptions:

a. CMND is excluded as a source register.

b. When M is used as a destination register, the operation is changed to a bit OR which modifies the next microinstruction. It does not modify the instruction as stored in the memory.

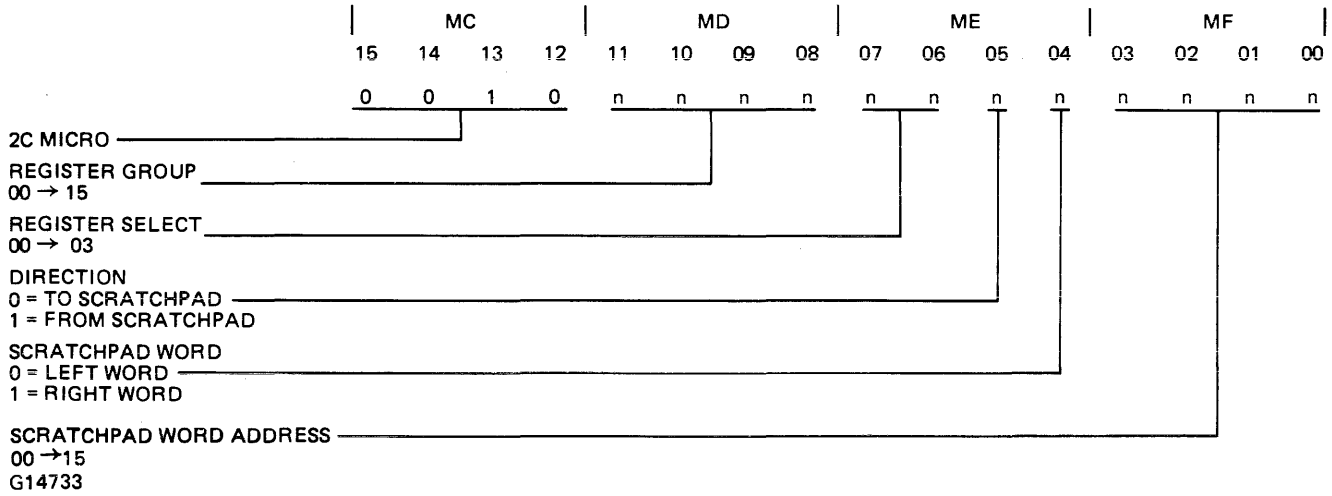
c. BICN, FLCN, XYCN, XYST, INCN, CSW, CMPX, CMPY, XANY, XORY, XEOY, MSKX, MSKY, DIFF, MAXS, and U are excluded as destination registers.

d. When DATA is designated as a source, CMND and DATA are prohibited as destinations.

e. U is excluded as a source register in the Single Micro mode.

f. TIME is excluded as a sink register.

2C Scratchpad Move



The contents of the register are moved to the scratchpad, or vice versa. If the source and destination of unequal lengths, the data is right-justified with left (most significant) zero bits supplied or with data truncated from the left, whichever is appropriate. The contents of the source register are unchanged.

Exceptions:

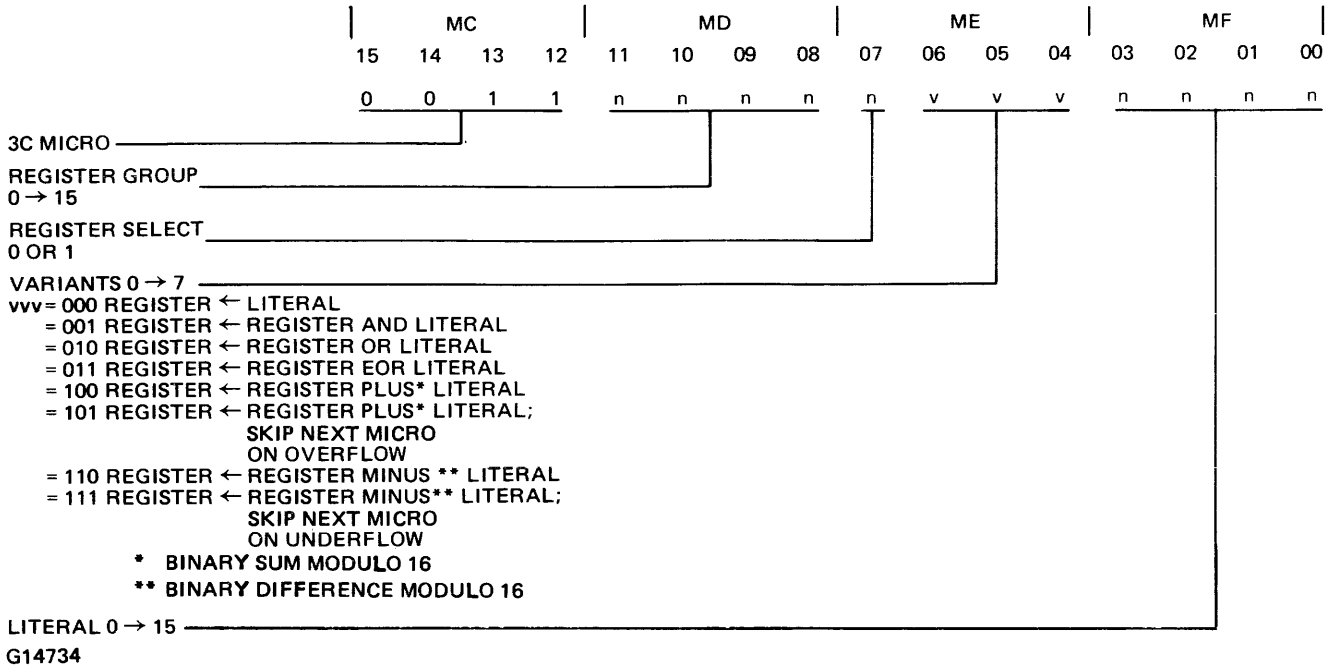
a. CMND is excluded as a source register; U is excluded as a source in the step mode.

b. When M is used as a destination register, the operation is changed to a bit OR which modifies the next microinstruction. It does not modify the instruction as stored in the memory.

c. BICN, FLCN, XYCN, XYST, INCN, CSW, SUM, CMPX, CMPY, XANY, XORY, XEOY, MSKX, MSKY, DIFF, MAXS, and U are excluded as destination registers.

d. TIME is excluded as a source or sink.

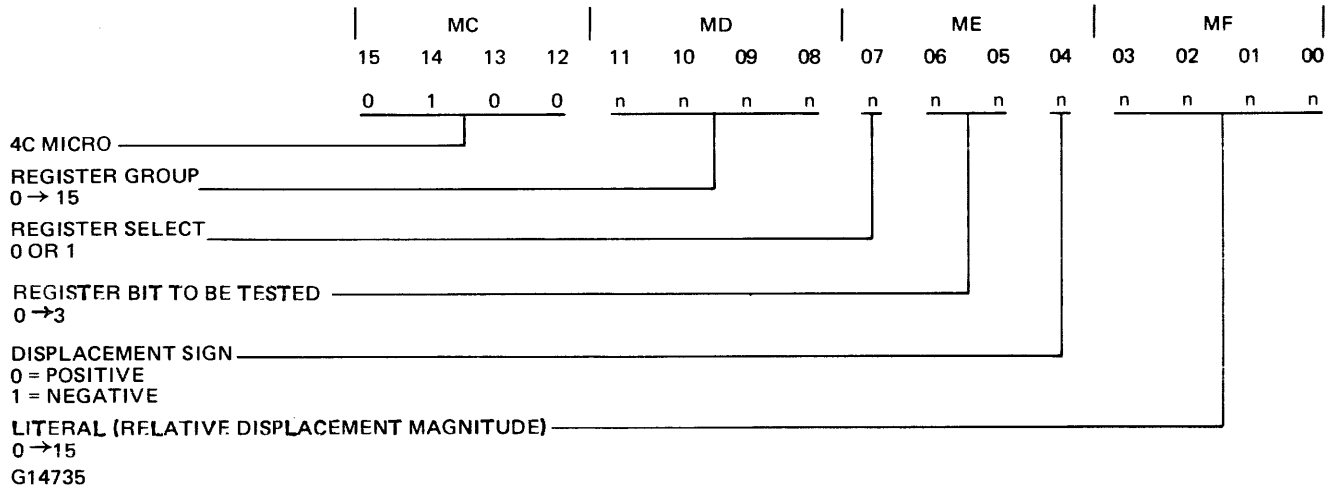
3C 4-Bit Manipulate



Exception: BICN, FLCN, XYCN, XYST, and INCN, when specified as operand registers, are not changed as a result of this operation. However, the carry and borrow outputs are produced and a skip can result.

The manipulate operation specified by the variants is performed on the 4-bit register identified by Register Group and Register Select.

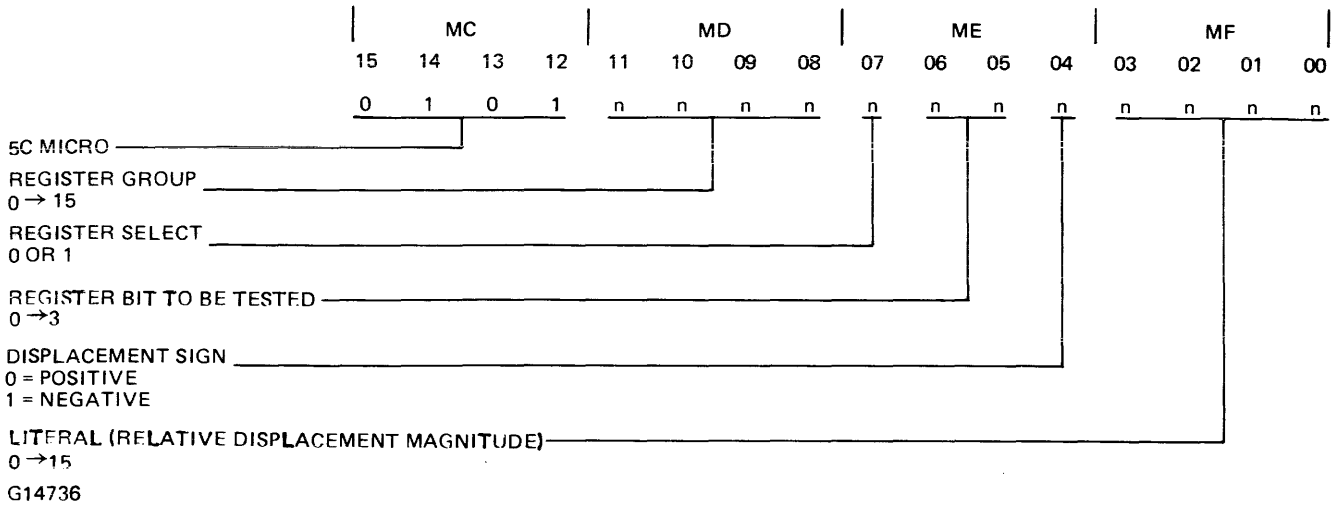
4C Bit Test Relative Branch False



The designated bit within the specified register is tested and a branch relative to the next instruction by the signed displacement value is taken if the bit is 0. If the bit is 1, a displacement value of 0 is assumed and control passes to the next in-line M-instruction. A displacement value indicates the number of 16-bit words from the next in-line instruction.

Exception: TIME is excluded as a source.

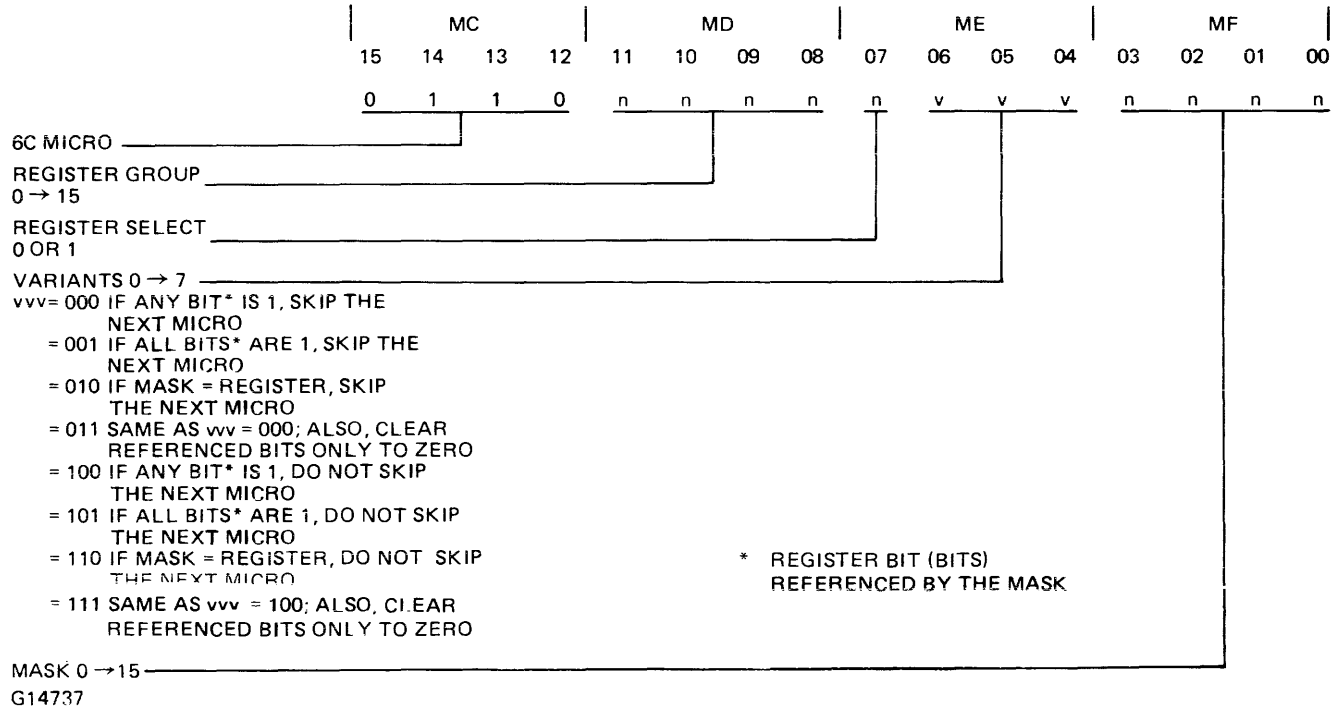
5C Bit Test Relative Branch True



The designated bit within the specified register is tested and a branch relative to the next instruction by the signed displacement value is taken if the bit is one. If the bit is zero, a displacement value of zero is assumed and control passes to the next in-Line M-instruction. A displacement value indicates the number of 16-bit words from the next in-line microinstruction.

Exception: TIME is excluded as a source.

6C Skip When



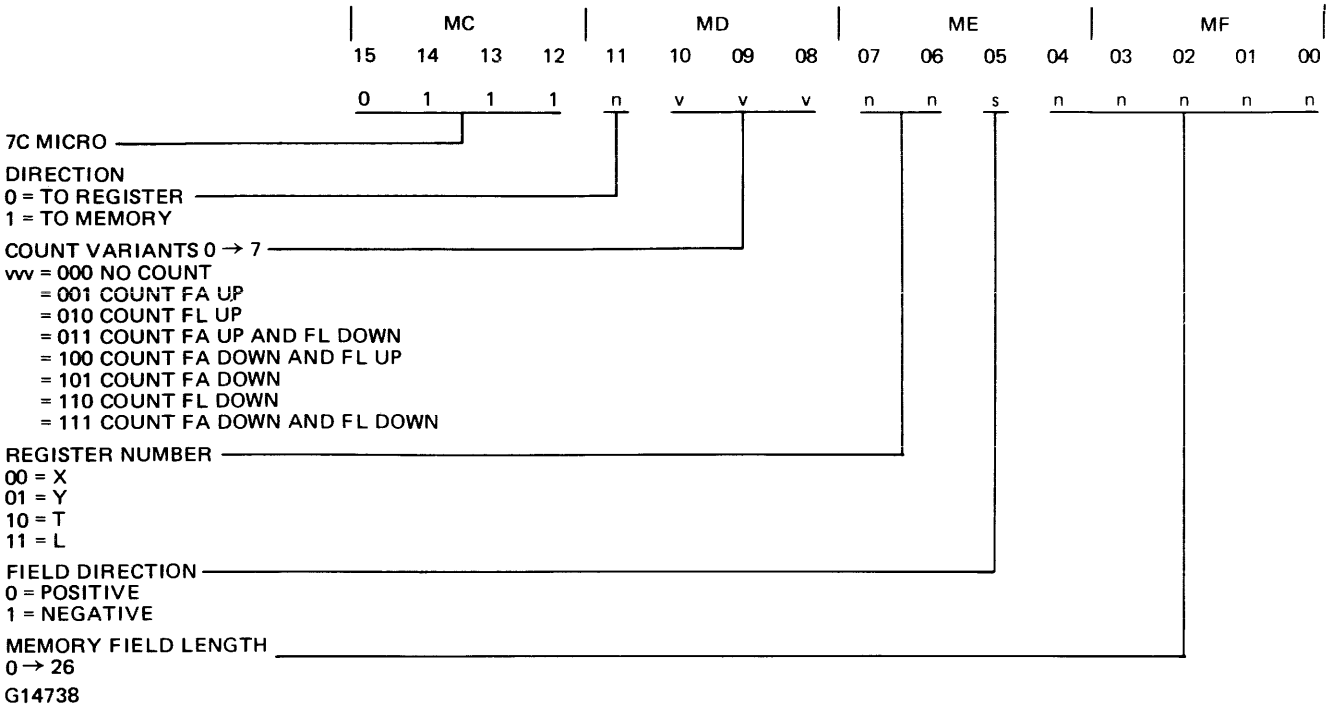
Four-bit registers are specified; register bits referenced by the 1 bits in the mask are tested and action is taken as specified by the variant. (Actions are listed in the figure.)

If the mask = 0000:

a. The "any" result is false, "all" is true.
b. The skip is made for vvv = 001, 011, 100.
c. The skip is not made for vvv = 000, 101, 111.

Exceptions: BICN, FLCN, XYCN, XYST and INCN can be tested but they cannot be cleared.

7C Read/Write Memory



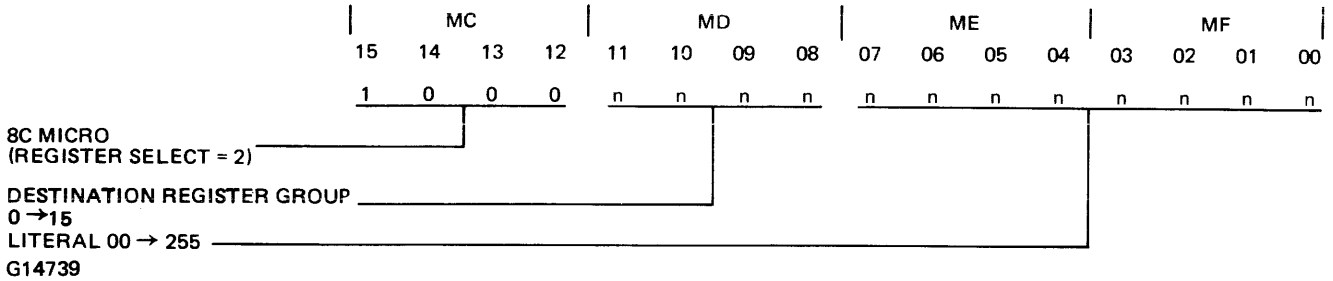
The contents of the register are moved to memory, or vice versa. If the value of the memory field length is less than 24, the data from memory is right-justified with left (most significant) zero bits supplied, while the data from the register is truncated from the left.

The contents of the source are unchanged. Register FA contains the bit address of the memory field while the memory field direction sign and memory field length are given in the instruction.

If the value of the memory field length as given in the instruction is zero, the value in CPL is used.

Memory field length values of 25 and 26 are truncated to the value 24. When used on a Write operation, the value 25 causes all error logging and reporting to be suppressed and correct. The value 26 used on a Write operation causes the same result, except that incorrect error correction code bits are written into memory (equivalent to forcing bad parity in earlier systems).

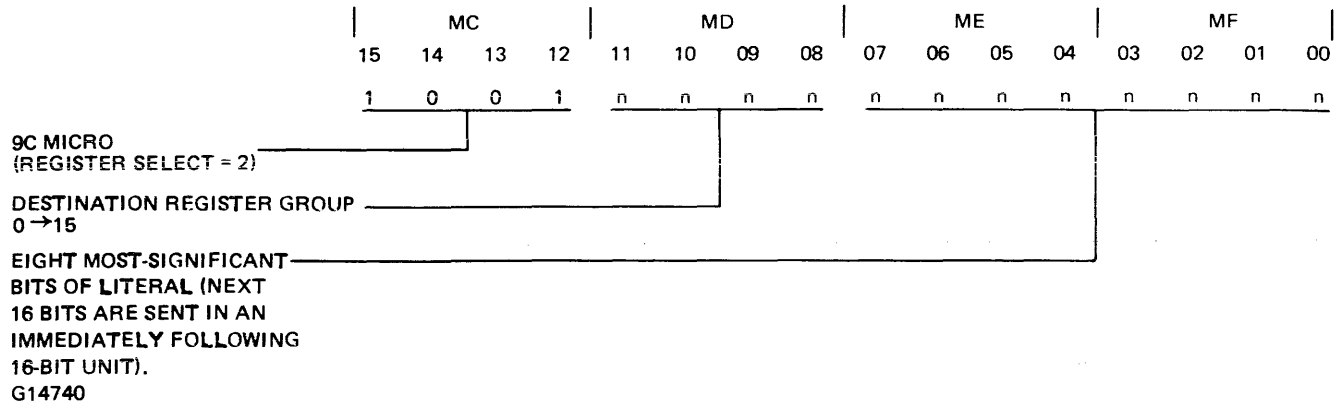
8C Move 8-Bit Literal



The 8-bit register literal given in the instruction is moved to the destination register. If the move is to a register that is greater than eight bits in length, the data is right-justified with left (most significant) zero bits supplied. A move to the TIME register results in resetting TIME to 0.

Exception: CSW is excluded as a destination.

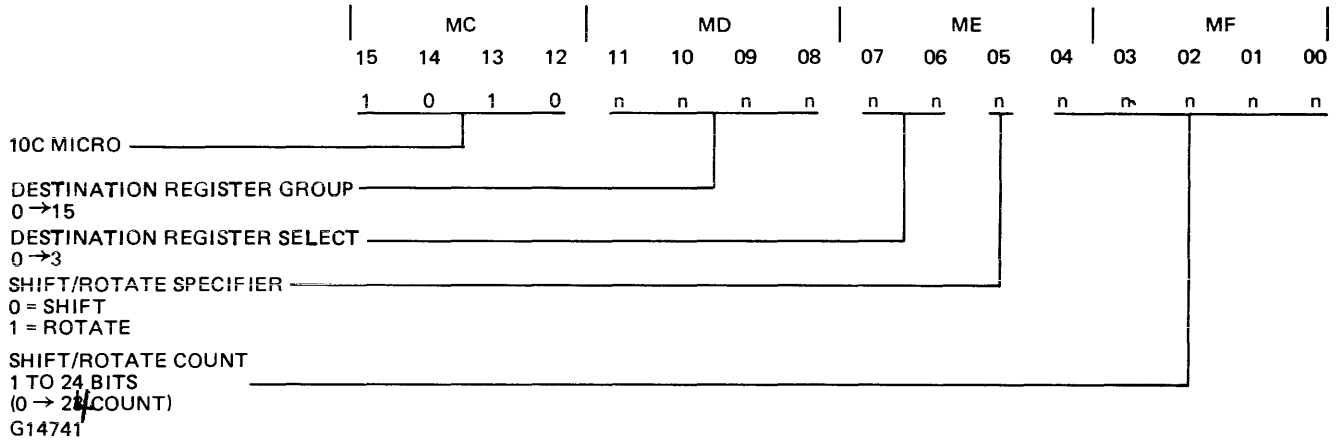
9C Move 24-Bit Literal



The 24-bit literal given in the instruction is moved to the destination register. The 16 least-significant bits of the literal are stored in the position of the next in-line microinstruction. If the move is between registers of unequal lengths, the literal is truncated from the left. A move to the TIME register results in resetting TIME to 0.

Exception: CSW and M are excluded as destinations.

10C Shift/Rotate T Register Left



Register T is shifted (rotated) left by the number of bits specified; then, the 24-bit result is moved to the destination register. If the move is between registers of unequal lengths, the data is right-justified with data truncated from the left.

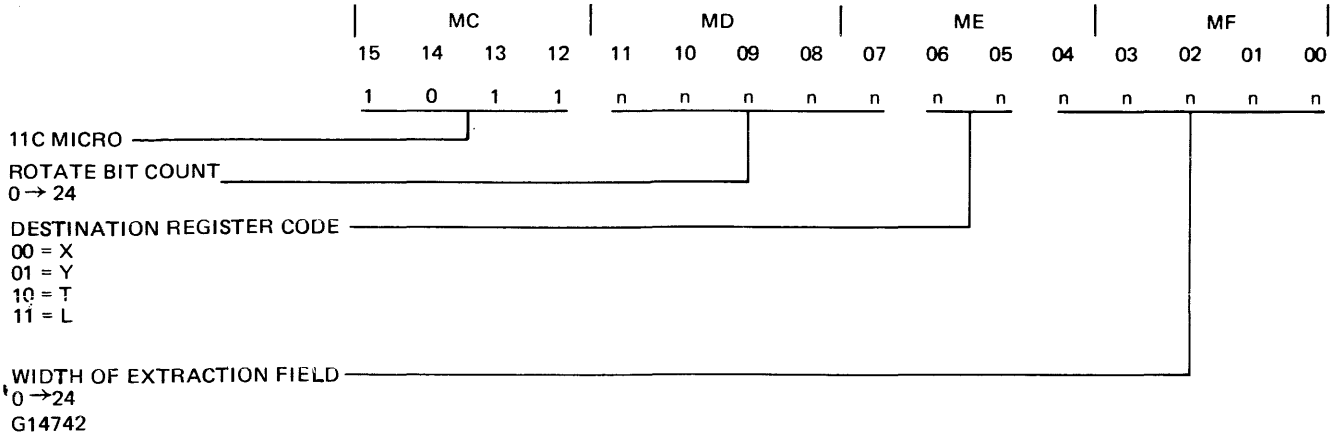
The contents of the source register are unchanged unless the register is also the destination register. Zero fill on the right and truncation on the left occurs for the shift operation. If the value of the shift/rotate count as given in the instruction is 0, the value given in CPL is used.

Exceptions:

a. When M is used as a destination register, the operation is changed to a bit OR which modifies the next microinstruction. It does not modify the instruction as stored in memory.

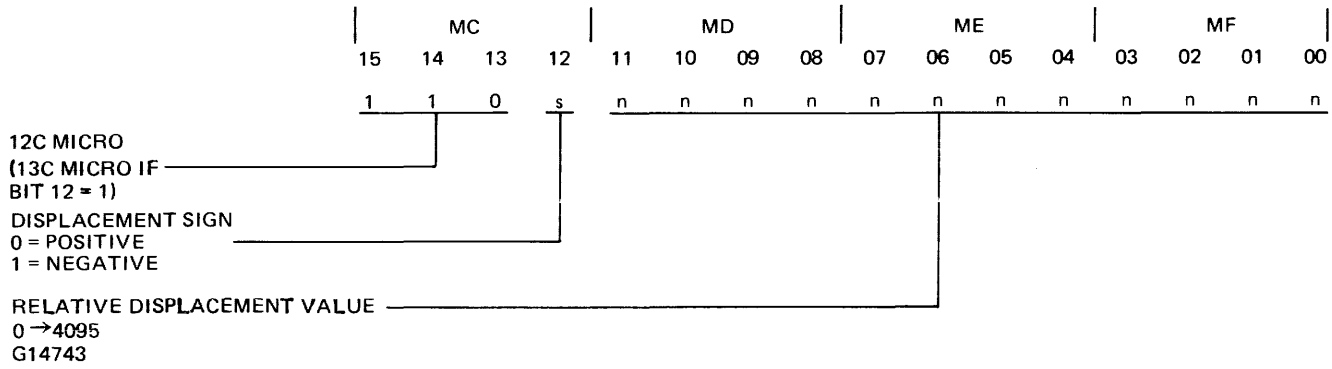
b. BICN, FLCN, XYCN, XYST, INCN, CSW, SUM, XEOY, XORY, CMPX, CMPY, XANY, MSKX, MSKY, DIFF, MAXS, and U are excluded as destination registers.

11C Extract from T-Register



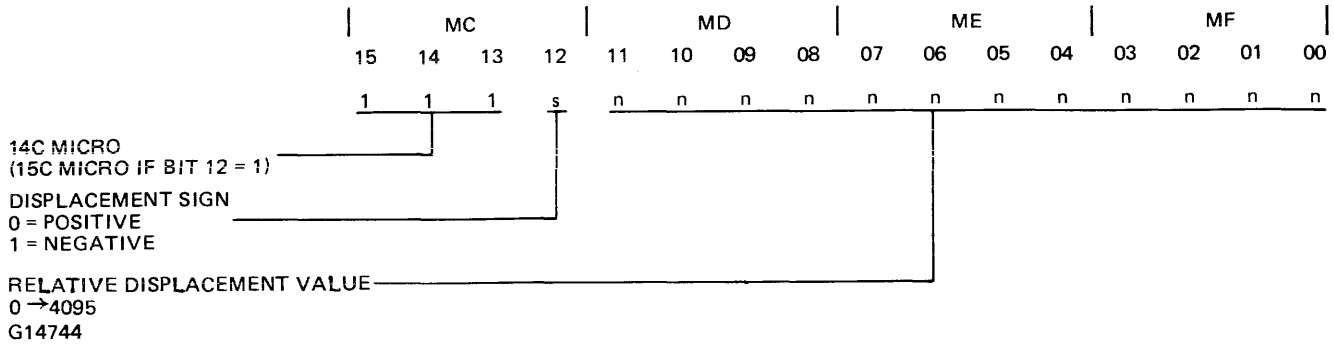
Register T is rotated left by the number of bits specified; then, the number of bits specified are extracted. The result is moved to the destination register. If the extract bit count is less than 24, the data is right-justified with left (most significant) zero bits supplied. The contents of the source register are unchanged unless it is also the destination register. The rotate value of 24 is equivalent to 0.

12C/13C Branch Relative



The next microinstruction is fetched from the location obtained by adding the relative displacement value given in this micro instruction to the word address of the next in-line microinstruction. A displacement value indicates the number of 16-bit words. Only the contents of the A register are affected.

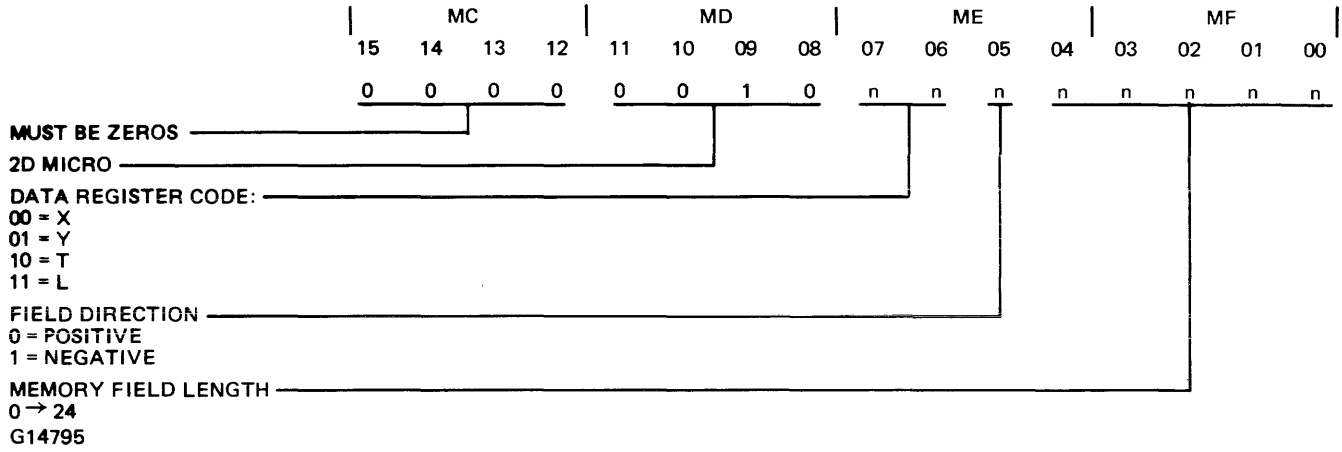
14C/15C Call



The address of the next in-line microinstruction is pushed into the A-stack; then, the next microinstruction is fetched from the location obtained by adding the signed relative displacement value given in this microinstruction to the word address of the next in-line microinstruction. The displacement value indicates the number of 16-bit words. Only the contents of the A register are affected.

Note that exit is accomplished by employing the 1C (Register Move) instruction with TAS as the source register and A as the destination register.

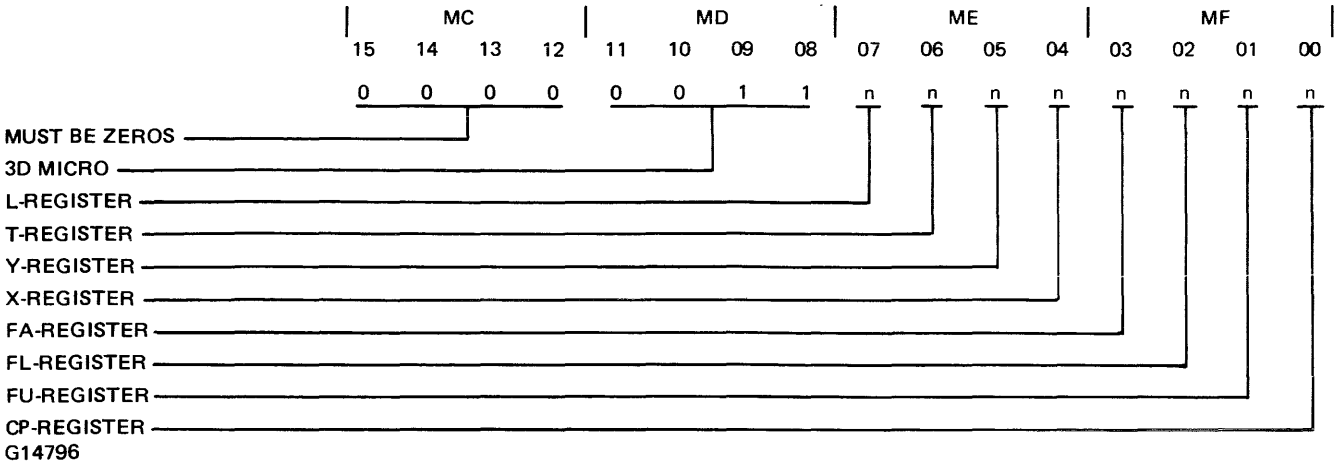
2D Swap Memory



Data from main memory is swapped with the data in the specified register.

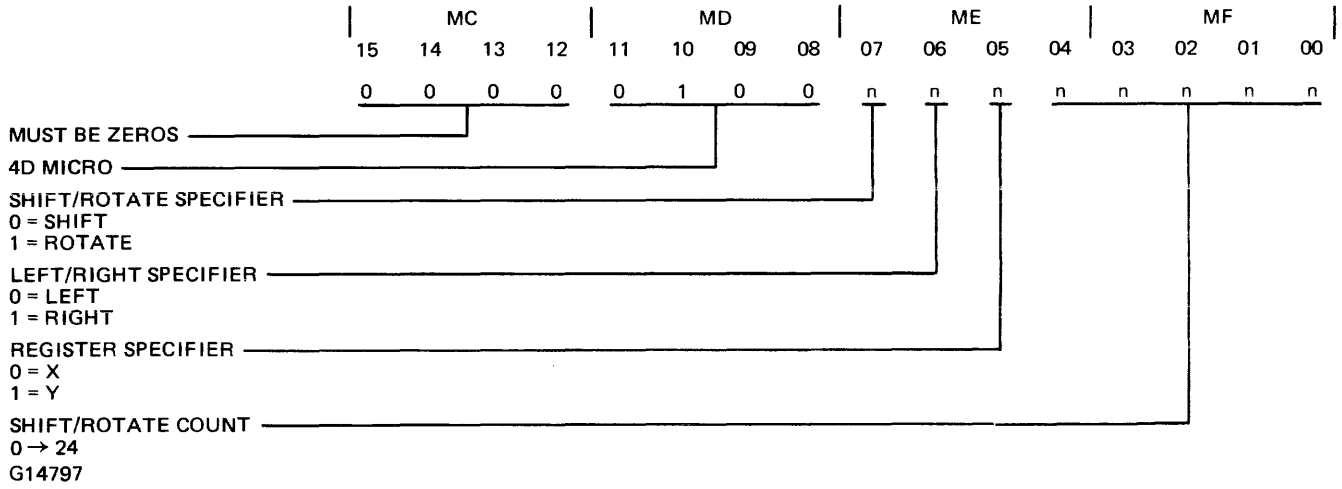
If the value of the memory field is less than 24, the data from memory is right-justified with left (most-significant) zero-bits supplied while the data from the register is truncated from the left. Register FA contains the bit address of the memory field. If the value of the memory field length as given in the instruction is zero, the value in CPL is used.

3D Clear Registers



The specified (n = 1) register is unconditionally cleared to zero. None, some, or all listed registers may be specified.

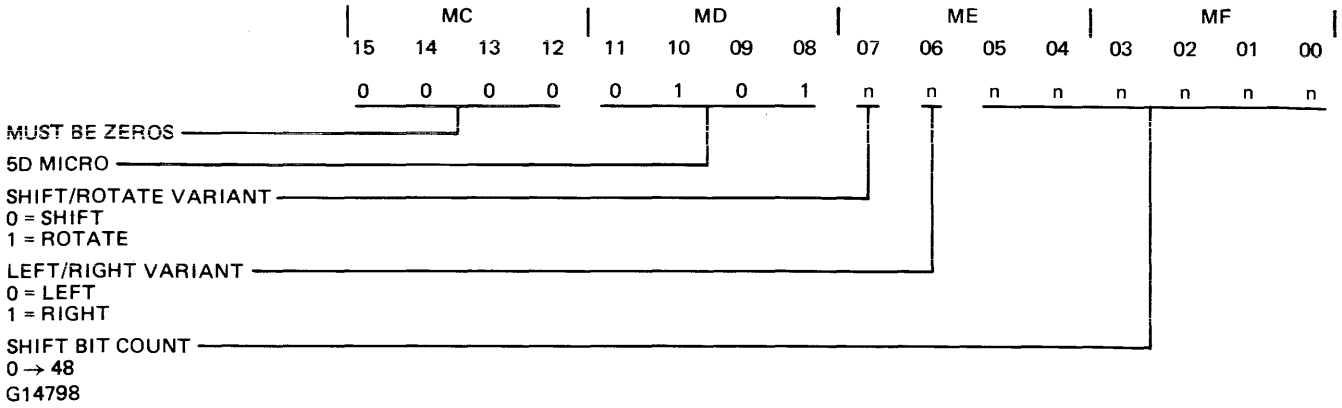
4D Shift/Rotate X or Y



Register X(Y) is shifted (rotated) left (right) by the number of bits specified. Zero-fill on the right and truncation on the left occurs for the left shift. Zero-fill on the left and truncation on the right occurs for the right shift.

If the value of the shift/rotate count as given in the instruction is 0, the amount the operand is shifted (rotated) is 0.

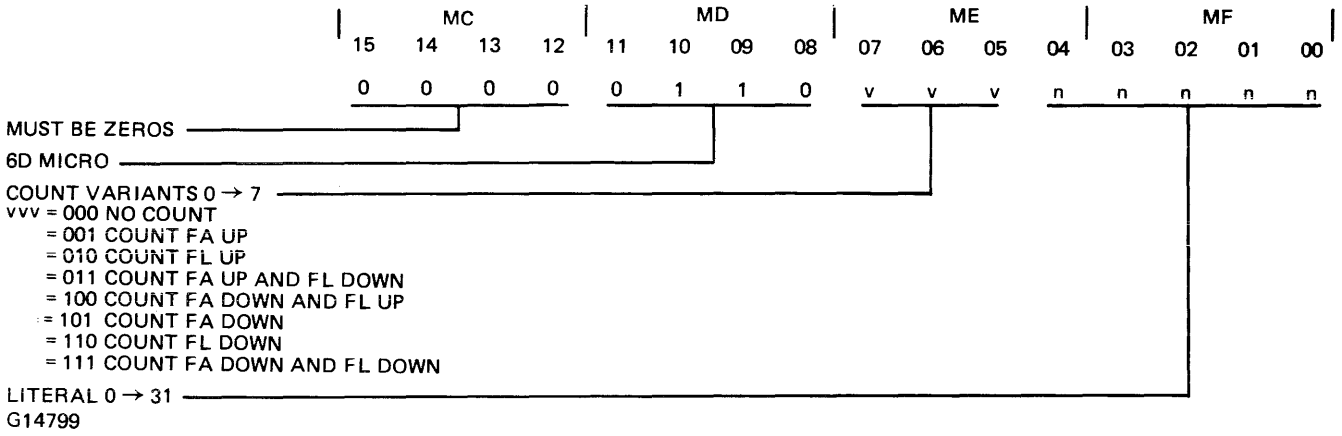
5D Shift/Rotate X and Y



Registers X and Y are shifted (rotated) left (right) by the number of bits specified. The X-register is the leftmost (more-significant) half of the concatenated 48-bit XY register.

Zero-fill on the right and truncation on the left occurs for the left shift. Zero-fill on the left and truncation on the right occurs for the right shift.

6D Count FA/FL

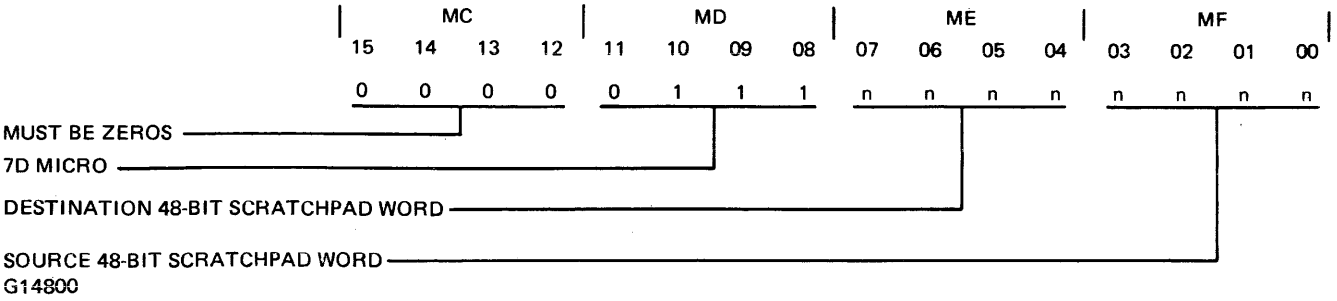


The designated register(s) are binarily incremented (decremented) by the value of the literal contained in the instruction or by the value of CPL if the value of the literal is 0.

Neither overflow nor underflow of FA is detected.

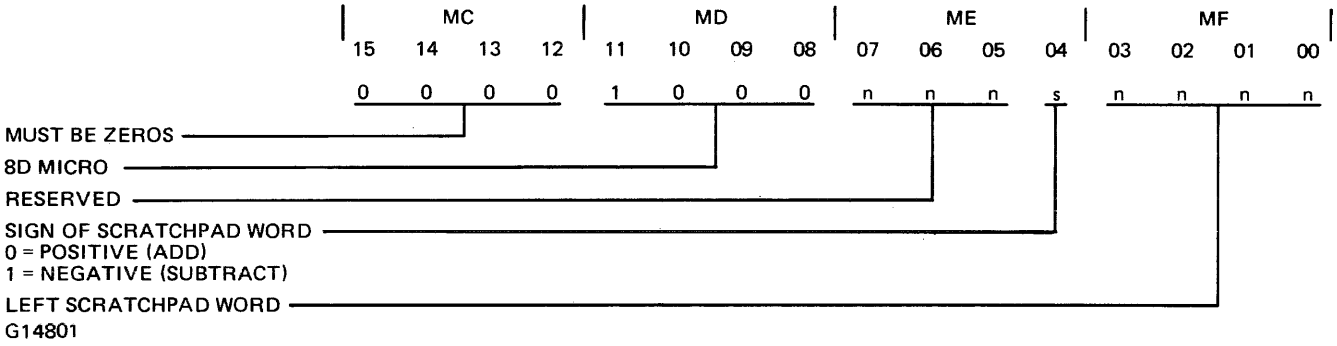
The value of FA may go through its maximum value or its minimum value and wrap around. Overflow of FL is also not detected. The value of FL may go through its maximum value and wrap around. Underflow of FL is detected and will not wrap around, zero is left in FL.

7D Exchange Doublepad Word



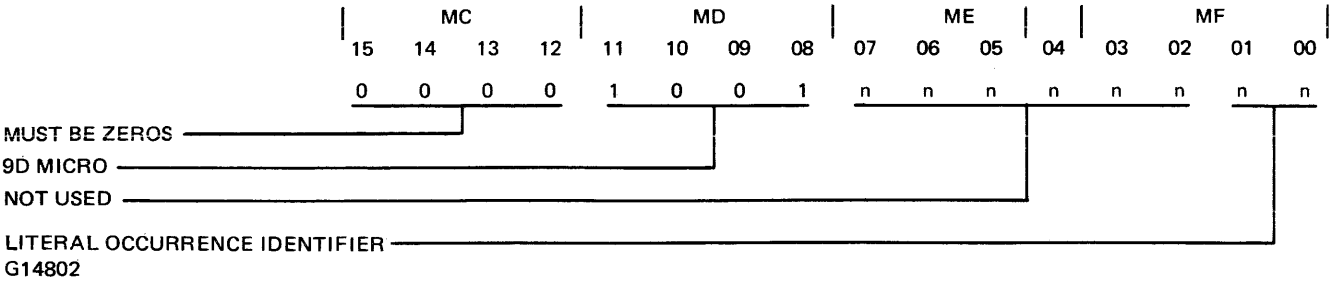
The contents of the FA and FB registers are moved to a holding register. The contents of the left and right source scratchpad words are moved to the FA and FB registers, respectively. The contents of the holding register are moved to the left and right words of the 48 bit destination scratchpad word.

8D Scratchpad Relate FA



The contents of the FA register are replaced by the sum of the FA register and the specified scratchpad register or the difference between them (subtract operation). Neither overflow nor underflow of FA is detected.

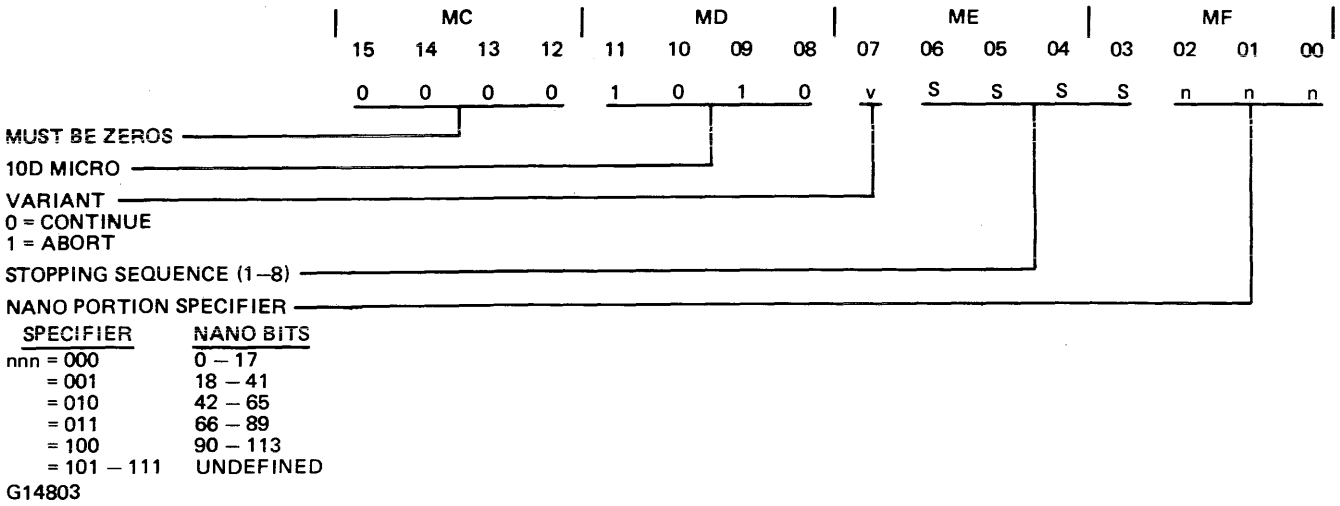
9D Monitor



Monitor has no function programmatically and is treated as a no-op. However, execution of a 9D micro generates a special marker pulse which may be used to activate or synchronize external test equipment. The Literal Occurrence Identifier (LOI) produces the following special identifying pulses when used:

LOI Value	Signal (Mnemonic)
00, 01, 10 or 11	MONTORE0
00	MNTR0.E0
01	MNTR1.E0
10	MNTR2.E0

10D Nano Move

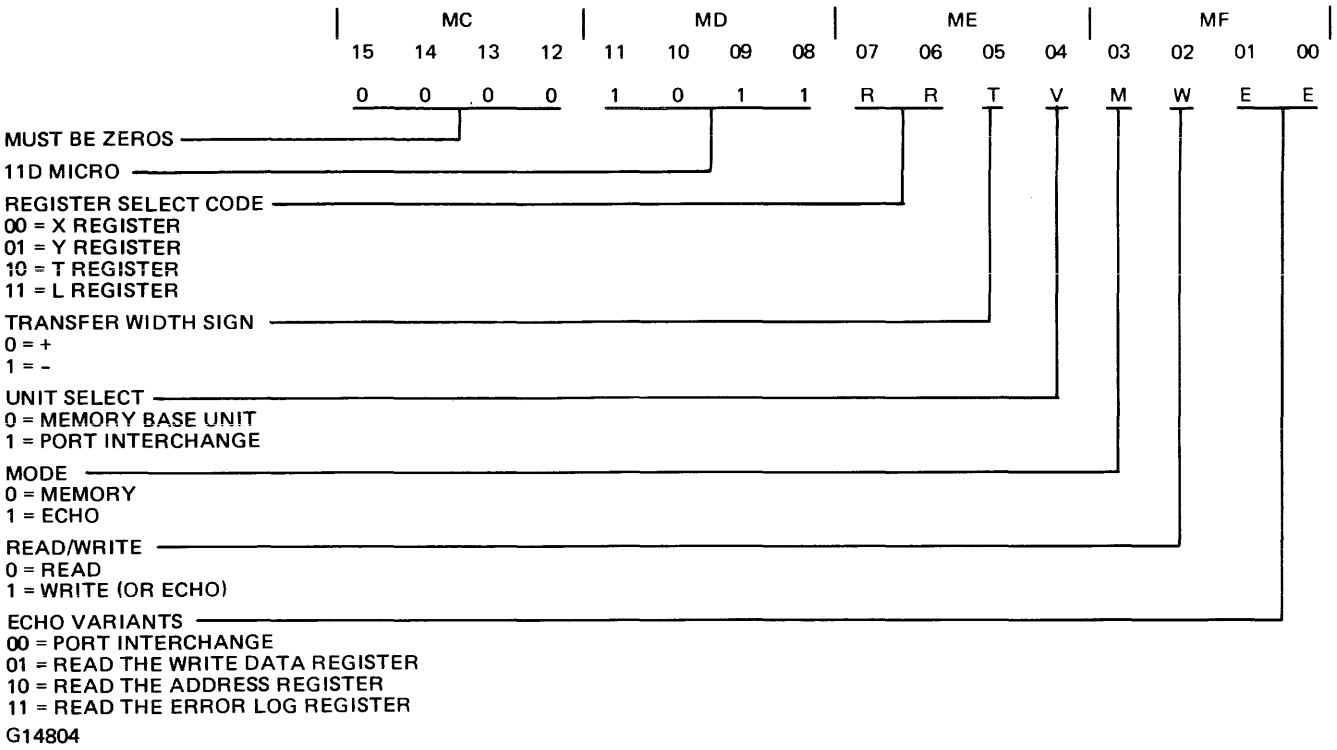


The contents of a specified portion of the Nano register are stored in the BR register during execution of the following micro. Nano Move is used to monitor conditions existing within the processor microdecoding structure for diagnostic purposes. It is treated as a no-op, and acts only to preset the control logic for carrying out the desired function during the following micro.

Execution of the following micro is altered as follows. The following micro begins executing in the normal manner, but the process is halted when the nano sequence number equals the Stopping Sequence Specifier in the 10D micro (this may occur during the first or any subsequent sequence, as required). At this time the nano portion (those bit positions of the Nano register called for by bits 00-02 of the 10D micro) is moved to the BR register.

Processor actions following the move to BR depend on the variant portion of the 10D micro. If the Abort option is selected, the micro being tested is terminated by clearing the Nano register. Following this, the next micro in sequence is executed normally. If the Continue option is selected, the nano register is shifted until the contents regain their original position, then execution of the micro being tested resumes. In either case (Abort or Continue), the original contents of BR are lost.

11D Diagnostic Read/Write Memory



Data is moved to or from the memory or port interchange as specified by the variants selected. The origin or destination for this data is the X, Y, T or L register in the processor. Where memory access is specified, the memory address is determined by the contents of FA. The possible operations and the associated data formats follow.

NOTE
Variant combinations other than those described below are illegal, and will produce undefined results.

WRITE MEMORY

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	1	0	1	1	R	R	T	0	0	1	x	x

x = DON'T CARE
G14805

Sixteen data bits plus six error-correction bits are written at the memory location (even word boundaries only) specified by FA. The ability to write into the check bit storage elements is provided primarily to permit performance verification. The following data format is used.

23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
C	C	C	C	C	C	0	0	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

CHECK BITS
ALWAYS ZERO
DATA
G14806

READ MEMORY

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	1	0	1	1	R	R	T	0	0	0	x	x

x = DON'T CARE
G14807

Sixteen data bits plus one parity bit and six error correction bits are read from the memory location (even word boundaries only) specified by FA.

Parity is odd for 16 data bits plus the parity bit. Performance verification for the error correction logic is incorporated into the applicable maintenance diagnostic programs. The following data format is used.

23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
C	C	C	C	C	C	0	P	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

CHECK BITS
PARITY
DATA
G14808

READ ERROR-LOG REGISTER

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	1	0	1	1	R	R	x	0	1	0	1	1

x = DON'T CARE
G14809

The contents of the Error Log Register (in the Memory Base Unit) are read and the register is cleared. The following data format is used.

23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
D	P	N	S	W	0	0	0	0	0	0	0	B	B	B	B	R	R	S	S	S	S	S	S

D = DUPLICATE ERROR
P = PROCESSOR ERROR
N = NON-PROCESSOR ERROR
S = SINGLE-BIT ERROR
W = READ/WRITE ERROR
NOT USED
BOARD LOCATION OF ERROR (0 → 15)
ROW LOCATION OF ERROR (0 → 3)
SYNDROME
G14810

READ WRITE-DATA REGISTER

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	1	0	1	1	R	R	x	0	1	0	0	1

x = DON'T CARE
G14811

The contents of the Write Data register (in the memory base unit) are read. Data format is the same as before transmission to memory.

READ ADDRESS REGISTER

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	1	0	1	1	R	R	x	0	1	0	1	0

x = DON'T CARE
G14812

The contents of the Address register in the memory base unit are read. Data format is the same as the A-register in the processor.

READ PORT INTERCHANGE LATCHES

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	1	0	1	1	R	R	x	1	1	0	0	0

x = DON'T CARE
G14813

The contents of the Port Interchange latches are read. These latches contain whatever data was placed there by a previous operation. The data format is the standard 24-bit field.

ECHO PORT INTERCHANGE WRITE DATA

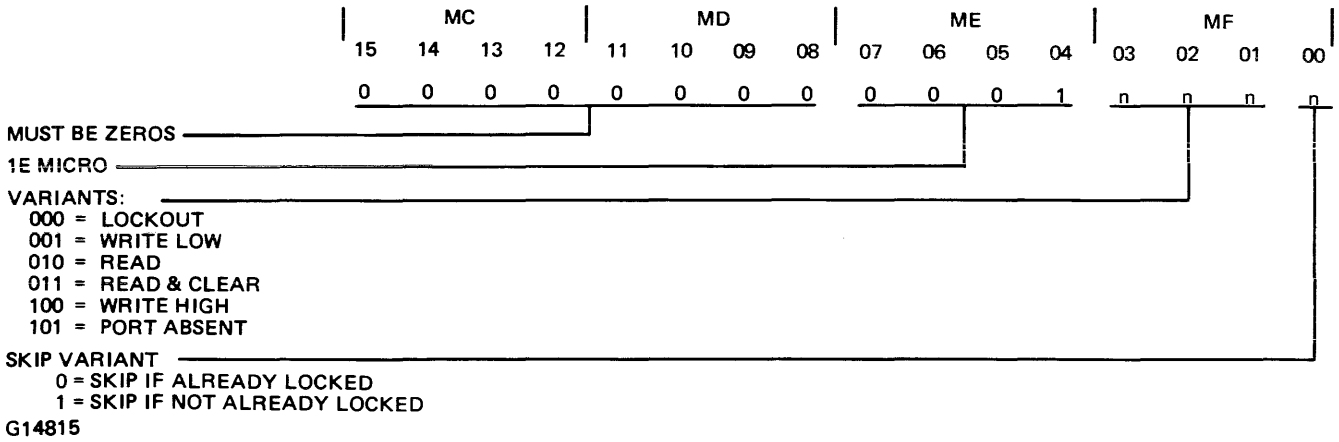
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	1	0	1	1	R	R	x	1	1	1	E	E

x = DON'T CARE
G14814

The contents of the selected register are returned to the Port Interchange where they are stored in the Read Data latches. The stored data is then returned to tne source by the route specified by the echo variant:

EE = 00 Data is returned directly.
EE = 01 Data is returned via port adapter 1.
EE = 10 Data is returned via port adapter 2.
EE = 11 Data is returned via port adapter 3.

1E Dispatch



The Dispatch micro is used to initiate port-to-port communications and to receive interrupt information from other ports. Since the dispatch system is shared by all ports, the processor must gain control of it by successfully completing a lockout operation prior to a dispatch write.

The skip variant allows skipping of the next 16-bit instruction based upon success or failure of the lockout attempt.

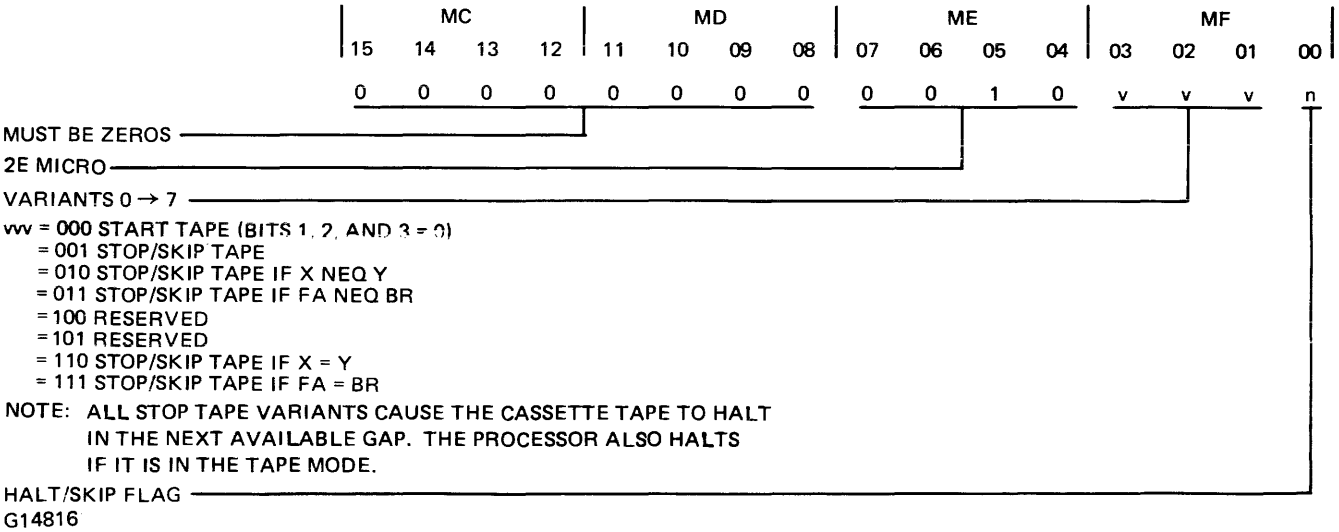
The Write Dispatch operation sets the lockout and interrupt flip-flops in the port interchange. This operation also causes the contents of the L-register to be stored in memory location 0 (24 bits) and the contents of the least-significant seven bits of the T-register (port and channel) to be stored in the port interchange dispatch register. In addition, the Write operation sets or resets the high-priority-interrupt flip-flop in the port interchange.

The Read Dispatch operation moves the contents of memory location 0 (24 bits) into the L-register and the contents of the port interchange dispatch register into the least-significant seven bits of the T-register. The other 17 bits of the T-register are unaffected.

The Read and Clear Dispatch operation, in addition to performing the Read Dispatch operation, clears the lockout flip-flop, the two interrupt flip-flops, and the port device absent flip-flop in the port interchange. It does not clear any memory locations.

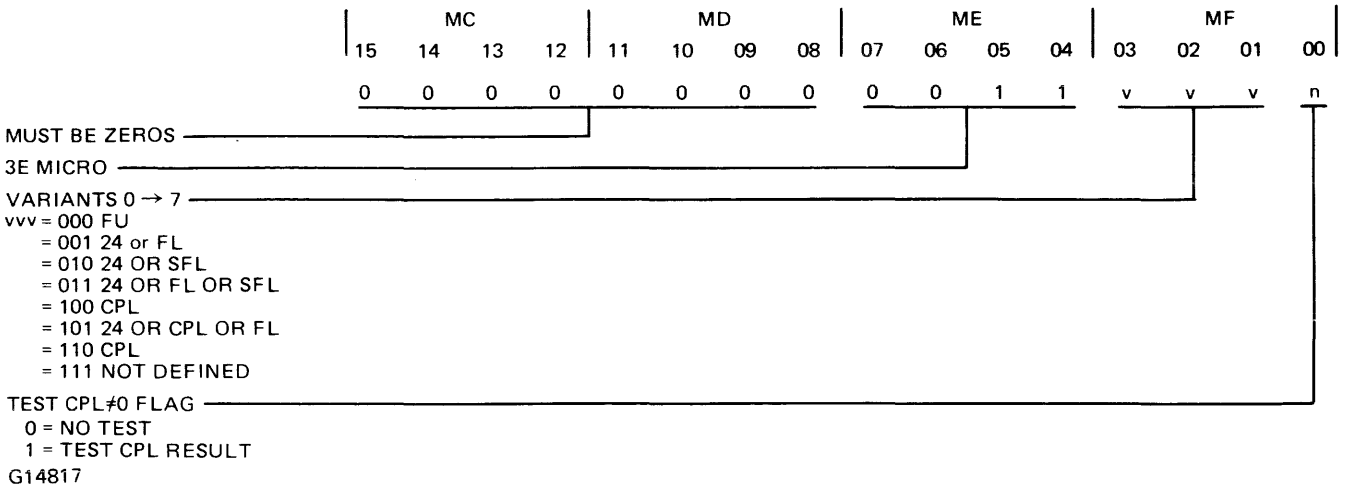
The Port Absent operation is executed by the processor when necessary to return a port absent level signal to another port, indicating the absence of the designated channel.

2E Cassette Control



The operation specified by the variants is performed by the tape cassette.

3E Bias

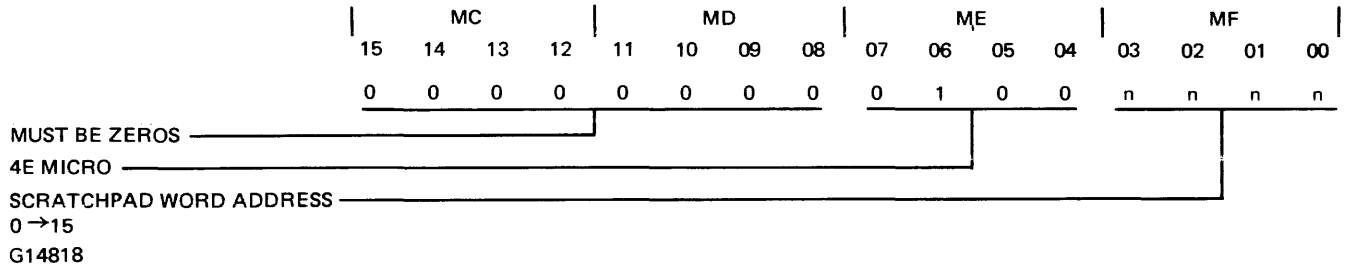


This microinstruction sets CPU to 1 if FU is 4 or 8; otherwise it sets CPU to 0. Exception if vvv = 010, SFU, not FU, is the determinant.

This microinstruction also sets CPL to the smallest of the values given in the applicable vvv variant.

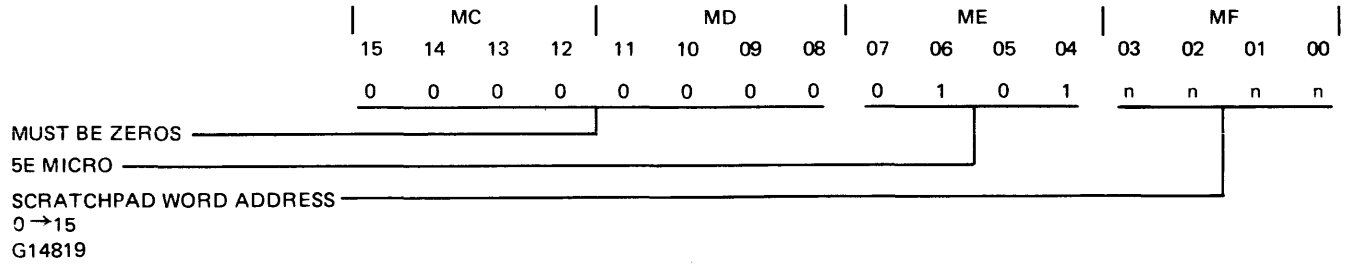
If Test CPL Unequal To Zero flag = 1 and the final value of CPL is not 0, the next microinstruction is skipped.

4E Store F in Doublepad Word



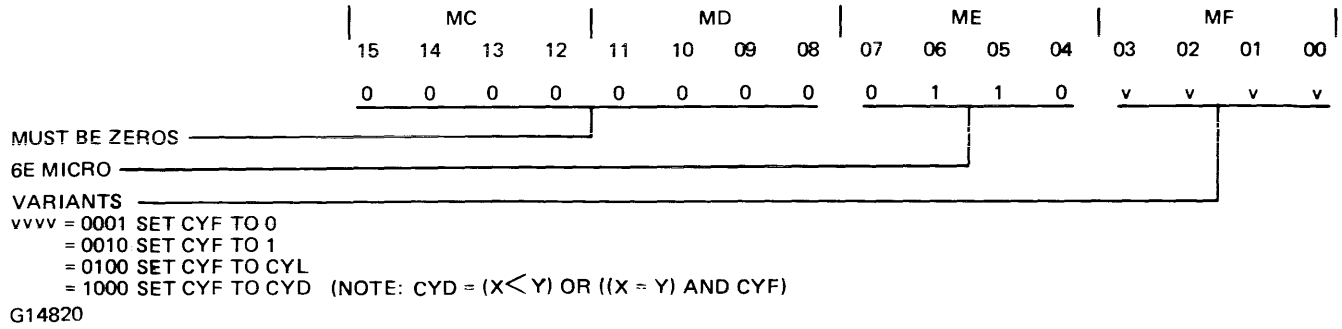
The contents of the FA and FB registers are moved to the left and right words, respectively, of the designated scratchpad address.

5E Load F From Doublepad Word



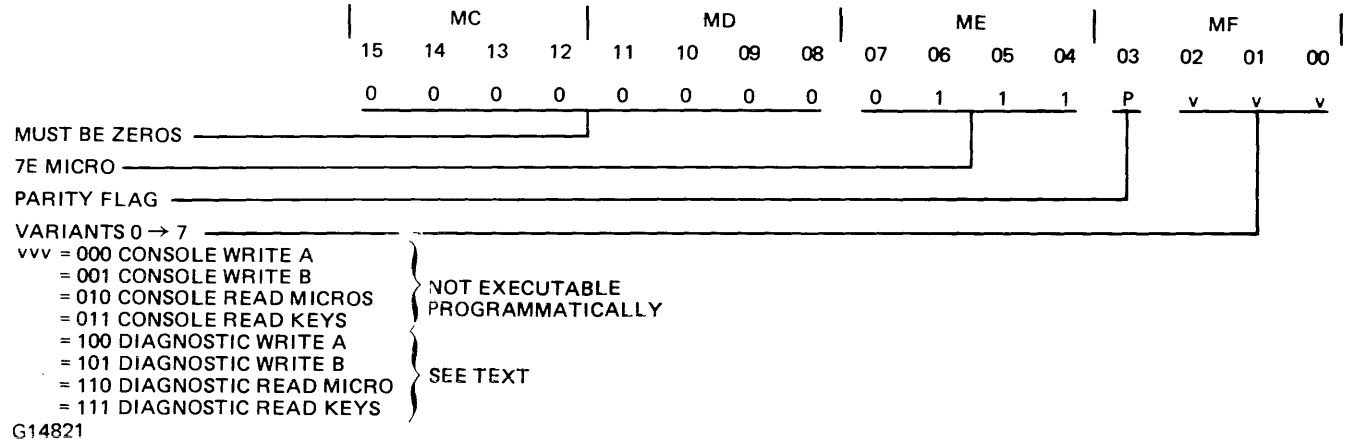
The contents of the left and right words at the designated scratchpad address are moved to the FA and FB registers, respectively.

6E Carry Flip-Flop Manipulate



The carry flip-flop is set as specified by the vari- ants.

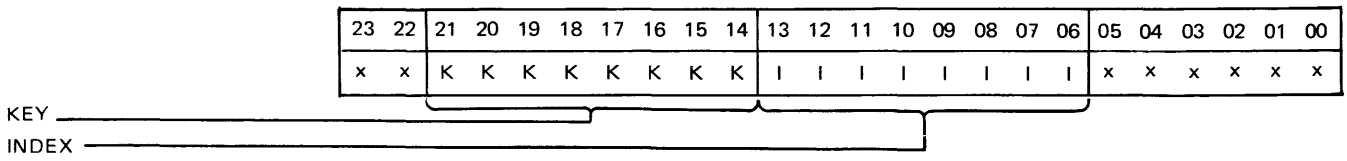
7E Read/Write Cache



Data is moved to or from Cache memory as specified by the variant selected. Diagnostic variants are described in the following paragraphs.

VARIANT 100: DIAGNOSTIC CACHE WRITE BLOCK A

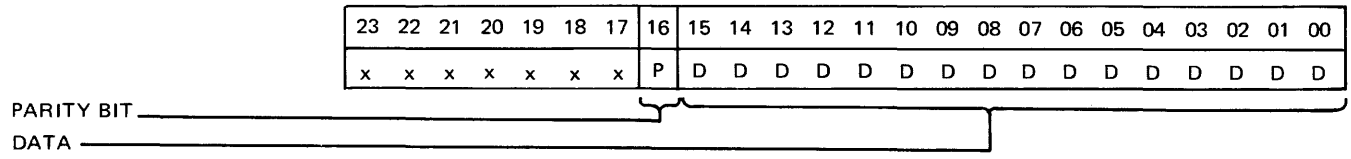
The contents of the X, Y, T, and L registers are written into block A of Cache at the addresses specified by the contents of FA. The FA address format is as follows.



The register contents are written into Cache as follows:

X to word 0
Y to word 1
T to word 2
L to word 3

The data format for X, Y, T and L is as follows:



The parity bit is selected for an odd sum for 16 data bits plus the parity bit itself. LRU does not change.

The sequence of operations is as follows:

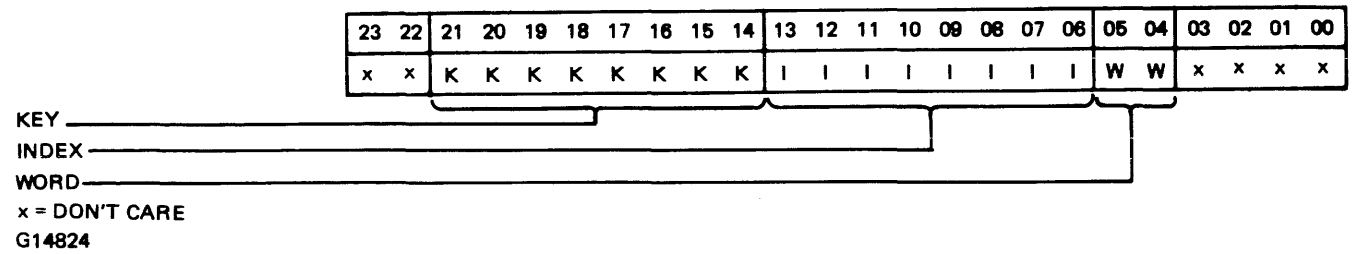
a. Save A.
b. Move the contents of FA to A.
c. Write the contents of X in Cache word 0, block A.
d. Write the "key" portion of the address in FA in the Cache key storage; set the validity bit in the key storage; generate and write parity in the key storage.
e. Write the contents of Y in Cache word 1, block A.
f. Write the contents of L in Cache word 3, block A.
g. Restore the A register.

VARIANT 101: DIAGNOSTIC CACHE WRITE BLOCK B

This operation is the same as for variant 100, except that the data is written into block B.

VARIANT 110: DIAGNOSTIC CACHE READ DATA

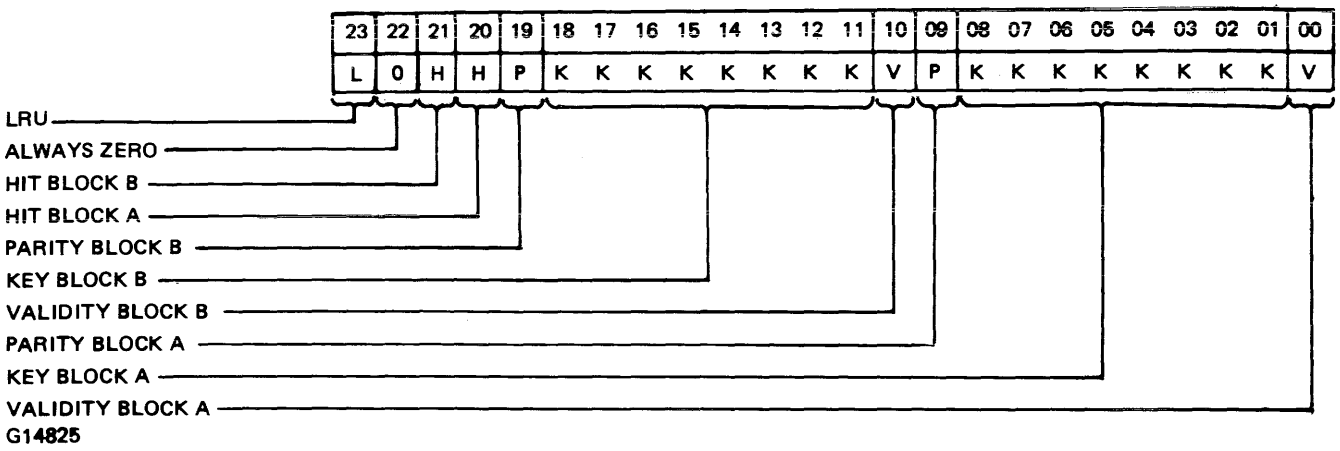
One word is read from Cache at the address specified by the contents of FA. The read data is moved to the X register. The FA address format is as follows.



An associative read is performed. The read occurs if the validity bit is false and the keys match. The data format is the same as for the Diagnostic Cache Write, except that the parity bit is absent (the read data bypasses the M register). If there is a Miss (failure of key comparison), all zeros will be returned to X. LRU will be set to the block not selected if there is a Hit.

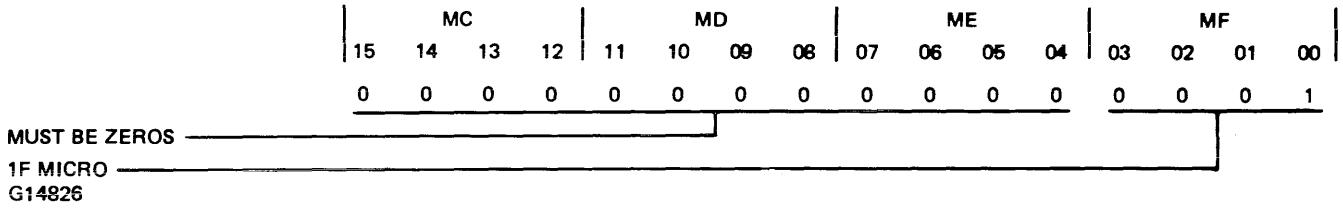
VARIANT 111: DIAGNOSTIC READ CACHE KEYS

The contents of both keys (A and B) at the specified index plus the Hit/Miss status, validity bits, and the LRU bit are read. The index address is determined by the contents of FA. The FA address format is the same as for the Diagnostic Cache Write, except that only the Index portion has significance. The data is moved to X in the following format:



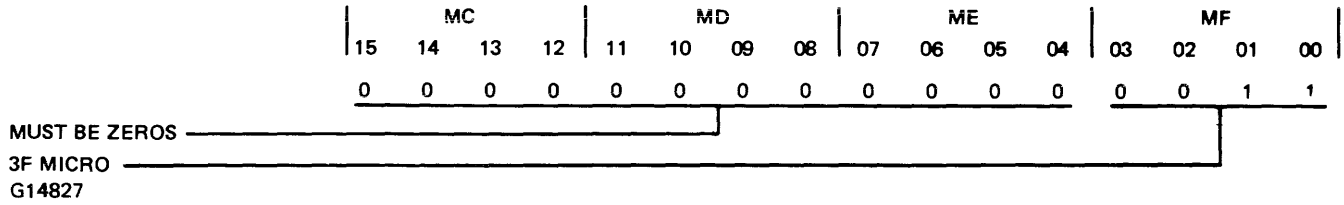
This is a non-associative read. Nothing in Cache is changed as a result of the operation. If there is a key parity error, PERP2 and CD3 are set.

1F Halt



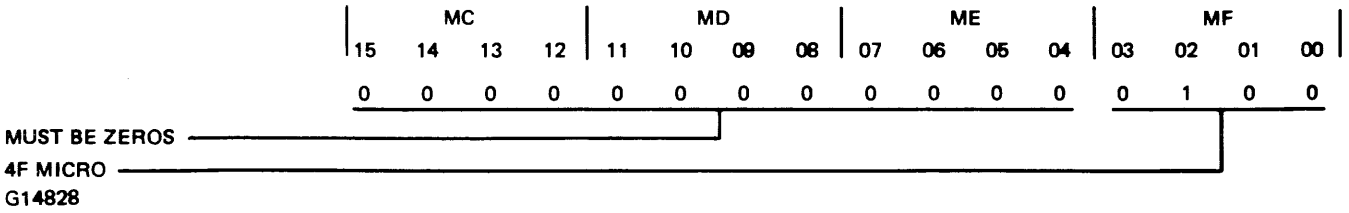
The execution of microinstructions is stopped, and the processor halts with the next micro in the M-register.

3F Normalize X



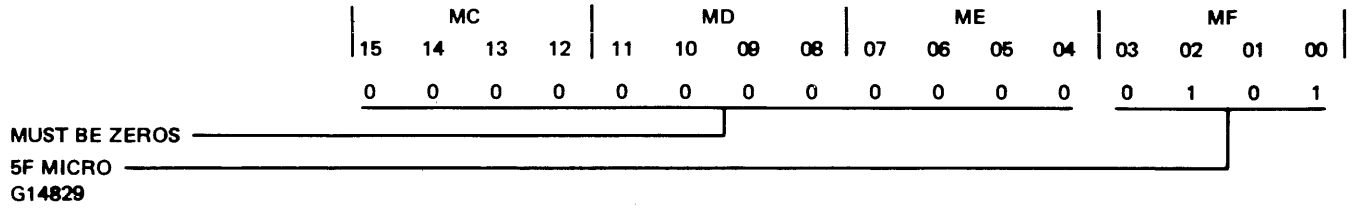
The X register is shifted left while counting FL down. This continues until FL = 0 or until the bit in X referenced by CPL = 1. Zeros are shifted into the rightmost end of Y. CPL = 1 references the rightmost bit of X, while CPL = 24 references the leftmost bits of X. CPL = 0 is undefined.

4F Bind



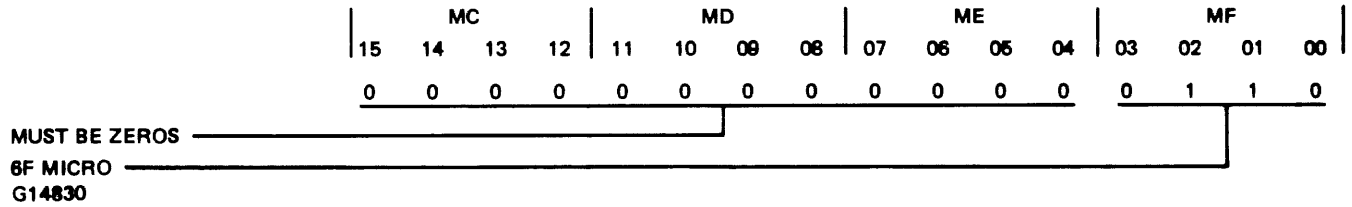
The 24-bit sum of the L register and T register contents are moved to the A register. Since A is 18 bis in length, the lower four bits and upper two bits of the sum are lost.

5F Clear Cache



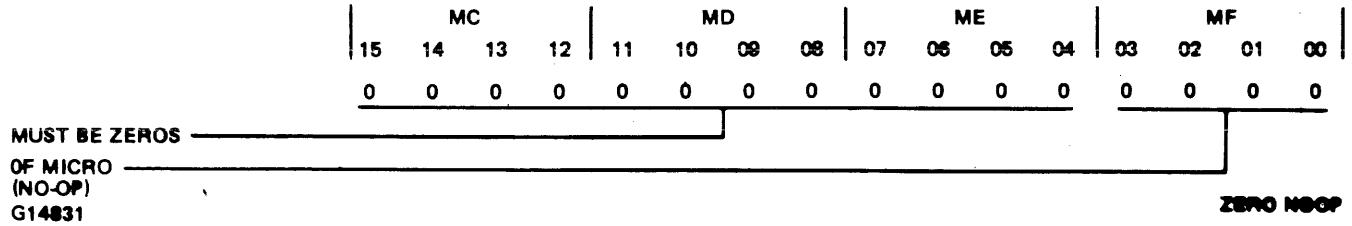
The entire Cache memory is cleared. This micro clears all key bit storage to 0, sets all validity bits to 1 and all parity bits to 0. The LRU bits are set to indicate that block B was most recently accessed; therefore the least recently used storage is block A. Actions taken regarding the micro storage portion of Cache are unspecified.

6F Increment A



The A register is incremented by 1 regardless of the processor mode of operation (A is not automatically incremented in the Tape mode).

Zero No Operation



This microinstruction specifies a skip to the next sequential instruction.

SECTION 2
INSTALLATION

GENERAL

This section describes the initial set-up and check-out procedures for the B 1870/B 1860 Central System, and provides instructions for field expansion. The information contained herein supplements the B 1870/B 1860 Planning and Installation manual (Form 1095593). To install a system, proceed as directed in the following paragraphs.

PHYSICAL PREPARATIONS FOR OPERATION

Physical preparation of the Central System involves unpacking, mechanical assembly, and making the necessary electrical connections. These procedures are described in the B 1870/B 1860 Planning and Installation Manual, FETM 1095593.

SUBASSEMBLY CHECKLIST

It is appropriate at this time that a check be performed to ensure the presence of all necessary subassemblies. Check the following items in the order listed. (Refer to figure 3-12 for orientation.)

a. Inspect the processor and I/O Base frontplane to ensure that the logic and memory cards are installed in their proper locations. Refer to figure 2-1.

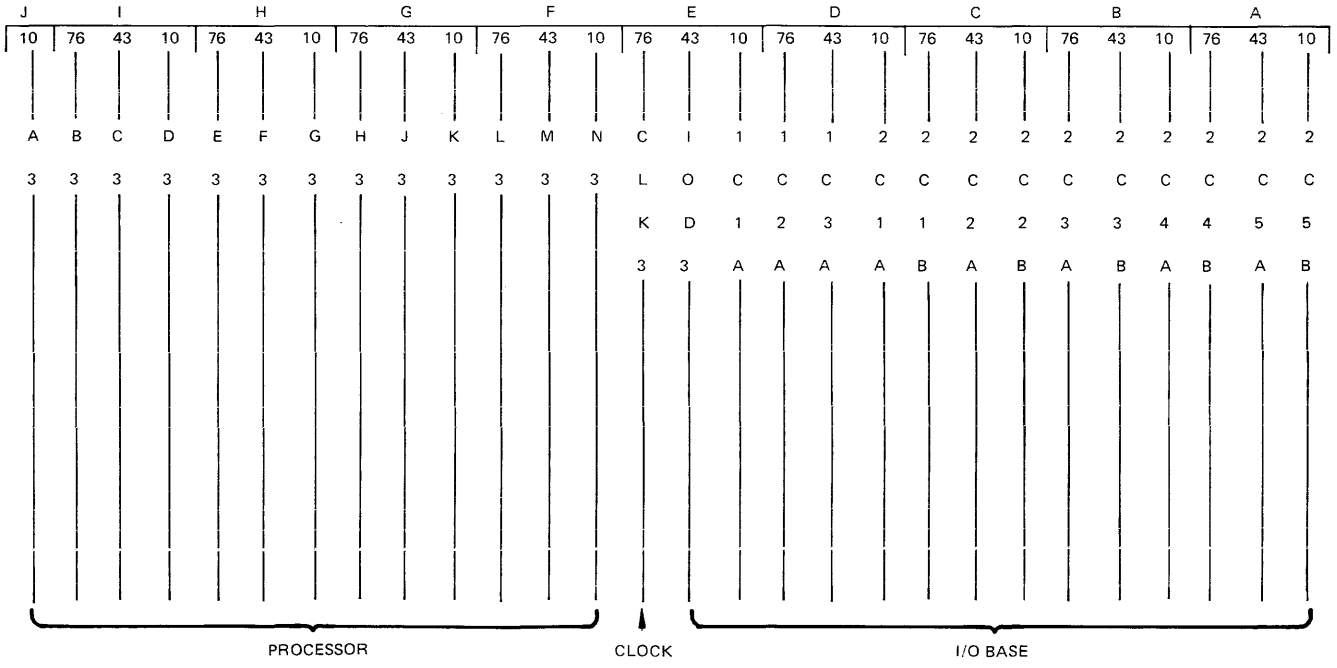
b. Inspect the memory base frontplane to ensure that the proper number of logic cards and S-memory storage cards are installed. Refer to figure 2-2.

c. Port-Connect Systems Only. Inspect the special 4-card backplane to ensure that the port interchange and port adapter cards are installed in their proper locations. Refer to figure 2-2.

d. Check to ensure that all frontplane cables are installed in their proper locations. Refer to table 2-1.

NOTE
Cables connected to the I/O controls are not shown.

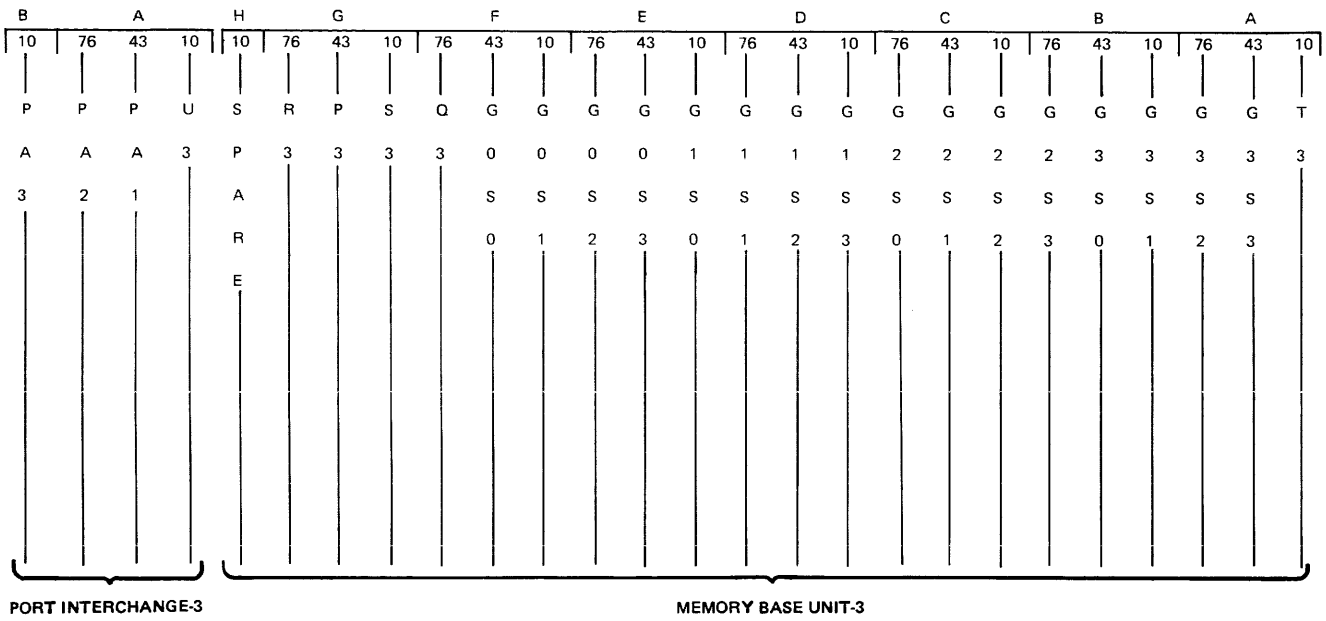
e. Check to ensure that all mechanical connections within the central system cabinet are secure, and that there are no loose wires, components, or other obvious compromises to the physical integrity of the unit.



NOTE
THE I/O CONTROLS INCLUDED WILL VARY ACCORDING TO CUSTOMER REQUIREMENTS

G14745

Figure 2-1. B 1870/B 1860 Processor and I/O Base Card Locations



NOTE
THE PORT INTERCHANGE IS OMITTED IN SYSTEMS WHICH DO NOT REQUIRE IT

G14746

Figure 2-2. Port Interchange-3 and Memory Base-3 Card Locations

Table 2-1. B 1870/B 1860 Frontplane Cable Locator

From	To
Card A3 X$	Card R3 Y#
	Card U3 Y#*
Card A3 X#	Card S3 Y#
	Card U3 X#*
Card A3 Y$	D/M Console J1
Card A3 Y#	D/M Console J2
Card E3 X$	Card F3 X$
Card E3 Y$	D/M Console J3
Card F3 X$	Card E3 X$
Card F3 X#	Card G3 X#
Card F3 Y$	Card G3 Y$
Card G3 X#	Card F3 X#
Card G3 Y$	Card F3 Y$
Card N3 Y#	Shared Cassette Board J4
Card P3 X$	Card R3 X$
Card P3 X#	Card S3 X#
Card Q3 X$	Card S3 Y$
Card Q3 Y#	Card R3 Y$
Card R3 X$	Card P3 X$
Card R3 Y$	Card Q3 Y#

From	To
Card R3 Y#	Card A3 X$
	Card S3 Y$*
Card S3 X#	Card P3 X#
Card S3 Y$	Card Q3 X$
Card S3 Y#	Card A3 X#
	Card U3 X$*
Card U3 X$	Card S3 Y#*
Card U3 Y#	Card A3 X$*
Card U3 Y$	Card R3 Y#*
Card U3 X#	Card A3 X#*
D/M Console J1	Card A3 Y$
D/M Console J2	Card A3 Y#
D/M Console J3	Card E3 Y$
D/M Console J7	Shared Cassette Board J5
Shared Cassette Board J1	Cassette No. 1 (Lower OP Panel) **
Shared Cassette Board J2	Cassette No. 2 (Upper OP panel)
Shared Cassette Board J3	Cassette Control Card 1 Y# **
Shared Cassette Board J4	Card N3 Y#
Shared Cassette Board J5	D/M Console J7

* Port Connect System Only
** When Used

CENTRAL SYSTEM OPERATIONAL CHECKOUT

When physical installation of the Central System has been completed and connection has been made to the electrical power source, an operational checkout must be made. This testing procedure is to ensure that the unit will perform as expected. The operational checkout procedure consists of the following phases:

a. Static tests (POWER OFF).
b. Static tests (POWER ON).
c. Dynamic tests.

These procedures should be performed in the order listed.

CAUTION

The Central System operational checkout concerns the processor and S-memory only. Therefore, do not connect or attempt to utilize any peripheral devices until the checkout is completed.

Static Tests (Power Off)

These tests are to ensure that the Central System will not fail due to either shorts or open circuits.

a. Make sure that both the system and source circuit breakers are in the OFF position.
b. Using a Triplett 630 VOM or equivalent, make sure that a measurable amount of resistance exists between the +4.75V, –2.0V, +12V and –12V logic supply outputs and ground.
c. Check to ensure that a measurable amount of resistance is present between each of the logic supply outputs mentioned in step b.
d. Check for continuity between the logic power supply outputs and the backplane pins listed in table 2-2.

Table 2-2. Logic Power Continuity Test

Voltage	Backplane Pin(s)	Card(s)
+4.75V	OAX, IAX	All logic cards.
- 2.0V	OZX, 1ZX	All logic cards.
GND	IDX, 1JX, 1QX, 1WK	All logic cards.
+12.0V	1LY	I/O Control cards only.
- 12.0V	OZX, 1AY	All logic cards.

Static Tests (Power On)

These tests are performed to ensure that the basic conditions for proper system operation are present, and that those parameters which are adjustable are set to the proper values. The power-on Static tests involve three major areas within the system:

a. Power Supplies
b. Clock Circuits
c. Console.

This testing is performed by manipulation of the console controls. For further information on use of the console controls, refer to section 1 of this manual.

Powering Up

Apply power to the system as follows:

CAUTION

Prior to powering up, ensure that the retaining plate for the power supply swing arms is in place; if not, this arm will contact the lower bus board and destroy the –2V supply.

a. Place both the source and system circuit breakers in the ON position.
b. Switch POWER to ON. The POWER switch is located beneath the console table, on the left pedestal.

If power is applied, the ON lamp lights, the blowers start, and some of the console lights may flicker. If not, refer to section 4 of this manual.

Power Supply Tests

When the system has been successfully powered up, check the output voltages of the logic power supply. The proper voltages are shown in table 2-3.

NOTE

Supply voltages are measured on the backplane.

Table 2-3. System Operating Voltages

Voltage Output	Nominal Voltage	Tolerance
+4.75V	+4.95V	±0.010V
- 2.0V	- 2.15V	±0.010V
+12.0V	+12.00V	±0.10V
- 12.0V	- 12.00V	±0.10V

Clock Circuit Tests

Perform the Clock Circuit Adjustment Procedure outlined in section 5 (Adjustments), taking corrective action only if the measured signals fail to meet specifications.

Console Tests

Before operation under program control is attempted, it is desirable to verify that all operational functions and capabilities of the Central System logic are working correctly and are accessible.

Perform the following tests in order listed, using the following Test Execution procedures.

TEST EXECUTION PROCEDURE

a. Press the CLEAR pushbutton.
b. Place the REGISTER SELECT rotary switch in the designated position.
c. Place the REGISTER GROUP rotary switch in the designated position.
d. Set the 24 console switches to the required value (expressed in hexadecimal).
e. Press ther LOAD pushbutton.
f. Follow the Special Instructions specified for the test.

Card Test 1

Verify the ability to load all registers in the Register Select 2 grouping. Set the following controls as indicated:

a. Press CLEAR
b. REGISTER SELECT rotary switch = 2
c. REGISTER GROUP rotary switch = X
d. Toggle switches = FFFFFF (all "up")
e. Press the LOAD pushbutton.

After each depression of the LOAD pushbutton, rotate the REGISTER GROUP switch clockwise one position, until one revolution is completed. The test results are shown in table 2-4.

Table 2-4. Register Loading Test Results

Register Group	Indicator Lights
X	FFFFFF
Y	FFFFFF
T	FFFFFF
L	FFFFFF
A	3FFFF0
M	--FFFF
BR	FFFFFF
LR	FFFFFF
FA	FFFFFF
FB	FFFFFF
FL	--FFFF
TAS	No Change (source only)
CP	----FF
NULL	000000
DATA	000000
CMND	000000
TIME	Counts up (continuously)

- = don't care.

Test 2

Verify the ability to change all registers in the REGISTER SELECT 2 grouping.

a. Press CLEAR.
b. REGISTER SELECT rotary switch = 2.
c. REGISTER GROUP rotary switch = X.
d. Toggle switches = 000000 (all "down").
e. Press the LOAD pushbutton.

Each time the LOAD pushbutton is pressed, rotate the REGISTER GROUP switch one position clockwise until one revolution is completed. The test results are shown in table 2-5.

Table 2-5. Register Change Test Results

Register Group	Indicator Lights
X	000000
Y	000000
T	000000
L	000000
A	--0000
M	--0000
BR	000000
LR	000000
FA	000000
FB	000000
FL	--0000
TAS	No change (source only)
CP	----00
NULL	000000
DATA	000000
CMND	000000
TIME	Counts up (Continuously)

Test 3

Verify the ability to address the T and L registers in 4-bit increments.

a. Press CLEAR.
b. REGISTER SELECT rotary switch to 2.
c. REGISTER GROUP rotary switch to T.
d. Toggle switches to ABCDEF (10, 11, 12, 13, 14, 15).
e. Press LOAD.
f. REGISTER GROUP rotary switch to L.
g. Press LOAD.

Next, set the following switches:

a. REGISTER SELECT rotary switch to 0
b. REGISTER GROUP rotary switch from TA through LF, disregarding the contents of CA and CB. The expected results are shown in table 2-6.

Table 2-6. T and L Register Test Results

Register Group	Indicator Lights
TA	00000A
TB	00000B
TC	00000C
TD	00000D
TE	00000E
TF	00000F
LA	00000A
LB	00000B
LC	00000C
LD	00000D
LE	00000E
LF	00000F

Test 4

Verify the ability to address registers CA, CB, CC, and CD as either four-bit sources or destinations.
a. Press CLEAR.
b. REGISTER SELECT rotary switch to 0.
c. REGISTER GROUP rotary switch to CA.
d. Toggle switches to 00000F.
e. Press LOAD.
f. Rotate the REGISTER GROUP rotary switch clockwise one position.
g. Press LOAD.
h. Repeat steps f and g until the REGISTER GROUP rotary switch is at TE.
i. Set the REGISTER GROUP rotary switch to CA.
j. Toggle switches = 000000.
k. Repeat steps e, f, g, and h.

The test results are shown in table 2-7.

Table 2-7. C Register Test Results

Toggle Switches = 00000F	Toggle Switches = 000000
CA = 00000F	CA = 000000
CB = 00000F	CB = 000000
CC = 00000F	CC = 000004*
CD = 000008	CD = 000000

* Real Time Clock Interrupt sets CC2.

Test 5

Verify the ability to address the FB register in four-bit increments.
a. Press CLEAR.
b. REGISTER SELECT rotary switch = 2.
c. REGISTER GROUP rotary switch = FB.
d. Toggle switches = ABCDEF.
e. Press LOAD.

Next set the following controls as indicated:
a. REGISTER SELECT rotary switch = 1.
b. REGISTER GROUP rotary switch: rotate 1 position at a time from FU to FLF.

The test results are shown in table 2-8.

Table 2-8. FB Register Test Results

Register Group	Indicator Lights
FU	A
FT	B
FLC	C
FLD	D
FLE	E
FLF	F

Test 6

NOTE
In tests 6 through 11, the X and Y conditions are checked. Performing these tests verifies that the basic logic of the ALU is functioning properly.

Verify that X = Y when X and Y are set to 0.
a. Press CLEAR.
b. Set X and Y registers to 0.
c. REGISTER SELECT rotary switch = 1.
d. REGISTER GROUP rotary switch = XYCN (X and Y conditions).

No further action is needed. The results will appear on the indicator lights, and should be 000004 (bit 3 of XYCN register true) which indicates that X=Y.

Test 7

Verify that X > Y when the contents of the X register are greater than those of the Y register. Set the following controls as indicated:

a. Press CLEAR.
b. Set Y register to 0.
c. REGISTER SELECT rotary switch = 2.
d. REGISTER GROUP rotary switch = X.
e. Toggle switches = 000001.
f. Press LOAD.
g. REGISTER SELECT rotary switch = 1.
h. REGISTER GROUP rotary switch = XYCN.

The results should be 000001 (X > Y).

Test 8

Verify that X < Y when the contents of the X register are less than those of the Y register.

a. Press CLEAR.
b. Set X register to 0.
c. REGISTER SELECT rotary switch = 2.
d. REGISTER GROUP rotary switch = Y.
e. Toggle switches = 000001.
f. Press LOAD.
g. REGISTER SELECT rotary switch = 1.
h. REGISTER GROUP rotary switch = XYCN.

The results should be 000002 (X < Y).

Test 9

Detect the most significant bit of X (MSBX).

a. Press CLEAR.
b. REGISTER SELECT rotary switch = 2.
c. REGISTER GROUP rotary switch = X.
d. Toggle switches = 800000.
e. Press LOAD.
f. REGISTER GROUP rotary switch = CP.
g. Toggle switches = 000018.
h. Press LOAD.
i. REGISTER SELECT rotary switch = 1.
j. REGISTER GROUP rotary switch = XYCN.

The results should be 000009 (MSBX and X > Y).

Test 10

Verify that the X register not equal to 0 (X NEQ 0) and not least significant unit of X (LSUX) true may be detected.

a. Press CLEAR.
b. REGISTER SELECT rotary switch = 2.
c. REGISTER GROUP rotary switch = X.
d. Toggle switches = 000001.
e. Press LOAD.
f. REGISTER GROUP rotary switch = Y.
g. Toggle switches = 000000.
h. Push the LOAD pushbutton.
i. REGISTER SELECT rotary switch = 1.
j. REGISTER GROUP rotary switch = XYST.

The results should be 00000D (X unequal to 0, LSUX and INT OR).

Test 11

Verify that Y register not equal to 0 (Y NEQ 0) may be detected.

a. Press CLEAR.
b. REGISTER SELECT rotary switch = 2.
c. REGISTER GROUP rotary switch = Y.
d. Toggle switches = 000001.
e. Push the LOAD pushbutton.
f. REGISTER SELECT rotary switch = 1.
g. REGISTER GROUP rotary switch = XYST.

The results should be 000006 (Y unequal to 0 and INT OR).

Test 12

Verify the ability to address the CP and CPU register as a sink.

a. Press CLEAR to set CP to zero.
b. REGISTER SELECT rotary switch = 1.
c. REGISTER GROUP rotary switch = CPU.
d. Toggle switches = 000003.
e. Press LOAD.
f. REGISTER SELECT rotary switch = 2.
g. REGISTER GROUP rotary switch = CP.

Results should be 000060 (CPU is bits 5 and 6 of CP).

Test 13

NOTE

Tests 13, 14, 15, and 16 check the ability to read and write into memory from the console.

Verify that the A register is incremented when the INC pushbutton is pressed.

a. Press CLEAR pushbutton.
b. REGISTER SELECT rotary switch = MEMORY MODE.
c. REGISTER GROUP rotary switch = CMR.
d. Press the INC pushbutton seven times.
e. REGISTER SELECT rotary switch = 2.
f. REGISTER GROUP rotary switch = A.

Results should be 000070. (Each increment of A is binary weight 16.)

NOTE

The A register may be incremented only when CAW, CBW, CMR, or CKR is selected.

Test 14

Verify that 16 bits may be written into Cache Memory at Block A Address Zero (0).

a. Press CLEAR.
b. REGISTER SELECT rotary switch = 2.
c. REGISTER GROUP rotary switch = A.
d. Toggle switches = 000000.
e. Press LOAD. (This action clears A.)
f. REGISTER SELECT rotary switch = MEMORY MODE.
g. REGISTER GROUP rotary switch = CAW (Cache Block A Write).
h. Toggle switches = FFFFFF (Write Data).
i. Press LOAD.
j. REGISTER GROUP rotary switch = CMR (Cache Memory Read).
k. Press LOAD.

The result should be 00FFFF.

Test 15

Verify that the FA register is incremented when SR (S-Memory Read) or SW (S-Memory Write) is selected and the INC pushbutton is pressed.

a. Press CLEAR.
b. REGISTER SELECT rotary switch = 2.
c. REGISTER GROUP rotary switch = FA.
d. Toggle switches = 000000.
e. Press LOAD. (This action clears FA.)
f. REGISTER SELECT rotary switch = MEMORY MODE.
g. REGISTER GROUP rotary switch = SR16 (S-Memory Read 16 Bits).
h. Press INC once.
i. REGISTER SELECT rotary switch = 2.
j. REGISTER GROUP rotary switch = FA.

Result should be 000010 (FA increments by binary weight 16 each time INC is pressed).

NOTE
FA will increment when REGISTER SELECT is in SR or SW.

Test 16

Verify that 24 bits may be written into S-memory at address 0.

a. Press CLEAR.
b. REGISTER SELECT rotary switch = 2.
c. REGISTER GROUP rotary switch = FA.
d. Toggle switches = 000000 (Address).
e. Press LOAD. (This selects address 0.)
f. REGISTER SELECT rotary switch = MEMORY MODE.
g. REGISTER GROUP rotary switch = SW24 (S-Memory Write 24 Bits).
h. Toggle Switches = FFFFFF (Write Data).
i. Press LOAD.

Result should be 000000 (write data is not displayed).

NOTE
Any memory address may be used for Tests 16 and 17.

Test 17

Read the 24 bits that have been written in memory (starting at memory address 0).

a. Press CLEAR.
b. REGISTER SELECT rotary switch = MEMORY MODE.
c. REGISTER GROUP rotary switch = SR24 (S-Memory Read 24 Bits).
d. Toggle switches = 000000.
e. Press LOAD.

Results should be FFFFFF.

Dynamic Tests

Once it has been determined that the basic central system functions may be implemented under manual control, tests under program control can begin. The dynamic tests consist of software routines that exercise the processor and memory with sequences of microinstructions. The tests are arranged to check out the various portions of the logic against known proper responses, and to indicate error conditions by way of halt interrupts, and bit patterns stored in various registers. Note that these same tests are also used for maintenance purposes.

The following are dynamic tests for proving the operational integrity of the Central System:

a. MTR Mode Processor test.
b. Dynamic Processor test.
c. Port Interchange-3 test (for systems employing a port interchange).
d. Dynamic S-memory test.
e. Dynamic Cache test.

Each of these programs is contained in a cassette tape, and is loaded into the machine by way of the console cassette tape reader. Some are executed directly from the tape, while others are loaded into S-memory for execution. It is recommended that the above tests be run in the sequence listed. Refer to section 4 of this manual for directions on how to use the test routines.

S-MEMORY EXPANSION

The B 1870/B 1860 S-memory is modular, and may be expanded in increments of 64K bytes from 64K bytes to 512K bytes. Electrically, S-memory is strappable in 32K byte increments.

S-memory is configured from S-memory card groups which are contained within a memory base unit. Each S-memory card group consists of four storage cards, each containing a maximum of 128K bytes storage. Four card groups (maximum) may be installed in the memory base unit, for a storage capacity of 512K bytes.

Parts

Increasing the size of S-memory requires that the appropriate number of storage card groups (four cards each) be ordered. The card groups (M&E 2565 0589 are installed as shown in figure 2-2.

Since only one memory base unit is employed and all power for the memory is derived from the system logic supply, the only parts required for an expansion of memory are the storage cards themselves.

NOTE
The installation of additional storage cards may cause the existing logic supply current delivery capacity to be exceeded. Refer to the B 1870/B 1860 Planning and Installation Manual (form number 1095593) for current draw calculation data. If the expansion creates an overload, the addition of a Logic Power Supply Booster Kit-3 (P/N 2212 9027) is required. This device increases the logic supply current capacity by 80 amperes (+4.75 and –2.0 Volt outputs).

Detailed information on S-memory installation procedures is provided in the Test and Field (T&F) documentation for the B 1870/B 1860 processor.

SECTION 3
DOCUMENTATION AND COMPONENTS

GENERAL

To assist the field engineer in performing maintenance work, a number of publications and diagnostic programs have been produced. These include documentation which is part of the system, and other data which is available for reference purposes.

EQUIPMENT DOCUMENTATION

Each system when assembled is furnished with a basic issue of Test and Field documentation. Included are schematics and logic diagrams for all portions of the system, Assembly Drawings, a Backplane Circuit List, Diagnostic Program listings, Card Test Data, and a Hardware Rules Book. Since these documents are used extensively during maintenance operations, a guide to the use of each is provided.

Logic Schematics

The B 1870/B 1860 Logic Schematics are used to present a graphic representation of the circuits which make up the system. In order to create documents of a practical physical size, it was necessary to sectionalize the schematics. The sections thus produced follow the physical rather than electrical divisions of the system, with each individual schematic representing one of the logic cards. Where necessary to avoid crowding, several sheets are used to show the circuits on a single card.

Schematic Rules

To present a uniform appearance and avoid confusion, all schematics conform to a predetermined set of rules. Briefly, the rules for schematic layout are as follows:

a. Schematics depict the logic contained on a single card, and may consist of one or more pages.

b. Logic flow is left to right.

c. Signal connections may be either unidirectional or bidirectional as circuit requirements dictate, but must be identified as such.

d. Unidirectional signals entering a card by way of frontplane connectors will enter the schematic at the top of the page.

e. Unidirectional signals leaving a card by way of frontplane connectors will leave the schematic at the bottom of the page.

f. Bidirectional signals using frontplane connectors may appear at either the top or bottom of the page.

g. Backplane and interpage input signals will enter the page from the left.

h. Backplane and interpage output signals will exit the page to the right.

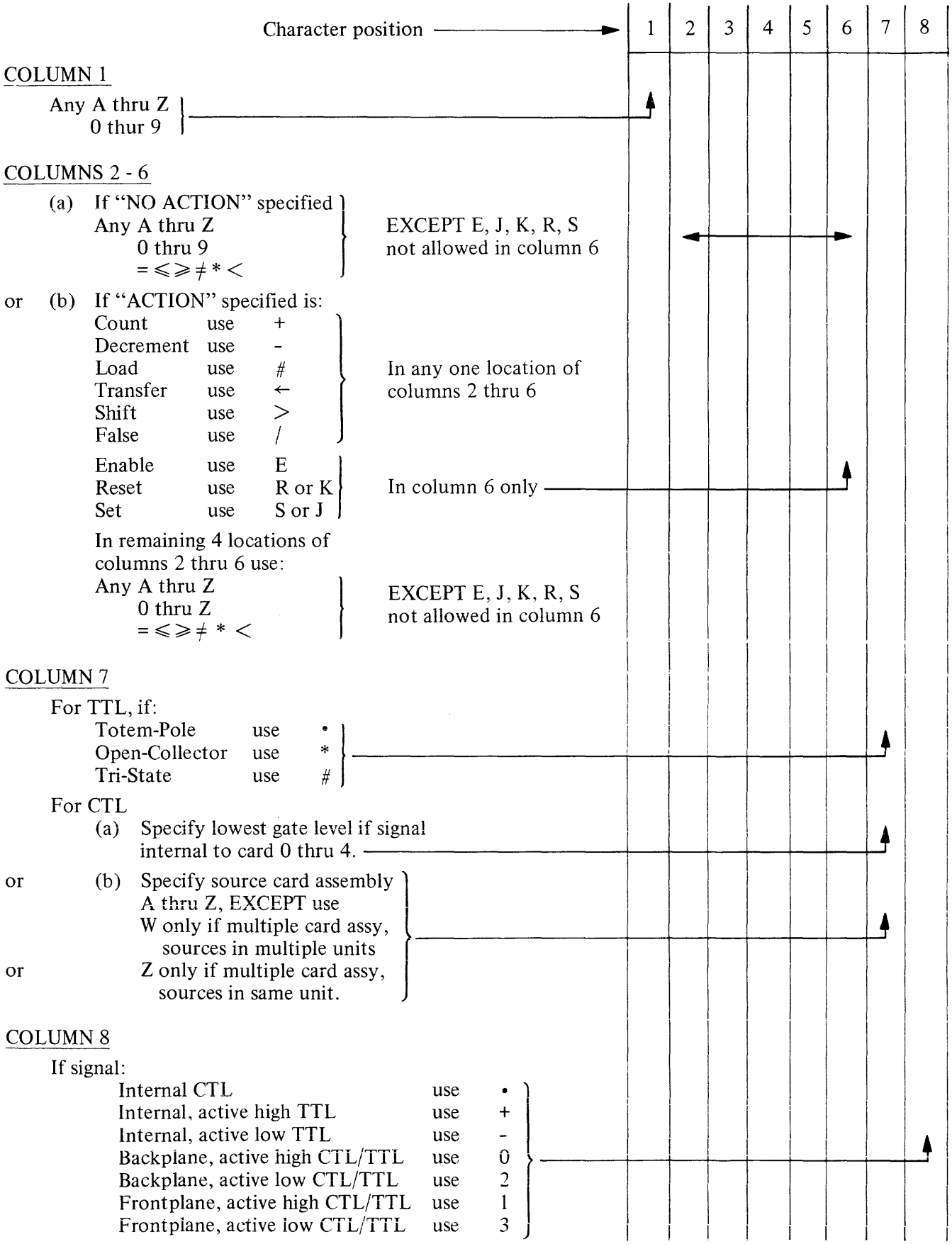
Signal Names (Mnemonics)

To aid in understanding circuit functions, and to simplify tracing signals through the various logic sections, the output of each active device has been assigned a mnemonic name. The mnemonic comprises an abbreviated description of the purpose and location of the signal it is associated with. Mnemonics consist of eight characters, and are composed of letters, digits, special symbols, and spaces. The rules applying to the composition of mnemonics are summarized in table 3-1.

Schematic Connection Symbols

To alleviate crowding and improve legibility, logic circuit schematic diagrams are drawn in a multiple-page format. To indicate the various types of connections which can exist between pages, and to differentiate between physical and graphical circuit divisions, a system of symbolic notation was created. The schematic connection symbols consist of internal page symbols, backplane pin symbols, frontplane pin symbols, inter-page symbols, and special symbols. Each type is discussed separately in the following subsections.

Table 3-1. Mnemonic Signal Name Rules



INTERNAL PAGE SYMBOLS

Figure 3-1 illustrates internal page symbols. A numeral directly to the right of any of these symbols designates the numbers of places that the signal goes to on a particular page.

BACKPLANE PIN SYMBOLS

Backplane pins are identified by a three-character code which describes their location. The meaning of the characters is as follows (example: OAX).

O = Component side of logic card (1 = solder side).

A = First pin of group. (Pins are numbered A-Z, with O being omitted.)

X = Upper half of card (Y = lower).

Backplane pin codes are listed to the left of an input signal, and to the right of an output signal. Refer to figure 3-2.

FRONTPLANE PIN SYMBOLS

Frontplane pins are identified in a manner similar to backplane pins, except that the pin groups are stacked vertically rather than being on opposite sides of the card. Since the same number of pins (100) as the backplane is possible, this means that two groups per card half are required. The locations are identified as follows (example, $NY):

$ = Upper group on card half (# = lower group).

N = 12th pin of group. (Pins are numbered A-Z, omitting O).

Y = lower half of card (X = upper half).

Frontplane pin codes are listed above input signals, and below output signals. Refer to figure 3-3.

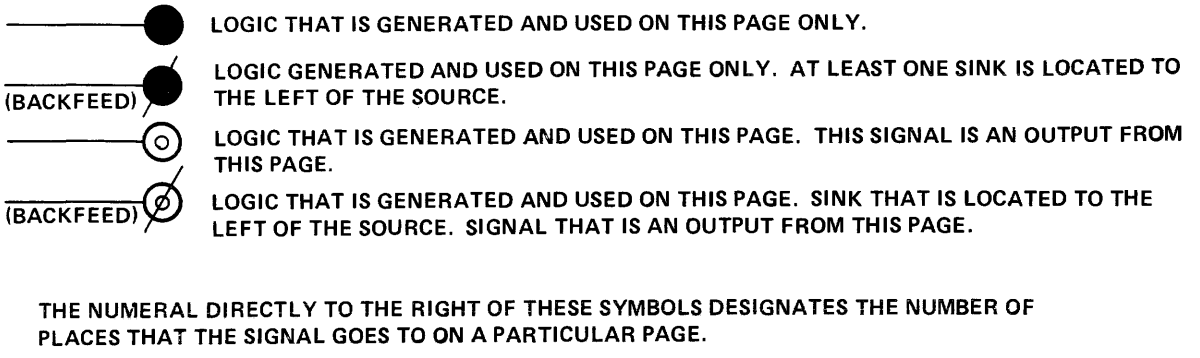
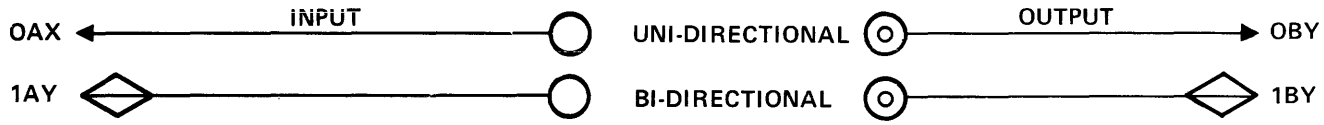


Figure 3-1. Schematic Internal Page Symbols



BACKPLANE PINS ARE LABELED A THROUGH Z WITH THE LETTER O BEING OMITTED. BACKPLANE PINS ARE LISTED TO THE LEFT OF AN INPUT SIGNAL, AND TO THE RIGHT OF AN OUTPUT SIGNAL.

G11510

Figure 3-2. Schematic Backplane Pin Symbols

FRONTPLANE PINS ARE LABELED A THROUGH Z WITH O BEING OMITTED.

G11511

Figure 3-3. Schematic Frontplane Pin Symbols

INTER-PAGE SYMBOLS

Where to or more schematic pages are needed to depict the logic circuitry on a single card, inter-page connection symbols are used to indicate through-connections. Since no pin connections are involved, only the schematic page number(s) associated with that signal are shown. Refer to figure 3-4.

Special Symbols

A triangle placed perpendicular to an output signal line (example: H4G) indicates that a pull-down or load resistor is connected to this circuit. The accompanying code number shows the chip location and pin where this resistor is located.

An inverted triangle placed on an output line (example: F9B) indicates a 150-ohm load resistor to ground on the solder side of the board. The code number shows the pin location to which the resistor is tied.

Hardware Rules Book

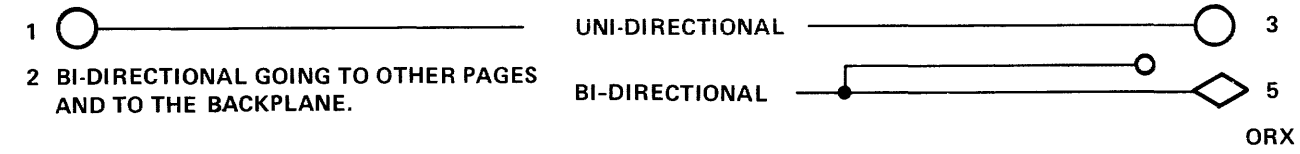
The integrated circuit elements employed in the B 1870/B 1860 systems are identified by a special designator code. The code is the same as that used for B 1700 series systems, and serves as an abbreviated specification for commonly used devices. Since the system, for the most part, consists of a limited number of individual IC types, it is practical to compile detailed information concerning them in a single reference publication. This publication is known as the B 1700 Hardware Rules Book (Part Number 2209 6150), and is an essential part of the system documentation.

The Hardware Rules Book is arranged in alphabetical order by code designator, with the designators assigned in a manner roughly approximating abbreviated device operational functions. Device designator codes consist of four characters, the first two of which are always alphabetical. The third character can be a letter or a number, depending upon whether one or more devices with the same general function (but with minor individual differences between them where there are two or more) exist. The last character of the code always appears as an N (meaning "number") in the references. Often such devices are packaged two or more to a chip, requiring that numbers be assigned to distinguish between them in actual applications. Such numbers appear only in the Logic Schematics and discussions which refer to them. Several examples of circuit element designator codes follow:

Designator Code	Chip Function
AFAN	Adder/Subtractor
CFAN	Comparator
FFAN	Flip-Flop
LFAN	Latch
RFAN	3-Bit Register

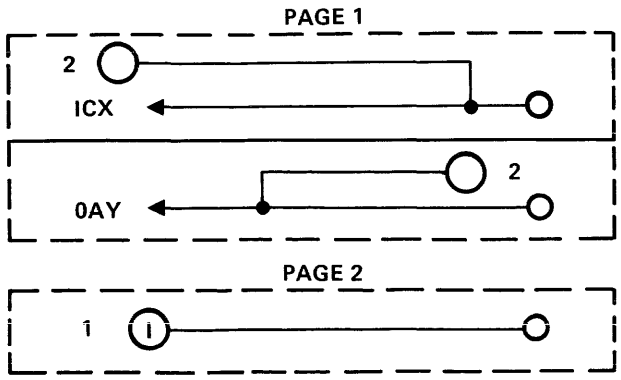
Backplane Circuit Lists

For each portion of the system which uses a wire-wrap backplane for interconnection of the plug-in logic cards, a Backplane Circuit List is provided. This is a complete listing, by signal name and pin numbers, of all point-to-point connections on the backplane itself. The listing serves to complement the schematics, providing a means of tracing wiring circuits external to the logic cards.



THE NUMBER TO THE LEFT OF AN INPUT SIGNAL DESIGNATES THE PAGE WHERE THE SIGNAL ORIGINATED.

THE NUMBER TO THE RIGHT OF AN OUTPUT SIGNAL REFERENCES THE PAGE OR PAGES WHERE THAT SIGNAL IS USED.



LOGIC GENERATED ON PAGE 2 IS OR-ED WITH BACKPLANE INPUTS ON PAGE 1.

AN INPUT FROM THE BACKPLANE ON PAGE 1 WHERE THE LOGIC IS USED. IT IS ALSO USED ON PAGE 2 WHERE THE INPUT SIGNAL WILL CONTAIN AN (I).

THIS SYMBOL SIGNIFIES THAT THE INPUT IS A BACK-PLANE PIN INPUT TO PAGE 1.

G11512

Figure 3-4. Schematic Inter-Page Connection Symbols

Card Test Data

One of the several means available for trouble-shooting the central system is use of the Logic Card Tester. This device provides an external means of exercising the circuit elements of any desired logic card. Cards so tested are subjected to an individual routine which is designed to produce a predictable set of responses. The results of the tests, known as "node counts," are compared with published specifications, thus serving as a means for detecting malfunctioning circuitry. The card test data serves as a guide to the use of the Card Tester, providing both set-up instructions and expected results. A separate section is provided for each logic card included in the system.

Diagnostic Program Listing

Diagnostic Programs provide for system fault analysis through special exercising of suspected portions of the logic. Included with each such program is a listing which contains operating instructions and result analysis data. Refer to the Diagnostic Programs discussion in section 4 for further information.

GENERAL SYSTEM COMPONENT AND SUBSYSTEM REFERENCES

The following data is to be used for general reference purposes during maintenance work. Included are directions for locating and/or identifying components, connections, pins and other portions of the hardware.

Integrated Circuit Chips

The integrated circuit chips employed in the B 1870/B 1860 system are of the 14-, 16-, and 18-pin dual in-line package type. The individual chip pins are assigned identifying letters as shown in figures 3-5, 3-6, and 3-7. Certain pins in all dual in-line chips are reserved (dedicated) for the following specific purposes.

Pin E:	Ground
Pin M:	+4.95V
Pin L:	–2.15V

Otherwise, the individual types of chips vary greatly as to pin connections. For further information on chip types and functions, refer to the B 1700 Hardware Rules book, form A2209 6150A.

B 1870/B 1860 LOGIC CARDS

Circuit logic for the B 1870/B 1860, including the Processor, S-memory, the I/O Base and individual I/O controls, is physically packaged on pluggable circuit cards. The logic cards are uniform in overall configuration, and have the following characteristics:

a. 14-1/2" long by 12-1/2" high, with etching on both sides.

b. Maximum capacity is 120 integrated circuit chips.

c. All chips are located on the same side of the card, which is known as side 0.

d. Solder connections and some discrete components are located on the opposite side (side 1).

14 PIN CHIP

SEVEN PINS ON EACH SIDE OF THE CHIP. ONE SIDE IS LETTERED A THROUGH G, THE OTHER SIDE IS LETTERED H THROUGH P WITH THE LETTERS I AND O BEING OMITTED.

G11514

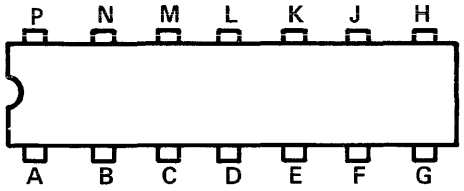


Figure 3-5. 14-Pin Chip

16 PIN CHIP

THE 16 PIN CHIP IS SIMILAR TO THE 14 PIN CHIP EXCEPT FOR THE ADDITION OF PIN R AND PIN S.

G11515

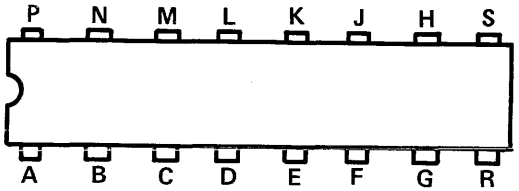


Figure 3-6. 16-Pin Chip

18 PIN CHIP

THE 18 PIN CHIP IS SIMILAR TO THE 16 PIN CHIP EXCEPT FOR THE ADDITION OF PIN T AND PIN U.

G11516

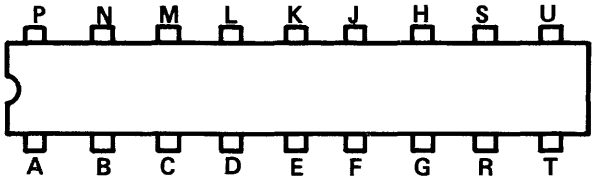


Figure 3-7. 18-Pin Chip

e. Signal connections between individual chips are made primarily by etched conductors on the card surface. Some wire-wrap type construction is also used.

f. Operating voltages and the system clock signal are distributed by way of bus-bars which are mounted perpendicular to the surface of the card, and cross it lengthwise.

g. Signal connections into and out of the cards are by way of frontplane and backplane connectors. The maximum number of connections to one card is 200, divided evenly between frontplane and backplane.

h. Clock signals are distributed to the cards by way of coaxial cables.

Chip Locations

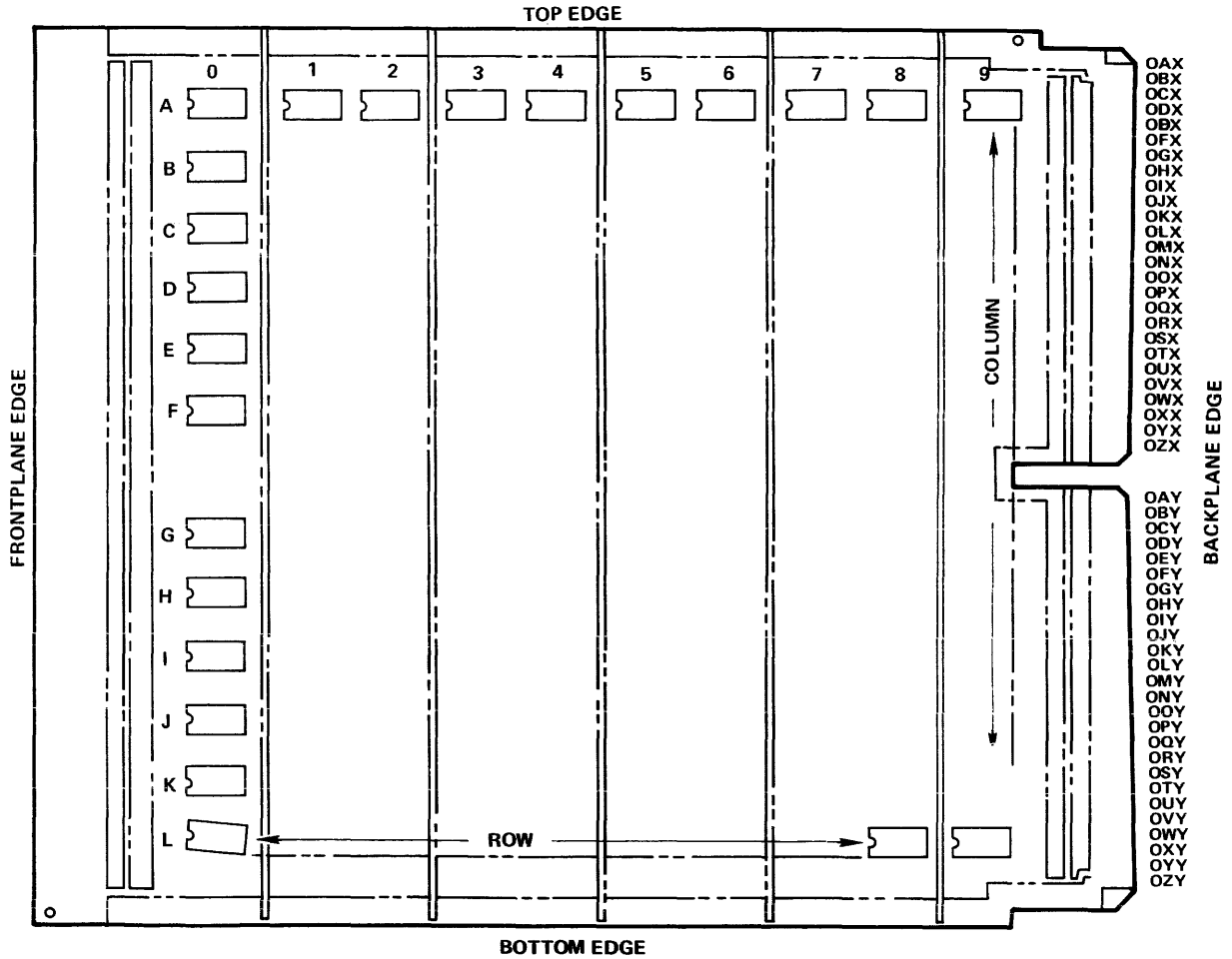
To provide a rapid, easily understood method of identifying chip positions on logic cards, a system of coordinates is employed. In this system, vertical columns of chips are assigned numbers (0 through 9) and horizontal rows are assigned letters (A through L). Thus, the identity of a chip is determined by the column and row coordinates which it occupies. These coordinates are used primarily in the card schematics. Chip location coordinates are illustrated in figure 3-8.

NOTE

The component identification system for S-memory storage cards is different from that used for the other logic cards in the system. This system is described separately below.

Pin and Connector Designations

Input/output connections are separated into several groups which correspond to physical sections of the card. To provide a distinctive method of identifying the location of a particular connection, certain conventions have been adopted. The rules differ for frontplane and backplane connections, but follow the overall scheme of identifying those located on the upper half of the card with an X, and those on the lower half with a Y.



NOTE:
THE ROW, COLUMN COORDINATE LOCATION OF A CHIP IS USED AS ITS REFERENCE DESIGNATION ON THE CARD LOGIC DIAGRAM; E.G., A CHIP LOCATED IN ROW C, COLUMN 5 HAS THE REF. DESIGNATION C5.

G11517

Figure 3-8. Logic Card Chip Location Coordinates

Backplane pins are identified with a three-character code which describes the location of the pin. Essentially, the pins are divided into four groups of 25 each, with the divisions being the upper and lower card halves, and the component (0) and solder (1) sides of the board. The location code is explained in figure 3-9.

Frontplane pins are also identified with a three-character code. However, since the frontplane connectors are all located on the component side of the board, and are four in number, a slightly different identity system is employed.

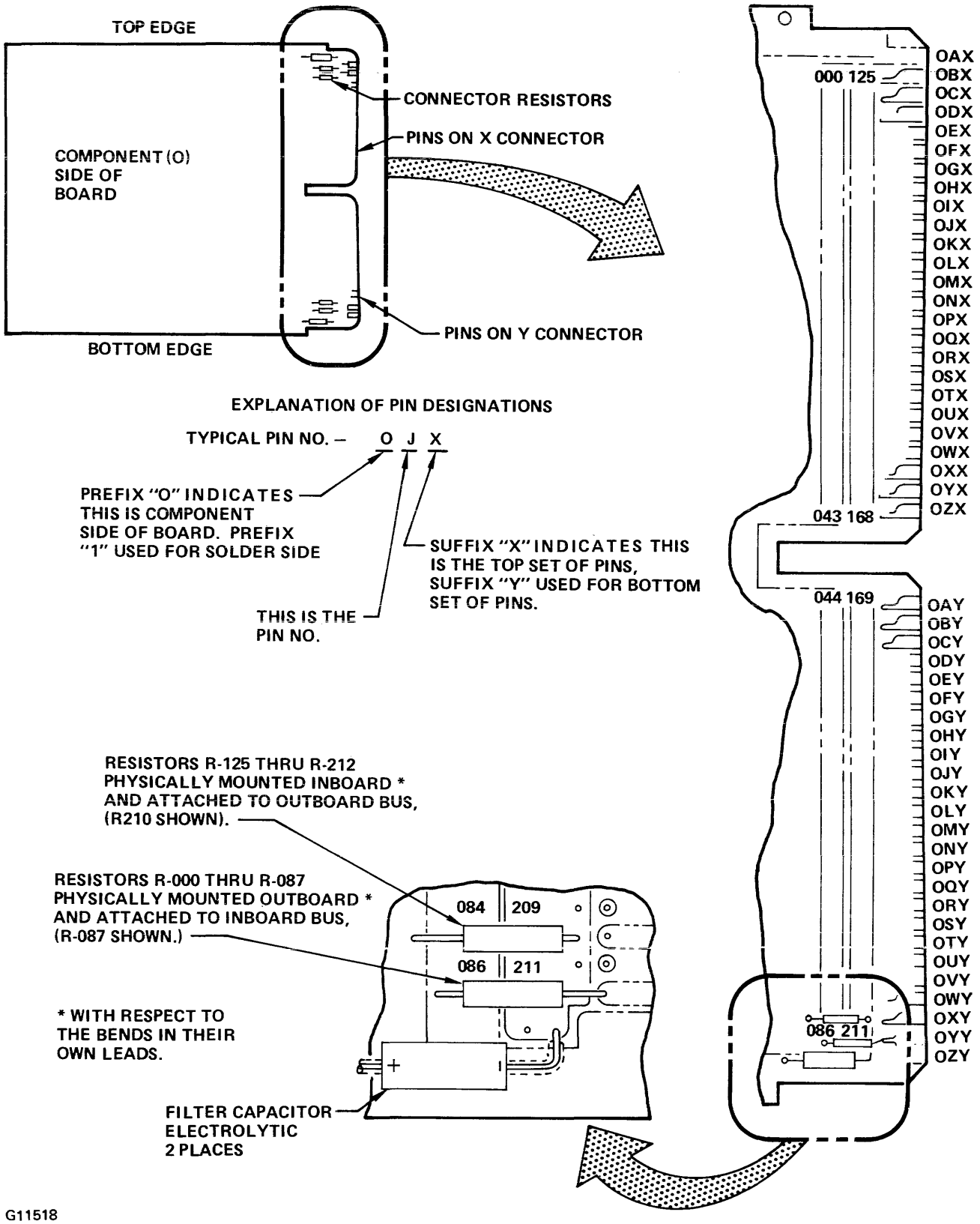


Figure 3-9. Backplane Pin and Resistor Designations

In the frontplane numbering system, the X and Y designations are retained, with an additional symbol being added to indicate position within the card half concerned. The symbols $ and # (dollar sign and pound sign) have been adopted for this purpose, with dollar sign indicating the upper connector of the X or Y group, and pound sign the lower connector. Refer to figure 3-10.

Discrete Component Locations

In addition to integrated circuit chips, discrete resistors, capacitors, and diodes are used on the logic cards.

Resistors are located in vacant chip positions (on a jumper chip or soldered directly to the card), and/or are installed adjacent to the frontplane or backplane in special locations reserved for pull-up/pull-down resistors, and/or are located on the solder side of a card between a chip pin and ground, and/or are located in resistor packs (which resemble IC chips).

Capacitors are located in vacant chip positions (on a jumper chip or soldered directly to the card), and/or are located along etched voltage distribution busses, and/or are located on the solder side of a card between a chip pin and ground.

Diodes are located in vacant chip positions (on a jumper chip or soldered directly to the card).

S-Memory Storage Cards

S-memory storage cards are similar in size and design to the logic cards, but differ in the chip-mounting configuration employed. (See figure 3-11). Essentially, the card consists of 44 columns (numbered 0-44) and 27 rows (lettered A thru Z, then AA thru AD, excluding I, O, and Q). Chip locations are identified in the same manner as with logic cards. Note that RAM storage chips are located only in columns 0 through 20 and rows A, D, H, L, R, V, Y, and AB. Fully populated cards have all four columns filled, whereas half-populated cards have chips installed only on the first two columns.

Discrete components on the S-memory storage cards may be located by way of the same coordinates that are used for the integrated circuit chips.

Central System Architecture

The various subsystems which make up the B 1870/B 1860 Central System are located within the main cabinet as shown in figure 3-12. The distribution of individual logic circuits (in the processor, port interchange, and memory base unit) is indicated alphabetically in table 3-2 which lists the circuit name, the card letter and the sheet number. (Every logic card type in these units has its own letter designation: processor A-N; port interchange, U; memory base unit, P,Q,R,S).

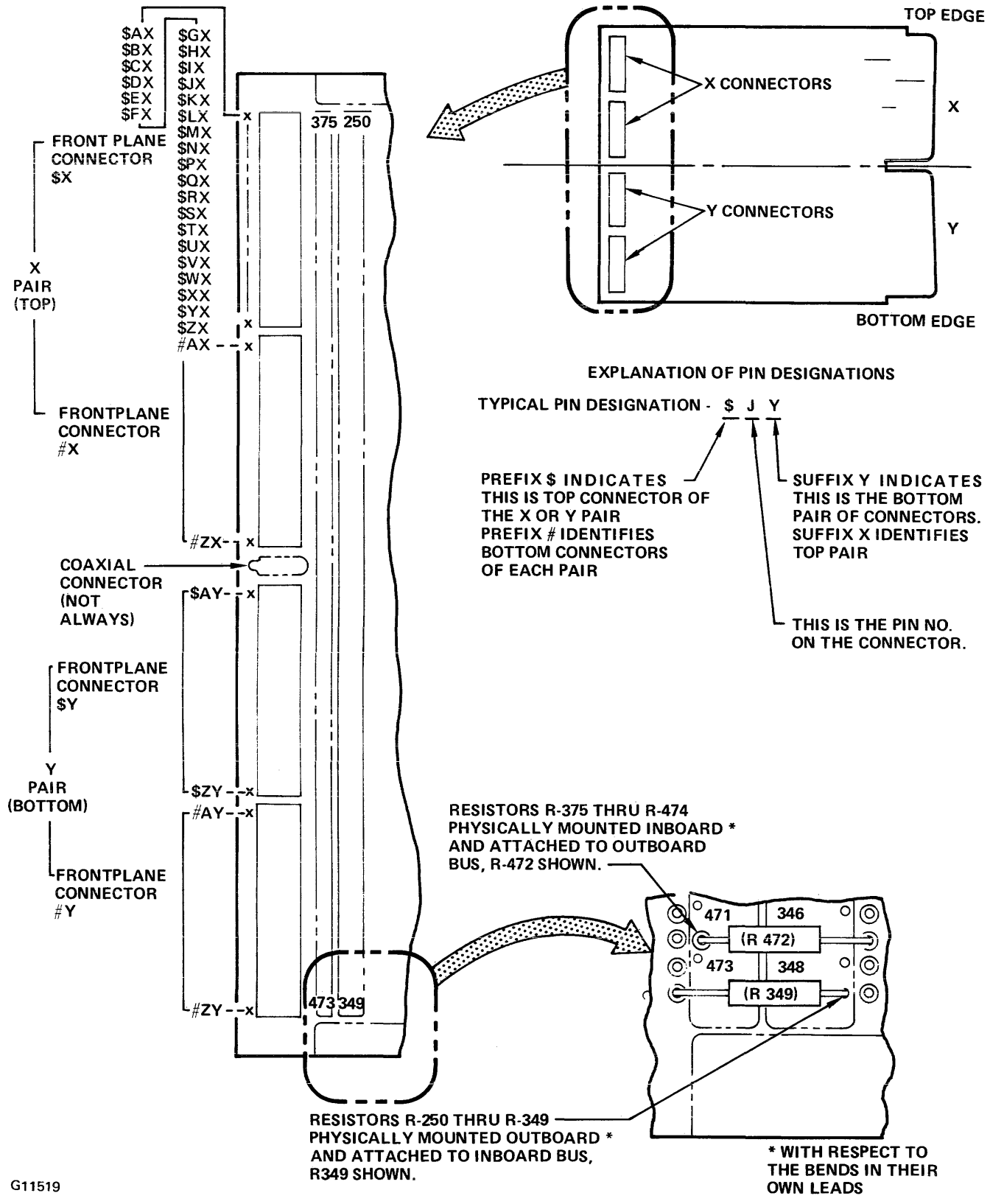


Figure 3-10. Frontplane Pin and Resistor Designations

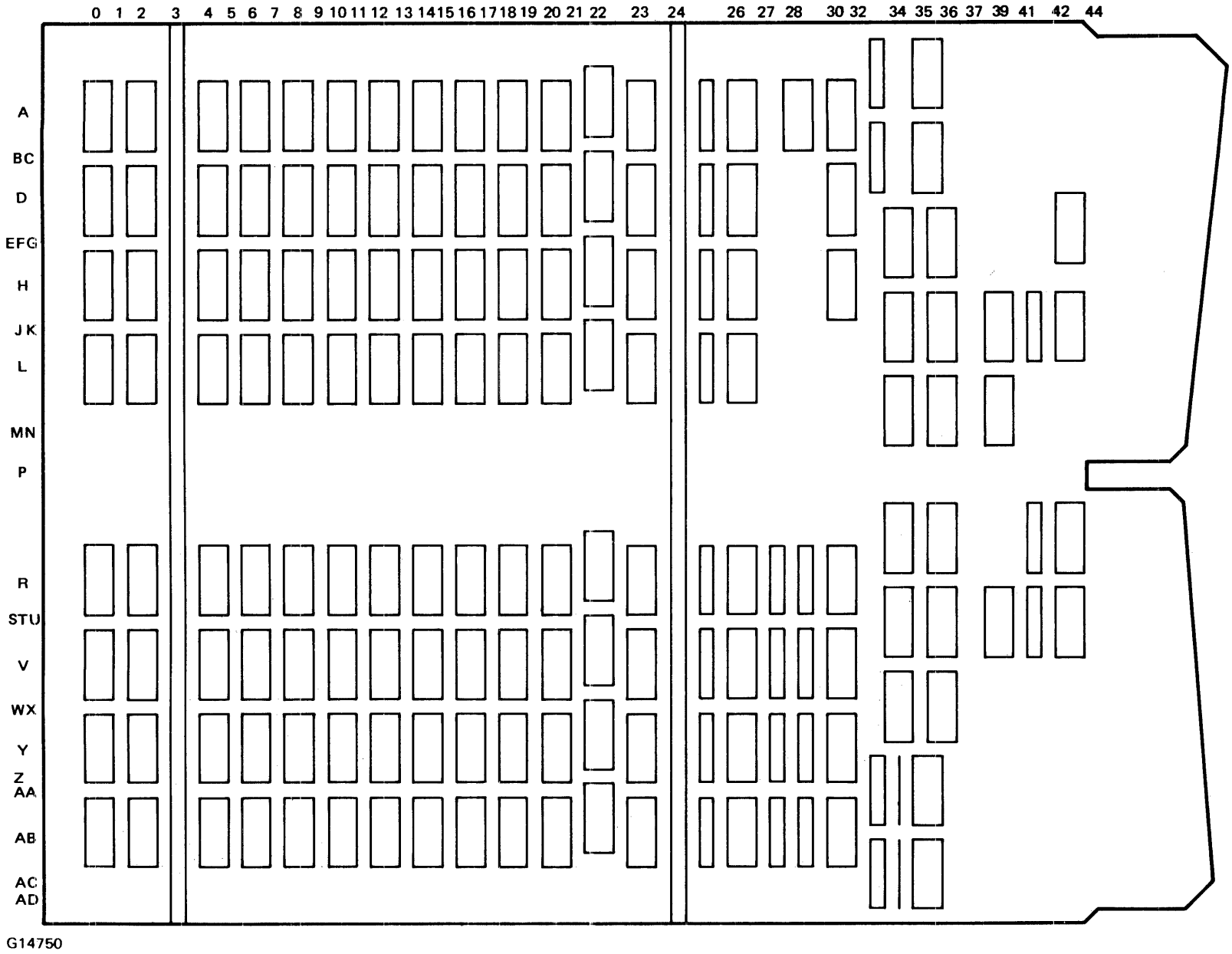
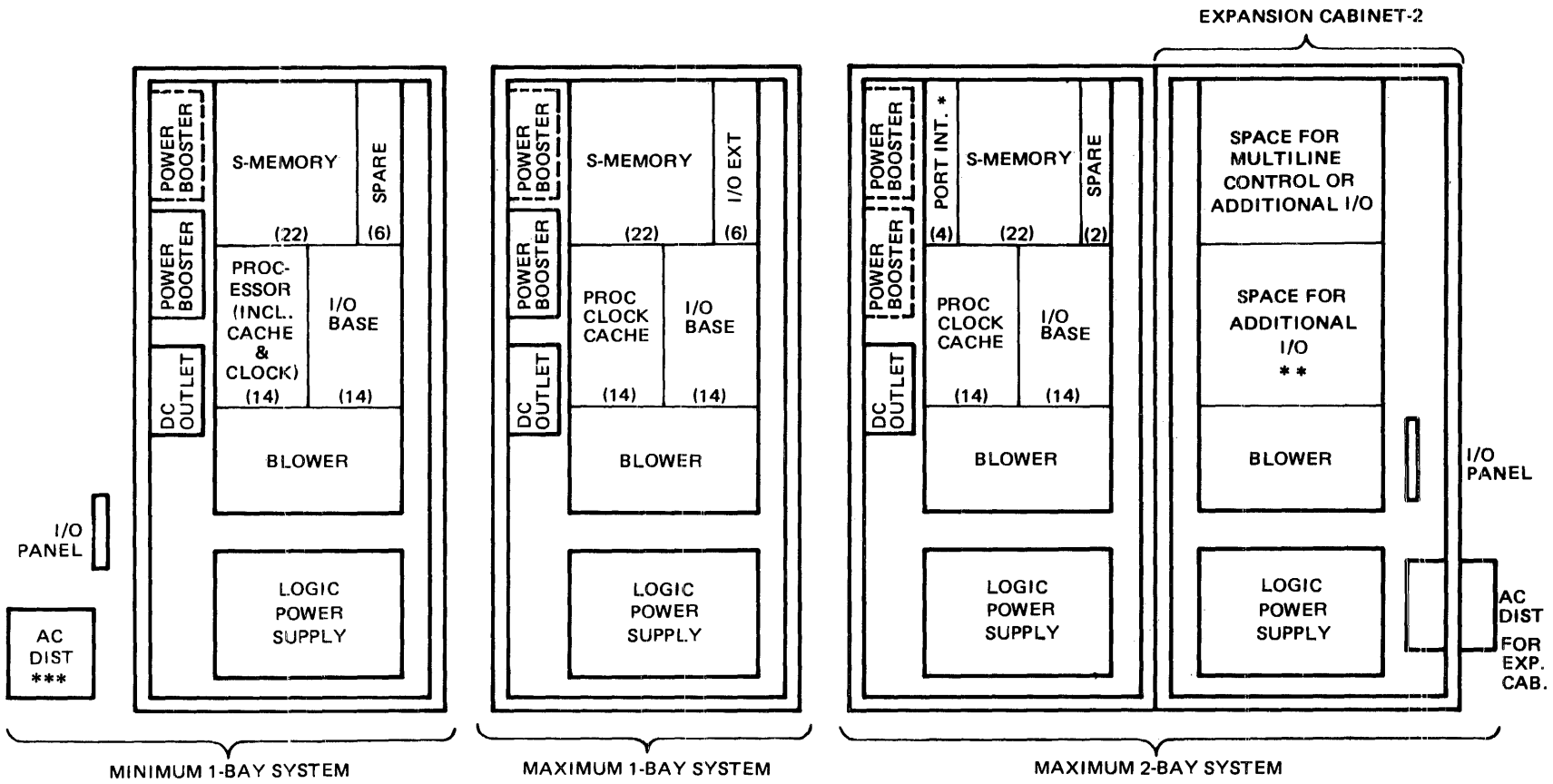


Figure 3-11. S-Memory Storage Card Component Location Coordinates



--- OPTIONAL

( ) NUMBER OF CARD SPACES REQUIRED

* IN PORT-CONNECT CONFIGURATIONS, THE PORT INTERCHANGE (4 CARDS) IS LOCATED IN THE LEFTMOST PORTION OF THE UPPER CARD HOUSING, THE MBU IS MOVED RIGHT, AND TWO SPACES ARE UNUSED.

** THIS SPACE CAN ACCOMMODATE I/O CONTROLS IN I/O EXTENSIONS OR ON SEPARATE BACKPLANES.

*** SAME LOCATION (BENEATH CONSOLE TABLE), ALL 3 CONFIGURATIONS

G14751

Figure 3-12. Central System Physical Layout

Table 3-2. B 1870/B 1860 Central System Circuit Locator

Circuit	Card/Sheet
A/B 5-BIT COMPARATOR	L6
A & B DATA MOVE DECODING	A2
A DATA B DATA COMPARATOR	J6/L6
A DATA GATES	J1/L1
A DATA "OR" LOGIC	L6
A DATA SELECTORS	H7/K7/M7
A DATA TO BUS DRIVERS	A5
A & M REGISTER CONTROL LOGIC	E6
A REGISTER ADDERS	C5/D5
A0 REGISTER	C5/C6/D6
A1 REGISTER	C6/D6
A1 REGISTER TAS OUTPUT MULTIPLEXORS	C7/D7
A STACK	C2/D2
A STACK ADDRESS DRIVERS	C2/D2
A STACK CONTROL	E7/G7
A STACK POINTER	C3
A STACK TO TAS GATES	D1
A STACK WRITE ENABLE CONTROL	D8
B DATA GATES	L2
B DATA "OR"	J6
B DATA SELECTORS	H7/K7/M8
B DATA TO BUS DRIVERS	A8
BINARY ADDER BCD CORRECTOR (24-BIT FUNCTION BOX)	J4/J5/L4/L5
BR REGISTER	H3/K3/M3
CA REGISTER	M6
CACHE CONTROL	C8/D8
CACHE HIT/MISS LOGIC	B7
CACHE KEY COMPARE	B3/B4
CACHE KEY PARITY GENERATOR	B2
CACHE KEY PARITY CHECK LOGIC	B7
CACHE KEY STORE	B2
CACHE MICRO OUTPUT "OR"	B7
CACHE MICRO STORE	B5/B6
CACHE WRITE ENABLE CONTROL	C8/D8/G6
CASSETTE CONTROL	N2/N3
CASSETTE HALT SIGNAL GENERATION	G8
CB REGISTER	M6
CC REGISTER	K6
CD REGISTER	K6
CLEAR LOGIC	A6/E1
CONSOLE LAMP CONTROL	E3
CONSOLE LAMP DRIVERS	A2
CONSOLE SWITCH INTERFACE	A4/E1
CONSOLE SWITCHES ADDRESS COMPARE	A4
CP REGISTER	M6
CYD LOGIC	L7
CYF LOGIC	M6
CYL LOGIC	J6/L6
DISABLE M LOGIC	E4
DISPATCH LOGIC (PROCESSOR)	A5
ERROR LOG REGISTER (MEMORY BASE)	R4
EXECUTE CONTROL SIGNAL GENERATION	E5
FA REGISTER	H4/K4/M4
FA/BR COMPARE LOGIC	H6/K6/M6
FB REGISTER	H5/K6/M5
FETCH MODE CONTROL	E5
FORCE WORD GENERATOR	D6
FORCED WORD COMPARE WITH A0 WORD	D6
HALT LOGIC	E3
HFA REGISTER	H4/K4/M4
HMA REGISTER	H4/K4/M4
INCN REGISTER	A7
INCREMENT A LOGIC	E2
I/O INTERFACE LOGIC	N1/N4/N7/N8
L REGISTER	H3/K3/M3
LITERAL STORAGE AND PROCESSING	G10
LOAD LOGIC	E3
LOAD/SKIP DECODING	A7
LSUX LOGIC	L7
LR REGISTER	H3/K3/M3
LSUY LOGIC	L7

Table 3-2. B 1870/B 1860 Central System Circuit Locator (Cont)

Circuit	Card/Sheet
M REGISTER	C3/D3
M REGISTER PARITY LOGIC	C3/D3
MASK GENERATOR	J5/L5
MAXS REGISTER	J2
MEMORY BASE ACTIVE ADDRESS REGISTER	S4
MEMORY BASE ADDRESS MODIFIER	P4/S5
MEMORY BASE ADDRESS REGISTERS	P2/S3/S4
MEMORY BASE CONTROL INPUT AND STORAGE	R5
MEMORY BASE DATA ACCUMULATOR	Q4
MEMORY BASE E-BIT ADDER SUBTRACTOR	R6
MEMORY BASE MASK GENERATOR	Q6
MEMORY BASE MASK GENERATOR CONTROL	R7
MEMORY BASE MEMORY CYCLE CONTROL	P3/R8/R9
MEMORY BASE MEMORY CYCLE DECODING	P1
MEMORY BASE MEMORY CYCLE REQUEST STORAGE	S7
MEMORY BASE MERGER	P4/Q5
MEMORY BASE ODD PARITY GENERATOR	R3
MEMORY BASE READ DATA REGISTERS	R1
MEMORY BASE REFRESH ADDRESS COUNTER	S4
MEMORY BASE ROTATOR	Q3/Q3
MEMORY BASE ROTATION CONTROL	R8
MEMORY BASE STACK SELECT LOGIC	S8
MEMORY BASE SYNDROME DECODER AND CORRECTOR	Q1
MEMORY BASE SYNDROME GENERATOR	R2
MEMORY BASE SYNDROME INTERPRETER	R3
MEMORY BASE TIMER	R6
MEMORY BASE WRITE DATA REGISTERS	P5/R6
MEMORY CONTROL SIGNAL GENERATION (PROCESSOR)	A6/G7
MEMORY STACK ADDRESS GENERATION	F7
MEX GATING CONTROL LOGIC	F7
MEX IN/OUT GATING	A1/A8/C1/D1/N1/N6
MEX SOURCE CONTROL	G6/N7/N8
MICRO DECODING	E/F/G
MICRO SEQUENCING LOGIC	E4/G8
MODE LOGIC	E1
MOVE AND CLEAR LOGIC	E6
MSBX LOGIC	L6
NANO MOVE DECODING	E8
NANO REGISTER	F10/F11/G11
PERM REGISTER	H6
PERP REGISTER	H6
PORT INTERCHANGE CONTROL LOGIC	U9
PORT INTERCHANGE DISPATCH LOGIC	U8
PORT INTERCHANGE READ DATA REGISTER	U4
PORT INTERCHANGE STATE MACHINE	U10
REGISTER MOVE CONTROL SIGNAL GENERATION	H1
REGISTER SELECT DECODING	E2
ROTATOR	J3/L3
ROTATION CONTROL	F6/L7
RUN/HALT LOGIC	E1
S-MEMORY DATA ROUTING CONTROL	F7
SCRATCHPAD (LEFT)	H4/K4/M4
SCRATCHPAD (RIGHT)	H5/K5/M5
SCRATCHPAD ADDRESS STORAGE	H1/K1/M1
SCRATCHPAD ADDRESS GENERATION	F8
SCRATCHPAD CONTROL	G6/H6/K6/M9
SINK REGISTER SELECTION LOGIC	M1/K1
SKIP CONTROL LOGIC	M6/G9
SOURCE AND SINK CONTROL GENERATION	F4/F5/G4/G5
STATE MACHINE	E4/E7
T REGISTER	H3/K3/M3
TAS (TOP OF A-STACK)	C2/D2
TIMER REGISTER	C8/D8

Table 3-2. B 1870/B 1860 Central System Circuit Locator (Cont)

Circuit	Card/Sheet
U-REGISTER	N2
WRITE ENABLE TIMING LOGIC	C8
X REGISTER	H2/K2/M2
Y REGISTER	H2/K2/M2
4-BIT FUNCTION BOX	N4
24-BIT FUNCTION BOX	J/L
9D LITERAL STORAGE	E7

Example: L6 is Card L, Sheet 6.

SHIPPING AUTHORIZATION

Each system, I/O control, or peripheral device shipped to a site is accompanied by the following paperwork:

a. Shipping Authorization (SA).
b. Unit Travel Log (UTL) OR
c. Processing Order if manufactured in Liege, Belgium.
d. Label kit.

The shipping authorization (SA) (figure 3-13) is a two-part document. All applicable areas on this document are identified on figure 3-13 by means of circled letters. The usage of the areas indicated by the circled letters is defined in the following list.

1. Item (A) indicates the bill-of-lading number. This number must be used to trace lost or delayed shipments.
2. Item (B) indicates the date the item(s) was shipped from the factory.
3. Item (C) indicates the expected date of arrival.
4. Item (D) indicates method of shipping: air, surface, or water.
5. Item (E) indicates the sender.
6. Item (F) indicates the recipient.
7. Item (G) indicates the number and type of item in the shipment.
8. Item (H) indicates who is responsible for the shipping charges.
9. Item (I) indicates the item number identification (as listed on the first part of the SA).
10. Item (J) indicates the order number for the item(s).
11. Item (K) indicates the quantity of a given item.
12. Item (L) indicates the manufacturing and engineering part number of an item.
13. Item (M) indicates the model number and the description of an item.
14. Item (N) indicates the serial number assigned to an item.
15. Item (O) indicates any special comments, information, or clarification concerning the item(s) in this shipment.

UNIT TRAVEL LOG (UTL)

The UTL is a document designed to inform the recipient of the manufacturing level of the device. The UTL also provides the unit name, unit number, and build-level of the unit, and lists any changes (EI's or DCN's) that have been incorporated above the build-level. Discrepancies (EI's or ECN's that should have been incorporated in this build-level but are not) are listed in the lower-right quadrant of this document. A sample of a UTL is shown in figure 3-14.

PROCESSING ORDER

The Processing Order is a document issued by the Burroughs Liege manufacturing plant in place of the UTL. A processing order contains essentially the same information as that contained on a UTL. An example of a processing order is shown in figure 3-15.

LABEL KIT

The label kit consists of a 1/2" x 1-1/2" metallic, gummed back label with the unit name and 8-digit (M&E) number. If the device is an I/O control, this label is to be affixed to a designated location on the side of the I/O base or extension that receives the control. If a system unit or peripheral unit is involved, the label is affixed to the unit itself.

(6236-3-72)
3021423

STRAIGHT BILL OF LADING - SHORT FORM - ORIGINAL - Not Negotiable

DATE SHIPPED

CARRIER'S NO.

RECEIVED, SUBJECT TO THE CLASSIFICATIONS AND TARIFFS IN EFFECT ON THE DATE OF THE ISSUE OF THIS BILL OF LADING.

the property described below, in apparent good order, except as noted (contents and condition of contents of packages unknown), mark, consigned, and destined as indicated below, which said carrier (the word carrier being understood throughout this contract as meaning any person or corporation in possession of the property under the contract) agrees to carry to its usual place of delivery at said destination, if on its route, otherwise to deliver to another carrier on the route to said destination. It is mutually agreed, as to each carrier of all or any of said property over all or any portion of said route to destination, and as to each party at any time interested in all or any of said property, that every service to be performed hereunder shall be subject to all the terms and conditions of the Uniform Domestic Straight Bill of Lading set forth (1) in Uniform Freight Classification, in effect on the date hereof, if this is a rail or a rail-water shipment, or (2) in the applicable motor carrier classification or tariff if this is a motor carrier shipment.

Shipper hereby certifies that he is familiar with all the terms and conditions of the said bill of lading, including those on the back thereof, set forth in the classification or tariff which governs the transportation of this shipment, and the said terms and conditions are hereby agreed to by the shipper and accepted for himself and his assigns.

(A)

FROM BURROUGHS CORPORATION

6300 HOLLISTER AVE.
GOLETA, CA. 93017

(E)

ROUTING

TO: (F)

B&C TRANSFER
8146 BYRON RD.
WHITTIER, CA.

M/F: SBP INVENTORY

(B) SCHEDULED SHIPMENT DATE: 7/3/75

DATE PREPARED: 7/3/75

REBILL TRANSPORTATION: YES ☐ NO ☒XX

QA INITIALS OF APPROVALS: DATE 7/3/75

BILL OF LAD. NO. 278389

CHG. NO.

PAGE 1 OF 1

(C) DEST. DUE DATE: 7/10/75

PARTS/EQUIPMENT/FORMS: EQUIPT

(D) MODE OF SHIPMENT: SURFACE

MACHINE ORDER NO.

USE CODE | BILL TO GRP: N/A

ORIG DEST	NO.	NAME
	641	GOLETA
	595	B&C

CAR OR VEHICLE INITIALS NO. CAPTIVE

NUMBER PKGS. (G)	KIND OF PACKAGE, DESCRIPTION OF ARTICLES, SPECIAL MARKS, AND EXCEPTIONS	*WEIGHT SUB. TO CORP.	CLASS OR RATE	CHECK COLUMN
	BOXES ADDING OR COMPUTING MACHINES OR PARTS			
	BOXES BOOKKEEPING MACHINES OR PARTS			
	BOXES TYPEWRITERS AND COMPUTING MACHINES COMBINED PARTS			
	BOXES ADDING MACHINES STANDS, I.S. (KNOCKDOWN / SET UP)			
	BOXES PRINTED MATTER, PAPER N.O.I.			
	TABULATING OR AUXILIARY MACHINES (UNCRATED) OR PARTS RELEASE VALUE $5.00 PER LB. (HHG-VAN)			
	ELECTRONIC MACHINES AND/OR PARTS RELEASED VALUE $0.50 PER LB. (AIR FRT.)			

Subject to Section 7 of conditions of applicable bill of lading, if this shipment is to be delivered to the consignee without recourse on the consignor, the consignor shall sign the following statement.

The carrier shall not make delivery of this shipment without payment of freight and all other lawful charges.

(Signature of Consignor)

If charges are to be prepaid, write or stamp here "To be Prepaid."

PREPAID

Received $ _____ to apply in prepayment of the charges on the property described hereon

Agent or Cashier

Per _____ (The signature here acknowledges only the amount prepaid)

Charges Advanced:

$ _____

(H)

SEND FREIGHT BILL TO:
BURROUGHS CORP.
ATTN: TRAFFIC
6300 HOLLISTER AVE.
GOLETA, CA. 93017

1 Burroughs Corporation SHIPPER

PER _____

PERMANENT POST-OFFICE ADDRESS OF SHIPPER

AGENT _____

PER _____

The fibre boxes used for this shipment conform to the specifications set forth in the box maker's certificate thereon, and all other requirements of Rule 41 of the Consolidated Freight Classifications.

*If the shipment moves between two ports by a carrier by water, the law requires that the bill of lading shall state whether it is "carrier's or shipper's weight." NOTE - where the rate is dependent on value, shippers are required to state specifically in writing the agreed or declared value of the property. The agreed or declared value of the property is hereby specifically stated by the shipper to be not exceeding

per

G10274/SHT 1 OF 2

Figure 3-13. Shipping Authorization (Sheet 1 of 2)

1

FROM: BURROUGHS CORPORATION

6300 HOLLISTER AVE.
GOLETA, CA. 93017

TO:

B&C TRANSFER
8146 BYRON RD.
WHITTIER, CA.
M/F: SBP INVENTORY

SCHEDULED SHIPMENT DATE: 7/3/75	BILL OF LAD NO. 278389 CHG. NO.	PAGE 1 OF 1	
DATE PREPARED: 7/3/75	DEST. DUE DATE: 7/10/75	PARTS/EQUIPMENT/FORMS: EQUIPT	
REBILL TRANSPORTATION: YES ☐ NO XX	MODE OF SHIPMENT: SURFACE	NO.	NAME
QA INITIALS OF APPROVALS: H	DATE: 7/3/75	MACHINE ORDER NO.	ORIGDEST 641 GOLETA
	USE CODE: N/A	BILL TO GRP	595 B&C

ROUTING

CAR OR VEHICLE INITIALS NO. CAPTIVE

ITEM NO. (I)	QTY. (K)	PART NO. (L)	CUM. NO.	ORDER NO. (J)	MODEL NO./DESCRIPTION (M)	SERIAL NO. (N)	ACCOUNTING USE ONLY: STANDARD COST	START UP	INTER GROUP MARGIN	INTRA GROUP MARGIN	PLANT MARGIN	TRANSFER PRICE
1.	1	1630 1251			B9112 CARD RDR	B10046-004						

(O)

UNIT IS SBP OWNED,
TEMPORARY STORAGE AT B&C.
THIS SA FOR FOLLOW-UP ONLY.
UNIT SHIPPED TO B&C 7/2/75
WITH B5500 ON SA 184349.

G10274/SHT 2 OF 2

Figure 3-13. Shipping Authorization (Sheet 2 of 2)

UNIT TRAVEL LOG

SYSTEM NO.

PAGE 1 OF 1

UNIT NAME	UNIT NUMBER	REV.	D/L	CUM NO.	SERIAL NUMBER
CONT-M/T CASSETTE	2208-2830				00 -
CASS TAPE-CO 1	2209-0914				
CASS TAPE-CO 2	2209-0963				
CA-C/TAPE DRIVE #1	2210-4970				

INCORPORATED CHANGES ABOVE PARTS LIST LEVEL (P.L.L.)

EI ECN EWI	M.C.	INST.	INSP.	EI / ECN / EWI	M.C.	INST.	INSP.	EI / ECN / EWI	M.C.	INST.	INSP.

OPERATION	BY	DATE	DISCREPANCIES: DISCREPANCY / PART NUMBER	QTY	M.C.	INST.	INSP.
START OF FINAL ASSEMBLY							
ELECTRICAL INSP.							
MECH VISUAL INSP.							
PLUGGABLE INSP.							
FINAL BUILD ACCEPT.							
POWER TEST ACCEPTANCE							
FINAL ACCEPTANCE TEST							
UNIT (PRE-SHIP.) INSP.							
FINAL (SHIPPING) INSP.							

UNINCORPORATED CHANGES WITHIN P.L.L.

VARIANCE REQUESTED

Q.A. APPROVAL

SBP 1062 REV. 6-73

PRODUCT DISTRIBUTION/PROD. Q. C.

Figure 3-14. Unit Travel Log

COMPAGNIE BELGE BURROUGHS S.A.
HERSTAL - LIEGE - BELGIUM

PROCESSING ORDER No 9742 *

Sequence Number
Page of

Assembly Schedule	Pro number	Order number	Group	Style	Cabinets	Cycle	Completion date

Issued by Product Distribution Mgr.
Date: Sign.

Approved by Mfg. Control Mgr.
Date: Sign.

* remarks at bottom

Scheduled by Product Distribution Mgr.
Date: Sign.

Sold to:

Shipped to:

Customer:

Configuration level:

Job order:

Item	Model No.	M & E number	Description	Serial No.	Selling Price to BISA/BIAL	Selling Price to Subs./Dist.	Domestic value	Head Office Brussels
								Acknowledged receipt Date: Signature:

Incorporated changes above manufacturing parts list level

No.	EI/ECN/EWI	Insp.	No.	EI/ECN/EWI	Insp.	No.	EI/ECN/EWI	Insp.	No.	EI/ECN/EWI	Insp.

Unincorporated changes

Operation	By	Date
Start of final assembly		
Final Assembly Inspection		
X circuit list		
X mechanical		
X pluggables		
X O.L verification		
X visual		
Unit inspection		
Final Accept Standards		
Final Inspection		

* Manufacturing Control remarks:

Accepted by Product Assurance Mgr.
Date:
Sign.:

1. PRODUCT DISTRIBUTION - LIEGE

Form. Lie 459 (June 74)

G10277

Figure 3-15. Processing Order

SECTION 4
MAINTENANCE TECHNIQUES

INTRODUCTION

This section contains maintenance and troubleshooting procedures for the B 1870/B 1860 Central Systems. Included are discussions of general maintenance procedures and the aids which are available to assist in fault isolation, plus specific maintenance-related data pertaining to the processor and S-memory. Instructions for gaining access (only) are provided for the logic power supply, booster supply, and cassette tape reader, since these devices are described fully in separate publications. For similar reasons, no discussion of I/O subsystem maintenance is included.

MAINTENANCE CONCEPT

Maintaining a B 1870/B 1860 Central System in operating condition includes proper preventive maintenance, installing and checking any recently released hardware changes, plus appropriate corrective action when required. Since there are few electromechanical devices in the Central System itself, the need for continuing attention is minimal. However, certain precautions apply, and these are listed in the preventive maintenance discussion. When the central system does fail, the repair effort should be directed toward locating the fault (to the failing component) on site, correcting the fault, and restoring the system to operation. In general, the direct substitution of subassemblies is to be avoided, and is reserved for cases where all other approaches fail.

As with most devices, a malfunction of the B 1870/B 1860 Central System is characterized by its failure to perform one or more of the functions for which it was intended. Unlike simpler computers, however, problems occurring within the Central System are likely to be difficult to detect and isolate. This is due to the overall complexity of the system, and to the fact that control through several levels of software makes establishing a cause-effect relationship between hardware faults and improper program results extremely difficult. For example, on a typical maintenance call involving a logic fault, determining what the system is failing to do will take longer than finding and fixing the problem once the failure mode is established.

TEST EQUIPMENT

A basic kit of test equipment, in addition to common mechanical and electronic tools and work aids, is required to perform the troubleshooting and maintenance procedures described herein. The following equipment should be available whenever Central System maintenance work is to be performed:

a. Tektronix 465 oscilloscope.
b. Triplett 630 multimeter or equivalent.
c. Burroughs 3300 digital voltmeter (DVM) or equivalent.
d. Field Card Tester.
e. Logic Card Extender (P/N 2207 1237).

PREVENTIVE MAINTENANCE SCHEDULE

Preventive maintenance for the B 1870/B 1860 Central System consists of inspection, checking operating voltages, and cleaning. Keeping the hardware in good order is of considerable importance to maintaining an operational and reliable system. The following items should be checked each time some portion of the system is serviced:

a. Ensure that all logic cards and connectors are firmly and accurately seated in their sockets.
b. Check power voltages and adjust if needed. (Refer to Special Troubleshooting Procedures for nominal voltage settings.)
c. Inspect the interior and exterior portions of the Central System cabinet and subassemblies for dust, foreign matter and corrosion. Take corrective action as needed.
d. Ensure that all fans are operational and rotate freely.
e. Check the air filter located just above the Logic Power supply in each cabinet bay. Replace if necessary.
f. Check Error Log for possible failing memory. Replace storage chips if needed.

TROUBLESHOOTING PROCEDURES

Dynamic Troubleshooting

Dynamic troubleshooting involves the execution in sequence, of six diagnostic programs:

a. MTR Mode Processor Test.
b. Dynamic Processor Test.
c. Port interchange-3 Test.
d. Dynamic S-Memory Test.
e. Dynamic Cache Test.
f. Central System Interaction Test.

These Programs exercise the central system logic in a progressively complex manner, and can indicate faults down to the logic card level. When suspect cards have been identified, the field card tester is employed to further isolate the problems to failing circuits or IC chips. Faulty components are replaced as they are located, then the repaired cards are again checked with the Tester. Finally, the system is reassembled, and the diagnostic programs are again executed to verify the repairs. Successful completion proves the ability of the system to perform as intended.

There may be times when a diagnostic test does not indicate hardware failures, but the system fails during operation under MCP (Master Control Program) control. The following is a list of conditions which could cause system failure but not diagnostic test failures:

a. Power Supply Voltage. The logic power supply Voltages may be out of tolerance. Refer to the "Special Troubleshooting Procedure, Use of Voltage Margins" section, this manual, for a listing of the voltages and their nominal settings.

b. System Timing. System timing may be out of tolerance. Refer to section 5 of this manual for adjustments of system timing.

c. I/O's and Peripherals. An I/O control may cause the system to fail. Use the I/O Diagnostic Test provided with each control to determine if there is a faulty control. Occasionally a peripheral device may fail, which could cause the central processor to fail. The I/O diagnostic tests may also be useful for indicating a faulty peripheral device.

d. System at Incorrect Operating Level. Required hardware or software changes, if not incorporated, may cause MCP failures. Check the system to ensure all released hardware or software changes have been incorporated. Take appropriate corrective action as needed.

e. Margin Testing. Failures may be found by the diagnostic tests with the use of voltage margin testing. For testing instructions, refer to "Special Troubleshooting Procedure - Use of Voltage Margins" in this section.

f. Loading. Each logic power supply is designed to handle a load of up to 200 amps. If the system is near its load limit, MCP failures could occur. Check to ensure that power supply loading is not in excess of the amounts permitted. Refer to the Installation section in this manual for loading allowances.

g. Software. Ensure that the amount of memory required for the programs is installed. Ensure that all required peripherals are powered up and ready for operation.

To perform the dynamic troubleshooting procedure, follow figure 4-1. Refer to the paragraph entitled "Diagnostic Programs" and "Field Card Tester" for further guidance in the use of these items.

Diagnostic Programs

Diagnostic programs exercise the processor with sequences of microinstructions, and are designed to produce specific identifiable results. Included with each program is a listing of proper responses and those which are indicative of certain faults. All diagnostic programs are stored on cassette tapes, and produce their response by way of the 24 console lamps or the console CRT. Directions for running and analyzing the results of each program are contained in the accompanying documentation. The loading procedure for these programs has now been standardized. Included in this set of standards are halt codes, methods for entering program options, operator selectable modes of operation, register and scratchpad usage, and loading procedures. The standard loading and usage procedures are described in the following paragraphs.

NOTE

The following procedures deal with processor, S-memory, and Cache. The I/O subsystem, cassette tape subsystem and power supplies are covered in other B/1870/B/1860 documents.

Throughout the remainder of this section, halt codes written in hexadecimal will be indicated by the parenthesized notation (HEX) following the code. Hexidecimal notation includes the numerals 0-9 and the letters A-F. variants included with a hexadecimal code will be indicated by lower case letters. (Example: xxAAAA.)

STANDARD LOADING

Loading procedure for all these diagnostics (except the MTR Mode Processor Test) conforms to the following general format:

a. Check that the cassette in console cassette reader has a part number and revision identification matching the listing of the desired test program.

b. Place the MODE switch (Op panel) in the MTR position.

c. Place the MICRO SOURCE switch (D/M panel) in the NORMAL position.

d. Press CLEAR.

e. Enter block of Cache desired for use into the BR register. (A=000000(HEX), B=000001(HEX)).

f. Press START, then select LR (REGISTER GROUP 7, REGISTER SELECT 2). The processor will halt with LR=AAAAAA(HEX).

g. Place the MODE switch in NORMAL.

h. Enter desired options. Refer to the program documentation. (No entry = default to standard execution.)

i. Press START.

The test will then run under the chosen options until one of the following occurs:

a. A change of options is desired.

b. The end of test occurs (LR=EEEEEE(HEX) processor halt).

c. An error is detected.

Note that not all diagnostic programs use all of the options provided. The program documentation will state which options are valid and any illegal entry will be reported by means of LR=DDDDDD(HEX) halt.

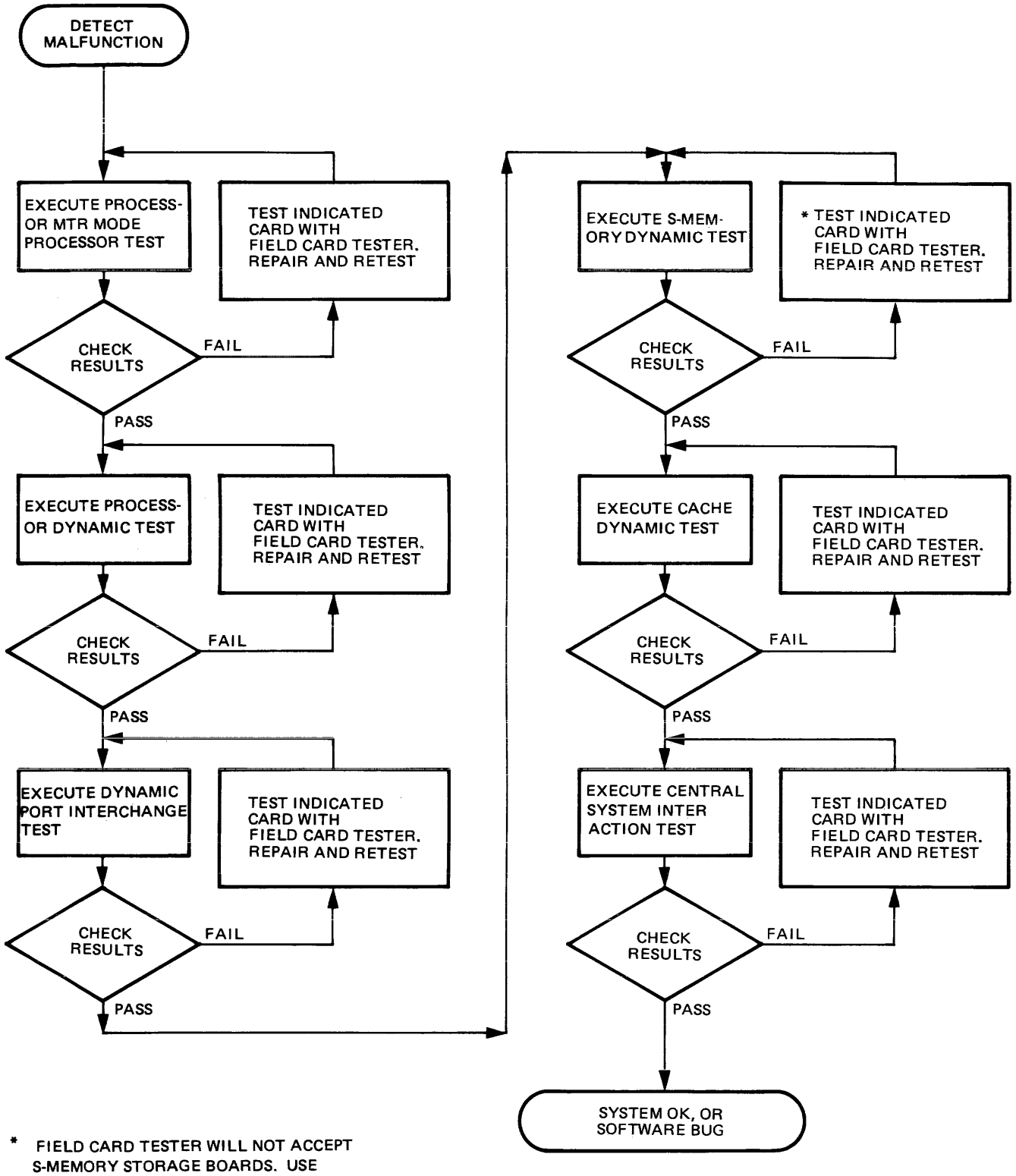


Figure 4-1. Dynamic Troubleshooting Flow

HALT STANDARDIZATION

When a program halt occurs, the LR register will contain a condition indicator value for interpretation by the operator. These halts (which are standard for all central system programs) are described in tables 4-1 and 4-2.

Table 4-1. Standard Halts

Standard Halts	Meaning
LR=xxvnnn(HEX)	Error Halt. xx = test section where error occurred (00 = executive or dynamic test MTR error); v = halt variant to inform the operator that a specific diagnostic procedure is optionally available to further isolate (1 = Lockup Loop is available, 2 = Diagnostic routine is available; machine state will be lost if enacted); nnn = error number.
LR=xxAAAA(HEX)	Begin Test Section Halt. Occurs only when optionally selected. Indicates that test number xx is Loaded, and will execute upon pushing START.
LR=AAAAAA(HEX)	Enter Options Halt. Also indicates the end of MTR mode operations during loading. The operator may at this time display the listing and cassette part and version numbers and may change certain options if desired.
LR=BBBBBB(HEX)	"Blow-up" Halt. Unexpected halt within a test section.
LR=DDDDDD(HEX)	Illegal Option Halt. An illegal operator-selected option was entered. Press START to return to the Enter Options halt.
LR=EEEEEE(HEX)	End of Test Halt. All selected loops and passes of the test have completed. If the program is resident in S-memory, press START to restart; if in the Cache only mode, rewind the cassette tape and begin again from operating instruction 1.

The error halts listed in table 4-2 are used when an error is encountered within a test's executive routines during testing.

Table 4-2. Standard Executive Error Halts

Executive Halts	Meaning
LR=000005(HEX)	MTR Mode failure (Cache-only mode). Halt code residing in LR during MTR Mode Loading when Cache is the intended executive memory.
LR=000020(HEX)	Cassette Read Error. Cassette Read error detected after an executing program has read cassette to load either S-memory or Cache memory.
LR=000015(HEX)	MTR Mode Failure (S-memory-only mode). Halt code residing in LR during MTR Mode Loading when S-memory is the intended executive memory.
LR=000020(HEX)	Correctable S-memory Error. Correctable S-memory error detected while still in the MTR mode.
LR=000030(HEX)	Run Mode Failure (Cache-only mode). Where possible, this halt code is placed in LR following a failure in the C (Cache) Micro Source mode.
LR=000035(HEX)	Run Mode Failure (S-memory-only mode). Where possible, this halt code is placed in LR following a failure in either the S or Normal Micro Source modes.
LR=000045(HEX)	Read Cache Data Error. Cache micro data or parity error detected while checking loaded micro code in Cache.
LR=000050(HEX)	Correctable S-memory Error. Correctable S-memory error detected by a dynamic routine while checking loaded micro code in S-memory
LR=000055(HEX)	Uncorrectable S-memory Error (PERM3). Uncorrectable S-memory error detected by a dynamic routine while checking loaded or relocated micro code in S-memory. This halt is used when the error is detected by testing bit 3 in the PERM register. The Error Log is saved in S9A (SAVE.ELOG) for display.
LR=000060(HEX)	Uncorrectable S-memory Error (Data). Uncorrectable S-memory error detected by a dynamic routine while checking loaded or relocated micro code in S-memory. This code is used when a "Read Not Equal to Write" condition is detected.
LR=000070(HEX)	Extraneous Port Device S-Memory Access Error. Erroneous access to S-memory by a port device detected by port and channel code not being its expected value after MTR-mode loading.

STANDARD EXECUTION OPTIONS

There are three ways in which operator-selected options may be entered. These modes of entry utilize the BR register, the console switches, and certain scratchpad (SPAD) locations.

BR Register

BR, used only prior to loading a test, serves to select the block of Cache (A or B) to receive the program. In the MTR Mode Processor test, the contents of BR indicate the block of Cache whose integrity is to be verified for use in subsequent tests. Note that the selected block of Cache must remain consistent throughout the series of tests to ensure adherence to the "test before use" philosophy.

Console Switches

The console switches are used for selection of test options during program execution. This feature allows the operator to select or modify options dynamically (without a manual restart procedure). The console switch contents are periodically sampled by each test program to determine if a change has occurred since the last sampling. The left most switch (bit 0) provides a validity bit that serves to prevent sampling of inadvertent residual switch settings or partial entry settings. To modify options, the operator makes certain that the leftmost switch (Validity) is reset (down), then changes the console switches to the desired setting. The Validity switch is then returned to the set (up) position.

Scratchpad

Certain scratchpad locations are used for pre-execution selection of test options. These options are entered into scratchpad at a control halt. (LR=AAAAAA(HEX) or LR=xxAAAA(HEX)). These preselected options may be overridden from the D/M panel whenever the console switch Validity bit is true. In other words, when the Validity bit is on (leftmost console switch up) the other console switches determine what the program is to do. When the Validity bit is reset (down), the preselected options become effective. To change a preselected option, a dynamic Begin Section halt (or Enter Options halt) must be selected on the console switches. This action will cause the LR=xxAAAA(HEX) (or LR=AAAAAA(HEX)) control halt. The desired SPAD location may then be loaded with the selected option, after which the program is restarted. The significance of the various bit positions is shown in table 4-3. (Refer to figure 4-2.)

Table 4-3. Test Execute Options

Bit	Options
0	Validity. If set, the program will utilize the setting of the console switches rather than the SPAD setting (S1A). If reset, the program uses the contents of S1A for program options.
1-15	Individual Test Program Options. These bits select the individual diagnostic program routines.
16	Reserved.
17	Automatic Restart. This bit is checked a minimum of once every 10 seconds to determine if a program restart has been requested. If this bit is set, the program executing is immediately discontinued and the LR=AAAAAA(HEX) halt is automatically entered. This option allows the operator to restart (even from within a long test section) in an orderly fashion without cumbersome manual operations. If this bit is reset, normal execution is continued.
18	Start of Pass Halt. When set, this bit causes entry into the LR=AAAAAA(HEX) halt when the test program has completed all selected test sections the specified number of times. If this bit reset, no LR=AAAAAA(HEX) halt will occur.
19	Start of Section Halt. When set, this bit causes the LR=AAAAAA(HEX) halt to be entered prior to the execution of each test section. If this bit is reset, the halt is bypassed.
20-23	Error-time options.
22	Diagnose. If diagnosis is possible when an error has occurred, the v digit in LR=xxvnnn will be set to some defined value. At this time, the "diagnose" bit (22) can be set and the program will attempt to further isolate the fault (possibly destroying the original conditions surrounding the failure). After the diagnosis routine the program will re-enter the halt, at which time other options may be selected. The options normally selected at this point are re-diagnosis (bit remains set), continue program (bit reset), or lockup for scoping (bit 23 set).
23	Scope Loop. Following an error halt, setting this bit causes the program to enter a tight loop (without halts) having sync points for triggering an oscilloscope. In the loop the failing test case is re-executed repeatedly (until bit 23 is reset). Execution of the main program continues upon resetting bit 23. Note: This bit should never be set unless a scope loop is desired; otherwise, the program will lock up on the first test case encountered. Not all test cases have this option available. The v digit in the LR=xxvnnn(HEX) halt code indicates its availability. (Refer to the halt code description.)

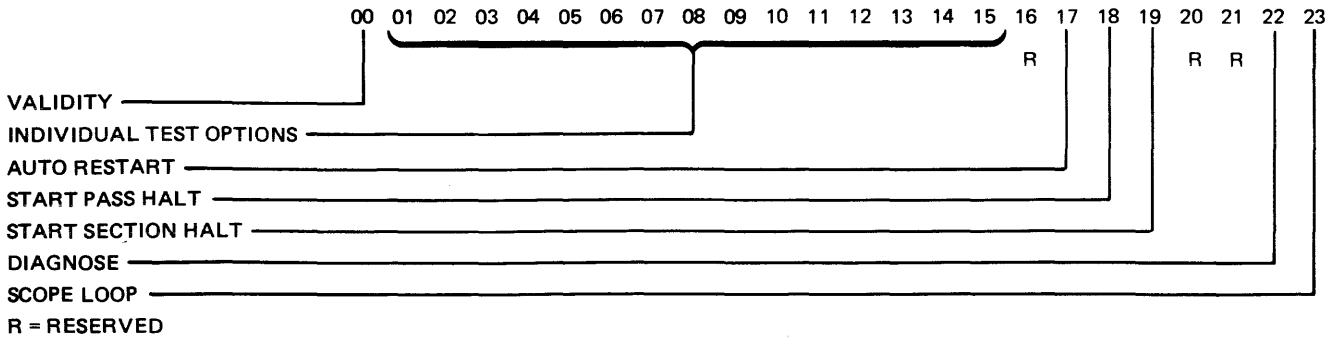


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Figure 4-2. Test Execution Option Selection

STANDARD SCRATCHPAD OPTIONS

Certain Scratchpad (SPAD) locations are used to store option designators for use during the test routines. The SPAD options may be entered during either the LR=AAAAAA(HEX) or LR=xxAAAA(HEX) halt. Since SPAD locations may be accessed from the console, it is expedient to enter the desired options directly. The available options and option designators are listed below. The capabilities provided include selection of all standard run options.

If a test section is deselected at the LR=xxAAAA(HEX) HALT, that section will not be executed if it has a test number higher than xx. If the deselected section is equal to or less than xx, it will not be re-executed on the present pass and will be skipped on subsequent passes. If the Pass Counter, Pass Limit, Loop Counter, or Loop Limit has been modified, the changes made will have no effect until execution of the currently selected section (xx) is completed. Neither the Section Number nor the Run Mode SPAD locations should be modified by the operator. The option designators and corresponding SPAD locations that have common definitions in all central system diagnostic test programs are listed in table 4-4.

Table 4-4. Scratchpad Option Specifications

SPAD	Designator
SOA	Run Mode. This SPAD location holds a value which is ORed with the contents of the Micro Source Switch Register (MSSW). This value should not be altered unless the tape is rewound and a complete reload is to be accomplished. The Run Mode designators are as follows: 000000(HEX)(0) = S-memory to Cache (Normal execution). 000001(HEX)(1) = Run from S-memory only. 000002(HEX)(2) = Run from Cache only. Default = Dependent upon test program.
S1A	Preselected Option Storage designator. This SPAD location holds option bits which are used when the console validity switch is reset. Default (no options specified) equals XXXXXXXXXXXXXXXXOOOOXXXX
S2A	Test Section Designators. Specify the test sections to be run. Each bit position matches the corresponding "decimal" section number (bit 9 for test section 9, bit 10 for test section 10, etc). Each true bit selects the corresponding test section. Default = run all valid test sections.
S3A	Test Section Number Indicator. Indicates the test section currently executing: xxAAAA(HEX), where XX is the test section number.
S4A	Test Section Loop Limit Designator. Specifies the executions per selected test section (in binary) to be performed prior to proceeding to the next selected test section. Default =000001(HEX).
S5A	Present Section Loop Counter. Indicates the present loop (executing test section) in effect. When this counter matches S4A, the test proceeds to the next selected section.
S6A	Test Pass Limit Designator. Specifies the number of executions desired for all test sections (in binary). If FFFFFF(HEX) is entered, the test will execute continuously (infinite number of passes). Default =000001(HEX)
S7A	Present Test Pass Counter. Indicates the present pass (of the complete test cycle) in effect. When the binary value in S7A matches that in S6A, the program terminates with the LR=EEEEEE(HEX) halt.
S8A	Cache Block Designator. Specifies the block of Cache being utilized by the test (if any). This SPAD location contains the BR value set prior to test loading, and should not be altered during testing. Default = Block A (000000(HEX))
S9A	ELOG Value After Test Case. Contains the error Log (register) value saved following a specific S-memory related test case within the program. If no error condition was incurred, the contents of S9A will equal 0.
S10A-SnA	Special options dependent upon specific test programs.

NOTE

There are several options which may not be preselected by way of SPAD, and if so specified will be ignored:

a. Automatic Restart
b. Diagnose
c. Scope Loop

TEST DESCRIPTIONS

The six diagnostic programs are described below. Areas of responsibility, test type, special optional features, deviations from the standards (explained earlier) and their isolation and diagnosis capabilities are covered. The programs are listed in the sequence in which they would be run in a system "bring-up" environment.

MTR Mode Processor Test

The purpose of the MTR Mode Processor Test is to establish confidence in the basic integrity of the B 1870/B 1860 processor and to verify those functions needed by the Dynamic Processor Test to examine all other processor functions. The MTR Mode Test also checks error conditions and diagnostic/maintenance console operations. These latter checks are performed in the MTR Mode test because they are inconvenient or impossible to accomplish during the Dynamic Processor Tests. The requirements and restrictions inherent in a bring-up, self-test, program require a specialized, step-by-step format. For this reason, the execution procedure for the MTR Mode Test differs considerably from the standard test procedure previously described. Because of this departure from standards, a separate set of instructions are provided in the program listing.

All test cases in the program are diagnostic in nature. The general rules to be applies are as follows:

a. Test a function's control logic by NANO MOVE instructions.

b. Check that the function's result is as expected. When either test fails, the processor is halted. The error indications identify the function being tested, the previously untested control/data paths involved, and where this logic is located (MP-3 cards). In many cases, enough information is available to indicate which portion of logic (one card) or single-card subfunction has failed.

A minimal amount of both blocks of Cache are tested in the MTR Mode Test. The remainder of one block of Cache (selected by the operator) is also tested (default is Block A). The purpose of the latter test is to verify enough Cache storage to execute the Dynamic Processor Test. Successful completion of the above tests proves that the processor meets a confidence level at which the Dynamic Processor Test can be executed under its default conditions. Optional termination at this point may be selected if it is desired to proceed directly to the Dynamic tests. Otherwise, the MTR program can be continued to test the following:

a. Read/Write S-memory.

b. Execution from S-memory (S micro source).

c. S-memory error detection and fetch error halts.

d. Console Switch Compare functions.

e. Execution in the MICRO SOURCE = NORMAL mode.

Dynamic Processor Test

The Dynamic Processor Test, in combination with the MTR Mode Test, is intended to verify all processor functions and Logic for correct operation. Building on the level of confidence provided by the MTR Mode Processor test, verification continues with diagnostic, confidence, and reliability testing. These tests are performed on previously untested and partially tested processor logic.

Overlap testing between this program and the MTR Mode Processor test is handled in two ways:

a. Where the MTR test contains a comprehensive verification of a logical area, the Dynamic Processor Test considers this logic to be functional and performs only a cursory check prior to using it. In the event of a failure, the error description directs the user to the MTR Test for isolation.

b. Where the MTR Test has checked only part of a function (specific cases) of a micro, comprehensive tests are provided in the Dynamic Processor Test. Failure isolation is then provided for each test case.

The Dynamic Processor Test may be executed using three different micro sources. The default condition is the MICRO SOURCE switch setting C (Cache only), in which case each test section is loaded one micro at a time from cassette to Cache and executed from Cache. The user may choose to alter the Run Mode SPAD setting, when initially loading the test, so that the micro source is S or NORMAL. In these cases the entire test will be loaded from cassette to S-,memory. If the S setting is select3ed, micros will be fetched, and executed directly from S-memory. The NORMAL setting causes code to be fetched from S-memory and loaded in Cache (when not already present in Cache) and then executed from there. The block of Cache used for CACHE ONLY execution should be the same as was tested by the MTR Mode Test. Block A of Cache is used by default.

The Dynamic Processor program is divided into logical areas based upon hardware functions and micro groups. Each division is tested in a similar manner as follows:

a. Utilization of the Nano Move (10D) micro to test the basic functions of any previously untested micros in a group. Some test groups have no new (untested) micros.

b. Testing of all variants of each micro and exercising associated registers and data paths with basic test patterns. This is done on a "one-time" basis.

c. Exercising the logical area with reliability type tests (where applicable).

In all cases, detected failures are diagnosed to a functional area on a card. All other operations and procedures are as specified by the preceding standards.

Dynamic Port Interchange-3 Test

The Port Interchange Test utilizes a latch on the Port Interchange (PI) card (U3) that allows data to pass through the PI card and a Port Adapter card, and then echo back to the processor. This program is a dynamic type and uses the reliability testing methods previously defined. The Port Interchange Test program uses the standard defined B 1870/ B 1860 hardware test rules, with the following additional options:

a. Scratchpad location S10A is defined as Test Card, and designates the Port Adapter card to be tested in Section 2. If the contents of the SPAD location are undefined by the user (all zeros), the program will attempt to test all port locations sequentially, resulting in errors at those locations where a Port Adapter card is not present.

b. Scratchpad location S11A is defined as User Data, and is used to store operator-entered data for use in test sections where this option is permitted. The User Data scratchpad contents are used when specified by the dynamic USE DATA switch. (Bit 1 on the console switches = dynamic; bit 1 in the Switch Settings scratchpad = Preselected.)

The Port Interchange Test program deviates from the standard in the following respects:

a. The run mode specifies Cache-only micro sourcing during both loading and execution. An exception to the above is Section 4, which constructs and dispatches an I/O descriptor from S-memory.

b. Defaults to the correct run mode are made without reporting.

This program, by design, overlaps some functions of both the Dynamic Processor Test and the Dynamic S-memory Test. Therefore, the user should refer to either of these programs for further error resolution.

Dynamic S-Memory Test

The Dynamic S-memory Test verifies the integrity of the storage cards, MBU, portions of the processor/memory interface, and the higher level aspects of all memory related micros. The test is primarily a reliability verification program, but contains both diagnostic and confidence test sections. The default operating mode of this test is to load each test section into Cache (only one block is used), and execute exclusively from Cache. In this case, only one test pass is required to test all of S-memory. Available as an option is the Normal execution mode. This latter option loads the complete test into S-memory starting at location 0. The test micros are then fetched to Cache and executed from there, implies. In the Normal mode, S-memory is tested above the program residence area, then the program is moved higher in S-memory and the original program residence area is tested. When the program is residing in other than its original area, the STATE lamp on the console is lit. One pass of this test is defined as testing ALL selected S-memory. Each test section will execute twice (once with, and once without, the STATE lamp on) before incrementing the loop counter. The option of running from the S-memory only mode is not available in this program.

As an additional option, the operator may select base and limit addresses for testing. All other features of this test are consistent with the standards described earlier.

The general purpose of the Dynamic S-memory Test program is to test with the goal of separating the MBU from the storage cards. This is accomplished by means of the diagnostic constructs available for exercising the MBU (11D) micro. The initial memory tests consist of both diagnostic and confidence routines.

When a certain level of confidence in the MBU and processor operations has been established, storage card and addressing test sections appear. These test sections are, for the most part, reliability tests. The storage card test sections attempt to isolate the failure to a storage chip. When multiple bits are incorrect, further analysis of the error condition is attempted to determine which logical area on the storage card or in the MBU is at fault.

Dynamic Cache Test

The Dynamic Cache Test serves to verify performance of the Cache storage elements and the Hit/ Miss/Replace logic in the processor. The test is loaded into S-memory from cassette, with most test sections being executed exclusively from S-memory (some sections are automatically switched to the Normal mode). No "Cache only" mode testing is employed.

Proper execution of this test requires that the following functions have been verified and are operational:

a. All non-Cache processor functions.
b. S-memory storage of data.
c. Execution from S-memory only.

Execution of the program proceeds as follows. First, in the S-memory - only mode, the Cache key storage and key related functions are tested. Following this, the keys are used to address and exercise the micro-store area of Cache. The program then enters the Normal mode and uses the tested keys and micro-store to check the Hit/Miss/Replace logic (resident primarily in the processor).

In checking the keys, diagnostic tests are run first to ensure that they can store data. Next come confidence tests which yield isolation between address and data lines. This same hierarchy is used in testing the micro-store elements. The Hit/Miss/Replace logic tests follow, beginning at the confidence level. This is done because several new processor functions are utilized when a Miss is encountered. When individual testing of the keys, micro-store, and Cache-related processor logic have been completed (one at a time to the confidence level), all three sections are exercised together in reliability tests.

Central System Interaction Test

The Central System Interaction Test program is designed to induce and detect failures that are related to an actual operating environment (MCP complexity). Most sections of the test provide reliability verification, with only limited confidence type verification being performed. No logic-level diagnosis is provided, but complete explanations of the circumstances surrounding the failure are reported. Also included are references to other test programs for further investigation of the function that failed.

The standard operations and procedures are adhered to within this test program, with the following exceptions:

a. Operation is in the NORMAL mode only.

b. LR halts, operating instructions, and register values are reported via I/O (printer or SPO) rather than on the console lamps. In the event of an I/O or system malfunction, the standard console panel procedures may be used as backup.

Field Card Tester

The Field Card Tester is provided as a means of external (out of system) troubleshooting for B 1870/B 1860 logic circuits. This device allows the logic on each plug-in card to be independently exercised and analyzed for proper responses. The Field Card Tester is a portable unit which obtains its operating power directly from the dc voltages present in the Central System. Testing is accomplished by pre-programming the tester to generate control signals appropriate to a particular circuit, exercising that circuit, then examining the results. Result reports from the tests are in the form of 4-digit codes known as "Node Counts" which are compared with published specifications. Complete operating instructions for the Field Card Tester are contained in the Field Card Tester Technical Manual, Form Number 2102 380. Card test data for specific logic cards is a part of the system Test and Field Documentation. Refer to these publications for further information.

Manual Troubleshooting

When machine-assisted troubleshooting is not possible or not desirable, several alternate approaches may be employed. These approaches include, but are not limited to the following:

a. Console tests by manual manipulation of the controls (refer to section 2 of this manual).

b. In-circuit tests utilizing test equipment (primarily voltage measurements and tracing signals with the aid of an oscilloscope).

c. Physical examination of suspected components, including static testing.

The methods used in manual troubleshooting may vary, but a A definite sequence, or set of objectives is common, however, to most successful repair efforts. A typical approach should contain the following elements:

a. Define the problem. This is the most important single requirement and is likely to be the most time-consuming. Determine exactly what the system is doing wrong or failing to do. If, for example, the 1C Micro (register move) is not performed correctly, check the operation of both the source and sink registers, the intermediate data path, and the logic which decodes and implements execution of the micro. Check also to ensure that the micro is reaching the decoding logic properly.

b. Look for obvious solutions. Make sure that a malfunction has actually occurred. Relate problems to recent events such as cleaning, servicing, or the installation of new or replacement components. Look for improperly set controls, accidental disconnections of cables, and other mechanically caused circuit discontinuities. Consider miscellaneous temporary failures, such as mechanical jamming of peripheral equipment.

c. Locate the trouble area. Isolate the fault to a functional area of the system by a process of elimination.

d. Analyze the isolated area. Use the logic schematics and appropriate test equipment to identify the faulty circuit element.

e. Correct the fault through repair or replacement. Attempt to determine the cause of the failure, and take the necessary steps to prevent recurrence.

f. Restore the system to operation. Return all components, cables and subassemblies which have been removed to their proper locations. Correctly set all controls, then verify the repair work by running appropriate test programs.

Special Troubleshooting Procedures

The following paragraphs contain descriptions of troubleshooting procedures that may be useful to the Field Engineer.

USE OF VOLTAGE MARGINS

Occasionally marginal logic problems develop which by their very nature are difficult to isolate. Operating the Central System with the logic voltages set at their upper or lower tolerance levels tends to induce failures at a greater frequency than at the nominal settings. Therefore, use of the voltage margin settings list in table 4-5 is suggested as an aid in diagnosing intermittent logic problems. These settings are to be used at the discretion of the field engineer. Note that it is usually desirable to adjust more than one, or all, supply voltages to the high or low margin at one time. This tends to further aggravate system weaknesses, providing better failure indications.

Table 4-5. Voltage Margins

Voltage	Nominal Setting		Margin High	Margin Low
+4.75	+4.95	±0.010	+5.15	+4.75
- 2.00	- 2.15	±0.010	- 2.05	- 2.25
+12.00	+12.0	±0.100	+12.50	+11.50
- 12.00	- 12.0	±0.100	- 11.50	- 12.50

USE OF CARD EXTENSION

Marginal logic problems sometimes develop which are difficult to isolate even by use of voltage margins. It has been found that extending the suspect logic card (by use of the Logic Card Extender, P/N 2207 1237) tends to induce failures at a greater frequency or cause an intermittent problem to become a solid failure.

USE OF CLOCK CARD

The Clock card has special features incorporated in its design that may be helpful when troubleshooting the B 1870/B 1860 system. The following paragraphs are descriptions of these special features.

Clock Stop

All system clocks (except the SYS7 clock to the MBU), may be stopped whenever it is desired to save the machine state. The Clock Stop function may be triggered by any positive-going signal greater than 30 ns in width. Clock Stop is effected by installing a jumper between the backplane pin on which the desired signal appears and pin 1 YX (or the Stop Test point on the Clock card. The STOP switch (S1 on the clock card) must also be placed to the STOP position. When the control signal goes true, the system clocks are stopped and the desired machine state may be viewed. To restart the clocks, remove the jumper and return the STOP MODE switch to the NORMAL position. Refer to volume 3, section 2 of this manual (Theory of Operation, form number 1095551) for a detailed description of the Clock Stop operation.

Single Pulse

All system clocks may be single-pulsed if it is desired to view the machine states one clock at a time. Single-pulsed clocking is accomplished by placing the CLOCK MODE switch (S2) on the clock card in the SINGLE PULSE position. At this time all clocks halt in the false state, and may thereafter be single-pulsed with the SINGLE PULSE pushbutton. Each time the SINGLE PULSE pushbutton is pressed, all clock outputs emit a synchronous positive pulse, with each clock signal in proper order and at the proper time. Note that the STOP MODE switch must be in the NORMAL mode when attempting to single-pulse the clocks. To restart the clocks, return the CLOCK MODE switch to the CONT position. Refer to volume 3, section 2 of this manual (Theory of Operation, form number 1095551) for a detailed description of the single pulse clock operation.

Special Processor Problems and Scoping Techniques

At times during manual testing, the means for scoping a looping program or stopping a "hanging" program are required. The capabilities available at certain backplane pins can be used to take advantage of these troubleshooting techniques. A description of these procedures and their troubleshooting use are given in the following paragraphs.

PROCESSOR HANG

Occasionally a program may "hang" the processor with the front panel lamps either all ON or all OFF, with the system still in Run condition. At this time, the processor registers may contain valuable information to assist in determining what caused the problem. To avoid having to halt the "hung" processor by way of the CLEAR button (thus clearing the registers), momentarily connect processor backplane pin J1EY (card A3, pin 1EY) to +4.75V. This action causes the S-memory micro time-out to go true, halting the processor without clearing the registers.

NOTE

PERM bit 3 will also be set as a result of this action. Refer to volume 3, section 2 of this manual (Theory of Operation, form number 1095551) for a description of the Halt logic.

DELIBERATE LOOP

When a program hangs or does not run when attempting to execute a microinstruction or a sequence of microinstructions, it is helpful to cause the failing portion of the program to loop continuously. A continuous loop is accomplished by simultaneously pressing the HALT, CLEAR, and START front panel buttons (causing the program to start over again). With this type of loop, the Clear signal will cause the program to restart even if the processor is "hanging."

The procedure for entering the deliberate loop is as follows:

a. Write the failing microinstruction or sequence of instructions in Cache or S-memory, starting at address 0.

b. If the instructions are written into Cache, set MICRO SOURCE switch to C (Cache only). If the instructions are written into S-memory, the MICRO SOURCE switch can be set to either Normal or S (S-memory).

c. If single-step operation is desired, set the SINGLE MIC/CONT toggle switch to SINGLE MIC. Otherwise set this switch to CONT.

d. Connect a 24-pin frontplane ribbon cable from Y of Processor card D3 to Y of processor card E3.

The above cable connection causes GPCLR.AO (Clear) and START.1 to be continuously active. GPCLR.AO clocks every 500 microseconds and START.1 clocks every 2 microseconds, this means that START.1 will occur 12 times between each GRCLR.AO pulse. GRCLR.AO clears all registers (as does the CLEAR button on the D/M panel) each time this signal appears. Cache is also cleared if the MICRO SOURCE switch is not in "C" (Cache only) position. START.1 will start the program each time it appears. In the Step mode, one microinstruction will be executed for each Start pulse.

MEMORY OUT OF BOUNDS

Occasionally, a processor may indicate an attempt to access S-memory beyond its actual size. To determine the exact point in the program where this attempt is being made, connect a jumper between Processor backplane pins J1FY (card A3, pin 1FY) and J1EY (card A3, pin 1EY). This action ORs the S-memory Out of Bounds signal and the S-memory Micro Time-out Signal, causing the program to be halted at the time the access is attempted.

SCOPE JITTER

When scoping a looping program, it occasionally is difficult to observe the signals because of jitter. In such cases it may be helpful to disable Memory Refresh by tieing MBU backplane pin GOCY (card S3, pin OCY) to 4.95 Volts with a jumper. Note that using this procedure requires execution from the Cache memory in the Cache-only mode, since any data in S-memory will be lost. If deliberate looping is being used, the Cache-only mode must be used to avoid clearing Cache.

Use of 7E (Read/Write Cache) Micro

The 7E micro is used to write or read Cache memory and to read the Cache Key storage. This micro uses two registers for memory addressing (A and FA). The addressing format for both registers is the same (refer to figure 4-3). The console variants (Write from Console Switches or Read to Console Lamps) utilize the A register for memory addressing. The Diagnostic variants address memory by use of the FA register. Refer to figure 4-4 for the variants of the 7E Micro.

When a word is written into Cache, the data field length is 16 bits plus 1 parity bit, totaling 17 bits. The 17th (parity) bit must be set for odd parity for each word written. The data format is shown in figure 4-5. During the Diagnostic Write, data is read from the X, Y, T, and L registers. The data in each register is also 17 bits long. The sequence of operation on a Diagnostic Write is as follows:

a. Save the A register.
b. Move the contents of the FA register to the A register.
c. Write the X register to Cache, word 0; write key (A) to Cache (key); Set Validity bit in key; generate and write parity in key.
d. Write the contents of the Y register to Cache, word 1.
e. Write the contents of the T register to Cache, word 2.
f. Write the contents of the L register to Cache, word 3.
g. Restore the A register.

NOTE
The key information is the same for all write accesses.

When reading from Cache during a Diagnostic Read, the data will be displayed in the Y register. The data is again 17 bits long, consisting of 16 data bits and 1 parity bit.

On a Cache Key Read variant, both keys (A and B), validity bits, parity bits, Hit status, and the LRU (Least Recently Used) bit are moved to the Y register. The format of the data in the Y register is shown in figure 4-6.

If a Cache memory failure occurs, determine which bit is failing and use figure 4-7 to locate the apparently faulty storage chip. The chip designations that are enclosed in parentheses on the chart are for Cache Block B; all others are Cache Block A.

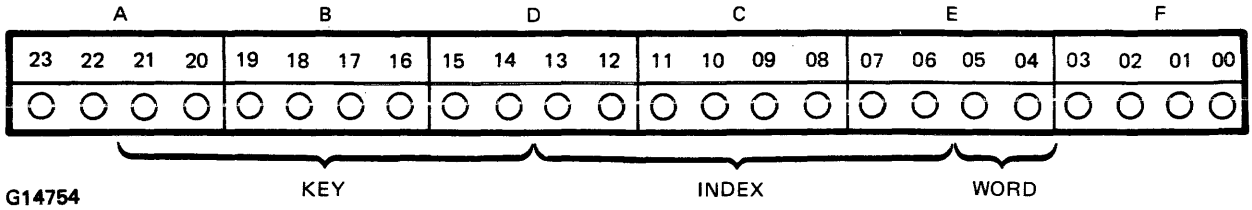


Figure 4-3. 7E Micro Addressing (A and FA Registers)

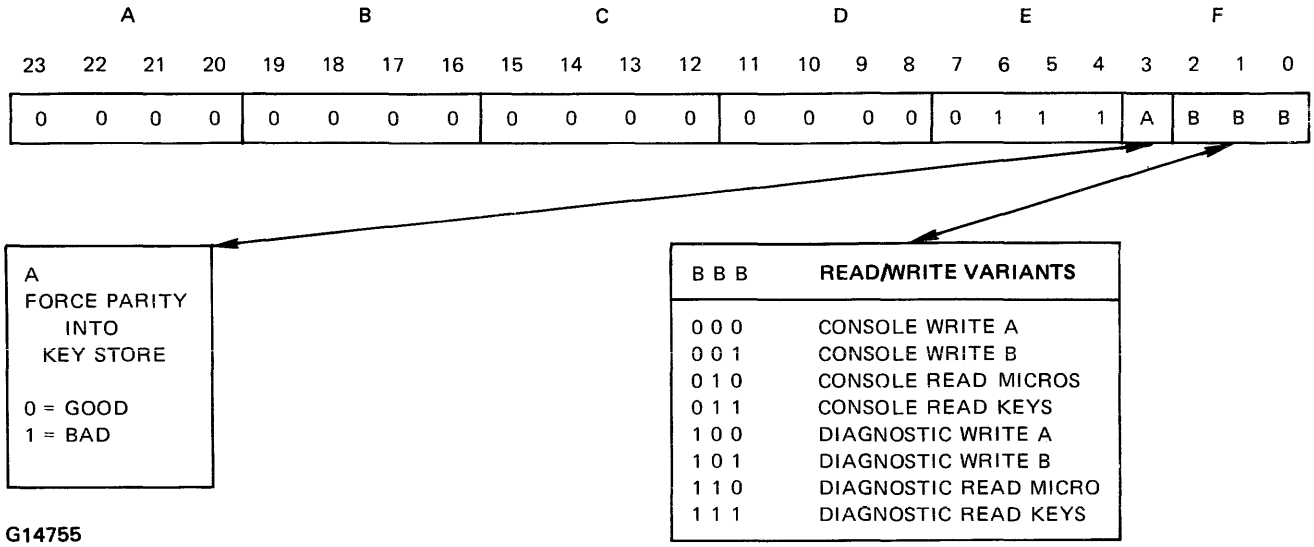


Figure 4-4. Read/Write Cache Micro (7E)

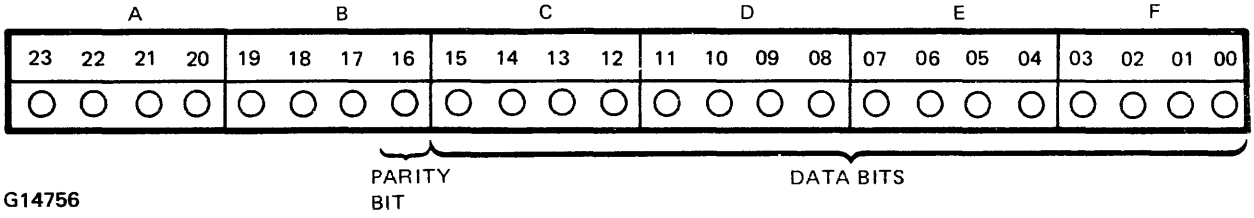


Figure 4-5. 7E Micro Data Format

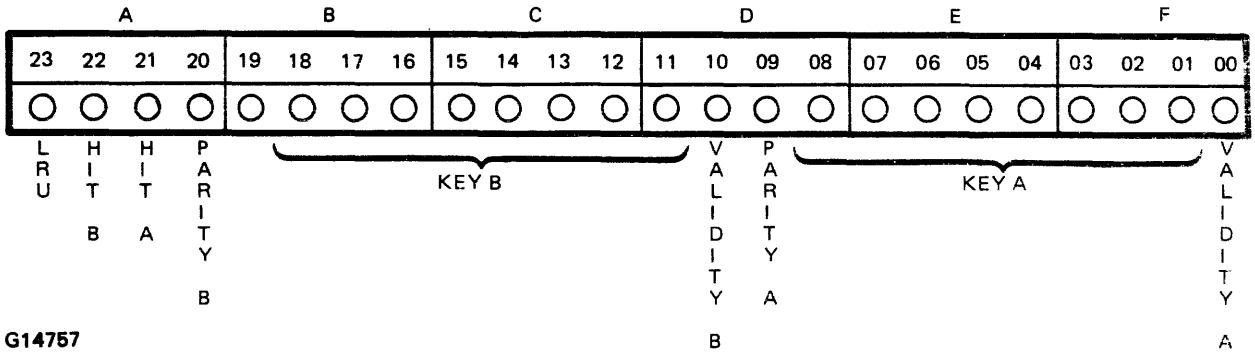


Figure 4-6. Cache Key Bit Assignment

MICRO BIT NO.	RW07 CHIP	LFAN LATCH
00 A (B)	G0 (G2)	A7 (A8)
01 A (B)	A0 (A2)	
02 A (B)	H0 (H2)	
03 A (B)	B0 (B2)	
04 A (B)	I0 (I2)	C7 (C8)
05 A (B)	C0 (C2)	
06 A (B)	J0 (J2)	
07 A (B)	D0 (D2)	
08 A (B)	K0 (K2)	D7 (D8)
09 A (B)	E0 (E2)	
10 A (B)	L0 (L2)	
11 A (B)	F0 (F2)	
12 A (B)	B1 (G1)	E7 (E8)
13 A (B)	C1 (H1)	
14 A (B)	D1 (I1)	
15 A (B)	E1 (J1)	
16 A (B)	F1 (K1)	

CACHE MICRO STORE

KEY BIT NO.	RW07 CHIP
VAL A (B)	K5 (K4)
KY0 A (B)	J5 (J4)
KY1 A (B)	I5 (I4)
KY2 A (B)	H5 (H4)
KY3 A (B)	G5 (G4)
KY4 A (B)	F5 (F4)
KY5 A (B)	E5 (E4)
KY6 A (B)	D5 (D4)
KY7 A (B)	C5 (C4)
PAR A (B)	B5 (B4)

CACHE KEY STORE

G14758

Figure 4-7. Cache Memory Chip Location (Card B3)

Use of 9D (Monitor) Micro

The 9D micro is used (by position) to signal programmatic events. The micro has no function other than to produce a one-pulse signal for use by external test equipment. This capability is used in software development to record the number of times another micro or subroutine is executed. For troubleshooting work, the monitor pulse is most often used for oscilloscope triggering. The monitor pulse appears on the frontplane pin ZY and backplane pin 0BX of logic card E3. A typical application of the 9D micro is to examine the execution of another micro which is suspected of failing. To do this, a small micro program consisting of the 9D micro, the suspect micro, and a branch-backward instruction is composed. This routine is then loaded in memory, address, and executed. Since the program terminates in a Branch Back to Start instruction, continuous repetitions are performed. While this is occurring, the logic functions exercised by the suspect micro may be examined with a scope, using the monitor pulses for triggering. Depending on variant selection of the two least-significant bits (0 and 1), The 9D micro may generate up to four different backplane monitor signals. The names of these signals and their backplane locations and variant selections are as follows:

MONTOREO	H6BX	True if last two bits are 00.
MNTRO.EO	H6CX	True if last two bits are 00
MNTR1.EO	H6DX	True if last two bits are 01.
MNTR2.EO	H6EX	True if last two bits are 10.

A typical monitor routine would consist of the following micros (expressed in hexadecimal):

0900	9D (Monitor) micro.
10A1	Suspect micro, e.g., 1C (move X to Y).
D003	13C (Branch Back) micro.

Use of 11D (Diagnostic Read/Write S-Memory) Micro.

The 11D Micro is used for diagnostic tests on the Memory Base Unit (MBU), Port Interchange (PI), and Port Adapter (PA). The various diagnostic tests (see figure 4-8 for the micro format) which can be accomplished are as follows:

a. Write S-memory.
b. Read S-memory.
c. Echo Address.
d. Echo Write Data.
e. Read Port Interchange Latch.
f. Echo Data via Port Interchange/Port Adapter.
g. Read and Clear Error Log.

The FA register is used to address memory for the Write/Read variants. Refer to figure 4-9 for the FA register address format.

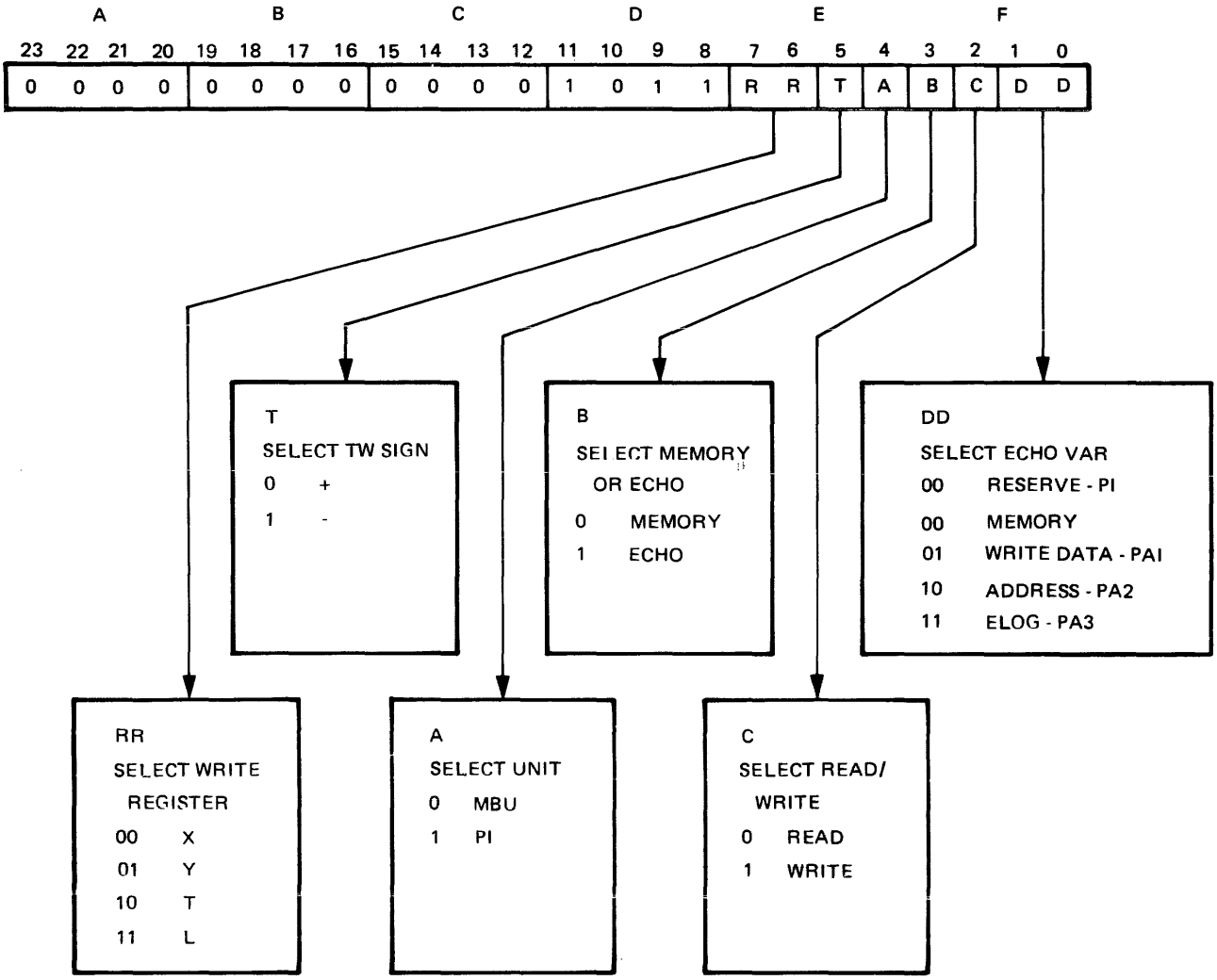


Figure 4-8. Diagnostic Read/Write S-memory (11D)

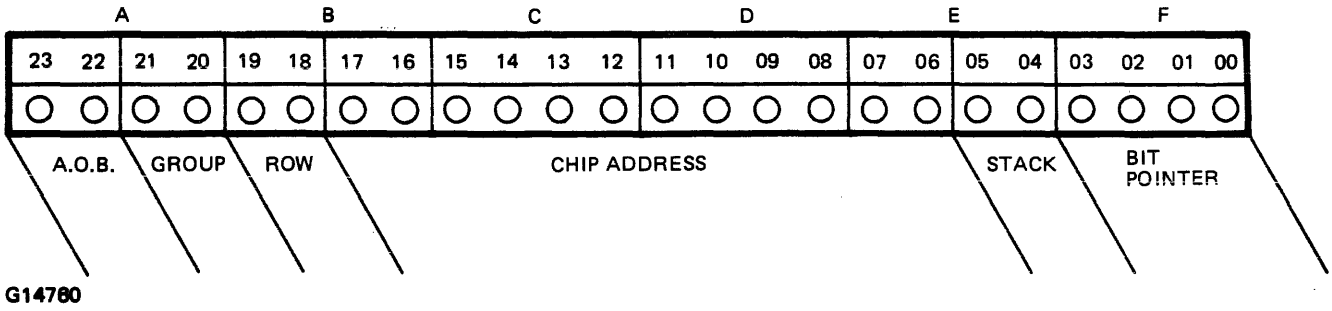


Figure 4-9. FA Register Address Format As Viewed On Console Lamps

The Diagnostic Write causes 22 bits (16 data and 6 Error Correction Code) to be stored. No actual error correcting or reporting is performed for this operation. The Diagnostic Write access must be in the forward direction, and must be on stack boundaries. (The bit pointer must point at bit 0 of the stack.)

The Diagnostic Read causes 22 bits of a storage word to be read out. An odd parity bit is supplied with the 16 data bits. Single-bit errors are not reported. If a single-bit error is detected within the 16 data bits, the odd parity bit is inverted, causing it to actually represent even parity.

The Diagnostic Echo Address variant instructs the MBU-3 to modify and return the address sent to it. This address is modified in either the forward direction or the reverse direction, depending upon FDS (Field Direction Sign). The address returned is ADDR+16 if FDS=0 or ADDR-16 if FDS=1. The Y register contains the modified data.

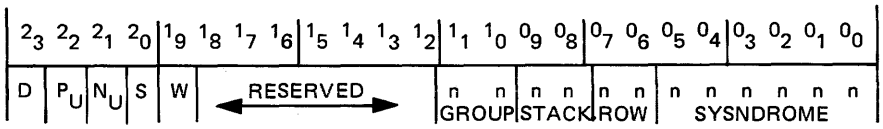
The Diagnostic Echo Write Data variant instructs the MBU-3 to return the write data sent to it. The Y register contains the echoed data.

The Read Port Latch variant causes the data in the port interchange latch to be moved to the processor.

The Echo Data Via PI and PA variants causes data to be written to the PI latch, and then returned to the processor by either the PI or any of three port adapters.

The Diagnostic Read and Clear Error Log variant is not an access to S-memory but rather to the Error Log register. The Error Log contents are moved to the Y register; then the Error Log is cleared at the end of the cycle. If the Error Log indicates an S-memory failure (refer to figure 4-10 for Error Log interpretation), the failing storage chip may be identified by using figure 4-11 (Group/Stack location of S-memory cards in the card housing). Figures 4-12 and 4-13 are useful in locating storage chips on the S-memory storage board.

S–MEMORY ELOG INTERPRETATION



D = DUPLICATE PU, NU, OR S ERROR
PU = PROCESSOR ACCESSED UNCORRECTABLE ERROR
NU = NON-PROCESSOR ACCESSED UNCORRECTABLE ERROR
S = SINGLE BIT CORRECTED ERROR

*W = (0) ERROR ON READ
(1) ERROR ON WRITE

SYNDROME INTERPRETATION

SYNDROME (HEX)	MEMORY BIT
@01@	21
@02@	20
@04@	19
@08@	18
@0B@	15
@0D@	14
@0E@	13
@10@	17
@13@	12
@16@	11
@19@	10
@1A@	09
@1C@	08
@20@	16
@23@	07
@25@	06
@26@	05
@29@	04
@2C@	03
@31@	02
@32@	01
@34@	00

* REPORTED ONLY UPON DETECTION OF A SINGLE-BIT CORRECTED ERROR.
@ SIGNIFIES HEXADECIMAL

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Figure 4-10. Error Log Interpretation

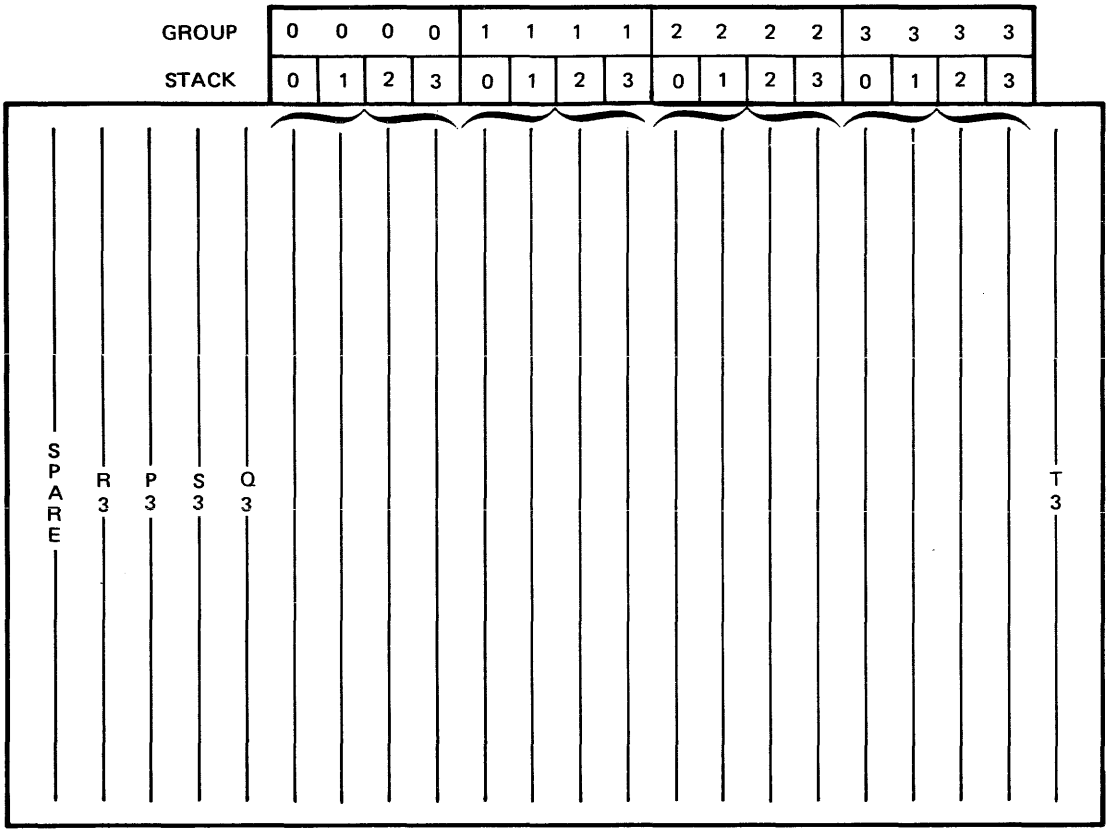

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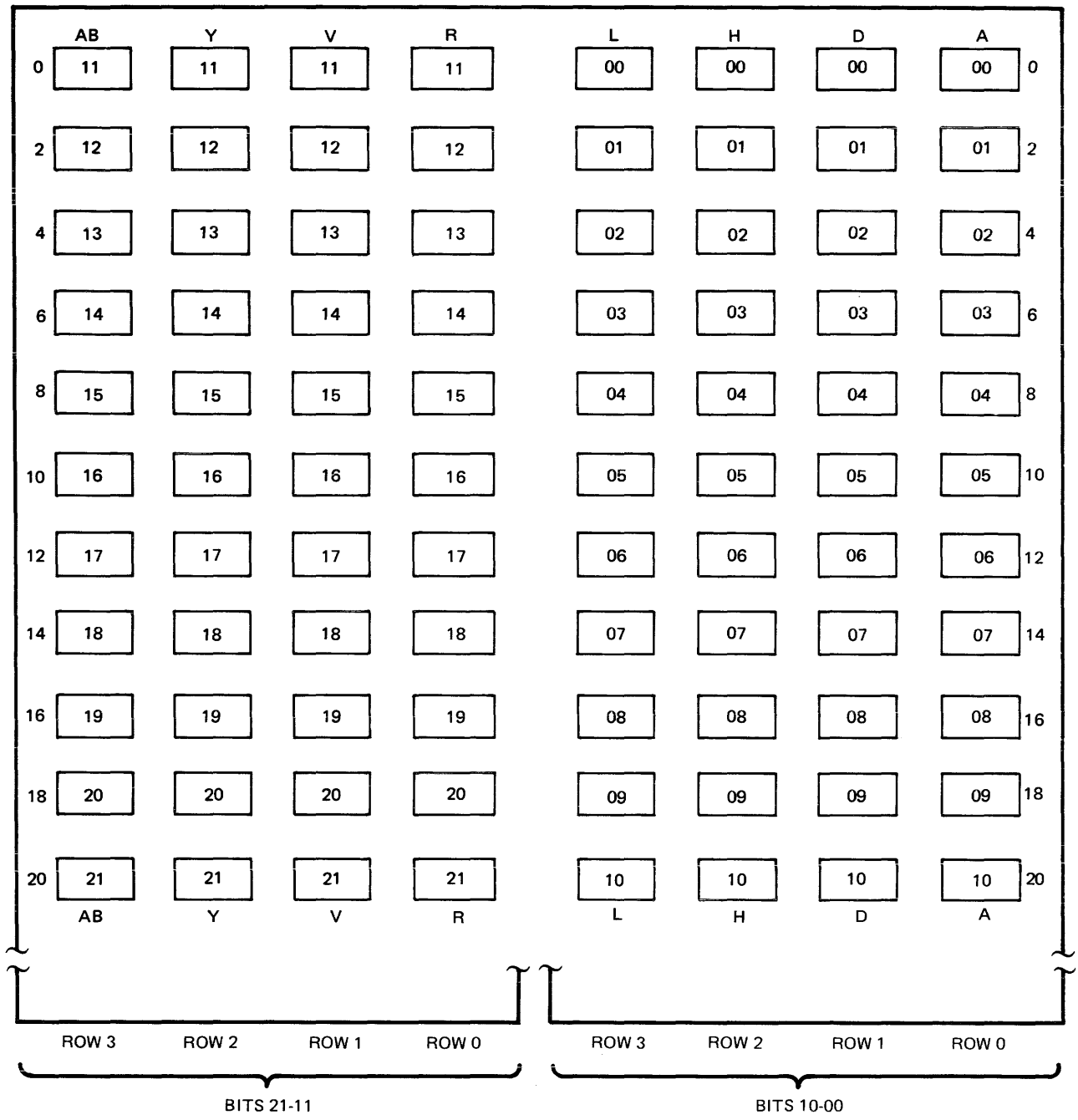
Figure 4-11. Memory Board Group/Stack Interpretation

MEMORY BIT	00	01	02	03	04	05	06	07	08	09	10	ROW
STORAGE CHIP LOCATION	A0	A2	A4	A6	A8	A10	A12	A14	A16	A18	A20	00
	D0	D2	D4	D6	D8	D10	D12	D14	D16	D18	D20	01
	H0	H2	H4	H6	H8	H10	H12	H14	H16	H18	H20	02
	L0	L2	L4	L6	L8	L10	L12	L14	L16	L18	L20	03

MEMORY BIT	11	12	13	14	15	16	17	18	19	20	21	ROW
STORAGE CHIP LOCATION	R0	R2	R4	R6	R8	R10	R12	R14	R16	R18	R20	00
	V0	V2	V4	V6	V8	V10	V12	V14	V16	V18	V20	01
	Y0	Y2	Y4	Y6	Y8	Y10	Y12	Y14	Y16	Y18	Y20	02
	AB0	AB2	AB4	AB6	AB8	AB10	AB12	AB14	AB16	AB18	AB20	03

G14763

Figure 4-12. Memory Board Chip Locator (Table)



NOTES: DRAWING IS STYLIZED; SHOWS ONLY STORAGE PORTION OF BOARD. NUMERALS WITHIN BLOCKS (CHIPS) ARE BIT NUMBERS. (REFER TO FIGURE 4-12.)

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Figure 4-13. Memory Board Chip Locator (Physical Layout)

SUBASSEMBLY REMOVAL AND REPLACEMENT

Performing maintenance and/or adjustment work on the various portions of the Central System may require the removal of subassemblies to allow access to a desired area. Instructions for removal and replacement of all significant system subassemblies are provided in the following paragraphs.

Diagnostic/Maintenance Panel

The D/M panel is mounted to the cabinet frame by means of hinges attached at the right-hand side, and may be swung open as if it were a door. The panel is held closed by magnetic latches and may be opened by pulling outward on the left side. With the panel open, access may be gained to the rear of the hardware mounted thereon. The panel itself should never require removal from the cabinet (except in cases of physical damage), but opening is a necessary step in removing and/or replacing the subassemblies mounted on it.

Console Switches and Indicators

The 24 console switches and corresponding 24 indicator lamps, plus several other control switches and indicators are mounted on a printed circuit board. Removal of the board is necessary if component replacement is required. To replace a component, perform the following steps:

a. Open the D/M panel.
b. Remove the circuit board cables.
c. Remove the eight retaining nuts which attach the console board to the front panel.
d. Remove the printed circuit board.
e. Unsolder the defective component.
f. Install a new component in the vacant position and solder in place.
g. Replace the console components in reverse order from which they were removed.

To remove the cassette drive from the Operator's panel for repair or adjustments, proceed as follows, (see figure 4-14):

a. Switch system power OFF.
b. Remove the left side panel from the console table, and the panel covering the cassette mounting latches on the front of the table.
c. Locate the two mounting latches pertaining to the cassette device to be removed. These latches are at the center of the left and right sides of the cassette chassis, and must be adjusted from the front with a screwdriver.
d. Loosen the mounting latches and rotate them (about 1/4 turn) until the cassette chassis is free.
e. Remove the cassette drive by pulling directly backward.
f. The drive may now be placed on the table top for adjustments or repair while still electrically connected to the shared cassette board. (The cables attached are of sufficient length to allow such extension.)
g. If repair or adjustment is needed on the shared cassette board, the board may be removed by pulling outward on the six black retainers located at the top and bottom.
h. Replacement of the devices may be accomplished by performing the above steps in reverse order.

Logic Power Supply Booster

The logic power supply booster functions as a slave to the existing power supply, and is not usable separately. Each booster increases the +4.75 and –2.0V logic current delivery capability of the B 1870/B 1860 system by an additional 80 amps. The B 1870/B 1860 System may use up to two boosters for a total added current capacity of 160 amps.

Most required troubleshooting can be accomplished with the booster supply still mounted in the system. The Inverter board can be removed from the supply for easier access when testing.

NOTE
The cable connecting the inverter board to the control board is long enough to permit the inverter board to be placed on the console table.

If the booster supply must be removed from the system, proceed as follows (see figure 4-15):

a. Turn system power OFF.
b. Remove the left side cover.
c. Disconnect the two jacks (J2 and J6) and the two cables from the booster assembly +4.75 and –2.00V output bus bars.
d. Remove the four (4) retaining screws which attach to the supply cabinet frame and lift the supply from the cabinet.
e. Replacement of the supply may be accomplished by performing the above steps in reverse.

Logic Power Supply

The logic power supply is mounted in the base of the system cabinet. The supply may be extended from the cabinet on tracks, and rotated upwards for access to the underside. (See figure 4-16.)

To gain access to the interior of a logic power supply, proceed as follows:

a. Turn system power OFF.
b. Disconnect the three bus bar terminals at the rear of the supply (+4.75V, GND, –2.0V outputs). Also disconnect plugs JLG, J12A, and J12B. The AC Power cable need not be disconnected.
c. Remove the four retaining screws which attach the front panel of the supply to the cabinet frame. The supply may now be extended from the cabinet.
d. Remove the top and/or bottom covers of the supply as required.

WARNING
The logic power supply contains high voltage circuits.

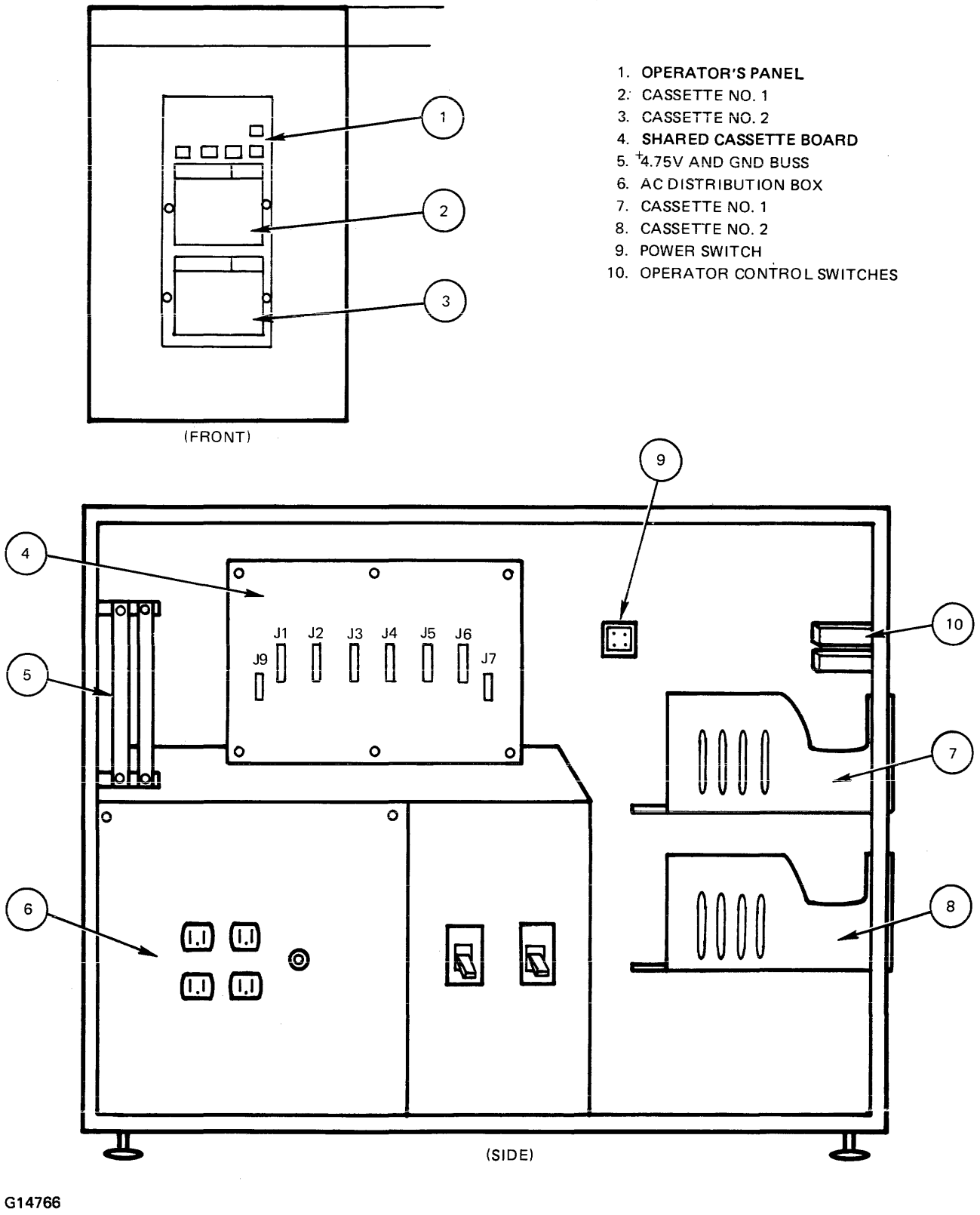
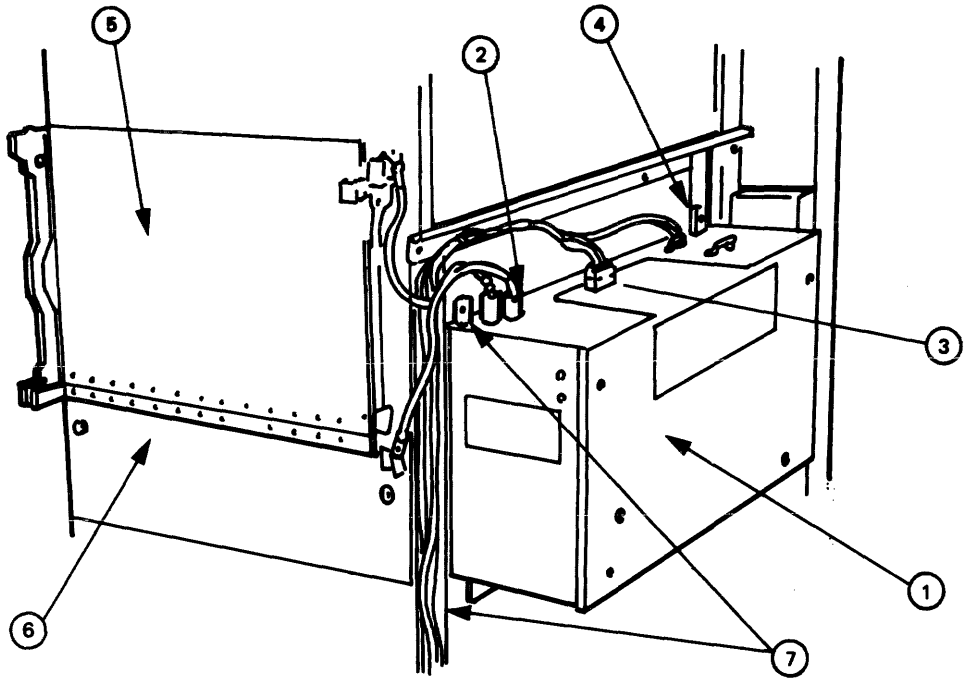


Figure 4-14. Operators Panel and Cassette Subsystem (Physical Configuration)



1. BOOSTER POWER SUPPLY
2. 4.75V AND -2.0V CABLES
3. J2 (SENSE LINES)
4. J6 (AC POWER)
5. CARD HOUSING BACKPLANE
6. SYSTEM BLOWER ASSEMBLY
7. RETAINING SCREWS
   (2 OTHERS ON OPPOSITE END)

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Figure 4-15. Booster Power Supply Removal

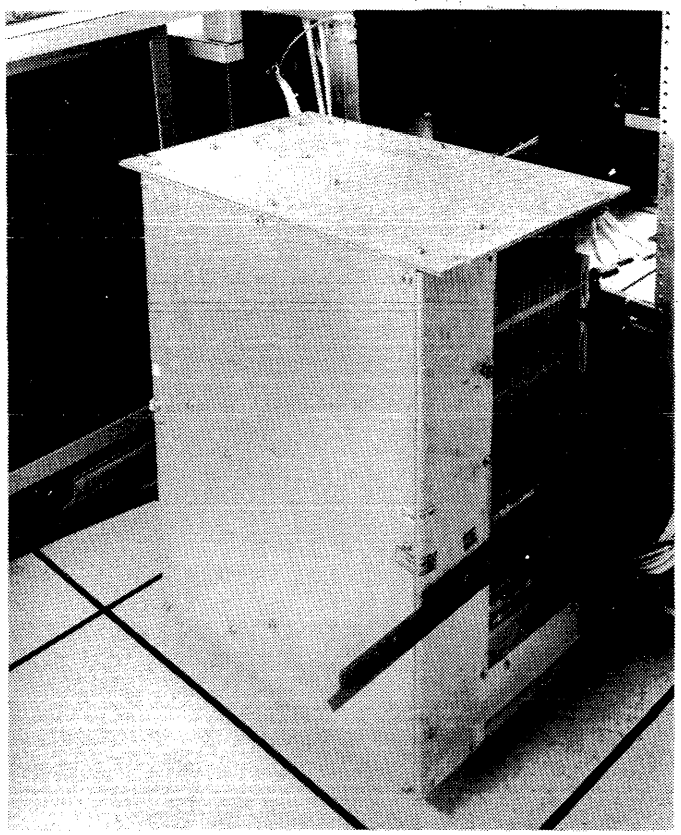

Figure 4-16. Logic Power Supply Extended and Tilted Upward

Logic Cards and Cables

Each logic card and memory card is equipped with plated contacts which mate with matching sockets mounted on the backplane. In addition, many cards are also equipped with frontplane sockets into which logic cables (having matching plugs) are inserted.

CAUTION

These connections are fragile, and must be handled carefully to avoid damage. Insertion and removal instructions for the cards and cables are as provided in the following subsections.

Removal

a. Cables may be removed by moving the plastic connector handle up and down slightly while exerting a gentle outward pull. Do not twist the connectors or move from side to side. Remove coaxial cables by pulling straight out.

b. Logic cards should be removed with the aid of an extraction tool, P/N 2207 6228. To use the tool, locate the hole near the lower front corner of the desired card and insert the pry pin into it (pointed end of tool downwards). Pull outwards on the handle until release of the backplane connectors is felt. The card may now be readily removed from its slot. Refer to figure 4-17.

Replacement

a. When preparing to replace a logic card, first ascertain that it is oriented properly. The component side must be to the right when facing the frontplane. Slide the card carefully into the slot, making sure that the top and bottom edges are inside the guide tracks. When the limit of travel is reached, seat the backplane connectors by giving a firm push (using both hands) on the front edge of the card. Check to ensure that the front edge of the card is even with those on either side of it.

b. Replace logic cables by visually aligning the socket and plug, then push straight together. Replace coaxial cables in the same way.

Component Replacement

Replacement of individual circuit components in the B 1870/B 1860 Central System should be performed in a manner consistent with that employed for other devices utilizing printed circuit technology. However, since the B 1870/B 1860 uses integrated circuit chips and wire-wrap terminals extensively, the special precautions to be observed when working with these parts are included in the following subsections.

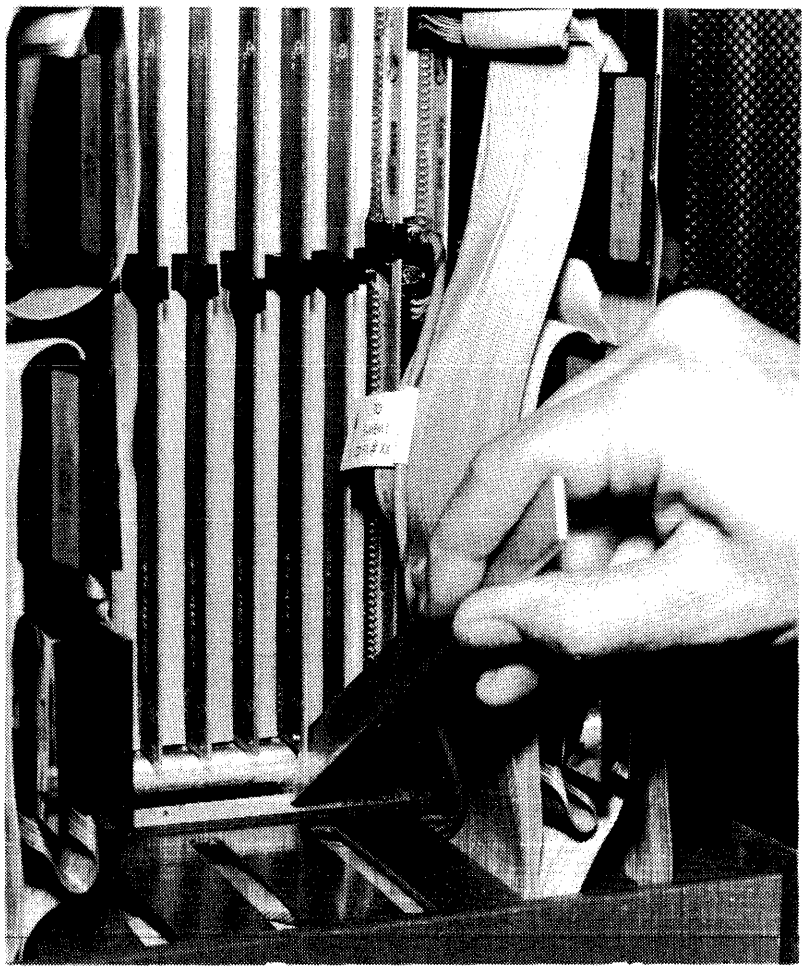

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Figure 4-17. Logic Card Removal

Chip Replacement

To replace a faulty IC chip, proceed as follows:

CAUTION

Never permit a hot soldering iron to come in contact with the insulated bus bars which cross the card.

CAUTION

Use of excessive heat will damage the card etching.

a. Using a clean low heat soldering iron and a desoldering tool, remove the solder from each leg of the chip. This should be done from the solder side of the board.

b. Using a soldering aid or small screwdriver, press each leg toward the chip body (on component side). This should break loose any residue of solder which may remain.

c. Lift out the chip with a chip removal tool. Do not pry with a screwdriver or other tool, as this can break the etching. Refer to figure 4-18.

NOTE

Desolder pump tool is P/N 1622 2887.
Chip removal tool is P/N 1622 4206.

Making Wire-Wrap Connections

Wire-wrap connections provide a rapidly made, high-quality joint, and are adaptable to automatic manufacturing processes. However, the tolerances involved are quite small, and require careful attention to detail when such connections are made by hand.

WIRE-WRAP SPECIFICATIONS

The following specifications discussed in the following paragraphs must be observed when making wiring changes in the field.

Number of Turns

The minimum number of turns (per connection) of bare wire is 5, and maximum number is 7. The maximum number of turns of insulation preceding the bare wire is 3 for any connection.

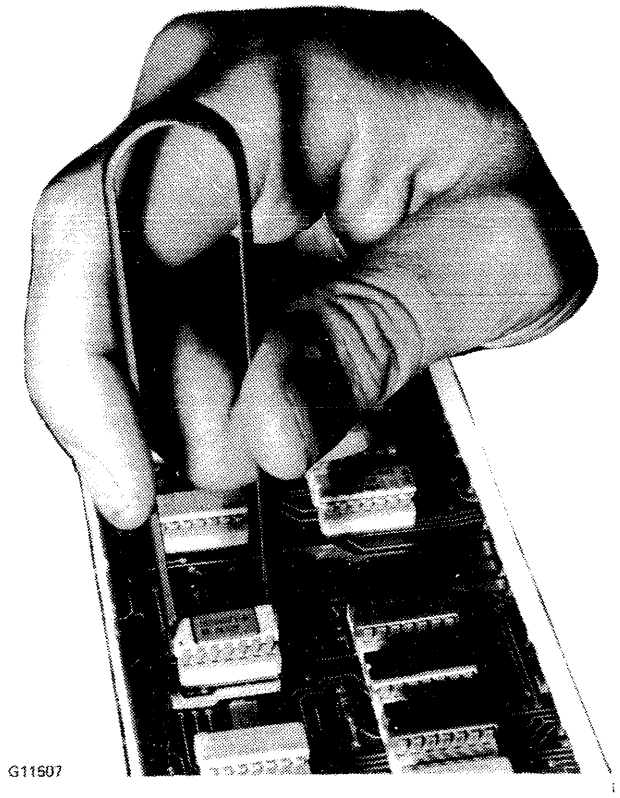


Figure 4-18. IC Chip Removal

Insufficient Insulation

Wire insulation shall be no greater than 1/32 inch from wire wrapped connections.

Wire and Terminal Contact

Bare wire must make contact with the terminal at all corners.

Separation of Turns

Turns may have a maximum separation of one-half the thickness of wire being used to make the wrapped connection.

Excessive Tail Wire

The wire tail shall be construed as being "that end of bare wire which follows the last wrap." The wire tail shall be parallel to the terminal surface within 1/32 of an inch.

Overlapping of Turns

This condition is caused when succeeding wraps overlap the ones previously made. If overlaps exist, it will be necessary to make a new connection.

Clearance

There shall be at least 1/32 inch clearance between grid pattern connections, terminals, bare wire and components.

Height

The maximum clearance between the connector block and the first turn of the first connection shall be 1/16 inch.

Height for Single Wrap

The maximum height for a single wrap shall be 1/4 inch.

Height for Two Wraps

The maximum height for two wrapped connections shall be 1/2 inch.

Unwrapping

The connection shall be capable of being unwrapped from the wire wrap terminal without breaking. The unwrapping operation shall be done with a standard unwrapping tool only, so as to ensure the life of the wire-wrap terminal.

Wire Re-Use

NOTE

If a wire has previously been wrapped, the portion of the wire which was wrapped cannot be used again.

If the old wire is not long enough to strip off enough insulation to permit another wrap, a new wire must be routed in its place. Soldering a wrapped connection directly at the terminal is not recommended.

Terminal Reuse

Prior to re-wrapping, the terminal should be inspected for damage. When there is plating loss, corrosion or other damage which would cause a poor connection, the terminal must be replaced.

APPROVED WIRE WRAP INSTALLATION PROCEDURE

To make an acceptable wire wrap connection, proceed as follows (Refer to figure 4-19):

NOTE

A separate wire wrap tool is available for each guage of wire which is used. Be sure that the correct tool is on hand before beginning work.

a. Remove the insulation from the end of the wire. Approximately 1 1/4 inches of wire is required for a six-turn connection of wire.

b. Select the wire-wrap tool applicable for the specific guage wire used.

c. Place the tool over the wire as shown in figure 4-19, B.

d. Anchor the wire as shown in figure 4-19, C and insert the tool over the pin as shown in the D portion of figure 4-19.

e. Rotate the tool in a clockwise direction. The wire will wrap around the pin as shown in figure 4-19, E and F. Too much downward pressure will cause the wire to bunch.

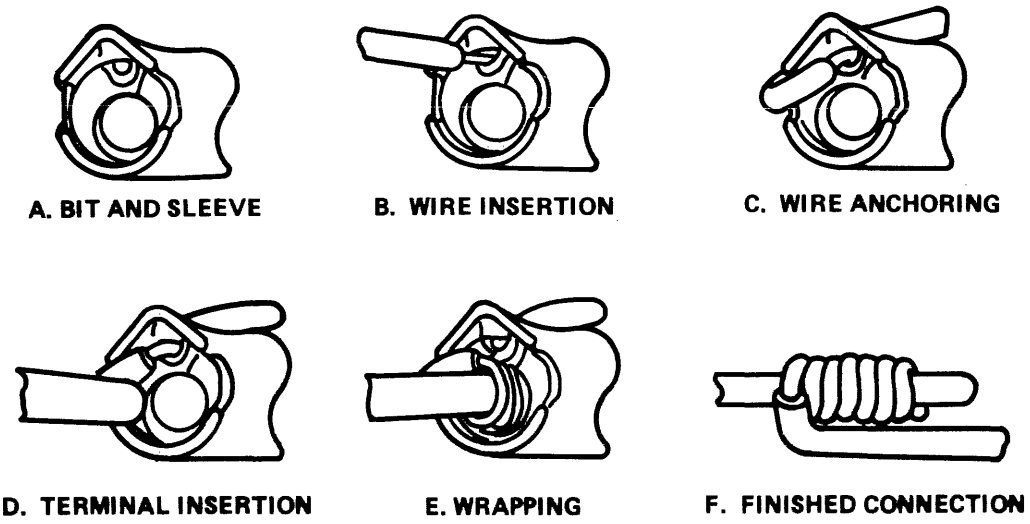


Figure 4-19. Wire-Wrap Installation

SECTION 5
ADJUSTMENTS

INTRODUCTION

This section contains adjustments which may be used to restore a system to proper operation. Included are procedures for testing the various adjustable circuits against specifications for diagnostic purposes.

NOTE

This section is a guide, and the specifications provided herein may be changed at a later date. Refer to the system T & F Documents for proper timing specifications.

CENTRAL SYSTEM CLOCK CHECKS

The central system clock is generated by a 12-megahertz crystal-controlled oscillator whose sine wave output is converted to an approximate 6-MHz square wave signal alternating between 4.95 volts and 0 volts. The clock signal is subjected to buffering and delays before being passed to the processor, MBU and I/O Base. Refer to volume 3 section 2 of this manual (Theory of Operation, form number 1095551) for a detailed description of the clock circuit. Normally, clock adjustments are unnecessary because the timing is preset at the factory. However, should the timing relationship between the various clock signals fall outside the specifications outlined in this test procedure (or the T & F Documents), the discrepancy may be corrected by changing delay taps.

Test Equipment Required for Clock Adjustments

A Tektronix 465 oscilloscope with 10:1 probes (or equivalent) is required to perform the clock adjustments.

NOTE

All timing must be checked at nominal voltages.

Clock Card Test Procedure

The following procedure verifies that the timing of the system clocks and related clock signals is within acceptable limits. Perform the following steps in the order listed:

a. Set S-1 on the clock card to NORMAL mode.

b. Set S-2 on the clock card to CONTINUOUS mode.

c. Connect the channel 1 scope probe to Reference Clock (Clock card backplane pin OWX), and the channel 2 scope probe to Processor Clock 1 (backplane pin OYX). Trigger the scope from channel 1.

d. Verify the width and frequency of the Reference Clock signal at the 1-volt level, as shown in figure 5-1.

e. Check Processor Clocks 1 and 2 using the channel 2 probe, with the scope being triggered by channel 1 (Reference Clock). Check the delay, width and frequency of these clock signals at the 1-volt level. Refer to figure 5-2 for delay and figure 5-3 for width specifications.

f. Check the I/O Clock output at backplane pin 1ZX for proper delay, width and frequency. Use the channel 2 scope probe. Refer to figure 5-4.

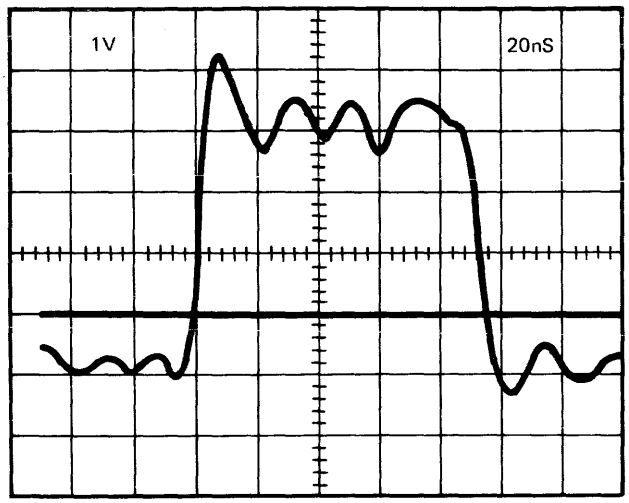
g. Move the channel 2 probe to MBU Clock ("doghouse" connector 7 on the frontplane of the clock card). Verify the delay, width and frequency of the MBU Clock (System Clock 1) at the 1-volt level. Refer to figure 5-5 for procedure.

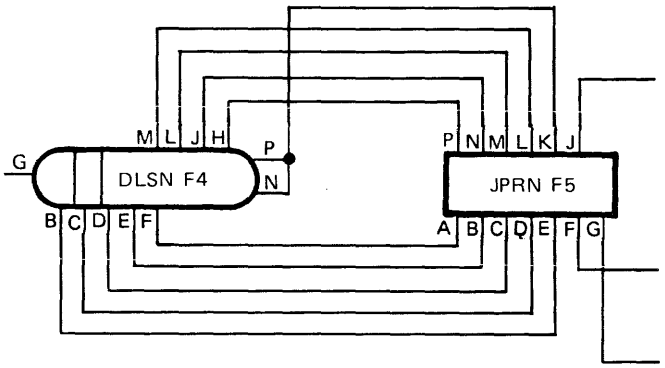
h. Check the remaining system clocks (System Clocks 1 to 6) in the same manner as step g, using scope probe 2.

i. Switch S-2 to SP (single pulse) and verify that on every push of S-3 (SINGLE PULSE switch) that the Reference clock output emits a positive pulse of the proper width. All clocks emit a synchronous positive pulse at this time, having proper delay and width with respect to Reference Clock. The single pulse is generated when S-3 is pushed (not when it is released).

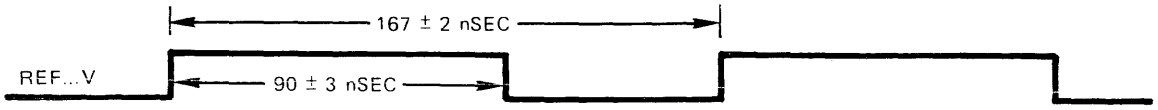
PROCESSOR CLOCK SKEW CHECKS

The B 1870/B 1860 Processor Clock is calibrated on the Clock Card. However, individual processor cards also have on-board clock nets that require calibration. The calibration procedure guarantees proper delay from the card clock input (backplane pin OWX) to the first element of each clock net on that card. Each card contains a different number of nets to be calibrated.





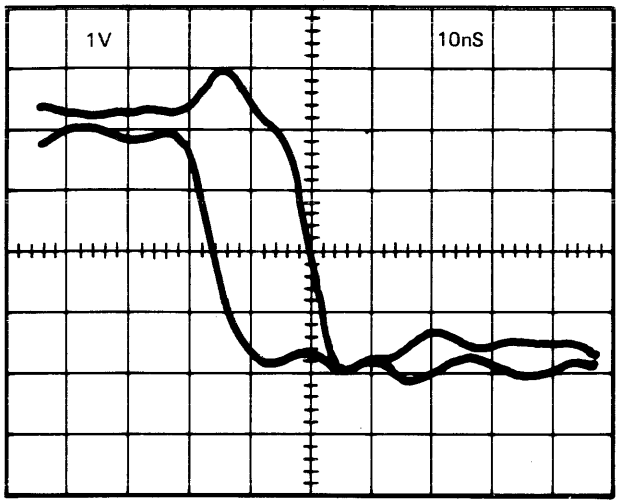
A.	TRIGGER	INTERNAL, POSITIVE
B.	CHANNEL ONE	REF...V (OWX)
C.	CHANNEL TWO	PCLK1.VO (OYX)
D.	HORIZONTAL	2 uSEC/cm. X10 ON (20nSEC/cm.)
E.	VERTICAL	1 VOLT/cm.
F.	TRIGGER SOURCE	CHANNEL ONE
G.	DISPLAY MODE	CHANNEL ONE
H.	MACHINE STATE	IDLE
I.	ADJUSTMENT	ADJUST JPRN F5G

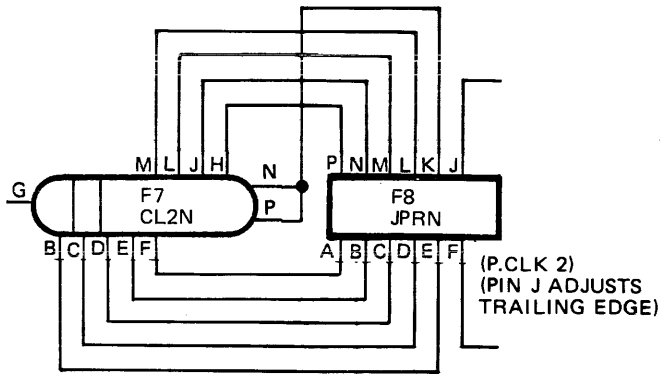


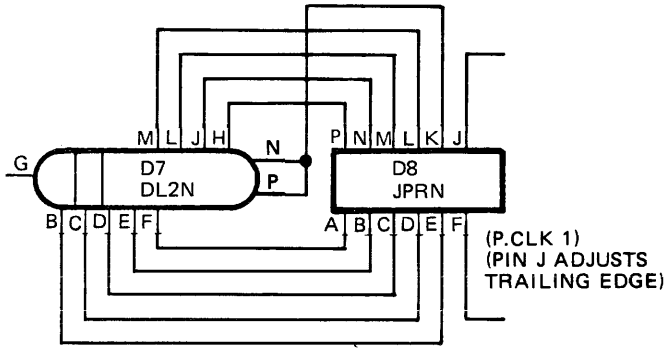
MEASURES AT +1 VOLT LEVEL
VOLTAGES AT NOMINAL

G14771

Figure 5-1. Reference Clock

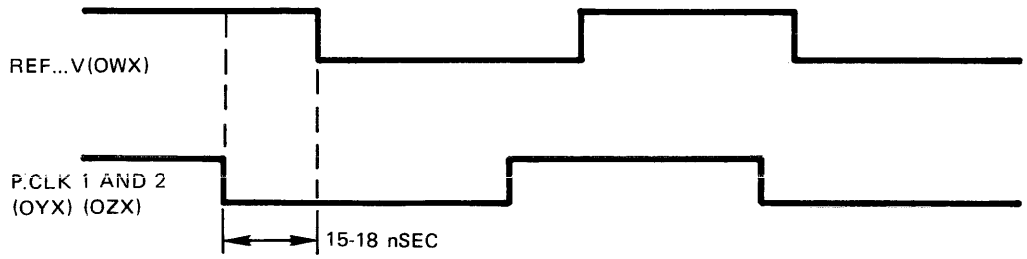






XE6Y (OYX CLOCK CARD P.CLK 1)
XE6Z (OZX CLOCK CARD P.CLK 2)

A.	TRIGGER	INTERNAL, POSITIVE
B.	CHANNEL ONE	XE6W (OWX CLOCK CARD)
C.	CHANNEL TWO	P.CLK 1 (OYX), P.CLK 2 (OZX)
D.	HORIZONTAL	1 uSEC/cm. X10 ON (10 nSEC/cm.)
E.	VERTICAL	1 VOLT/cm.
F.	TRIGGER SOURCE	CHANNEL ONE
G.	DISPLAY MODE	ALTERNATE
H.	MACHINE STATE	IDLE
I.	ADJUSTMENT	JPRN AT D-8(P.CLK 1), JPRN AT F-8(P.CLK 2) (SEE ABOVE FOR PROPER PINS)

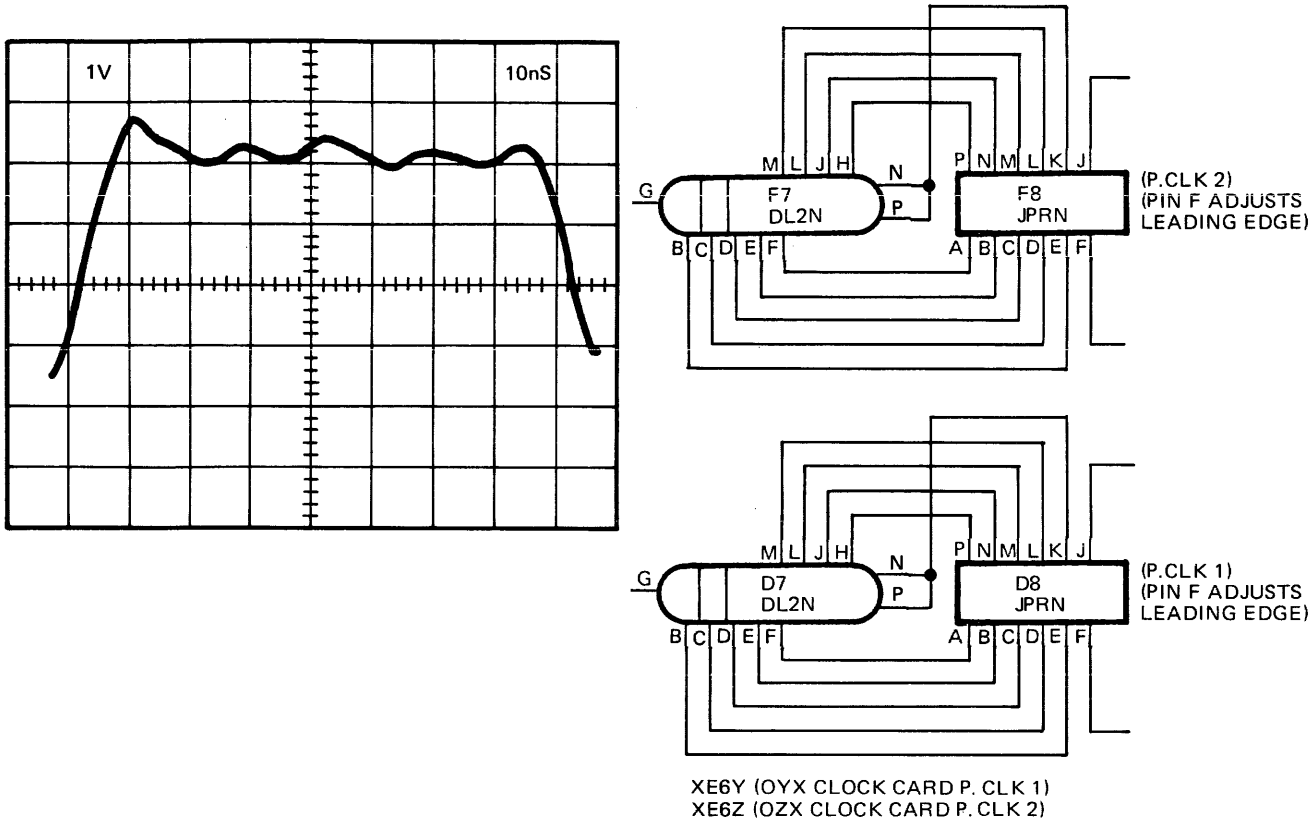


THE TRAILING EDGE OF P.CLK 1 AND 2 LEADS THE TRAILING EDGE OF REF...V BY 15-18 nSEC.

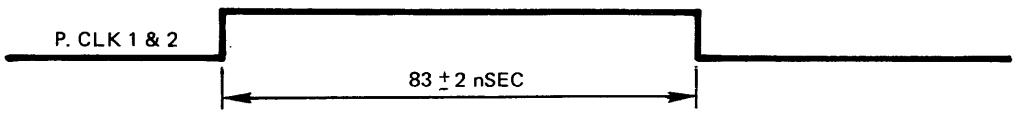
MEASURE AT +1 VOLT LEVEL
VOLTAGES AT NOMINAL

G14772

Figure 5-2. P.CLK Skew



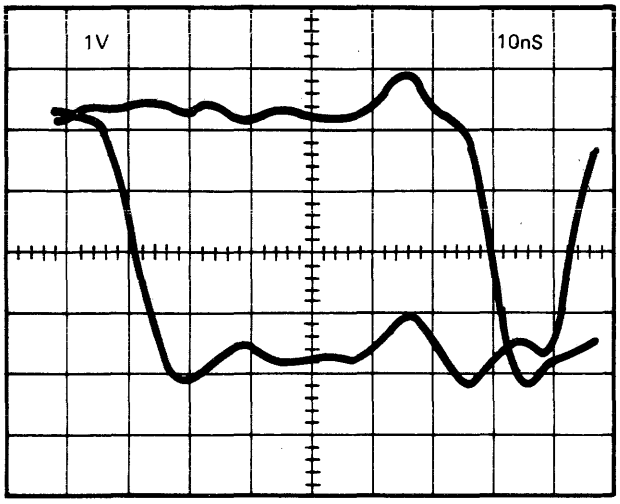
A.	TRIGGER	INTERNAL, POSITIVE
B.	CHANNEL ONE	XE6W (OWX CLOCK CARD)
C.	CHANNEL TWO	P.CLK 1 (OYX), PCLK 2 (OZX)
D.	HORIZONTAL	1 uSEC/cm. X10 ON (10 nSEC/cm.)
E.	VERTICAL	1 VOLT/cm.
F.	TRIGGER SOURCE	CHANNEL ONE
G.	DISPLAY MODE	CHANNEL TWO ONLY
H.	MACHINE STATE	IDLE
I.	ADJUSTMENT	JPRN AT D-8-F)P.CLK 1), JPRN AT F-8-F(P.CLK 2)

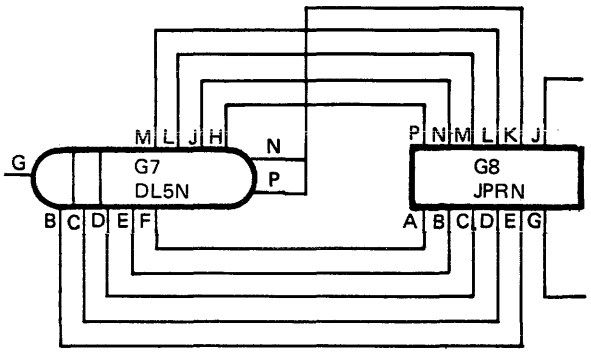


MEASURE AT +1 VOLT LEVEL
VOLTAGES AT NOMINAL

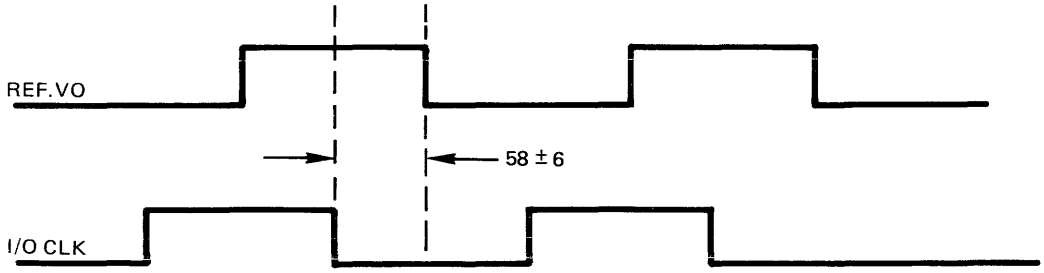
G14773

Figure 5-3. P.CLK Width





A.	TRIGGER	INTERNAL, POSITIVE
B.	CHANNEL ONE	XE6W (OWX) REF...V0
C.	CHANNEL TWO	XE7Z (1ZX) IOCLK.V0
D.	HORIZONTAL	1 uSEC/cm. X10 ON (10 nSEC/cm.)
E.	VERTICAL	1 VOLT/cm.
F.	TRIGGER SOURCE	CHANNEL ONE
G.	DISPLAY MODE	ALTERNATE
H.	MACHINE STATE	IDLE
I.	ADJUSTMENT	JUMPER CHIP AT G8 (SEE DIAGRAM)

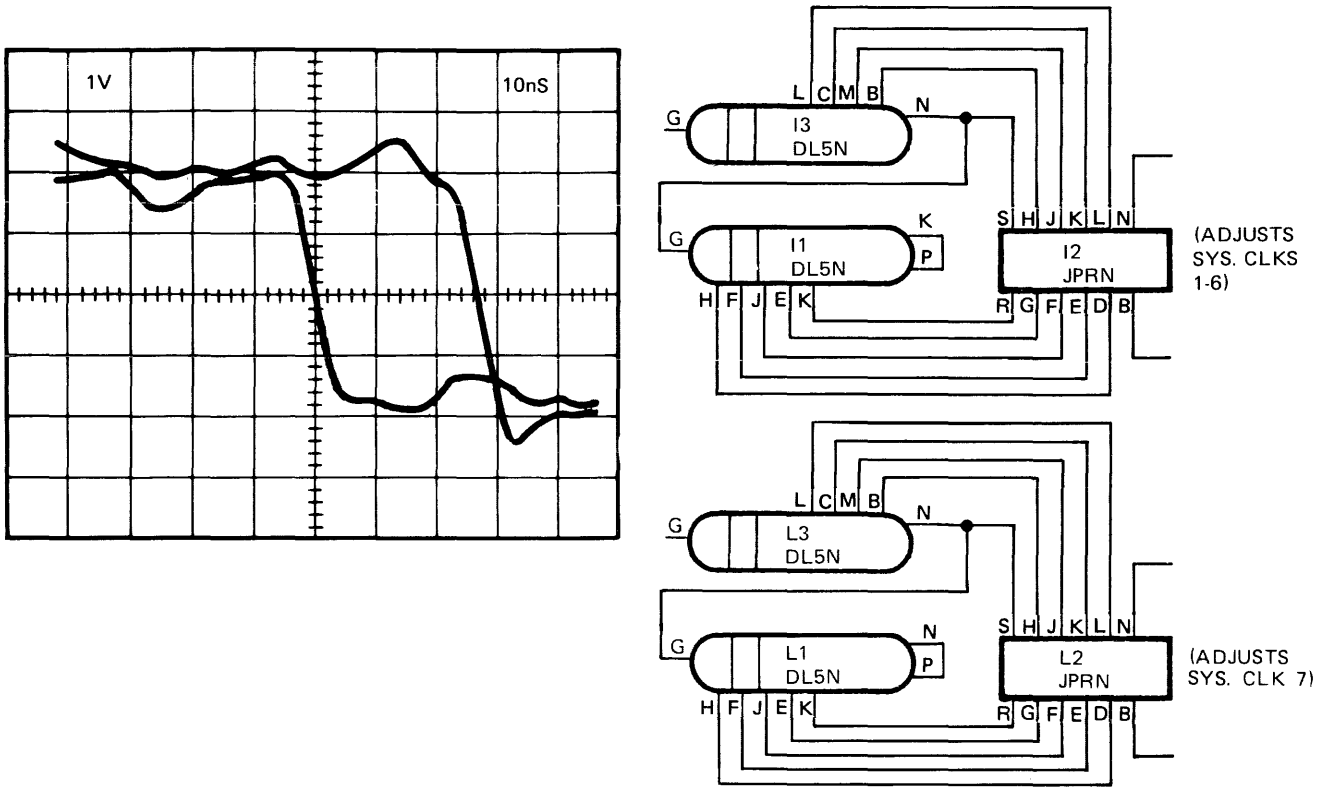


THE TRAILING EDGE OF I/O CLOCK SHOULD LEAD THE TRAILING EDGE OF REF.VO BY 58-6 nSEC.

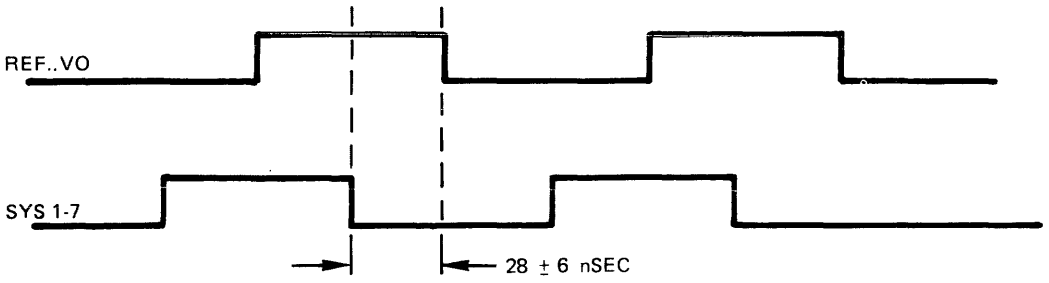
MEASURE AT +1 VOLT LEVEL
VOLTAGES AT NOMINAL

G14774

Figure 5-4. I/O Clock



A.	TRIGGER	INTERNAL, POSITIVE
B.	CHANNEL ONE	XE6W (OWXCLOCK CARD)
C.	CHANNEL TWO	CLOCK CARD DOGHOUSE, SYS. CLOCKS 1-7
D.	HORIZONTAL	1 uSEC/cm. X10 ON (10 nSEC/cm.)
E.	VERTICAL	1 VOLT/cm.
F.	TRIGGER SOURCE	CHANNEL ONE
G.	DISPLAY MODE	ALTERNATE
H.	MACHINE STATE	IDLE
I.	ADJUSTMENT	JPRN AT I-2 ADJUSTS CLOCKS 1-6, JPRN AT L-2 ADJUSTS CLOCK 7



MEASURE AT +1 VOLT LEVEL
VOLTAGES AT NOMINAL

G14775

Figure 5-5. System Clocks 1-7

Test Equipment

The following test equipment is required for the Processor Clock skew checks:

a. Tektronix 465 oscilloscope with 10:1 probes (or equivalent).

b. Logic Card Extender (P/N 2207 1237).

Processor Card Test Procedure

The clock skew calibration procedures for the various processor cards are shown in figures 5-6 through 5-14. Perform steps A through I for each card, ensuring that each net listed is calibrated within 22 to 25 nanoseconds of PCLK.VO (at backplane pin OWX of the card being tested). Note that each card to be checked must be extended with a card extender.

SCRATCHPAD TIMING ADJUSTMENTS

Scratchpad is located on three different processor cards (H3, K3, M3). Each card contains a timing adjustment for one-third of scratchpad.

NOTE

These cards must be extended to gain access to the scratchpad clock logic.

Test Equipment

The following test equipment is required for the scratchpad timing adjustments: Tektronix 465 oscilloscope with 10:1 probes (or equivalent), and Logic Card Extender, (P/N 2207 1237).

Scratchpad Test Procedure

Perform the following procedure to verify that the scratchpad clock timing is within acceptable limits:

a. Extend the card to be tested with card extender.

b. Load 002000 (HEX) into the M register.

c. Place the MICRO SOURCE switch (D/M panel) in the FROZEN M position.

d. Place the processor in the run mode and press the START button.

e. Set the scratchpad skew as shown in figure 5-15 and the scratchpad width as shown in figure 5-16.

TOP OF A-STACK TIMING ADJUSTMENT

The adjustments for Top of A-Stack (TAS) is located on two processor cards (C3 and D3). These cards must be extended to gain access to the Stack Clock.

Test Equipment

The following test equipment is required to perform the TAS clock adjustment: Tektronix 465 oscilloscope with 10:1 probes (or equivalent), and Logic Card Extender (P/N 2207 1237).

TAS Test Procedure

The following procedure verifies that the timing of TAS clocks are within acceptable limits:

a. Extend the D3 card with the card extender.

b. Load 000074 (HEX) into the M register.

c. Place the MICRO SOURCE switch (D/M panel). in the FROZEN M position.

d. Place the processor in the run mode and press the START button.

e. Set TAS timing by following figure 5-17.

f. Repeat steps a thru e for the C3 card.

NOTE

Cache memory timing (following) may be checked at the same time as TAS because the Cache timing adjustment is the same as TAS on card C3. Check and set TAS on card D3 then check card C3.

CACHE MEMORY TIMING ADJUSTMENTS

The adjustment for Cache timing is located on processor card C3. The timing must be set for writing to both blocks A and B. Note that this card need not be extended to be checked.

Test Equipment

A Tektronix 465 oscilloscope with 10:1 probes (or equivalent) is required for the Cache memory timing adjustments.

NOTE

If TAS timing was checked and is correct, the Write Block A and B timing should be correct. If the timing is incorrect a component problem may exist in the Cache Write circuit.

Cache Test Procedure

The following procedure verifies that the timing of Cache Write is within acceptable limits:

a. Load 000074 (HEX) into the M register.

b. Place the MICRO SOURCE switch (D/M panel). in the FROZEN M position.

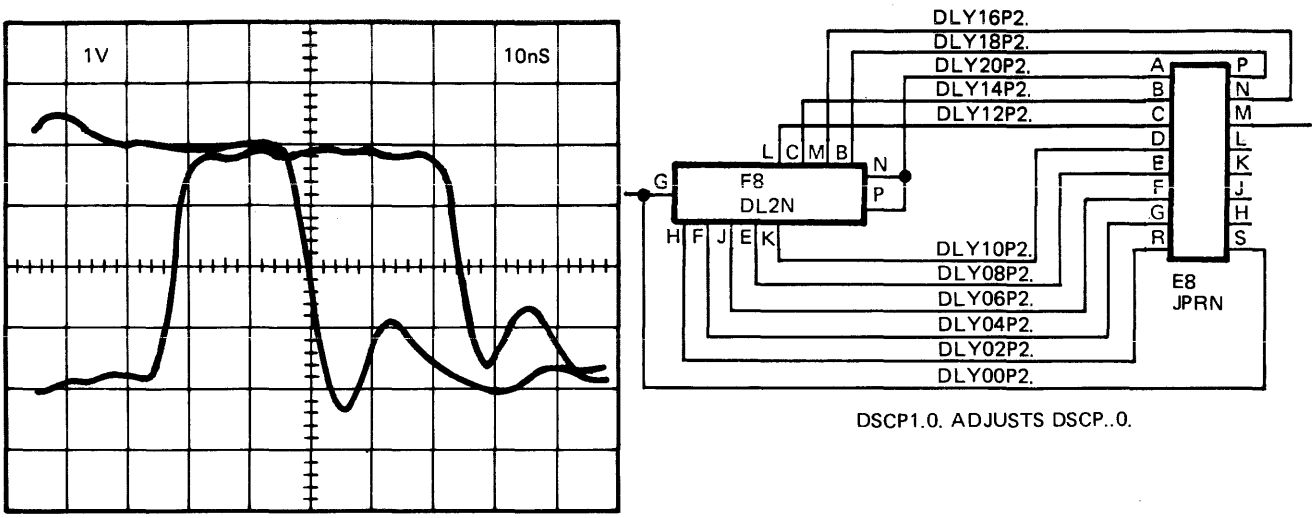
c. Place the processor in the run mode and press the START Button.

d. Check Write Block A (WBA) by following figure 5-18.

e. Check Write Block B (WBB) the same way as WBA, but load the M register with 000075 (HEX).

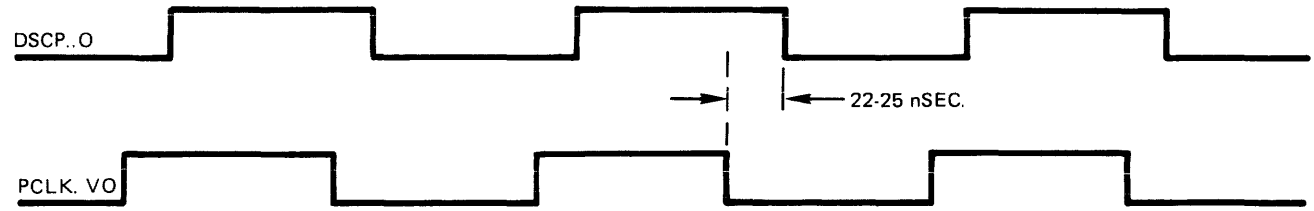
S-MEMORY TIMING ADJUSTMENTS

The S-memory timing adjustments are located on MBU card P3. Refer to the T & F Documents for proper calibration procedures and specifications.



CLOCK SKEW MUST BE ADJUSTED BETWEEN THE POINT WHERE THE CLOCK ENTERS THE CARD, AND THE POINT WHERE THE CLOCK IS ACUTALLY FED TOA CLOCKED DEVICE.

A.	TRIGGER	INTERNAL, POSITIVE
B.	CHANNEL ONE	PCLK .V0 (OWX)
C.	CHANNEL TWO	DSCP..0. (F9J)
D.	HORIZONTAL	1 uSEC/cm. X10 ON (10 nSEC/cm.)
E.	VERTICAL	1 VOLT/cm.
F.	TRIGGER SOURCE	CHANNEL ONE
G.	DISPLAY MODE	ALTERNATE
H.	MACHINE STATE	IDLE
I.	ADJUSTMENT	JUMPER CHIP AT E8 (SEE DIAGRAM)

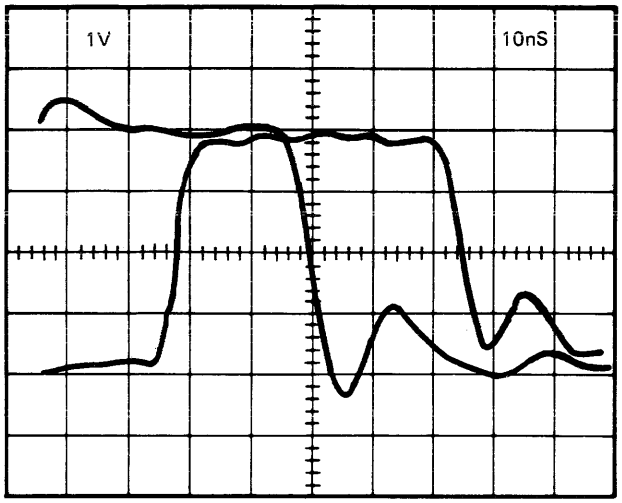


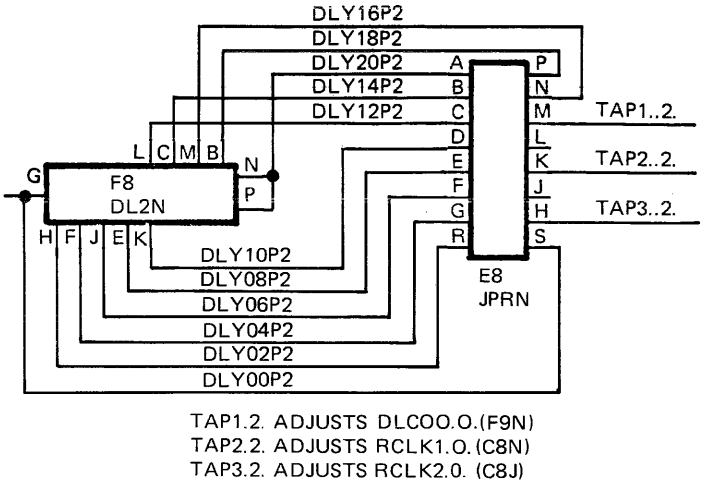
THE TRAILING EDGE OF PCLK.VO SHOULD LEAD THE TRAILING EDGE OF DSCP.O BY 22-25 nSEC.

MEASURE AT +1 VOLT LEVEL
VOLTAGES AT NOMINAL

G14776

Figure 5-6. Processor Clock Skew (A3)

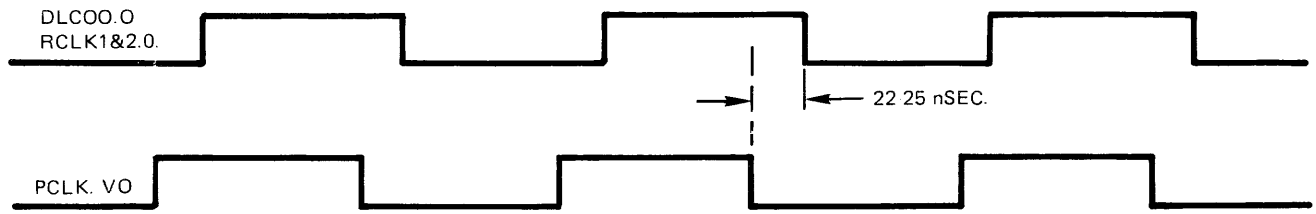




TAP1.2. ADJUSTS DLCOO.O.(F9N)
TAP2.2. ADJUSTS RCLK1.O.(C8N)
TAP3.2. ADJUSTS RCLK2.0. (C8J)

CLOCK SKEW MUST BE ADJUSTED BETWEEN THE POINT WHERE THE CLOCK ENTERS THE CARD, AND THE POINT WHERE THE CLOCK IS ACTUALLY FED TO A CLOCKED DEVICE.

A.	TRIGGER	INTERNAL, POSITIVE
B.	CHANNEL ONE	PCLK .V0 (OWX)
C.	CHANNEL TWO	DLCOO & RCLK1 & 2
D.	HORIZONTAL	1 uSEC/cm. X10 ON (10 nSEC/cm.)
E.	VERTICAL	1 VOLT/cm.
F.	TRIGGER SOURCE	CHANNEL ONE
G.	DISPLAY MODE	ALTERNATE
H.	MACHINE STATE	IDLE
I.	ADJUSTMENT	JUMPER CHIP AT E8 (SEE DIAGRAM)

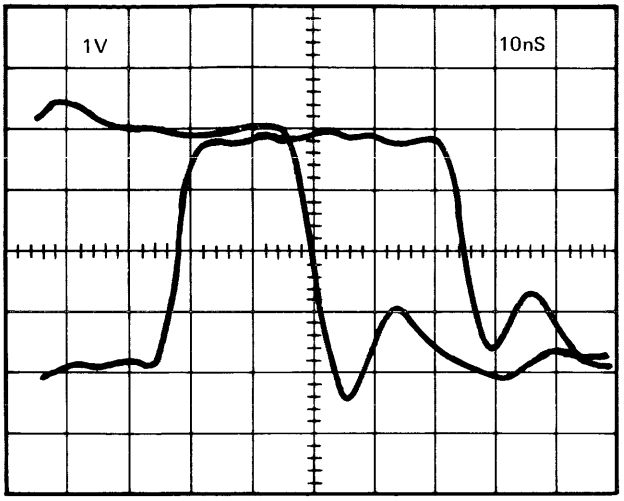


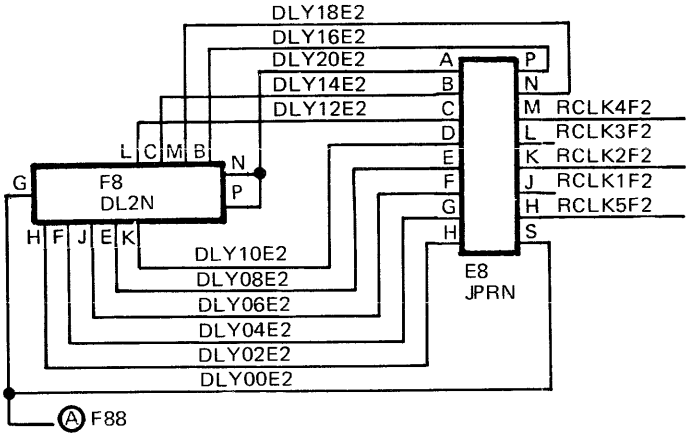
THE TRAILING EDGE OF PCLK.VO SHOULD LEAD THE TRAILING EDGE OF RCLK1 & 2.0. BY 22-25 nSEC.

MEASURE AT +1 VOLT LEVEL
VOLTAGES AT NOMINAL

G14777

Figure 5-7. Processor Clock Skew (C3, D3)

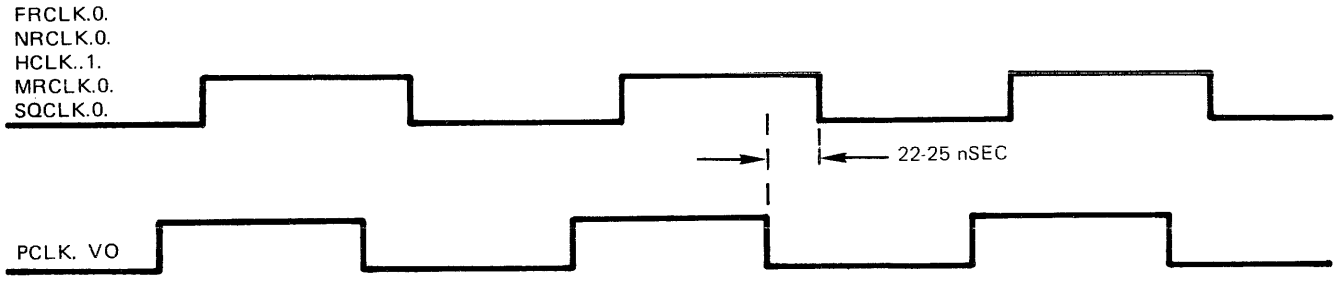




NET LIST

RCLK5F2. ADJUSTS HCLK..1. (B8K)
RCLK1E2. ADJUSTS RMCLK.0. (C8J)
RCLK2E2. ADJUSTS SQCLK.0. (G8N)
RCLK3E2. ADJUSTS NRCLK.0. (G8J)
RCLK4E2. ADJUSTS FRCLK.0. (C8N)

A.	TRIGGER	INTERNAL, POSITIVE
B.	CHANNEL ONE	PCLK .VO (OWX)
C.	CHANNEL TWO	SEE NET LIST ABOVE
D.	HORIZONTAL	1 uSEC/cm. X10 ON (10 nSEC/cm.)
E.	VERTICAL	1 VOLT/cm.
F.	TRIGGER SOURCE	CHANNEL ONE
G.	DISPLAY MODE	ALTERNATE
H.	MACHINE STATE	IDLE
I.	ADJUSTMENT	JUMPER CHIP AT E8 (SEE DIAGRAM)

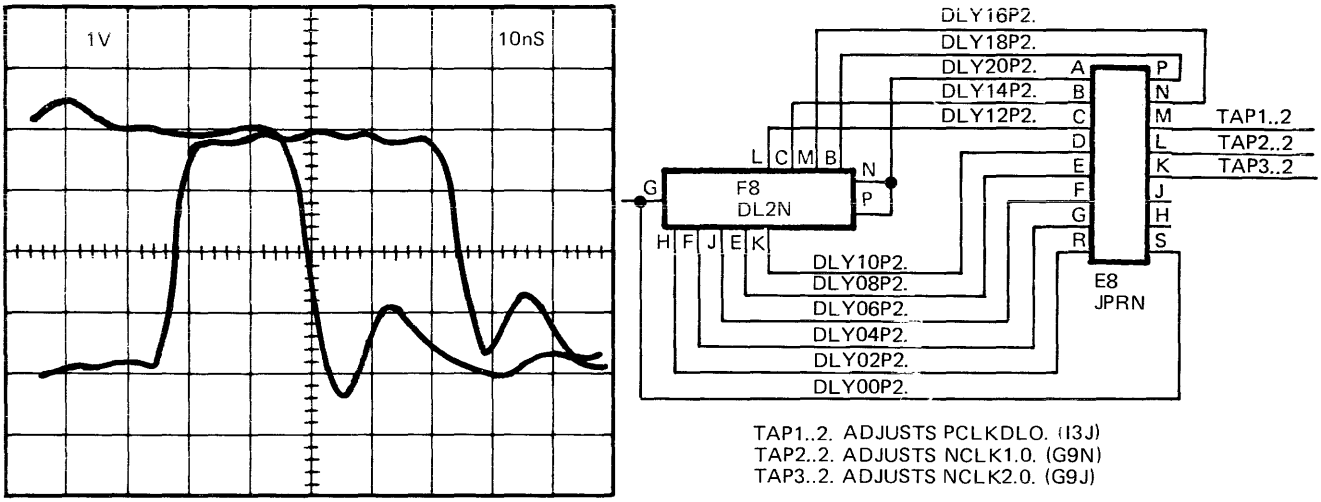


THE TRAILING EDGE OF PCLK. VO SHOULD LEAD THE TRAILING EDGE OF SEE LIST BY 22-25 nSEC.

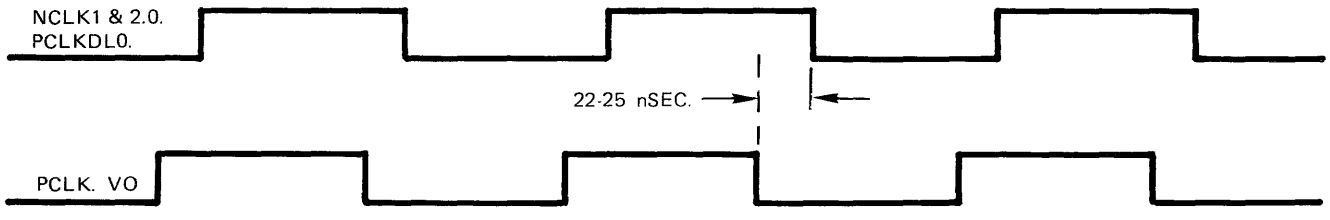
MEASURE AT +1 VOLT LEVEL
VOLTAGES AT NOMINAL

G14778

Figure 5-8. Processor Clock Skew (E3)



A.	TRIGGER	INTERNAL, POSITIVE
B.	CHANNEL ONE	PCLK .VO (OWX)
C.	CHANNEL TWO	PCLKDLO.,NCLK 1&2.0.
D.	HORIZONTAL	1 uSEC/cm. X10 ON (10 nSEC/cm.)
E.	VERTICAL	1 VOLT/cm.
F.	TRIGGER SOURCE	CHANNEL ONE
G.	DISPLAY MODE	ALTERNATE
H.	MACHINE STATE	IDLE
I.	ADJUSTMENT	JUMPER CHIP AT E8 (SEE DIAGRAM)

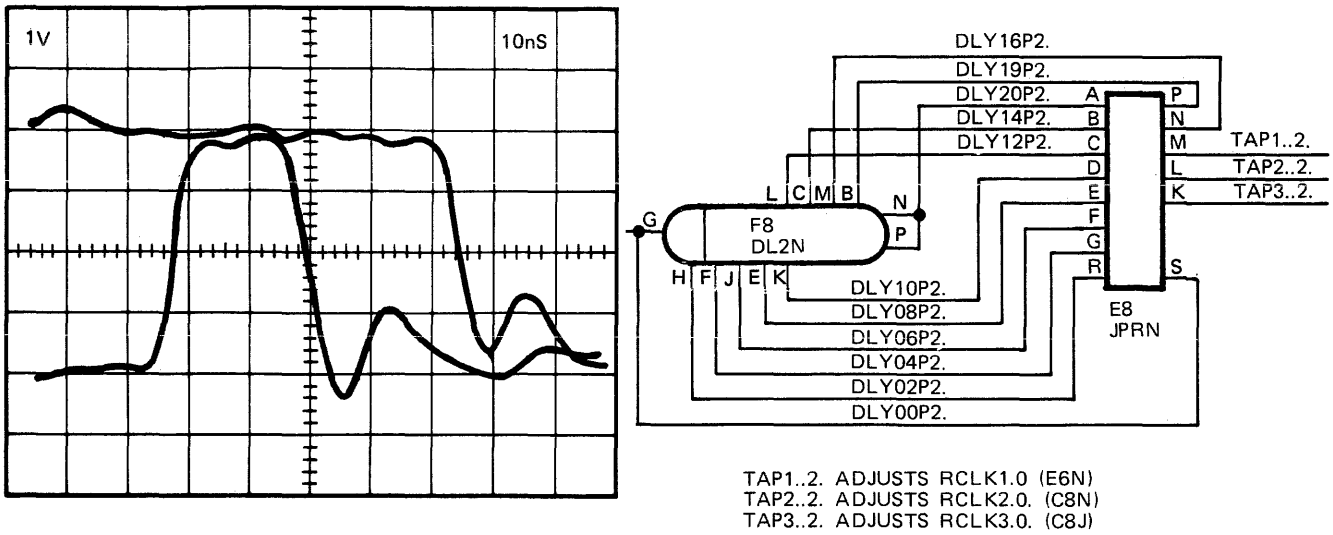


THE TRAILING EDGE OF PCLK.VO SHOULD LEAD THE TRAILING EDGE OF PCLKDLO. & CLK1 & 2.O. BY 22-25 nSEC.

MEASURES AT +1 VOLT LEVEL
VOLTAGES AT NOMINAL

G14779

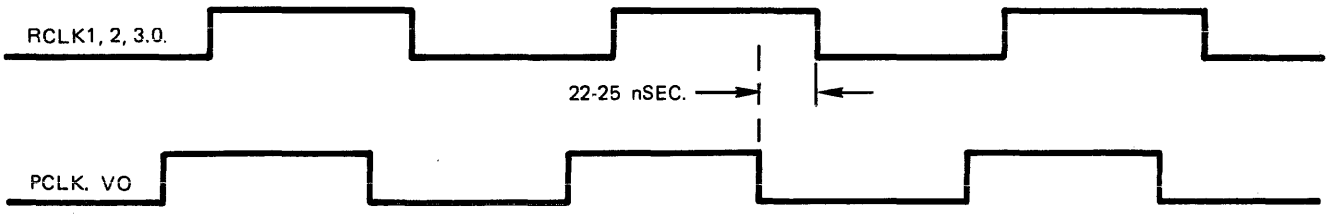
Figure 5-9. Processor Clock Skew (F3)



TAP1..2. ADJUSTS RCLK1.0 (E6N)
TAP2..2. ADJUSTS RCLK2.0. (C8N)
TAP3..2. ADJUSTS RCLK3.0. (C8J)

CLOCK SKEW MUST BE ADJUSTED BETWEEN THE POINT WHERE THE CLOCK ENTERS THE CARD, AND THE POINT WHERE THE CLOCK IS ACTUALLY FED TO A CLOCKED DEVICE.

A.	TRIGGER	INTERNAL, POSITIVE
B.	CHANNEL ONE	PCLK .VO (OWX)
C.	CHANNEL TWO	RCLK1,2&3.0.
D.	HORIZONTAL	1 uSEC/cm. X10 ON (10 nSEC/cm.)
E.	VERTICAL	1 VOLT/cm.
F.	TRIGGER SOURCE	CHANNEL ONE
G.	DISPLAY MODE	ALTERNATE
H.	MACHINE STATE	ADLE
I.	ADJUSTMENT	JUMPER CHIP AT E8 (SEE DIAGRAM)

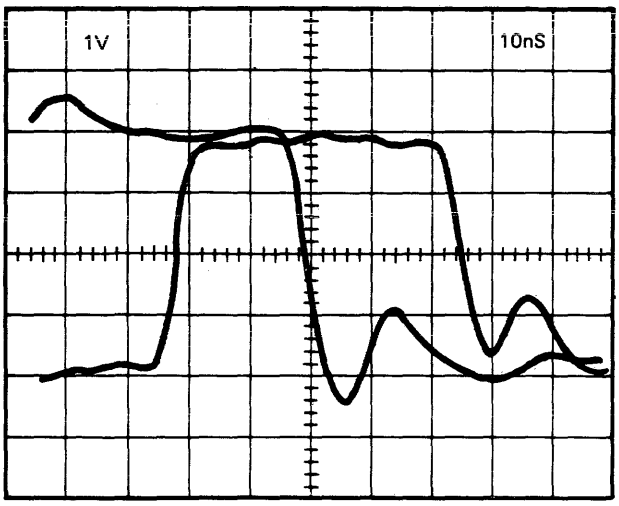


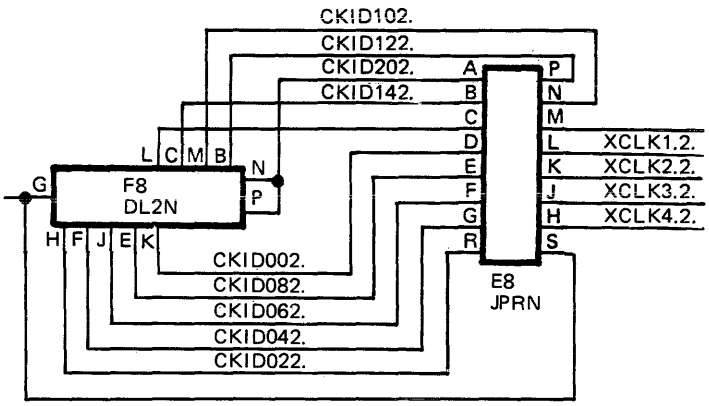
THE TRAILING EDGE OF PCLK.VO SHOULD LEAD THE TRAILING EDGE OF RCLK1, 2, 3.0. BY 22-25 nSEC.

MEASURE AT +1 VOLT LEVEL
VOLTAGES AT NOMINAL

G14780

Figure 5-10. Processor Clock Skew (G3)



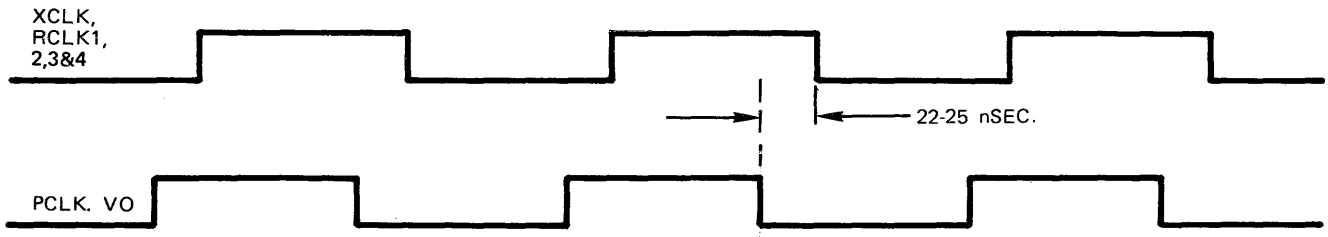


NET LIST

XCLK0.2. ADJUSTS XCLK0.0. (F9N)
XCLK1.2. ADJUSTS RCLK1.0. (D7J)
XCLK2.2. ADJUSTS RCLK2.0. (D7N)
XCLK3.2. ADJUSTS RCLK3.0. (E7N)
XCLK4.2. ADJUSTS RCLK4.0. (E7J)

CLOCK SKEW MUST BE ADJUSTED BETWEEN THE POINT WHERE THE CLOCK ENTERS THE CARD, AND THE POINT WHERE THE CLOCK IS ACTUALLY FED TO A CLOCKED DEVICE.

A.	TRIGGER	INTERNAL. POSITIVE
B.	CHANNEL ONE	PCLK .VO (OWX)
C.	CHANNEL TWO	XCLK, RCLK 1-4 (SEE NET LIST)
D.	HORIZONTAL	1 uSEC/cm. X10 ON (10 nSEC/cm.)
E.	VERTICAL	1 VOLT/cm.
F.	TRIGGER SOURCE	CHANNEL ONE
G.	DISPLAY MODE	ALTERNATE
H.	MACHINE STATE	IDLE
I.	ADJUSTMENT	JUMPER CHIP AT E8 (SEE DIAGRAM)

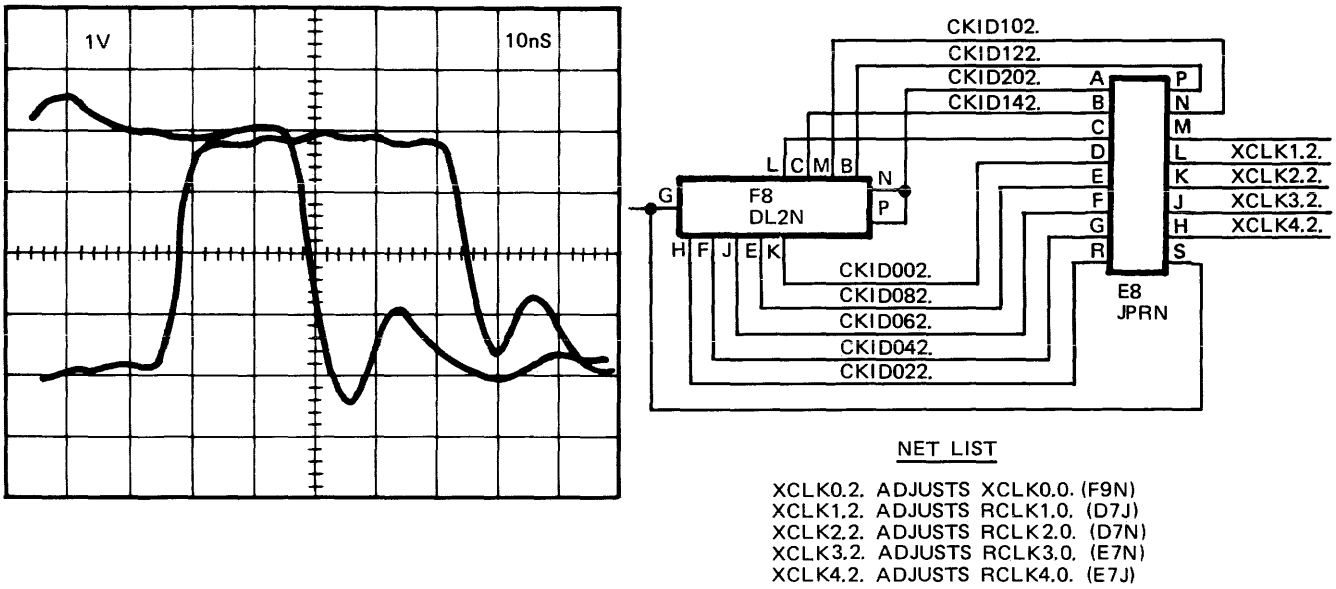


THE TRAILING EDGE OF PCLK. VO SHOULD LEAD THE TRAILING EDGE OF SEE LIST BY 22-25 nSEC.

MEASURE AT +1 VOLT LEVEL
VOLTAGES AT NOMINAL

G14781

Figure 5-11. Processor Clock Skew (H3)

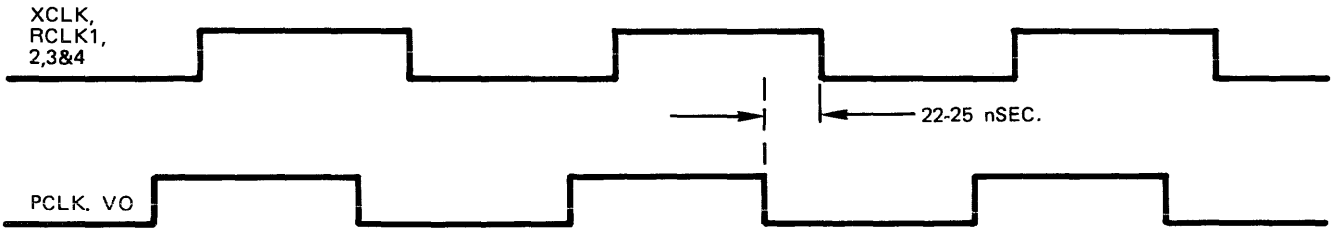


NET LIST

XCLK0.2. ADJUSTS XCLK0.0. (F9N)
XCLK1.2. ADJUSTS RCLK1.0. (D7J)
XCLK2.2. ADJUSTS RCLK2.0. (D7N)
XCLK3.2. ADJUSTS RCLK3.0. (E7N)
XCLK4.2. ADJUSTS RCLK4.0. (E7J)

CLOCK SKEW MUST BE ADJUSTED BETWEEN THE POINT WHERE THE CLOCK ENTERS THE CARD, AND THE POINT WHERE THE CLOCK IS ACTUALLY FED TO A CLOCKED DEVICE.

A.	TRIGGER	INTERNAL, POSITIVE
B.	CHANNEL ONE	PCLK .VO (OWX)
C.	CHANNEL TWO	XCLK, RCLK 1-4 (SEE NET LIST)
D.	HORIZONTAL	1 uSEC/cm. X10 ON (10 nSEC/cm.)
E.	VERTICAL	1 VOLT/cm.
F.	TRIGGER SOURCE	CHANNEL ONE
G.	DISPLAY MODE	ALTERNATE
H.	MACHINE STATE	IDLE
I.	ADJUSTMENT	JUMPER CHIP AT E8 (SEE DIAGRAM)

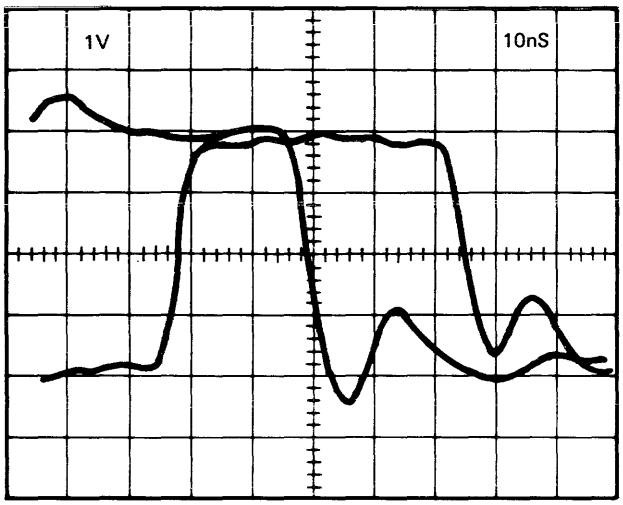


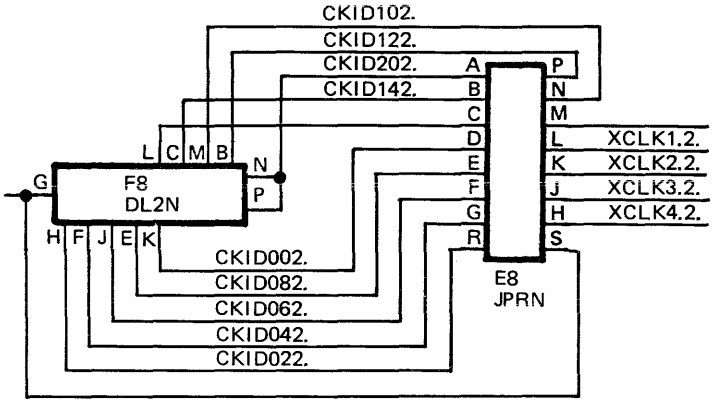
THE TRAILING EDGE OF PCLK. VO SHOULD LEAD THE TRAILING EDGE OF SEE LIST BY 22-25 nSEC.

MEASURE AT +1 VOLT LEVEL
VOLTAGES AT NOMINAL

G14782

Figure 5-12. Processor Clock Skew (K3)



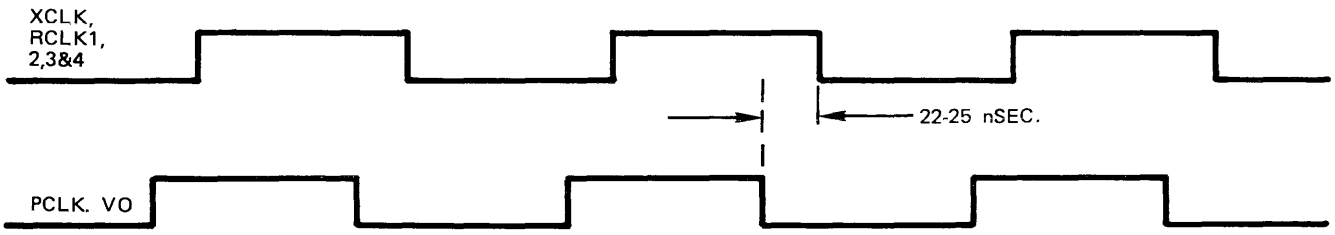


NET LIST

XCLK0.2. ADJUSTS XCLK0.0. (F9N)
XCLK1.2. ADJUSTS RCLK1.0. (D7J)
XCLK2.2. ADJUSTS RCLK2.0. (D7N)
XCLK3.2. ADJUSTS RCLK3.0. (E7N)
XCLK4.2. ADJUSTS RCLK4.0. (E7J)

CLOCK SKEW MUST BE ADJUSTED BETWEEN THE POINT WHERE THE CLOCK ENTERS THE CARD, AND THE POINT WHERE THE CLOCK IS ACTUALLY FED TO A CLOCKED DEVICE.

A.	TRIGGER	INTERNAL, POSITIVE
B.	CHANNEL ONE	PCLK .VO (OWX)
C.	CHANNEL TWO	XCLK, RCLK 1-4 (SEE NET LIST)
D.	HORIZONTAL	1 uSEC/cm. X10 ON (10 nSEC/cm.)
E.	VERTICAL	1 VOLT/cm.
F.	TRIGGER SOURCE	CHANNEL ONE
G.	DISPLAY MODE	ALTERNATE
H.	MACHINE STATE	IDLE
I.	ADJUSTMENT	JUMPER CHIP AT E8 (SEE DIAGRAM)

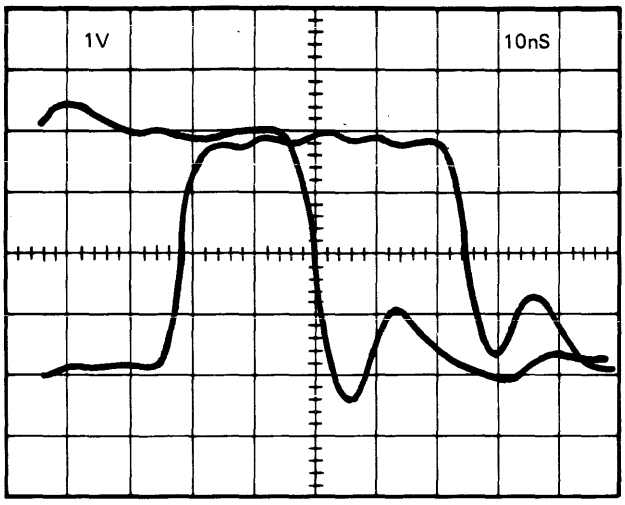


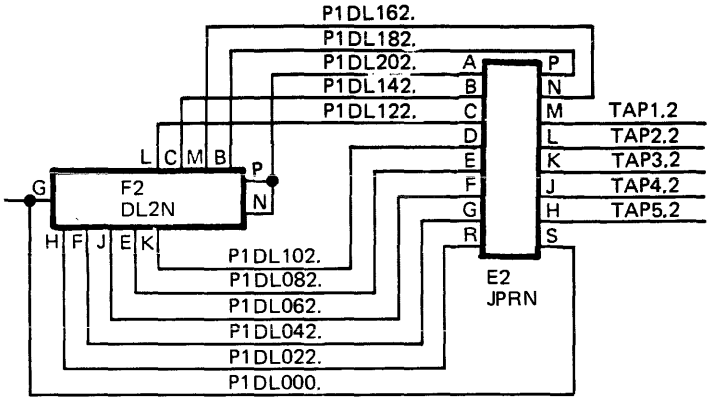
THE TRAILING EDGE OF PCLK. VO SHOULD LEAD THE TRAILING EDGE OF SEE LIST BY 22-25 nSEC.

MEASURE AT +1 VOLT LEVEL
VOLTAGES AT NOMINAL

G14783

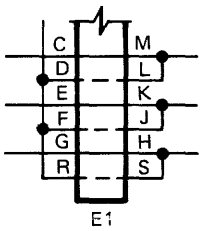
Figure 5-13. Processor Clock Skew (M3)





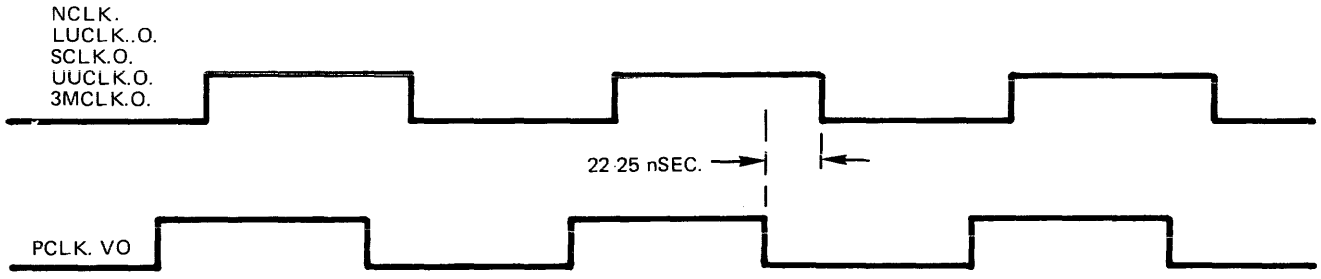
NET LIST

TAP1.2. ADJUSTS NCLK.O. (D0J)
TAP2.2. ADJUSTS LUCLK.O. (D0N)
TAP3.3. ADJUSTS SCLK..O. (D1J)
TAP4.2. ADJUSTS UUCLK.O. (D1N)
TAP5.2. ADJUSTS 3MCLK.O. (G2K)



FOR CALIBRATION, JUMPERS AT E1 SHOULD BE AS SHOWN BY THE DASHED LINES. FOR NORMAL OPERATION, JUMPERS SHOULD BE AS SHOWN BY THE SOLID LINES.

A.	TRIGGER	INTERNAL, POSITIVE
B.	CHANNEL ONE	PCLK VO (0WX)
C.	CHANNEL TWO	SEE NET LIST ABOVE
D.	HORIZONTAL	1 uSEC/cm. X10 ON (10 nSEC/cm.)
E.	VERTICAL	1 VOLT/cm.
F.	TRIGGER SOURCE	CHANNEL ONE
G.	DISPLAY MODE	ALTERNATE
H.	MACHINE STATE	IDLE
I.	ADJUSTMENT	JUMPER CHIP AT E2 (SEE DIAGRAM)

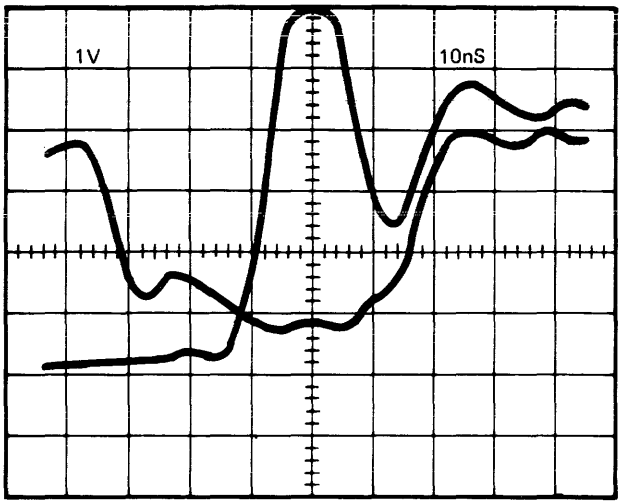


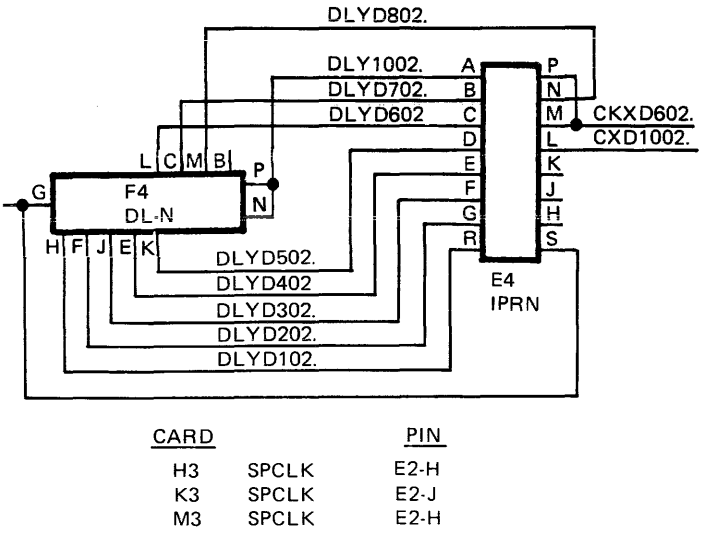
THE TRAILING EDGE OF PCLK. VO SHOULD LEAD THE TRAILING EDGE OF SEE LIST BY 22.25 nSEC.

MEASURE AT +1 VOLT LEVEL
VOLTAGES AT NOMINAL

G14784

Figure 5-14. Processor Clock Skew (N3)

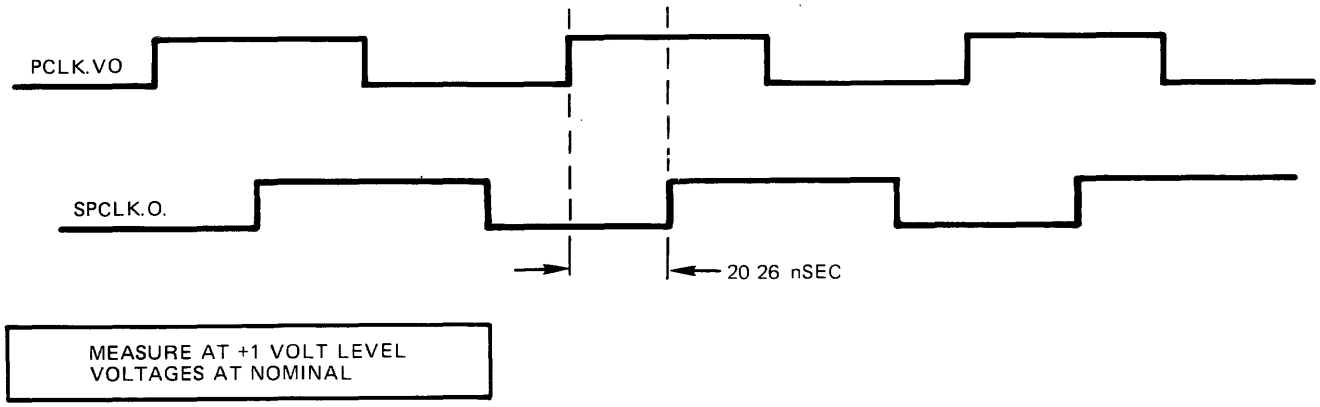




CARD		PIN
H3	SPCLK	E2-H
K3	SPCLK	E2-J
M3	SPCLK	E2-H

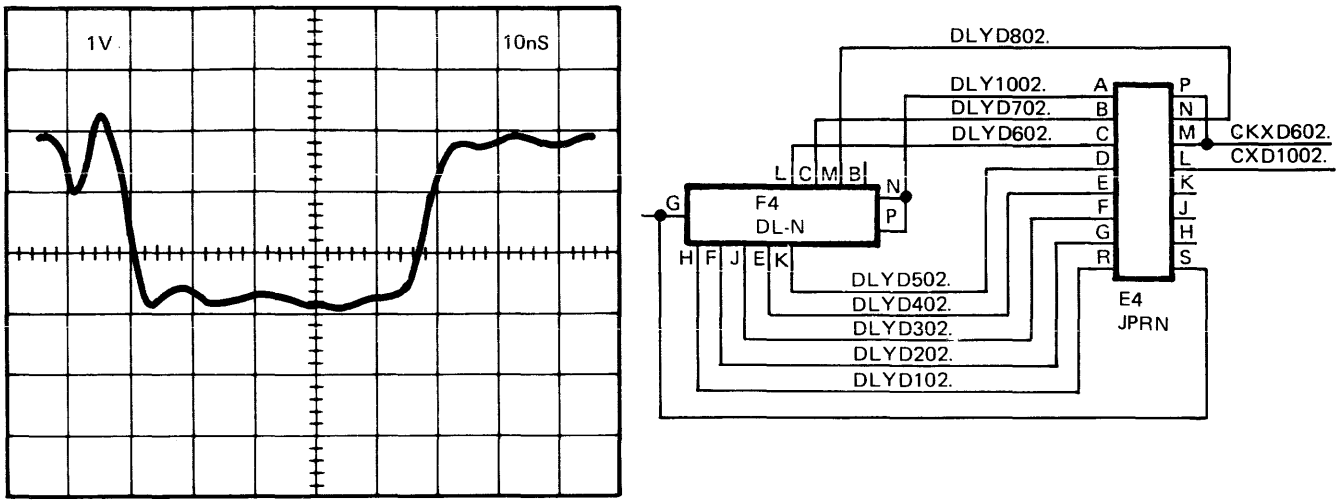
NOTE: THIS PROCEDURE IS THE SAME FOR THE H3, K3, & M3 CARDS.

A.	TRIGGER	INTERNAL, POSITIVE
B.	CHANNEL ONE	PCK1.VO (OWX)
C.	CHANNEL TWO	SPCLK.O. (SEE LIST ABOVE)
D.	HORIZONTAL	1 uSEC/cm. X10 ON (10 nSEC/cm.)
E.	VERTICAL	1 VOLT/cm.
F.	TRIGGER SOURCE	CHANNEL ONE
G.	DISPLAY MODE	ALTERNATE
H.	MACHINE STATE	EXECUTING 2C MICRO
I.	ADJUSTMENT	JPRN E4 PIN L



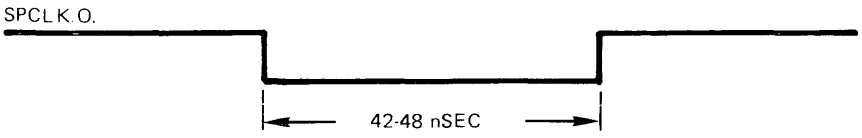
G14785

Figure 5-15. Scratchpad Skew



NOTE: THIS PROCEDURE IS THE SAME FOR THE H3, K3, & M3 CARDS.

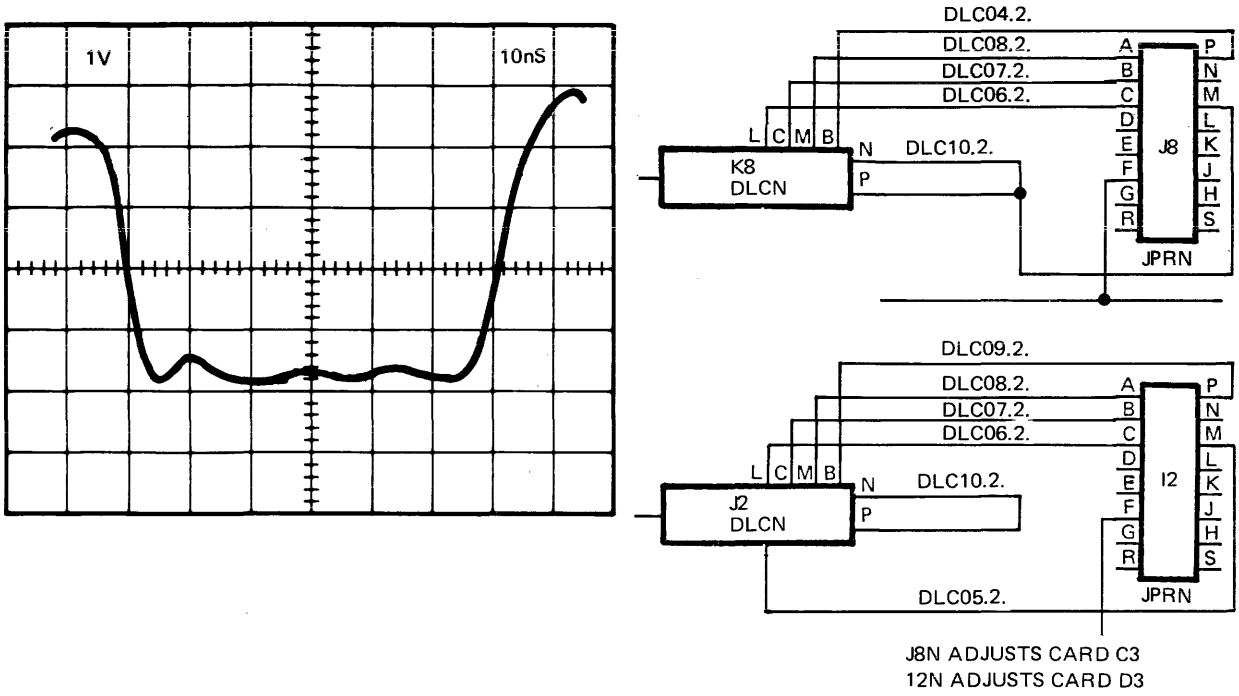
A.	TRIGGER	INTERNAL, POSITIVE
B.	CHANNEL ONE	SPCLK.O.
C.	CHANNEL TWO	NONE
D.	HORIZONTAL	1 uSEC/cm. X10 ON (10 nSEC/cm.)
E.	VERTICAL	1 VOLT/cm.
F.	TRIGGER SOURCE	CHANNEL ONE
G.	DISPLAY MODE	CHANNEL ONE
H.	MACHINE STATE	EXECUTING 2C MICRO
I.	ADJUSTMENT	JPRN E4 PIN M TO CORRECT DELAY



MEASURE AT +1 VOLT LEVEL
VOLTAGES AT NOMINAL

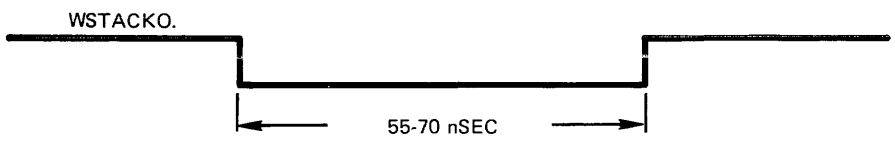
G14786

Figure 5-16. Scratchpad Width



NOTE: THIS PROCEDURE IS THE SAME FOR CARDS C3 AND D3.

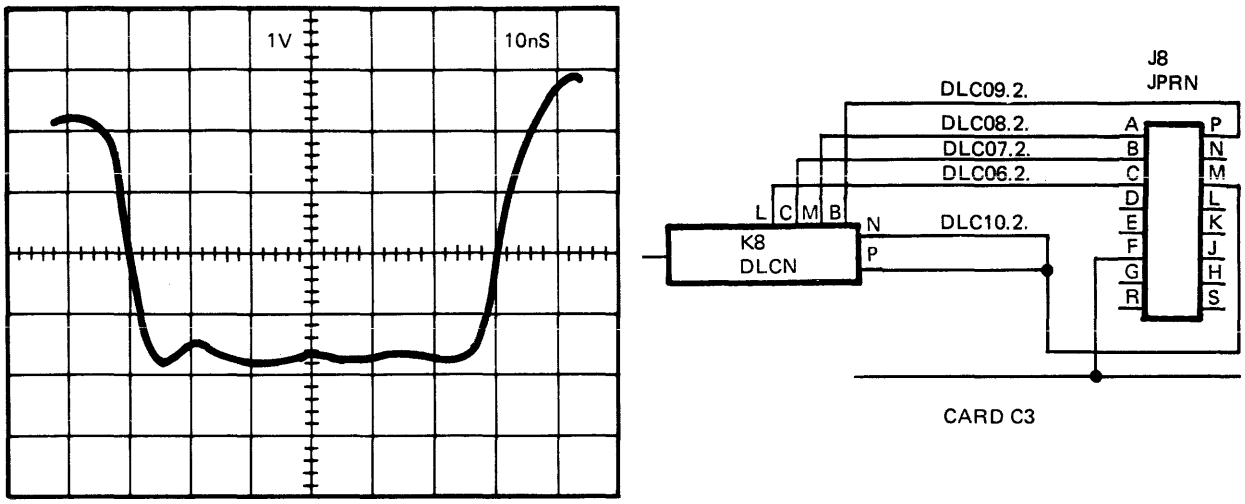
A.	TRIGGER	INTERNAL, POSITIVE
B.	CHANNEL ONE	W STACKO. (A8J) (H2J)
C.	CHANNEL TWO	NONE
D.	HORIZONTAL	1 uSEC/cm. X10 ON (10 nSEC/cm.)
E.	VERTICAL	1 VOLT/cm.
F.	TRIGGER SOURCE	CHANNEL ONE
G.	DISPLAY MODE	ALTERNATE
H.	MACHINE STATE	FROZEN M– EXECUTING A 7E MICRO
I.	ADJUSTMENT	JPRN J8 PIN N



MEASURE AT +1 VOLT LEVEL
VOLTAGES AT NOMINAL

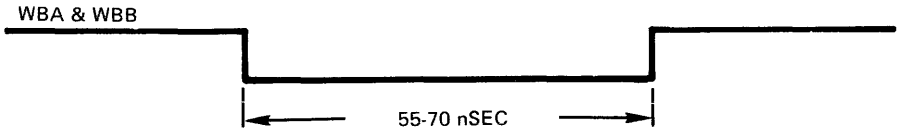
G14787

Figure 5-17. A-Stack



NOTE: THE ADJUSTMENTS FOR WBA & WBB ARE THE SAME AS A-STACK. BE SURE AND CHECK BOTH WRITE BLOCK A & WRITE BLOCK B.

A.	TRIGGER	INTERNAL, POSITIVE
B.	CHANNEL ONE	WBA (1AY), WBB (OBY)
C.	CHANNEL TWO	NONE
D.	HORIZONTAL	1 uSEC/cm. X10 ON (10 nSEC/cm.)
E.	VERTICAL	1 VOLT/cm.
F.	TRIGGER SOURCE	CHANNEL ONE
G.	DISPLAY MODE	ALTERNATE
H.	MACHINE STATE	FROZEN M- EXECUTING A 7E MICRO
I.	ADJUSTMENT	JPRN J8 PIN N



MEASURE AT +1 VOLT LEVEL
VOLTAGES AT NOMINAL

G14788

Figure 5-18. Cache Width

I/O CLOCK TIMING ADJUSTMENTS

The B 1870/B 1860 I/O Base contains several clock circuits which require calibration. The following procedures ensure proper width, delay and frequency of these I/O clocks.

Test Equipment

The following test equipment is required for the I/O Timing Adjustments:

a. Tektronix 465 oscilloscope with 10:1 probes (or equivalent).

b. I/O Debug Test Tape.

SCPCn Calibration Procedure

This procedure ensures that the clocks at the frontplane "doghouse" connectors on the I/O distribution card have the correct delay, as compared with the reference clock on the clock card. Refer to figure 5-19 for the calibration procedure. First ensure that SCPC.O at 1BY is correct, then check each "doghouse" connector to ensure they are the same delay as SCPC.O. If a "doghouse" signal is not correct, there may be a component problem in that circuit.

SCPMn Calibration Procedure

This procedure ensures that the SCPMn clocks at the Distribution card backplane are correct in width and delay before being distributed to the I/O controls. Refer to figure 5-20 for calibration of the SCPM width. Make sure that all SCPM clocks are the same. Refer to figure 5-21 for calibration of the SCPM delay as compared to reference clock. Make sure that all SCPM clocks are the same.

I/O Receive Calibration Procedure

The I/O Receive signal must be delayed before being distributed to the receive buffers on the Distribution card. To ensure that I/O Receive is delayed properly, use the following test procedure.

a. Place a jumper between pins A and P on JPRN D7 on the distribution card.

b. Load the I/O Debug Test tape into the system.

c. Loop the "Test Operation" test to any I/O control in the system (800000 (HEX) loaded in T register).

d. Refer to figure 5-22 for the calibration procedure.

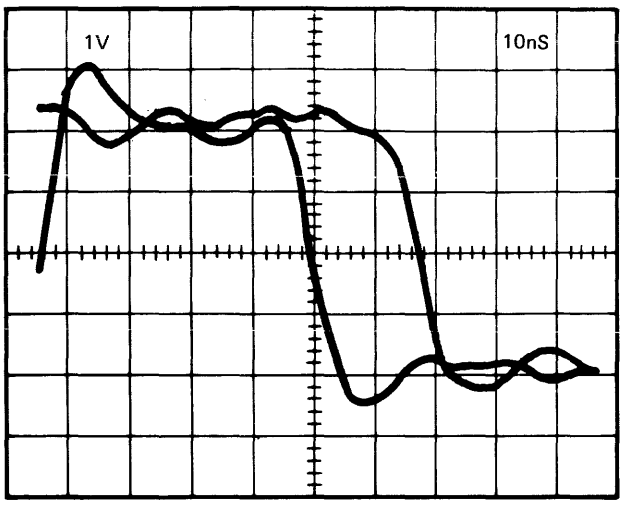
e. Remove test jumper from pins A and P of JPRN D7 when finished.

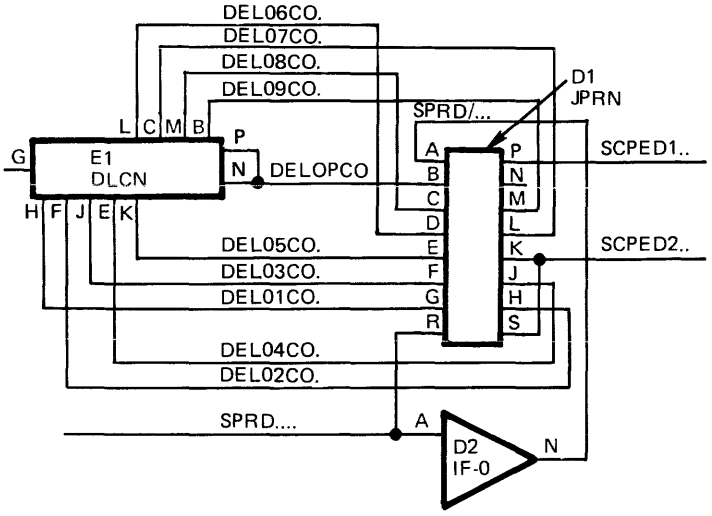
8 MHz Clock

The 8-MHz clock is generated on the distribution card by a crystal controlled oscillator. The distribution card uses the 8-MHz signal in conjunction with the master clock to generate the slow clocks. The 8-MHz clock is also made available to independent backplane controls for their utilization, and is transmitted along the I/O bus by a frontplane connection at #Y. Refer to T & F Documents for the calibration procedure of this clock.

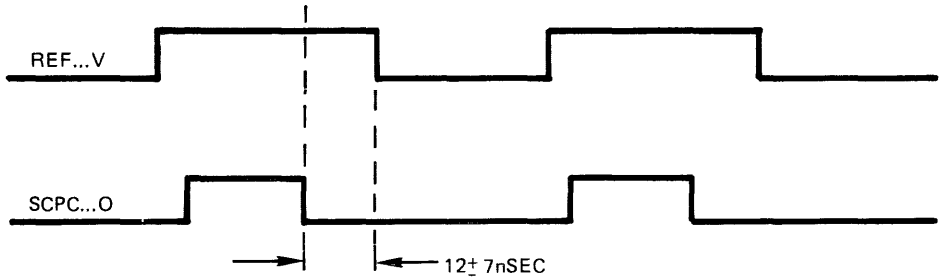
I/O Control Skew

All B 1870/B 1860 I/O controls having independent backplanes and all I/O sub-distribution cards require calibration of DSCP clock skew. DSCP as appearing at OWX of each independent backplane must be within 5 nanoseconds of SCPM...O on the Distribution card (pin OWX). Check each control in the system against SCPM...O at the distribution card, and adjust if needed by use of schematics for the control under test. Refer to figure 5-23 for the calibration procedure and scope settings.





A.	TRIGGER	INTERNAL, POSITIVE
B.	CHANNEL ONE	REF...V (OWX CLOCK CARD)
C.	CHANNEL TWO	SCPC...O (1BY DIST. CARD)
D.	HORIZONTAL	1 uSEC/cm. X10 ON (10 nSEC/cm.)
E.	VERTICAL	1 VOLT/cm.
F.	TRIGGER SOURCE	CHANNEL ONE
G.	DISPLAY MODE	ALTERNATE
H.	MACHINE STATE	IDLE
I.	ADJUSTMENT	ADJUST SCPED1. (DIP)

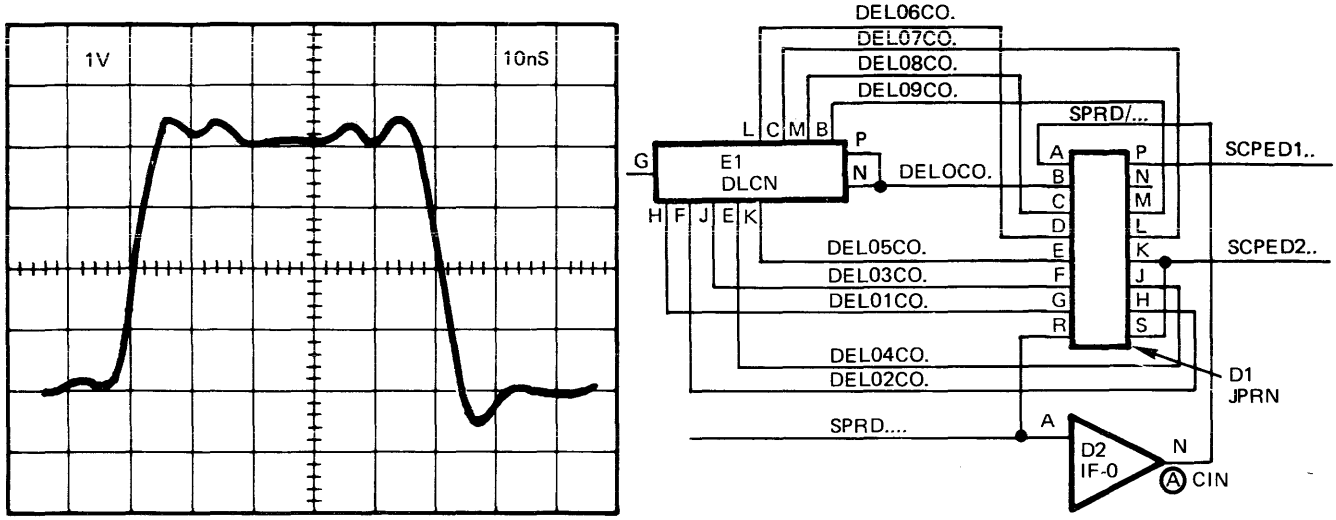


THE TRAILING EDGE OF SCPC...O SHOULD LEAD THE TRAILING EDGE OF REF...V BY 12 ± 7 nSEC.

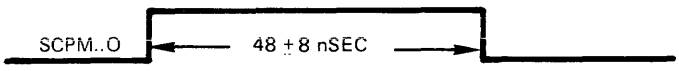
MEASURES AT +1 VOLT LEVEL
VOLTAGES AT NOMINAL

G14789

Figure 5-19. SCPC...O Skew



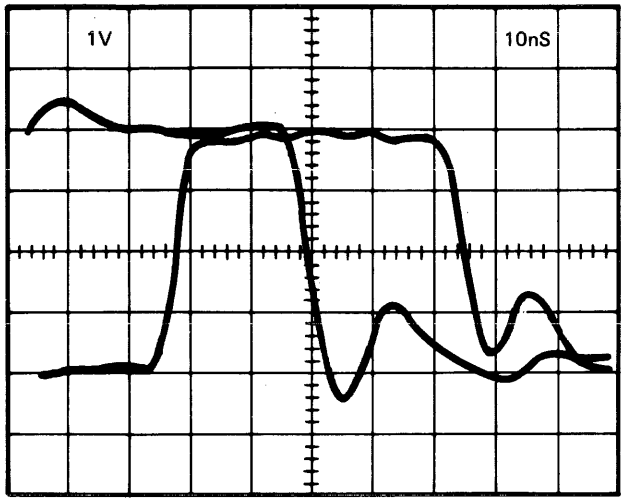
A.	TRIGGER	INTERNAL, POSITIVE
B.	CHANNEL ONE	REF...V (OWX CLOCK CARD)
C.	CHANNEL TWO	SCPM...O (OWX DIST. CARD)
D.	HORIZONTAL	1 uSEC/cm. X10 ON (10 nSEC/cm.)
E.	VERTICAL	1 VOLT/cm.
F.	TRIGGER SOURCE	CHANNEL ONE
G.	DISPLAY MODE	CHANNEL TWO
H.	MACHINE STATE	IDLE
I.	ADJUSTMENT	ADJUST SCPED2. (D1K)

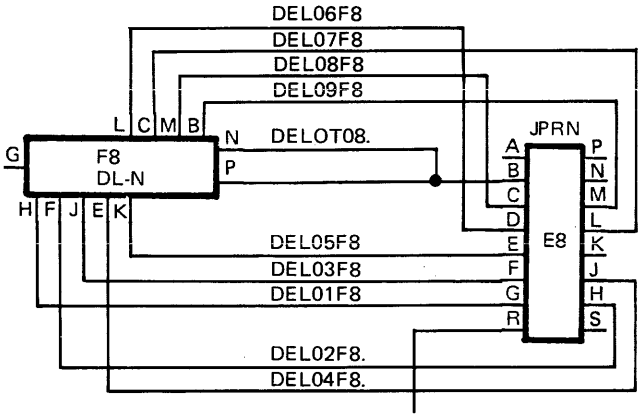


MEASURE AT +1 VOLT LEVEL.
VOLTAGES AT NOMINAL

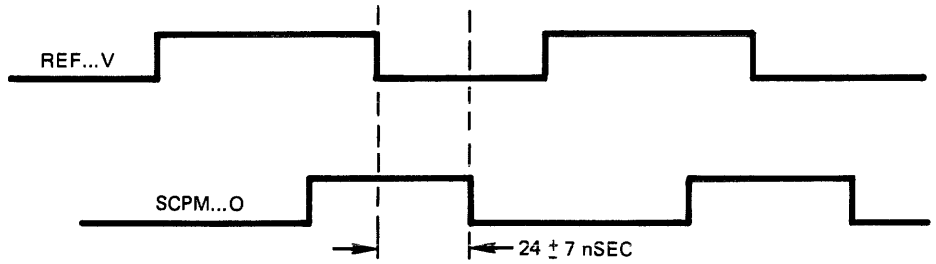
G14790

Figure 5-20. SCPM Width





A.	TRIGGER	INTERNAL, POSITIVE
B.	CHANNEL ONE	REF...V (OWX CLOCK CARD)
C.	CHANNEL TWO	SCMP...O (OWX DIST. CARD)
D.	HORIZONTAL	1 uSEC/cm. X10 ON(10 nSEC/cm.)
E.	VERTICAL	1 VOLT/cm.
F.	TRIGGER SOURCE	CHANNEL ONE
G.	DISPLAY MODE	ALTERNATE
H.	MACHINE STATE	IDLE
I.	ADJUSTMENT	ADJUST SCPD... (E8R)

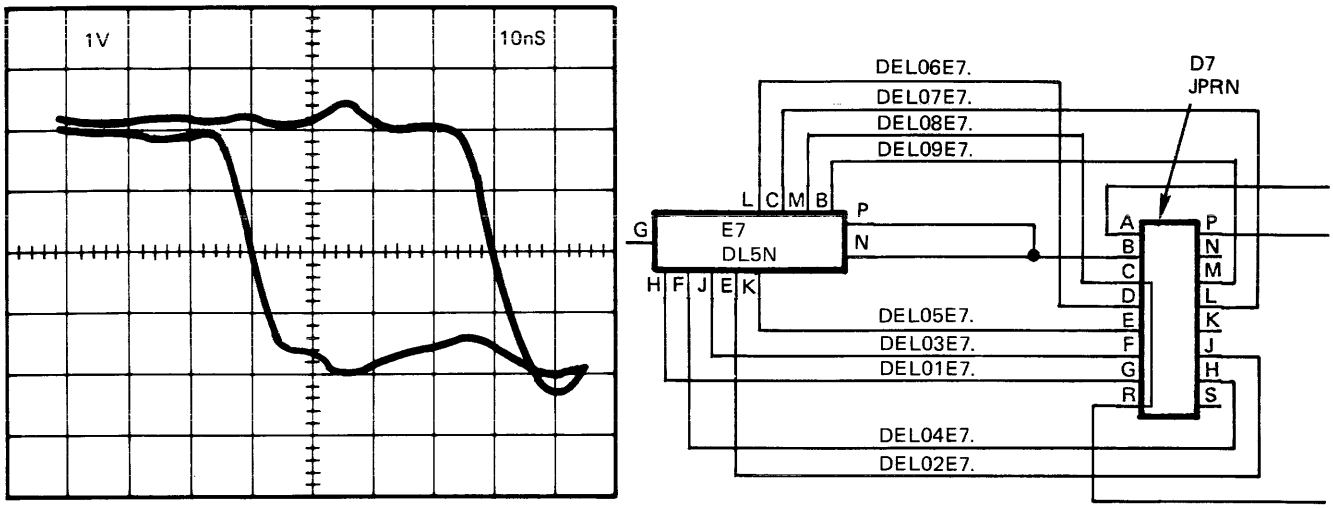


THE TRAILING EDGE OF SCPM...O SHOULD TRAIL REF...V BY 24 ± 7 nSEC.

MEASURE AT +1 VOLT LEVEL
VOLTAGES AT NOMINAL

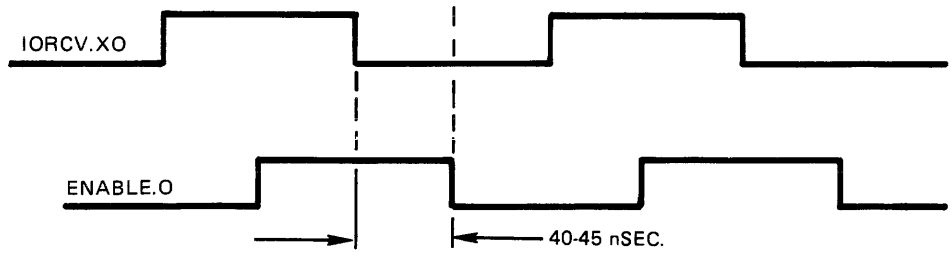
G14791

Figure 5-21. SCPM Skew



NOTE: JUMPER D7 MUST HAVE A JUMPER INSTALLED BETWEEN PINS A & P FOR THIS TEST. BE SURE TO REMOVE THIS JUMPER AFTER COMPLETING THE CALIBRATION.

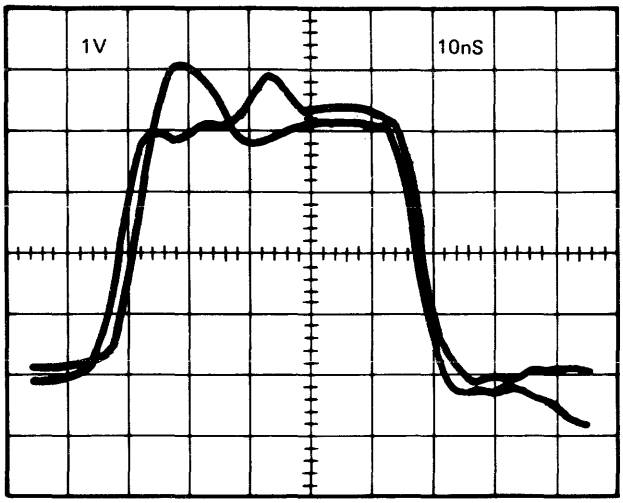
A.	TRIGGER	INTERNAL, POSITIVE
B.	CHANNEL ONE	IORCV.XO (OJY DIST. CARD)
C.	CHANNEL TWO	ENABLE.O (OAY DIST. CARD)
D.	HORIZONTAL	1 uSEC/cm. X10 ON (10 nSEC/cm.)
E.	VERTICAL	1 VOLT/cm.
F.	TRIGGER SOURCE	CHANNEL ONE
G.	DISPLAY MODE	ALTERNATE
H.	MACHINE STATE	TEST OP. WITH I/O DEBUG
I.	ADJUSTMENT	ADJUST IORD... (D7R)



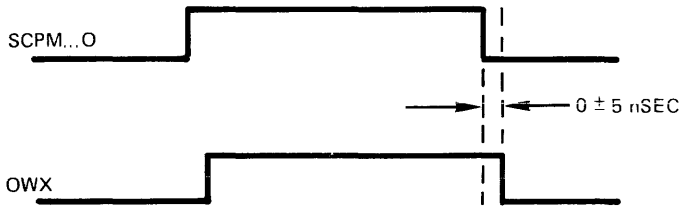
MEASURE AT +1 VOLT LEVEL
VOLTAGES AT NOMINAL

G14792

Figure 5-22. I/O Receive



A.	TRIGGER	INTERNAL, POSITIVE
B.	CHANNEL ONE	SCPM...O (OWX DIST. CARD)
C.	CHANNEL TWO	OWX OF CONTROL UNDER TEST
D.	HORIZONTAL	1 uSEC/cm. X10 ON (10 nSEC/cm.)
E.	VERTICAL	1 VOLT/cm.
F.	TRIGGER SOURCE	CHANNEL ONE
G.	DISPLAY MODE	ALTERNATE
H.	MACHINE STATE	IDLE
I.	ADJUSTMENT	SEE SCHEMATIC FOR CARD UNDER TEST



THE TRAILING EDGE OF CONTROL UNDER TEST LEADS OR LAGS THE TRAILING EDGE OF SCPM...O BY 0-5 nSEC.

MEASURES AT +1 VOLT LEVEL
VOLTAGES AT NOMINAL

G14793

Figure 5-23. I/O Control Skew

Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE	SYSTEM SERIES B1800	No. L8282-001
		STYLE/MODEL B1870/60	PAGE 1 OF 1
ORIGINATOR: Santa Barbara		TOP UNIT NO. 22128953 and 22129142	
STD. INSTALL. TIME 1 Hour	UNITS AFFECTED 22180541	UNIT DESCRIPTION Card U3	
TITLE FIELD CARD TESTER COMPATABILITY (EI 6545)			DATE 8-13-77

INSTALLATION IS MANDATORY

PREREQUISITE: Card U3 must be at O/N 22180541. Installation of this LIN does the following:

1. Changes signatures and node counts.
2. Changes the Order Number to 22181234.

CONDITION: Card test procedure calls for a connection to an element on the logic board that poses a logic short hazard.

CAUSE: No provision on the logic card for a terminal post.

CORRECTION: Add a terminal post to the logic card so that either a logic short or a power short cannot occur when connecting the card tester to a logic element.

PARTS REQUIRED:

Number	Description	Quantity	Unit List Price
22009005	30 Gauge Wire	1 ft.	$ .07/ft.
22054803	W/W Terminal	1	.28

INSTRUCTION MEDIA PACKAGE NO. 1102084
(Includes one set of the following media:)

Installation Procedure	(1 page)
Card History Sheet	(1 page)
Card Test Data	(7 pages)

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Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE	SYSTEM SERIES B1800	NO. L8282-003
		STYLE/MODEL B1870/60	PAGE 1 OF 1
ORIGINATOR: Santa Barbara		TOP UNIT NO. 2212 8649	
STD. INSTALL. TIME N/A	UNITS AFFECTED O/N 2218 0418	UNIT DESCRIPTION Mem Base Unit-3 Backplane	
TITLE Signal Wire Rerouting, to Clear Power Leads (EI6555)			DATE 9/3/77
INSTALLATION IS MANDATORY			

PREREQUISITE: MBU-3 must be at O/N 2218 0418. Installation of this LIN changes the backplane to O/N 2218 1358.

CONDITION: For manufacturing purposes only. No retrofit instructions necessary.

CORRECTION: Relabel backplane with new O/N 2218 1358. File Backplane history sheet, included with this LIN.

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SANTA BARBARA PLANT

BACKPLANE HISTORY SHEET

CHG CONTROL DOC NO.	ORDER NUMBER (O'N)	CIRCUIT LIST	REV	SCHEMATIC	REV	CARD TEST DATA	REV	REMARKS OR RELATED B/P & CARD CHANGES	MFG DASH
ER 6371 A 2-4-77	2218 0418	T-2216 7845	AC	NOT REEQ'D	-	NOT REQ'D	-	RELEASED FOR PRODUCTION	
EI 6555 A 7-15-77	2218 1358	T-2216 7845	AD	↓	↓	↓	↓	REROUTE SIGNAL WIRES	

ISSUE	DATE	HISTORY SHEET REVISIONS
01	7-15-7	EI 6555A

UNIT NO. 2212 8649
CARD ASSY NO. 2216 7837
CARD NAME B/P ASSY, MBU-3 (22 C D)

LATEST ORDER NO. A-2218 1358
DOC ISSUE 01

PAGE 1 OF 1

SBP 1257 5-73

Burroughs FIELD ENGINEERING	RELIABILITY IMPROVEMENT NOTICE	SYSTEM SERIES B1800	NO. R8282-004
		STYLE/MODEL B1870/60	PAGE 1 OF 1
ORIGINATOR: Santa Barbara		TOP UNIT NO. 2212 8953 and 2212 9142	
STD. INSTALL. TIME: Up to 4 Hours	UNITS AFFECTED: Checkpoint Note	UNIT DESCRIPTION: Port Interchange-3 Card U3	
TITLE: Memory Interface Load Reduction (EI 6543)			DATE: 8-27-77

TYPE OF CHANGE
☒ FUNCTIONAL ☐ IMPROVED MAINTAINABILITY ☐ IMPROVED RELIABILITY

CHECKPOINT NOTE: Installation of this RIN can be made to either O/N 2218 0541 or 2218 1234. If it is made to O/N 1218 0541, then the O/N becomes 2218 1218. If it is made to O/N 2218 1234, then the O/N remains 2218 1234. O/N 2218 1218 must have LIN 8282-001 installed to bring the card to O/N 2218 1234.

PREREQUISITE: Card U3 must be either O/N 2218 0541 or O/N 2218 1234. Visual inspection of O/N 2218 1234 must be made to ensure that this RIN need not be installed. Signatures and node counts are not affected by this RIN.

CONDITION: Memory interface signal loading problems that will not allow future memory bases to function properly in the system.

CAUSE: MBU-3 or MBU-4 does not utilize the newer, faster interface gates and buffers needed with future memory bases.

CORRECTION: Install the new load resistors to reduce the load on the interface between the MBU and Card U3.

PARTS REQUIRED:

Part Number	Description	Quantity	Unit List Price
1111 8627	348 Ohms, 1/4 w Resistor	27	$ .88
1111 8676	562 Ohms, 1/4 w Resistor	31	.91
2212 2725	330 Ohms, .3 W SIP	1	3.20

INSTRUCTION MEDIA PACKAGE NO. 1102092
(Includes one set of the following media:)

- Installation Procedure (1 page)
- Card History Sheet (1 page)
- Logic Schematics (8 pages)

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Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE	SYSTEM SERIES B1800	NO. L8282-004
		STYLE/MODEL B1870/60	PAGE 1 OF 3
ORIGINATOR: Santa Barbara		TOP UNIT NO. 2212 8631	
STD. INSTALL. TIME 1/2 Hr.	UNITS AFFECTED O/N 2218 1069	UNIT DESCRIPTION M-PROC-3, Card N3 (HYB)	
TITLE Eliminate Glitch in Net 6CMICRXO (EI 6556)			DATE 8/29/77

INSTALLATION IS MANDATORY

PREREQUISITE: Card N3 must be at O/N 2218 1069. Installation of this LIN changes the card to O/N 2218 1366. Does not change card test data.

CONDITION: The 6CMICRXO nano, entering the N3 card under certain machine state conditions, has a 1 volt negative going glitch 50us after the nano goes true.

CAUSE: Improperly terminated.

CORRECTION: Relocate terminator closest the end of the Net.

PROCEDURE:

1. Delete the 180 ohm 1/2 watt resistor at location 033 and relocate it at location E3W to -2V.
2. Add wires per figure 1.

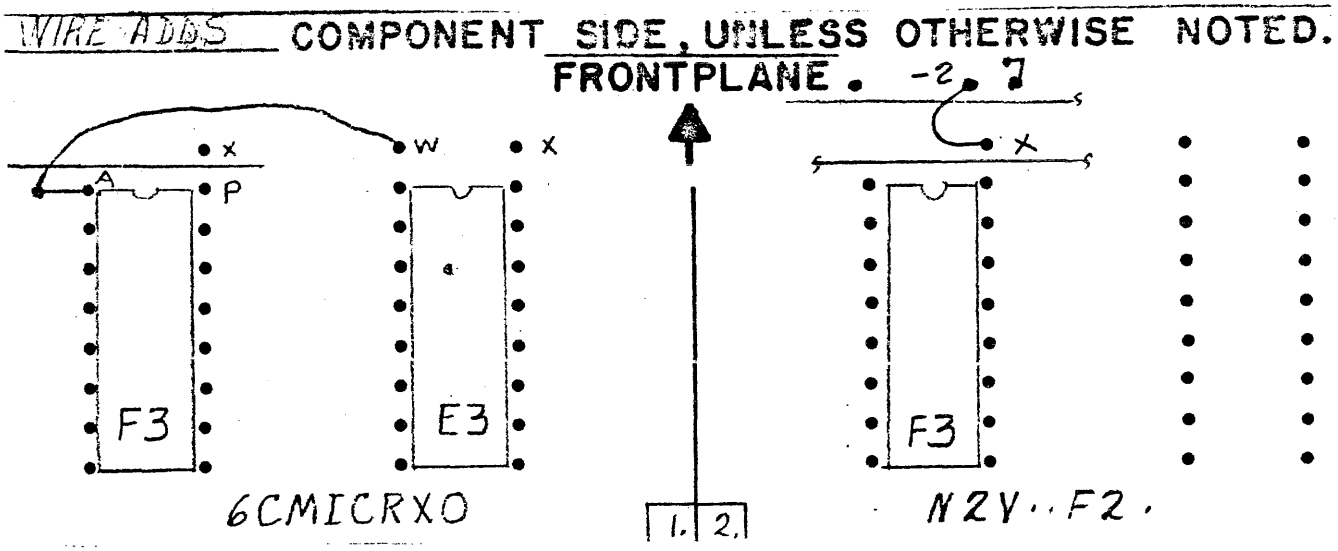

Figure 1

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3. On page 4, Zone A6, of the schematics change as per figure 2.

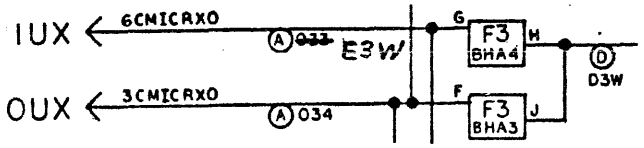
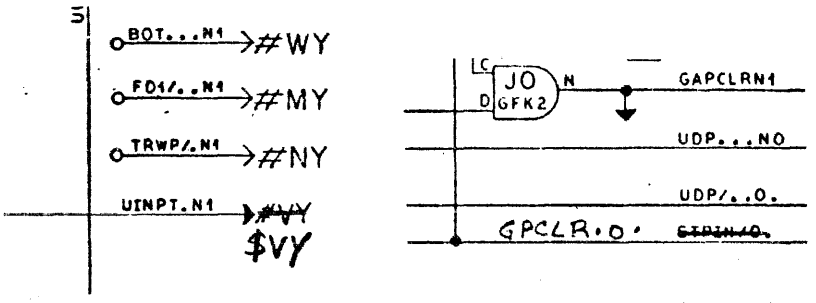


Figure 2

4. Correct schematic errors on page 2, Zone B1 and Zone B5 as per figure 3.



Zone B1 Zone B5

Figure 3

5. Relabel all schematic pages with "EI 6556 O/N 2218 1366".

6. Relabel card with new O/N 2218 1366.

7. File logic card history sheet included with this LIN.

Burroughs Corporation
SANTA BARBARA PLANT

LOGIC CARD HISTORY SHEET

CHG CONTROL DOC NO.	ORDER NUMBER (O N)	CIRCUIT LIST	REV	SCHEMATIC	REV	CARD TEST DATA	REV	REMARKS OR RELATED B/P & CARD CHANGES	MFG DASH
ECN 6613 A	2218 0186	T-2217 2522	AA	D-2217 2399	AC	B-2219 7131	A	INCORP EI'S 6204A, 6220A, & RLSD TIF INDEX & HISTORY SHEET.	
EI 6526 A 4-19-77	2218 1069	↓	↓	D-2217 2399	AC + EI	B-2219 7131	B	REVISE CARD TEST PROCEDURE TO FACILITATE LOGIC TEST.	
ECN 6683 A 5-6-77	↓	↓	↓	D-2217 2399	D	↓	↓	INCORPORATED EI 6526A. RLSD ENHANCED SCHEMATIC	
EI 6556A 7-19-77	2218 1366	↓	↓	D-2217 2399	D+ EI	↓	↓	TO ELIMINATE GLITCH IN NET 6CMICRXO	

LIN NO. L8282-004
Page 3 of 3
Date 8/29/77

ISSUE	DATE	HISTORY SHEET REVISIONS
01	7.19.7	EI 6556A

UNIT NO. 2212 8631
CARD ASSY NO. 2217 2381
CARD NAME CD N3, M/PROC (HYB)

LATEST ORDER NO. A-2218 1366
DOC ISSUE 01

PAGE 1 OF 1

SBP 1257 5-73

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Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE	SYSTEM SERIES B1800	NO. L8282-002
		STYLE/MODEL B1870/60	PAGE 1 OF 1
ORIGINATOR: Santa Barbara		TOP UNIT NO. 2212 8631	
STD. INSTALL. TIME: Up to 2 Hours	UNITS AFFECTED: O/N 22181002	UNIT DESCRIPTION: M-Proc. 3 Card F3 (W/W)	
TITLE: SCRATCHPAD MOVE (2C) FAILURE (EI 6546)			DATE: 8-29-77

INSTALLATION IS MANDATORY

PREREQUISITE: Card F3 must be at O/N 2218 1002. Installation of this LIN changes the card to O/N 2218 1259 and affects signature and node counts.

CONDITION: The MICRO 275F (Move FLCN to S15R) does not function.

CAUSE: The Field Length Conditions (FLCN) are not written into Scratchpad 15R (S15R) when SPDWREF1 is high due to a race condition between HOLDPAX0 and WMPATHX0. This condition results in the Main Exchange not receiving the FLCN data for writing into Scratchpad 15R.

CORRECTION: Install this LIN so that (1) SPDWREF1 will not influence the gating for the Main Exchange, and (2) WMPATHX0 and HOLDPAX0 will be synchronized by MCLKZ1F1 to ensure proper loading of the Scratchpad.

PARTS REQUIRED:

Part Number	Description	Quantity	Unit List Price
2200 9005	30 Gauge Wire	3 ft.	$ .07/ft.
2206 6773	150 Ohms, 1/2W Resistor	1	.21

INSTRUCTION MEDIA PACKAGE NO. 1102118
(Includes one set of the following media:)
- Installation Procedure (1 page)
- Circuit change list (1 page)
- Card history sheet (1 page)
- Logic Schematics (2 pages)
- Card Test Data (7 pages)

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Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE	SYSTEM SERIES B1800	NO. L8282-006
		STYLE/MODEL B1870/60	PAGE 1 OF 1
ORIGINATOR: Santa Barbara		TOP UNIT NO. 2212 8631	
STD. INSTALL. TIME 1 1/2 Hours	UNITS AFFECTED O/N 2218 0137	UNIT DESCRIPTION M-Processor-3 Card H3 (etched)	
TITLE ELIMINATE SCRATCHPAD WRITE CLOCK NOISE (EI 6547A)			DATE 10-15-77

INSTALLATION IS MANDATORY

PREREQUISITE: Card H3 must be at O/N 2218 0137. This LIN upgrades card H3 to O/N 2218 1267 and changes card signatures and nodes.

CONDITION: Undefined data intermittently being written into scratchpad locations.

CAUSE: Through the multiple component output "OR"ing of SPCLK.O. (scratchpad write clock), a current source switching spike occurs when one or more of the source inputs is turned off.

CORRECTION: Re-route and gate the sources for the Scratchpad write clock, re-named SPMWE.O..

NOTE: Although this LIN may be installed independently of all others, LINS 8282-007 and -008 should be incorporated as soon as possible. Since the B1870/60 Scratchpad is contained on 3 logic cards, (H3, K3, M3), a similar change must be performed to cards K3 and M3.

PARTS REQUIRED:

Part Number	Description	Quantity	Unit List Price
22009005	30 gauge wire	4 ft.	$ .06/ft.

INSTRUCTION MEDIA PACKAGE NO. 1102142
(Includes 1 set each of the following media:)

Installation instructions (5 pages)
Schematics (1 page)
Card test data (4 pages)
History sheet (1 page)

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Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE	SYSTEM SERIES B1800	NO. L8282-007
		STYLE/MODEL B1870/60	PAGE 1 OF 1
ORIGINATOR: Santa Barbara		TOP UNIT NO. 2212 8631	
STD. INSTALL. TIME 1 1/2 Hours	UNITS AFFECTED O/N 2218 0152	UNIT DESCRIPTION M-Processor-3 Card K3 (Etched)	
TITLE ELIMINATE SCRATCHPAD WRITE CLOCK NOISE (EI 6547A)			DATE 10-15-77

INSTALLATION IS MANDATORY

PREREQUISITE: Card K3 must be at O/N 2218 0152. This LIN upgrades card K3 to O/N 2218 1275 and changes card signatures and nodes.

CONDITION: Undefined data, intermittently written into scratchpad locations.

CAUSE: Through the multiple component output "OR"ing of SPCLK.O. (scratchpad write clock), a current source switching spike occurs when one or more of the source inputs is turned off.

CORRECTION: Re-route and gate the sources for the Scratchpad write clock, re-named SPMWE.O..

NOTE: Although this LIN may be installed independently of all others, LINS 8282-006 and -008 should be incorporated as soon as possible. Since the B1870/60 Scratchpad is contained on 3 logic cards, (H3, K3, M3) a similar change must be performed to cards H3 and M3.

PARTS REQUIRED:

Part Number	Description	Quantity	Unit List Price
22009005	30 gauge wire	4 ft.	$ .06/ft.

INSTRUCTION MEDIA PACKAGE NO. 1102159
(Includes one set each of the following media:)

Installation instructions (4 pages)
Schematics (3 pages)
Card test data (5 pages)
History Sheet (1 page)

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Burroughs FIELD ENGINEERING	RELIABILITY IMPROVEMENT NOTICE	SYSTEM SERIES B1800	No. R8282-006
		STYLE/MODEL B1870/60	PAGE 1 OF 2
ORIGINATOR: Santa Barbara		TOP UNIT NO. 22201107	
STD. INSTALL. TIME 1/4 Hour	UNITS AFFECTED See Checkpoint Note *	UNIT DESCRIPTION Expansion Cabinet-3	
TITLE CIRCUIT BREAKERS TRIPPING (REE 5718)			DATE 1-9-78

TYPE OF CHANGE

☐ FUNCTIONAL ☐ IMPROVED MAINTAINABILITY ☒ IMPROVED RELIABILITY

*CHECKPOINT NOTE: This RIN affects systems with an Expansion Cabinet-3.

CONDITION: Power supply circuit breaker tripping.

CAUSE: Ground strap from expansion cabinet-3 door shorting to the -2.0 volt bus bar.

CORRECTION: Re-configure the ground strap to prevent the strap from weaving towards the -2.0 volt bus bar.

PROCEDURE:

1. Open the back door skin on the expansion cabinet-3.

2. If the ground strap mounted on the retma rail is in a position other than shown in Figure 1, loosen the screw attaching it to the rail, and re-configure it with the lug pointing down. See Figure 1.

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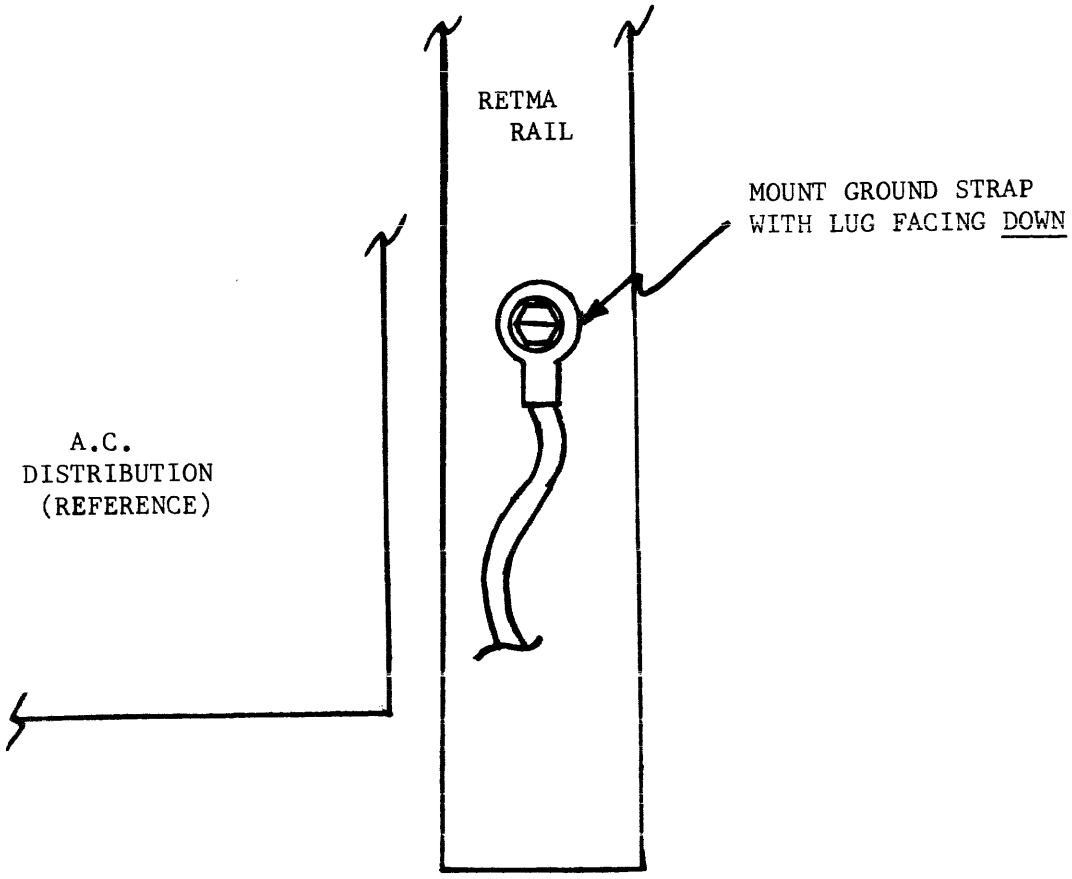

Figure 1

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Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE	SYSTEM SERIES B1800	NO. L8282-010
		STYLE/MODEL B1870/60	PAGE 1 OF 1
ORIGINATOR: Santa Barbara		TOP UNIT NO. 2212 8631	
STD. INSTALL. TIME 2 Hours	UNITS AFFECTED O/N 2218 1259	UNIT DESCRIPTION M-Processor-3 Card F3 (W/W)	
TITLE MODIFICATION OF BIAS MICRO (EI 6563A)			DATE 10-30-77

INSTALLATION IS MANDATORY

PREREQUISITE: Card F3 must be at O/N 2218 1259. Installation of this LIN upgrades card F3 to O/N 2218 1390 and changes card test data.

CONDITION: Improper clearing of the Nano register or improper setting of the HCLK flip/flop.

CAUSE: Critical data path times during execution of the BIAS micro.

CORRECTION: Modify the BIAS micro from one system clock to 2 system clocks to allow sufficient time for all data paths associated with the BIAS micro to clear or set.

PARTS REQUIRED:

Part Number	Description	Quantity	Unit List Price
2217 8925	IC, PRO8	1	N/A
1918 4282	IC, GFKN	1	$ 5.13
1111 8460	75 ohm, 1/4w resistor	1	$ 1.51
2206 6773	150 ohm, 1/2w resistor	1	$ .20
2200 9005	30 gauge wire	4 ft.	$ .07/ft.

INSTRUCTION MEDIA PACKAGE NO. 1102217
(Includes one set each of the following media:)

Installation Instructions (2 pages)
Schematics (3 pages)
Card Test Data (8 pages)
Circuit List (5 pages)
History Sheet (1 page)
JLF2701 Truth Table (1 page)

F.E. Dist Code BB

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Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE	SYSTEM SERIES B1800	NO. L8282-009
		STYLE/MODEL B1870/60	PAGE 1 OF 1
ORIGINATOR: Santa Barbara		TOP UNIT NO. 2212 8631	
STD. INSTALL. TIME 2.5 Hours	UNITS AFFECTED O/N 2218 1168	UNIT DESCRIPTION M-Processor-3 Card F3 (Hybrid)	
TITLE MODIFICATION OF BIAS MICRO (ECN 6993A)			DATE 10-30-77

INSTALLATION IS MANDATORY

PREREQUISITE: Card F3 must be at O/N 2218 1168. This LIN upgrades card F3 to O/N 2218 1432 and changes card test data.

CONDITION: Improper clearing of the Nano Register or improper setting of HCLK.

CAUSE: Critical Data path time during execution of BIAS micro.

CORRECTION: Change the BIAS micro from one system clock to two system clocks in length when using the test variant.

PARTS REQUIRED:

Part Number	Description	Quantity	Unit List Price
2217 8925	IC, PR08	1	N/A
2200 9005	30 gauge wire	3 ft.	$ .07/ft.

INSTRUCTION MEDIA PACKAGE NO. 1102209
(Includes one set each of the following media:)
Installation instructions (4 pages)
Schematics (10 pages)
Card test data (8 pages)
Logic Card History Sheet (1 page)
PROM Truth Table (1 page)

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FOR F.E. TECHNICAL MANUAL FORM 1098282

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Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE	SYSTEM SERIES B1800	NO. L8282-008
		STYLE/MODEL B1870/60	PAGE 1 OF 1
ORIGINATOR: Santa Barbara		TOP UNIT NO. 2212 8631	
STD. INSTALL. TIME 1 1/2 Hour	UNITS AFFECTED O/N 2218 0178	UNIT DESCRIPTION M-Processor-3 Card M-3 (Etched)	
TITLE ELIMINATE SCRATCHPAD WRITE CLOCK NOISE (EI 6547A)			DATE 10-15-77

INSTALLATION IS MANDATORY

PREREQUISITE: Card-M3 must be at O/N 2218 0178. This LIN upgrades card M3 to O/N 2218 1283 and changes card signatures and nodes.

CONDITION: Undefined data intermittently being written to scratchpad locations.

CAUSE: Through the multiple component output "OR"ing of SPCLK.O. (scratchpad write clock), a current source switching spike occurs when one or more of the source inputs is turned off.

CORRECTION: Re-route and gate the sources for the Scratchpad write clock, re-named SPMWE.O..

NOTE: Although this LIN may be installed independently of all others, LINS 8282-006 and -007 should be incorporated as soon as possible. Since the B1870/60 Scratchpad is contained on 3 logic cards, (H3, K3, M3), a similar change must be performed to cards K3 and H3.

PARTS REQUIRED:

Part Number	Description	Quantity	Unit List Price
2200 9005	30 gauge wire	4 ft.	$ .06/ft.

INSTRUCTION MEDIA PACKAGE NO. 1102167
(Includes one set each of the following media:)

Installation instructions (4 pages)
Schematics (2 pages)
Card test data (4 pages)
History sheet (1 page)

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Burroughs FIELD ENGINEERING	RELIABILITY IMPROVEMENT NOTICE	SYSTEM SERIES B1800	NO. R8282-003
		STYLE/MODEL B1870/60	PAGE 1 OF 1
ORIGINATOR: Santa Barbara		TOP UNIT NO. 22128631	
STD. INSTALL. TIME N/A	UNITS AFFECTED All	UNIT DESCRIPTION M-Processor-3 Card G3 (W/W)	
TITLE CARD TEST DATA ENHANCEMENT (EI 6534A)			DATE 7/5/77
TYPE OF CHANGE ☐ FUNCTIONAL	☒ IMPROVED MAINTAINABILITY	☐ IMPROVED RELIABILITY	

CONDITION: Difficulty in fault isolation when trouble-shooting card G3 in the field card tester.

CAUSE: Wire "OR"ing outputs of PROMS causes difficulty in locating the source of a bad signal.

CORRECTION: Replace card test data and the logic card history sheet with that ordered in the Instruction Media Package.

PARTS REQUIRED. None.

INSTRUCTION MEDIA PACKAGE NO. 1102043
(Includes one set of the following media:)
Card Test Data (15 pages)
Logic Card History Sheet (1 page)

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Burroughs FIELD ENGINEERING	RELIABILITY IMPROVEMENT NOTICE	SYSTEM SERIES B1800	NO. R8282-001
		STYLE/MODEL B1870/60	PAGE 1 OF 2
ORIGINATOR: Santa Barbara		TOP UNIT NO. 2212 8631	
STD. INSTALL. TIME N/A	UNITS AFFECTED *See Checkpoint Note	UNIT DESCRIPTION M-Processor-3 Card E3 (W/W)	
TITLE SCHEMATIC CORRECTION (EI 6536-A)			DATE 7/5/77
TYPE OF CHANGE ☐ FUNCTIONAL	☐ IMPROVED MAINTAINABILITY	☐ IMPROVED RELIABILITY	

*CHECKPOINT NOTE: This RIN is a schematic correction only. It does not affect the E3 card's signatures or node counts and does not require an O/N change. The schematics must be labeled with D-2216 5377 REV AA + EI 6523A.

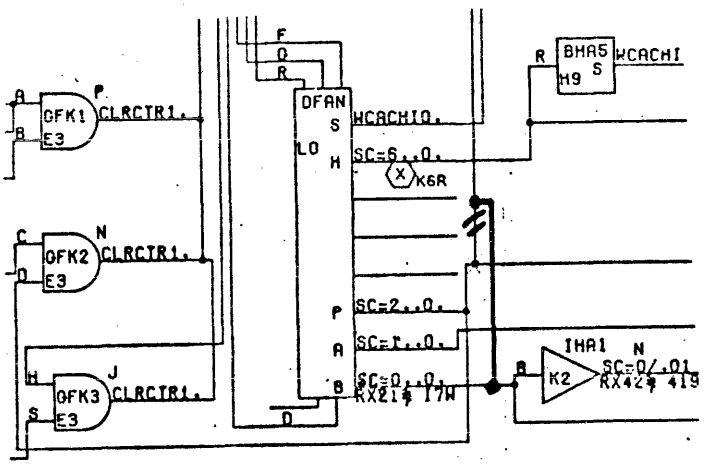
CONDITION: Schematic error.

CAUSE: None

CORRECTION: Revise schematics as per the following procedure.

PROCEDURE:

1. Redline page 10 of the schematics as shown:



COORDINATE: B5, C5
NET: SC=0..0.

2. Label schematics with D-2216 5377 REV AA + EI6536-A.

3. File logic card history sheet, enclosed.

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LOGIC CARD HISTORY SHEET

CHG CONTROL DOC NO.	ORDER NUMBER (O'N)	CIRCUIT LIST	REV	SCHEMATIC	REV	CARD TEST DATA	REV	REMARKS OR RELATED B/P & CARD CHANGES	MFG DASH
ECN 6613 A	2218 0103	T-2216 5427	AD	D-2216 5377	AA	B-2219 6810	A	INCORPORATED EIs 6210A, 6211B & 6214A	RIN NO. R8282-001 Page 2 of 2
EI 6523 A 4-15-77	2218 1036	〃	〃	D-2216 5377	AA + EI	〃	〃	ADDED LOAD RES TO NET NBCTOOO. AND CORRECT SCHEM.	
EI 6536 A 5-25-77	〃	〃	〃	D-2216 5377	AA + EI	〃	〃	TO CORRECT SCHEM ERROR FOR FOR NET: SC=0..0.	

ISSUE	DATE	HISTORY SHEET REVISIONS
01	4/15/7	EI 6523 A
02	5/25/7	EI 6536 A

UNIT NO. 2212 8631
CARD ASSY NO. 2216 5369
CARD NAME CD E3, N/PROC-3 (W/W)

LATEST ORDER NO. A-2218 1036
DOC ISSUE 02

PAGE 1 OF 1

SBP 1257 5-73

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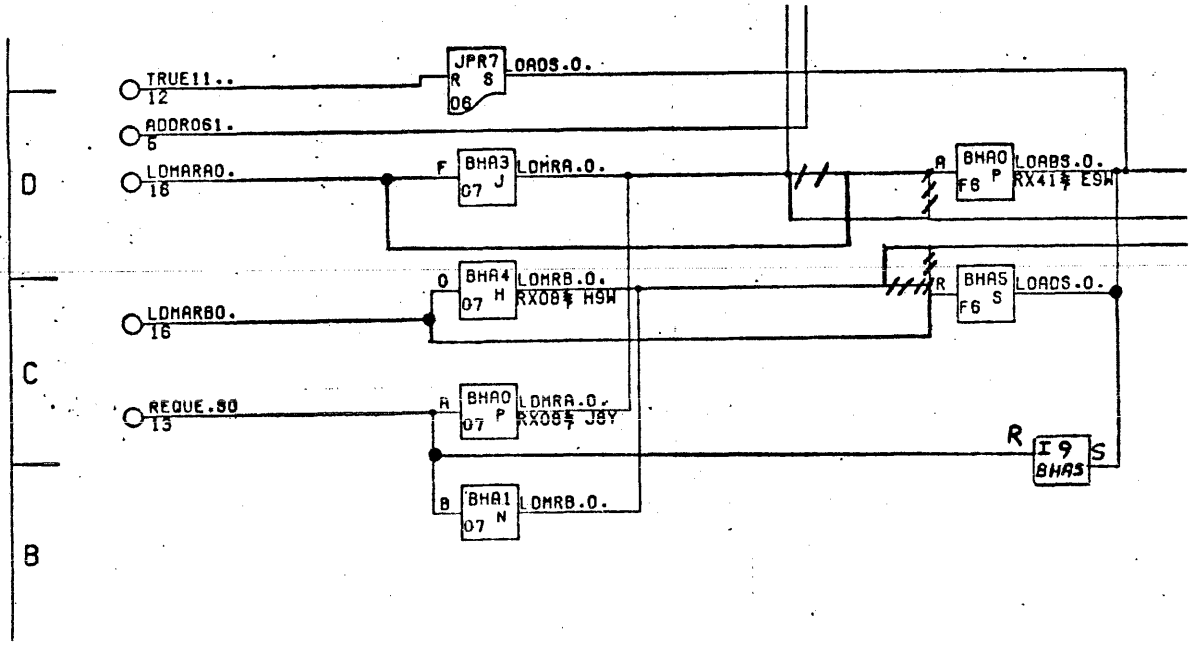
Burroughs FIELD ENGINEERING	RELIABILITY IMPROVEMENT NOTICE	SYSTEM SERIES B1870/B1860	NO. R8282-002
		STYLE/MODEL B1060/B1070	PAGE 1 OF 2
ORIGINATOR: Santa Barbara		TOP UNIT NO. 2212 8649 and 2212 9134	
STD. INSTALL. TIME 1/2 Hr.	UNITS AFFECTED O/N 2218 0897	UNIT DESCRIPTION Memory Base Units -3 and -4	
TITLE SCHEMATIC CORRECTIONS FOR CARD S3 (EI6537)			DATE 7/5/77
TYPE OF CHANGE ☐ FUNCTIONAL	☒ IMPROVED MAINTAINABILITY	☐ IMPROVED RELIABILITY	

PREREQUISITE: Revision AD of logic schematics.

CONDITION: Schematic errors on page 7 at zones D3 - D7, B3 - B7 and J5 of Rev AD logic schematics.

CORRECTION: 1. Make schematic changes to page 7 of AD logic schematics as noted below:



2. Connect H8B at zone J5 to Net TRUE6...

3. Replace Logic Card History Sheet with the one provided with this RIN.

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LOGIC CARD HISTORY SHEET

CHG CONTROL DOC NO.	ORDER NUMBER (O'N)	CIRCUIT LIST	REV	SCHEMATIC	REV	CARD TEST DATA	REV	REMARKS OR RELATED B/P & CARD CHANGES	MFG DASH
ECN 6371 A 2-4-77	2218 0251	NOT REQ'D	-	D-2216 6805	AD	B-2219 6919	A	INCORP. EI'S 6192A, 6217A & RLSD T/F INDEX & HISTORY SHEET	RIN NO. R8282-002 Page 2 of 2
EI 6491 A B 3-21-77	2218 0897	↓		D-2216 6805	AD +EI	↓	↓	CORRECT DELAY TIME ON CLK NET IDLE..0.	
EI 6508 A 3-23-77	↓	↓		↓	↓	B-2219 6919	B	UPDATE UNTESTED CIRCUIT LIST TO MATCH SCHEMATIC	
EI 6537 A 5-26-77	↓	↓		D-2216 6805	AD +EI	↓	↓	CORRECT SCHEM ERROR NET: TRUE6... & LFAN H8	

ISSUE	DATE	HISTORY SHEET REVISIONS
01	3 9 7	EI 6491 A
02	3 21 7	EI 6491 B RES P/N CORRECTION
03	3 23 7	EI 6508 A
04	5 27 7	EI 6537 A

UNIT NO. 2212 8649 /2212 9134
CARD ASSY NO. 2216 6797
CARD NAME CD S3, MBU (ETCH)

LATEST ORDER NO. A-2218 0897
DOC ISSUE 04

PAGE 1 OF 1

SBP 1257 5-75

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Burroughs FIELD ENGINEERING	RELIABILITY IMPROVEMENT NOTICE	SYSTEM SERIES B 1800	NO. R8282-005
		STYLE/MODEL B 1870/60	PAGE 1 OF 1
ORIGINATOR: Santa Barbara		TOP UNIT NO. 2212 8631	
STD. INSTALL. TIME Up to 4 Hours	UNITS AFFECTED 2218 0962	UNIT DESCRIPTION M-Proc-3, Card A3	
TITLE Memory Interface Load Reduction (EI 6542)			DATE 8-27-77

TYPE OF CHANGE
☒ FUNCTIONAL ☐ IMPROVED MAINTAINABILITY ☐ IMPROVED RELIABILITY

PREREQUISITE: Card A3 must be at O/N 2218 0962. Installation of this RIN does not change either signatures or node counts; but the O/N changes to 2218 1200.

CONDITION: Memory interface signal loading problems that will not allow future memory bases to function properly in the system.

CAUSE: MBU-3 or MBU-4 do not utilize the newer, faster interface gates and buffers needed with future memory bases.

CORRECTION: Install the new load resistors to reduce the load on the interface between the MBU and Card A3.

PARTS REQUIRED:

Number	Description	Quantity	Unit List Price
1111 8627	348 Ohms, 1/4w Resistor	27	$ .88
1111 8676	562 Ohms, 1/4w Resistor	31	.91

INSTRUCTION MEDIA PACKAGE NO. 1102100
(Includes one set of the following Media:)

Installation Procedure (1 page)
Card History Sheet (1 page)
Logic Schematics (7 pages)

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