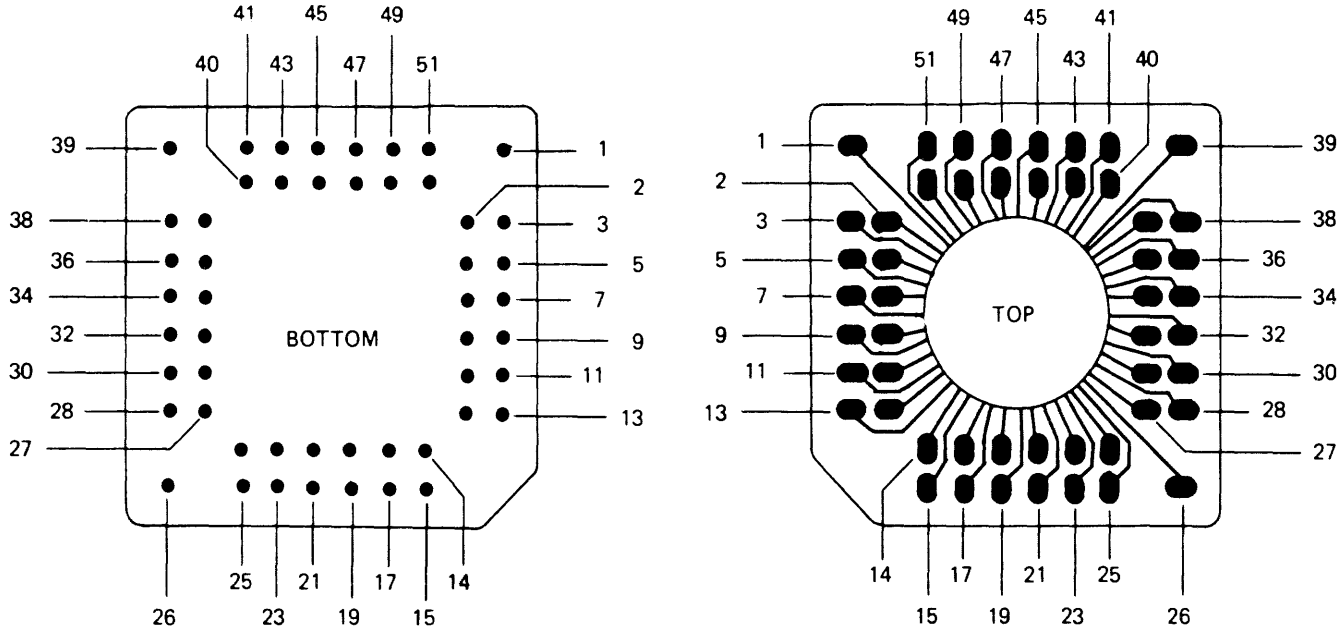
Fig. IIC-116 illustrates the pin identification layout of an LSIC. Pins 13 and 15 are located closest to the double-edged side of the LSIC. All input/output signals are accessible for probing on the top surface of the chip.



TPU LSIC Inputs and Outputs

All TPU LSIC inputs and outputs (FigureIIC-116) are Negative MOS Logic Levels. A logic "1" = 0V and a logic "0" = +5V.

Pin No.	Signal Name	Function	Pin No.	Signal Name	Function
1	VSS	+5 VOLTS	27	TPUD6/-M	IN/OUT
2	CTL	OUTPUT	28	TPUD5/-M	IN/OUT
3	DIR	OUTPUT	29	TPUD4/-M	IN/OUT
4	PAD 0/	OUTPUT	30	TPUD3/-M	IN/OUT
5	PAD 1/	OUTPUT	31	TPUD2/-M	IN/OUT
6	PAD 2/	NOT USED	32	TPUD1/-M	IN/OUT
7	XAD 0/	OUTPUT	33	ROM 9/	INPUT
8	XAD 1/	OUTPUT	34	ROM 8/	INPUT
9	XAD 2/	OUTPUT	35	ROM A/	INPUT
10	XAD 3/	OUTPUT	36	ROM B/	INPUT
11	RQST	INPUT	37	ROM 7/	INPUT
12	IOX/	OUTPUT	38	ROM 6/	INPUT
13	ADD7/	OUTPUT	39	VD	-3 VOLTS
14	ADD6/	OUTPUT	40	ROM 5/	INPUT
15	ADD5/	OUTPUT	41	ROM 4/	INPUT
16	ADD4/	OUTPUT	42	Ø2	CLOCK INPUT
17	ADD3/	OUTPUT	43	Ø1	CLOCK INPUT
18	ADD2/	OUTPUT	44	INIT/	INPUT
19	ADD1/	OUTPUT	45	ROM 3/	INPUT
20	ADD0/	OUTPUT	46	ROM 0/	INPUT
21	FETCH	OUTPUT	47	ROM 1/	INPUT
22	T4	NOT USED	48	ROM 2/	INPUT
23	TFLAG	NOT USED	49	INTRPT/	NOT USED
24	TPUD8/-M	IN/OUT	50	R/W	NOT USED
25	TPUD7/-M	IN/OUT	51	RM	NOT USED
26	VDD	-12 VOLTS			

FIG. IIC-116 TPU LSIC INPUTS & OUTPUTS

L9000 TPU MICRO-PROCESSOR

The PCF functions of the L9000 are controlled by a TPU Micro-processor consisting of a single TPU LSIC in conjunction with 1K X 12 of ROM program memory and other associated logic found on the PCF Control, 60 CPS P.C. card. The TPU Micro-processor receives PCF control and data characters from the basic processor via the Front End output FIFO, processes this data, and sends instructions to the PCF ports for execution. A brief description of all the elements of the L9000 TPU Micro-processor follows; reference should be made to the block diagram shown in Fig. IIC-117.

TPU LSIC

The TPU LSIC is a complete micro processor contained within a standard 51 pin LSIC package. The TPU LSIC is shown in block diagram form in Fig. IIC-118 and consists of an instruction register, a number of seperate storage registers (A, B, X, Y and Q), an arithmetic logic unit (ALU), a decoder and state machine along with other internal logic which together form a complete processor. The TPU LSIC contains no internal micro instruction set. All micro instructions required for the TPU LSIC to cycle and control PCF functions in the L9000 are contained in two externally connected micro program ROM chips.

MICRO PROGRAM ROMS

There are two (512 X 12) ROM chips which contain 1024 12 bit wide micro instructions required to cycle the TPU LSIC micro processor. The implementation of these micro instructions in the TPU LSIC allows the TPU micro processor to act upon the PCF control codes. The PCF control codes, both control characters and data characters, are sent to the TPU micro processor from the console through the Front End output FIFO. The TPU LSIC micro processor, acting upin the PCF control codes, directs the operation of the PCF mechanics and electronics and reports back the execution of the PCF control codes to the console via the TPU microprocessor Flags port.

The inputs and outputs of both ROM chips are wired in parallel, however, only one ROM chip will output a 12 bit wide micro instruction at a time. This is accomplished by the PAD1/ signal into both ROMS. One ROM will be enabled when PAD1/ goes high while the other ROM will be enabled when PAD1/ goes low.

TPU MICRO PROCESSOR PORTS

The TPU Micro-processor controls four ports which cause PCF functions to occur as directed by the TPU Micro-processor. These ports are the carrier port, flags port, forms port and the printer port. Each of these ports performs a specific PCF function when addressed by the TPU Micro-processor. The TPU Micro-processor generates 4 address lines (XAD0 - XAD3) which are decoded into a specific port address (PORT0-PORT15) , which in conjunction with the TPU WRITE-1 command, cause TPU data (TPUD1/-M - TPUD8/-M) to load the specific PCF function into the addressed port for execution. The TPU data lines (TPUD1/-M - TPUD8/-M) are sent to the addressed port through the four Half-Duplex Xmitter/Receiver chips when the WRITE-1 control line is high. The condition of the TPUD1/-M - TPUD8/-M are inverted in the

Half-Duplex Xmitter/Receiver chip and are routed to the ports as the TPUD1 - TPUD8 signals. All four ports receive the TPUD1 - TPUD8 signals, but only the addressed port will load and execute the TPU command.

The addressed port will now execute the TPU command. The TPU Micro-processor waits until the present TPU command is executed. The completion of the command by the addressed port is signaled to the TPU Micro-processor via it's RQST line. RQST is a multiplexed signal consisting of selected feedback signals from the four ports used to signal the performance or completion of a PCF command to the TPU Micro-processor. The RQST line may also be brought high prior to the performance of a PCF function to insure correct timing prior to performing the function. To illustrate, the TPU Micro-processor will look at the O/CKY state at prot 0 time prior to loading data into the printer port at prot 4 time to insure that the carriage is closed before printing occurs. If the carriage is open and printing is to take place, the TPU Micro-processor will first ensure that it is closed before printing can take plae. Likewise certain forms functions must be done in time with the forms timing unit and RQST would signal the TPU Micro-processor prior to loading the forms port at Port 1 time.

TPU MICRO-PROCESSOR FUNCTIONAL DETAIL

The TPU Micro-processor, under ROM program firmware control, causes the 8 bit (byte) PCF control code to be read into the TPU LSIC via the Front End Output FIFO. The TPU Micro-processor decodes the PCF code and writes the proper instructions into the four PCF ports via the TPU address lines for execution of the PCF function.

The reading of data into the TPU and the subsequent writing of instructions and print codes to the ports is controlled by three internally generated signals from the TPU. These signals are CTL (Control), IOX/ (Input Output Exchange) and DIR (Direction). These three signals are decoded on the PCF Control 60 cps P.C. card by a series of gates to generate the signals WRITE, WRITE/, WRITE-1 and ODC/ (Output Dump Command).

The condition of these signals determines the mode of operation of the TPU Micro-processor and are summerized below.

FUNCTION	CTL	IOX/	DIR	WRITE	WRITE/	WRITE-1	ODC/
READ	L	L	L	L	H	L	L
WRITE	L	L	H	H	L	H	H

READ - With the READ function enabled ODC/ causes the next byte from the Front End Output FIFO to appear on the OBD1L - OBD8L lines as inputs to the Half-Duplex Xmitter/Receiver chips. WRITE/ and WRITE-1 are the controling inputs to the Half-Duplex Xmitter/Receiver and cause the OBD1L - OBD8L lines to be read into the TPU LSIC via the TPUDX/-M lines out of the Half-Duplex Xmitter/Receiver.

WRITE - With WRITE-1 and WRITE/ controlling the Half-Duplex Xmitter/Receiver TPU Data on the TPUDX/-M lines will be transferred through the Half-Duplex Xmitter/Receiver to the TPUDX lines. TPUDX along with WRITE will cause this TPU data to be written to the port addressed by the TPU.

The TPU Micro-processor continues to cycle, reading the micro program ROM's and writing TPU data to the ports at selected addresses until the PCF function is complete.

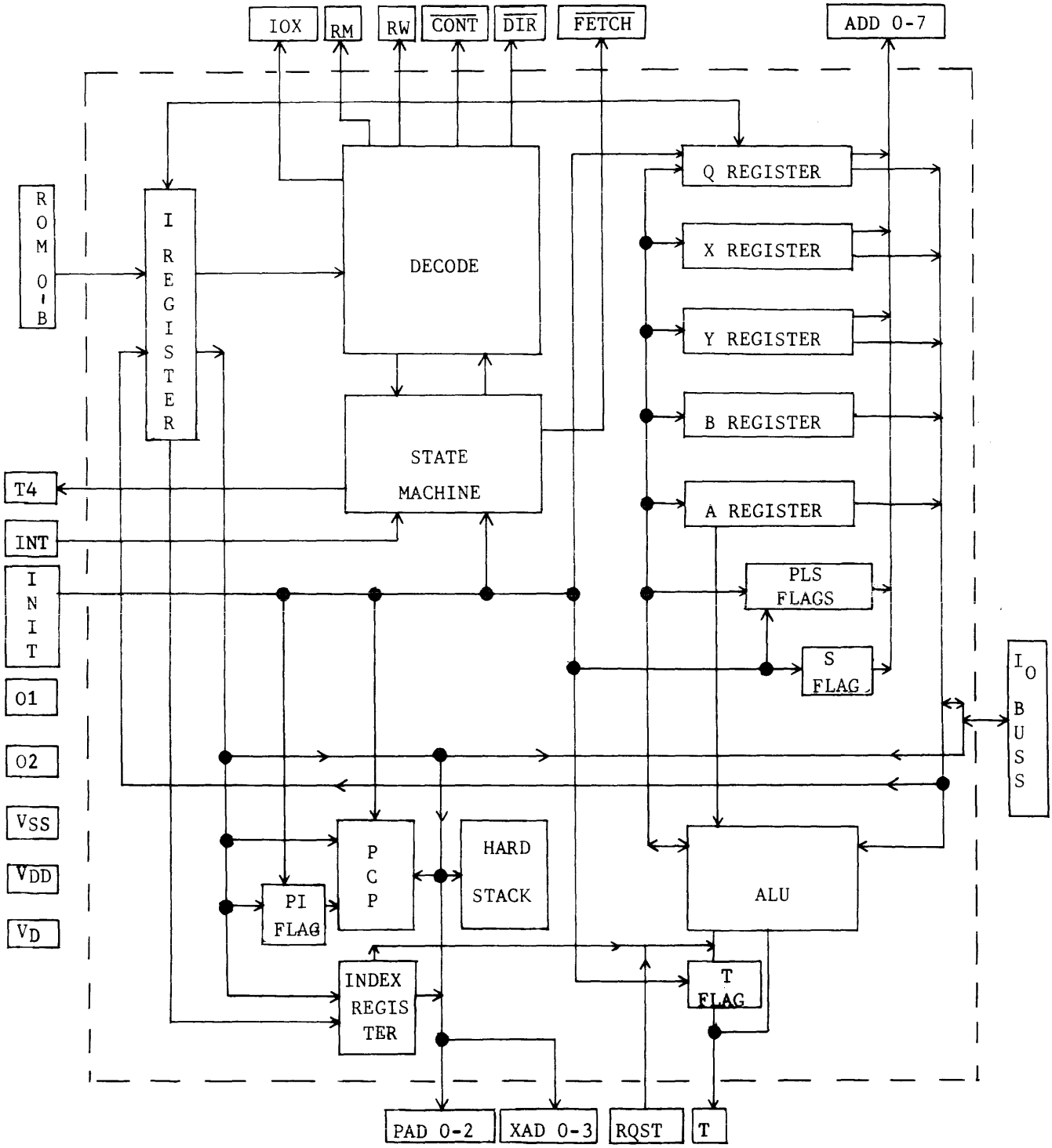


FIG. IIC-118 BLOCK DIAGRAM TPU LSIC

PORT ADDRESS GENERATION

The TPU Micro-processor generates 16 active addresses (0-15), used to load the four PCF ports and interrogate the status of the PCF mechanisms via the RQST/-B signal. Fig. IIC-120 shows the port load functions when the port addresses 0-4 are active. Port addresses 5-15, when active, will bring up the RQST/-B line. The TPU monitors the RQST line at these times as the TPU Micro-processor must know the status of the PCF mechanics so that loading of the four ports, and, execution of the commands loaded will occur at the correct time in relation to the mechanics. Referring to the TPU program flow shown in Fig. IIC- it can be seen that the TPU interrogates the Forms Timing Unit (FTU) for every decoded PCF function. The status of the FTU is interrogated at the TPU port 9 address time. Since there are 4 TPU generated address lines, XAD0-XAD3, it can be seen that port address 9 consists of:

	XAD0	XAD1	XAD2	XAD3
Binary Value	1	2	4	8
	1	0	0	1

These four address lines are inputs to both the 1 of 10 Decoder as well as the RQST Multiplexer as shown in Fig. IIC-120. The 1 of 10 Decoder generates the PORT9/ signal, however, this signal is not used and merely serves as a test point. There are only five active addresses out of the 1 of 10 decoder which are actually used. These are Port 0 - Port 4. Their functions are shown in Fig. IIC-120.

XAD0 - XAD3 are also inputs to the RQST Multiplexer. XAD3 is inverted and acts as the select or enable line to the Multiplexer. Whenever XAD3 is set, addresses 8-15, the RQST Multiplexer will be enabled to reflect the status of the control inputs, O/CRY - DCEL, onto the RQST/-B output as shown in Fig. IIC-120.

The generation of the port addresses 8-15 is a function of the RQST Multiplexer with XAD3, TPU address of 8, required to enable the Multiplexer.

The Port 8 - Port 15 addresses are valid TPU generated addresses decoded internally by the RQST Multiplexer. With exception of PORT8/ and PORT9/ signals out of the 1 of 10 Decoder no signal line is provided showing the Port 10 - Port 15 addresses. The Port 10 - Port 15 address, however, are used internally by the RQST Multiplexer to develop RQST/-B.