B 0489

DISK DDP

(FOR B700 SYSTEMS)

Burroughs

FIELD ENGINEERING

TECHNICAL MANUAL

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LIST OF ILLUSTRATIONS

INTRODUCTION AND OPERATION

The B0489 DDP provides the interface between the A9480-X Magnetic Disk Unit and the B700 System computer. The B0489 DDP controls the transfer of information to and from disk. A magnetic disk unit may be either a single drive A9480-1 or a dual drive A9480-2 configuration. The recording medium is provided by the magnetic disk cartridge.

The disk DDP acts upon Control Word from the processor, performs the operation specified, and upon completion of the operation, generates a status word containing operation status and/or error status information. The Port Select Unit will control the synchronization of the DDP interface with the processor.

The processor in operating the disk DDP can do a Device Write (DW), a Device Read (DR) or an Address Status Request (ASR). Below are the device operating tables.

DEVICE OP'S		CONTROL BITS (MIR)	COMMENTS
DW	OS1 & Dev. Addr.	MIR16/	Seek OP.
DW	OS1 & Dev. Addr.	MIR15/	Read Next Sec. OP.
DW	OS1 & Dev. Addr.	MIR16/ & 15/	Not Allowed
DW	OS1 & Dev. Addr.	MIR14/	Write Next Sec. OP.
DW	OS1 & Dev. Addr.	MIR16/ & 14/	Enable Marks OP.
DW	OS1 & Dev. Addr.	MIR15/ & 14/	Locate and Verify OP.
DW	OS1 & Dev. Addr.	MIR16/, 15/ & 14/	Not Allowed
DW	Dev. Addr.		Write Data to Disk
DR	OS1 & Dev. Addr.		Read Status
DR	Dev. Addr.		Read Data from Disk
ASR			Read Address of Device and Device Status

The processor device operations DW, DR and ASR will be enabled to the Port Select Unit. The address of the device to receive the operation will be contained in the Base Register (1 or 2) and will be enabled to the OS lines. The OS lines will select which of the two PSU's is to be enabled and which of the four device connected to that PSU.

DW will enable the Write line to the device selected by the OS lines. DR will enable the Read line to the device selected by the OS lines. ASR will enable the Enable Status (ENST) line to the device DDP that is sending an IRQ and has the highest priority. It also encodes the address of that DDP to the EXT lines from the PSU.

OS1, which is the instruction bit, will enable the Instruction (INST) line to all devices, but only that device selected by the OS lines will act upon the INST.

The DDP will send Data Interrupts (DINT) and Status Interrupts (SINT) to inform the processor when necessary. The processor receives the DINT's and SINT's as IRQ, SRQ and URQ. The processor will act upon these conditions with the device operations as shown previously.

INTERRUPT	UNSELECTED	SELECTED	CONDITION
DINT.	*		IRQ
DINT		*	SRQ
SINT	*		IRQ
SINT		*	URQ

WORD FORMATS

There are four word formats that are used in operations involving the disk DDP. Refer to Fig. I-1

Control Word – Operations of the disk unit are initiated by the transfer of a Control Word on the MIR lines from the processor to the disk DDP. The Control Word will consist of an operation field which defines the function to be performed by the disk, and a Disk Address Field which specifies the unit, drive, surface and track of the disk to be operated on.

Data Word – Data that is tranferred between the processor and the disk will be contained in the Data Word. The Data Word is 16 bits long, where Bit 16 is considered the least significant bit and is contained in the MIR lines.

Status Word – The Status Word contains a status field that is inserted by the DDP and a Device Address Field which is inserted by the Port Select Unit. The Status Word will be enabled to the EXT lines upon request by the processor.

Address Verify Word – The Address Verify Word will be contained in the MIR register. This word will be sent to the DDP as part of the Locate and Verify operation. The Address Verify Word will contain a Sector Address Field, a Surface Field and a Track Address field.

DISK DDP WORD FORMATS

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Select	Drive Select	Track 8	Track 7	Track 6	Track 5	Track 4	Track 3	Track 2	Track 1	Track 0	Face	Term	Oper 2	Oper 1	Oper 0
Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
Data Request	Time out	- -	Dev Addr 4	Dev Addr 3	Dev Addr 2	Dev Addr 1	Dev Addr 0	File Not Oper	Sector Mark	Index Mark	Pos Set	Pos Er	III Addr	Write Inhibit	Service Late
Track 7	Track 6	Track 5	Track 4	Track 3	Track 2	Track 1	Track 0	Track 1	Track 0	Surface Select	Sector 4	Sector 3	Sector 2	Sector 1	Sector 0

NOTE: Device Address Bits of the Status Word are inserted at the PSU.

	OP2	OP1	OP0
No OP	0	0	0
Seek	0	0	1
Read Next Sect	0	1	0
Not Allowed	0	1	1
Wrt Next Sect	1	0	0
Enable Mks	1	0	1
Loc & Verify	1	1	0
Not Allowed	1	1	1

Fig. I-1

DESCRIPTION OF THE DISK DDP WORD FORMATS

CONTROL WORD

MIR BIT(S)	FUNCTION
1	Unit Select – (Don't care bit)
2	Drive Select – Selects upper or lower drive of the disk unit selected by bit 1.
3-11	Track Address – Selects one of 203 or 406 disk tracks to be accessed for an operation.
12	Surface Select – Selects upper or lower surface of the disk cartridge in the drive selected by bits 1 and 2.
13	Terminate – Notifies the DDP to discontinue all data interrupts to the processor. This will terminate the data transfer between the DDP and the processor.
14, 15, 16	Operation Code – Notifies the DDP of the operation to be performed by the disk.

CODE	OPERATION
000	No OP.
001	Seek – Positions read/write heads to track specified by the address field.
010	Read Data – Initiate read OP. starting at the next sector mark of disk.
100	Write Data – Initiate write OP. starting at next sector mark of disk.
101	Enable Disk Marks – Enable SINT's for each [illegible] sector mark.
110	Locate and Verify – Initiate the addr. locate and verify procedure.
111	Illegal Code

DATA WORD

MIR BIT(S)	FUNCTION
1-16	Data – Used to transfer a byte pair of data between the disk and the Disk DDP.

STATUS WORD

EXT BIT(S)	FUNCTION
1	Data Request – The Disk DDP is ready to receive or transmit the next character. This status condition follows the data interrupt signal to the processor.
2, 3	Not Used
4 - 8	Device Address – The device address bits are inserted into this field by the Port Select Unit.
9	File Not Operational – The addressed disk is not available for operation.
10	Sector Mark – A sector mark has been detected, signalling the start of a new sector. This signal is received from the disk unit every 1.25 milliseconds.
11	Index Mark – An index mark has been detected, signalling the start of a new revolution. This signal is received from the disk unit every 40 milliseconds.
12	Seek Complete – Positioner movement has stopped; that is, sufficient time has elapsed for the positioning and settling of the read/write heads.
13	Seek Error – Seek operation required more than 200 milliseconds to complete.
14	Illegal Address – Disk unit has received a track address in excess of 202 or 405.
15	Write Inhibit – File protect condition has been detected while an attempt was made to write on disk.
16	Service Late – Read or write command not issued to the DDP within two sector marks after address verification.

ADDRESS VERIFY WORD

MIR BIT(S)	FUNCTION
2-10 ~~1-8~~	Track Address
~~9-10~~ /	Not Used
11	Surface Select
12 - 16	Sector Address

DISK SEGMENT FORMAT

A disk segment is formatted as such: the first part of the segment is the preamble, followed by the data and then the postamble. Refer to Fig. I-2.

Segment Preamble – The Segment Preamble consists of the first 36 bytes. The first 32 bytes are all zeros and are used for timing. The next two bytes are the sync bytes and are used for synchronization. The last two bytes are used for the address and consist of two bits of zeros, one bit for surface select, eight bits of track address and five bits of the segment address.

Segment Data – The data portion of the segment immediately follows the preamble and consists of 180 bytes of data recorded in bit serial form.

Segment Postamble – The Segment Postamble consists of approximately 16 bytes. The first byte is a parity byte and the remainder of the postamble is all zeros.

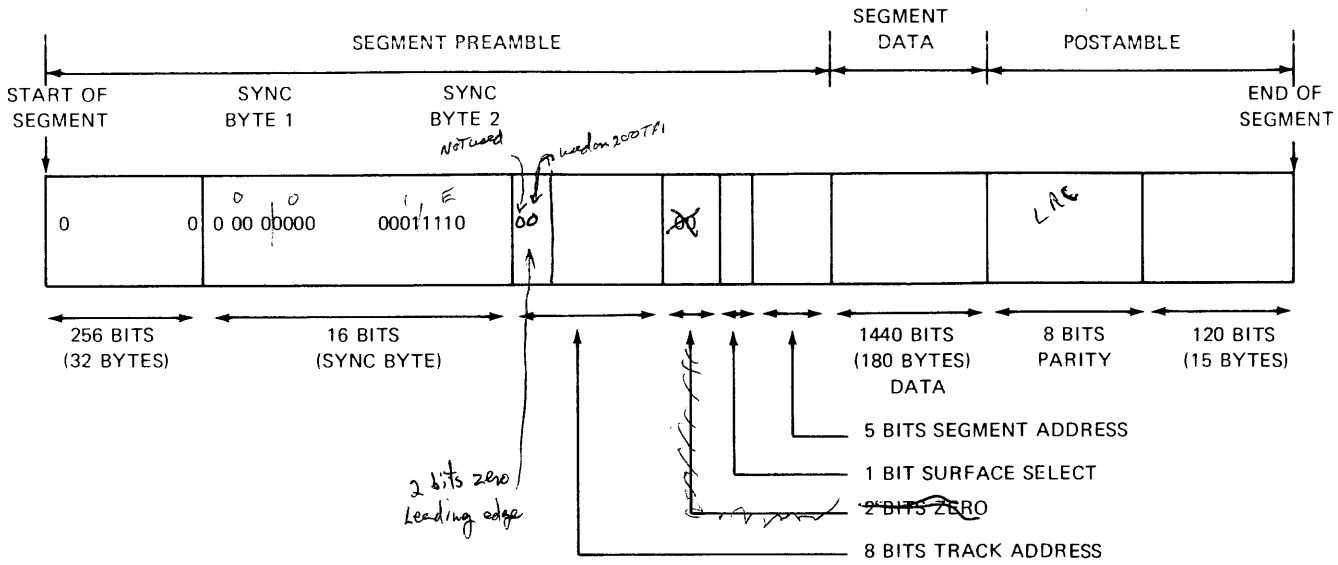


Fig. I-2 DISK SEGMENT FORMAT

PROCESSOR FIRMWARE DESIGN CONSIDERATIONS

Initialization – To initialize the disk, the processor firmware issues a Control Word with the Enable Disk Marks bit set. The writing of data is performed without address verification on a per sector basis, starting at the index mark of each track.

Seek – To initiate a Seek operation, the processor firmware issues a Seek command to the DDP with the appropriate bits set in the track, drive, and unit select fields. To perform a Seek operation simultaneously on both drives of a disk unit, the processor firmware may issue a Seek command sequentially to each disk drive.

Address Verify – The processor firmware may at any time issue the Locate and Verify command in order to initiate the Sector Locate and Verify procedure. Upon receiving a Data Interrupt from the DDP, the processor firmware transfers a Disk Address Word to the DDP. Upon Seek completion, the DDP compares the Disk Address with that of each segment of the track. Upon receiving a second Data Interrupt from the DDP which specifies that the DDP has located the appropriate segment and stored its Disk Address into the Buffer Register, the processor firmware reads the Disk Address Word from the DDP and compares it with the Disk Address Word that was issued.

Word Count – Prior to the initiation of a Read Data or Write Data instruction, the processor stores in main memory a word count corresponding to the number of words to be transferred to or from disk. This count is decremented by one for each word received from or transmitted to the disk. When the word count reaches zero, a Terminate instruction is sent to the DDP disabling further Data Interrupts.

Read/Write – A Read or Write command is issued following the Address Verify procedure. If a Read or Write command is not issued to the DDP within one sector mark after Address Verification, the DDP returns a sector mark Status Interrupt to notify the firmware of the condition. If a Read or Write command is not issued to the DDP within two sector marks after Address Verification, the DDP sets the Service Late Status bit.

Block Check – When data is written to the disk, a Block Check is generated for the 180 data characters transmitted and stored in the Block Check position of the segment (parity byte). Then, when this same segment is subsequently Read from disk, a second Block Check is generated for the 180 data characters received from disk and compared with that Block Check which was previously computed and stored in the segment. If they are equal, the data is accepted; otherwise, a retry is entered.

HARDWARE DESIGN CONSIDERATION

Data Buffers – Two 16-bit data registers are contained within the DDP, which are provided to buffer data transfers between the processor and the disk.

Control Word – If a control signal is received from the processor coincident with the Write signal and the Instruction bit, it specifies that information on the MIR lines is a Control Word.

Read Status – If a control signal is received from the processor coincident with the Read signal and the Instruction bit, it directs the DDP to place all status indicators on the EXT lines to the processor.

Seek – This command directs the disk unit to position its read/write heads to the track specified on the Track Address lines. Upon receipt of the Seek complete signal from the disk, the DDP will initiate the sector Locate and Verify command if received from the processor; otherwise, it will wait until the next instruction is received from the processor. If a Seek command is received from the processor for the other disk drive while the first Seek is in process, the DDP will execute the command.

Write Data – A Write Data command causes the disk unit to initiate a Write operation starting at the appropriate sector, and the Data Interrupt line to the processor is energized to request a Data Word. The processor responds by sending a Write signal, which causes the DDP to accept the Data Word from the Data lines and transmit it to disk, bit by bit in a serial manner. This cycle is repeated for each word until a Terminate instruction is received from the processor, after which zeros are sent to the disk until the next sector mark is sensed.

Terminate – A Terminate command causes the DDP to discontinue Data Interrupts to the processor for the sector currently being operated on. If a subsequent Read or Write instruction is not received from the processor (indicating a multiple record transfer), the Read or Write line to the disk is disabled at the next sector mark.

Enable Disk Marks – If this command is received coincident with a Read Data instruction, the Status Interrupt is enabled for each sector mark received from disk. The function is disabled if a Read Data instruction is received and this bit is zero.

The Enable Disk Marks function is used normally during disk initialization.

Locate and Verify – Upon receipt of a sector Locate and Verify command from the processor, the DDP (upon Seek completion if in process) will return a Data Interrupt to the processor. Upon receipt of the Disk Address Word from the processor, the DDP will compare it with that read from the disk address field of each segment of the track. Upon locating the proper segment, the DDP stores the address read from the disk and energizes the Data Interrupt line to the processor.

Service Late – If upon completion of Address Verify the DDP does not receive a Read or Write command within one sector mark, the DDP returns a sector Mark Status Interrupt to the processor. If the DDP does not receive a Read or Write command within two sector marks after Address Verification, the DDP sets the Service Late status bit and returns a Status Interrupt to the processor upon receipt of the Read or Write command.

Status Indicators – All Status Indicators are returned to the processor in response to an Enable Status signal (ASR) or a Read Status request from the processor.

Status Interrupts – The Status Interrupt line to the processor is energized with the leading edge of any status condition except Data Request, Seek complete and index mark, none of which results in a Status Interrupt when the device is executing an operation.

SIGNAL INTERFACE

There are 23 signal lines in the interface between the magnetic disk unit and the disk DDP. Of these, 14 are lines from the disk DDP to disk unit and nine are from the disk to the disk DDP.

SIGNAL LINES FROM DDP TO DISK

SIGNAL NAME	DEFINITION
Data (Write to Disk) (WRTDATA/)	Used for transfer of information from the disk DDP to the disk. This information is transmitted bit serially to the disk at a rate of 1.56 MHz.
Seek (SK/)	Position read/write heads to the track specified by the address on the Track Address lines.
Write (WRTEN/)	Write the data received over the Write Data line on the selected segment of the track. Writing starts at the beginning of a sector and continues until a complete sector is written.
Read (RDEN/)	Transmit over the Read Data line the information read from the selected segment of the track. Reading starts at the beginning of a sector and continues until a complete sector is read.
Drive Select (UNITSEL1/)	Specifies which of the two disk drives to select for operation.
Surface Select (HEADSEL/)	Specifies which of the two surfaces of a disk to select for operation.
Track Address (ADD1/-ADD256/)	Specifies the track address at which the read/write heads are to be positioned during a Seek operation.

SIGNAL LINES FROM DISK TO DDP

SIGNAL NAME	DEFINITION
Data (Read from Disk) (DFD/)	Used for the transfer of information from disk to the disk DDP. This information is received bit serially from disk at a rate of 1.56 MHz.
File Operational (FILEOP/)	Addressed disk is fully operational.

Write Inhibit (WIH/)	Write inhibit condition was detected by the disk while the file protect feature in the addressed disk was actuated.
Illegal Address (ILLGADD/)	Disk has received a track address in excess of 203.
Positioner Error (POSERR/)	Seek operation required more than 200 milliseconds.
Positioner Settled (POSSET/)	Disk positioner movement has stopped and a sufficient period of time has elapsed for settling of the read/write heads.
Index Mark (INDEX/)	Indicates the start of a new revolution. This signal is received from disk every 40 milliseconds.
Sector Mark (SMK/)	Indicates the start of a new sector. This signal is received from disk every 1.25 milliseconds.
Data Clock (DCLK/)	This signal is received from disk at a pulse rate of 1.56 MHz and is used to strobe the read/write data from/ to the disk.

PSU INTERFACE LINES TO THE DDP

CLEAR	Clear
WRITE/	Write Line
READ/	Read Line
INST	Instruction Line
ENST/	Enable Status Line

PROCESSOR INTERFACE LINES TO THE DDP

LUMIR01/-16/	Memory Information Register
PONCL/	Power On Clear

DISK INTERFACE LINES TO THE DDP

POSSET/	Disk Seek Complete Level
DCLK	Disk Clock
DFD/	Data from Disk
FILEOP/	File Operational
ILLGADD/	Illegal Address
INDEX/	Index Mark
POSERR/	Seek Error
SMK/	Sector Mark
WIH/	Write Inhibit

B0489 INTERNAL SIGNAL NAMES

D1CLEAR	Clear Line from PSU
D1DIN	Data Request
D1DINT/	Data Interrupt
D1EXT02/	Time Out Status Bit
D1GSMK/	Gated Sector Mark
D1INSF	Instruction Flip-Flop
D1INWT	Instruction Write
D1LATEF	Late Flip-Flop
D1LDIR	Load Input Register
D1OPCMP	Operation Compare Enable
D1RDAT/	Read Data – Enables the Output Register to the EXT lines
D1RDES	Read Data – Enables Status, True = Enable Status, False = Read Status
D1SINTF/	Status Interrupt Flip-Flop
D1SMK/	Sector Mark
D1STEN	Status Enable – Enables the Status Bits to the EXT lines
D1WNS	Write Next Sector
D2EXT09/-16/	External Lines to Processor
D2FACE	Selects 1 of 2 Surfaces
D2OPRD-OPRD/	Operation Read – Enabled by Control Bit MIR15/
D2OPWT-OPWT/	Operation Write – Enabled by Control Bit MIR14/
D2RDENF	Read Enable Flip-Flop
D2SINT/	Status Interrupt Level to set the Status Interrupt Flip-Flop
D2SK/	Seek Command Level to Disk enabled by Control Bit MIR16/
D2SR9	Shift Register Bit 9
D2ADD1/-ADD4/	Three Bits of Track Address to Disk
D2WTEN/	Write Enable Line to Disk
D2WTENF	Write Enable Flip-Flop
D3CEND/	Compare End Flip-Flop
D3DFD	Data from Disk
D3UNITSEL2/	Selects 1 of 2 Drives
D3WRTDATA/	Data to Disk Line to Disk
D3EXT01/-08/	External Lines to Processor
D3HEADSEL/	Surface Select Line to Disk
D3ORDI/	Output Data Interrupt
D3RDEN/	Read Enable Line to Disk
D3TADD8/-ADD256/	Six Lines of Track Address to Disk
D3UNIT/	Selects 1 of 2 Disk Units
D4CMPEL	Compare Enable
D4DCLK2	Disk Clock
D4DIRQ/	Disk Interrupt Request
D4DFD	Data from Disk
D4LDOR/	Load Output Register
D4LDSR/	Load Shift Register
D4DRYF	Read Ready Flip-Flop

DISK DDP OPERATION

The B0489 Disk DDP is made up of four printed circuit cards. The four printed circuit cards are connected in pairs by the use of foreplane connectors.

Seek – The processor before doing a read or write next sector must first initiate a Seek, and then a Locate and Verify operation.

The processor initiates a Seek operation by doing a Device Write with the base register loaded with the Instruction bit and the address of the device. The processor enables the Control Word to the MIR lines. The Control Word will contain the unit, drive, track and the surface information, along with the type of operation to be performed. For a Seek operation, MIR16/ will be false. The Address Information will be enabled into the address register of the DDP and sent to the disk on the Address lines. The operation code will be enabled into the operation register. The output of the operation register will enable the disk Seek command to the disk, D2SK/.

Locate and Verify – While the disk is performing the Seek operation, the processor will initiate a Locate and Verify operation. The processor will execute a Device Write operation with the Instruction bit set in the base register along with the address of the device. The processor also sends a Control Word to the DDP on the MIR lines. The Control Word contains the disk address and the operation code for a Locate and Verify operation. The PSU will enable the Write and Instruction lines to the DDP. For the operation code, MIR14/ and 15/ will be false, and enabled into the operation register. The outputs of the operation register will enable the following control levels: D2OPRD and D2OPWT. (See Fig. II-1) The Write and Instruction line from the PSU will set the Instruction flip-flop (INSF). See Fig. II-2. INSF, along with OPWT, will set the Data Interrupt flip-flop (DINT). See Fig. II-3. The DINT will go to the PSU and enable an SRQ if the DDP is selected, or an IRQ if the DDP is unselected. When the processor responds to this DINT, the Address Verify Word will be sent to the DDP via the MIR lines. The processor executes a Device Write with the Instruction bit not set since this word is not an instruction, but data. The DW will enable the Write line to the DDP as directed by the OS lines. The Write line will enable the control level to load the input register (D1LDIR) so that the data on the MIR lines may be stored for further use. See Fig. II-2 and II-5.

Control level OPRD will set the Read Enable flip-flop (D2RDENF) following the next Sector Mark from disk (SMK/) and the Seek operation is complete, POS SET/. See Fig. II-1. D2RDENF will enable the Read line to the disk (D3RDEN/) to go false. The disk will start to read data to the DDP. As shown previously, the first part of the segment is the preamble. The segment address is contained in the preamble and must be separated.

The DDP will locate the address by first detecting the sync byte. The preamble, as it is being read, is directed into a sync detector circuit. A MOD 16 counter is used to count the number of 1's read from disk. The sync byte is identified by four 1's. When the fourth 1 is detected, the sync flip-flop will set. The sync flip-flop will reset the counter and set the Read Ready flip-flop (RDRYF). See Fig. II-4.

NOTE: If the 1's counted are not in consecutive order, the counter will be reset.

Control levels OPRD and OPWT will enable the Operation Compare Level (D1OPCMP). See Fig. II-2. D1OPCMP and sync will transfer the data in the input register to the shift register by enabling control level D4LDSR/ to go false. See Fig. II-4 and II-5. The Address Verify Word is now in the shift register.

D1OPCMP and RDRYF will enable Level Compare Enable (D4CMPEL). See Fig. II-4. RDRYF will also reset the Sync flip-flop. Once the Sync flip-flop is reset, the counter will release to count disk clocks. This is done since the segment address is only 16 bits. The DDP must know when those 16 bits have been read; each clock represents one bit of data. When the first clock is counted, level LDSR/ goes true, allowing the Address Verify Word that is in the shift register to be shifted out serially on the Data to Disk line (DTD). At the same time, the data being read from disk is loaded into the shift register serially on the Data from Disk line (DFD). See Fig. II-5. The DTD line contains the Address Verify Word and the DFD line contains the segment address of the segment being read from disk. These two addresses will now be compared.

The DTD and DFD lines are fed into the comparator circuit as shown on Fig. II-6. If all of the address bits compare, the comparator output will remain true. The comparator output is the clock input for the Compare flip-flop (CMPF). The Compare flip-flop was enabled by the level Compare Enable (CMPEL/) going false. CMPEL/ goes false when the Sync flip-flop is reset by the RDRY FF. The Compare flip-flop was set at the start of the compare. If the addresses compare, the flip-flop will remain set. When the last address bits are being compared, the counter is being reset. The counter equal to zero level (CNT=0) will enable the load output register level (D4LDOR/) to go false. The segment address that was loaded into the shift register is now transferred into the output register. D4LDOR/ False will enable CMPF to set the Compare End flip-flop (D3CEND) and enable the output register data interrupt level (D4ORDI/ to go false. See Fig. II-6. D4LDOR/ False also allows the Terminate flip-flop to set (TERM). See Fig. II-9. TERM/ will disable the Compare flip-flop by causing D4CMPEL/ to go true. TERM/ will also disable the counter. D4ORDI/ False will set the data Interrupt flip-flop. This DINT will go to the PSU and enable an SRQ or an IRQ to the processor. In the above routine, if the address bits do not compare,

the output of the comparator will drop false causing the Compare flip-flop to be reset. When CNT=0 and D4LDOR/ are enabled, the Compare End flip-flop will not be set and D4ORDI/ will not go true. The shift register will be transferred to the output register, but will not be used. When the next sector mark occurs, Read Enable flip-flop and the Read Ready flip-flop will be reset. The RDRY FF being reset will cause D4LDOR/ to go true. D4LDOR/ going true will cause the Term flip-flop to reset.

The sector mark will also set the Read Enable flip-flop which will enable the Read line to the disk. The next segment will be read. This routine continues until the correct address is found and a DINT is set. The processor will respond to the DINT with a Read Next Sector or a Write Next Sector.

WRITE NEXT SECTOR

Once the Locate and Verify operation is complete, the processor can now initiate a Write Next Sector operation. The processor executes a device operation, Device Write. The processor will also enable the base register to contain the Instruction bit and the address of the device.

The DW operation and the base register will be enabled to the PSU. The DW will enable the Write line to the device selected by the base register on the OS lines. The Instruction bit, OS1, will enable the INST line to the DDP. The processor will send a Control Word to the DDP from the MIR register. The Control Word will contain the unit, drive, track, surface and the type of operation to be performed.

For Write Next Sector, the operation code will have MIR14/ False. MIR14/ False will be enabled into the operation register. The operation register will enable the control level (D2OPWT). D2OPWT/ False will clock the Write Enable flip-flop (D2WTENF) following the next sector mark. D2WTENF will enable the Write line to the disk (WRTEN) to go false. See Fig. II-1.

The Write and INST levels from the PSU will enable the setting of the Data Interrupt flip-flop (DINT). When the processor responds to this DINT, the processor will do a Device Write (DW) and insure that the base register contains the Device Address and the Instruction bit reset. The PSU will enable the Write line to the DDP, as selected by the base register OS lines. The Write line will enable the control level D1LDIR, load input register. D1LDIR will enable the MIR lines that now contain data into the input register. See Fig. II-2 and II-5. The input register will be transferred into the shift register by control level D4LDSR/ going false, when the Write Enable flip-flop was set. See Fig. II-4. D2WTENF will also enable the MOD 16 counter to count disk clocks. At the first count, the control level D4LDSR/ goes true, enabling the shift register to shift the data serially to the disk on the DTD line. Before the counter starts, counter CNT=0 was true, which caused D4LDSR/ to go false and enabled level DATRQ, data request. See Fig. II-4. DATRQ will set the Data Interrupt flip-flop. When the processor responds to this DINT, the processor will send another word of data on the MIR lines to the DDP. This word is loaded into the input register by the write level from the PSU, so while the data is being shifted out to the disk, the next word is loaded into the input register.

When the last bit in the shift register has been shifted out to the disk, the counter will be reset. CNT=0 will go true, enabling DATRQ to go true and D4LDSR/ to go false. DATRQ will set the Data Interrupt flip-flop and D4LDSR/ being false will enable the next word from the input register into the shift register. The data will again be shifted out to disk while the processor is responding with another word of data. This operation continues until the processor has sent the last word of data to the DDP.

When the processor has sent the last word of data to the DDP, the processor will execute a Terminate operation. The Terminate operation will disable the counter and any other loading of the input register to the shift register. 0's will be shifted out of the shift register to fill in the postamble. The Terminate operation will be discussed further.

After the processor issues a Terminate operation, the processor may issue another Write Next Sector operation, if the next segment is also to be written on. In this case, the next sector mark will reset the Terminate operation and the Write Next Sector operation will take over. If the next segment is not to be written on, the next sector mark will reset the Write Enable flip-flop and disable the Write line to the disk.

Functional Detail

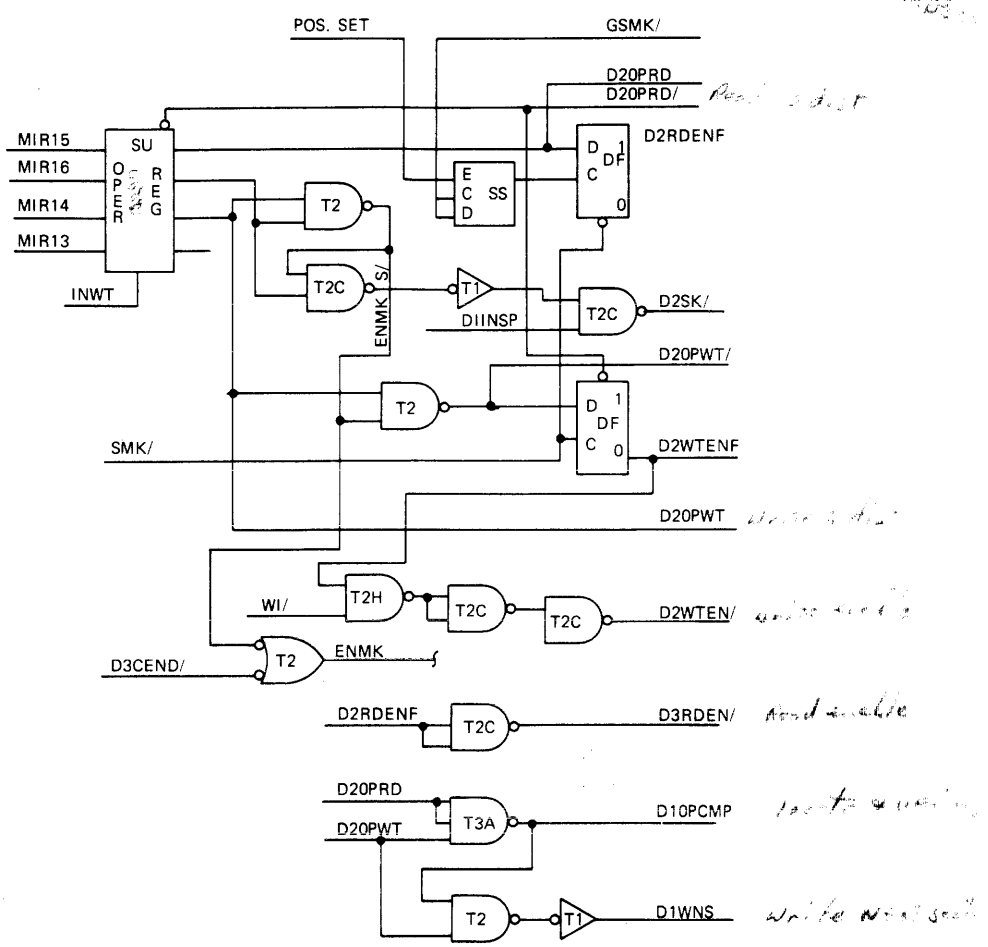


Fig. II-1 CONTROL WORD INPUT

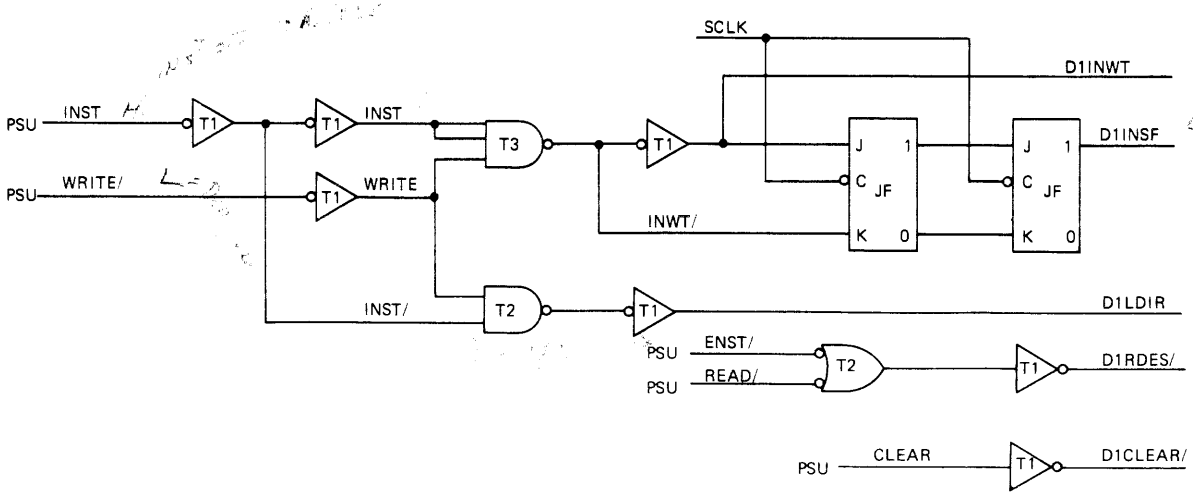


Fig. II-2 PSU CONTROL LINE INPUTS

Functional Detail

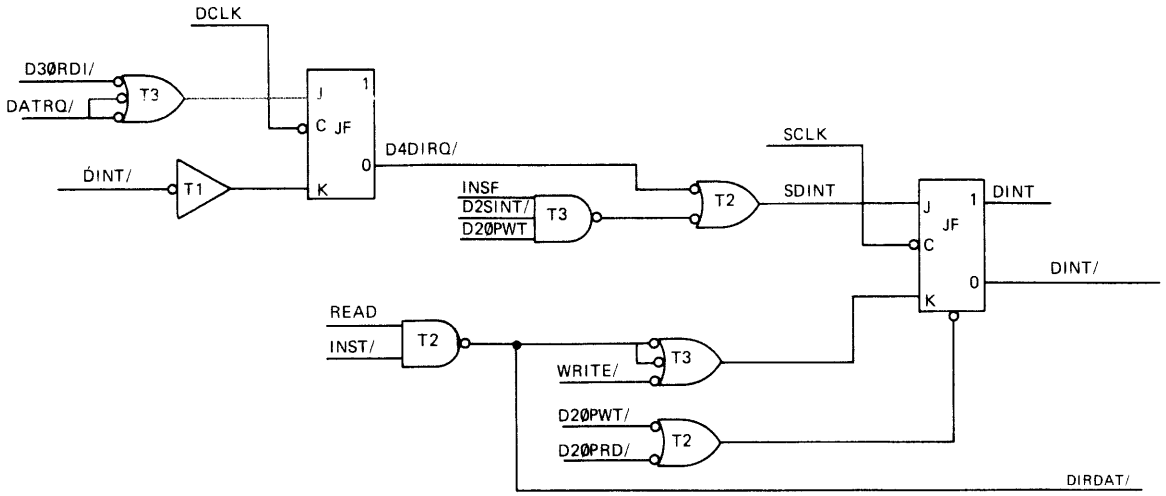


Fig. II-3 DATA INTERRUPTS

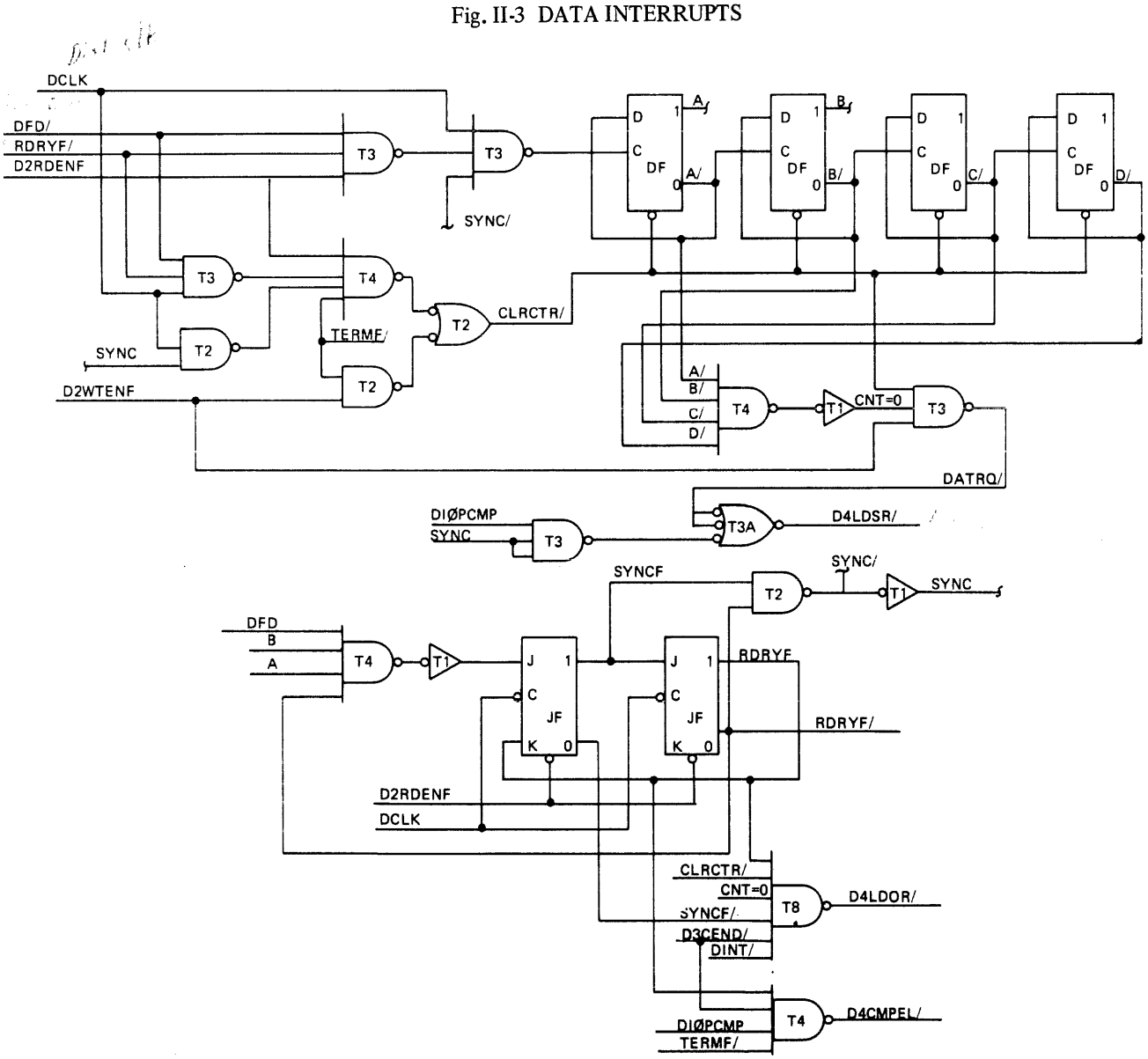


Fig. II-4 SYNC BYTE DETECTOR AND MOD 16 COUNTER

Functional Detail

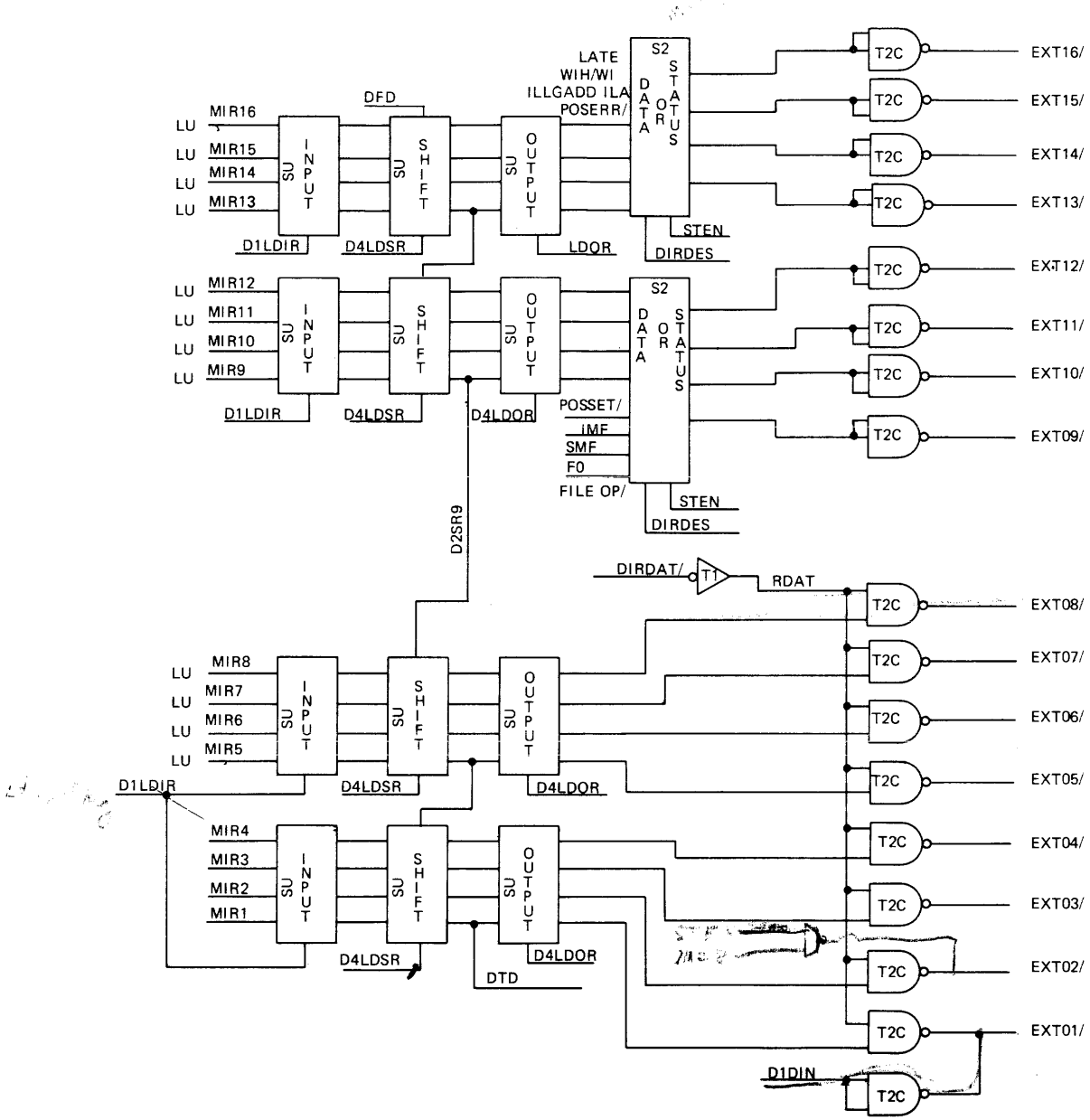


Fig. II-5 INPUT, SHIFT AND OUTPUT REGISTERS

READ NEXT SECTOR

The processor may execute a Read Next Sector operation after the Locate and Verify operation is completed. The processor does a Device Write operation and enables the base register to contain the Instruction bit and the address of the device. The DW OP and the base register OS lines are sent to the PSU, which will enable the Write line to the DDP as selected by the OS lines. The processor sends the Control Word to the DDP on the MIR lines. The Control Word will contain the unit, track, drive, surface of the disk to be operated on and the operation code. The OP code for Read Next Sector is MIR15/ False. MIR15/ being false will be enabled into the operation register by the write and INST levels from the PSU by enabling the control level D1INWT. See Fig. II-2. The operation register will enable control level D2OPRD. D2OPRD will set the Read Enable flip-flop following the next sector mark. See Fig. II-2. When the Read Enable flip-flop sets, the Read Line (D2RDEN/) to the disk will go false.

The Sync byte detector circuit will be enabled. When the Sync byte has been detected, four 1's, the Sync flip-flop will set. The Sync flip-flop will reset the counter and set the Read Ready flip-flop. See Fig. II-4.

The counter will now start to count disk clocks as the data on the DFD line is being shifted into the shift register. The Read Ready flip-flop will reset the Sync flip-flop. When the counter reaches a count of 15, the next count will reset the counter. The address byte, 16 bits, is now in

the shift register. The counter equal to zero (CNT=0) being true, the Read Ready flip-flop set and the Sync flip-flop reset will enable the control level D4LDOR/ to go false. See Fig. II-4. D4LDOR/ being false will enable the shift register to be transferred to the output register. D4LDOR/ being false also enables D3ORDI/ to go false, which will set the Disk Interrupt Request flip-flop output (D4DIRQ/) to go false. See Fig. II-3.

D4DIRQ/ being false will set the Data Interrupt flip-flop. The counter continues to count disk clocks and the shift register is being loaded with the next byte of data. The processor responds to the DINT by doing a Device Read operation. The base register will contain the device address, but not Instruction bit. The PSU will enable the Read line to the DDP as selected by the OS lines. The Read line will enable control level D1RDAT/ to go false. See Fig. II-3. The output register outputs will be enabled to the EXT lines. See Fig. II-5.

When the last bit of the next byte of data is loaded into the shift register, the counter is reset enabling control level D4LDOR/ to go false. The shift register will be transferred to the output register and the Data Interrupt flip-flop will be set. The processor will again respond with a Device Read operation. This operation continues until the processor has received all the data. The processor will then issue a Terminate operation which will disable the setting of the Data Interrupt flip-flop. If the processor wants to read the next segment, the processor must issue another Read Next Sector operation. When the next sector mark occurs, the Terminate operation will be discontinued and the Read Enable flip-flop will be reset. If the processor did issue another Read operation, the Read Enable flip-flop will be set and the Read will take place as explained.

TERMINATE

The processor may at any time during a Read or Write operation issue a Terminate operation. The processor executes a Device Write and enables the base register to contain the device address and the Instruction bit. The Control Word will contain MIR13/ False. The Write and INST line from the PSU will enable MIR13/ into the operation register. Write and INST will also allow MIR13/ to set the Terminate flip=flop (TERMF). See Fig. II-9. TERMF/ being false will disable the Data Interrupt flip-flop from setting by keeping the counter in a reset state with level CLRCTR/ being false. CLRCTR/ False will cause D4LDOR/ to go true. See Fig. II-4. If the processor does not issue another Read or Write operation, the Read Enable or Write Enable flip-flop will reset with the next sector mark.

ENABLE DISK MARKS

The processor will normally issue an Enable Disk Marks operation when the disk is being initialized. The processor will execute a Device Write operation and insure that the base register contains the Device Address and the Instruction bit. The PSU will enable the Write line to the DDP as selected by the OS lines. The INST line will also be enabled to the DDP. A Control Word will be enabled to the DDP on the MIR lines. The Control Word will contain the disk address and the operation code. MIR14/, [redacted] and MIR16/ will be false. The Write and INST lines will enable the MIR bits to the operation register. The operation register output will enable the control level ENMKS/ to go false. ENMKS/ will enable the Index and Sector Marks flip-flops to set when they occur. These flip-flops will be enabled to the EXT lines when the processor enables status. The processor may enable status by doing a Device Read and the Instruction bit set in the base register or by doing an ASR. In each case, the control level D1STEN will be enabled. D1RDES/ will go false. D1STEN True and D1RDES/ False will allow IM to EXT 11 and SM to EXT 10. D1STEN will also reset both flip-flops. See Fig. II-5 and II-7.

STATUS INDICATORS

Late – When the Locate and Verify operation is complete, the processor must respond with a Read or Write Next Sector operation within two sector marks. When the DDP has located the address specified in the Address Verify Word, the Compare End flip-flop was set. The Data Interrupt flip-flop also was set at this time. D3CEND/ will be false and will release the SECMKF flip-flop to set when a sector mark occurs. When a sector mark occurs, the SECMKF flip-flop will set. If the processor does not send a Read or Write operation to the DDP before the next sector mark, the next sector mark will enable the Late flip-flop to set. The late status does not set the Status Interrupt flip-flop. The processor must send an operation to the DDP to set the SINT FF. When the processor does send an operation, the Write line will be false and INST line will be true. These two levels will enable the Instruction flip-flop. Level D1INSF will be true and will enable D1LATE to enable D2SINT/ to go false. D2SINT/ being false will set the Status Interrupt flip-flop. See Fig. II-7. The Late flip-flop may also be set when a Data Interrupt exists and another data interrupt condition occurs before the processor can respond to the first data interrupt.

Write Inhibit – When the processor initiates a Write Next Sector operation and the Write Inhibit line is enabled by the disk, the Status Interrupt flip-flop will be set. See Fig. II-7.

Illegal Address – When the processor initiates a Seek operation and the disk receives a track address greater than 202, the disk will enable level ILLGADD/ to go false. ILLGADD/ False does not set the Status Interrupt flip-flop. The processor will issue another operation, normally a Locate and Verify, which will enable the time out circuit. The time out circuit which consists of a binary counter will

count with each index mark. When the eighth index mark occurs, the time out level will go true. Time out will set the Status Interrupt flip-flop. Time out will be enabled to EXT02/ when the processor reads status. ILLGADD/ being false will also be enabled to the EXT lines when status is read. See Fig. II-7.

Positioner Error – When the disk is performing a Seek operation and it requires more than 200 milliseconds to complete the Seek, the disk will enable the seek error level POSERR/. POSERR/ does not set the Status Interrupt flip-flop. The processor will issue another operation, normally a Locate and Verify operation, which will enable the time out circuit. After the eighth index mark, the Status Interrupt flip-flop will be set. When the processor reads status, time out will be enabled to EXT02/ and POSERR/ will be enabled to EXT13/. See Fig. II-7.

File Not Operational – When the processor initiates an operation and the disk is not operational, the disk will enable level FILEOP. FILEOP and the Instruction flip-flop will set the Status Interrupt flip-flop.

Sector Mark and Index Mark – The sector mark occurs every 1.25 milliseconds. When the processor issues an Enable Marks operation, the sector mark will set the Sector Mark flip-flop. SMF and Enable Marks will set the Status Interrupt flip-flop. See Fig. II-7. The index mark occurs every 40 milliseconds. When the processor issues an Enable Marks operation, the index mark will set the Index Mark flip-flop. The index mark does not set a Status Interrupt; the processor must read status. See Fig. II-7.

Positioner Set – When the disk completes a Seek operation, POSSET/ will be false. POSSET/ being false does not set the Status Interrupt flip-flop. The processor must read status.

Data Request – Whenever the processor reads status and a Data Interrupt condition occurs, Data Interrupt will enable the Data Request line. Data request will be enabled to EXT01/. See Fig. II-7.

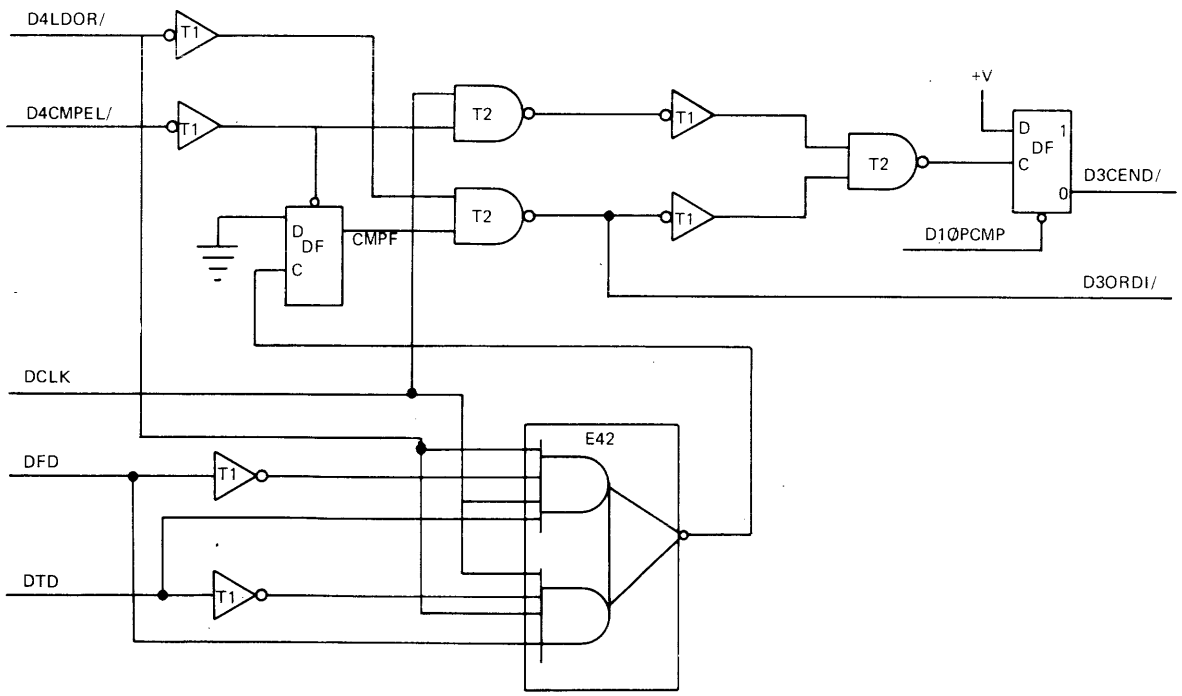


Fig. II-6 COMPARATOR

Functional Detail

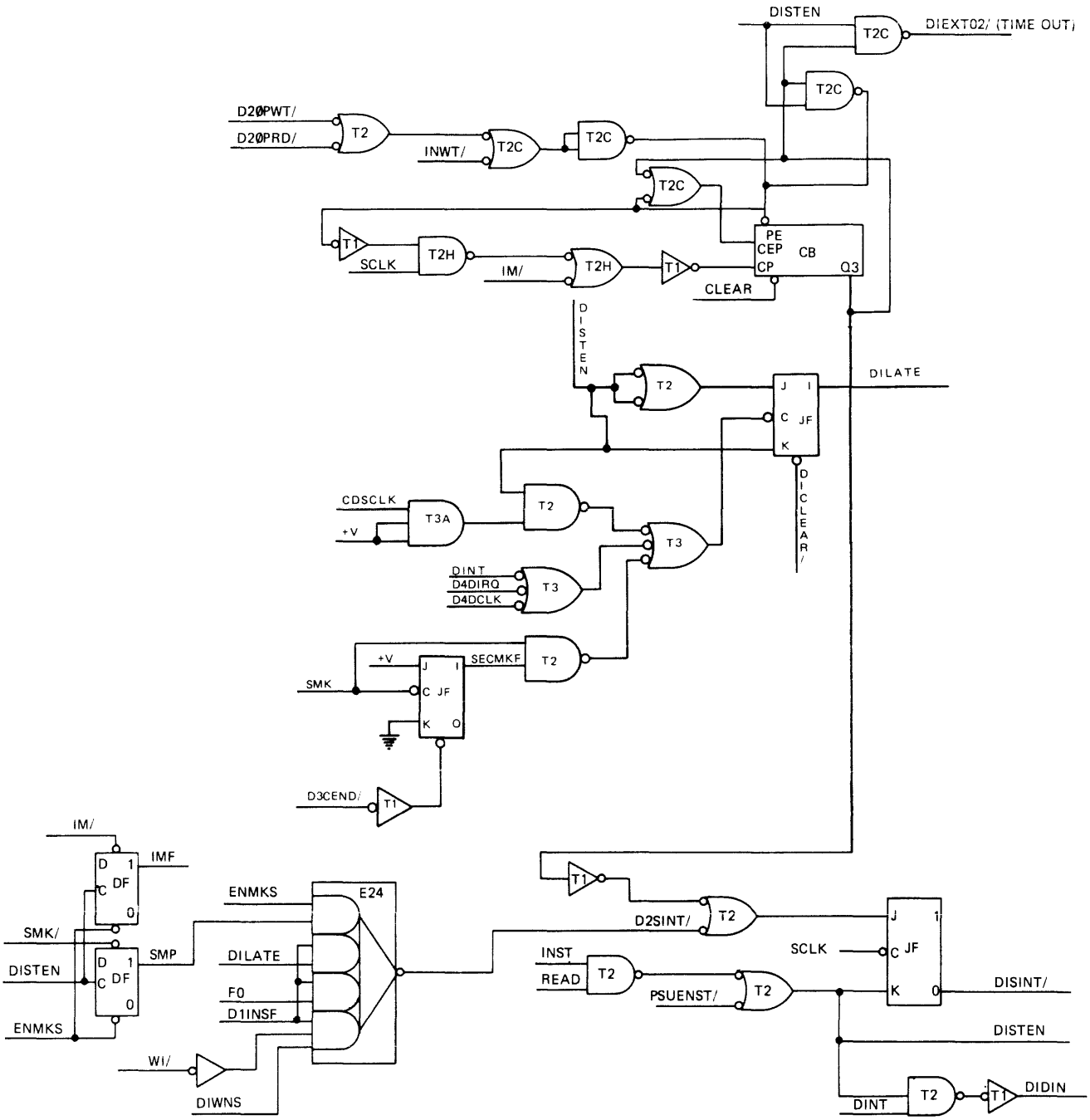


Fig. II-7 INTERRUPTS

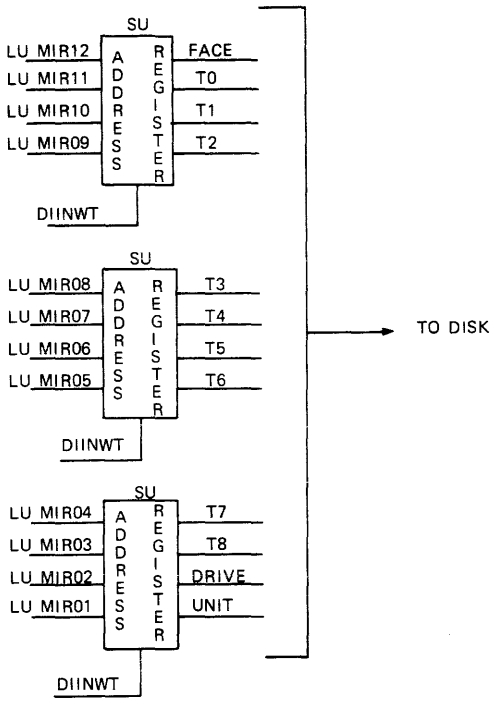


Fig. II-8 ADDRESS REGISTER

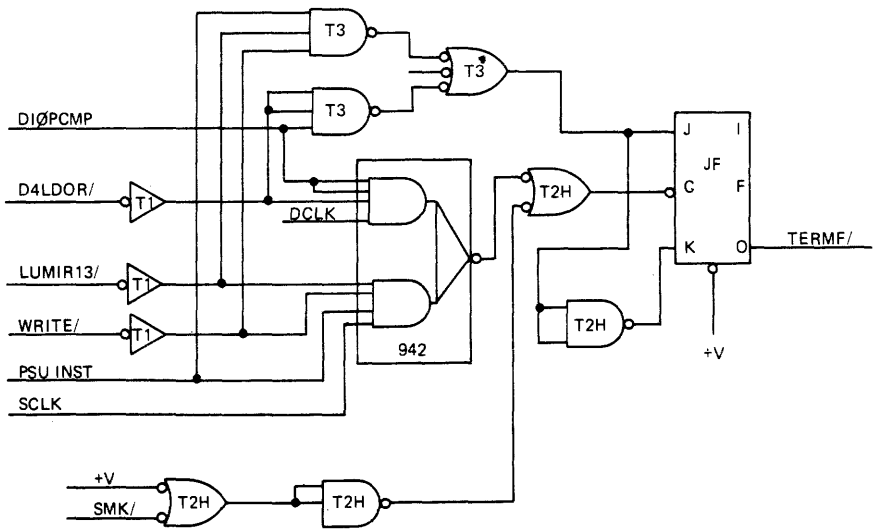


Fig. II-9 TERMINATE

INTRODUCTION

Section III contains the detailed description of the circuits used in the B0489 DDP. The following subsections explains the electronic functions of all the Transistor-Transistor Logic (TTL) circuits used in the B0489 DDP.

TRANSISTOR-TRANSISTOR LOGIC (TTL)

The Monolithic Elements, known as chips, are Dual-In-Line packages with either 14 or 16 pins. See Fig. III-1. The supply voltage for the TTL chips is +5.0 volts. A logical true level (HIGH LEVEL) is between +2.4 volts and +5.25 volts, and a logical false level (LOW LEVEL) is between 0 volts and 0.4 volts.

NAND GATES

The various Nand Gates used in the B0489 DDP are shown in Fig. III-2. The Nand Gates are 2, 3, 4 or 8 input gates. The 2, 3 and 4 input Nand Gates have a high speed gate series. The Nand Gates are identified by: T2 for the 2 input Nand Gate, T3 for the 3 input Nand Gate, T4 for the 4 input Nand Gate and T8 for the 8 input Gate.

The High Speed Gates are identified by T2H for the 2 input gate, T3H for the 3 input gate and T4H for the 4 input gate. The T2C series Nand Gate chips are open-collector output gates and are used for wire or functions. Whenever a Nand Gate is used from this chip, the output of the gate will be connected for a wire or function.

Operation for all Nand Gates used in the B0489 DDP is as follows: a high level output is produced by any low level input and a low level output is provided when all inputs are high.

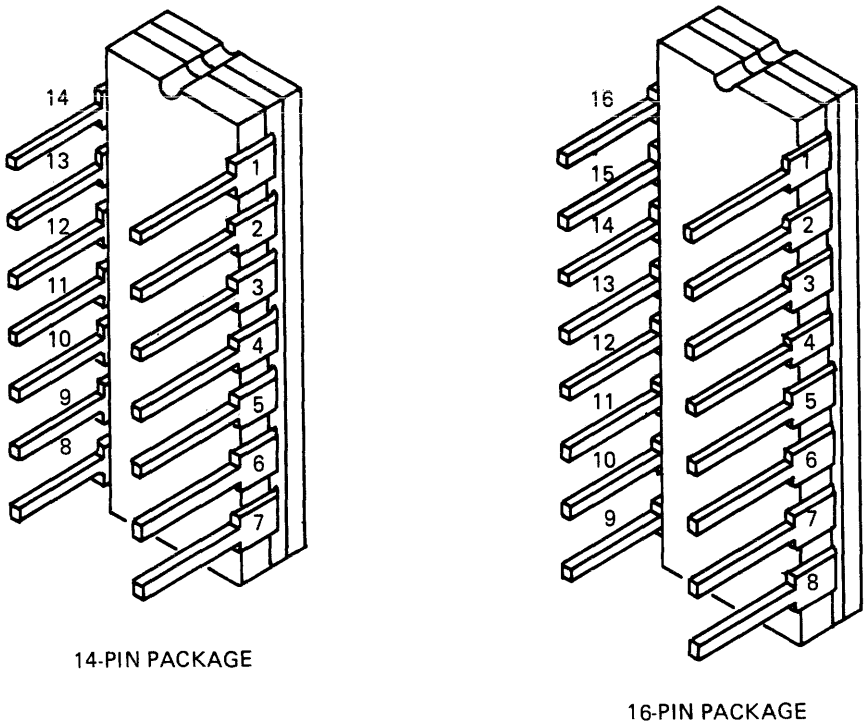
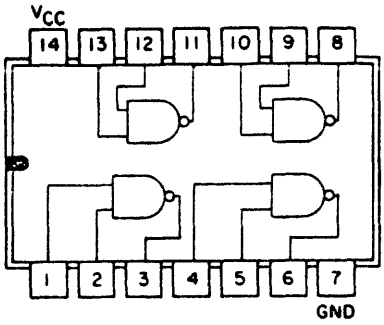
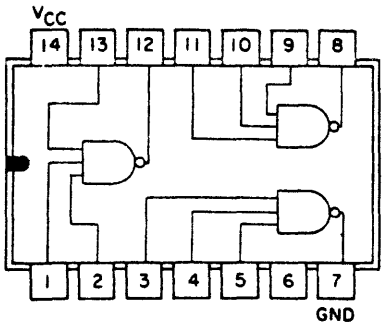


Fig. III-1 14 AND 16 PIN CHIPS

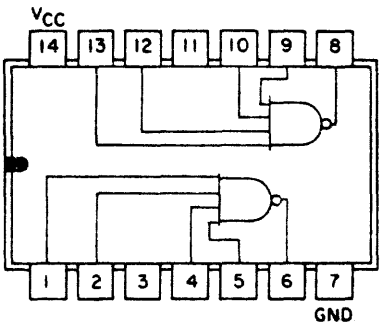
Circuit Detail



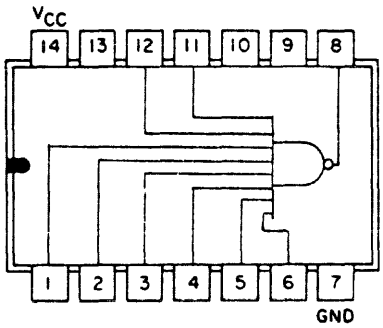
1447 3516
T2 2–INPUT NAND GATE
1479 0240
T2H 2–INPUT HIGH SPEED NAND GATE
1447 3581
T2C 2–INPUT NAND GATE OPEN COLLECTOR



1447 3540
T3 3–INPUT NAND GATE
1486 8780
T3H 3–INPUT HIGH SPEED NAND GATE



1447 3565
T4 4–INPUT NAND GATE
1479 0265
T4 4–INPUT HIGH SPEED NAND GATE

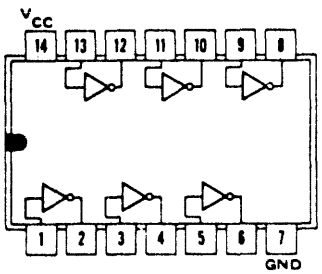


1447 3573
T8 8–INPUT NAND GATE

Fig. III-2 NAND GATES

T1 HEX INVERTER

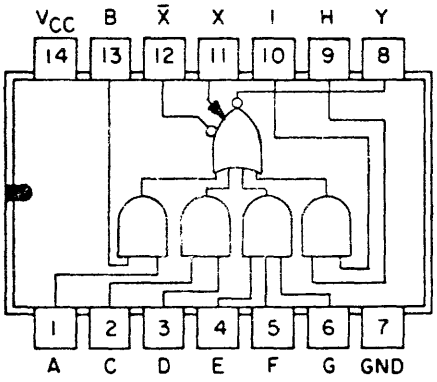
The Hex Inverter contains 6 inverter gates as shown in Fig. III-3. T1 is a standard inverter whereby a high level output is produced by a low level input and a low level output is produced by a high level input.



1447 3532
T1 HEX INVERTER

Fig. III-3

Circuit Detail



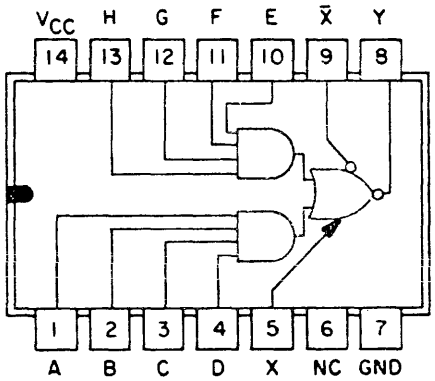


Fig. III-4 AND/OR INVERTER GATES

E24 2-2-2-3 INPUT AND/OR INVERTER GATE

The 2-2-2-3 Input And/Or Inverter Gate chip is shown in Fig. III-4. The function performed by this chip is specified by the following logical equation: Y = (AB)+(CD)+(EF)+(GHI). Refer to Fig. III-4.

A high level is required at all inputs of a AND gate to produce a low level output from this circuit. A low level at any of the AND gate inputs produce a low level output from this circuit.

E42 4-4 INPUT AND/OR INVERTER GATE

The 4-4 Input AND/OR Inverter Gate chip is shown in Fig. III-4. The function performed by this chip is specified by the following logical equation: Y = (ABCD)+(EFGH). Refer to Fig. III-4.

A high level is required at all inputs of a AND gate to produce a low level output from this circuit. A low level at any of the AND gate inputs produces a low level output from this circuit.

S2 QUAD 2- INPUT MULTIPLEXOR

The Quad 2-Input Multiplexor chips as shown in Fig. III-5, consists of four 2-Input Multiplexors with common input select logic, common active low enable, and active high output. It allows four bits of data to be switched in parallel to the appropriate output from the four 2-bit data sources. When the enable is not active, all the outputs are held at a low level. The functional logic and the truth table for this chip is shown in Fig. III-6.

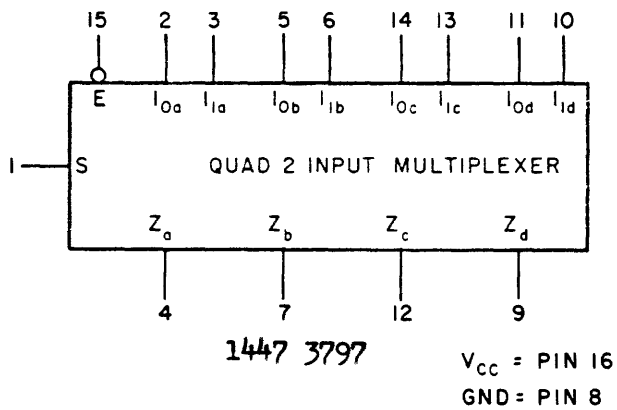
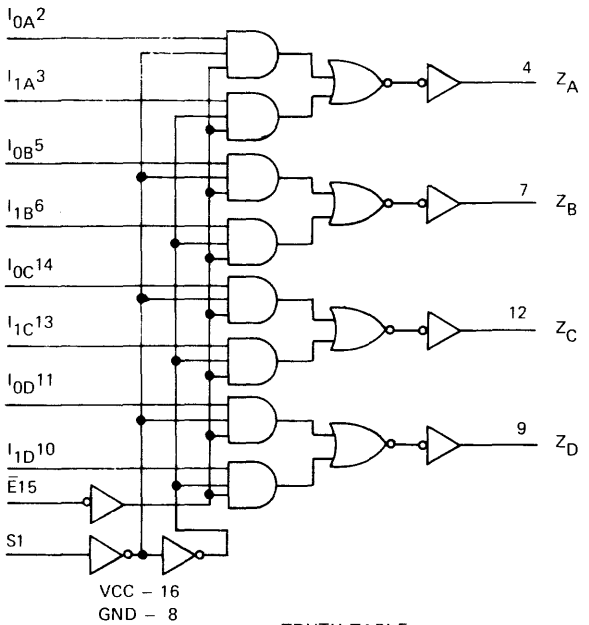


Fig. III-5 QUAD 2-INPUT MULTIPLEXOR



PIN NAMES

S	COMMON SELECT INPUT
$\bar{E}$	ENABLE (ACTIVE LOW) INPUT
MULTIPLEXERS A,B,C,D	
I_0,I_1	MULTIPLEXER INPUTS
Z	MULTIPLEXER OUTPUT

TRUTH TABLE

E	S	I_{0a}, I_{0b}, I_{0c}, I_{0d}	I_{1a}, I_{1b}, I_{1c}, I_{1d}	Z_a, Z_b, Z_c, Z_d
H	X	X	X	L
L	L	H	X	H
L	L	L	X	L
L	H	X	H	H
L	H	X	L	L

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE CONDITION

Fig. III-6 S2 QUAD 2-INPUT MULTIPLEXOR, FUNCTIONAL LOGIC AND TRUTH TABLE

SU FOUR-BIT SHIFT REGISTER

The Four-Bit Shift Register chip is shown in Fig. III-7. This chip is a synchronous four-bit shift register and performs such functions as storage and shifting. This register has assertion outputs on each stage. A negation output on the last stage, an overriding asynchronous master reset, JK input configuration, and a synchronous parallel load facility. Data entry is synchronous with the registers changing state after each low level to high level.

Transition of the clock pulse with the Parallel Enable input (PE) at a low level, the parallel inputs (P0,P1,P2,P3) determine the next condition of the shift register. When the Parallel Enable (PE) input is at a high level, the shift register performs a one bit shift to the right, with data entering the First Stage flip-flop through the JK inputs. When the two inputs (JK) are connected to each other, D type entry is obtained. When the asynchronous active low master reset is activated, all other input conditions are overridden and the register is cleared. The functional logic of this chip is shown in Fig. III-8.

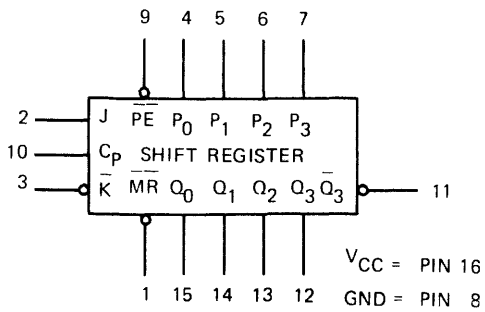
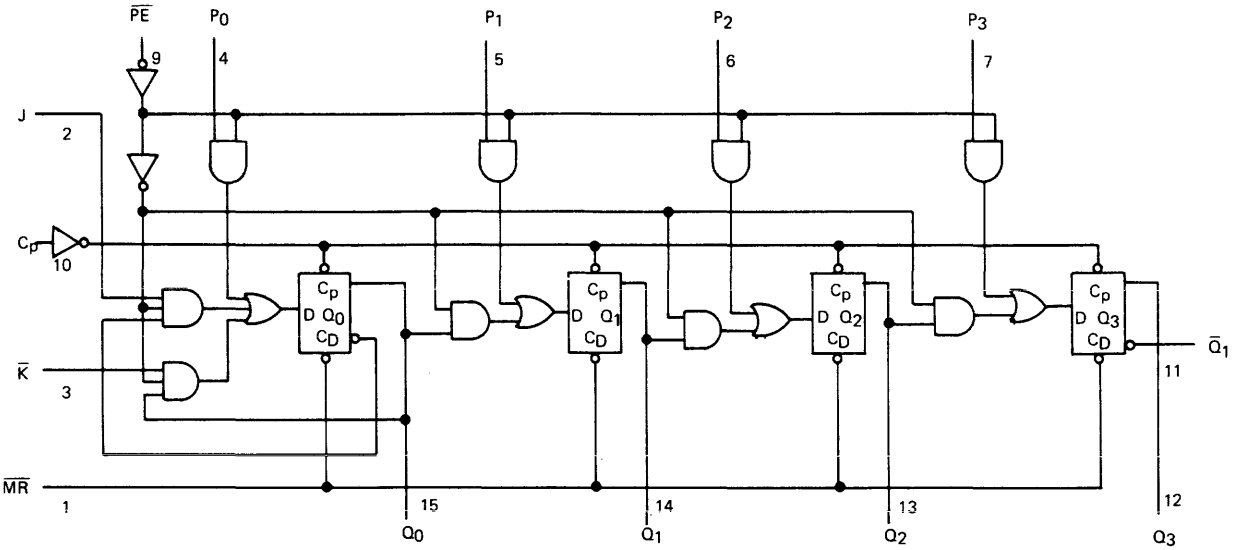


Fig. III-7 SU 4-BIT SHIFT REGISTER

Circuit Detail



J	K	Q_0 AT n + 1
L	L	L
L	H	Q_0 AT n (NO CHANGE)
H	L	Q_0 AT n (TOGGLES)
H	H	H

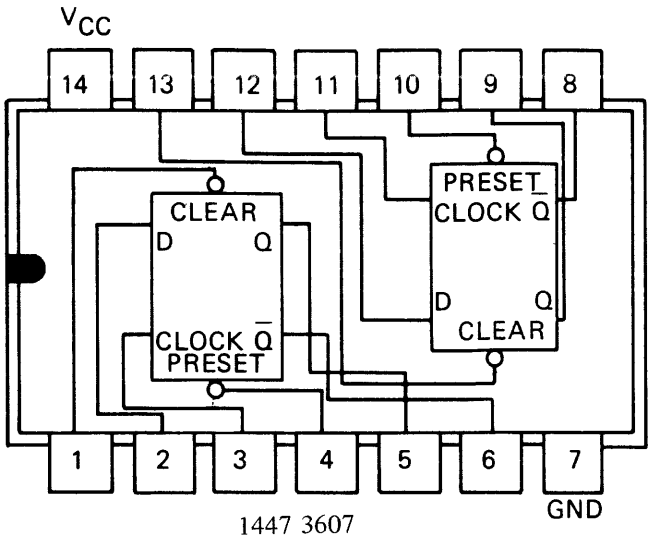
PE = HIGH, MR = HIGH,
(n + 1) INDICATES STATE
AFTER NEXT CLOCK

PE	PARALLEL ENABLE (ACTIVE LOW) INPUT
P_0,P_1,P_2,P_3	PARALLEL INPUTS
J	FIRST STAGE J (ACTIVE HIGH) INPUT
K	FIRST STAGE K (ACTIVE LOW) INPUT
C_p	CLOCK ACTIVE HIGH GOING EDGE INPUT
MR	MASTER RESET (ACTIVE LOW) INPUT
Q_0,Q_1,Q_2,Q_3	PARALLEL OUTPUTS
$\overline{Q}_3$	COMPLEMENTARY LAST STAGE OUTPUT

SU TRUTH TABLE

Fig. III-8 SU – 4-BIT SHIFT REGISTER – FUNCTIONAL LOGIC AND TRUTH TABLE

Circuit Detail



1447 3607

Fig. III-9 DF

TRUTH TABLE
(EACH FLIP-FLOP)

INPUT D	OUTPUT Q	OUTPUT $\bar{Q}$
0	0	1
1	1	0

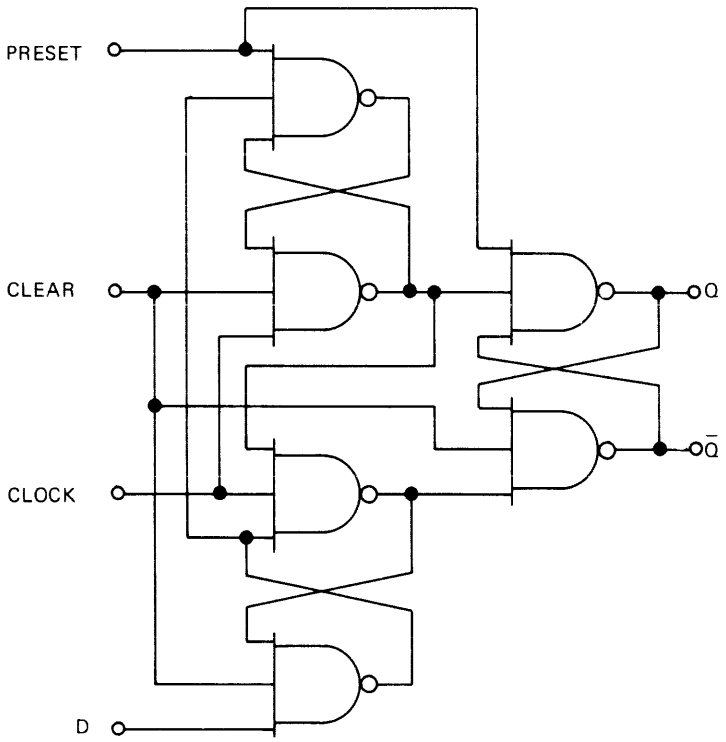
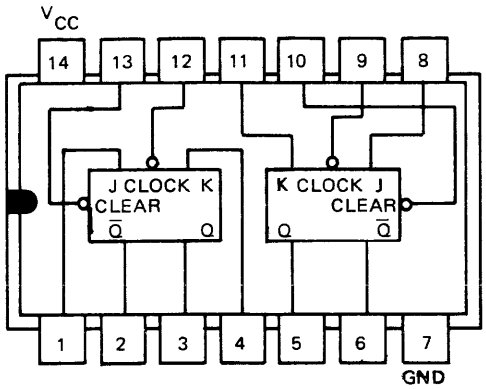


Fig. III-10 DF FUNCTIONAL LOGIC

DF DUAL D-TYPE EDGE TRIGGERED FLIP-FLOP

The DF Dual D Type Edge Triggered flip-flop chip, Fig. III-9 contains 2 flip-flops. The functional block diagram for each flip-flop is shown in Fig. III-10. These flip-flops have a direct clear and a preset inputs and complementary Q and Q outputs. Input information is transferred to the outputs on the positive edge of the clock pulse. A low level signal to the preset input sets Q to a logical 1 level. A low level signal to the clear input sets Q to a logical 0 level. The preset and clear inputs to each flip-flop are independent of the clock.

Circuit Detail



1447 3615

Fig. III-11 JF

TRUTH TABLE (EACH FLIP-FLOP)		
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

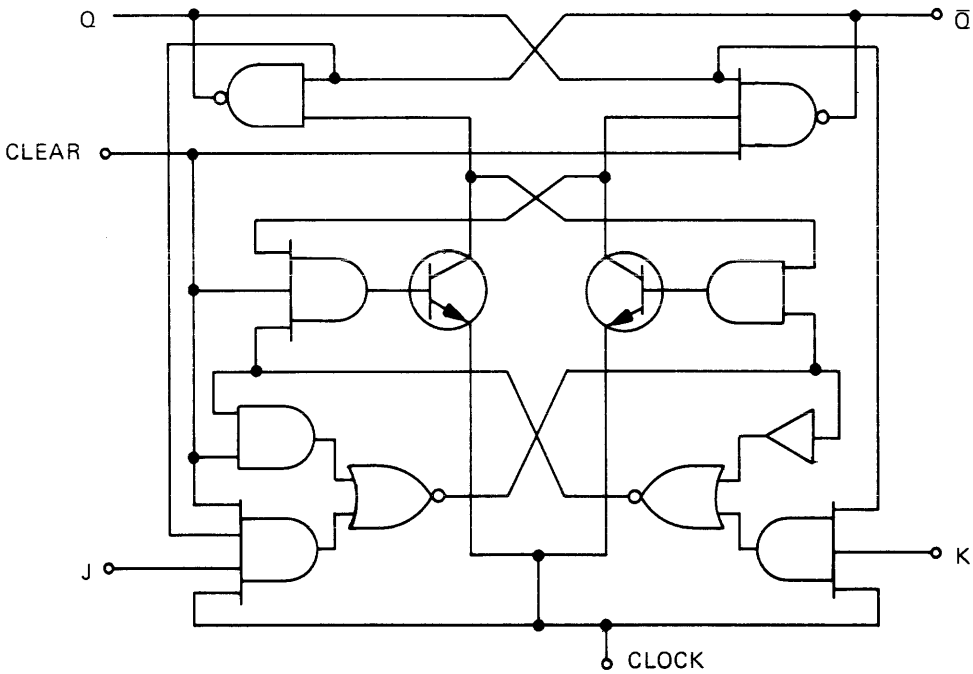


Fig. III-12 JF FUNCTIONAL LOGIC

JF DUAL J-K MASTER SLAVE FLIP-FLOP

The JF Dual J-K Master Slave flip-flop chip is shown in Fig. III-11. These J-K flip-flops are based on the master slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regualtes the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows.

1. Isolate slave from master.
2. Enter information from the J-K inputs to the master.
3. Disable J&K inputs.
4. Transfer information from master to slave.

A low level signal applied to the clear input sets Q output to a logical 0. The clear signal is independent of the clock. Refer to Fig. III-12 for the functional logic of this chip.

SS MONOSTABLE MULTIVIBRATOR CHIP

The SS Monostable Multivibrator chip and Truth Table are shown in Fig. III-13. The SS features D-C triggering from positive or gated negative going inputs with an inhibit facility provided. Both positive and negative going output pulses are provided with a full fan-out of up to 10 normalized loads.

Negative edge-triggered inputs at A1 and A2 allow the One-Shot Multivibrator to be triggered when either or both inputs are at a logical 0 level and the B input is at a logical 1 level. The B input is a Positive Schmitt-Trigger input, which allows jitter free triggering from inputs with slow transition times.

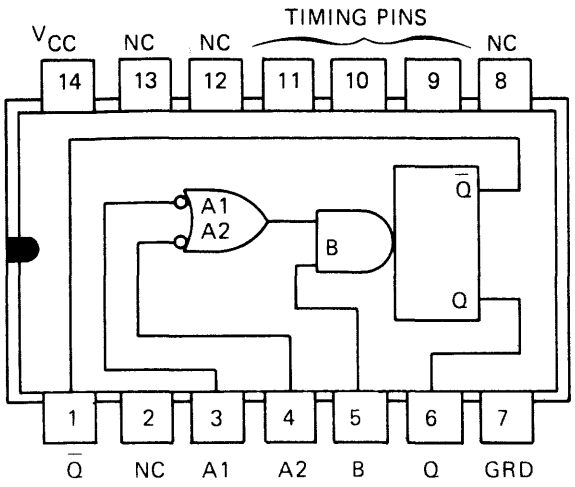
Whenever the B input is at a logical 1 level and both the A1 and A2 inputs are at a logical 1 level, the output is

Circuit Detail

TRUTH TABLE

INPUT			OUTPUT
A1	A2	B	
1	1	1	INHIBIT
0	X	0	INHIBIT
X	0	0	INHIBIT
0	X	1	ONE SHOT
X	0	1	ONE SHOT
X	0	1	ONE SHOT
0	X	1	ONE SHOT
X	1	0	INHIBIT
1	X	0	INHIBIT
1	1	1	INHIBIT
1	1	1	INHIBIT
X	0	0	INHIBIT
0	X	0	INHIBIT

NOTE: X INDICATES THAT EITHER A LOGICAL 0 OR 1 MAY BE PRESENT.



1447 3706

Fig. III-13 SS

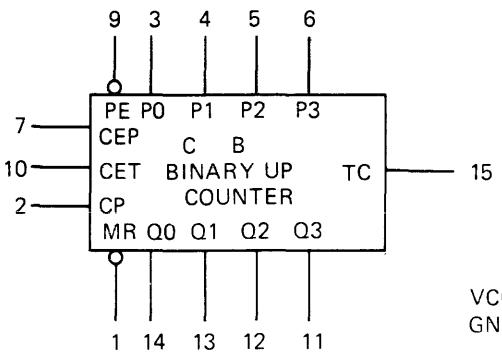
inhibited. The output is also inhibited whenever the B input is at a logical 0 level. Refer to Fig. III-13. Once the One-Shot Multivibrator is triggered, the output is independent of further transistions of the input fulse and relies only on the external timing component (RC netword) added to the circuit. The output pulse length may be varied from 40 nanoseconds to 40 seconds by selection of the appropriate timing components. With no external timing components added to the circuit, an output pulse of 30 nanoseconds can be obtained.

CB UP BINARY COUNTER

The CB Binary Counter chip is shown in Fig. III-14. This chip is a four bit synchronous binary up counter with synchronous parallel load facility, overriding asynchronous master reset, and carry lookahead logic for high speed multi-stage operation. This counter is synchronous with the counter ouput changing state after the low level to high level transition of the clock pulse. When conditions for counting are satisfied, a clock pulse will change the counter to the next state of the binary sequence. When the Parallel Enable (PE) input is a low level the parallel inputs determine the next state of the counter synchronously with the clock pulse. Mode selection is accomplished as shown in Fig. III-15. However, a restriction is placed on the manner of selection. The transition of signal CEP or CET from a high level to a low level or of signal PE from a low level to a high level may only be done when signal CP is a high level. By using the Two Count Enable inputs (CEP&CET) and Terminal Count (TC) output, multi-stage synchronous counting is obtained, with operating speeds equivalent to that of a single stage. When the synchronous master reset is active outputs Q0 through Q3 are unconditionally reset.

Circuit Detail

CIRCUIT DETAIL



PIN NAMES

$\overline{PE}$	PARALLEL ENABLE (ACTIVE LOW) INPUT
P0, P1, P2, P3	PARALLEL INPUTS
CEP	COUNT ENABLE PARALLEL INPUT
CET	COUNT ENABLE TRICKLE INPUT
CP	CLOCK (ACTIVE HIGH GOING EDGE) INPUT
$\overline{MR}$	MASTER RESET (ACTIVE LOW) INPUT
Q0, Q1, Q2, Q3	PARALLEL OUTPUTS
TC	TERMINAL COUNT OUTPUT

Fig. III-14 CB 1447 3771

PE	CE (COUNT ENABLE)	MODE
1	1	COUNT UP
1	0	NO CHANGE
0	X	PRESET

WHERE CE = CEP · CET 1 = HIGH VOLTAGE LEVEL
0 = LOW VOLTAGE LEVEL
X = DON'T CARE CONDITION

Fig. III-15 CB MODE SELECTION

MTR DIAGNOSTIC

The B489 IOC is maintained by running the Disk MTR. The Disk MTR is designed to diagnose problems in the IOC and point to possible problems in the drive. The disk MTR also provides all the necessary tests for disk drive adjustments.

The following tests are included in the disk MTR:

TEST 00 – Write all tracks and segments – drive 0, face 0
TEST 01 – Write all tracks and segments – drive 0, face 1
TEST 02 – Write all tracks and segments – drive 1, face 0
TEST 03 – Write all tracks and segments – drive 1, face 1
TEST 04 – Read all tracks and segments – drive 0, face 0
TEST 05 – Write all tracks and segments – drive 0, face 1
TEST 06 – Write all tracks and segments – drive 1, face 0
TEST 07 – Write all tracks and segments – drive 1, face 1
TEST 08 – Locate and verify test
TEST 09 – Service late and time out test
TEST 10 – Write inhibit for a 1 drive disk unit
TEST 11 – Write inhibit, postamble time test and rive compatibility test for a 2 drive disk unit.
TEST 12 – RPM time test – Top drive
TEST 13 – RPM time test – Bottom drive
TEST 14 – Detent addressing test – top dirve (runs for 8 mins.)
TEST 15 – Detent addressing test – bottom drive (runs for 8 mins.)

The following tests are for signal tracing:

TEST 16 – Seeks all tracks – drive 0
TEST 17 – Seeks all tracks – drive 1
TEST 18 – Loop on Write
TEST 19 – Loop on Read

The following tests are for F.E. Test and adjustments:

TEST 20 – Discriminator adjustment
TEST 21 – Loop on seek test
TEST 22 – Head alignment, drive 0, face 0
TEST 23 – Head alignment, drive 0, face 1
TEST 24 – Head alignment, drive 1, face 0
TEST 25 – Head alignment, drive 1, face 1
TEST 26 – Write current test, drive 0, face 0
TEST 27 – Write current test, drive 0, face 1
TEST 28 – Write current test, drive 1, face 0
TEST 29 – Write current test, drive 1, face 1
TEST 30 – Positioner timing, drive 0
TEST 31 – Positioner timing, drive 1
TEST 32 – Indicates to MTR that drive is double track density.

Tools required for diagnosing B489 IOC problems are:

a. MTR Meter
b. 453 Tektronix Oscilloscope
c. Extender kit (may be necessary).

NOTE: It should be noted that for proper diagnosis, all previous MTR's must be run without error.

INSTALLATION

The B0489 Disk DDP cards may be installed in any of the four-card interchangeable I/O ports (DDP's) of the processor unit. Refer to the B 700 Planning and Installation manual, form 1061223, and the B 700 Processor FETM, form 1064482, for card location and installation data. The four B0489 cards are identified as follows:

Designation	Part Number	Function
DC1	1447 4530	Control
DC2	1447 4498	Data 9-16
DC3	1447 4514	Data 1-8
DC4	1447 8507	Special

After the cards are installed, connect frontplane connectors (1534 3940) between DC1 and DC2, and between DC3 and DC4.

Connect cable 1446 6072 from the external disk unit to the corresponding DDP port I/O connector. Check +5 volt operating power as instructed in Section IV of FETM 1064482. Load and execute disk MTR to check operation of disk I/O subsystem.

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REMARKS FORM

TITLE: B 0489 DISK DDP
(FOR B 700 SYSTEMS)

FORM: 1061702
DATE: 3-25-75

CHECK TYPE OF SUGGESTION:

☐ ADDITION ☐ DELETION ☐ REVISION ☐ ERROR

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STAPLE

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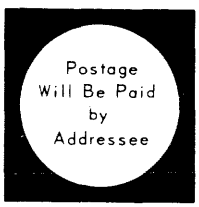

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