B 0346/B 0346-1
CONSOLE
I/O CONTROL
(B 700 SYSTEMS)

Burroughs

FIELD ENGINEERING

TECHNICAL
MANUAL

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INTRODUCTION

This Technical Manual covers the B0264 and B0264-1 Console I/O Controls (IOC's). The B0264 Console IOC services the B9343-XX Consoles with the 64-print character set; the B0264-1 Console IOC services the B9343-XX Consoles with the 94-print character set. Each IOC consists of 12 cards installed in dedicated ports (DDP's) of the B705/711-1 and B721 Processors. The logic cards are the same for all types, except that CC6E and CC7E cards are used in the B0264 IOC, and CC6EK and CC7EK cards are used in the B0264-1.

The B0264/B0264-1 Console I/O Control (IOC or DDP), hereinafter called the IOC, provides the interface between the B9343 Console equipped with an electronic keyboard and a B700 Central Processing Unit (processor). (See Figure I-1.) The IOC controls the transfer of information and commands between the processor and the console.

The IOC acts upon control words sent by the processor, performs specified operations, and upon completion of an operation, generates a status word containing the status and error information. The port select unit (PSU) of the processor controls the synchronization of the IOC interface with the processor.

PROCESSOR INTERFACE

Interface communications between the processor and the IOC are accomplished by word transfers over input and output data lines, and by various control lines as described below:

PROCESSOR-TO-IOC
a. Error Indicators (B711-1 only-EOIND1, EOIND2, EOIND4, EOERIND) (B721 only-CGHALT). When high, cause appropriate indicator to light.
b. Input Data Lines (LUMIRn/). When low, indicate a logical true at the appropriate bits.
c. Output Data Lines (EXTn/). When low, indicate a logical true at the appropriate bits.
d. Enable Status Line (PSENSTn/). When low, initiates the status word from IOC to the processor.
e. Clock Line (CDSCLKn). Provides system clock pulses from the processor.
f. Instruction Line (PSINSTn). When high, indicates that the data on the MIR lines is a control word.
g. Read Line (PSREADn/). When low, initiates a one-character data transfer from the IOC to the processor.
h. Write Line (PSWRITn/). When low, initiates a one-character data transfer from the processor to the IOC.
i. Clear Line (CGCLEARn). When high, clears all control flip-flops in the IOC.
j. Power On Clear (ACPONCL/). Resets motor-on and motor up-to-speed flip-flops.

IOC-TO-PROCESSOR
a. Status Interrupt (SINTn/). When low, indicates to the processor that the IOC has a status word for the processor.
b. Data Interrupt (DINTn/). When low, indicates to the processor that the IOC is ready for another data transfer operation.
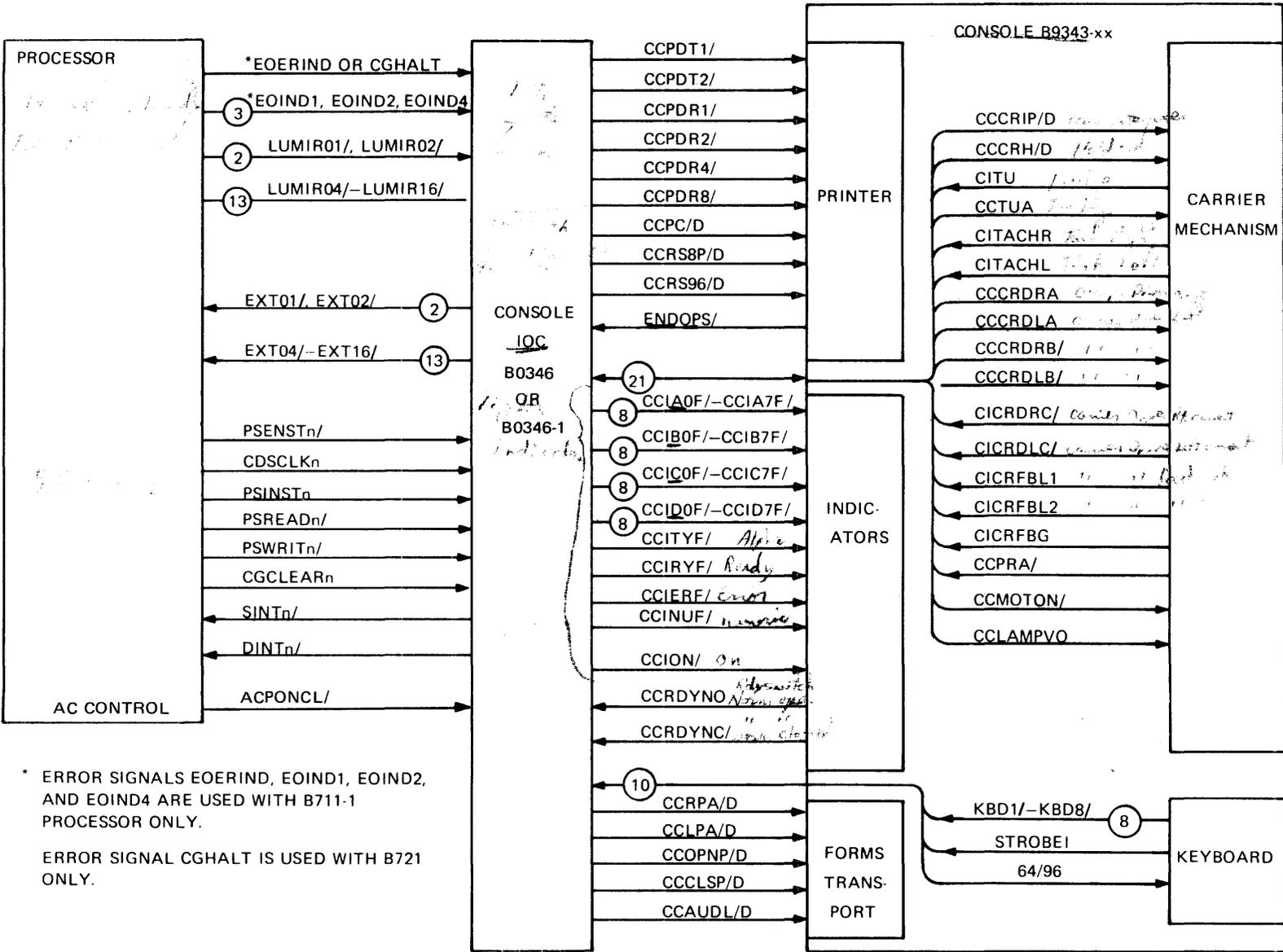
WORD FORMATS

The initiation of an information transfer between the processor and the IOC is the same for all devices, the distinction being in the device address contained in the base register (BR1 or BR2) of the processor output select gates. The port select unit decodes three bit groups from the processor to completely define the operation that is to take place. Nanobits 51 through 54 establish whether an operation is to be a device read or a device write. The four least significant bits of BR1 or BR2 contain the specific device address; the most significant bit of BR1/BR2, in conjunction with the type of operation, distinguishes between control, data, and status words. The word formats are illustrated in Figure I-2.

Control Word

Operation of the console is controlled by the transfer of a control word from the processor to the IOC. The control word consists of an operation field which specifies the function to be performed by the IOC as follows:

MIR Bits	Function
1 thru 11	Not used.
12	Enable Carrier Data Interrupt: a ONE in this bit enables data interrupts to the processor when the console is ready to accept carrier positioning data.
13	Enable Forms Data Interrupt: a ONE in this bit enables data interrupts to the processor when the console is ready to accept forms control data.
14	Enable Printer Data Interrupt: a ONE in this bit enables data interrupts to processor when console is ready to request print data.
15	Enable Keyboard Data Interrupt: a ONE in this bit enables data interrupts to processor when console is ready to transmit keyboard data.
16	Not used.

Fig. I-1. INTERFACE BLOCK DIAGRAM

CONSOLE B9343-xx

PROCESSOR

*EOERIND OR CGHALT
*EOIND1, EOIND2, EOIND4 ③
LUMIR01/, LUMIR02/ ②
LUMIR04/—LUMIR16/ ⑬

EXT01/, EXT02/ ②
EXT04/—EXT16/ ⑬

PSENSTn/
CDSCLKn
PSINSTn/
PSREADn/
PSWRITn/
CGCLEARn
SINTn/
DINTn/
ACPONCL/

AC CONTROL

CONSOLE
IOC
B0346
OR
B0346-1

CCPDT1/
CCPDT2/
CCPDR1/
CCPDR2/
CCPDR4/
CCPDR8/
CCPC/D
CCRS8P/D
CCRS96/D
ENDOPS/

PRINTER

CCIA0F/—CCIA7F/ ⑧
CCIB0F/—CCIB7F/ ⑧
CCIC0F/—CCIC7F/ ⑧
CCID0F/—CCID7F/ ⑧
CCITYF/
CCIRYF/
CCIERF/
CCINUF/
CCION/
CCRDYNO
CCRDYNC/

�21

INDIC-
ATORS

⑩
CCRPA/D
CCLPA/D
CCOPNP/D
CCCLSP/D
CCAUDL/D

FORMS
TRANS-
PORT

CCCRIP/D
CCCRH/D
CITU
CCTUA
CITACHR
CITACHL
CCCRDRA
CCCRDLA
CCCRDRB/
CCCRDLB/
CICRDRC/
CICRDLC/
CICRFBL1
CICRFBL2
CICRFBG
CCPRA/
CCMOTON/
CCLAMPVO

CARRIER
MECHANISM

KBD1/—KBD8/ ⑧
STROBEI
64/96

KEYBOARD

* ERROR SIGNALS EOERIND, EOIND1, EOIND2,
AND EOIND4 ARE USED WITH B711-1
PROCESSOR ONLY.

ERROR SIGNAL CGHALT IS USED WITH B721
ONLY.

| | MSB | | | | | | | | | | | | | | | LSB |
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
CONTROL WORD	–	–	–	–	–	–	–	–	–	–	–	ENABLE CARR DATA INTER	ENABLE FORMS DATA INTERRUPT	ENABLE FORMS DATA INTERRUPT	ENABLE FORMS DATA INTERRUPT	–
KEYBOARD DATA WORD				–	–			–	DATA 7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0
CARRIER DATA WORD	0	0	–	–	–	–	INITIALIZE	CARRIER DIRECTION	DATA 7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0
PRINT DATA WORD	0	1	–	–	ESCAPE RIGHT	ESCAPE LEFT	RED RIBBON	PRINT	–	DATA 6	DATA 5*	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0
INDICATOR DATA WORD	1	0	–	IND BANK ADDR A	IND BANK ADDR B	INDICATOR BANK ADDRESS C	INDICATOR BANK ADDRESS D	INDICATOR BANK ADDRESS S	DATA 7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0
FORMS DATA WORD	1	1	–	–	–	–	–	–	–	LEFT PLAT	–	RIGHT PLATEN	OPEN PLATEN	CLOSE PLATEN	POWER OFF	ALARM
STATUS WORD	DATA REQUEST	END OF PAPER	–	DEVICE ADDR 4	DEVICE ADDR 3	DEVICE ADDR 2	DEVICE ADDR 1	DEVICE ADDR 0	CARR RDY	FORMS READY	PRNTR READY	KYBD READY	READY PB	INTRPT NOT HONORED	OVER SPEED	STALL

NOTE: DEVICE ADDRESS BITS OF STATUS WORD ARE INSERTED AT PSU

* USED FOR 94-CHARACTER SET; NOT APPLICABLE TO 64-CHARACTER SET.

Fig. I-2 CONSOLE IOC WORD FORMATS

Keyboard Data Word

Keyboard data transfer between the IOC and the processor is in 8 bit parallel form, where bit 16 is the least-significant bit of the low-order digit and bit 12 is the least-significant bit of the high-order digit. The functions are as follows:

EXT Bits	Function
1 thru 8	Not used.
9 thru 12	Data: High-order digit portion of 8-bit byte of data from keyboard to processor.
13 thru 16	Data: Low-order digit portion of 8-bit byte of data from keyboard to processor.

Carrier Data Word

Carrier data transfer between the processor and the IOC determines the horizontal direction of movement of the print ball and the number of horizontal positions which the print ball is to be moved. The assigned bit positions are as follows:

MIR Bits	Function
1 and 2	Control Select: Defines console function. Code 00 selects carrier control.
3 thru 6	Not used.
7	Initialize: a ONE in this bit position causes a routine to be performed which moves the carrier to the extreme left or right, as determined by bit 8.
8	Carrier Direction: Defines horizontal direction of printer ball. A ONE specifies movement to left and a ZERO specifies movement to right.
9 thru 16	Data: Defines number of horizontal positions which the printer ball is to be moved from its present position.

Print Data Word

Print data transfer between the processor and the IOC defines the carrier escape, selects red or black ribbon, and the tilt and rotate position of the print ball. The functions are as follows:

MIR Bits	Function
1 and 2	Control Select: Defines console function. Code 01 selects system printer.
3 and 4	Not used.
5 and 6	Escape: Determines that carrier positioning is to be left (01), right (10), or no escape (00). The printer escapes first, then prints.

7	Each ribbon: A ONE in this bit shifts the ribbon mechanism to red ribbon, otherwise black ribbon is used.
8	Print: a ONE in this bit causes the character defined by bits 9 through 16 to be printed following escapement specified in bits 5 and 6. Otherwise escapement takes place but no printing occurs. Since there is no space position on the 64-character print ball, a space is printed by suppression of print bit plus appropriate escape bit; bit 7 is zero and data bits equal zero to avoid ribbon or print ball movement at this time.
9	Not used.
10 thru 16	Data: Defines tilt and rotate positions of print ball. For the 64-character set the code conversion is as follows:

Bit	Print Ball
10	Rotate 8
12	Rotate 4 NOT (negated value)
13	Tilt 2
14	Tilt 1
15	Rotate 2
16	Rotate 1

For the 96-character set the code conversion is as follows:

Bit	Print Ball
10	Tilt 2
11	Rotate code expansion
12	Tilt 1
13	Rotate 8
14	Rotate 4
15	Rotate 2
16	Rotate 1

Indicator Data Word

Indicator data transfer between the processor and the IOC specifies the indicator bank and the particular indicator to be lit. The bit assignments are as follows:

MIR Bits	Function
1 and 2	Control Select: Defines console function. Code 10 selects indicator control.
3	Not used.
4	Indicator bank address A.
5	Indicator bank address B.
6	Indicator bank address C.
7	Indicator bank address D.
8	Indicator bank address S.
9 thru 16	Data: Specifies the direct code to a particular bank of indicators on the console panel. An indicator is lit on receipt of a data word with a ONE in the appropriate data bit position. This indicator remains lit until receipt of a new data word for the same bank and a ZERO in the data bit position, or unless it is extinguished by system clear.

Forms Data Word

Forms data transfer between the processor and the IOC controls platen operation, system power, and console audible alarm. The functions are as follows:

MIR Bits	Function
1 and 2	Control Select: Defines console function. Code 11 selects forms control.
3 thru 9	Not used.
10	Left Platen: A ONE in this bit causes the left platen to be advanced one line.
11	Not used.
12	Right Platen: A ONE in this bit causes the right platen to be advanced one line.
13	Open Platen: A ONE in this bit causes the forms control chute to open.
14	Close Platen: A ONE in this bit causes the forms control chute to close.
15	Power Off: A ONE in this bit turns off system power.
16	Alarm: A ONE in this bit activates the audible alarm.

Status Word

Status word transfer between the IOC and the processor notifies the processor that a failure or particular functional condition has occurred. It consists of a device address (inserted at the port select unit) and a device status field. The functions are as follows:

EXT Bits	Function
1	Data Request: IOC is ready to receive or send a data character. This status condition follows the data interrupt to the processor.
2	End of Paper: Paper on either or both platens has been exhausted.
3	Not used.
4 thru 8	Device Address: Device address bits are inserted at the port select unit.
9	Carrier Ready: Carrier buffer is ready for next data word; a ONE whenever carrier data interrupt is true.
10	Forms Ready: Forms buffer is ready for next data word; a ONE whenever forms data interrupt is true.
11	Printer Ready: Print buffer is ready for next data word; a ONE whenever printer data interrupt is true.
12	Keyboard Ready: Keyboard character is available for transfer to processor; a ONE whenever keyboard data interrupt is true.
13	Ready: Ready pushbutton has been pressed and console is ready for operation.
14	Interrupt Not Honored: Processor did not service data interrupt. A ONE bit when a key is pressed and keyboard data has not been shifted from the first stage of the output buffer.
15	Overspeed: Carrier is moving too fast. A ONE in this bit after carrier data word is received and an overspeed condition is detected.
16	Stall: Carrier is moving too slow. A ONE in this bit after carrier data word is received and a stall condition is detected.

CONSOLE INTERFACE

The console is comprised of five functional sections: the printer, indicators, forms transport, carrier mechanism, and the keyboard sections. Each section is controlled by a respective part of the IOC.

Print data from the IOC provides the mechanical positioning of the print head. The carrier position operation is interleaved with the print function. The firmware of the

processor maintains records of print ball locations and vertical positioning of the forms.

The indicators are divided into five banks: A, B, C, D, and S, plus a power-on indicator. The power-on indicator is lit when power is on at the processor; the remaining indicators are controlled by processor firmware.

The keyboard is used for data entry and for program control. The console interface is illustrated in Figure I-1; the signals are described under the following headings:

IOC TO CONSOLE
a. Print Decode Tilt (CCPDT1/, CCPDT2/). Two lines which determine the proper tilt position of the print head.
b. Print Decode Rotate (CCPDR1/, CCPDR2/, CCPDR4/, CCPDR8/). Four lines which determine the proper rotate position of the print head.
c. Print Clutch Driver (CCPC/D). Activates hammer fire solenoid and causes print ball to impact paper.
d. Ribbon Shift or Rotate-8P (CCRS8P/D). For 64-character printers, a low causes ribbon solenoid to shift to red ribbon. For 96-character printers, provides for expansion of the rotate code for the print head.
e. Ribbon Shift, 96-Character Printers (CCRS96/D). For 96-character printers, a low causes ribbon solenoid to shift to red ribbon.
f. Indicator Group A (CCIA0F/ to CCIA7F/). A low on any line in this group causes the corresponding indicator to light.
g. Indicator Group B (CCIB0F/ to CCIB7F/). A low on any line in this group causes the corresponding indicator to light.
h. Indicator Group C (CCIC0F/ to CCIC7F/). A low on any line in this group causes the corresponding indicator to light.
i. Indicator Group D (CCID0F/ to CCID7F/). A low on any line in this group causes the corresponding indicator of the left-most group of eight indicators to light.
j. Indicator Group S (CCITYF/, CCIRYF/, CCIERF/, CCINUF/). A low on any line in this group causes the ALPHA, READY, ERROR, or NUMERIC indicator to light.
k. Audible Alarm (CCAUDL/D). When low, activates the audible alarm solenoid and causes the alarm to sound.
l. Power On (CCION/). Always low (ground).
m. Right Platen Advance (CCRPA/). When low, activates right platen solenoid and causes left platen to advance.
n. Left Platen Advance (CCLPA/). When low, activates left platen solenoid and causes the left platen to advance.

o. Open Platen (CCOPNP/D). When low, activates open platen solenoid and causes the forms control chute to open.
p. Close Platen (CCCLSP/D). When low, activates close platen solenoid and causes the forms control chute to close.
q. Carrier Interposer (CCCRIP/D). When low, activates carrier interposer solenoid and causes the carrier detent latches to be driven away from the shaft-locking device.
r. Carrier Hold (CCCRH/D). When low, activates carrier hold solenoids and causes the carrier detent locking latches to be held away from the detent gears.
s. Timer Unit Input (CCTUA). Signal console to test timer unit (TU).
t. Carrier Drive Controls (CCCRDRA, CCCRDLA, CCCRDRB/, CCCRDLB/). Amplifier and bias signals providing drive controls to the carrier motor.
u. Motor-On Signal (CCMOTON/). When low, causes the decoder motor to be turned on.
v. Carrier Position Read-Out Lamp Voltage (CCLAMPVO). Supplies a current-limited voltage to carrier position read out lamp source.
w. 64/96 Character Mode (64/96). Allows 64- or 96-character mode to be selected.

CONSOLE TO IOC
a. End of Paper (ENDOPS/). When low during forms function, enables end of paper bit in status word to IOC.
b. Ready Switch, Normally-Open Contacts (CCRDYNO). When ready switch is pressed, CCRDYNO is 0 volts.
c. Ready Switch, Normally-closed contacts (CCRDYNC/). When ready switch is pressed, CCRDYNC/ is +5 volts.
d. Timer Unit (CITU). Core readout from rotating shaft of decoder motor, synchronizes mechanical timing in all functions.
e. Tachometer Right (CITACHR). When high, tachometer right output is monitored.
f. Tachometer Left (CITACHL). When high, tachometer left output is monitored.
g. Carrier Drive Controls (CICRDRC/, CICRDLC/, CICRFBL1, CICRFBL2, CRFBG). Signals sent from carrier control to carrier drive circuits for generation of control signals to the carrier motor.
h. Carrier Position Readout (CCCPR/A). Signal from Carrier photocell used to count position of carrier.

i. Keyboard Data (KBD1/ to KBD8/). When low, indicates a binary ONE bit at appropriate bit position.

j. Keyboard Strobe (STROBEI). Indicates to IOC that keyboard data lines contain a character.

GLOSSARY OF TERMS AND SIGNALS

The following is a list of the mnemonics and names of signals used in the console IOC:

Signal	Meaning
ACPONCL/	Power-on clear
CCAUDAL/	Audible alarm
CCAUDAL/D	Audible alarm signal driver
CCCARR	Carrier, indicates presence of a carrier data word on MIR lines.
CCCLR/	Clear
CCCLSP/	Close platen
CCCL+NP	Clear or not print
CCCOUNT/	Count signal used to count down the carrier position data as the carrier moves
CCCPR	Carrier position readout
CCCRDI/	Carrier data interrupt
CCCRDLA	Carrier drive left amplifier
CCCRDLB/	Carrier drive left bias
CCCRDRA	Carrier drive right amplifier
CCCRDRB/	Carrier drive right bias
CCCRGL/	Carrier go left
CCCRGR/	Carrier go right
CCCRHS/	Carrier high speed
CCCRH/	Carrier hold
CCCRH/D	Carrier hold solenoid driver
CCCRLT/	Carrier left time
CCCR4A/	Carrier 4 amperes
CCCS	Core Strobe
CCDINT	Data interrupt
CCDMIRn	Memory information register bit n redeveloped through inverter.
CCDREAD/	Data read
CCD125/	Delay 125 (used to disable CCCOUNT signal for 12.5 milliseconds)
CCEKDI/	Enable keyboard data interrupt
CCENSTA	Enable status

Signal	Meaning
CCEQ1	Equal to 1 (output from carrier buffer)
CCFRMS	Forms
CCIAnF/	Group A indicator n
CCIBnF/	Group B indicator n
CCICnF/	Group C indicator n
CCIDnF	Group D indicator n
CCIERF/	Error indicator
CCIMSK/	One Mask, (disables EQ1 for 10 milliseconds, and sets LSLPF for a carrier movement of one position)
CCINITF	Initialize flip-flop
CCINTU/	Interposer and TUF
CCION/	On indicator
CCIRYF/	Indicator ready
CCITYF/	Indicator alpha
CCINUF/	Indicator numeric
CCIW	Instruction write
CCKBF	Keyboard enable flip-flop
CCKINH/	Keyboard interrupt not honored
CCKDI	Keyboard data interrupt
CCKSTA/	Keyboard status
CCLAMPVO	Carrier position lamp voltage
CCLPA/	Left platen advance
CCLPA/D	Left platen advance driver
CCLSP/	Close forms control chute
CCLSP/D	Close forms control chute solenoid driver
CCLTEQ6	Less than or equal to 6, output from carrier buffer
CCMCTU/	Mechanical timing signal
CCMOTON	Motor on
CCNOOPT/	No option
CCOCARR	Operate carrier (signal true when a carrier data word is not equal to zero)
CCOPNP/	Open platen
CCOPNP/D	Open platen driver
CCPCLR	CCCL+NP
CCPC/	Print clutch
CCPC/D	Print clutch driver
CCPDRn/	Print rotate n driver
CCPDTn/	Print tilt n driver
CCPRA/	Carrier position readout

Signal	Meaning	Signal	Meaning
CCPRF	Printer flip-flop	CICRDRC/	Carrier drive right current
CCPRI	Printer interposer	CICRFBG	Carrier feedback ground.
CCPRNT	Print (decoded from MIR data)	CICRFBL1	Carrier feedback level one
CCPRRN/	Printer rotate n	CICRFBL2	Carrier feedback level two
CCPRTn/	Printer Tilt n	CITACHBK	Tachometer feedback
CCPWRO/	Programmatic power off	CITACHL	Tachometer left
CCRDY	Ready pushbutton	CITACHR	Tachometer right
CCRDYNC/	Ready switch normally-closed	CLEAR	Clear
CCRDYNO	Ready switch normally-open	CROP1F	Carrier operation #1 flip-flop
CCRENST/	Enable status	DINTn/	Data interrupt
CCRIP/	Carrier interposer, signal used to drive the interposer solenoid	ENDOPS/	End of paper signal
		EOERIND	B711-1 only, error indicator signal
CCRIP/D	Carrier interposer driver	EOIND1, 2, 4	B711-1 only, hard error indicators
CROP1F	Carrier operation #1 flip-flop	EXTn	External bus bit n
CCRPA/	Right platen advance	FMPR	Forms or print data
CCRPA/D	Right platen advance driver	F+PDATA	Forms or print data
CCRS96/	96-character ribbon shift	HOLD	Hold
CCRS96/D	96-character ribbon shift driver	IND1, 2, 4	Memory parity indicator
CCRS+8P/	Ribbon shift for 64 character printer or expansion of rotate code to 96 characters.	KBDn/	Keyboard data n
		PRTU	Printer timer unit
CCRS8P/D	CCRS+8P/ driver	PSENSTn/	Enable status
CCTU	Timer unit signal	PSINSTn	Port select instruction
CCTUA	Input signal to decoder transducer	PSREADn/	Port select read
CCTUF-1	Timer unit flip-flop	PSWRITn/	Port select write
CCXCRGL/	Escape carrier, go left	SCLK	Clock signal
CCXCRGR/	Escape carrier, go right	SINTn	Status interrupt
CCXCR4A/	Escape carrier 4 amperes	STALF	Stall flip-flop
CCZERO/	Signal indicates that the data on the MIR lines is not equal to zero	STROBEI	Keyboard strobe
		TU	Timer unit
CDSCLKC,D,n	Clock signals.	TUF	Timer unit flip-flop
CGCLEARn	System clear		
CGHALT	Error indicator signal (B721 only)	64/96	64- or 96-character mode
CICRDLC/	Carrier drive left current		

GENERAL OPERATION

As shown in Figure I-1, there are five major functional sections in the console; the logic in the IOC is divided into corresponding sections. Because of its complexity, the console IOC is located in a dedicated DDP area of the processor (B711-1 port 8 and B721 port 12).

The five logic sections of the IOC are as follows:

a. Keyboard Control.
b. Indicator Control.
c. Printer Control.
d. Carrier Mechanism Control.
e. Forms Transport Control.

Communications between the processor and the IOC is accomplished by means of control words, data words, and status words. The formats of the various words are shown in Figure I-2.

To enable any of the console mechanisms, the processor must send a control word with the appropriate bit set (MIR12, 13, 14, or 15). This enables the logic associated with a particular mechanism to generate a data interrupt when the logic is ready to send or receive a data word. The only exception is the indicator control logic, which neither requires a control word nor generates an interrupt. A data word may be addressed to the indicators at any time and will be acted upon.

The status word is send to the processor when a device-read to the console is executed with the instruction bit (most-significant bit in the active base register) set, or when the processor executes an Address and Status Request (ASR) and the console IOC is the highest priority IOC generating a status interrupt.

The four status-word bits associated with a data interrupt are EXT9, 10, 11 and 12. EXT13, 14, 15 and 16 are the bits associated with a status interrupt.

BASIC TIMING

The processor provides the IOC with clock pulses (CDSCLKn) at a rate of 1 MHz. This clock signal is redeveloped, distributed, and used for various operations between the IOC and processor.

To synchronize logic functions of the IOC with mechanical sections of the console, a timer unit signal (CITU) is generated by a transducer core readout from a rotating shaft in the console. A timing pulse TUA is generated once every 300 microseconds.

To strobe the transducer operation, signal CCCS is generated by three single-shot devices and a JK flip-flop (Figure II-1). This circuit produces a 10-microsecond pulse every 300 microseconds which is routed to the transducer core driver circuit. If the flag on the rotating shaft is not between the transducer and its associated magnet, then the field of the magnet saturates the transducer core so that it exhibits a low inductive impedance. Thus, when CCCS is applied to the circuit, the output of the transducer goes low. If a flag is present, it provides a shunt path for the magnetic field, the transducer core exhibits a high inductive impedance and, when CCCS is applied to the circuit, the output of the transducer remains high (Figure II-2). With CITU high, the timer unit input flip-flop (TUINF) remains in the set condition.

KEYBOARD CONTROL

To enable data to be read from the console keyboard, the processor must send a control word with MIR15 bit set, to the console to enable the keyboard strobe circuit. However, when the system is initially turned on, or if the halt and clear pushbutton is used, the keyboard strobe circuit is automatically enabled.

The keyboard control circuit is shown in Figure II-3. The receipt of a write signal (PSWRITn/ is low) and an instruction signal (PSINSTn is high) from the processor produces signal CCIW. CCIW is gated with the system clock to generate IWCLK/. With CCDMIR15 high, keyboard enable flip-flop KBF is set. Whenever the clear signal (CCCLR/) is present, the keyboard enable flip-flop is direct-set.

KEYBOARD BUFFER

A three-character first-in, first-out buffer is dedicated to keyboard operation. When any key is pressed, the keyboard ready status bit is set and a data interrupt signal is sent to the processor if the keyboard is enabled.

The shift clock pulses SC1/, SC2/, and SC3/ are used to clock keyboard data through the three stages of the keyboard buffer (Figure II-4). The keyboard buffer is comprised of six quad D-type flip-flop IC's (Figure II-5).

Initially, SC1F and SC2F flip-flops are reset by the system clear signal. When a key is pressed, the keyboard data (KBD1 through KBD8) is applied to the first stage of the buffer. Pressing a key also generates the keyboard strobe signal STROBEI. Signal STROBEI is gated with CCKBF. The resulting signal is inverted and gated with the $\overline{Q}$ side of flip-flop SC1F which produces SC1J. Signal SC1J is inverted to produce clock pulse SC1/ and is also fed back to set flip-flop SC1F. Input data from the first stage of the buffer is transferred to its output and to the input of the second stage on the positive edge of signal SC1/.

The output of the Q-side of flip-flop SC1F is gated with the $\overline{Q}$ side of flip-flop SC2F to set flip-flop SC2F, reset flip-flop SC1F, and generate an SC2/ pulse. On the positive edge of SC2/ the input data at the second stage is transferred to the input of the third stage.

The presence of signal CCDREAD/ (a read signal is present without an instruction signal) with flip-flop SC2F set, produces clock pulse SC3/. On the positive edge of pulse SC3/ the input data on the third stage of the keyboard buffer is applied to the MIR lines to the processor.
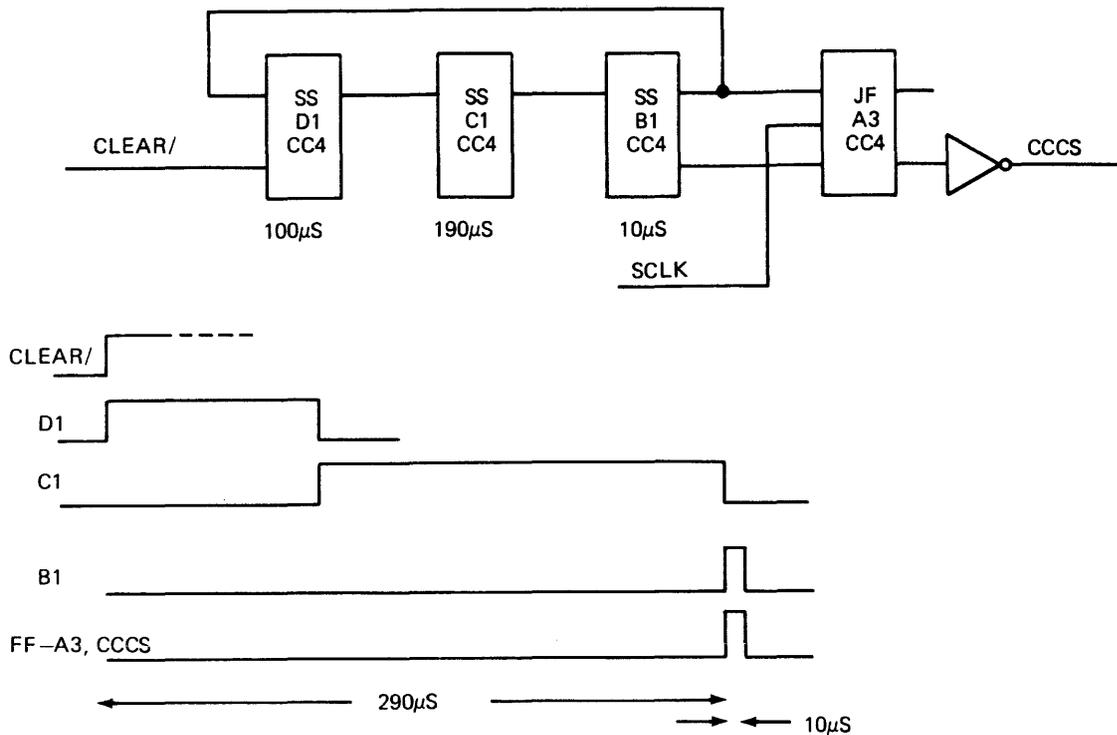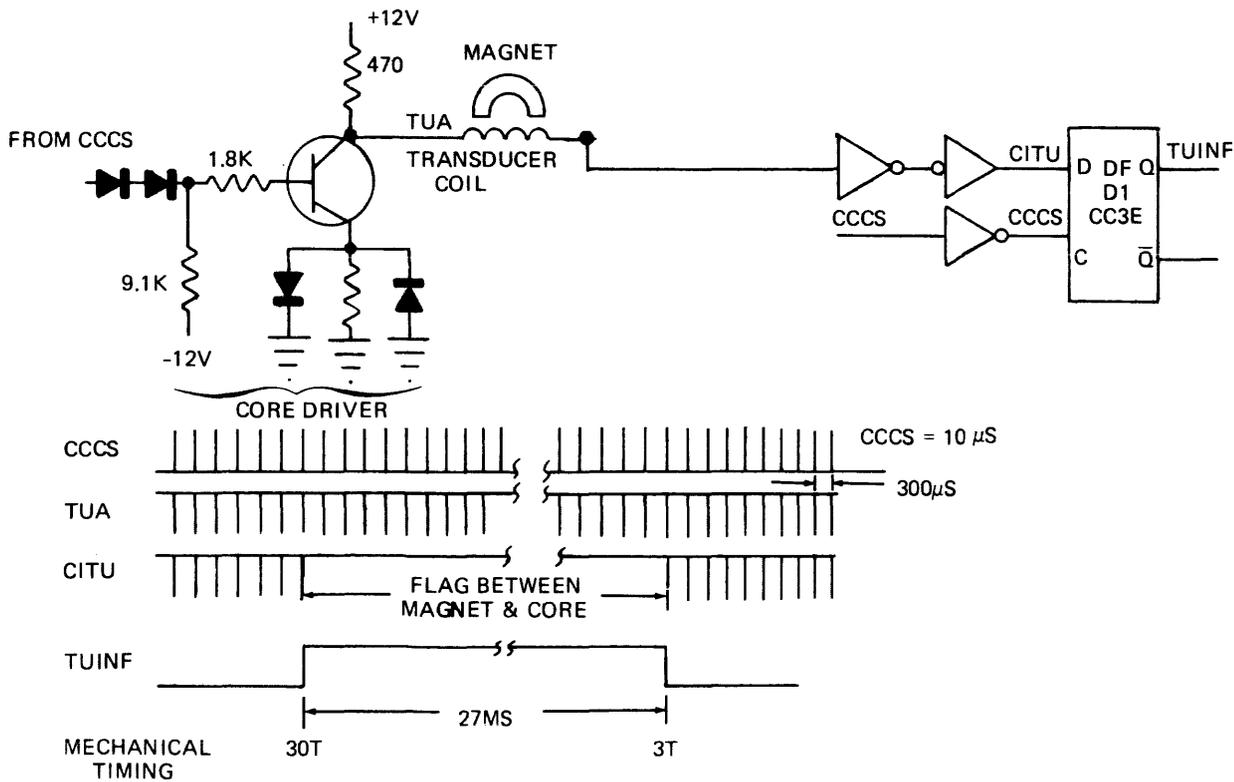
Functional Detail

Fig. II-1. CCCS GENERATION AND TIMING

Fig. II-2 TUINF GENERATION AND TIMING

Functional Detail

Fig. II-3 KEYBOARD ENABLE CIRCUIT

Fig. II-4 KEYBOARD BUFFER SHIFT CLOCK AND INTERRUPT NOT HONORED

INTERRUPT NOT HONORED

The interrupt-not-honored status is generated when a key is pressed before a keyboard character has been shifted from the first stage of the keyboard buffer. This condition results in a lost keyboard character. When the processor is notified of this condition, it enters an error routine to notify the operator that the condition must be corrected.

The shift clock pulse SC1/ is generated by the Q output of flip-flop SC1F and the keyboard strobe (STROBEI). Signal SC1 sets the SC1F flip-flop (Figure II-4), whose output generates SC2/ and also causes SC1F to be reset. If a STROBEI pulse is received before SC1F is reset, the interrupt-not-honored (CCKINH/) signal is generated, indicating that a character is still present in the first buffer stage. Signal CCKINH/ sets the INH flip-flop (Figure II-6), which sends a status interrupt to the processor (CCKSTA) and sets the interrupt-not-honored bit (EXT14/) in the status word.

Functional Detail

INDICATOR CONTROL

The indicators provide a visual indication to the console operator of machine and program status and of required keyboard entries. The indicators are lit by the generation of an indicator data word by the processor firmware; data interrupts are not involved in this implementation.
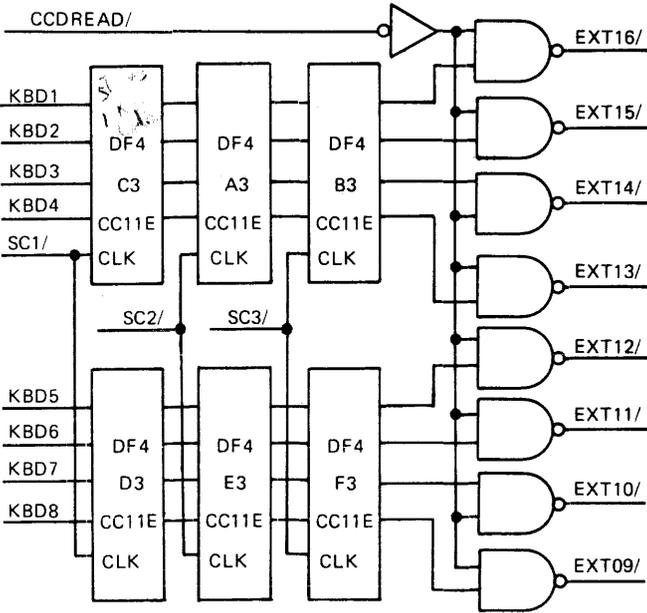
Fig. II-5 KEYBOARD BUFFER OUTPUT
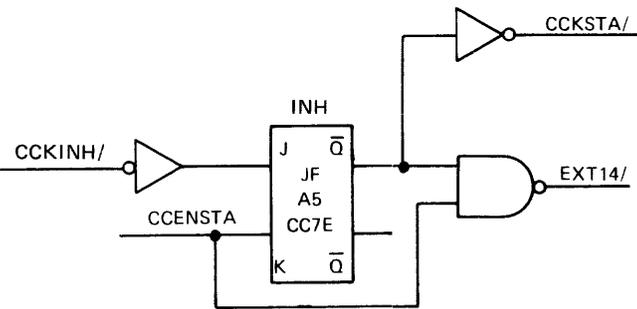
Fig. II-6 INTERRUPT NOT HONORED

Eight bits of the data word (Figure II-7) contain the code to be used by one of four banks (A, B, C, and D) of eight indicators and one bank (S) of four indicators.

Indicator data bits MIR9 through MIR16 are applied to shift registers (SU IC's) which are used as data buffers (Figure II-8). The data are clocked to the indicator drive circuits by the appropriate group select bit (MIR4 through MIR8). Note that indicators D1 through D4 have alternate inputs. These alternate inputs are routed from the external

operation (EO) control logic of the processor and are used to display hardware errors (B711-1 only).

PRINTER CONTROL

The printing element on the system is a moveable ball printer head with either a 64-character set or a 94-character set. Processor internal ASCII codes are translated into tilt and rotate positions of the printer head by the IOC. The IOC provides controls to cause the printer to escape right or left and print, to escape right or left, or to print in place.

To enable the printer data interrupt, the processor must send a control word with bit 14 enabled (MIR14) to the IOC. Provided that any previously indexed carrier operation is complete, the IOC returns printer data interrupt (PDI) to the processor. When the processor receives the data interrupt, it can then execute a device-write to send the data word to the IOC. The printer logic disables the data interrupt until the character has been transmitted to the mechanical sections of the printer. The format of the printer data words is illustrated in Figures II-9 and II-10 for the 64-character and 94-character sets, respectively.

The following printer description covers only those functions controlled by the printer section. The carrier escape-right, carrier escape-left, and carrier remain-in-place functions are covered in the description of the carrier control logic.

PRINTER DATA INTERRUPT

When a device-write to the console is executed with the instruction bit set, a low instruction write clock (IWCLK/) signal is generated as shown in Figure II-11. With the enable keyboard data interrupt bit of the control word (MIR14 is high) set and with IWCLK/ low, the print flip-flop is set (Figure II-12). PRF is then gated with TUF-1 and CCROP1F/ to produce signal PRENF. A high CCROP1F/ indicates that any previous carrier operation has been completed.

Signal PRENF produces a low CCCL+NP which makes RCLR/ high. With RCLR/ high, the printer forms data register (Figures II-14 and II-15) can be loaded. At the same time, PRENF is gated with the reset side of the DF flip-flop to produce a low SETPDI/. One clock time later, the DF flip-flop is set so that SETPDI/ is false for 1 microsecond.

As shown in Figure II-13, a low SETPDI/ sets the PDI flip-flop, the output of which is gated with PRENF and PRF to produce a low PDI/ (print data interrupt). This causes a data interrupt to be sent to the processor. When PDI/ goes low, it resets the ENPRTU flip-flop to disable the printer timer unit (PRTU) circuit.

PRINTER DATA WORD

When the data interrupt is received by the processor, the processor may execute a device-write with the instruction bit enabled to indicate that the data on the MIR lines

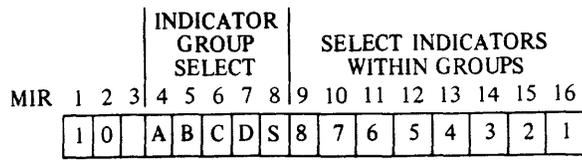| MIR	1	2	3	INDICATOR GROUP SELECT 4	5	6	7	8	SELECT INDICATORS WITHIN GROUPS 9	10	11	12	13	14	15	16
	1	0		A	B	C	D	S	8	7	6	5	4	3	2	1

Fig. II-7 INDICATOR DATA WORD
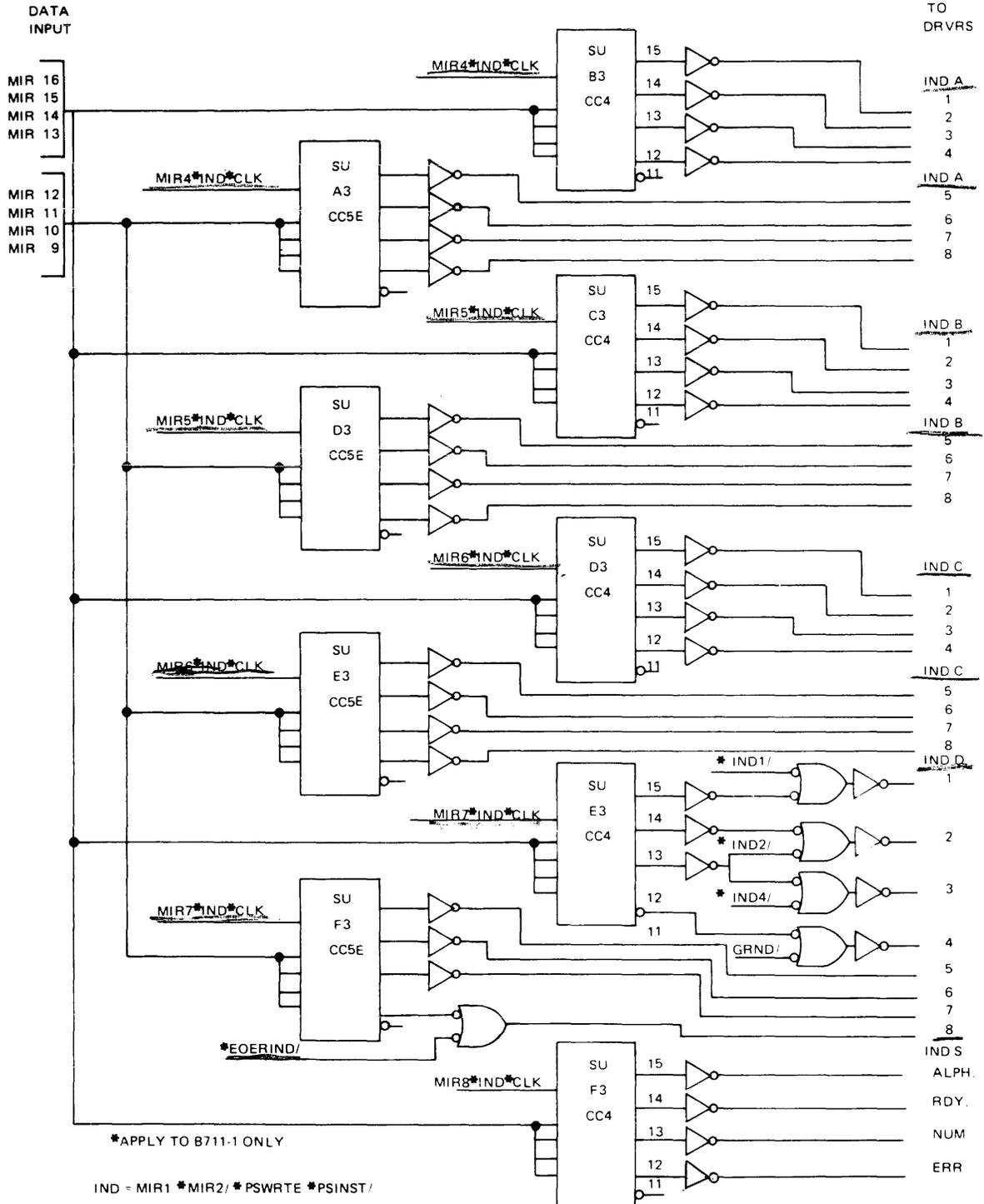
Fig. II-8 INDICATOR REGISTERS

* APPLY TO B711-1 ONLY

IND = MIR1 *MIR2/ * PSWRTE *PSINST/

is a control word. When MIR01/ and MIR02 are true, indicating a print data word, signal CCPRNT is generated (Figure II-11). CCPRNT then enables two clock pulses, BRCLK/ and PCLK/. BRCLK/ is used to load the printer/ forms data register (Figures II-14 and II-15), and PCLK/ is used to reset the PDI flip-flop (Figure II-13). Resetting the PDI flip-flop causes PDI/ to go high and inhibits the data interrupt to the processor.

Signals TUF/-1 and PDI/ set the ENPRTU flip-flop, which enables the next TUF-1 to generate signal PRTU.

The printing element on the system printer is a moveable ball which contains a 64-character set or a 94-character set. The 64-character set uses 16 rotational positions and four tilt positions to define the 64 characters. This requires two tilt bits and four rotate bits to provide coding of 64 characters (Figure II-14).

The 94-character set uses 24 rotational positions and four tilt positions to define the 94 characters. This requires two tilt bits and five rotate bits to provide coding of 94 characters (Figure II-15).
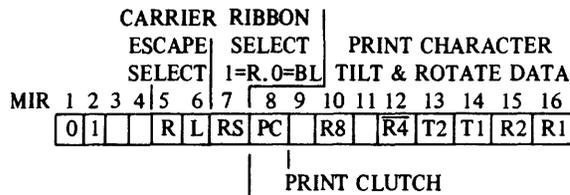
Fig. II-9 64-CHARACTER SET PRINT DATA WORD
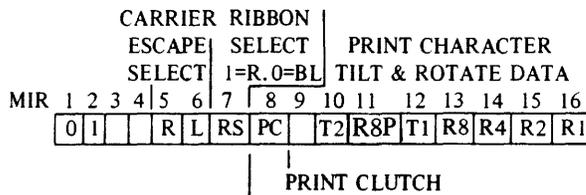
Fig. II-10 94-CHARACTER SET PRINT DATA WORD
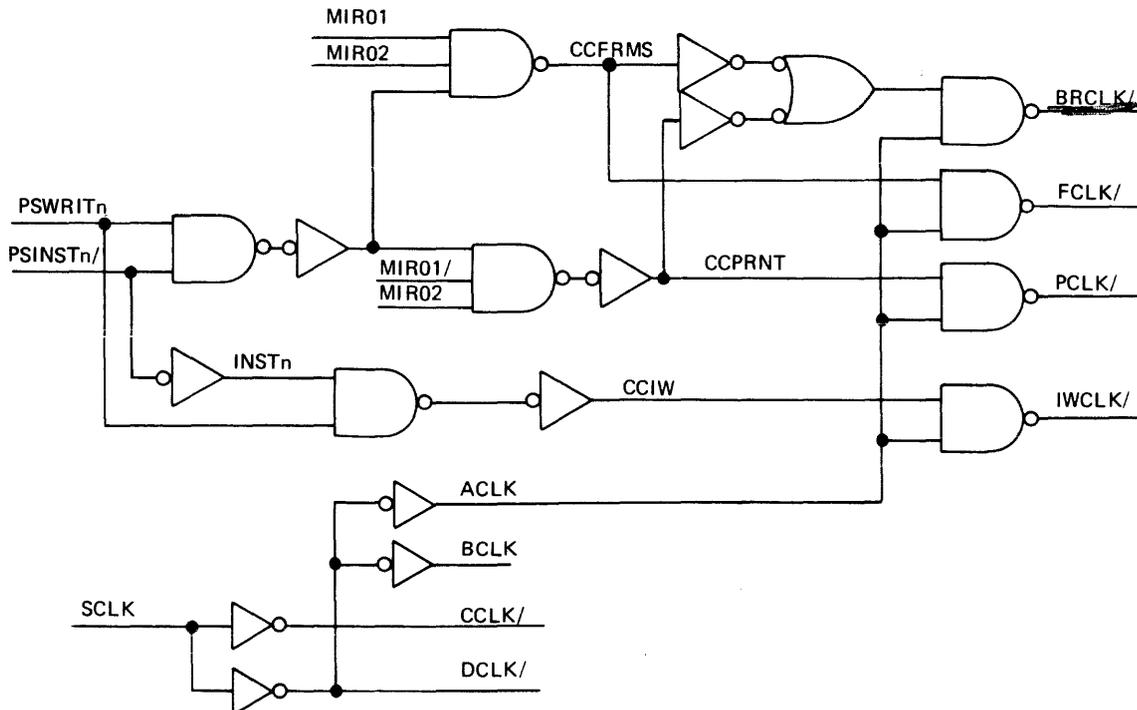
Fig. II-11 BRCLK/, PCLK/, FCLK/, AND IWCLK/ GENERATION

Functional Detail
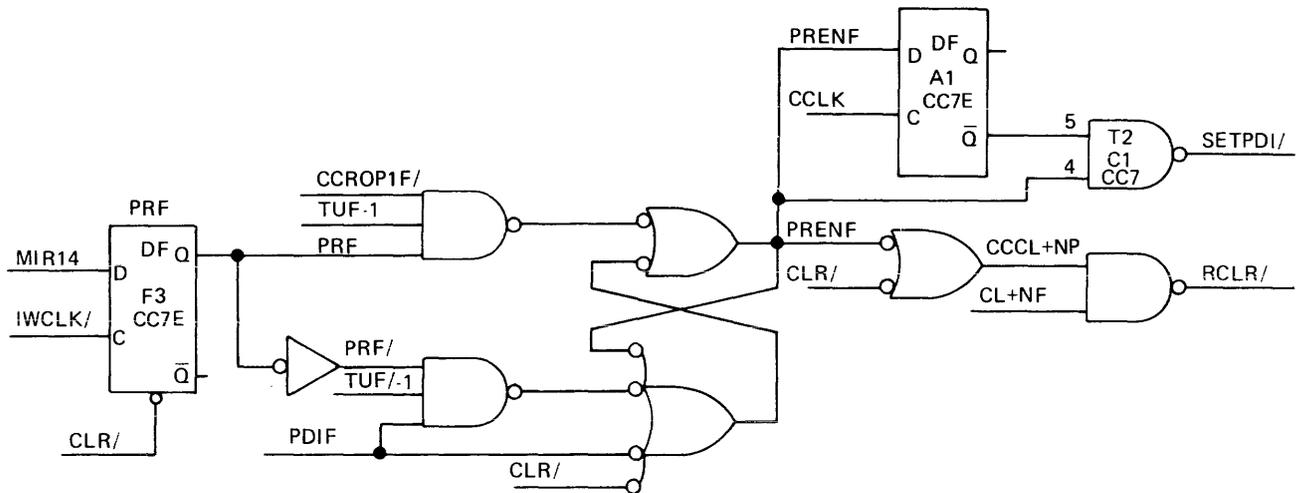
Fig. II-12 SETPDI AND RCLR/ GENERATION
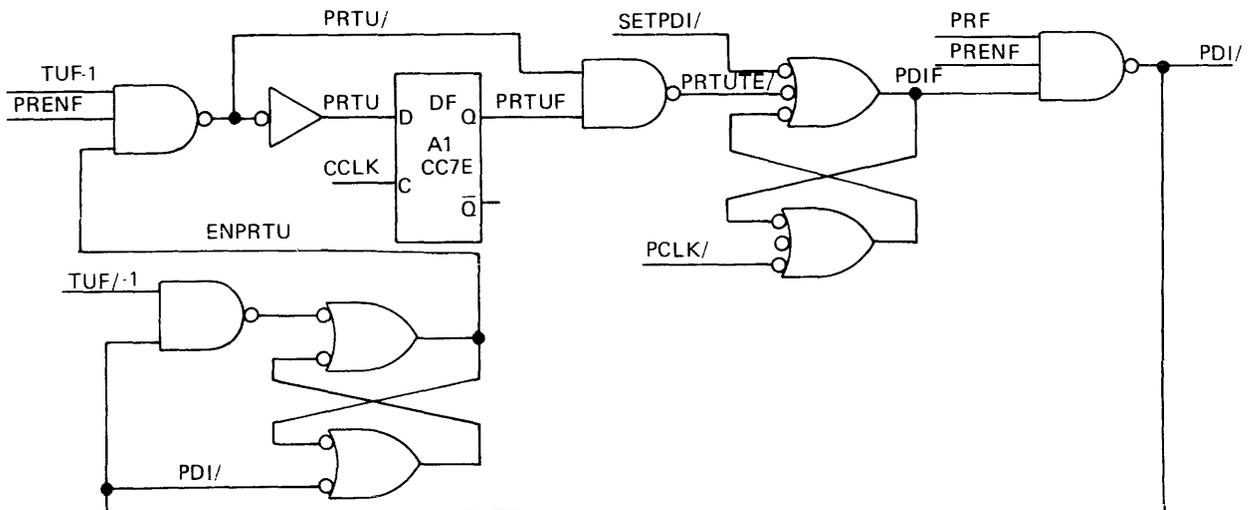
Fig. II-13 PRINTER DATA INTERRUPT

Functional Detail

Basically, the print operation is the same for both character sets. The differences are summarized below:

a. Printed circuit cards CC6E and CC7E (B0346) are used with the 64-character set. Printed circuit cards CC6EK and CC7EK (B0346-1) are used with the 94-character set.

b. The data bits of the print data word from the processor are assigned different bits positions as follows:

Bit	64-Character	94-Character
10	Rotate 8	Tilt 2
11	Not used	Rotate code expansion
12	Rotate 4 NOT	Tilt 1
13	Tilt 2	Rotate 8
14	Tilt 1	Rotate 4
15	Rotate 2	Rotate 2
16	Rotate 1	Rotate 1

c. For the 64-character set, signal CCRS+8P/ selects the red ribbon in response to receipt of a ONE in bit 7 of the print data word (Figure II-14). For the 94-character set, signal CCRS+8P/ provides expansion of the rotate code and CCRS96/ causes the shift to the red ribbon (Figure II-15). The line for CCRS96/ is present but not used in the 64-character printers.

d. For the 64-character set, the red ribbon is selected in response to the receipt of a print data word with the red ribbon bit set. For the 94-character set, two printer data words are required to change ribbon color. The first data word must have the ribbon color set to the desired state; the second data word then provides the character code in the data field and the ribbon color bit set to the same color.

Figures II-14 and II-15 show the printer/forms data register and the PCF and RSF flip-flops. With RCLR/ high, BRCLK/ strobes the MIR data into the buffers. When
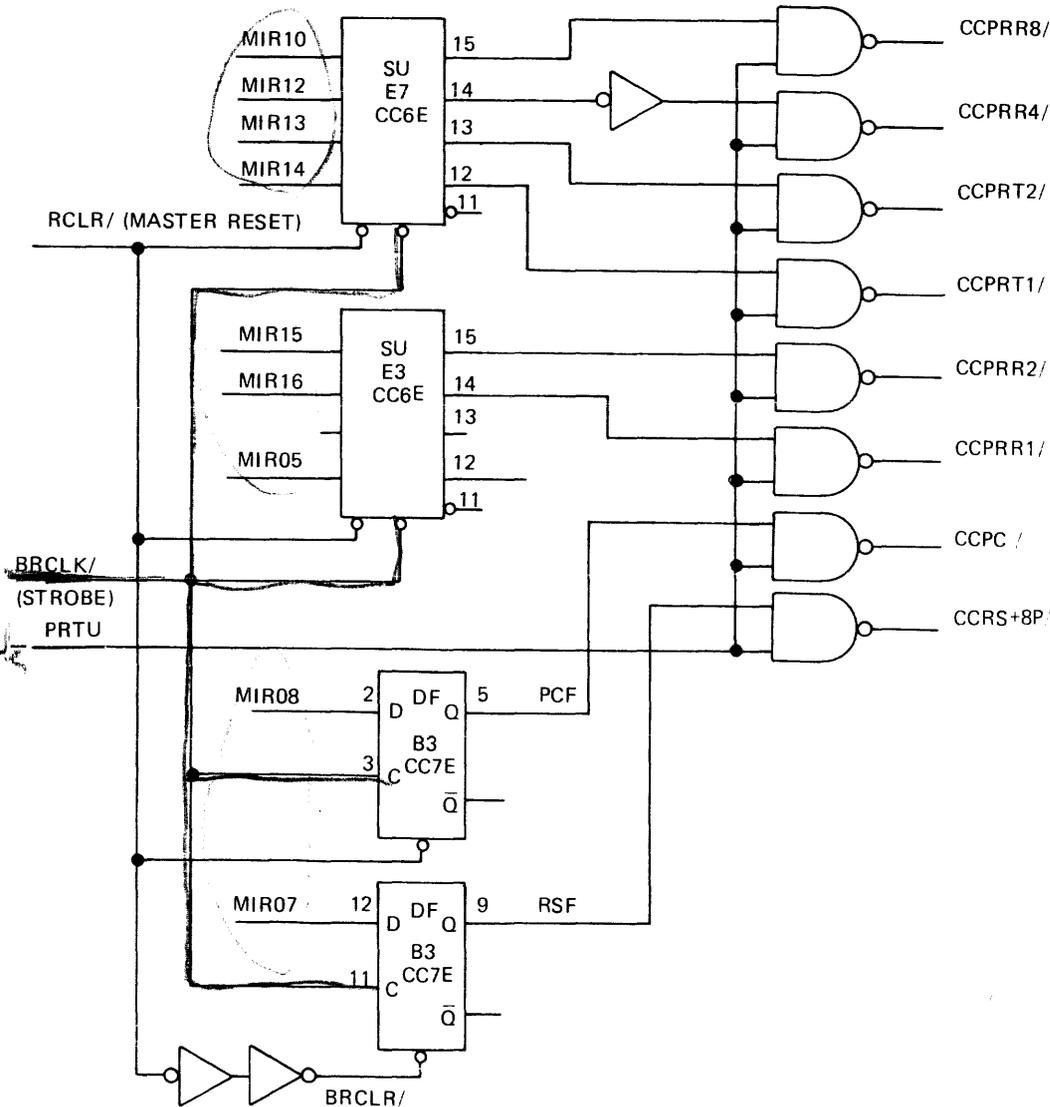
Fig. II-14 64-CHARACTER SET PRINTER/FORMS DATA REGISTER

Functional Detail
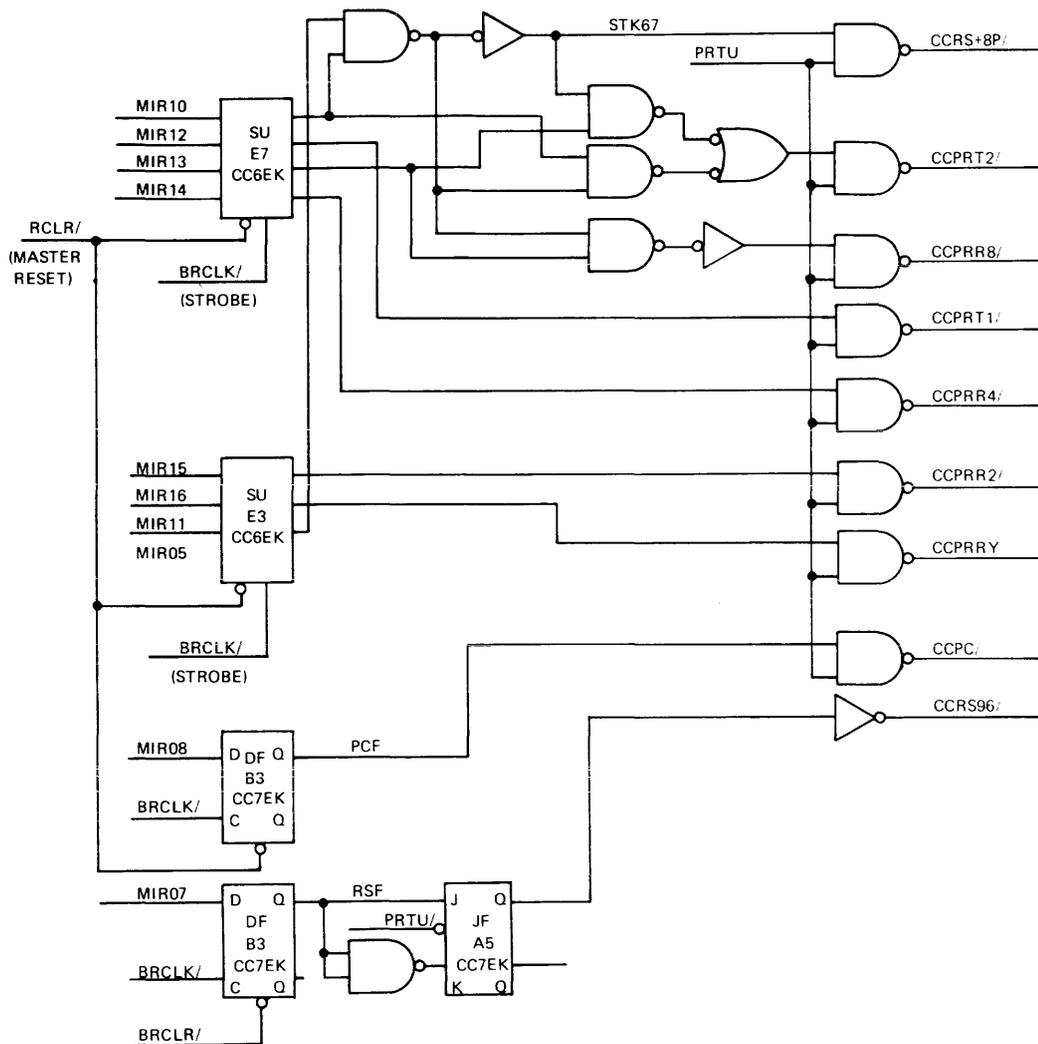
Fig. II-15 94-CHARACTER SET PRINTER/FORMS DATA REGISTER

PRTU goes high, the contents of the data registers and the flip-flops are gated out to the printer decoder. The outputs are present for 27 milliseconds to energize the clutch solenoids and index the required mechanical movement.

When TUF-1 goes low (after 27 milliseconds), PRTU goes low and disables the outputs of the data registers and the flip-flops. One clock time later, the PRTUF flip-flops is reset (Figure II-13), PRTUTE/ is low for 1 microsecond and PDIF is generated.

A high PDIF causes a low PDI/ to send a data interrupt to the processor requesting the next print data word. Signal PDI/ again resets the ENPRTU flip-flop, disabling PRTU until the next character is received. The print operation timing is illustrated in Figure II-16.

When the print operation is complete, the processor executes a device-write with the instruction bit set and MIR14 is equal to 0, which causes the PRF flip-flop to reset (Figure II-12). Flip-flop PDIF is set by PRTUTE/; PRF/, PDIF, and TUF/-1 reset flip-flop PRENF. PRF and PRENF/ generate a high PDI/ and disable any further data interrupts.
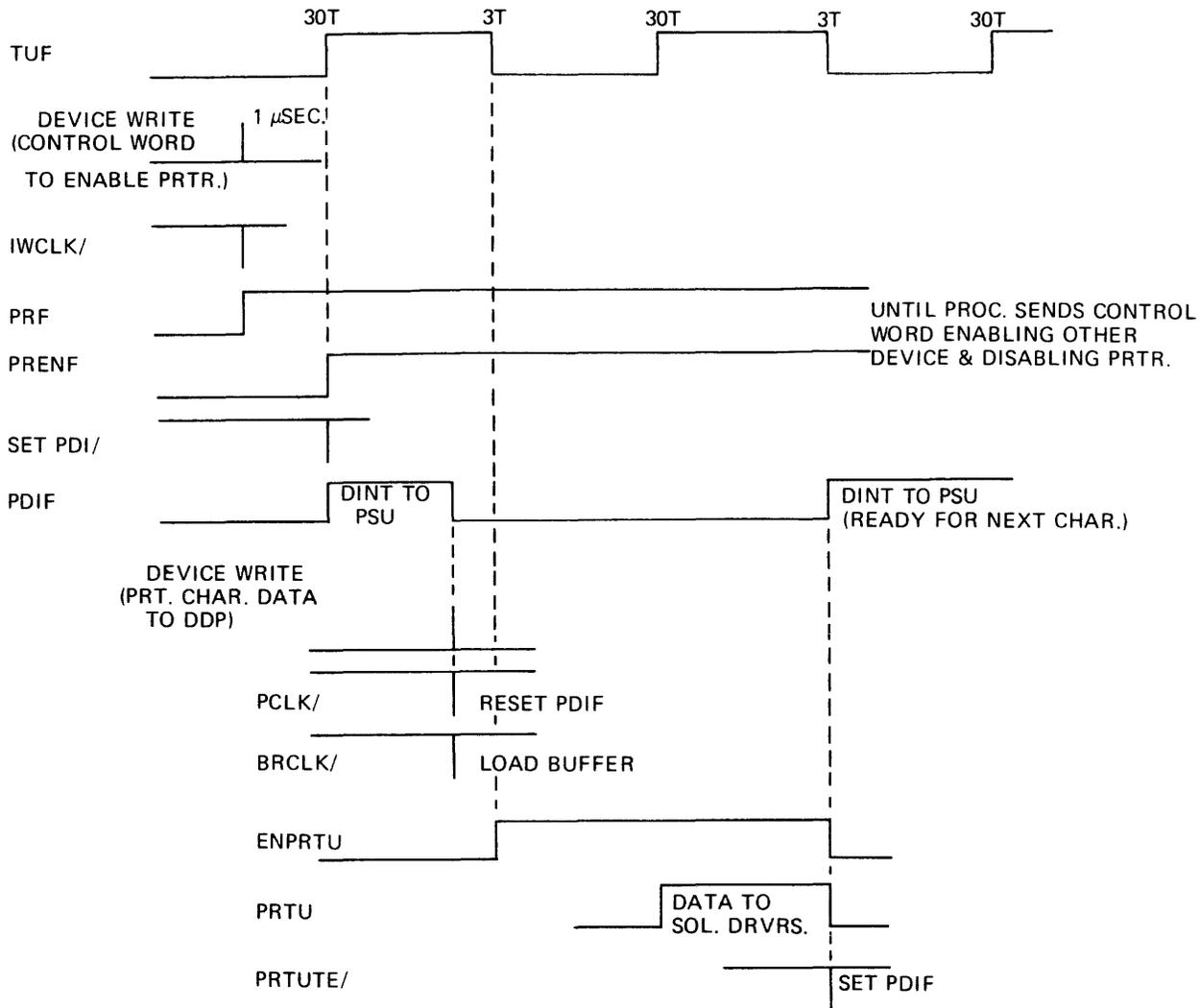
Fig. II-16 PRINT OPERATION TIMING

CARRIER CONTROL

The carrier mechanism control is used to horizontally position the character mechanism anywhere over the width of the printing area. The carrier is driven by a bi-directional 24 VDC motor. In addition to controlling the motor direction, the motor can be driven at a high or low speed with high or low power.

CARRIER MOTOR OPERATION

The carrier speed and power application depends upon the number of positions to be moved. Figure II-17 provides an example of carrier movement, 20 positions to the right. Upon receipt of a carrier data word from the processor, the number of positions to be moved is strobed into a buffer. The hold and interposer solenoids then release the carrier which is driven to the right at high speed

and full power. At the same time a photocell detects notches on a motor disk which enables a signal to count down the contents of the buffer by one for each print position.

When the carrier reaches a position six away from the desired position, (data buffer count is equal to six) the logic reverses the drive signals to the carrier causing the motor to decelerate. At the same time the low speed signal is generated.

When the carrier decelerates to 3.25 inches per second (ips), the logic causes the motor to again drive the motor in the original direction but at low speed (3.25 ips).

As the carrier passes the position one away from the desired position (data buffer count is equal to one), the logic releases the interposer hold coils and reduces the motor power to 2 amperes. Thus the carrier coasts into the desired position.
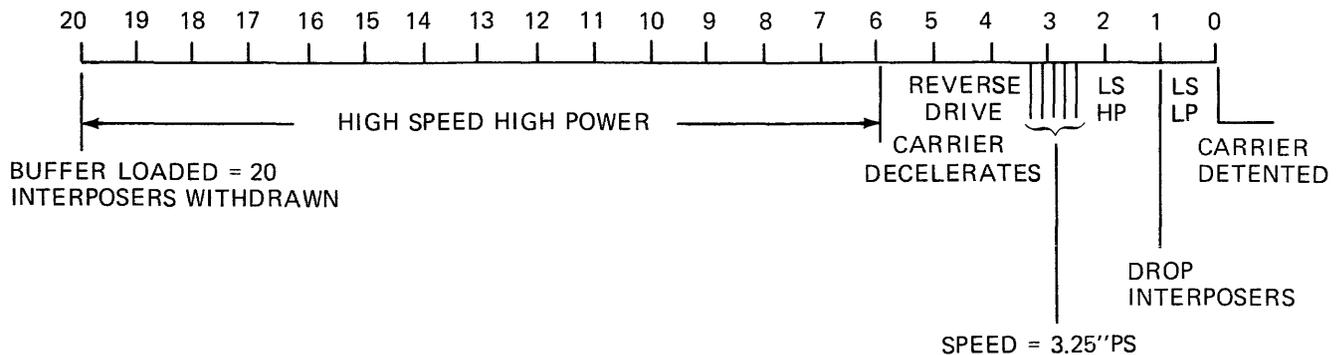
Fig. II-17 CARRIER MOVEMENT (20 POSITIONS RIGHT)

If a movement of six positions or less is required, the logic drives the carrier at low speed and full power and again counts down the data buffer. When the data buffer equals one, then the carrier motor power is reduced to 2 amperes and the interposer latches are released to detent the carrier.

When a single stop position movement is required, as when printing sequential characters, the hold coils are not used. The logic calls for low speed, full power and the interposer solenoid is energized. The resulting mechanical withdrawal of the interposer latches enables the carrier to move one position.

Direction Control

The carrier motor is controlled by four drive circuits which are selectively enabled to drive the carrier either to the left or to the right. Figure II-18 shows the carrier motor, driver circuits, and the directional control signals CRGR/ and CRGL/.

Drivers D1 and D2 provide the +24 VDC to the motor and drivers D3 and D4 are connected to ground through R1. In order to drive the carrier to the right, drivers D2 and D3 must be enabled. As shown in the upper diagram of Figure II-18, when CRGR/ is low, CRGL/ is high, drivers D2 and D3 are turned on, and drivers D1 and D4 are turned off. Thus a circuit from ground to C24V+F is enabled through D3, the motor, and D2 to drive the carrier to the right.

When CRGL/ is low, as shown in the lower diagram of Figure II-18, CRGR/ is high, drivers D2 and D3 are turned off, and drivers D1 and D4 are turned on. Thus a circuit from ground to C24V+F is enabled through D4, the motor, and D1 to drive the carrier to the left.

Note that if CRGR/ and CRGL/ are both low, then the outputs of G2, G3, G6 and G7 are low. The outputs of G3 and G7 clamp the outputs of G4 and G8 low, no drivers turn on, and no carrier movement results.

Speed Control

The output of the motor tachometer is used to monitor and control the speed of the carrier. The tachometer is a small DC generator, the output of which is proportional to the rotational velocity.

As shown in Figure II-19, Signal CRLT/ controls the selection of the tachometer output. If the carrier is to move to the left, CRLT/ is low. A low CRLT/ grounds TACHL and enables TACHR. When CRLT/ is high, TACHR is grounded and TACHL is enabled.

C1 and C2 are comparators whose operation is such that the output (pin 7) is low until input pin 2 is equal to, or greater than, input pin 3. The input to pin 3 of C1 and C2 is controlled by a level generator, LG1. For low speed carrier movement (3.25 ips), CRHS/ is high and the output of LG1 is 0.5 VDC. When a high speed carrier movement (20 ips) is required, CRHS/ is low and the output of LG1 is 3 VDC. With the carrier moving at 3.25 ips, the output of the tachometer is also 0.5 VDC, and at 20 ips it is 3 VDC. The outputs of the tachometer and the level generator are fed to a comparator, and the result is used to control the selected motor drivers, either D1 and D4, or D2 and D3.

For example, if low speed-movement to the left is required, CRHS/ is high and CRLT/ is low. A low CRLT/ enables TACHL, and LG1 applies 0.5 VDC to pin 3 of C1. The output of C1 remains low until the carrier accelerates to 3.25 ips at which time TACHL is equal to the output of LG1, the output of C1 goes high, and CRUTSL/ goes low. A low CRUTSL/ causes drivers D1 and D4 to be turned off. As a result, the carrier motor slows down until TACHL is less than 0.5 VDC, at which time the output of LG1 goes low, CRUTSL/ goes high, and drivers D1 and D4 are turned on. During normal operation, the TACHL or TACHR signals are hunting about 0.5 VDC for low speed, and the drivers are turning on and off to control the speed of the carrier.

The difference between low speed and high speed operation is the higher output from LG1 for high speed movement. The higher output from LG1 requires that the tachometer be rotated faster to generate 3 VDC.

The signal TACHBK is low when the carrier is moving at, or faster than the selected speed. TACHBK is high when
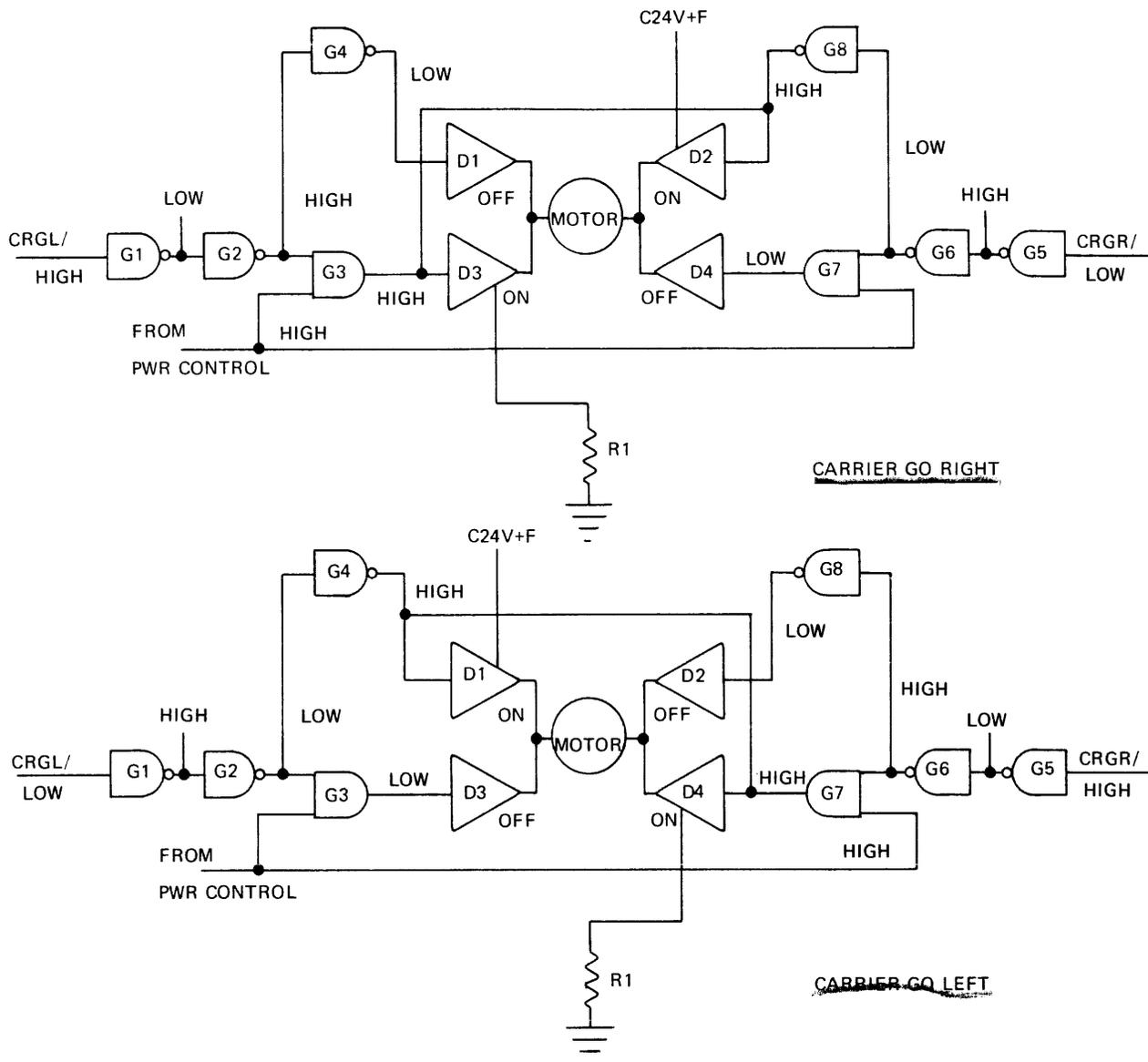
Functional Detail

Fig. II-18 CARRIER MOTOR DIRECTION CONTROL

the carrier is moving slower than the selected speed. This signal is fed back to the logic for control purposes.

Motor Power Control

At either high speed or low speed, the logic can control power to the carrier motor. Control is achieved by regulating the current through the motor drivers to either 4 amperes (high power) or 2 amperes (low power). (See Figure II-20.)

Signal CR4A/ controls level generator LG2. When CR4A/ is high, the output of LG2 is 0.5 VDC. When CR4A/ is low, the output of LG2 is 1 VDC. The output of LG2 is applied to pin 3 of comparator C3.

The ground circuit for the motor drivers D3 and D4 is through R1, which is a precision 0.25-ohm resistor. With 2 amperes flowing through this circuit, the voltage across R1 is 0.5 VDC; with 4 amperes flowing through the circuit, the voltage across R1 is 1 VDC. Resistor R1 is connected to pin 2 of comparator C3.

Whenever the voltage across R1 exceeds 0.5 or 1 VDC, depending on the power selected, the output of C3 goes high and causes an increase in conduction through driver D5. As D5 conducts more current, the voltage level inputs to G3 or G7 reduce the output level from the active gate. This in turn causes the active driver D3 or D4 to conduct less current and reduce power supplied to the motor.

When the voltage across R1 falls below either 0.5 or 1 VDC, depending on the power selected, the output of C3 goes low. Driver D5 then conducts less current and raises

Functional Detail
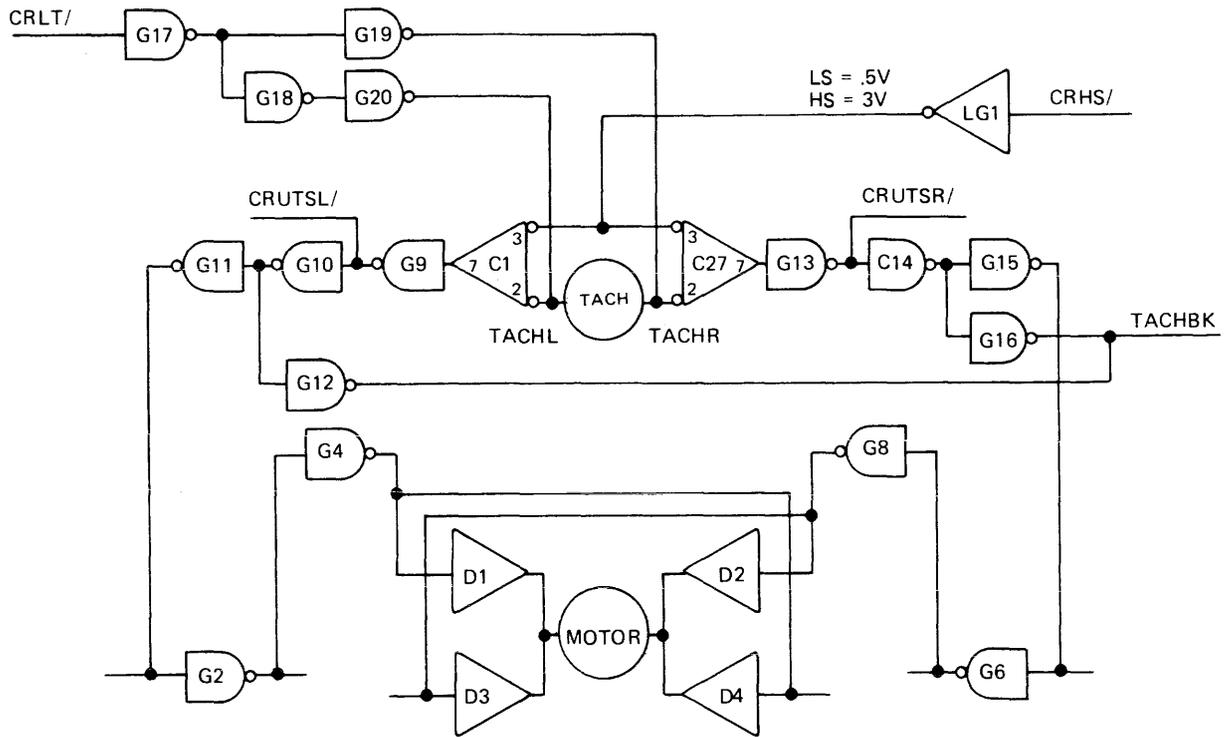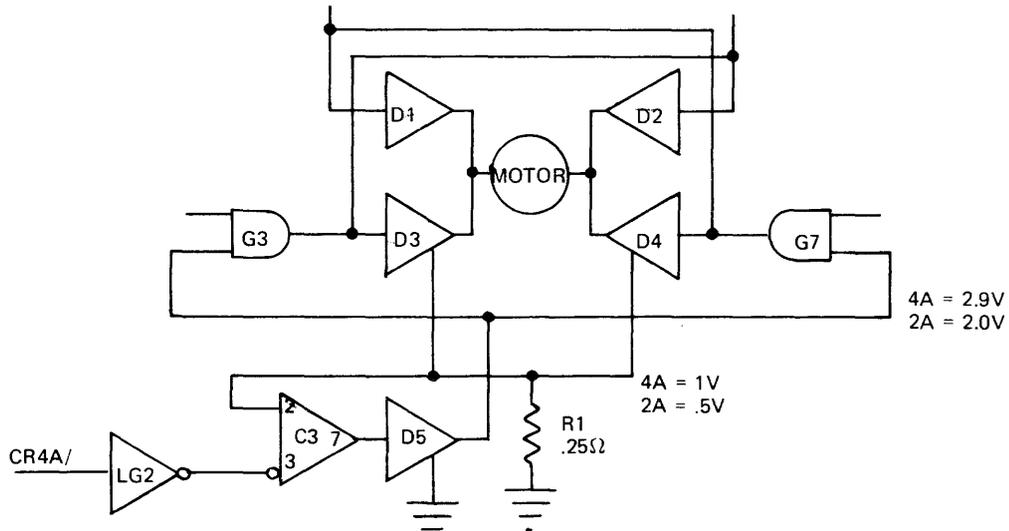

Fig. II-19 CARRIER SPEED CONTROL

Fig. II-20 CARRIER MOTOR POWER CONTROL

the voltage level at G7 and D4, or G3 and D3, to increase the drive current to the motor.

In normal operation, the output of C3 and D5 constantly varies about the selected level to regulate the current through the motor.

Figure II-21 is a complete logical representation of the carrier control circuit and shows the voltage levels at most points of the circuit as they exist for either left or right direction, high or low speed, and high or low power.

The figures in parenthesis are the levels existing when the circuit is inactive; that is, CRGR/, CRGL/, and CR4A are all high.

Figure II-22 illustrates the circuit in detail. Most of the components are located on printed circuit card CC0. The exceptions are D1, D2, D3 and D4 which, together with some associated diodes and resistors, are mounted on a heat-sink panel in the console.
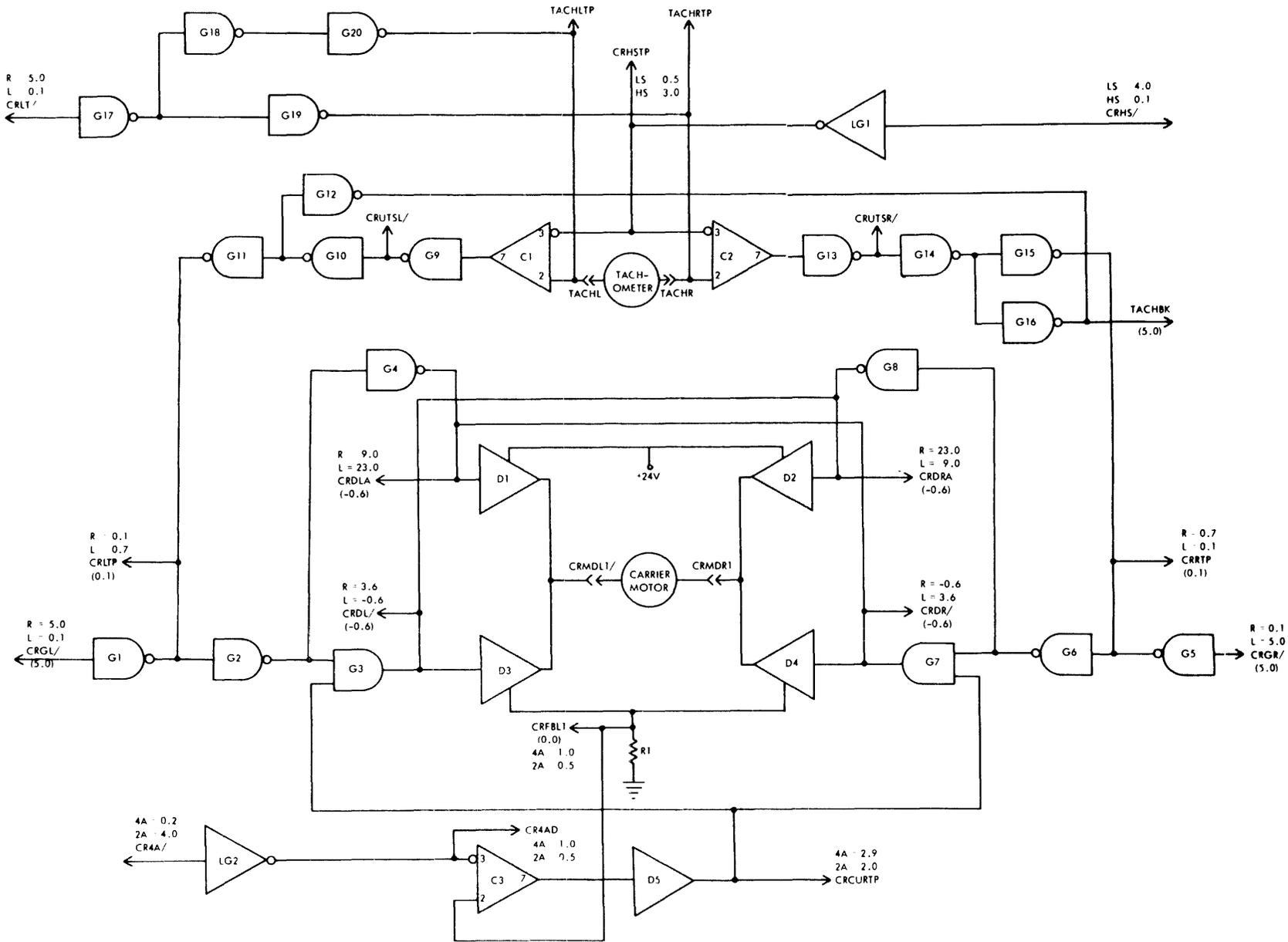
Fig. II-21 CARRIER CONTROL BLOCK DIAGRAM

Fig. II-22 CARRIER CONTROL SCHEMATIC
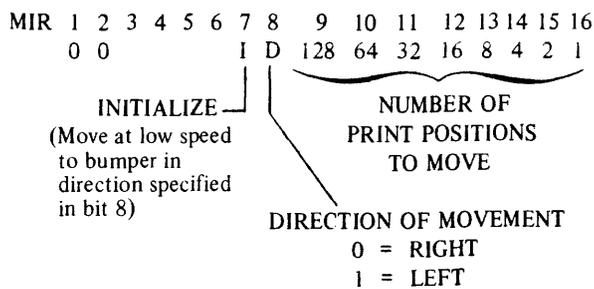
Fig. II-23 CARRIER DATA-WORD FORMAT
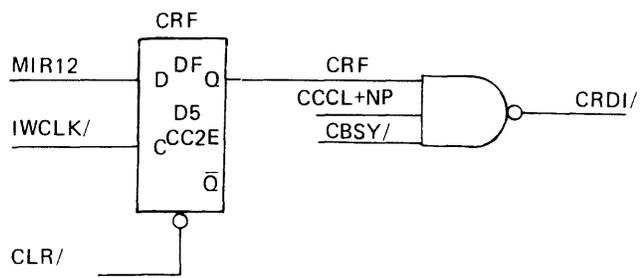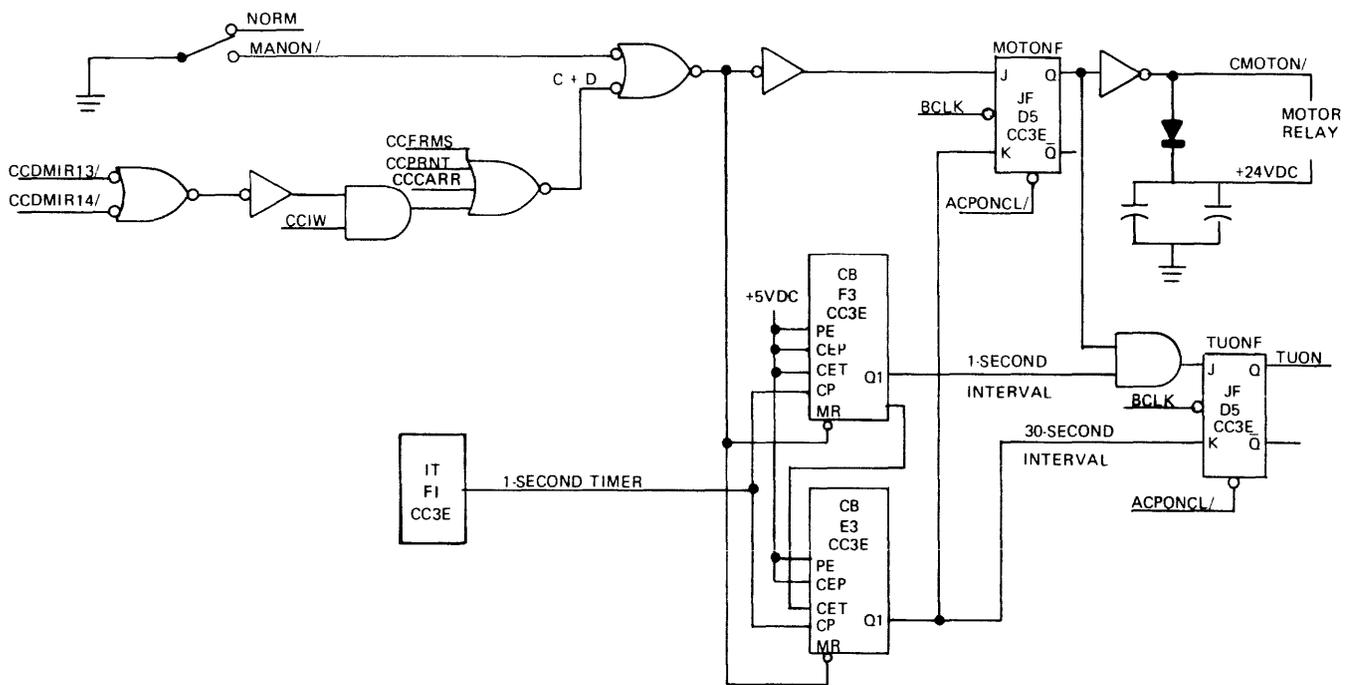

Fig. II-24 CRDI CONTROL

Fig. II-25 DECODER MOTOR ON-OFF

CARRIER LOGIC OPERATION

To enable the carrier data-interrupt, the processor executes a device write to the IOC with the instruction bit set and MIR12 high. This condition causes carrier flip-flop CRF to be set, provided that any indexed print operation is complete, and causes a carrier data interrupt to be returned to the processor.

Upon receipt of the data-interrupt, the processor may execute a device write with the instruction bit reset, to notify the IOC to accept a carrier data word from the processor. The format of the carrier data word is illustrated in Figure II-23.

The processor notifies the IOC of the number of positions to move the carrier. It is a function of the processor software to maintain a record of the actual position of the carrier. The direction of movement is specified in MIR8. MIR7 is the initialize bit and is used only to move the carrier to the extreme left bumper or the right bumper of the chassis. When this bit is set, the carrier moves at low speed until it stalls against the bumper. Data in MIR9 through MIR16 have no effect on the initialization routine.

Carrier Data-Interrupt

The carrier data interrupt circuit is illustrated in Figure II-24. When the processor transmits a control word to the IOC to enable the carrier data interrupt, a high MIR12 and a low IWCLK/ set the carrier flip-flop (CRF). If the carrier and printer mechanisms have completed any previously indexed operations, the signals CBSY and CCL+NP are high. These signals gated with CRF produce a low CRDI to return a data interrupt to the processor.
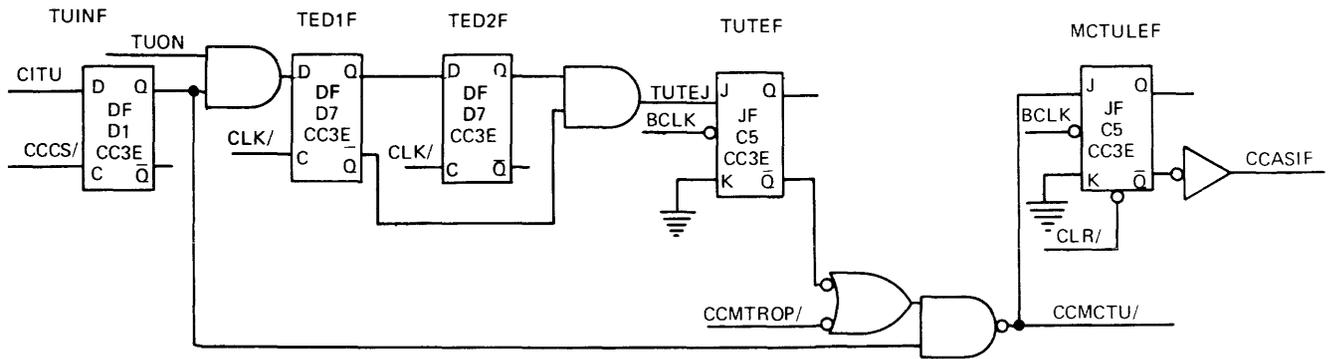
Functional Detail

Fig. II-26 TIMER UNIT GENERATION

Decoder Motor On/Off Feature

The decoder motor on-off feature provides a means of automatically turning the motor on or off as needed by the system. The motor is turned on following receipt at the IOC of a data word or a control word with the appropriate bit set; that is, carrier data, printer data, printer enable, forms data, or forms enable. There is a 1-to-2 second delay following turnon to allow the motor and associated mechanical hardware to attain operating speed. If the IOC does not receive the appropriate control or data word for a period of 30 seconds, the motor is automatically turned off.

Figure II-25, shows that the initial power application produces clear signal ACPONCL/, which resets the motor-on flip-flop (MOTONF) and the timer-unit on flip-flop (TUONF). The presence of bits MIR13 or MIR14 and the write instruction signal (CCIW), or CCFRMS, CCPRNT, or CCCARR sets the motor on flip-flop (MOTONF) and resets the timer counter CB. The output signal CMOTON/ is applied to the motor relay. When low, CMOTON/ causes the motor to be turned on. Signal MOTON is also applied to a set gate to the timer-unit on flip-flop (TUONF).

The output of internal timer IT is a 1-second pulse which clocks the timing counter. The output of timing counter CB-F3 is also a continuous 1-second pulse which enables the set gate to flip-flop TUONF. Thus, signal TUON is generated between 1 and 2 seconds after motor turnon. This delay allows the motor to attain operating speed before applying timer unit pulses to the appropriate IOC logic.

The motor can be turned on and the timer unit flip-flop can be set, independent of the processor, by placing the NORMAL/ MANUAL switch in the MANUAL position. The switch is located on board CC3 and is used in the manual position for maintenance purposes only.

With the presence of a data or control word, or with the maintenance switch in the MANUAL position, a low is applied to the master reset (MR) pins of CB-F3 and CB-E3. The application of a low master reset to the counter inhibits the counter function. With the maintenance switch in NORMAL position and signal C+D high, the master reset input to the counter is high. This allows the counter to count, and after a 30-second interval, the output of CB-E3 resets flip-flops MOTONF and TUONF. With CMOTON/ low the motor is turned off and signal TUON goes low.

The logic used to generate basic timing signal CCMCTU/ and signal CCAS1F is illustrated in Figure II-26; a timing diagram is provided in Figure II-27. Signal CCCS/ is the basic core strobe signal and is low for 10 microseconds every 300 microseconds. Signal CITU is the console interface timer unit signal, which remains high during the time that the flag passes through the transducer in the console. The timer unit input flip-flop (TUINF) remains set during the period that the flag passes through the transducer. Signal TUIN is gated with TUON to set trailing edge detector 1 flip-flop (TED1F). Both trailing edge detector flip-flops are cleared by the processor clock pulse (CLK). As shown in Figure II-27, the timer unit trailing edge signal (TUTEJ) is produced during the time that TED1F is reset and before TED2F is reset (1 microsecond). The timer unit trailing edge flip-flop (TUTEF) is set by TUTEJ and the first trailing edge of BCLK after TUONF has been set. TUTEF remains set until the motor is turned off. With TUTEF set, signal CCMCTU/ is produced by the output of TUINF. Motor-controlled timer-unit leading-edge flip-flop (MCTULEF) is set by the leading edge of CCMCTU/. This flip-flop remains set until reset by the CGCLEAR signal from the processor. As long as flip-flop MCTULEF is set, signal CCAS1F is present.
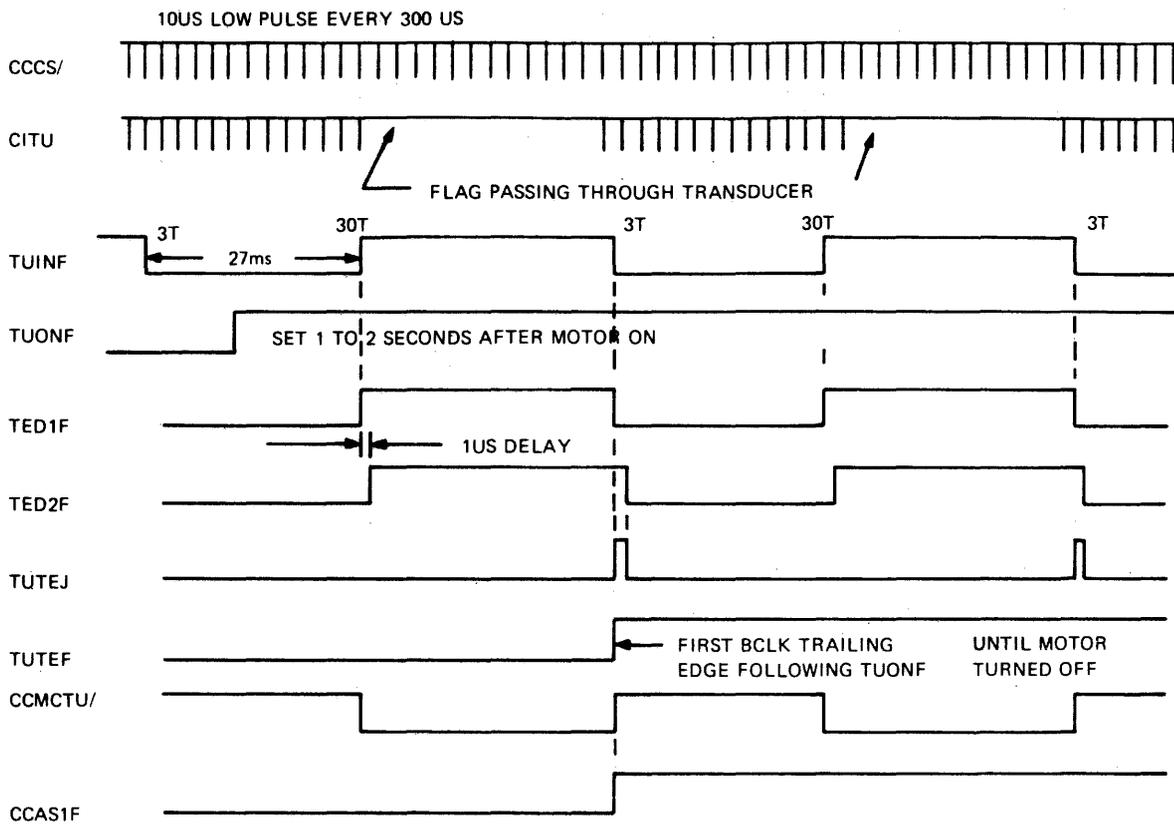
Fig. II-27 CARRIER TIMING DIAGRAM

Carrier Data Word

When the processor receives the data interrupt, it can then send a carrier data word to the IOC to request a carrier movement. A write signal (WRITE) and the absence of an instruction signal (INSTn/) gated with MIR01/ and MIR02/ to generate signal CCCARR. (See Figure II-28.) MIR09 through MIR16 are decoded and, if the data does not equal zero, signal CCZERO/ goes high. CCZERO/ is gated with CCCARR to set flip-flop CROP1F. A low CROP1F/ produces a high CBSY, which causes CRDI/ to go high and remove the data interrupt to the processor.

Load Carrier Buffer

When CCOCARR/ goes low it enables the clock pulse, at the end of the device-write operation, to strobe MIR09 through MIR16 into the data buffer. The carrier data buffer, shown in Figure II-29, consists of two 4-bit up-counters (CB). Because the logic counts down carrier position data, the buffer is loaded with the complement of MIR09 through MIR16.

Interposer and Hold Control

When signal XCARR sets flip-flop CROP1F (Figure II-28), flip-flop CRS1F (Figure II-30) is also set. CRS1F is gated with CCAS1F so that, at the next 30T, CRS2F is set. CRS2F then resets CRS1F at the next clock pulse.

CRS2F is gated with TUF/-2 to set flip-flops ENINTF and HOLDF at the next 3T. When flip-flop HOLDF is set, the carrier interposer hold coils are energized. Signal ENINTF is gated with CRS2F and TUF/-2 to set flip-flop INTF at the following 30T. Signal INTF/ enables the next clock pulse to reset flip-flop ENINTF, and INTF is gated with TUF/-2 to enable the clock pulse to reset flip-flop CRS2F at the following 3T. A low CRS2F resets flip-flop INTF. Thus, flip-flop INTF is set for 27 milliseconds, and the carrier interposer solenoid is energized to index a mechanical withdrawal of the interposer latches. Flip-flop HOLDF remains set, holding the interposers until LSLPF/ or STALF/ is present.

Carrier Speed and Power Control

When the data loaded in the carrier buffer requires a greater than six-print position movement, the initial carrier movement is at high speed and high power. This is controlled by signal CCLTEQ6 which is true only when the buffer contents equal 6 or less (Figure II-29).

As shown in Figure II-31, the carrier high speed flip-flop (CRHSF) is set by CCLTEQ6/, which is gated with INTF and TUF/-2. With CRHSF set, CCCRHS/ and CCCR4A/ are both low and cause the carrier to be driven at high speed and high power.
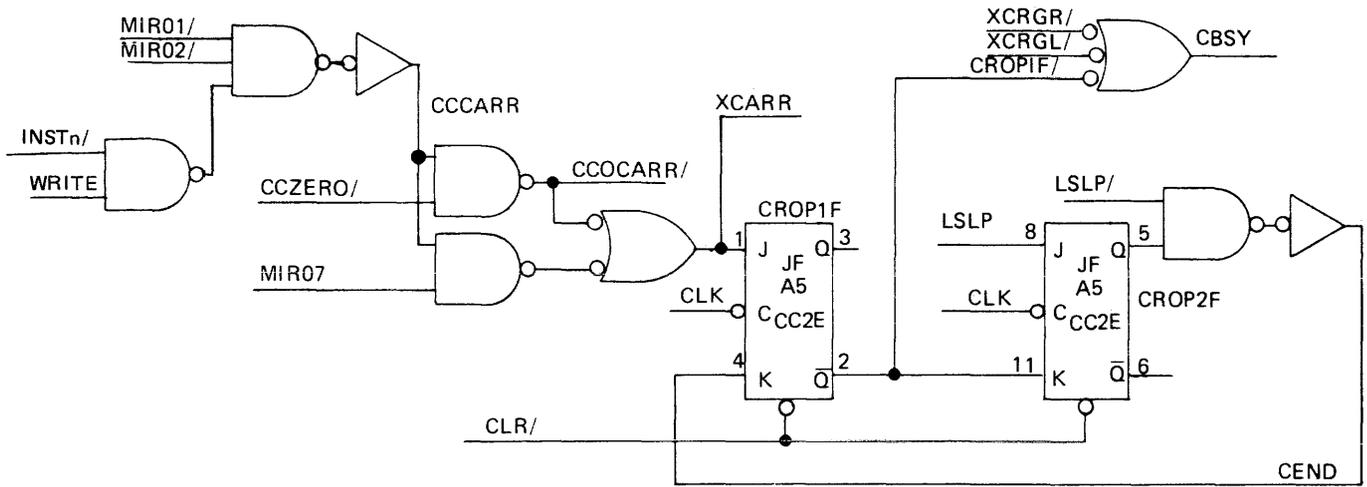
Functional Detail
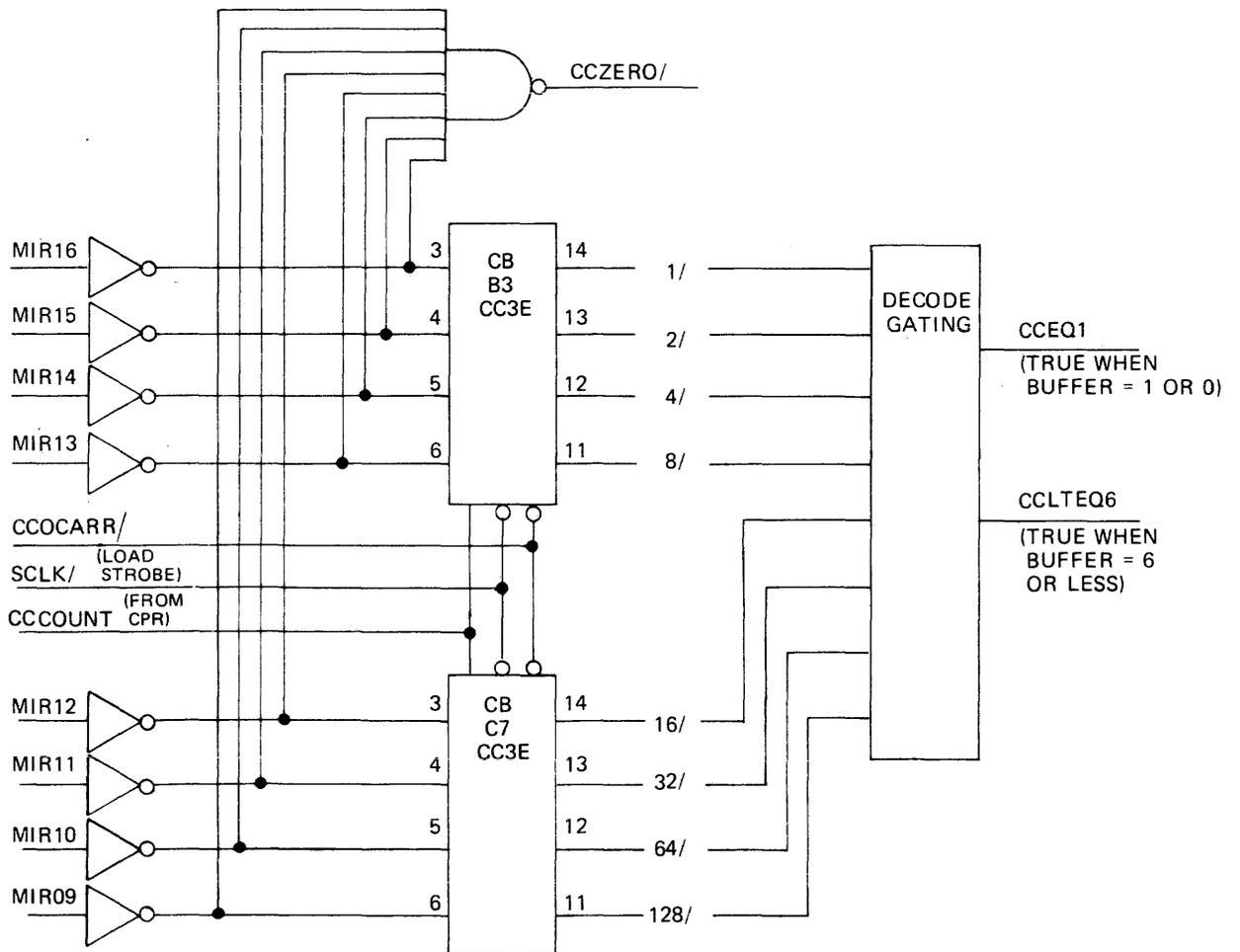
Fig. II-28 CROP1F, CROP2F AND CBSY

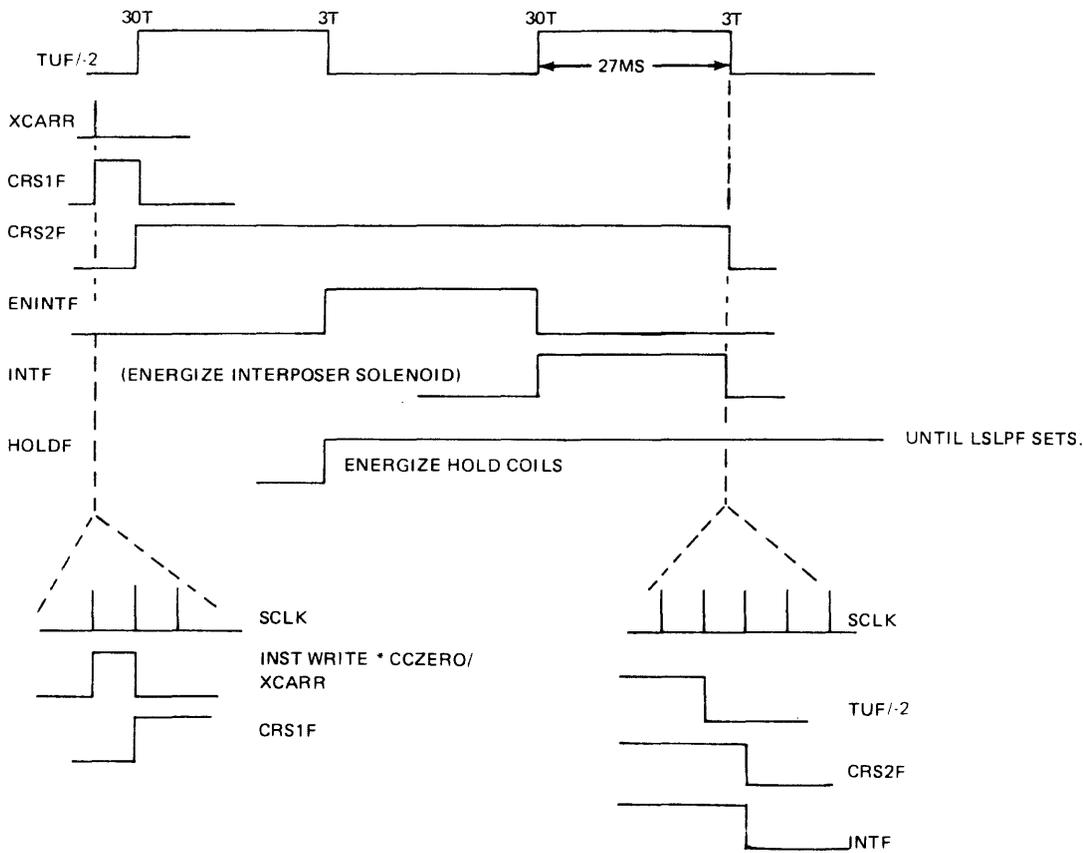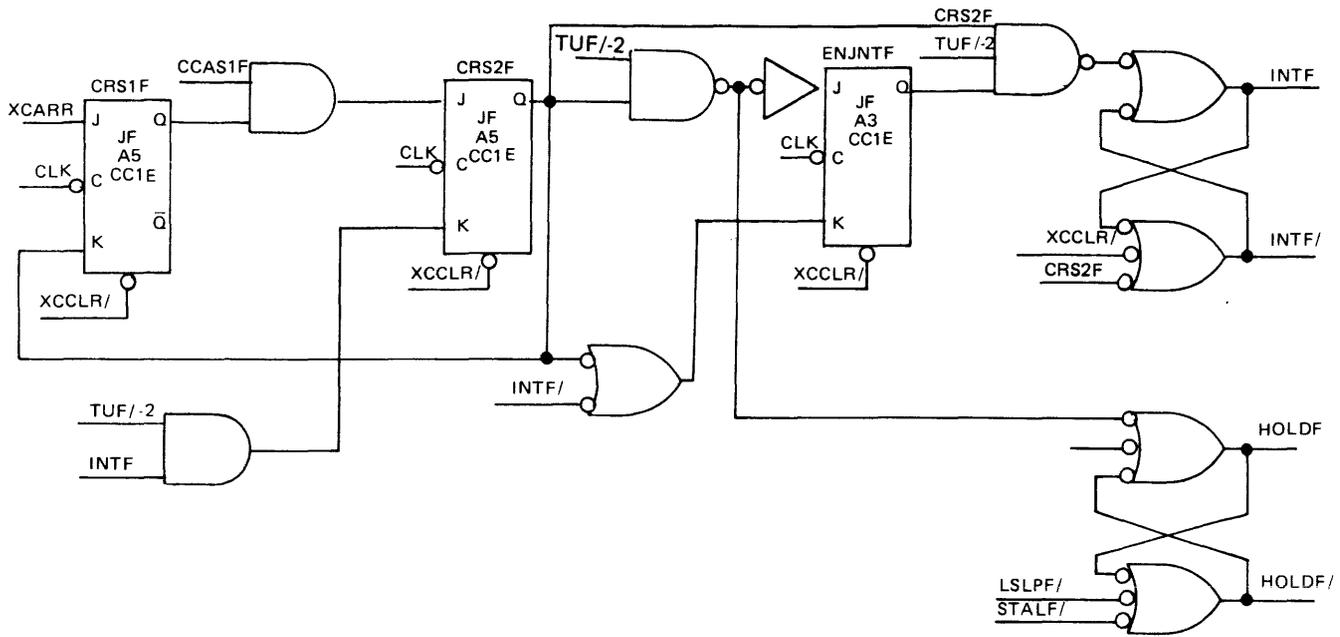Fig. II-29 CARRIER DATA BUFFER

Functional Detail

Fig. II-30 INTERPOSER AND HOLD LOGIC
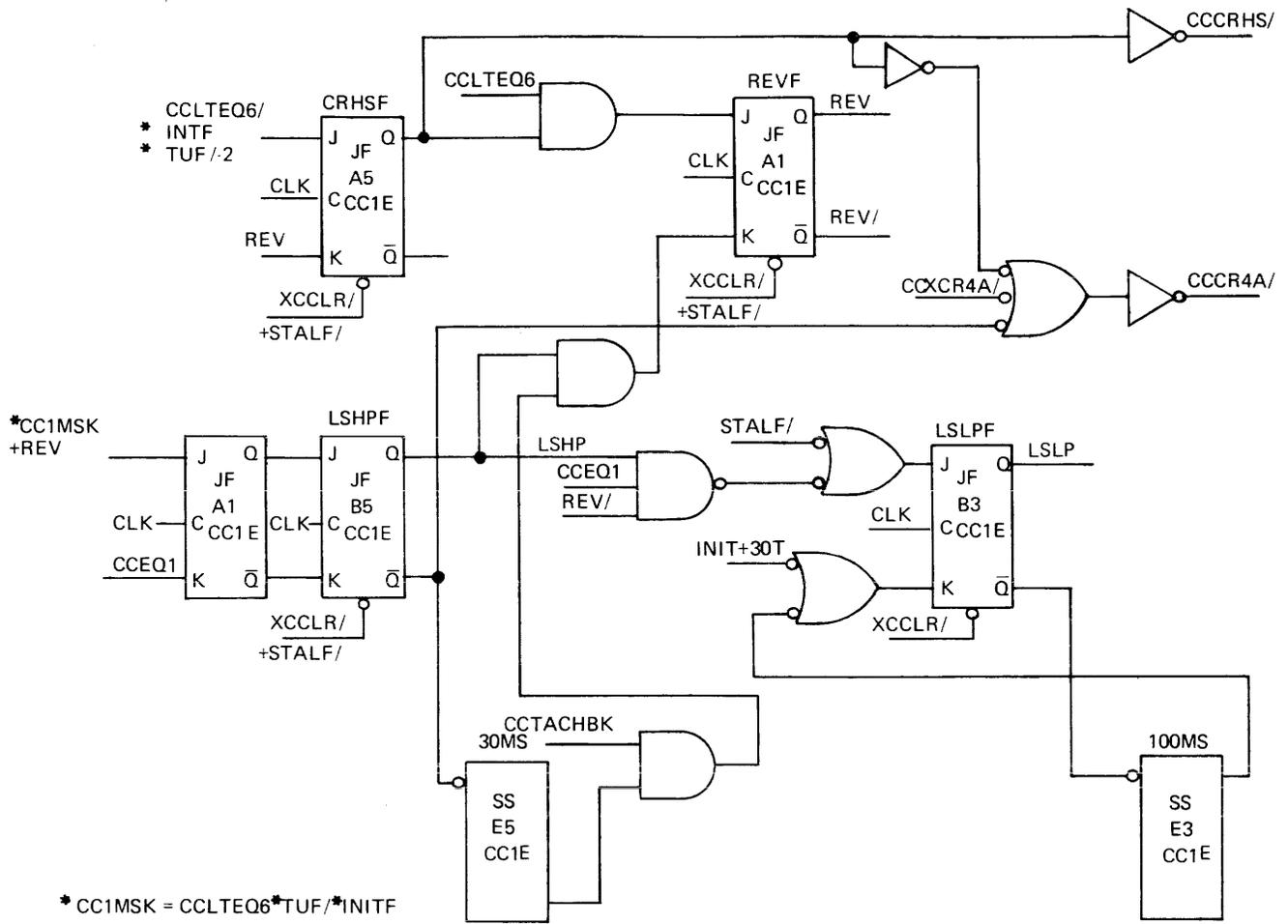
Functional Detail

Fig. II-31 CARRIER SPEED AND POWER CONTROL

When the carrier reaches a position six print positions from the final position, signal CCLTEQ6 goes high and sets the reverse flip-flop REVF. The signal REV enables the next clock pulse to reset flip-flop CRHSF and to set the low speed high power flip-flop LSHPF. At the same time, REV reverses signals CCCRGR/ and CCCRGL/ so that the motor rapidly decelerates. With flip-flop CRHSF reset, CCCRHS/ is high, indicating low-speed movement.

When flip-flop LSHPF is set, the 30-millisecond single-shot is triggered and disables the CCTACHBK gate. This gating is to block noise which appears on the CCTACHBK line due to the change in input to the level generator (LG1, Figure II-21) as flip-flop CRHSF resets. After 30 milliseconds, the gate is enabled and CCTACHBK goes high when the carrier decelerates to 3.25 ips. The output of the gate is then gated with LSHP to reset flip-flop REVF.

When the carrier reaches one print position from the final position, signal CCEQ1 goes high. Signal CCEQ1, REV/, and LSHP set the low-speed, low-power flip-flop (LSLPF), whose output resets the hold flip-flop HOLDF

(Figure II-30) and releases the carrier interposers. At the same time, LSLP/ triggers the 100-millisecond single-shot. Within 31 milliseconds, the carrier is detected in its final position. When the 100 millisecond single-shot times out, flip-flop LSLPF is reset and all drive signals are removed from the carrier.

Carrier Position Readout

As the carrier moves from one print position to another, signal CCCPRA/ is produced by a photocell readout of a notched disk attached to the carrier motor shaft in the console. Signal CCCPR, developed from CCCPRA/, is used to count the carrier positions moved which enables the logic to monitor the position of the carrier. However, when the interposer latches are withdrawn, a certain interval of time is required before the carrier motor can accelerate the carrier. During this time, the CCCPR signal is unpredictable and is prevented from generating a count signal for 12.5 milliseconds.

As shown in Figure II-30, there is one clock-time delay between TUF/-2 going low and flip-flops CRS2F and INTF resetting. Signals INTF and TUF/-2 are gated to
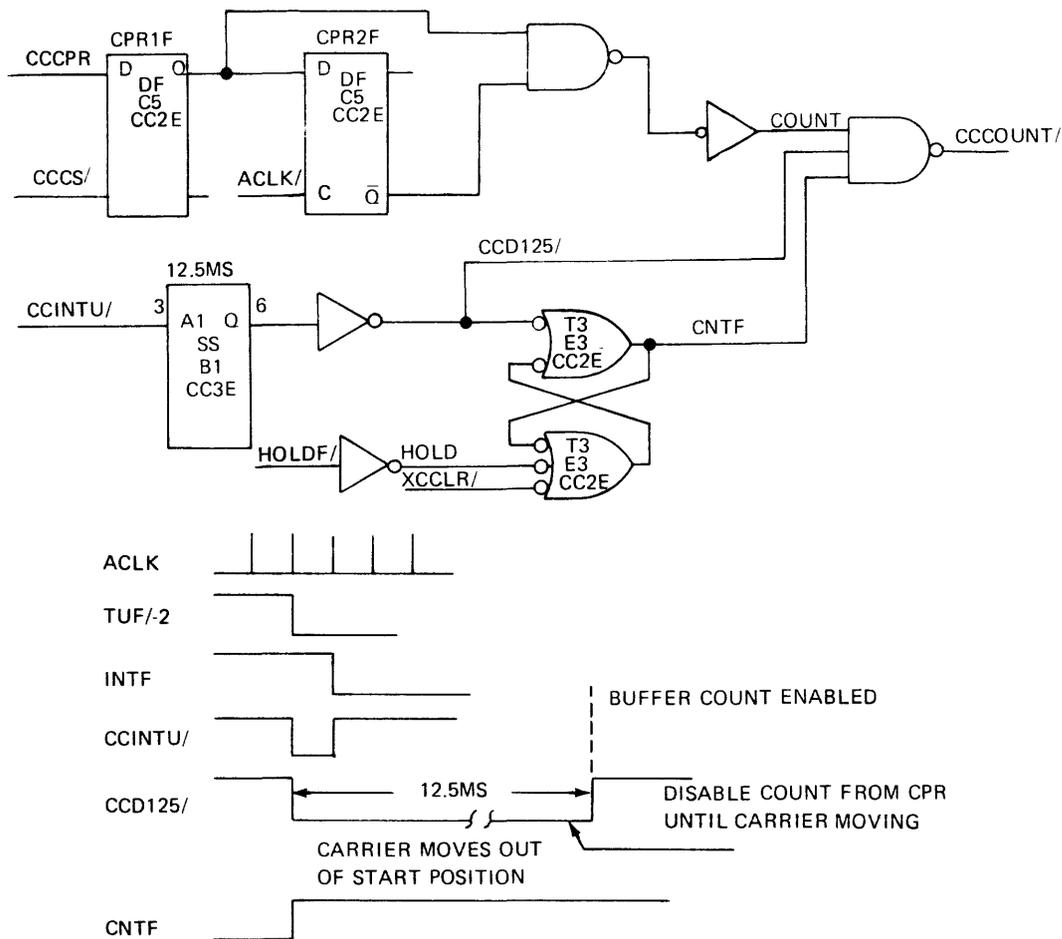
Fig. II-32 COUNT GENERATION AND CONTROL TIMING

generate a 1-microsecond pulse, CCINTU. Signal CCINTU triggers a single-shot device which causes CCD125/ to go low for 12.5 milliseconds. A low CCD125/ (Figure II-32) sets the counter flip-flop (CNTF) and also disables the CCCOUNT/ gate. Signal CNTF is high only if the HOLDF flip-flop is set.

Signals CCCPR from the carrier motor and CCCS/ control the CPR1F flip-flop, which is set and reset for each print position. The CPR2F flip-flop follows the CPR1F flip-flop, but is delayed one clock time. The outputs of flip-flops CPR1F and CPR2F are gated together as shown in Figure II-32 to generate a count signal each time CPR1F is set.

When CCD125/ goes high, the CCOUNT/ signal is enabled to count the carrier data buffer. Since the carrier has a nominal acceleration of 400 ips, 12.5 microseconds represents approximately one-third of a print position from the start position (Figure II-33).

Carrier Move Less Than Six

If MIR9 through MIR16 data in a carrier data word is equal to six or less, then the signal CLTEQ6 goes high as

soon as the data is strobed into the buffer (Figure II-29), thus preventing the setting of the CRHSF flip-flop (Figure II-31).

Signal CCLTEQ6 is gated with TUF/-2 and INTF to produce a low CC1MSK/. Signal CC1MSK/ then enables the next clock pulse to set LSHPF to initiate a low-speed movement of the carrier. The high-speed and reverse functions are not used at this time. When CCEQ1 becomes true, flip-flop LSHPF is reset and flip-flop LSLPF is set to reduce carrier power and to drop the interposers.

If the MIR9 through MIR16 data is equal to one stop position, the signal CCEQ1 could be high as soon as the data is loaded into the buffer. Because this signal resets flip-flop LSHPF to reduce the carrier motor power in normal operation, it is necessary to disable CCEQ1 until the carrier has moved out of its present position. This is accomplished when CC1MSK/ goes low and triggers a single-shot device which disables CCEQ1 for 10 milliseconds (Figure II-34). Thus, LSHPF is high for 10 milliseconds to drive the carrier out of the present position before half power is applied.

Referring to Figure II-33, it can be seen that

Functional Detail
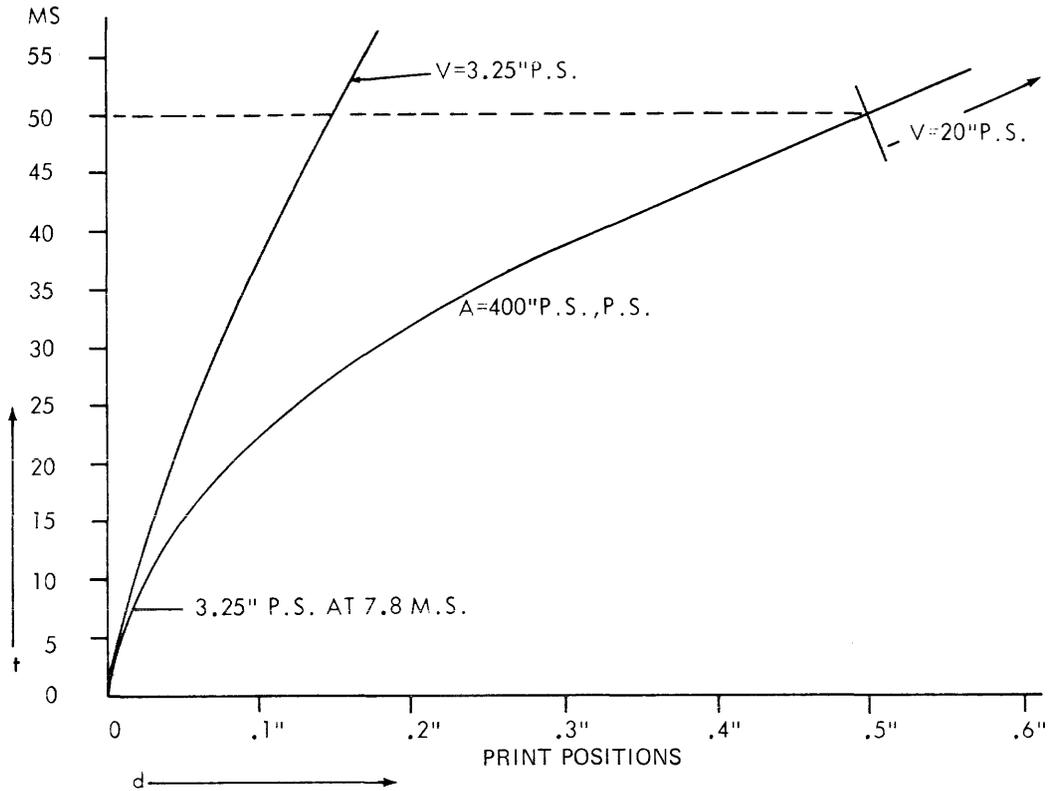
AT 20" PER SEC. EACH PRINT POSITION = 5MS
AT 3.25" PER SEC. EACH PRINT POSITION - 30.77MS
CARRIER ACCELERATION = 400" PER SEC., PER SEC.
CARRIER DECELERATION = 800" PER SEC., PER SEC.
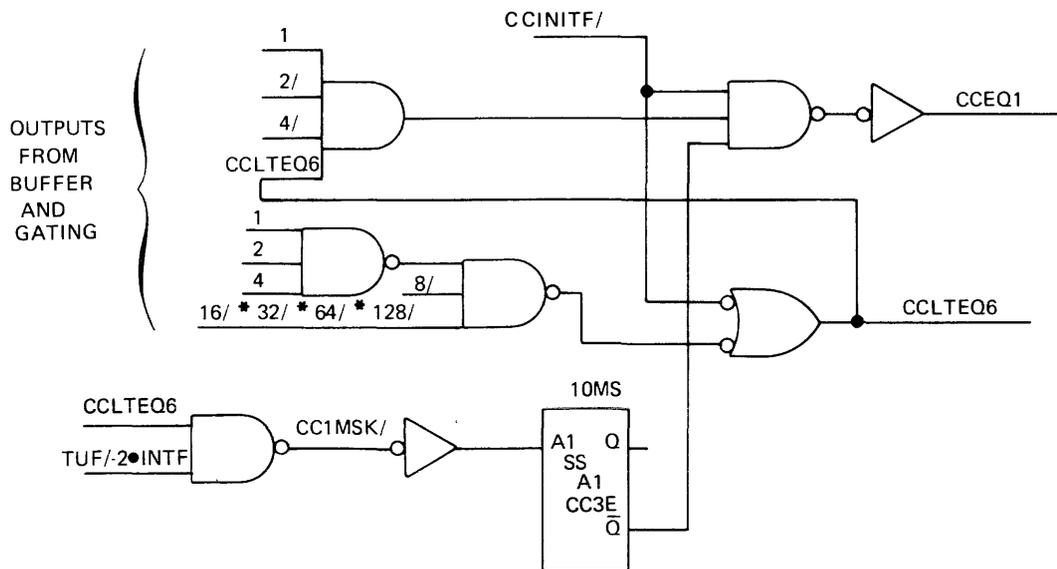
Fig. II-33 CARRIER ACCELERATION CHART

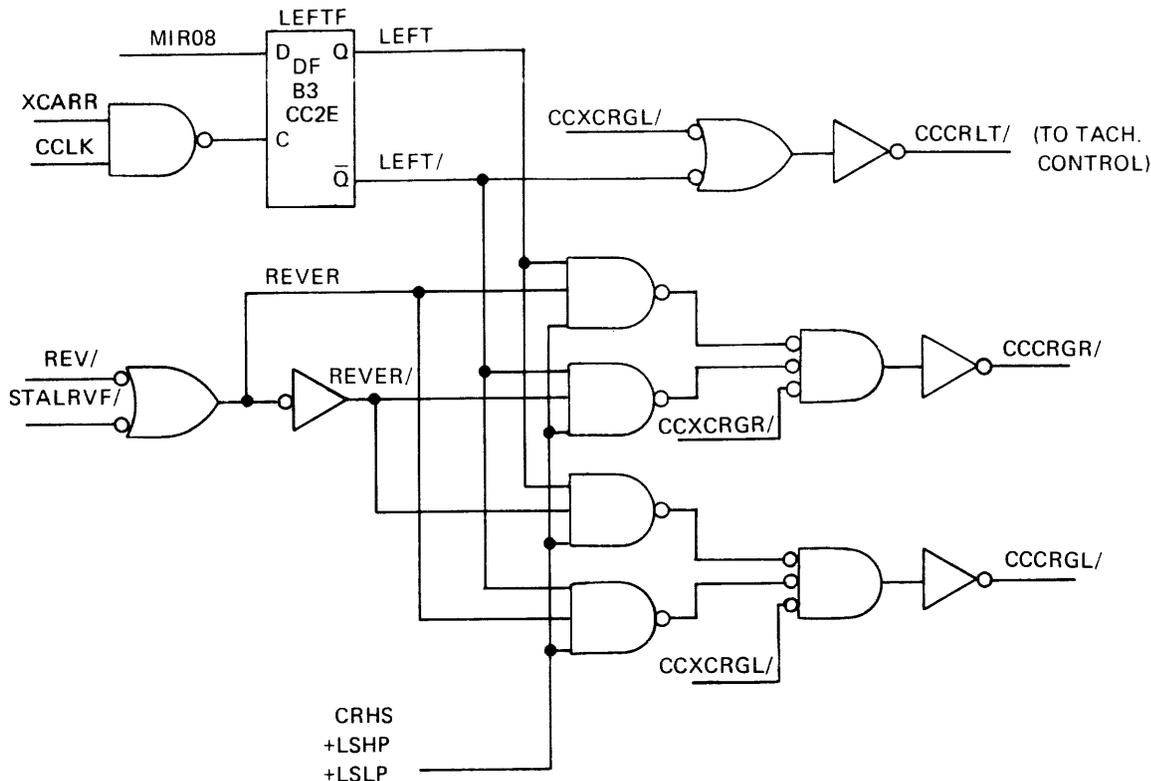Fig. II-34 CARRIER BUFFER AND CTR OUTPUT CONTROL

Fig. II-35 CARRIER DIRECTIONAL CONTROL

10 milliseconds enables the carrier to accelerate to 3.25 ips and travel less than one-third of a print position.

Carrier Directional Control

When the carrier data word is transmitted to the IOC, MIR08 is used to set or reset LEFTF flip-flop. The outputs of the flip-flop are then used to generate signals CCCRGR/ and CCRGL/, which determine the direction of carrier movement.

As shown in Figure II-35, XCARR controls the clock input to flip-flop LEFTF, so that the flip-flop is only set or reset when a carrier operation is indexed. Signals LEFT and LEFT/ are gated with CRHS or LSHP or LSLP and REV/ to make either CCCRGR/ or CCCRGL/ low.

When flip-flop REVF is set at a point six print positions away from the final position, signal REVER is generated to reverse carrier direction and decelerate the carrier. When flip-flop LSLPF is reset and the carrier is detented the gates are disabled and CCCRGR/ and CCCRGL/ are both high.

Overspeed Flag Logic

If the reverse flip-flop, REVF is still set at the time CCEQ1 goes high, it indicates that the carrier failed to decelerate to 3.25 ips in the normal time. When this action occurs, the carrier drive is turned off and a flip-flop is set to indicate this condition to the processor.

In Figure II-36, REV and CCEQ1 set status read 15 flip-flop (SR15F), the overspeed status flag. A low SR15F/ generates a low XCCLR/ which resets the carrier logic flip-flops except the HOLDF flip-flop.

This action causes the carrier motor to be turned off and the interposers held while the mechanism comes to a halt. The low SR15F/ causes a low SINTn/ which produces a status interrupt to the processor.

When the processor executes an address and status request, or a device read with the instruction bit set, CCENSTA strobes signal SR15F to EXT15/ and resets flip-flop SR15F.

Stall Flag Logic

If the carrier mechanism is physically prevented from moving by some obstruction, the carrier drive is turned off and a flip-flop is set to indicate the condition to the processor. The signal XCHOLD goes high when flip-flop CNTF is set and the 1.25-millisecond single-shot has timed out (Figure II-37). Flip-flops CNT1F and CNT2F comprise a counter which is clocked by TUF-2. Each CCCOUNT/ pulse from CCCPR directly resets flip-flops CNT1F and CNT2F. If the carrier is obstructed and stops moving, CCCPR pulses are not generated and CCCOUNT/ stays high. With CCCOUNT/ high, TUF-2 clocks the counter and, after three TUF-2 pulses, TUF-2 is gated with signals CNT1F and CNT2F to set the stall flip-flop STALF. With flip-flop

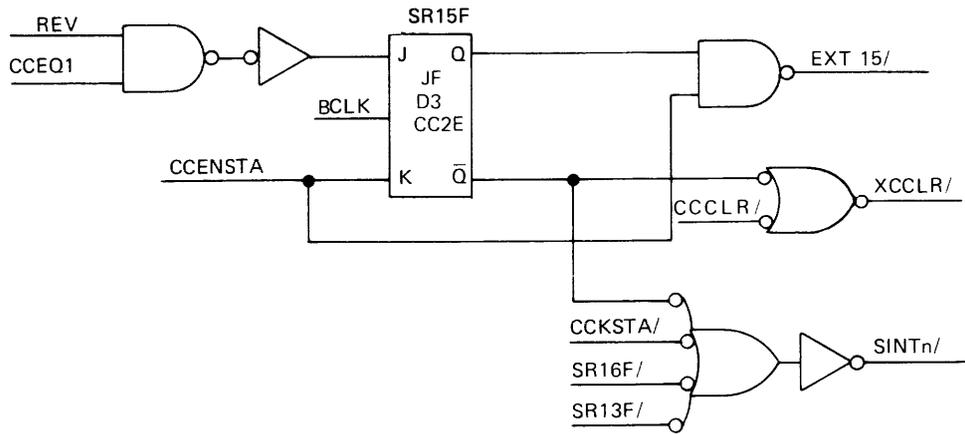Functional Detail

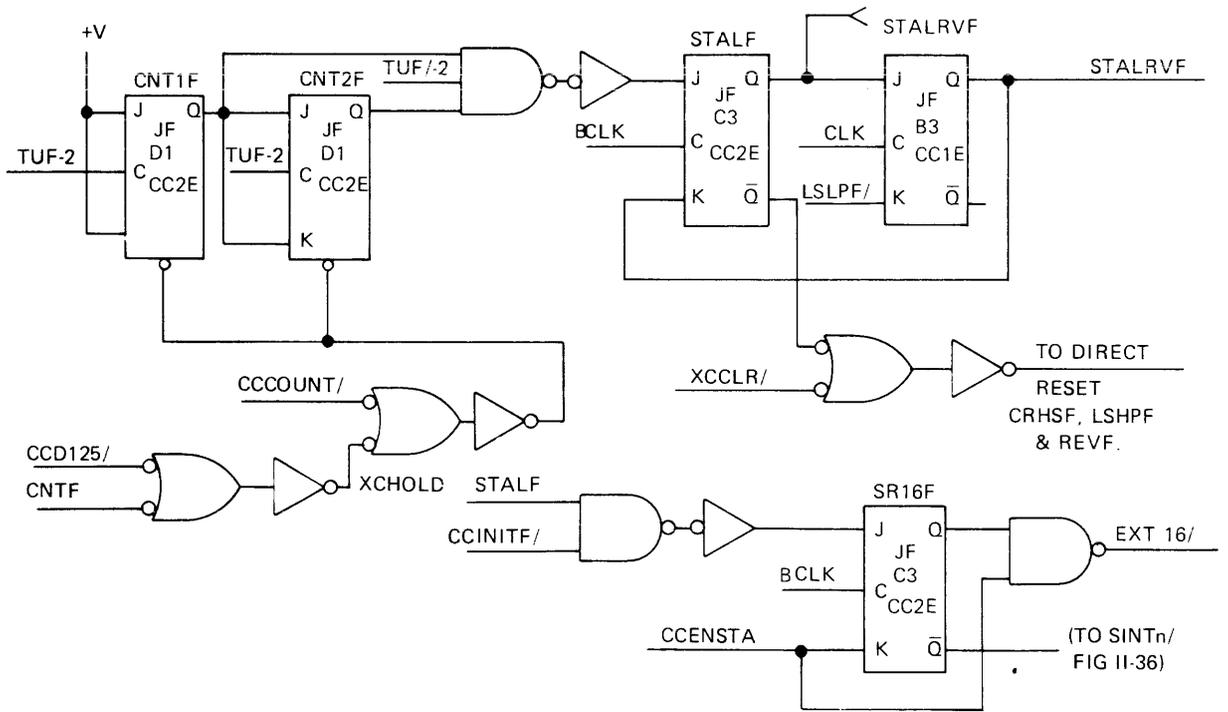Fig. II-36 OVERSPEED FLAG AND STATUS INTERRUPT

Fig. II-37 STALL FLAG

Functional Detail

Fig. II-38 INITIALIZE FLIP-FLOP

Fig. II-39 ESCAPE RIGHT

Fig. II-40 ESCAPE LEFT

Fig. II-41 INTERPOSER AND HIGH POWER CONTROL

Functional Detail

MECH TIMING   30   3   30   3

TUF

PRTU   ENERGIZE
              DECODER
              SOLENOIDS

PEXR/

ENEXR/

EXRF

XCRGR/

CCPRI/   ENERGIZE
              INT. SOL.

CARRIER   2A   4A
POWER   0A

MECHANICAL ACTION

3T 4T   20T   30T   45T   5T
                                                    PRINT HEAD DWELL
CARRIER   38T   IN INDEXED POS.
RELEASED   3T
                                              PRINT HEAD
                                              STRIKES
                                              PLATEN
              PRINT SHAFT
              CLUTCH   CARRIER LIMITS
              RELEASED   ON INTERPOSER
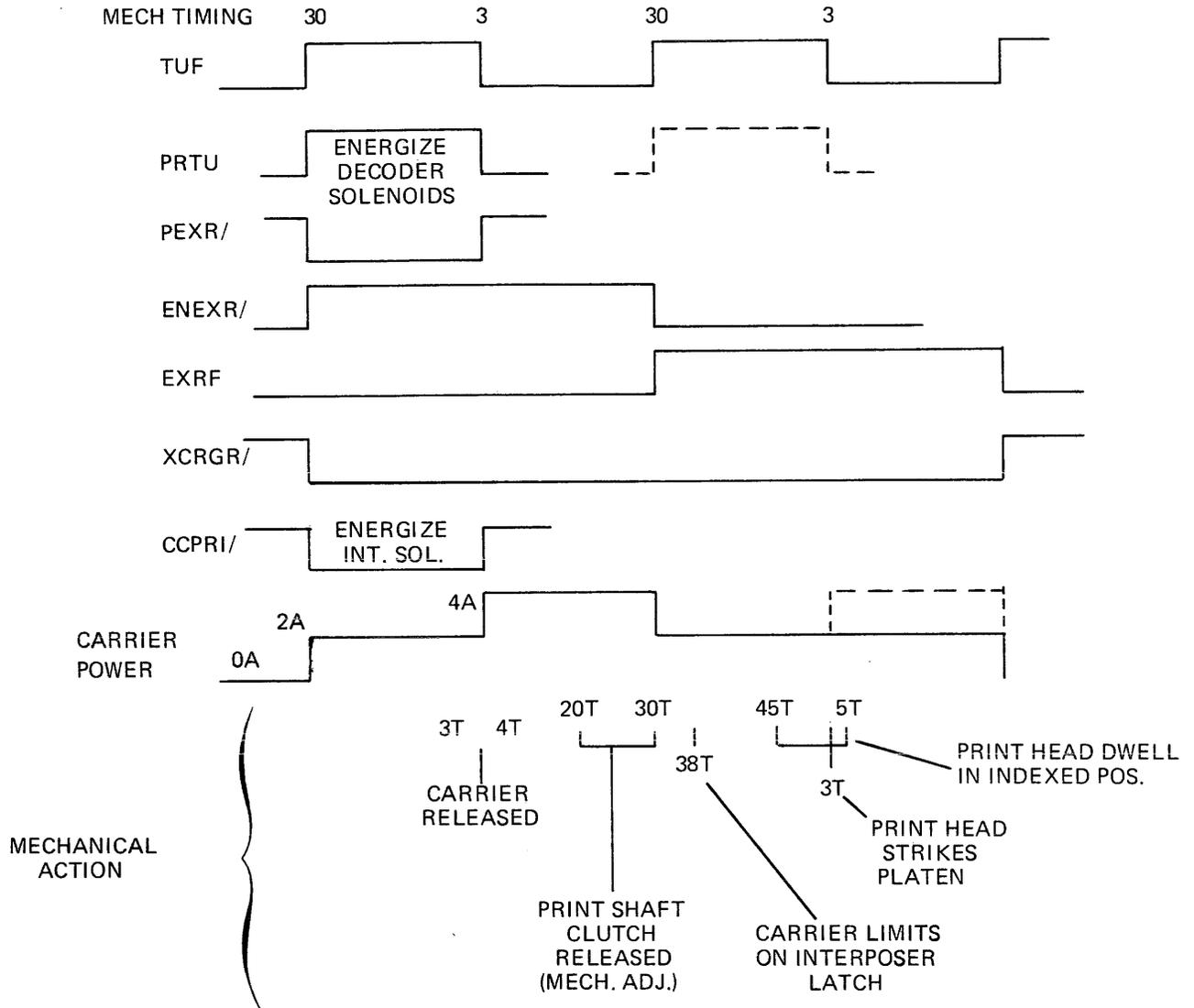   (MECH. ADJ.)   LATCH

Fig. II-42 CARRIER ESCAPE TIMING

STALF set, STALF/ directly resets flip-flops CRHSF, LSHPF, and REVF (Figure II-31). STALF enables the next clock pulse to set flip-flops LSLPF, STALRVF, and SR16F (Figure II-37). A low LSLPF/ resets HOLDF flip-flop (Figure II-30) to drop the carrier interposers and also triggers the 100-millisecond single-shot (Figure II-31).

Signal STALRVF generates REVER to reverse the carrier direction drive signals (CCCRGR/, CCCRGL/, Figure II-35) and enables the next clock pulse to reset flip-flop STALF. When the 100-millisecond single-shot times out, flip-flop LSLPF is reset and enables the next clock pulse to reset flip-flop STALRVF.

When the processor executes an address and status request, or a device read with the instruction bit set, the signal CCENSTA strobes SR16F to EXT16 and enables the resetting of flip-flop SR16F.

Carrier Initialization

When MIR07 is equal to 1 in a carrier data word, it indicates that a low speed movement, in the direction specified by MIR08, is required. As shown in Figure II-38, a high MIR07 enables CCLK and XCARR to set the initialize flip-flop (INITF). Signal CCINITF/ maintains flip-flop SR16F in the reset state, generates a low CCEQ1, and a high CCLTEQ6. This condition causes the carrier to be driven at low speed and high power in the same manner as a move of less than six positions, except that the contents of the data buffer have no effect on the logic. When the carrier contacts the bumper at the end of its travel, the stall logic turns off the carrier drive signals and detents the carrier.

Carrier Escaping

When a print data word is sent to the IOC, MIR05

Functional Detail

MIR 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
    1 1   L   R O C PO AL

PLATEN ADVANCE LEFT⌐
            RIGHT────┘
OPEN TRANSPORT ──────────────┘
CLOSE TRANSPORT ──────────────┘
POWER OFF ──────────────────────┘
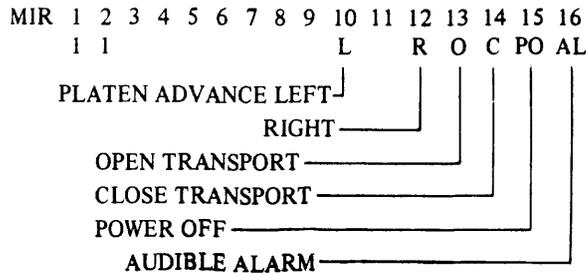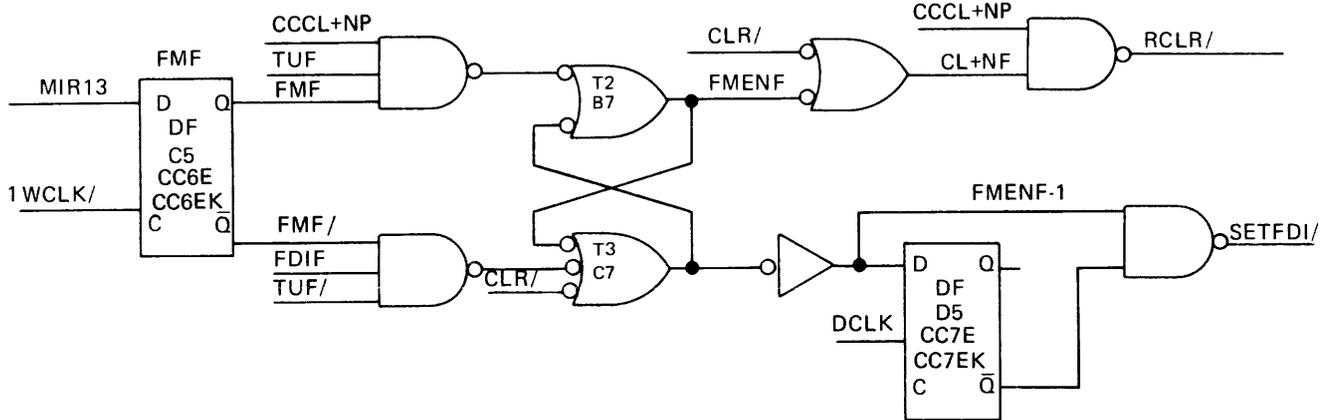AUDIBLE ALARM ─────────────────────┘

Fig. II-43 FORMS DATA WORD

Fig. II-44 FORMS AND FORMS ENABLE FLIP-FLOPS

and MIR06 specify an escape right or escape left. As BRCLK/ loads the printer/forms data register, BRCLK/ also loads MIR05 into a shift register and MIR06 into a flip-flop (Figures II-39 and II-40). If an escape right is specified, PRTU generates a low PEXR/ to set energize escape right flip-flop ENEXR. This action occurs at the same time that PRTU energizes the decode solenoids.

At the next TUF, flip-flop EXRF is set and flip-flop ENEXR is reset. This specifies that unless another print character is loaded into the printer/forms data register, flip-flop EXRF will be reset at the next TUF.

Signals ENEXR/ and EXRF/ are gated to produce a low CCXCRGR/ which turns on the carrier motor drivers. CCXCRGR/ is then gated with TUF/-1 to produce a low CCXCR4A/ to drive the motor at high power when the interposers are withdrawn (Figure II-41). Figure II-42 shows the timing and mechanical actions of a print and escape operation.

Forms Control

To enable the forms data interrupt, the processor sends a control word to the IOC with MIR13 equal to 1. Provided that any previously indexed print operation is complete, the IOC returns forms data interrupt (FDI) to the processor. In order to advance the forms, open or close the forms transport, sound the alarm, or turn processor power off, the processor must wait for the data interrupt,

then execute a device-write to send the data-word to the IOC. The format of the forms data word is illustrated in Figure II-43.

Bits 10 and 12 through 16 are stored in the printer/forms data register. As the register is loaded, the data interrupt is disabled.

Forms Data Interrupt

When a device-write to the console is executed and the instruction bit is set, a single-low going IWCLK/ is enabled by PSWRITn and PSINST1/ (Figure II-11).

When MIR13 is equal to 1, IWCLK/ sets forms flip-flop FMF (Figure II-44). Signal FMF is gated with CCCL+NP and TUF to set flip-flop FMENF. A high CCCL+NP indicates that any previous printer operation has been completed. Signal FMENF produces a low CL+NF, which makes signal RCLR/ high. A high RCLR/ signal disables the master reset from the printer/forms data register (Figure II-14) so that the register can be loaded. A low FMENF/ produces a high FMENF-1, which is gated with the Q̄ output of a D flip-flop to produce a low SETFDI/. On the next clock pulse, the D flip-flop is set; therefore SETFDI/ is low for 1 microsecond.

As shown in Figure II-45, a low SETFDI/ sets the forms data interrupt flip-flop FDI whose output is gated with FMF and FMENF-1 to produce a low FDI/. A low FDI/ causes a data interrupt to be sent to the processor. A
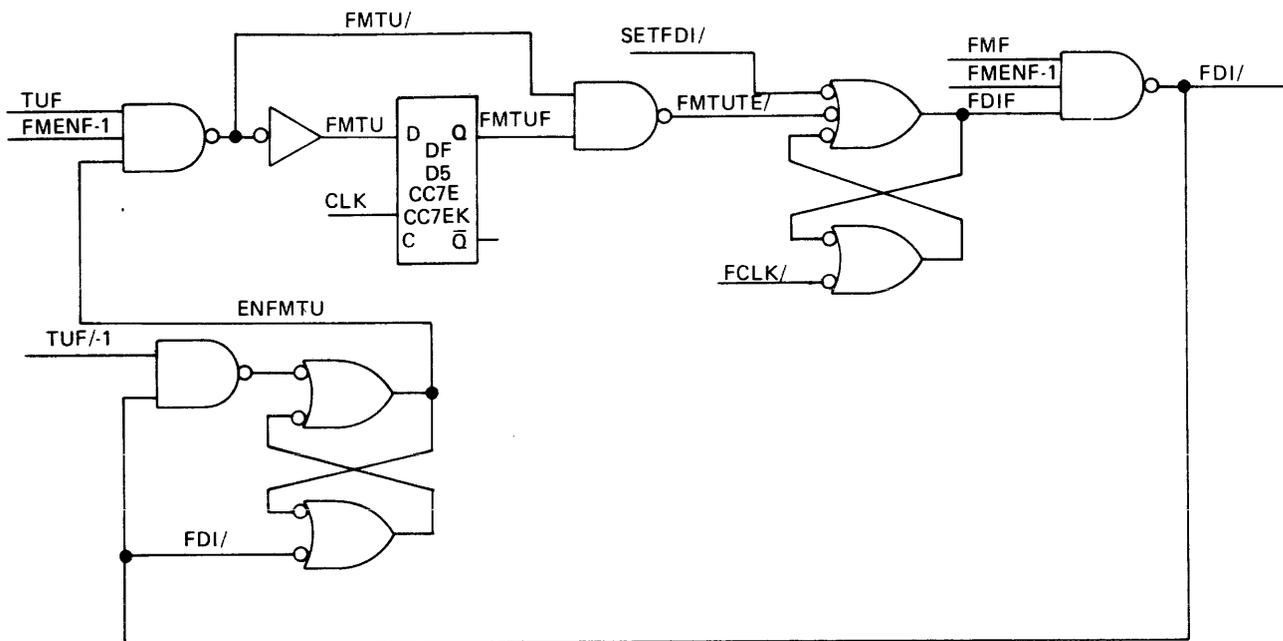
Functional Detail

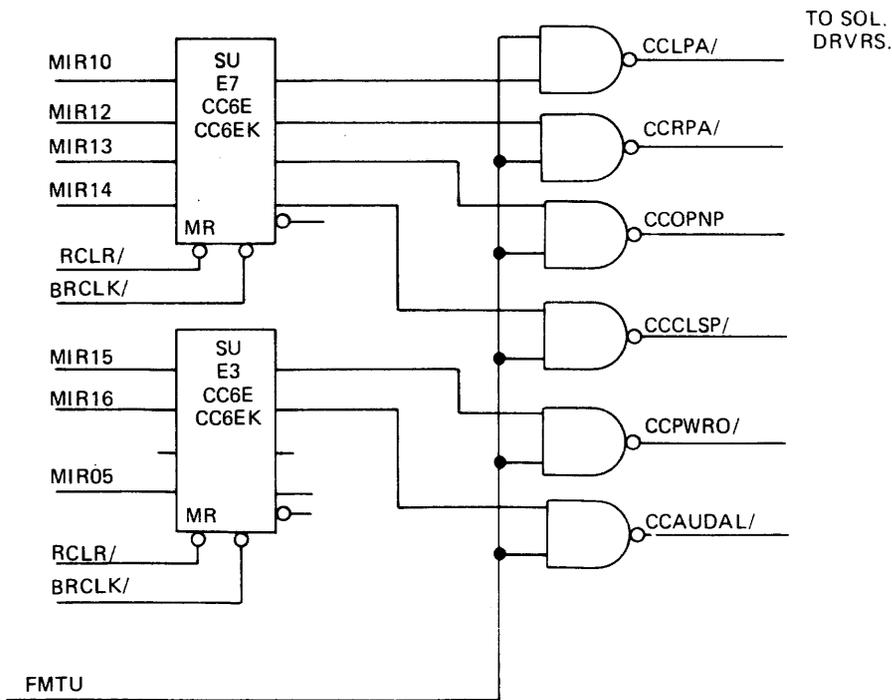Fig. II-45 FORMS DATA INTERRUPT CONTROL

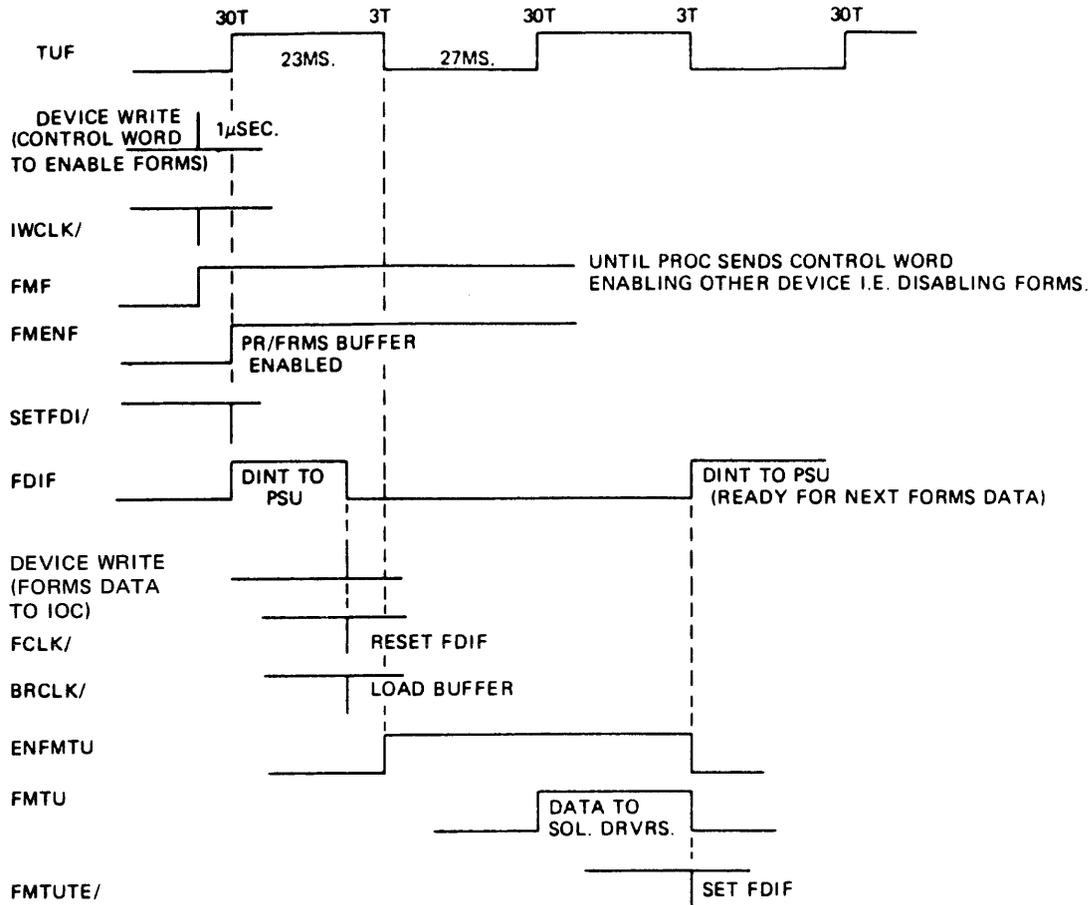Fig. II-46 PRINTER/FORMS DATA REGISTER

Functional Detail

Fig. II-47 FORMS OPERATION TIMING

low FDI/ also resets the ENFMTU flip-flop, causing FMTU to go low.

Forms Data Word

When the processor receives a data-interrupt, the processor may execute a device-write with the instruction bit reset, to transmit the data word to the IOC. When MIR01 and MIR02 are both high, indicating a forms data-word, the signal CCFRMS is generated (Figure II-11). CCFRMS enables two clock pulses: BRCLK/ and FCLK/. BRCLK/ is used to load the printer/forms data register; FCLK resets the FDIF flip-flop (Figure II-45). When TUF goes low, FDI/ and TUF/-1 set the ENFMTU flip-flop, which enables the following TUF to generate signal FMTU.

When FMTU goes high, the contents of the printer/forms data register (Figure II-46) are gated to the solenoid drivers, which remain enabled for 27 milliseconds to initiate the required action. When TUF goes low, FMTU goes low and disables the printer/forms data register. One clock time later, flip-flop FMTUF is reset. Signal FMTUTE/ is low for 1 microsecond to again set flip-flop FDIF. Signal FDIF produces a low FDI/ to initiate another data interrupt to the processor.

When finished with the forms transport, the processor executes a device-write with the instruction bit set and with MIR13 equal to 0. This condition resets the FMF flip-flop (Figure II-44). At the end of a forms operation, FDIF is high and is gated with FMF/ and TUF/ to reset flip-flop FMENF. A low FMENF-1 causes SETFDI/ to go high and to disable any further forms data interrupts.

Figure II-47 illustrates an example of a forms operation to show the relative timing of various signals.

End of Paper Detection (Figure II-48)

The presence of paper in the console is monitored by the separation of two bails by the paper. The absence of paper allows the bails to make contact and applies a ground to the normally-high ENDOPS/ line. With the forms function signal (FMF) present, the end-of-paper flip-flop is set by a low ENDOPS/ signal. When signal CCENSTA is high, signifying status interrogation by the processor, the EXT02 bit of the status word is set. No status interrupt is developed for the end of paper status condition.
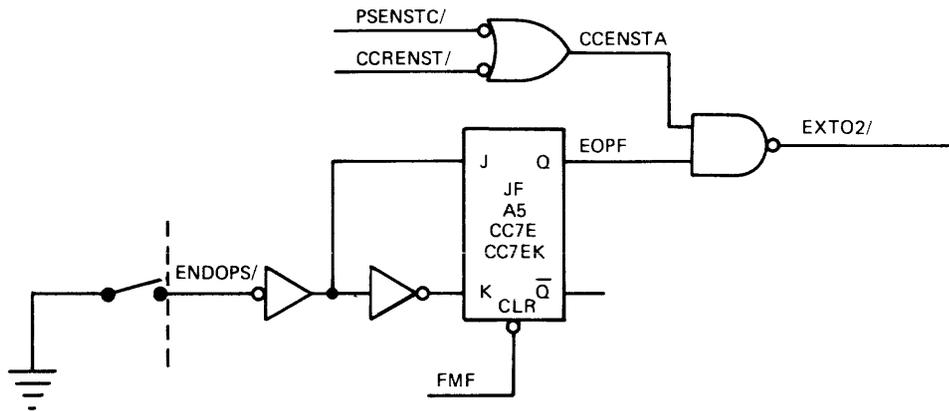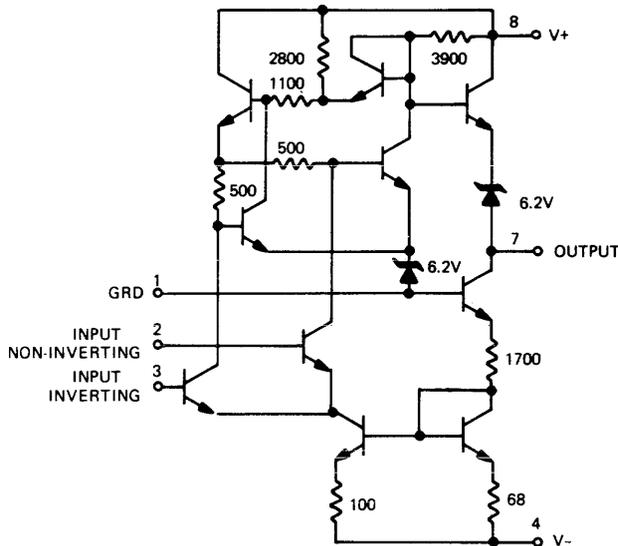
Functional Detail

Fig. II-48 END OF PAGE DETECTION

Circuit Detail

INTRODUCTION

Most of the IC chips (modules) used in the B0346/B0346-1 Console IOC are also used in the B700 Processors. The IC's used in both units are described in the B700 Processor FETM, form 1064482, and the B721 Processor FETM, form 1077534; the IC's unique to the IOC are described in this section.

NOTES:

   1. ALL RESISTANCE VALUES ARE IN OHMS.

   2. PINS 5 AND 6 ARE NOT CONNECTED.

Fig. III-1 DIFFERENTIAL COMPARATOR (1471 4406)

DIFFERENTIAL COMPARATOR (1471 4406)

The differential comparator used in the console IOC is illustrated in Figure III-1. The output at pin 7 is high when the non-inverting input (pin 2) is more positive than the inverting input (pin 3). When pin 2 is less positive than pin 3, the output is low.

QUAD D-TYPE FLIP-FLOP (1449 1278)

The D-type flip-flop module is illustrated in Figure III-2. The flip-flops have a direct clear and complementary Q and Q outputs. Input information is transferred to the outputs on the positive edge of the clock pulse. A low-level signal to the clear input sets Q to a logical 0 level. The clear inputs to each flip-flop are independent of the clock.

RESISTOR MODULE (1447 5396)

The resistor module illustrated in Figure III-3 is comprised of six 402-ohm resistors and six 237-ohm resistors which are arranged such that a variety of resistive values can be tapped at the pins. These resistance values are used for pullup functions.

RESISTOR MODULE (1448 2319)

The resistor module, illustrated in Figure III-4, is comprised of 13 1.5K resistors used as pullup resistors.

LINEAR TIMER (1409 1039)

The linear timer is shown in Figure III-5. This circuit is highly stable and capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free-running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on down-clocks and the output can drive TTL circuits.

When the circuit is connected as shown in Figure III-5, the timer triggers itself and operates as a free-running multivibrator. The external capacitor charges through Ra and Rb and discharges through Rb only. The duty cycle may be precisely set, therefore, by the ratio of these two resistors. In this mode of operation, the capacitor charges and discharges between 1/3 Vcc and 2/3 Vcc. The charge and discharge times, and therefore the frequency, are independent of the supply voltage.
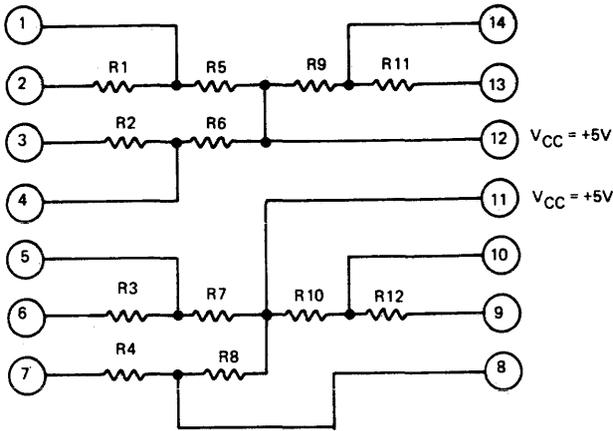
Circuit Detail
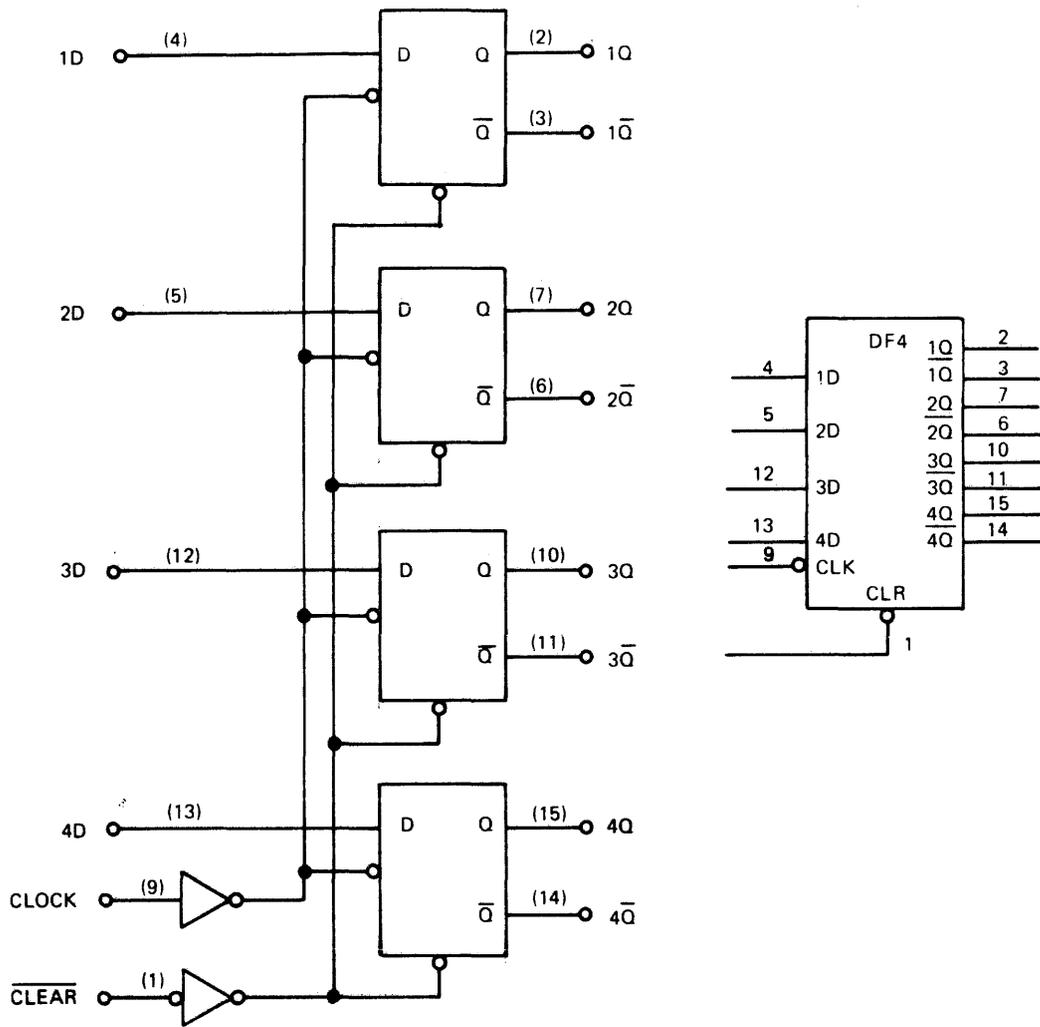
NOTES:

1. NUMBERS IN PARENTHESIS
   INDICATE PIN NUMBERS.

2. V_{CC} IS PIN 16.
   GROUND IS PIN 8.

FUNCTION TABLE
(EACH FLIP-FLOP)

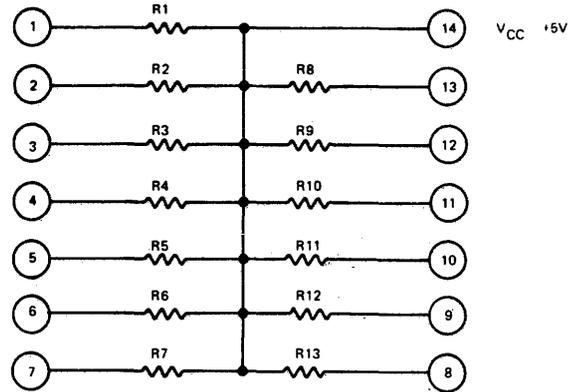| INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$
L	X	X	H	L
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

Fig. III-2 QUAD D-TYPE FLIP-FLOP (1449 1278)

Circuit Detail

RESISTOR NO.	RESISTANCE (25°C)	MAXIMUM OPERATING POWER DISSIPATION (70°C)
R1, R2, R3 R4, R11, R12	402Ω±2%	125 MW
R5, R6, R7 R8, R9, R10	237Ω±2%	250 MW

Fig. III-3 RESISTOR MODULE (1447 5396)

RESISTOR NO.	RESISTANCE (25°C)	MAX. OPERATING POWER DISSIPATION (70°C)
R1 THRU R13	1.5K ±5%	50 MW

Fig. III-4 RESISTOR MODULE (1448 2319)

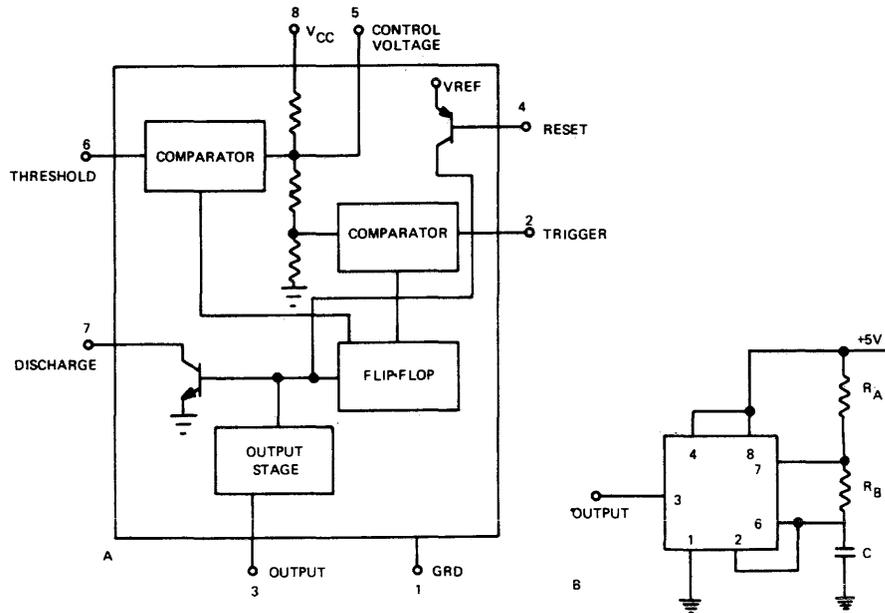
Fig. III-5 LINEAR TIMER (1449 1039)

MAINTENANCE PHILOSOPHY

The approach used in detecting, diagnosing, and repairing failures in the console IOC is to run the appropriate Maintenance Test Routines (MTR's) and then replace or repair defective circuit chips or discrete components in accordance with the diagnostic information obtained from the MTR's. Additional manual diagnostic operations, using this technical manual, FT&R documentation, and test equipment may be required by the Field Engineer to further diagnose and repair failures if the MTR's do not locate the defective component/circuit.

MAINTENANCE AIDS AND EQUIPMENT

The following maintenance aids are required to implement the MTR's and perform maintenance on the IOC:

a.   Field Engineering (F.E.) cards FE-1 through FE-4.
b.   MTR meter.
c.   Tektronix Model 453 oscilloscope.
d.   Processor card extender kit (1447 7102).
e.   Applicable MTR's.
f.   Special maintenance tools (insertion/extraction, wire wrap/unwrap, pin extractor, and card puller tools).

Section V of the B700 Processor Technical manuals, forms 1064482 and 1077534, contain descriptions and identification/application data for the F.E. cards, MTR meter, and card extender kit.

MAINTENANCE TEST ROUTINES (MTR's)

Each B700 system installation is provided a set of MTR's on system-compatible media, tailored to the installation configuration and revision level. The MTR Configuration Document (2601 8200), issued by the respective branch office to each installation, provides a complete list of MTR reference data, including the revision status and applicability.

The MTR provided for the B0346 or B0346-1 console IOC is the ECONMTR (2602 9751). Program listings, complete operating instructions, failure dictionaries, and other data are provided in Operator Instructions Document, 2602 9744.

When implemented, ECONMTR detects and diagnosis failures within the IOC or validates the operation of the IOC and interfacing console. An MTR cannot diagnose a failure in the console, but can be interpreted to indicate or point to a failure in the console.

Note that, for complete diagnosis or validation of the IOC and the console operations, the FEMTMTR, ELDRMTR, PROCMTR, BSWMTR, and MCUMTR must be run in the sequence indicated before the ECONMTR or CONS96MTR is run. Refer to Section V of B700 Processor Technical Manuals, forms 1064482 and 1077534, for descriptions of the MTR implementation and diagnostic process.

Installation Procedures

INSTALLATION PACKAGE

The B0346/B0346-1 console IOC installation package is comprised of the following items:
a.   Twelve printed circuit cards (Table VI-1).
b.   Three frontplane connectors (1534 3940).
c.   Two backplane templates.
d.   One identification decal.

Table VI-1 identifies the IOC circuit cards, their functions and the allocated card slots for the B705/B711 and B721 Processors.

INSTALLATION PROCEDURE

Ensure that all items in the IOC installation package are available, then proceed as follows:
1.   Install cards in card slots for corresponding processor as listed in Table VI-1.

2.   Connect frontplane connectors between card pairs CC1E and CC2E, CC4 and CC5E, CC6E and CC7E (B0346) or CC6EK and CC7EK (B0346-1).
3.   On wiring side of backplane, slide large templates over backplane pins for console IOC location.
4.   On wiring side of the backplane, slide small templates over backplane pins for B705/B711 I/O connectors J89 and J90 or B721 I/O connectors EJ4 and EJ5.
5.   Attach 50-pin connectors of I/O cables which have strain relief brackets to corresponding I/O connectors on insertion side of backplane.
6.   Affix the decal, which identifies the IOC and contains the serial number, to the appropriate card location.
7.   Check +5-volt power as described in +5-Volt Tap Adjustment Procedure in Volume 1 of the Processor FT&R document.
8.   Connect I/O cables to console.
9.   Run appropriate MTR's to ensure proper system operation.

Type	Part No.	Card Slot B721	Card Slot B705/B711
CC0	1479 8839	BD3	DP1
CC1E	2600 5470	BD0	DN8
CC2E	2601 8796	BC7	DN5
CC3E	2600 5058	BB2	DM0
CC4	1447 4415	BA3	DL1
CC5E	2600 5082	BA0	DK8
* CC6E or	* 2600 5116	BC1	DM9
** CC6EK	** 2600 5140	BC1	DM9
* CC7E or	* 2600 5173	BC4	DN2
** CC7EK	** 2600 5207	BC4	DN2
CC8E	2600 5231	BB8	DM6
CC9	1479 0505	BA6	DL4
CC9	1479 0505	BA9	DL7
CC11E	2600 5264	BB5	DM8

NOTES:
*Used with 64-character set (B0346 IOC)
**Used with 94-character set (B0346-1 IOC)

TABLE VI-1 PROCESSOR CONSOLE IOC CARDS AND LOCATIONS

BURROUGHS CORPORATION
DATA PROCESSING PUBLICATIONS
REMARKS FORM

TITLE: B0346/B0346-1 Console I/O Control
Technical Manual

FORM: 1077542
DATE: 1-2-75

CHECK TYPE OF SUGGESTION:

☐ ADDITION   ☐ DELETION   ☐ REVISION   ☐ ERROR

GENERAL COMMENTS AND/OR SUGGESTIONS FOR IMPROVEMENT OF PUBLICATION:

FROM: NAME _____   DATE _____

          TITLE _____

          COMPANY _____
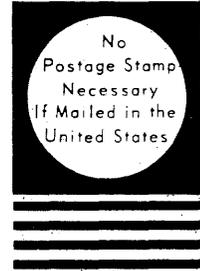
          ADDRESS _____

          _____

STAPLE

FOLD DOWN   SECOND   FOLD DOWN

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by
Addressee
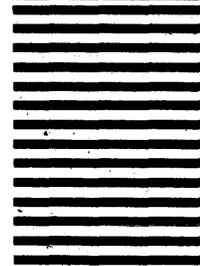
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       Technical Information Organization, TIC-Central

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