OWNER'S MANUAL

Model 2820
System Processor

California Computer Systems

CCS MODEL 2820

SYSTEM PROCESSOR

USER'S MANUAL

MANUAL 89000-02820 REV. A

CALIFORNIA COMPUTER SYSTEMS
250 CARIBBEAN DRIVE
SUNNYVALE CA 94086

The information contained in this manual is believed to be correct at the time of publication. However, CCS assumes no liability resulting from the use of this publication.

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CHAPTER 1

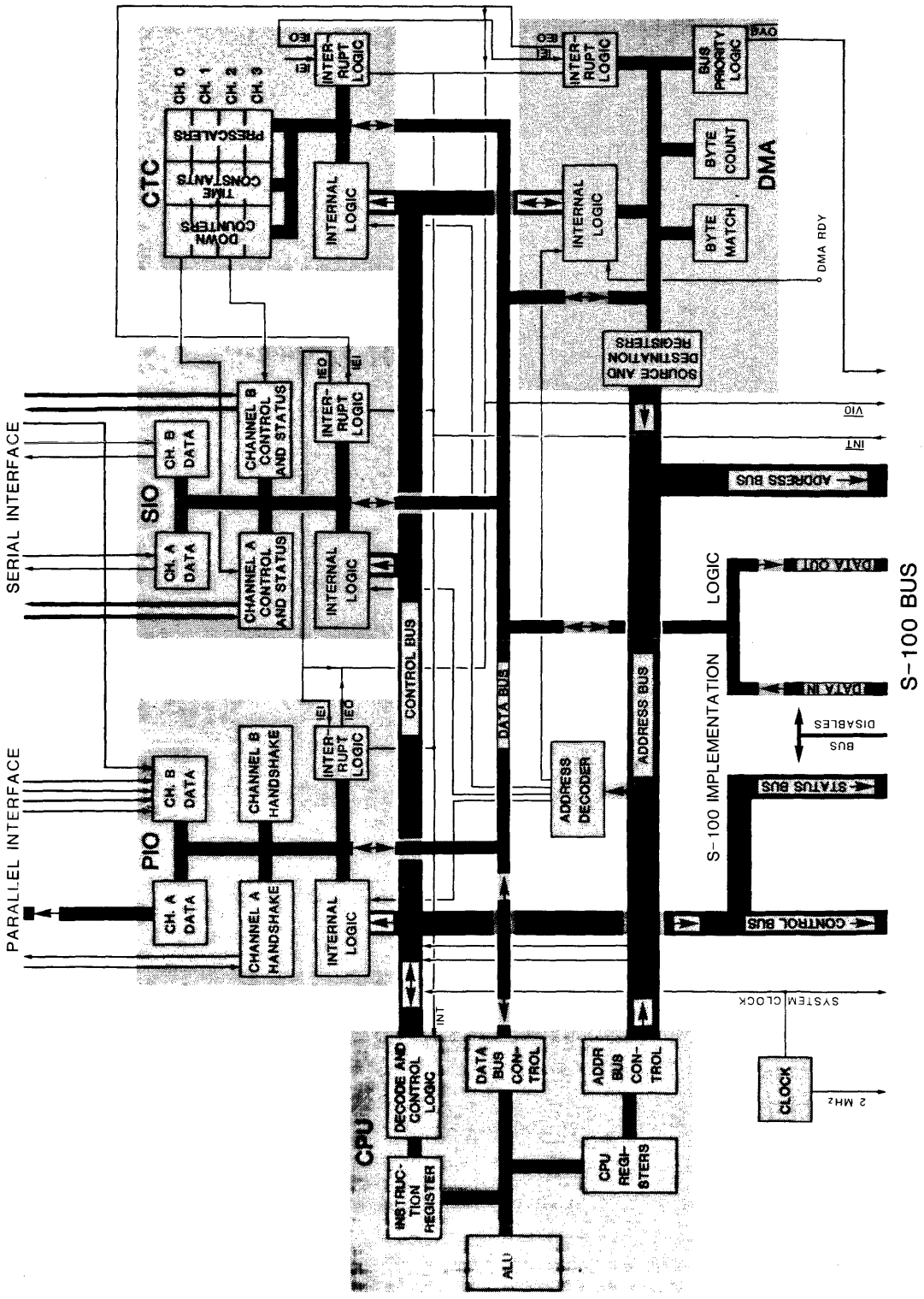
INTRODUCTION

1.1 BASIC FEATURES

The CCS 2820, the central processing unit of the CCS-200, 300, and 400 systems, has been designed to take full advantage of high-performance Z-80 technology. Besides the Z-80 CPU, the board features four devices designed especially for use with the Z-80 CPU: a Parallel I/O Controller (PIO), a Serial I/O Controller (SIO), a Clock Timer Circuit (CTC), and a Direct Memory Access Controller (DMA). The relationships of these devices are shown in Figure 1.1, a block diagram of the 2820. The Z-80 support devices interface with each other with a minimum of external logic. All four peripheral devices participate in an interrupt daisy chain to take advantage of the powerful interrupt-processing capabilities of the Z-80 CPU. The PIO interface is configured for a Centronics-type printer, while the SIO interface meets the RS-232-C specifications.

Much of the circuitry on the 2820 is devoted to implementation of the bus signals, adapting the Z-80 signals to the S-100 bus. Included is a crystal-controlled clock circuit which provides the 2 MHz bus signal and a 4 MHz system clock.

Several hardware-selectable options incorporated on the 2820 provide for flexibility in system configuration. All options are hardwired for the standard configuration, eliminating preliminary set-up procedures, but users who desire to select a non-standard option may easily do so. User-selectable options include peripheral base addresses, non-maskable powerfail interrupts, and automatic wait state generation.



2820 BLOCK DIAGRAM

1.2 USING THIS MANUAL

Most System 2ØØ, 3ØØ, and 4ØØ users will not find it necessary to consult this manual; the information they require is in the System Operation Manual for their particular system. This manual is provided for those who will at some time reconfigure, program, or trouble-shoot the 282Ø. Chapter 2 provides instructions for all of the configuration options of the 282Ø. Full programming instructions for the Z-8Ø family devices are provided in the Programming Guide that is included in the documentation package of each system. However, device implementation often limits the programming options; such limitations of the DMA, SIO, PIO, and CTC on the 282Ø are treated in Chapter 3. Chapter 4 and the schematic and pinouts in Appendix A provide information necessary for trouble-shooting the 282Ø.

IEEE conventions regarding signal names/mnemonics and the identification of low-active signals by an asterisk after the name/mnemonic (e.g., pWR*) are followed throughout the manual.

1.3 SERVICE

If at some point you need to return your 282Ø or other CCS product to the factory for service, first write to the Customer Service Department at the address given below to obtain an RMA (Return Materials Authorization) number. Products returned without an RMA number will be refused by the Shipping and Receiving Department.

Customer Service Department
California Computer Systems
25Ø Caribbean Drive
Sunnyvale Ca 94Ø86

1.4 SPECIFICATIONS

SIZE:

Board:	10" long x 5" wide
Connector:	6.365" long x .3" wide; 2.125" from right of board
Component Ht:	less than .5"

POWER SUPPLY:

+8 Volts	Regulated On-Board to +5 Volts
+16 Volts	Regulated On-Board to +12 Volts
-16 Volts	Regulated On-Board to -12 Volts
Consumption:	@ 600 mA at +8 V. @ 100 mA at +16 V. @ 100 mA at -16 V.
Heat Burden:	116 gram-calories/minute .48 BTU/minute

ENVIRONMENTAL REQUIREMENTS:

Temperature:	0°C. to +70°C.
Humidity:	less than 90%

ON-BOARD DEVICES:

Z-80 CPU
Z-80 Direct Memory Access Controller
Z-80 Parallel Input/Output Controller
Z-80 Serial Input/Output Controller
Z-80 Clock/Timer Circuit
Crystal-Controlled 2 and 4 MHz Clock Circuitry

INTERFACES:

System Bus:	S-100-Based Jumper-Enabled MREQ* and REFRESH* lines
Peripheral:	Two RS-232-C Serial Interfaces: DCE Programmable Baud Rates Re-configurable for DTE Jumperable External Clock, Port B One Parallel Printer Interface Centronics-Type Separate Data and Status Ports Selectable Peripheral Base Addresses

ADDITIONAL FEATURES:

4 MHz Operation
Two Programmable Real-Time Clocks
Jumperable Non-Maskable Interrupt on Power Fail
On-Board Peripheral Interrupt Daisy Chain with
Look-Ahead for Off-Board Expansion
DMA Daisy Chain Capability
Jumper-Enabled Single or Double Wait State
Generation in I/O, Memory, and/or M1 Cycles
Low-Power Schottky and MOS Devices for Minimum
Power Consumption
Sockets for All ICs
Fiberglass Epoxy (FR-4) PC Board
Solder-Masked Both Sides
Gold-Plated Connector Fingers
Silk-Screened Component Outlines, Part Designations,
Reference Numbers

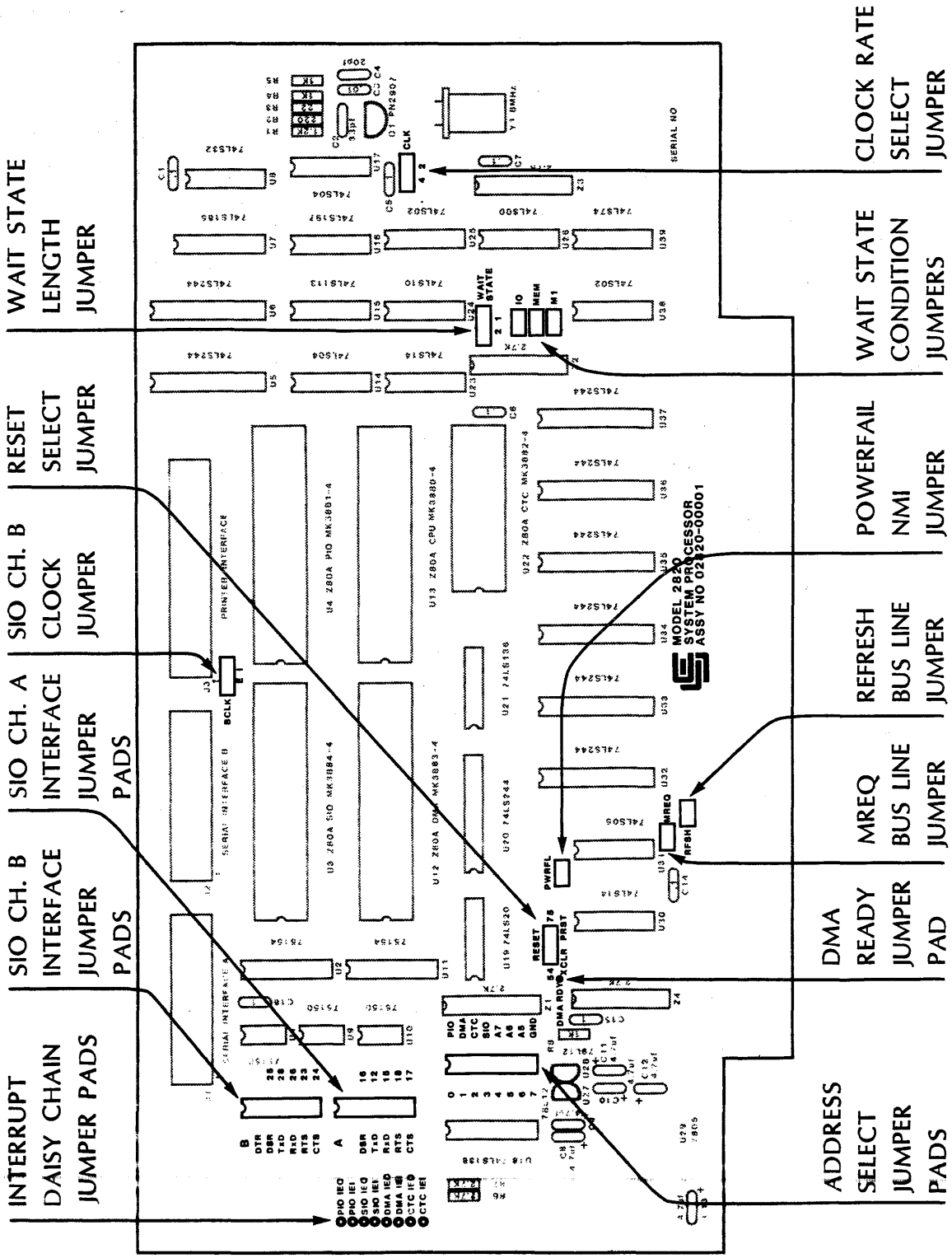
CHAPTER 2

CONFIGURATION

The 282Ø includes a number of user-configurable options. None of these options require configuration before the board can be installed and operated; all are hard-wired for standard operating parameters of Systems 2ØØ, 3ØØ, and 4ØØ. However, jumper pads have been included on the PC board to allow selection of alternatives to some hard-wired features. Selection of non-standard features involves the installation of jumper pins or wires and, in most cases, the cutting of traces on the PC board .

Figure 2.1 illustrates the 282Ø jumper locations. Individual jumpers and headers are illustrated in the descriptive sections that follow.

FIGURE 2.1. JUMPER LOCATIONS



2.1 THE CLOCK JUMPER

This jumper, present on some versions of the 2820, controls the system clock rate and is hard-wired for 4 MHz operation. Most users will want to take advantage of the Z-80's ability to operate at 4 MHz. However, users who have a specific hardware or software requirement for 2MHz operation may select a 2 MHz system clock by cutting the trace between the middle and 4 MHz pads and installing a jumper wire between the middle and 2 MHz pads. Figure 2.2 illustrates the CLK jumper configured for a 2 MHz system clock.

FIGURE 2.2

2.2 THE WAIT CONDITION AND LENGTH JUMPERS

The CPU's WAIT* input can be forced low by any one of three signals. The first two, RDY and XRDY, are bus lines controlled by peripheral devices. The third signal is produced on-board the 2820 and controlled by four jumpers. Three wait condition jumpers, M1, IO, and MEM, allow insertion of waits in every machine cycle of a given type. From 0 to 3 of these jumpers may be installed, allowing wait state generation to be tailored to the elements of a system. For example, because in M1 cycles the memory access time is about one half clock cycle shorter than in a memory read or write cycle, waits may be desired only during M1 cycles.

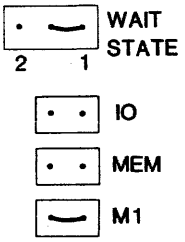


FIGURE 2.3

The WAIT STATE jumper selects the number of wait cycles--1 or 2--to be inserted. This jumper controls length of the wait state for all waits enabled by the wait conditon jumpers but does not affect wait states generated when either RDY or XRDY is forced low.

As shipped, the 2820 is configured for no wait generation, and no wait states will be necessary for any CCS system components. However, some non-CCS components may require waits. In Figure 2.3, a wait of one clock cycle in duration is selected for all M1 cycles; no other waits occur unless generated off-board.

2.3 THE RESET JUMPER

All devices on the 2820 share a common reset signal: either RESET* (bus pin 75) or EXTERNAL CLR* (bus pin 54), depending on the Reset jumper. Both of these signals are controlled by the motherboard in the 2220 mainframe; see the 2220 manual for an explanation of the generation of the signals. The 2820 is hard-wired to use EXT CLR* as its reset signal. Users who desire to reset the 2820 with the RESET* signal may cut the EXT CLR* trace and install a jumper wire as illustrated in Figure 2.4.

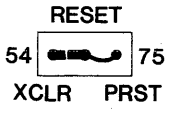


FIGURE 2.4

2.4 THE POWERFAIL JUMPER

The PWRFAIL* bus line, controlled by circuitry on the motherboard, gives the CPU notice of an imminent power failure. The PWRFL jumper allows this bus line to be connected to the CPU's NMI* (Non-Maskable Interrupt) input. This provides for an immediate and unconditional jump, whenever the power is about to fail, to an interrupt routine which will ensure an orderly halt to the system's operations.

FIGURE 2.5

On the 2820 as shipped from the factory, PWRFL is disabled; CCS system software does not support the PWRFL option. However, some users may choose to add a Powerfail routine to their systems. Figure 2.5 illustrates the PWRFL option enabled.

2.5 THE REFRESH AND MREQ JUMPERS

The jumpers labeled RFSH and MREQ enable REFRESH* and MREQ* signals on bus lines 66 and 65 respectively. REFRESH* is used by a number of dynamic RAM boards including the CCS 2065, which is part of Systems 300 and 400. Because most users will want to enable REFRESH*, the jumper is hard-wired to enable the line. To de-select the REFRESH* bus line, cut the trace between the two jumper pads.

The MREQ* bus line is less commonly used, but is required by some memory boards. To enable the MREQ* line, install a jumper wire between the two jumper pads.

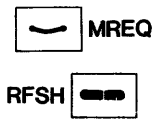


FIGURE 2.6

As shipped from the factory, the 282Ø enables REFRESH* and disables MREQ*. Figure 2.6 shows REFRESH* disabled and MREQ* enabled.

2.6 THE SIO BCLK JUMPER

SIO Port B's transmitter and receiver clocks share one input. The BCLK jumper allows that input pin to be controlled either on-board, by CTC Channel 2, or offboard, by the peripheral via interface line TSEC (DCE). When SIO Port B is used as shipped (as DCE), or as DTE in asynchronous mode, the on-board (I for Internal) clock should be used; therefore the BCLK jumper is hard-wired for the I option. If Port B is reconfigured as DTE and used in synchronous mode, the clock should be generated by the DCE, and therefore the BCLK jumper should be wired for the E (External) option.

To enable the external clock, cut the I trace and install a jumper wire between the middle and E pads, as illustrated in Figure 2.7.

FIGURE 2.7

2.7 THE ADDRESS SELECT JUMPERS

The base addresses of the four Z-8Ø peripheral devices on board the 282Ø are determined by the configuration of the Address Select Jumpers as follows: 1) all devices are located within a 32-address block determined by address bits A7-A5; 2) each device occupies a 4-address block determined by A4-A2; 3) devices need not be addressed contiguously or in any special order; and 4) unused addresses in the 32-address block may be used by off-board devices without interference from the 282Ø. As shipped, the 282Ø is configured for the following addresses: PIO, 1ØH-13H; DMA, 14H-17H; CTC, 18H-1BH; SIO, 1CH-1FH. These addresses are all used by the system software; therefore, it is unlikely that the user will have occasion to change the base addresses. However, the option is available for those who desire it.

Figure 2.8 illustrates the Address Select Jumpers. To select the 32-address block in which the four peripheral devices will reside, solder a wire from the appropriate address bit pad(s), labeled A7-A5, to the GND pad as indicated by Table 2.1 (i.e., ground the pad corresponding to each digit that is a 1). To select a 4-address block to be occupied by a given device, solder a jumper wire from the header pad labeled for that device to the appropriate pad on the left side of the header as indicated by Table 2.1. The configuration illustrated in Figure 2.8 assigns addresses to the Z-80 peripherals as follows:

PIO: 10000000-10000011 (80-83H)
DMA: 10000100-10000111 (84-87H)
CTC: 10001000-10001011 (88-8BH)
SIO: 10001100-10001111 (8C-8FH)

TABLE 2.1.
BASE ADDRESS SELECTION

BASE	GROUND
00000000	None
00100000	A5
01000000	A6
01100000	A6, A5
10000000	A7
10100000	A7, A5
11000000	A7, A6
11100000	A7, A6, A5

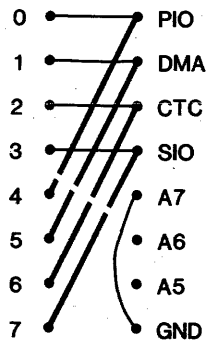


FIGURE 2.8

2.8 THE DMA RDY PAD

The RDY input to the Z-80 DMA Controller is used by I/O devices to signal that they are ready for a DMA operation. The DMA RDY pad is provided so that appropriate lines from on-board or off-board devices may be connected to the DMA RDY input at the user's discretion. Use of this pad is not mandatory, as the RDY signal may be forced via software and is not used at all in memory-to-memory operations. When the pad is not used, the RDY input is held high. Whether the RDY pin is active high or active low is controlled by software.

The RDY pad is located immediately to the left of the RESET jumper, as illustrated in Figure 2.1.

2.9 THE SIO INTERFACE JUMPERS

Both SIO Port Interfaces are RS-232-C-compatible and are hard-wired as Data Communication Equipment (DCE). However, provision has been made for either port to be configured as Data Terminal Equipment (DTE). On the left side of the 282Ø there are two sets of 14 pads each, arranged 2 x 7 and labeled A and B for Ports A and B. To configure a port for DTE, cut the traces between the bottom four pairs of pads and install jumper wires in a criss-cross pattern. Figure 2.9 shows Port B configured as DCE and Port A as DTE. If Port B is to be configured as DTE, the DTR and DSR traces should also be cut and criss-cross jumper wires installed.

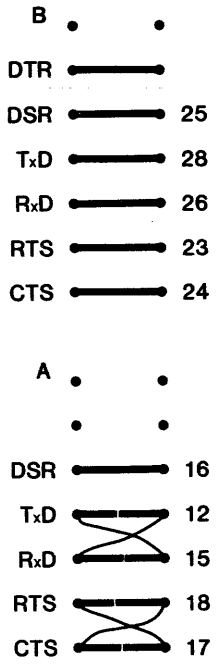


FIGURE 2.9

2.1Ø THE INTERRUPT DAISY CHAIN PADS

The interrupt daisy chain of on-board Z-8Ø peripherals is hard-wired as illustrated in Figure 2.1Ø but may be altered by the user. The hard-wired priority, from highest to lowest, is CTC, DMA, SIO, PIO. To re-configure the daisy chain, cut the necessary traces and install the necessary jumper wires so that: 1) the IEI of the highest-priority device is connected to a pull-up resistor; and 2) the IEO of the first-priority device is connected to the IEI of the second-priority device, the IEO of the second-priority device is connected to the IEI of the third-priority device, and the the IEO of the third-priority device is connected to the IEI of the fourth-priority device.

The traces between higher-priority IEOs and lower-priority IEIs, illustrated in Figure 2.10, are on the circuit side of the board. The IEI of the CTC is connected to pin 2 of resistor pack Z1 on the component side of the board. To give another device highest priority, first cut the trace from Z1 pin 2 before it connects with the trace from the CTC IEI pad, then jumper the IEI pad of the new highest-priority device to pin 2 of Z1.

FIGURE 2.10

CHAPTER 3

PROGRAMMING INFORMATION

A general guide to programming the Z-8Ø devices has been included with your system. The Programming Guide discusses the full range of programming options for each device. However, in many cases the implementation of a device on a given board will limit the options available to the programmer. This chapter describes the limitations and special features of the Z-8Ø devices on the 282Ø from the programmer's point of view.

3.1 THE CPU

The 282Ø's CPU will respond to all Z-8Ø instructions as described in the General Programming Guide and other publications treating Z-8Ø programming.

3.2 THE DMA CONTROLLER

In the factory configuration, the DMA's base address is 14H. It will respond to any address between 14H and 17H.

Except for the following minor limitations, the DMA Controller on the 282Ø may be programmed as described in the General Programming Guide and other publications.

2820-UNIQUE PROGRAMMING CHARACTERISTICS:

1. The CE*/WAIT* option is not available; the CE* input is controlled by the address-decoding logic only. Therefore Bit 4 of Command Register 4 should always be cleared.

2. Unless the DMA RDY pad is jumpered by the user to the appropriate signal from an I/O device, the Force Ready command (written to Command Register 5) must be used for all DMA operations.

3. No circuitry on the 2820 or other CCS system board takes advantage of the pulse which may be generated at the INT* output after every 256 bytes are accessed. Therefore Bits 2 and 3 of the Interrupt Control Register should be cleared.

3.3 THE PIO

As configured at the factory, the PIO resides at base address 10H. The addresses for the four separate ports are as follows:

Channel A Data:	10H
Channel A Command:	11H
Channel B Data:	12H
Channel B Command:	13H

The PIO on the 2820 is hardware-configured as a Centronics-type printer interface; therefore the programming options are considerably limited.

2820-UNIQUE PROGRAMMING CHARACTERISTICS:

1. Port A is used for outputting the data to the printer and therefore should be programmed for Mode 0 (Bits 7-6 of Command Register 0 cleared). Handshaking is handled by ARDY and ASTB* automatically; neither signal is accessible to the programmer.

2. PIO Port B is used for four printer status inputs, and also for SIO Port B's DTR input, necessary for synchronous operation of SIO Port B. The status byte format is shown at the right.

Bit Ø: FAULT*
Bit 1: BUSY
Bit 2: PAPER EMPTY
Bit 3: SELECT
Bit 4: Always Ø
Bit 5: Always Ø
Bit 6: Always Ø
Bit 7: SIO B DTR*

Port B should therefore be programmed for Mode 3 operation, with all bits programmed as inputs and the bits not being used (Bits 7-4 when the PIO is addressed and Bits 6-Ø when SIO Port B is addressed) set to 1 in the Mask Register.

3. The printer is reset via the INPUT PRIME* line whenever the 282Ø is reset. INPUT PRIME* is not controllable from software.

4. Use of PIO Port 2 Bit 7 is discussed in the SIO section.

3.4 THE CTC

As configured at the factory, the CTC resides at base address 18H. The four channels of the CTC are addressed as follows:

Channel Ø: 18H
Channel 1: 19H
Channel 2: 1AH
Channel 3: 1BH

The CTC is implemented on the 282Ø for a special purpose: Channel Ø provides the SIO Port A receiver and transmitter clocks; Channel 2 does the same for SIO Port B.

282Ø-UNIQUE PROGRAMMING CHARACTERISTICS:

1. All Clock/Trigger inputs are connected to the 2 MHz clock, eliminating the counter option; unless the wiring is modified, all four channels operate only as timers. Therefore Bit 6 of each Command Register should always be programmed with a Ø. Bit 4 should be programmed with a 1; Bit 3 is a don't-care bit.

2. Because Channels Ø and 2 are used for baud rate generation only, interrupts must be disabled for Channels Ø and 2.

3. Channels 1 and 3 may be used only in the interrupt mode and, unless an event-dependent trigger signal is jumpered in, only as real-time timers. However, if a signal from an external device is jumpered to the CLK/TRG input of a channel, that channel can be used in the counter mode by the external device to generate interrupt requests.

3.5 THE SIO

As configured at the factory, the SIO resides at base address 1CH. The separate ports are addressed as follows:

Channel A Data:	1CH
Channel A Command:	1DH
Channel B Data:	1EH
Channel B Command:	1FH

The SIO programming options are only slightly limited by the implementation of the chip on the 282Ø.

282Ø-UNIQUE PROGRAMMING CHARACTERISTICS:

1. The WAIT*/READY* pins are not connected, so Bit 7 of Command Register 1 should be programmed with a Ø for both ports; Bits 6 and 5 of the same register are then don't-care bits.

2. The SYNCA* and SYNCB* pins are not connected; therefore, External Synchronization mode should not be selected (i.e., Command Register 4 Bits 5-4 should not both be 1).

3. The SIO is configured as DCE, but either or both channels may be re-configured as DTE at the discretion of the user (see Chapter 2 for details). SIO pins and register bits are named assuming that the SIO is used as DTE; therefore the programmer will need to remember that transmit and receive are from the SIO's point of view in the Programming Guide, but from the peripheral's point of view in the RS-232-C specifications. The

SIO interface pins are connected to RS-232-C lines as follows:

RS-232-C	PORT A		PORT B	
	DCE	DTE	DCE	DTE
TxD	RxA	TxA	RxB	TxB
RxD	TxA	RxA	TxB	RxB
RTS	CTSA	RTSA	CTSB	RTSB
CTS	RTSA	CTSA	RTSB	CTSB
DSR	DTRA	XXXX	DTRB	PIO B7
RLSD	DCDA	XXXX	DCDB	XXXX
DTR	XXXX	XXXX	PIO B7	DTRB
TSEC (DCE)	XXXX	XXXX	XXXX	RxTxCLK

4. The DTR interface line for Port B, needed for synchronous interfacing, is inverted and made available at Bit 7 of Port B of the PIO. The DTR signal can thus be monitored by a read of PIO Port B, or the PIO may be programmed to interrupt when DTR goes active. Port A has no DTR interface line.

5. An external clock may be brought in on interface line TSEC (DCE) to control the Port B Rx and Tx Clocks if Port B is reconfigured for DTE. The jumpers involved are discussed in Chapter 2.

6. SIO pins CTSA*, CTSB*, DCDA*, and DCDB* can be programmed as auto-enables, the CTS* pins enabling a channel's transmitter when low, the DCD* pins enabling a channel's receiver when low. Note that this means that the RTS and RLSD interface lines (DCE configuration) are the auto-enable lines, not RTS and DTR as might be expected.

CHAPTER 4

HARDWARE DESIGN

This chapter gives a general description of the 2820 hardware. Because Z-80-family devices are software-intensive, much of the detail concerning the board's operation is presented in the General Programming Guide included in the documentation package with Systems 200, 300, and 400. Also, in the case of such specialized functions as wait request generation, details are more properly left to the schematic, which makes the circuitry clearer than a verbal description could. Therefore, this chapter aims at a sound general description of the relationships between the Z-80-family devices, going into detail only when some special feature of the board warrants.

4.1 THE Z-80 CPU

The 2820 features a Z-80A CPU, a third-generation microprocessor that offers a large and powerful instruction set and fast 4 MHz operation. The instruction set and a discussion of the Z-80 CPU registers are included in the CPU section of the Programming Guide. The CPU inputs and outputs are defined in Table 4.1.

4.2 Z-80 FAMILY INTERFACING

Z-80 family devices are designed to operate together with a minimum of external logic. The PIO, SIO, CTC, and DMA peripheral devices all have inputs M1*, IORQ*, RD*, and RESET*; these are controlled by the corresponding CPU

TABLE 4.1. CPU INPUTS AND OUTPUTS

SIGNAL	FUNCTION
A15-A0	During memory cycles, A15-A0 hold a valid memory address. During I/O cycles, A7-A0 hold a valid I/O address. During memory refresh time, A7-A0 hold the refresh address.
BUSRQ*	Bus Request is used by bus slaves to request control of the bus from the CPU.
BUSAK*	Bus Acknowledge indicates that the CPU's data, address, and control buses are in their high-impedance state; a bus slave may take control.
D0-7	The bi-directional data pins connect directly to the 2820 internal data bus.
M1*	This output indicates an op code fetch cycle. Both M1* and IORQ* low indicates an interrupt acknowledge by the CPU.
MREQ*	This output is pulled low when a valid memory address is present on A15-A0.
IORQ*	This output is pulled low when a valid I/O port address is present on A7-A0.
RD*	Read low indicates that the CPU expects valid data on the bus by a memory or I/O device.
WR*	The Write signal indicates when the CPU has placed valid data on the bus.
RFRSH*	This output low indicates that a dynamic memory refresh is occuring and that other signals should be appropriately interpreted.
HALT*	This output low indicates that the CPU has executed a HALT instruction and is now executing NOPs while waiting for an interrupt.
WAIT*	The CPU enters wait states during any cycle in which, and for as long as, this signal is low.
INT*	If interrupts are enabled, the CPU acknowledges an interrupt request when this input goes low.
NMI*	The Non-Maskable Interrupt input allows for higher-priority interrupts than INT*. NMI* cannot be disabled by software.
RESET*	Controlled by the S-100 RESET line, this input line disables interrupts, sets the interrupt mode to 0, and clears the I and R registers.
CLK	This is the CPU's system clock input.

outputs. The CPU INT* input is controlled by the INT* outputs of the Z-80 peripherals, which are open-collector and therefore may be tied together without buffers. Chip Enable and Port/Register Select inputs are usually controlled by the low-order address bits, the Select inputs directly by A1-A0 and CE through some kind of decoding scheme. (See Section 4.8 for a discussion of the 2820's address decoding scheme.) The DMA's IORQ* and RD* signals, along with MEMRQ* and WR*, are actually bi-directional, so that when the DMA has control of the bus it can duplicate the necessary CPU outputs. All Z-80 devices also share a common bi-directional data bus for data and command transfers. The inputs and outputs which make possible the Z-80's special Interrupt Daisy Chain are discussed in Section 4.7.

4.3 THE PIO

The Z-80 PIO consists of two independently programmable data channels for input or output in byte or bit modes, each channel including two-line Ready/Strobe handshaking. On the 2820 the PIO is implemented as a Centronics-type printer interface. Channel A is used in the output mode as the data channel. Its handshake lines, ASTB* and ARDY*, are connected to interface lines ACKNOWLEDGE* and DATA STROBE* respectively; shift register U?? is used to ensure that DATA STROBE* is 1 microsecond in duration. Channel B is used in the input mode as a Status Register, with status bits FAULT*, BUSY, PAPER OUT, and SELECT made available as BITS 0, 1, 2, and 3 respectively. Bits 4-6 are grounded. Bit 7 is used for the DSR interface line of SIO Port B and will be discussed in Section 4.4. The printer reset signal, INPUT PRIME*, is controlled by the 2820's internal reset line.

Table 4.2 defines the PIO inputs and outputs. One input, however, deserves special discussion: M1*. Due to pin constraints, M1*, along with its normal function, is also used as the PIO's reset input. A reset signal is distinguished from an M1* signal by duration: the signal is interpreted as a reset signal if it is significantly longer than a normal M1 signal. Therefore, the on-board M1* signal from the CPU has been ORed with the board's reset signal; either one going low gives a low to the M1* inputs of the four on-board Z-80 peripherals. M1* active during resete does not affect the other Z-80 devices on the board. The bus signal sM1 does not carry the reset signal; therefore, any other board in the system employing a PIO must therefore provide reset logic similar to that provided by the 2820.

For PIO programming instructions, see the Programming Guide and Chapter 3 of this manual.

TABLE 4.2. PIO INPUTS AND OUTPUTS

SIGNAL	FUNCTION
CE*	When Chip Enable is low, data is read from or written to the PIO during I/O cycles. CE* is controlled by the address select circuitry.
B/A*	This input, controlled by A0, determines whether Channel A or Channel B is selected.
C/D*	This input, controlled by A1, determines whether a control or data transfer will occur.
D0-7	The bi-directional data pins connect directly to the 2820 internal data bus.
IORQ*	Controlled by CPU output IORQ*, this pin low and CE* low indicate that a control/data word is to be gated from or onto the data bus.
M1*	M1*, controlled by CPU output M1* ORed with SLV CLR*, serves two purposes. If both M1* and IORQ* are active, the CPU is acknowledging an interrupt. If M1* is active and both RD* and IORQ* are inactive, the PIO is reset.
RD*	This input determines the direction of data transfer between the CPU and the PIO.
A7-0 B7-0	These lines form the bi-directional data buses for each channel.
STRBA* STRBB*	The handshake strobe STRBA* is used as the printer Acknowledge input; STRB* is not used.
RDYA RDYB	The Ready handshake output RDYA is delayed and lengthened to strobe data into the printer; RDYB is not used.
CLK	This is the PIO's system clock input.
INT* IEI IEO	See Section 4.7 for a discussion of these interrupt daisy chain signals.

4.4 THE SIO

The Z-80 SerialInput/Output Controller provides the 2820 with two extensively programmable synchronous/ asynchronous serial ports capable of serial-to-parallel and parallel-to-serial data conversions in all common protocols. The SIO ports' handshaking is implemented according to RS-232-C specifications. Both ports are hard-wired to operate as DCE. RS-232-C lines supported by both ports include Protective and Signal Grounds, TxD, RxD, CTS, RTS, DSR, and RLSD. DTR and TSEC (DCE) are supported by Port B only. DTR, which is not honored by the SIO, can be monitored at Bit 7 of PIO Channel B. TSEC may be jumpered to control the Port B Rx and Tx clocks (which are otherwise controlled, as the Port A clocks are, by the on-board CTC: see Section 4.5). See Section A.3 for pinouts of the RS-232-C connectors at the back of the mainframe.

Table 4.3 identifies the SIO inputs and outputs. Chapter 2 includes information on re-configuring the interface for either port as DTE. Instructions for programming the SIO are provided in the Programming Guide and in Chapter 3 of this manual.

4.5 THE CTC

The Z-80 Counter/Timer Circuit is implemented on the 2820 as a timer only. It can provide 512 different clock rates for each SIO port and may also be programmed for real-time CPU interrupts. Of its four independently-programmed channels, channels 0 and 2 provide both receiver and transmitter clocks for SIO ports A and B respectively, while channels 1 and 3 can be programmed to interrupt at intervals of from .008 to 32.8 milliseconds.

Timer rates are the product of the 2 MHz clock period, a prescaler (16 or 256), and a time constant (1 to 256). The downcounter is loaded with the value specified in the time constant register. The prescaler circuit, programmable for each channel, counts either 16 or 256 clock cycles, then decrements the downcounter. When the downcounter reaches zero a high pulse is output on the corresponding ZC/TO pin and the downcounter is automatically reloaded. Each channel can be programmed to generate an interrupt request when its downcounter reaches zero.

TABLE 4.3. SIO/O INPUTS AND OUTPUTS

SIGNAL	FUNCTION
CE*	When Chip Enable is low, data is read from or written to the SIO during I/O cycles. CE* is controlled by the address select circuitry.
B/A*	This input, controlled by A0, determines whethere Channel A or Channel B is selected.
C/D*	This input, controlled by A1, determines whether a control or data transfer will occur.
D0-7	The bi-directional data pins connect directly to the 2820 internal data bus.
IORQ*	As an input controlled by CPU output IORQ*, this pin and CE* low indicate that a control or data word is to be gated from or onto the data bus.
M1*	When M1*, controlled by CPU output M1*, and IORQ* are both low the CPU is acknowledging an interrupt.
RD*	This input determines the direction of data transfer between the CPU and the SIO.
TxDA TxDB	Serial data at TTL levels is output to interface lines RxD.
RxDA RxDB	Serial data at TTL levels is input at these pins via the TxD interface lines.
CTSA* CTSB*	The Clear To Send inputs, connected to the RTS interface lines, may be programmed as transmitter auto-enable or general-purpose signals.
RTSA* RTSB*	The Request to Send outputs are connected to the CTS interface lines. In sync mode they are under software control; in async mode they go high when the transmitter is empty.
DCDA* DCDB*	The Data Carrier Detect inputs, connected to the RLSD interface lines, may be programmed as receiver auto-enable or general purpose inputs.
DTRA* DTRB*	The Data Terminal Ready outputs are controlled by software for handshaking purposes and are connected to the DSR interface lines.
SYNCA* SYNCB*	These pins are not connected on the 2820.
RxCA TxCA RxTxCB	The Channel A and Channel B clocks are separately controlled by two CTC channels; the B clock may be jumpered to TSEC (DCE).
RESET*	A low at this pin resets both SIO channels.
CLK	This is the SIO's system clock input.
INT* IEI IEO	See Section 4.7 for a discusqion of these interrupt daisy chain signals.

CTC inputs and outputs are described in Table 4.4. Programming information, including a table of baud rates, is included in the Programming Guide and in Chapter 3 of this manual.

TABLE 4.4. CTC INPUTS AND OUTPUTS

SIGNAL	FUNCTION
CE*	When Chip Enable is low, data is read from or written to the CTC during I/O cycles. CE* is controlled by the address select circuitry.
CS0,CS1	The Channel Select inputs select one of four CTC channels. They are controlled by A0-A1.
CLK/TRG 0-3	The Clock/Trigger inputs control the decrementing of the downcounters of each channel. All are controlled by the 2MHz clock.
ZC/TO 0-2	A Zero Count/Timeout line pulses high when its downcounter reaches zero. ZC/TO 0 and 2 control SIO clocks; ZC/TO1 is unconnected.
D0-7	The bi-directional data pins connect directly to the 2820 internal data bus.
INT* IEI IEO	See Section 4.7 for a discussion of these interrupt daisy chain signals.

4.6 THE DMA

The Z-80 Direct Memory Access Controller processes and controls byte-by-byte, burst, and continous data searches and transfers. During DMA operations the DMA takes control of the system bus, returning control to the CPU when the DMA operation is completed. Extensive programmability provides a wide range of capabilities while the dedicated search and transfer circuitry ensures optimum speed. Source and destination may be any combination of memory and I/O. If the source and/or destination is memory the programmed base address may be automatically incremented or decremented.

On the 282Ø the DMA's RDY input, which is used by an I/O device to signal that it is ready for a DMA operation, is made available at a jumper pad. Use of the DMA RDY pad is not essential, however, as RDY may be software-activated. The RDY pin may be programmed to be active either high or low. When the pad is not connected to another device, a pull-up resistor holds the DMA's RDY input high.

A second DMA Controller (or group of DMA Controllers, if arbitration logic is included) may be daisy-chained with the 282Ø DMA as illustrated in Appendix B. DMA daisy-chaining is made possible by the Z-8Ø DMA's BAI* and BAO* (Bus Acknowledge In and Out) pins. When a DMA Controller finds its RDY input activated (whether by software or hardware) and BUSRQ* inactive, it requests control of the bus by pulling BUSRQ* low, the first DMA directly and all other DMAs via HOLD*. When the CPU detects BUSRQ* low it finishes the current machine cycle, tri-states its address, data, and control outputs, and forces BUSAK* low to indicate that it no longer controls the system bus. BUSAK* is the first DMA's BAI* input. If the first DMA's RDY input is active when its BAI* input goes low, it forces its BAO* output high and takes control of the bus. The first DMA's BAO* output is connected via bus line pHLDA to the second DMA's BAI* input; thus, when the CPU surrenders control of the bus, if the first DMA has requested control of the bus, the second DMA is blocked from taking control by the high at BAI*. However, if the first DMA has not forced BUSRQ* low, its BAO* will remain low when its BAI* is pulled low, pHLDA will remain low, and the resulting low at the the second DMA's BAI* input will allow the second DMA to take control of the bus. Thus, when the CPU acknowledges a Bus Request, DMA activity is initiated only in the highest-priority DMA whose RDY input is active. The DMA which takes control of the bus relinquishes it by letting BUSRQ* go high again only when its programmed operation is completed; it cannot be interrupted by the other DMA or any other device.

Table 4.5 identifies the DMA inputs and outputs. Programming information is provided in the Programming Guide and Chapter 3 of this manual.

TABLE 4.5. DMA INPUTS AND OUTPUTS

SIGNAL	FUNCTION
CE*	When Chip Enable is low, data is read from or written to the DMA during I/O cycles. CE* is controlled by the address select circuitry.
BUSRQ*	This bi-directional pin is used as an output to request bus control from the CPU and as an input to indicate when another DMAC has taken control of the bus.
BAI*	Controlled by CPU output BUSAK*, Bus Acknowledge In signals that bus control has passed to the DMAC.
BAO*	Bus Acknowledge Out is used to pass the CPU's BUSAK* signal from one DMAC to another in a Daisy chain.
A15-A0	These outputs are used by the DMA to address the source and destination.
D0-7	The bi-directional data pins connect directly to the 2820 internal data bus.
RDY	Programmable active high or low, this input is used by a peripheral device to indicate that it is ready for a DMA operation.
MREQ*	This output is pulled low when A15-A0 hold a valid source or destination address.
IORQ*	As an input controlled by CPU output IORQ*, this pin and CE* low indicate a control word write to or status read from the DMAC. As an output IORQ* is used to indicate during DMA that a valid I/O address is present on A7-A0.
M1*	Controlled by CPU output M1*, this input is used by the DMA in decoding the RETI instruction from the CPU. M1* low when IORQ* is low indicates an interrupt acknowledge by the CPU.
RD*	This bi-directional signal must be low when status is read from the DMAC (input) or data is read during DMA (output).
WR*	This bi-directional signal must be low when a control word is written to the DMAC (input) or data is written during DMA (output).
CLK	This is the DMAC's system clock input.
INT* IEI IEO	See Section 4.7 for a discussion of these interrupt daisy chain signals.

4.7 THE INTERRUPT DAISY CHAIN

The Z-8Ø CPU is capable of three modes of maskable interrupt response, the mode in which the CPU operates at a given time being determined by software. The three modes are defined in the CPU section of the Programming Guide. Mode 2 is the special Z-8Ø mode allowing device-controlled vectored interrupts and thereby eliminating the necessity of polling peripherals to determine where the interrupt originated.

In support of Mode 2 interrupts, the Z-8Ø peripherals have IEI and IEO (Interrupt Enable In and Out) pins which allow them to be linked in a hardware-prioritizing interrupt daisy chain. The highest-priority device's IEO is connected to the next-highest-priority device's IEI. If a device's IEI input is high, it may generate an interrupt request by forcing INT* low. A device's IEO output is forced low if either its IEI pin or its INT* pin is low. Thus a device generating an interrupt request disables the interrupt request logic of all lower-priority devices in the daisy chain. Higher-priority devices are unaffected, however, and may interrupt at any time, providing that CPU interrupts are enabled. (See Figure B.2 for an illustration.)

The peripheral devices on board the 282Ø are hard-wired in a daisy chain with the CTC having highest priority, the DMA second, the SIO third, and the PIO last. Jumper pads allow the user to re-prioritize the on-board daisy chain by connecting the IEO of any device to the IEI of any other device. See Section 2.1Ø for instructions.

If more than four devices are connected in a simple daisy chain, a low-priority interrupt request may not be disqualified by a higher-priority interrupt request soon enough to prevent the low-priority device from thinking its interrupt is being acknowledged and outputting its interrupt vector. However, look-ahead circuitry may be used to extend the daisy chain beyond four devices. CCS Systems 2ØØ, 3ØØ, and 4ØØ use the S-1ØØ Vectored Interrupt lines for look-ahead signals. On the 282Ø, the IEO's of the four 282Ø peripherals are ANDed to control VIØ*, which is used to tell off-board Z-8Ø peripherals that an on-board peripheral has generated an interrupt request. Thus, even if the 282Ø's highest-priority device requests an interrupt, the low at its IEO will be gated directly to the off-board devices without the delay of rippling through the other on-board devices. Whether additional off-board look-ahead logic will be necessary depends on the number of links added to the daisy chain; properly configured, a daisy chain may consist

of more than thirty devices. See Appendix B for a fuller dicussion of interrupt daisy chain implementation.

4.8 Z-8Ø PERIPHERAL ADDRESSING

A 74LS138 3-to-8 decoder and 2 x 8 DIP header provide selectable addressing for the Z-8Ø peripherals on the 282Ø. The Z-8Ø provides for 256 I/O ports addressed by A7-AØ. On the 282Ø, A7-A5 control whether or not the Peripheral Address Decoder (PAD) is enabled. Open-collector Ex-OR gates compare A7-A5 with high or low signals separately selected on the Address Select Header (ASH); if the outputs of all three gates are high (true) and IORQ* is active, the PAD is enabled. Use of A7-A5 to enable the PAD means that all ports must be located in one 32-address block whose base in binary form is xxxØ ØØØØ.

Address bits A4-A2 determine which of the eight PAD outputs will be active (low). The 32-address block which must be addressed for the PAD to be enabled is thus divided into eight 4-address blocks. The PAD output pins are linked to ASH pins; also linked to ASH pins are the CE* pins of each Z-8Ø peripheral device. Thus any peripheral device may occupy any 4-address block whose base in binary is xxxy yyØØ. The 16 unused addresses in the chosen 32-address block may be used to address other, off-board ports.

No matter how many internal registers it has, each Z-8Ø peripheral is designed to occupy no more than four port addresses. Thus Al and AØ are sufficient to address the register groups within a peripheral device. For example, SIO channels A and B are distinguished by AØ while Al determines whether control or data registers will be selected. On the other hand, the DMA occupies only one port address and so does not use Al or AØ for register group selection; the DMA registers may be addressed at any of the device's four addresses. Within a register group, separate registers are selected according to specific bits of the current or previous command written to a group's address. For details of register addressing, see the Programming Guide.

TABLE 4.6
OUTPUTS FROM THE 2820 TO THE BUS

MNEMONIC	PIN #	FUNCTION	TRUE CONDITIONS
sWO*	97	Indicates a write operation cycle.	CPU/DMA WR* output active.
sINTA	96	Indicates interrupt acknowledge cycle.	CPU outputs M1* AND IORQ* active.
sM1	44	Indicates an op code fetch cycle.	CPU/DMA output M1* active.
sHLTA	48	Indicates that a HALT instruction has been executed.	CPU HALT* output active.
sMEMR	47	Indicates a non-M1 memory read cycle.	CPU/DMA outputs MREQ* AND RD* active.
sOUT	45	Indicates output-to-I/O-port cycle.	CPU/DMA outputs IORQ* AND WR* active.
sINP	46	Indicates input-from-I/O-Port cycle.	CPU/DMA outputs IORQ* AND RD* active.
pSYNC	76	Indicates first T cycle in machine cycle.	Active for clock cycle if rising edge of clock finds CPU/DMA outputs MREQ* AND IORQ* inactive.
pDBIN	78	Requests that data be put on DI bus.	CPU/DMA output RD* active, OR sINTA active AND no on-board IEO low.
pWR*	77	Indicates valid data on DO bus.	CPU/DMA output WR* active.
MREQ*	65	Indicates non-M1 memory access cycle.	CPU/DMA output MREQ* active; jumper-enabled.
MWRT	68	Indicates data valid for memory write.	Bus lines pWR* AND sOUT active.
REFRESH*	66	Idicates volatile memory refresh time.	CPU output RFSH* active.
pHLDA	26	Acknowledges off-board DMA's request for bus control.	DMA output BAO* active.
VIO*	4	Disables interrupts by other boards in daisy chain.	Any on-board device's IEO low forces INT* and VIO* low.
CLOCK	49	2 MHz reference.	Crystal controlled, 2 MHz.
Φ2	24	Master timing.	Crystal controlled, 4 MHz.
DO7-DO0	35-36, 38-40 88-90	Data Out bus for transfers from CPU or DMA to off-board I/O or memory.	Output from 2820 bi-directional data bus shared by CPU, DMA, PIO, SIO, CTC.
A15-A0	29-34, 37, 79-87	Address bus for memory (A15-A0) or I/O (A7-A0).	CPU/DMA address outputs.

4.9 BUS IMPLEMENTATION

The implementation of the S-100 bus in CCS Systems 200, 300, and 400 is fairly straight-forward. Tables 4.6 and 4.7 and the schematic/logic diagram in Appendix A show how the signals are controlled or monitored by the 2820.

TABLE 4.7
INPUTS TO THE 2820 FROM THE BUS

MNEMONIC	PIN #	FUNCTION	2820 FUNCTION
HOLD*	74	Peripheral request for control of bus.	BUSRQ* inputs to CPU, DMA.
SLV CLR*	54	Resets bus slaves.	Resets 2820 devices.
RESET*	75	Resets bus master.	May be jumpered to reset 2820 devices.
INT*	73	Maskable interrupt request.	INT* input to CPU.
NMI*	12	Non-maskable interrupt request.	NMI* input to CPU.
PWRFAIL*	13	Indicates impending power failure.	May be jumpered to CPU NMI* input.
DODSB*	23	Disables data out bus.	Tri-states data out buffer.
CDSB*	19	Disables control bus.	Tri-states control buffer.
SDSB*	18	Disables status bus.	Tri-states status buffer.
ADSB*	22	Disables address bus.	Tri-states address buffer.
XRDY RDY	3 72	Bus slaves ready when both are true.	RDY OR XRDY inactive pulls CPU WAIT* pin low.
DI7-0	41-43, 91-95	Data In bus.	Inputs to bi-directional data bus; buffer enabled if: on-board peripheral selected AND CPU/DMA output RD* active, OR sINTA active.

4.10 THE SYSTEM CLOCK

A 16 MHz crystal is used to generate two separate clock signals on the 2820. The 16 MHz signal produced by the crystal clocks a 74LS197 binary counter whose outputs are a 2 MHz signal and a 4 MHz signal. The 2 MHz signal is used for the 2 MHz clock on bus pin 49. The 4 MHz signal provides the on-board and system (bus pin 24) clocks.

4.11 WAIT CIRCUITRY

The CPU may be caused to insert wait states in two ways. First, peripheral devices may cause waits to be inserted by forcing either XRDY or RDY (bus lines 3 and 72 respectively) low. Waits generated this way last until both RDY and XRDY are high again and are thus fully controlled by the bus slaves. The other method of causing the CPU to insert waits involves installing jumpers on the 2820 to specify the conditions and the length of the wait.

One set of jumpers allows CPU outputs MREQ*, IORQ*, and/or M1* to be connected as inputs to an AND gate; if any jumper-connected line goes active, the AND gate output goes low, which removes the PRESET* signal otherwise applied to a pair of J-K flip-flops. These flip-flops, clocked by the inverted system clock, are connected in such a way that during a cycle in which they are allowed to clock, the Q* output of one flip-flop will be high the first and second times the CPU is sampling its WAIT* input, while the Q output of the other flip-flop will be high only for the first sampling of WAIT*. The WAIT STATE jumper allows either the single or the double signal to control the CPU WAIT* input by determining whether the double signal will be NANDed with itself or with the single signal. Thus the user may select the conditions under which a wait will occur (i.e., in which cycles--Memory, I/O, and/or Op Code Fetch--the wait circuitry will be enabled) as well as the length (one or two clock cycles) of the wait.

APPENDIX A

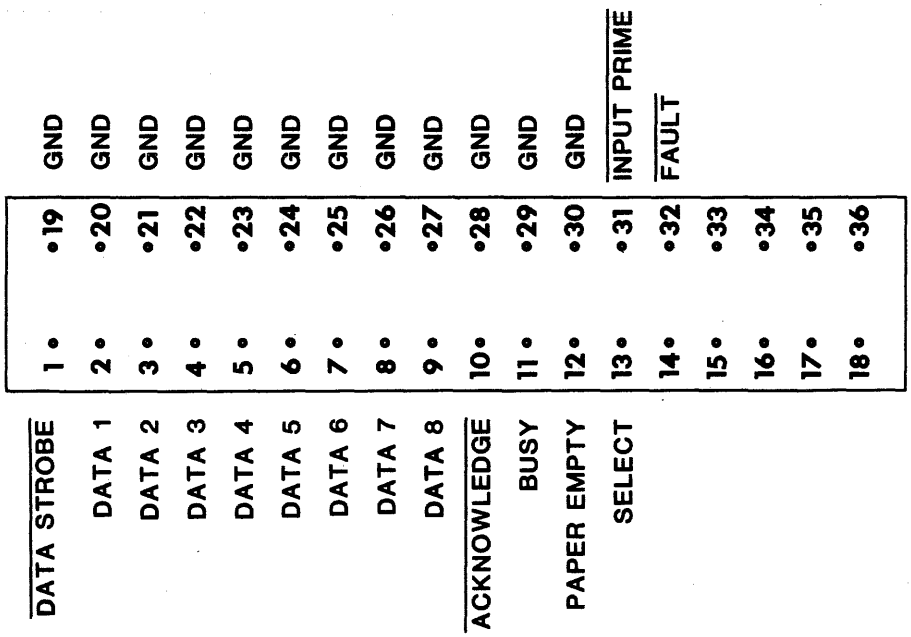
TECHNICAL INFORMATION

A.1 USER-REPLACEABLE PARTS

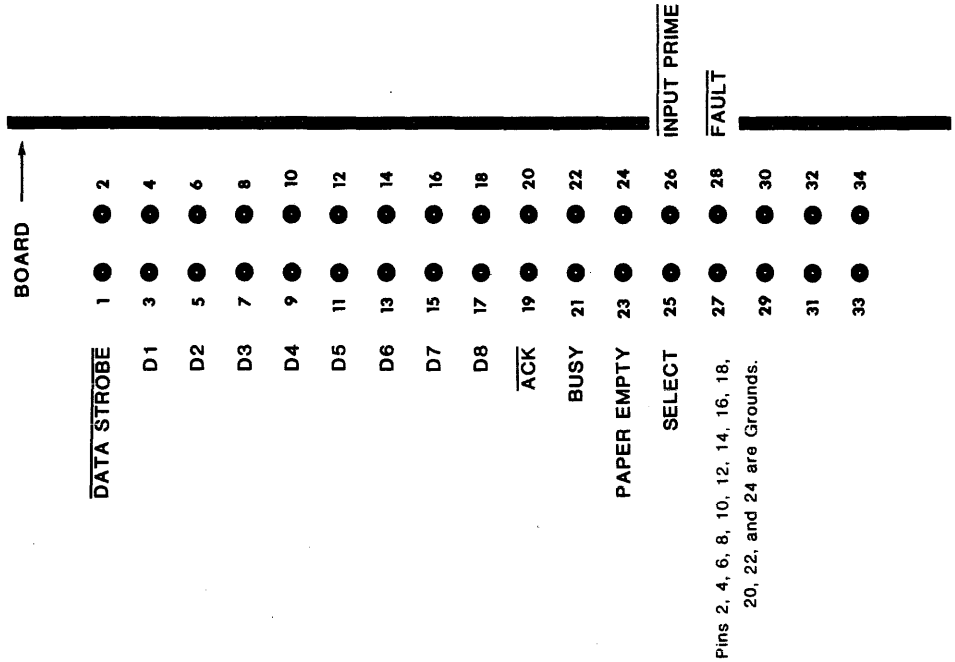
QTY	REF	DESCRIPTION	CCS PART #
	INTEGRATED CIRCUITS		
1	U13	Z-80A CPU	31200-38804
1	U12	Z-80A DMA	31200-38834
1	U22	Z-80A CTC	31200-38824
1	U4	Z-80A PIO	31200-38814
1	U3	Z-80A SIO/0	31200-38844
1	U26	74LS00 quad 2-in NAND	30000-00000
2	U25,38	74LS02 quad 2-in NOR	30000-00002
2	U14,17	74LS04 hex inverters	30000-00004
1	U31	74LS05 hex inverters, OC	30000-00005
1	U24	74LS10 tri 3-in NAND	30000-00010
2	U23,30	74LS14 hex Schmitt inverters	30000-00014
1	U19	74LS20 dual 4-in NAND	30000-00020
1	U8	74LS32 quad 2-in OR	30000-00032
1	U39	74LS74 dual D flip-flops	30000-00074
1	U15	74LS113 dual J-K flip-flops	30000-00113
1	U21	74LS136 quad EX-OR	30000-00136
1	U18	74LS138 3-to-8 decoder	30000-00138
1	U7	74LS165 8-bit shift register	30000-00165
1	U16	74LS197 binary counter	30000-00197
9	U5,6,20, 32-37	74LS244 octal buffers	30000-00244
2	U2,11	75154 line receiver	30300-00154
3	U1,9,10	75150 line driver	30300-00150
1	U29	7805 +5 V regulator	32000-07805
1	U27	78L12 +12 V regulator	32000-17812
1	U28	79L12 -12 V regulator	32000-17912
	IC SOCKETS		
3	XU1,9,10	8 pin DIP	58102-00080
15	XU8,14-17, 19,21,23-26,30,31, 38,39	14 pin DIP	58102-00140
5	XJ4,XU2, 7,11,18	16 pin DIP	58102-00160
9	XU5,6,20, 32-37	20 pin DIP	58102-00200
1	X22	28 pin DIP	58102-00280
4	XU3,4,12, 13	40 pin DIP	58102-00400

QTY	REF	DESCRIPTION	CCS PART #
	CAPACITORS		
6	C8-13	4.7 uf Tantalum, 35 VDC, 20%	4280Ø-54756
7	C1,5-7, 14-16	.1 uf Monolithic, 5Ø VDC, 20%	42Ø34-21Ø46
1	C2	33 pf Mica, 5ØØ VDC, 1Ø%	42215-533Ø5
1	C3	.Ø1 Uf Ceramic, 5Ø VDC, 20%	42142-21Ø36
1	C4	2Ø pf Mica, 5ØØ VDC, 1Ø%	42215-52ØØ5
	RESISTORS		
3	R4,5,8	1 K ohm, 1/4 W, 5%	4ØØØ2-Ø1Ø25
1	R2	22Ø ohm, 1/4 W, 5%	4ØØØ2-Ø2215
1	R3	22 ohm, 1/4 W, 5%	4ØØØ2-Ø22Ø5
1	R1	1.2 K ohm, 1/4 W, 5%	4ØØØ2-Ø1225
2	R6,7	2.7 K ohm, 1/4 W, 5%	4ØØØ2-Ø2725
4	Z1-4	2.7 K ohm x 7, SIP	4Ø93Ø-72726
	MISCELLANEOUS		
1	Q1	Transistor, 2N29Ø7	361ØØ-Ø29Ø7
2	J1,2	Connector, 2 x 13, rt angle	56ØØ5-Ø2Ø13
1	J3	Connector, 2 x 17, rt angle	56ØØ5-Ø2Ø17
1	J4	Header, 2 x 8	55ØØØ-1ØØØØ
1	Y1	Crystal, 8 MHz	48238-ØØØØ2
1		TO-22Ø Heatsink	6ØØ22-ØØØØ1
1		Screw, 6-32 x 3/8	71ØØ6-32Ø61
1		Nut, 6-32 KEP	73ØØ6-32ØØ1
2		Board Extractor	6ØØ1Ø-ØØØØ1
2		Roll Pins	6ØØ1Ø-ØØØØØ
1		User's Manual	89ØØØ-Ø282Ø

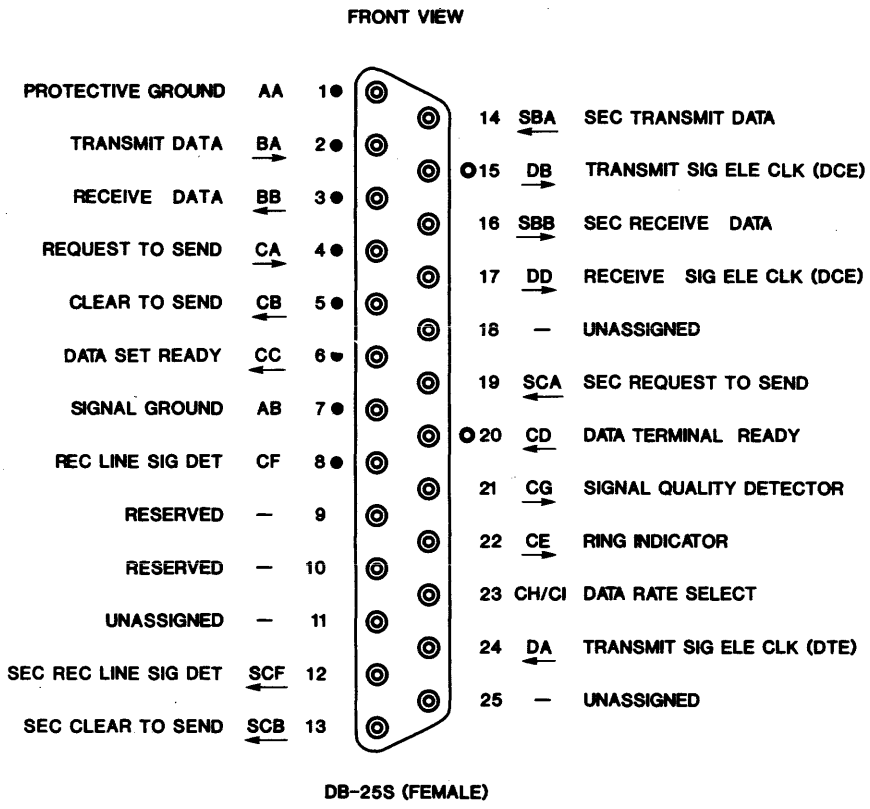
A.2 PARALLEL CABLE CONNECTOR PINOUTS



A.3 PARALLEL ON-BOARD CONNECTOR PINOUTS



A.4 SERIAL CABLE CONNECTOR PINOUTS



- ● Supported by Channels A and B
- o Supported by Channel B only

A.5 DEFINITION OF RS-232-C INTERFACE CONFIGURATIONS

A	Transmit Only
B	Transmit Only*
C	Receive Only
D	Half Duplex; or Duplex*
E	Full Duplex
F	Primary Channel Transmit Only* /Secondary Channel Receive Only
G	Primary Channel Receive Only / Secondary Channel Transmit Only*
H	Primary Channel Transmit Only / Secondary Channel Receive Only
I	Primary Channel Receive Only / Secondary Channel Transmit Only
J	Primary Channel Transmit Only* / Half Duplex Secondary Channel
K	Primary Channel Receive Only / Half Duplex Secondary Channel
L	Half Duplex Primary Channel / Half Duplex Secondary Channel; or
L	Duplex Primary Channel* / Duplex Secondary Channel*
M	Duplex Primary Channel / Duplex Secondary Channel
Z	Special (Circuits specified by supplier)

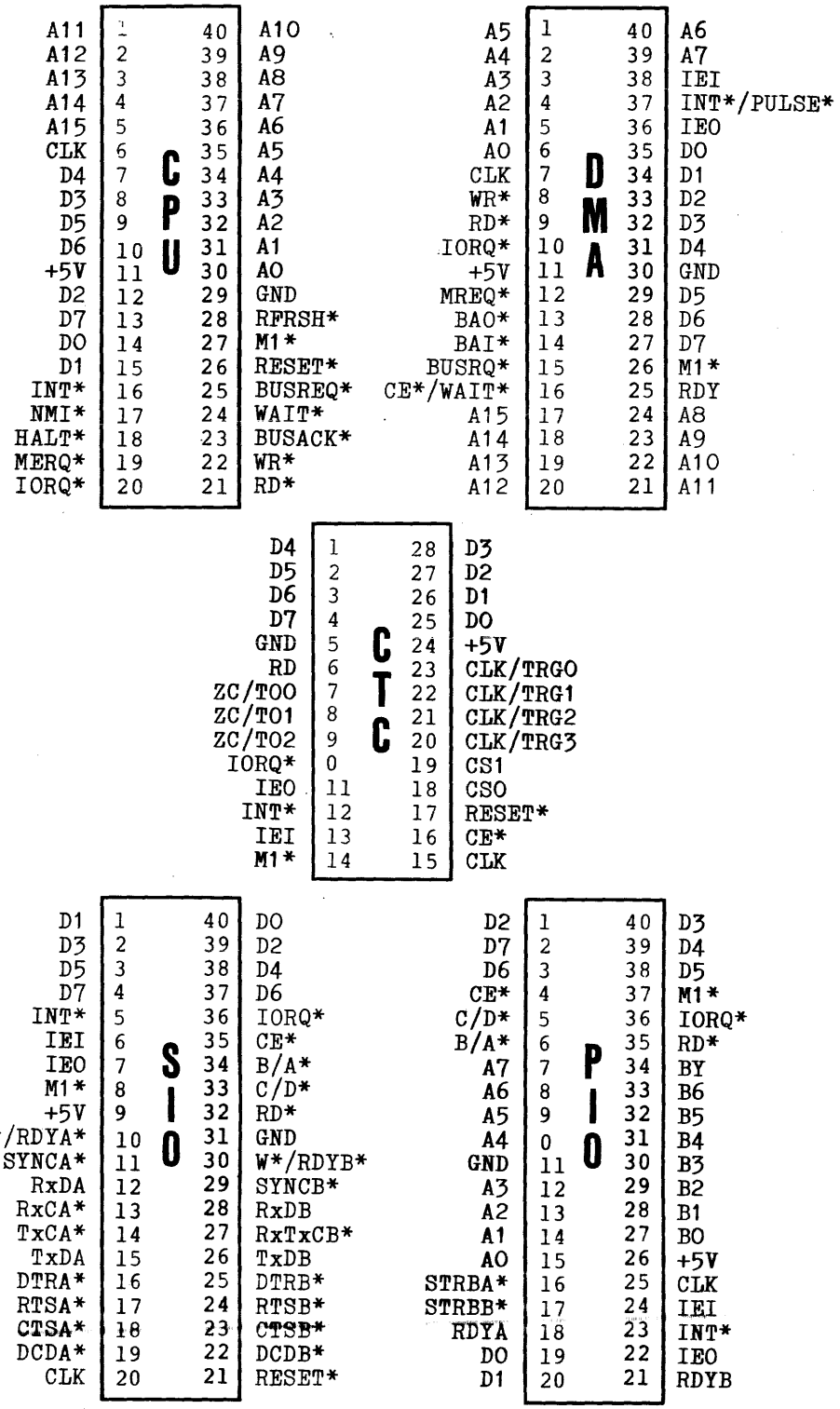
* Note the inclusion of Request to Send in a Transmit Function, where it would not ordinarily be expected, but could indicate a non-transmit mode to the data communications equipment (DCE) to permit it to remove a line signal or to send synchronizing or framing signals as required.

A.6 SIGNAL CHART FOR RS-232-C INTERFACE CONFIGURATIONS

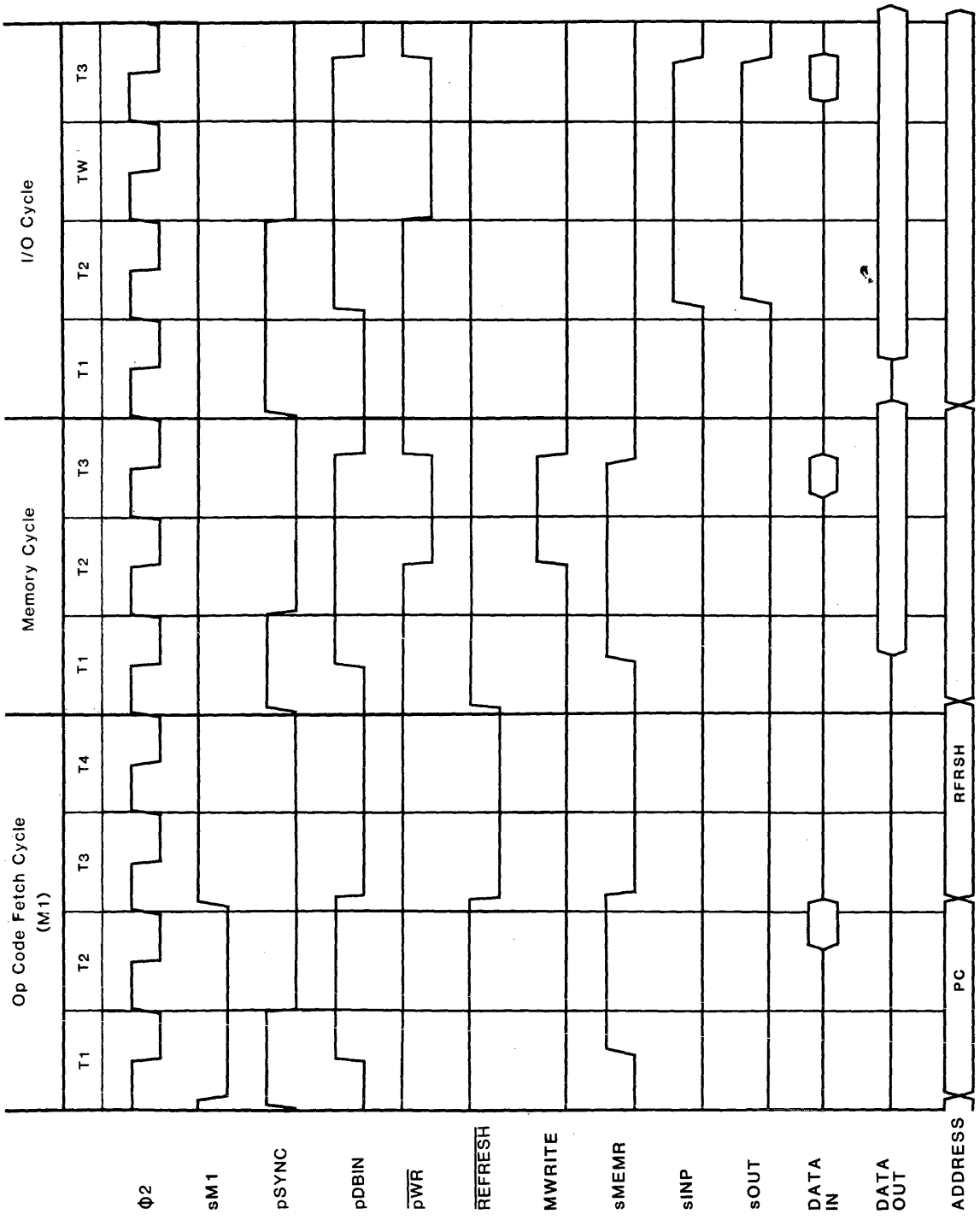
	Interchange Circuit	Interface Configuration A	B	C	D	E	F	G	H	I	J	K	L	M	Z
AA	Protective Ground	-	-	-	-	-	-	-	-	-	-	-	-	-	-
AB	Signal Ground / Common Return	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BA	Transmitted Data	X	X		X	X	X		X		X		X	X	O
BB	Received Data			X	X	X		X		X		X	X	X	O
CA	Request to Send		X		X		X				X		X		O
CB	Clear to Send	X	X		X	X	X		X		X		X	X	O
CC	Data Set Ready	X	X	X	X	X	X	X	X	X	X	X	X	X	O
CD	Data Terminal Ready	S	S	S	S	S	S	S	S	S	S	S	S	S	O
CE	Ring Indicator	s	s	s	s	s	s	s	s	s	s	s	s	s	o
CF	Received Line Signal Detector			X	X	X		X		X		X	X	X	O
CG	Signal Quality Detector														o
CH/CI	Data Signalling Rate Selector (DTE/DCE)														O
DA/DB	Transmit Signal Element Timing (DTE/DCE)	T	T		T	T	T		T		T	T	T	T	O
DD	Receiver Signal Element Timing (DCE)			t	t	t		t		t		t	t	t	o
SBA	Secondary Transmitted Data							x		x	x	x	x	x	o
SBB	Secondary Received Data						x		x		x	x	x	x	o
SCA	Secondary Request to Send							x			x	x	x		o
SCB	Secondary Clear to Send							x		x	x	x	x	x	o
SCF	Secondary Received Line Signal Detector						x		x		x	x	x	x	o

Upper case indicates a line supported by the CCS 2820.
Lower case indicates a line not supported by the CCS 2820.
X = Basic interchange circuits, all systems
T = Additional interchange circuits required for synchronous channel
S = Additional interchange circuits required for switched service
O = Specified by supplier as required
- = Optional; supported by the CCS 2820

A.7 Z-8Ø CHIP PINOUTS



A.8 2820 BUS OUTPUT WAVEFORMS



[1] The Z-80 automatically inserts a Wait state in every I/O cycle

A.9 SCHEMATIC/LOGIC DIAGRAM

MODEL 2820
SYSTEM PROCESSOR
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U7 74LS165
U5 74LS244
74LS244
U22 Z80A-CTC
U4 Z80A-PIO
U3 Z80A-SIO/O
75154
75150
R6 1K
R7 1K
INT DAISY CHAIN PADS
74LS136
74LS20
74LS05
74LS244
74LS32
74LS02
74LS14
74LS04
74LS10
74LS00
74LS113
74LS74
74LS138
74LS197
WAIT STATE
MEM
MREQ
RFSH
PWRFL
PN2907
8MHz
.01
U13 Z80A-CPU
U12 Z80A-DMA
U36 74LS244
U35 74LS244
U34 74LS244
U33 74LS244

STROBE (1)	PRIME (31)		
DO (2)	D1 (3)	D2 (4)	D3 (5)	D4 (6)	D5 (7)	D6 (8)	D7 (9)	
ACK (10)	FAULT (32)	BUSY (11)	PAPER OUT (12)	SELECT (13)				
DTR (20)	XCLK (15)							
CD (6)	DSR (6)	RTS (4)	CTS (5)	TxD (2)	RxD (3)			
RxD (3)	TxD (2)	CTS (5)	RTS (4)	DSR (6)	CD (6)			

VIO 4	CDSB 19		
pHLDA 26	REFRESH 66	pDBIN 78	pSYNC 76	MWRT 68	pWR 77		
sINTA 96	sM1 44	sMEMR 47	sINP 46	sOUT 45	sWO 97	sHLTA 48	SDSB 18
NMI 12	PWRFAIL 13	HOLD 74	INT 73	RESET 75	SLAVE CLR 54		
RDY 72	XRDY 3		
CLK 49	Φ2 24		

43 DI7	93 DI6	92 DI5	91 DI4	42 DI3	41 DI2	94 DI1	95 DI0
23 DO DSB			
90 DO7	40 DO6	39 DO5	38 DO4	89 DO3	88 DO2	35 DO1	36 DO0
22 ADD DSB			
32 A15	86 A14	85 A13	33 A12	87 A11	37 A10	34 A9	84 A8
83 A7	82 A6	29 A5	30 A4	31 A3	81 A2	80 A1	79 A0

APPENDIX B

DAISY CHAIN CONFIGURATION

The 282Ø has been designed to implement the Z-8Ø Interrupt and DMA Daisy Chains. Bus lines are used to make board-to-board daisy-chaining as convenient as possible. CCS System boards are designed for daisy chain intercompatibility as appropriate; other boards featuring Z-8Ø chips can often be easily modified to be compatible.

B.1 THE INTERRUPT DAISY CHAIN

Off-board devices on up to seven additional boards can be linked to the daisy chain using the VI* bus lines as illustrated in Figure B.1. The 282Ø uses VIØ* to disable interrupts by any other boards in the daisy chain; the second-priority board uses VI1* to disable interrupts by lower-priority boards; and so on. CCS boards designed to operate in Systems 2ØØ, 3ØØ, and 4ØØ and incorporating Z-8Ø peripheral chips support this interrupt daisy chain scheme; see the peripheral board manuals for configuration instructions.

B.2 DAISY-CHAINING DMA CONTROLLERS

The DMA Daisy Chain supported by Z-8Ø DMA Controllers differs from the Z-8Ø Interrupt Daisy Chain in that higher priority devices cannot interrupt lower priority devices. A higher priority device takes precedence over a lower priority device only if two devices request control of the bus before the CPU acknowledges the first request. If a DMA

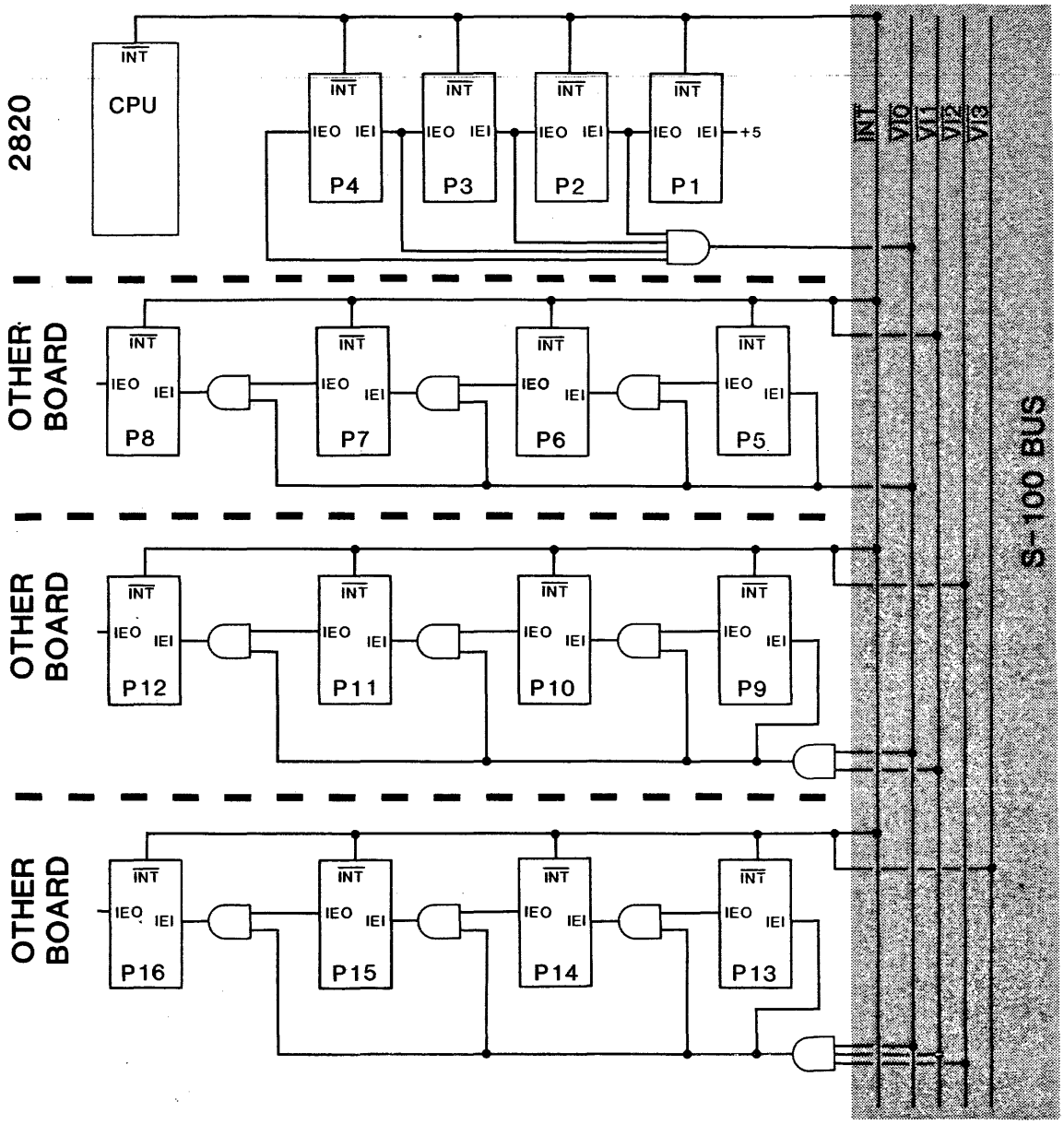

FIGURE A.1
INTERRUPT DAISY CHAIN CONFIGURATION

Controller has control of the bus when another DMA Controller requests the bus, that request will not be acknowledged until the DMA currently in control relinquishes the bus.

A Z-8Ø DMA daisy chain as described in Section 4.6 of this manual can be implemented between the 282Ø's DMA and either a single other DMA or the arbitration logic for a group of DMAs. CCS provides for the latter in its System 2ØØ, 3ØØ, and 4ØØ boards by implementing the S-1ØØ DMA prioritizing scheme for all DMA Controllers. The arbitration logic appears to the 282Ø's DMA exactly like a single other DMA. The 282Ø's DMA is tied directly to the CPU (DMA pins BUSRQ* and BAI* to CPU pins BUSRQ* and BUSAK* respectively) and therefore has first priority. DMA output BAO* and CPU input BUSRQ* are tied to bus lines pHLDA and HOLD* respectively; the arbitration logic for the other DMAs thus may use these lines to request control of the bus and to recognize when control has been granted.