89910700

CONTROL DATA CORPORATION

CONTROL DATA®
SYSTEM 17
CARD PUNCH CONTROLLER

DESCRIPTION
PROGRAMMING CONSIDERATIONS
MANUAL CONTROLS

REFERENCE MANUAL

REVISION RECORD

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PREFACE

This manual supplies reference information for CONTROL DATA ® 1725-1 Card Punch Controller. This controller is used with the 1784 Computer and the 1725-1 Card Punch. A knowledge of these equipments is necessary before using the controller.

The following listed CONTROL DATA CORPORATION publications may also be useful as reference:

Publication	Pub. No.
FE203-A Card Punch Controller Hardware Maintenance Manual	89910800
1784 Computer Reference Manual	89633400
AB107/AB108 Computer Customer Engineering Manual	89633300
I/O Specification Manual	89673100
SMM17 System Maintenance Monitor Manual	60182000

CONTENTS

FIGURES

TABLES

SECTION 1

DESCRIPTION

INTRODUCTION

The CONTROL DATA ® 1725-1 Card Punch Controller acts as an interface and control unit between the 1784 Computer and the 1725-1 Card Punch. The controller is mounted on one N-PAK printed wiring board (PWB) which is installed in any one of the A/Q slots in the 1784 Computer enclosure or the 1783-1 Expansion Enclosure. The controller requires +5 vdc which is supplied by computer power supply or the expansion enclosure power supply, in whichever enclosure it is installed.

FUNCTIONAL DESCRIPTION

System Relationship

The controller interfaces between the card punch device and the computer by way of the computer's A/Q channel. This configuration is shown in Figure 1. The interface logic in the controller provides access to the card punch device. The Q-Register input from the computer to the controller designates the Station Code, Equipment Code and Director bits which control use of the A-Register bits. The A-Register lines are bi-directional, allowing data, control and status information to flow or from the controller and the computer. Data is transferred to the A-bus in a 16-bit word, with the 12 least significant bits containing the information for punching one card column. Refer to Section 2 for a description of these registers.

The controller logic circuits perform the following functions:

1. Decode processor function codes.
2. Transmit processor function codes to the device.
3. Transfer data between the CPU and the device.
4. Transmit device status messages to the CPU.
5. Detect operation and transmission errors.

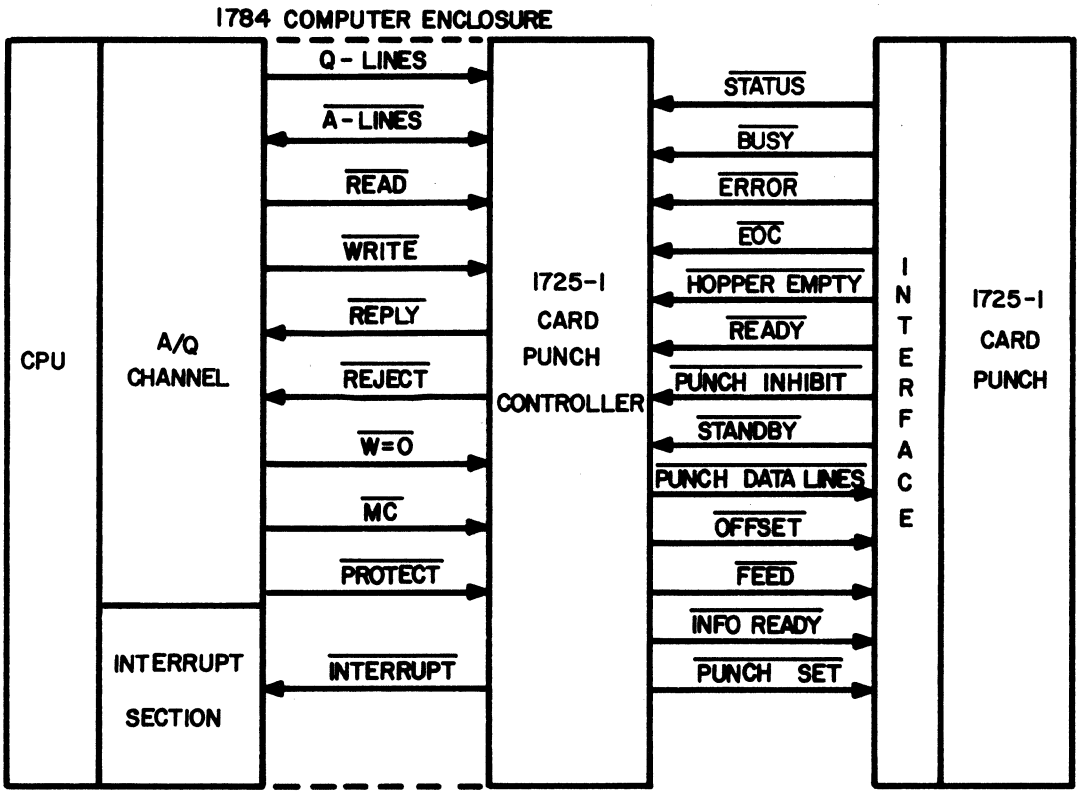

FIGURE 1. SYSTEM CONFIGURATION.

TABLE 1. SPECIFICATIONS

Specifications	
PHYSICAL CHARACTERISTICS	
Dimensions	
Width	$6\frac{13}{16}$ inches
Length	$12\frac{3}{8}$ inches
Depth	$\frac{3}{8}$ inches
ENVIRONMENT	
Temperature	
Shipping	-40°F to 158°F (-40°C to 70°C)
Storage	14°F to 122°F (10°C to 50°C)
Operating	40°F to 120°F (5°C to 50°C)
Humidity	
Shipping	0 to 100% RH non-condensing
Storage	10% to 90% RH non-condensing
Operating	10% to 90% RH non-condensing
POWER	
Input Requirements	5 Volts dc
Signal Level	
Low State (0)	0.4 Volts dc, or less
High State (1)	2.4 Volts dc, or more
Ground	Logic ground is connected to computer logic ground

1725-1
CARD PUNCH
CAPABILITIES

The maximum operating rate of the 1725-1 Card Punch is 100 cards per minute while punching all card columns. The punching rate is dependent on the number of columns sequenced for punching, with a maximum rate of 460 cards per minute if only one column is punched on each card. The capacity of the input hopper is 1,200 cards and the capacity of the output hopper is 1,300 cards.

INTERCON-
NECTION

Interconnection between the card punch controller and the device is made through the internal and external cables. The internal cable is connected between the enclosure backplane at P2 where the controller PWA is installed and the back panel of the enclosure. The external cable is connected to the internal cable (at the back of the enclosure) and the device.

An interrupt cable is also supplied. This cable is used to connect the Interrupts generated within the controller, to the selected CPU Interrupt line. For the CPU Interrupt lines available refer to Table 6.

OPERATION

The CLEAR CONTROLLER command (see Section 2) issued by the CPU clears all internal logic flip-flops and Status bits except for the Data status bit which is set if the device is READY. It is therefore assumed that a card is available for punching in the Punch Station. Refer to Figure 2 for the sequence of events.

The only condition sufficient and necessary for A/Q Data transfer is that the Data status bit is set.

The controller remains in this state until an A/Q DATA TRANSFER operation is performed. At that time Data Status drops, Busy Status is set, and the data received from the CPU is transferred to the device for column punching.

BUSY is set upon receipt of the first data word for the card, and remains set until the End of Card after punching all 80 card columns.

Upon completion of punching of a column, the Data Status bit is raised again, thus indicating that the controller is ready to accept from the CPU, the data word for the next column.

This continues until punching is completed on all 80 cards columns. At that time, EOP is set and BUSY reset (within 100 nanoseconds after EOP). Data status is reset. The controller waits for a CPU FEED REQUEST command.

The FEED REQUEST command causes the card presently in the Punch Station to be transferred to the Stacker, and moves a new card from the Hopper to the Punch Station. The FEED REQUEST is accepted by the controller at any time, provided that the card punch is READY, ON LINE and not PUNCH INHIBITED. It clears the Error and associated Alarm Status bits.

Each column punching is checked by the device for errors. A PUNCH ERROR sets the Error and Alarm status bits. Punching on that card may, however continue.

When the device becomes NOT READY or OFF LINE while processing a card, Alarm and EOP status bits are set, and BUSY is reset.

Fast punching of a deck of cards is achieved by applying the FEED REQUEST command immediately after performing the A/Q DATA TRANSFER for the last punched column of the card that is being processed. It is, however, preferable to wait for Data Status,or for EOP (if full 80 column punching is performed) before transmitting the FEED REQUEST, in order to sense a possible error in the last punched column.

A FEED REQUEST command applied after punching of less than 80 columns on a card, prevents EOP from being set for that card.

Offsetting is performed by the device on a card that leaves the Punch Station on its way to the Stacker. Therefore, FEED REQUEST and OFFSET commands applied simultaneously, offset only that card that was in the Punch Station when the command was received.

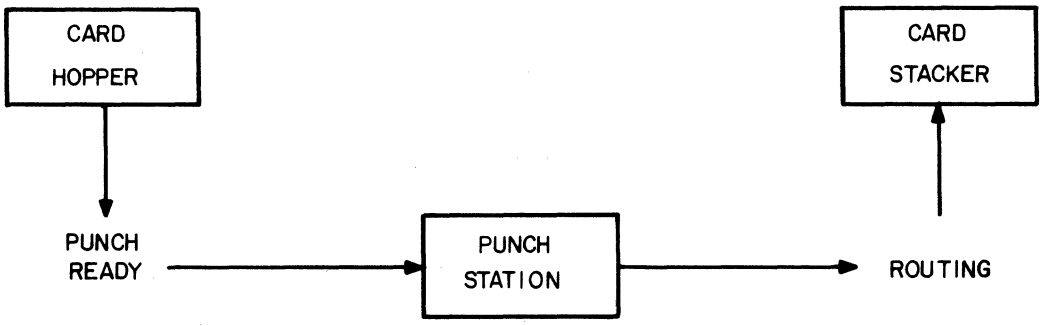

Figure 2. Card Punch Functional Stations

SECTION 2

PROGRAMMING CONSIDERATIONS

PROGRAMMING

Q-Register Format

Figure 3 describes the Q-Register format:

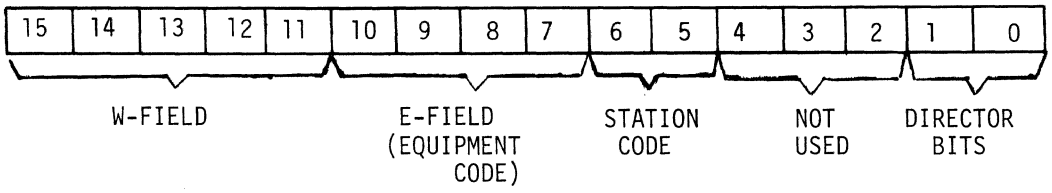

Figure 3. Q-Register Format

The W-Field MUST BE ZERO FOR ALL OPERATIONS.
The E-Field should contain the Equipment Number.
The Station Code bits must be Q05=0 and Q06=1.
The Director bits determine the type of instruction as specified by Table 2.
Bits Q02 through Q04 are not used (ignored by the controller).

Table 2 defines the Operation Codes:

TABLE 2. OPERATION CODES

Operation	Instruction	Signal	Director Bits	
			Q01	Q00
Punch Data	Output from A	Write	0	0
Director Function	Output from A	Write	0	1
Status 1	Input to A	Read	0	1
Status 2	Input to A	Read	1	1

A-Register Format

Punch Data (WRITE signal with Q00=0 and Q01=0)

The punch Data transfer operation is initiated by a WRITE signal with Q00=0 and Q01=0. A 12-bit Data word is transmitted from the CPU via the controller to card punch device. The operation is accepted when the Data Status bit is set.

The CPU Data Word is received on A-Register lines A00 through A11, and is transmitted to the card punch on interface lines CPD00 through CPD11, where the bit to row correspondence is according to Table 3. Bits A12 through A15 are not used (ignored by the controller).

TABLE 3. CORRESPONDENCE OF A-REGISTER DATA BITS TO PUNCHED ROWS

Row Number	A-Register bit
Row 12 (card top row)	A11
Row 11	A10
Row 0	A09
Row 1	A08
Row 2	A07
Row 3	A06
Row 4	A05
Row 5	A04
Row 6	A03
Row 7	A02
Row 8	A01
Row 9 (card bottom row)	A00

Director Function (WRITE signal with Q00=1 and Q01=0)

The Director Function is initiated by a WRITE signal with Q01=1 and Q01=0. The A-Register during Director Function is shown in Figure 4. The Clear commands in the Director Function (bits A00 and A01) are accepted even if the controller is NOT READY, provided that no other function is requested with the same instruction (bits A02 through A08 are all zero).

When several functions are selected by the Director Function, where some may be accepted while the other should be rejected, the controller will reject the Director Function.

Director Function bits A05, A06 and A09 through A15 are not used (ignored by the controller).

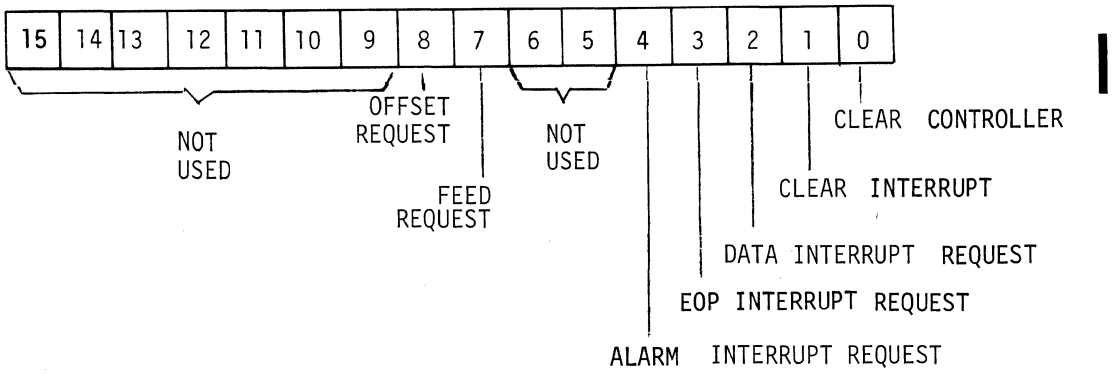

Figure 4. A-Register, Director Function

Clear and Interrupt selections may be requested simultaneously or individually. Clears (Controller and Interrupt) will be honored first, but are subordinate to requests that are executed later in the Director Function cycle.

Clear Controller (A00 = 1)

This function clears all Interrupt Requests and Responses, Motion Requests, Errors, and all other logic which may be cleared. This bit is subordinate to bits A02 through A08.

NOTE

The controller will execute and reply to this function even if it is NOT READY, provided that no other Director bit except A01, is transmitted with it (bits A02 through A08 must be zero).

Clear Interrupt (A01=1)

Clears all Interrupt Requests and Responses. It is subordinate to the Interrupt Request bits A02 through A04.

NOTE

The controller will execute and reply to this function even if it is NOT READY, provided that no other Director bit, except A00, is transmitted (bits A02 through A08 must be zero).

Data Interrupt Request (A02=1)

This function sets the Data Interrupt Request bit. It causes an INTERRUPT to be generated when an information transfer may occur.

The INTERRUPT RESPONSE is cleared by a REPLY TO DATA TRANSFER.Interrupt Requests and Responses are cleared by CLEAR INTERRUPT and CLEAR CONTROLLER.

EOP Interrupt Request (A03=1)

This function causes an EOP INTERRUPT to be generated at the end of an operation which occurred after this function was accepted. The INTERRUPT REQUEST and RESPONSE are cleared by CLEAR INTERRUPT, CLEAR CONTROLLER, or MC.

Alarm Interrupt Request (A04=1)

This function causes the generation of an interrupt when an alarm condition exists. An ALARM condition that exists at the time of the INTERRUPT REQUEST will immediately provide a response. It is cleared by CLEAR INTERRUPT, CLEAR CONTROLLER, or MC.

Feed Request (A07=1)

This function initiates a device FEED cycle. The card punch moves the punched card to the Stacker and feeds a new card from the Hopper through the Punch Ready Station, for punching. The FEED REQUEST instruction is accepted at any time, except when the card punch is in the Punch Inhibit mode. A FEED REQUEST issued while the controller is processing a card prevents setting of EOP for that card.

Offset Request (A08=1)

This function causes the device to offset the card moving from the Punch Station to the Hopper in response to a FEED REQUEST.

The controller transfers the OFFSET command to the card punch immediately upon receipt of that command from the CPU.

The OFFSET REQUEST is cleared by the FEED ACKNOWLEDGE signal by CLEAR CONTROLLER, or MC.

Director Status 1 (READ signal with Q00=1 and Q01=0)

The Director Status 1 instruction is initiated by a READ signal with Q00 = 1 and Q01 = 0. The A-Register during Director Status 1 is shown in Figure 5.

The controller accepts Director Status 1,even when NOT READY. The Director Status 1 instruction loads into the A-Register a Status Reply word showing the current operating conditions of the controller.

Status 1 bits A06, and A09 through A15, are always zero.

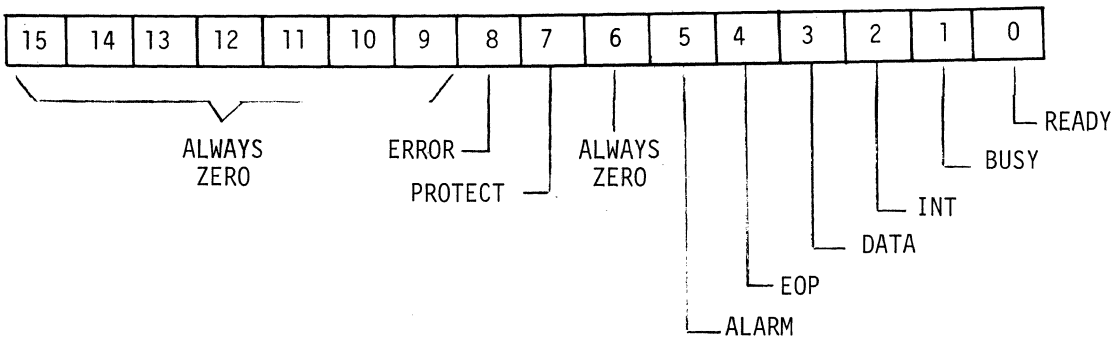

Figure 5. A-Register, Director Status 1

Ready (A00=1)

This status indicates that the card punch is READY and on-line. The card punch is ready when there is a card in the Punch Ready Station, the card punch supply is in operation, the card punch is on-line, the stacker is not full, there is no JAM condition and the interlock is closed.

The device becomes NOT READY when any of the above conditions are not met.

Busy (A01=1)

This status bit indicates that the controller is in operation.

The controller becomes BUSY when a REPLY is sent to the CPU for the first data transfer, and remains BUSY until completion of column 80 punching. A FEED REQUEST issued while the controller is busy, causes the BUSY status to be reset after punching of the column data received last from the CPU is completed.

It is cleared by CLEAR CONTROLLER, NOT READY or MC.

NOTE

The controller becomes NOT BUSY
0 to 100 nanoseconds after EOP is set.

Interrupt (A02=1)

This status bit indicates that one of the Interrupt Responses was generated by the controller. This bit is set within 100 nanoseconds after the Status bit causing the INTERRUPT RESPONSE.

Data (A03=1)

Indicates that an A/Q DATA TRANSFER operation may be performed.

The Data Status is set initially by CLEAR CONTROLLER or MC. The Data status is reset upon receipt of a PUNCH DATA instruction and set again after transfer of data to the card punch. It is reset when a FEED REQUEST is received from the CPU, or when the card punch is NOT READY or in PUNCH INHIBIT.

The Data status remains reset after data for the last card column (column 80) is transferred to the card punch for punching.

The Data status is set again after a new Card Feed cycle is initiated.

EOP (A04=1)

Indicates that the controller has completed a data transfer to the device for column 80 punching (End of Operation for the card in process).

EOP is not set if full 80-column punching is not completed as a result of a FEED REQUEST issued while the controller is busy.

EOP Status and ALARM are set if NOT READY occurred while the controller was processing a card, from the time that FEED REQUEST is accepted until the END OF CARD (EOC).

It is cleared by FEED REQUEST or CLEAR CONTROLLER or MC.

Alarm (A05=1)

Indicates the presence of ALARM conditions which occurred during operation.

The abnormal conditions are:

a. The card punch became NOT READY or PUNCH INHIBITED while the controller was processing a card.

b. PUNCH ERROR is indicated by the card punch.

The Alarm status is cleared by FEED REQUEST, CLEAR CONTROLLER or MC.

Protect (A07=1)

Indicates that the controller is protected.

Error (A08=1)

Indicates that a PUNCH ERROR in the card punch device has occurred (the PUNCH ECHO-CHECK does not agree with the requested punch data).

ERROR STATUS is cleared by FEED REQUEST, CLEAR CONTROLLER or MC.

Director Status 2 (READ signal with Q00=1 and Q01=1)(Fig. 6)

Director Status 2 is initiated by a READ signal with Q00 = 1 and Q01 = 1.

The controller accepts Director Status 2, even when NOT READY. Director Status 2 loads into the A-Register a Status Reply showing the current operating condition of the card punch device.

Status 2 bits A01 through A06 and A10 through A15 are not used.

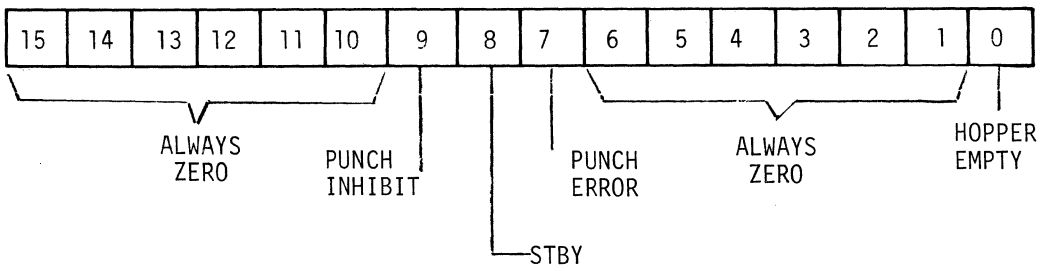

Figure 6. A-Register, Director Status 2

Hopper Empty (A00=1)

Indicates that the input Feed Hopper is empty.

Punch Error (A07=1)

Indicates a PUNCH ERROR sensed by the card punch device (PUNCH ECHO CHECK does not agree with the requested punch information).

Stand-By (A08=1)

Indicates that the card punch is Off-line.

Punch Inhibit (A09=1)

Indicates that the card punch is in the Punch Inhibit state, which prevents punching. When the card punch device is in this state, the controller rejects any PUNCH DATA or FEED REQUEST instructions.

Rejects

Conditions for External Reject

1. READ signal with Q00=0.
2. WRITE signal with Q01=1.
3. Protect violation.
4. Punch Data Instruction issued when the Data status is zero.
5. Director Function instruction issued by the CPU, while the controller is NOT READY and including functions other than Clear.
6. FEED REQUEST instruction issued when the card punch device is PUNCH INHIBITED.

Conditions for Internal Reject

1. Wrong Equipment Number.
2. Wrong Station Code.
3. The W-Field is not zero.

Interrupt Response Signals

The three Interrupt Response signals, DATA, EOP, and ALARM, are made available to the computer as three separate signals. A COMMON INTERRUPT RESPONSE is also available for transmission to the CPU. The Interrupt Request and Responses are cleared by CLEAR INTERRUPT, CLEAR CONTROLLER or MC.

Data Interrupt Response

DATA INTERRUPT RESPONSE is generated when both DATA INTERRUPT REQUEST and DATA STATUS are set.

The DATA INTERRUPT RESPONSE is cleared by Clear functions, upon completion of an A/Q Data Transfer operation, or by FEED REQUEST.

EOP Interrupt Response

The EOP INTERRUPT RESPONSE is generated upon completion of an operation which has ended after the EOP INTERRUPT REQUEST was made.

The EOP INTERRUPT RESPONSE is cleared by FEED REQUEST and the CLEAR FUNCTION or MC.

Alarm Interrupt Response

ALARM INTERRUPT RESPONSE is generated when Alarm conditions occur and the ALARM INTERRUPT REQUEST is set.

The ALARM INTERRUPT RESPONSE is cleared by the FEED REQUEST, CLEAR FUNCTIONS or MC.

Common Interrupt Response

The COMMON INTERRUPT RESPONSE is generated when one or more of the DATA INTERRUPT, EOP INTERRUPT, or ALARM INTERRUPT RESPONSE signals is generated.

SECTION 3

MANUAL CONTROLS

CONTROL

Removable jumper plugs for equipment and control definitions are located on the controller PW board.

EQUIPMENT NUMBER JUMPER PLUGS (Q07 through Q10)

Four jumper plugs are used to represent any number from 0 to F(hexadecimal). They are used to assign an Equipment Number to the controller. Any instruction sent by the computer must be accompanied by an Equipment Number (bits Q07 through Q10) that matches the setting of the jumpers. The jumper plugs are located between U28 and U30 (See Tables 4 and 5, and Figure 7).

PROTECT JUMPER PLUG (PRT)

The PRT jumper plug, when inserted, protects the card punch controller and device from receiving unprotected instructions.

Unprotected Status instructions to a protected controller are accepted.

Unprotected Director Function and Data Transfer instructions to a protected controller are rejected.

Protected instructions are accepted independent of the jumper plug setting.

The jumper plug is located between U27 and U28 (see Table 4 and Figure 7).

INTERRUPTS

The Interrupts generated by the controller are available at P1B24, P1B25, P1B26 and P1B27 on the back plane of the enclosure at the location where the controller PWA is installed. These Interrupts may be connected to a selected CPU Interrupt line by using the Interrupt cable supplied with the controller. Refer to Table 6 for a list of those Interrupts available and the CPU Interrupt lines where they may be connected.

TABLE 4. MANUAL CONTROL SELECTIONS

TO SELECT		AT LOCATION	ACTION
EQUIPMENT CODE -	Q-REGISTER	Between	
(Refer to Table 5 and Figure 7)	Q7 = "1"	U28 and U30	Install Jumper Plug
	Q8 = "1"	" " "	" " "
	Q9 = "1"	" " "	" " "
	Q10 = "1"	" " "	" " "
	Q7 = "0"	" " "	No Jumper Plug
	Q8 = "0"	" " "	" " "
	Q9 = "0"	" " "	" " "
	Q10 = "0"	" " "	" " "
PROTECTED		Between	
(PRT)		U27 and U28	Install Jumper Plug
UNPROTECTED		" " "	No Jumper Plug

TABLE 5. EQUIPMENT CODE REPRESENTATION

HEXADECIMAL CODE OF E-FIELD (Q07-Q10)	Jumper Plugs			
	Q10	Q09	Q08	Q07
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
A	1	0	1	0
B	1	0	1	1
C	1	1	0	0
D	1	1	0	1
E	1	1	1	0
F	1	1	1	1

A "1" in the binary code indicates the presence of a jumper plug for the setting of the equipment code and a "O" indicates its absence.

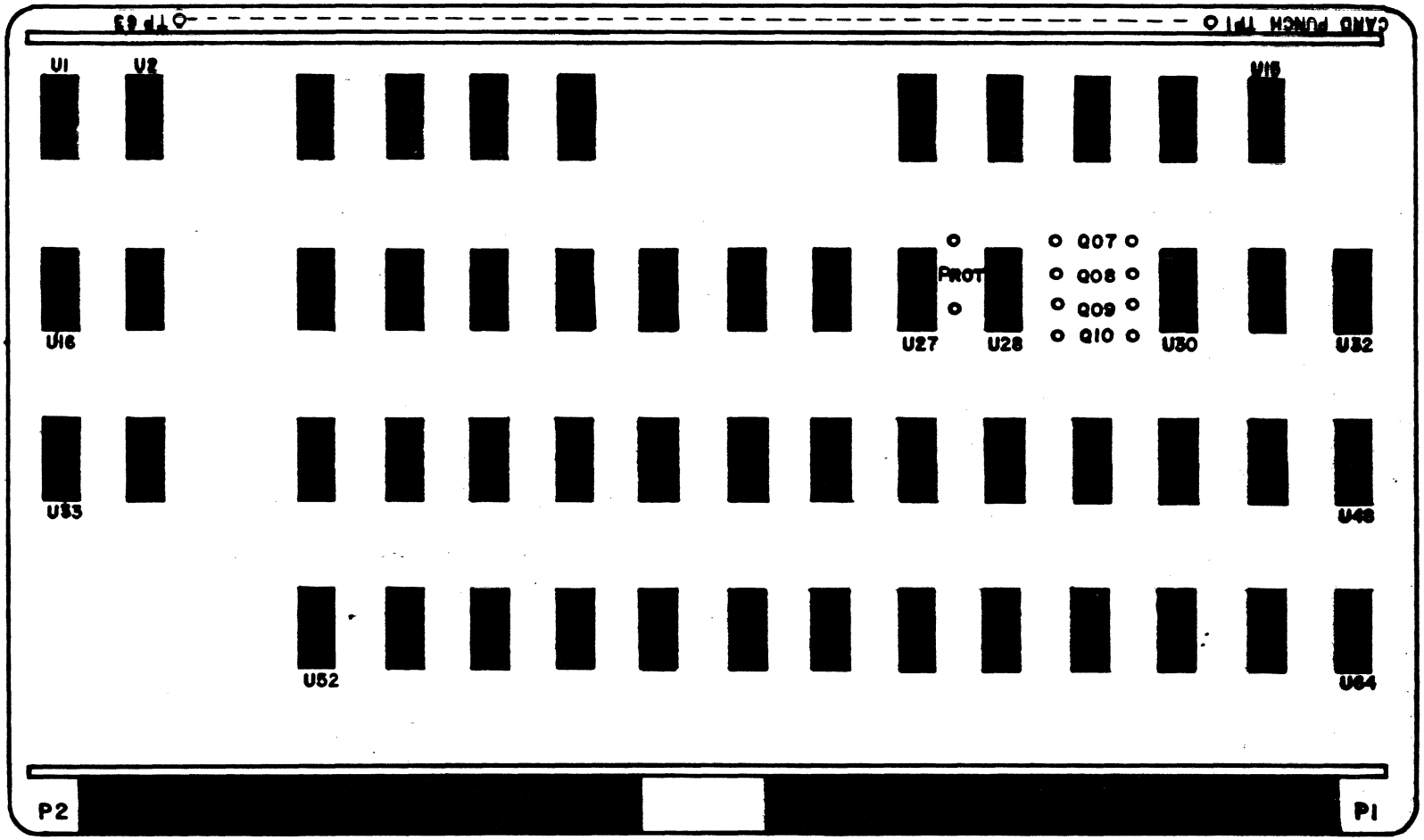

Figure 7. Locations for Placement of Manual Control Jumper Plugs on PWA

TABLE 6. INTERRUPT PIN ASSIGNMENTS

Card Punch Controller

EØP Interrupt	P1B25
Common Interrupt	P1B27
Data Interrupt	P1B24
Alarm Interrupt	P1B26

Connections may be made to any of the following:

CPU	(Position)	
Line 1	25	P1B10
" 2	25	P1A7
" 3	25	P1B7
" 4	25	P1A5
" 5	25	P1A6
" 6	25	P1B6
" 7	25	P1B5
" 8	26	P1A10
" 9	26	P1B10
" 10	26	P1A7
" 11	26	P1B7
" 12	26	P1A5
" 13	26	P1A6
" 14	26	P1B6
" 15	26	P1B5

COMMENT SHEET

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