SPECIFICATION

FOR

TM
LARK MICRO INTERFACE

G⋑ CONTROL DATA
CORPORATION

SPECIFICATION

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TM
LARK MICRO INTERFACE

MAGNETIC PERIPHERALS INC.

⋑ a subsidiary of
CONTROL DATA CORPORATION

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1.0   SCOPE

This document presents the interface specifications for the Lark™
Micro Interface used with the Model 9454 Lark Micro Unit. Within
this specification the disk storage device will be referred to as
the Lark Micro Unit, LMU, Micro Unit, or simply as the drive; and
the interface will be referred to as the Lark Micro Interface
(LMI). The user-designed controller which allows information
transfer between the LMU and the central processing unit will be
referred to as the adapter.

This document only defines the digital signal interface. For
power requirements, refer to the device Product Specification for
the specific disk storage device being used.

This document will be the common interface specification for
future MPI products utilizing the Lark Micro Interface. Future
products will utilize commonality in definition and timing con-
ditions wherever possible.

2.0   APPLICABLE DOCUMENTS

9454 Lark Micro Unit Product Specification, 77653527

3.0   GENERAL DESCRIPTION

The Lark Micro Unit (LMU) utilizes an asynchronous bus interface
which allows flexibility in the adapter design. The bus timing
and protocol is controlled by a micro-computer within the LMU
to also provide maximum flexibility and expandability of the
interface for future product enhancements. Bus timing require-
ments (that is, setup times, hold times, response times, etc.)
have been defined to require minimal hardware within the
adapter. These timing requirements also allow a wide range of
technologies (such as MOS, LSI, TTL, and/or micro-computers)
to be used to implement an adapter design. The physical inter-
face consists of a 40-pin command (C") cable and a 26-pin data

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("D") cable. The command cable can be daisy-chained and is
based on an 8-bit bidirectional bus for command/status trans-
fers between the adapter and the drive.

NOTE

The user must provide the daisy-chain facilities;
only one command I/O connector is provided on the
LMU.

A maximum of four LMU's may be daisy-chained. The data cable,
which contains high frequency (9.67 MHz) read/write signals,
must be radially connected. The maximum cumulative interface
cable length is 4.0 feet. Refer to Figure 1.

Interface dialogue is initiated by the adapter via a dedicated
signal line called the "Event" line. The LMU then responds
by requesting the adapter to transmit the Event Byte which
contains information relative to the desired activity. Subse-
quent requests for additional bytes of information from the
adapter may occur as a function of the original Event Byte
transfer.

For example, if the Event Byte requested a head change, the LMU
would respond by asking for the desired head address. Multiple
operations may be requested within a single Event Byte transfer
to minimize interface dialogue. Table 1 details combinations
of valid multiple events and the complementary information that
will be requested by the drive necessary to execute the specific
Events. After the adapter has transmitted this complementary
information, the LMU will begin execution of the Event in a
prescribed manner. At the completion of the Event(s), the LMU
will request the adapter to receive current status of the LMU
in one of two modes. In one of these modes an automatic status

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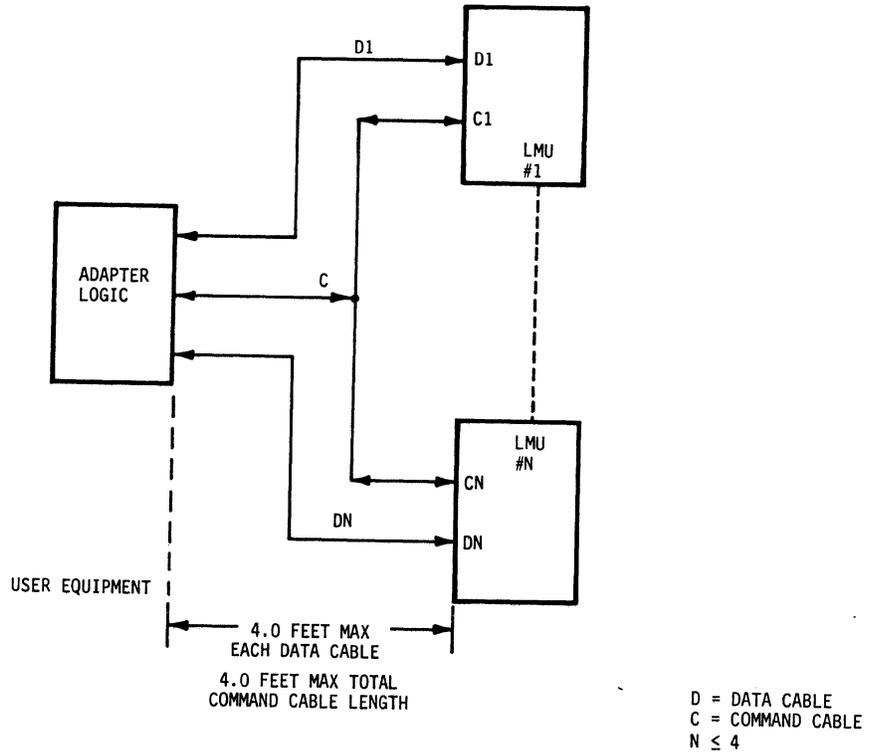
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Figure 1. Lark Micro Interface Cabling

transfer will be requested. The adapter should be prepared to respond to this request.

The LMU also provides an alternate method of handling status returns via a dedicated bit within the Event Byte called the Interrupt Bit. If this bit is true, the drive will signal the adapter of a Status change by means of the Interrupt Request line in the data cable. This line will function independently of Unit Select and will allow the user a capability to perform overlapping operations in a multiple-LMU or interrupt-driven system.

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A micro-computer within the LMU monitors all critical drive activity and will store conditions relative to this activity in its memory. As an aid to fault diagnosis, this information can be requested by the adapter and subsequently transferred across the interface. The interface also incorporates Early and Late Data Strobing capabilities to aid in read data recovery.

A comprehensive and detailed description of each signal line and commands/status will be contained in the following sections.

3.1 COMMAND CABLE SIGNAL DEFINITION

Interface signals for the command and data cables are illustrated in Figure 2 and discussed in the following paragraphs.

3.1.1 Event

The Event signal indicates the drive must execute a command. The drive will request the adapter's Event Byte to determine the operation to be performed. Response to the Event signal will be delayed if the LMU is currently performing the operation(s) specified by a previous Event (that is, the drive will honor a new Event after completion of a previous Event) or if the drive is responding to a status change.

The drive will inhibit writing of the media when Event is active. Writing is inhibited by drive electronics as soon as the leading edge of the Event signal is detected. The adapter must not activate Event while a data read or write operation is in progress. Writing will be inhibited until Event is deactivated. Depending upon the operation, writing may also be inhibited until the operation specified by Event is completed. Attempting to write during these times will generate a fault condition.

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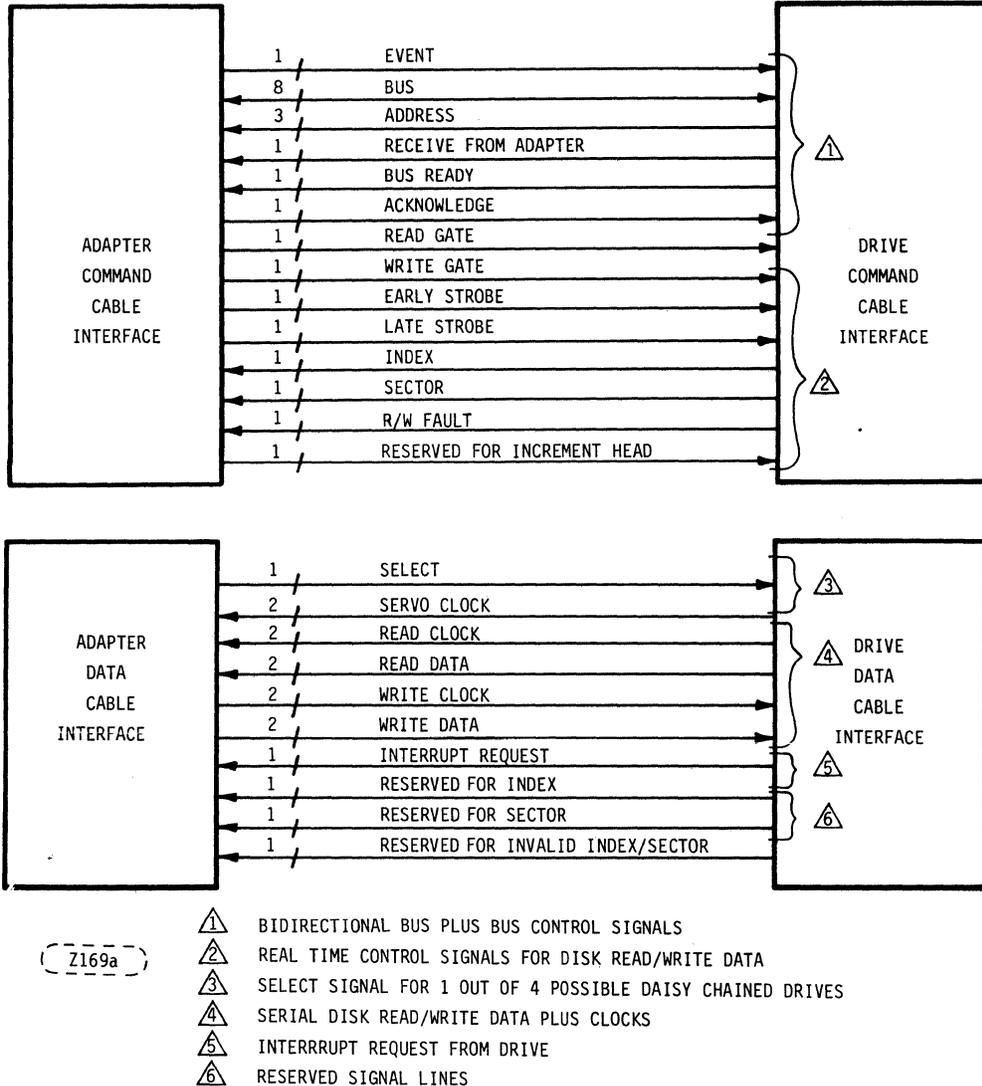
Figure 2. Lark Micro Interface Signals

The Micro Unit Interface has been designed to require a minimal utilization of the Event signal. Anytime the drive is selected and the status of the drive changes, the drive automatically requests to send the updated Status Byte to the adapter. Thus, the adapter need only use the Event function to specify operations to be performed and need not utilize Event to Request status. The LMU can, therefore, dedicate time to performing internal tests (such as RPM tests, etc.) without being continuously interrupted by status transfer commands from the adapter.

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If the Interrupt bit is active when the Event Byte is trans-
ferred or if the drive is deselected, the LMU will respond
to a status change by raising the Interrupt Request line. The
adapter may then respond by selecting the drive (if deselected),
initiating an Event request, and sending an Event Byte request-
ing the updated status.

To ensure the drive has detected that a command is to be exe-
cuted, Event should remain activated until the Bus Ready sig-
nal requesting the Event Byte (Address 111 with Receive From
Adapter active) is received from the LMU. The Event line must
be deactivated after the adapter acknowledges the Event Byte
transfer to the LMU to ensure that the drive will not execute a
redundant command.

See Figure 3 for timing requirements and Section 4.1 for a
definition of the Event Byte.
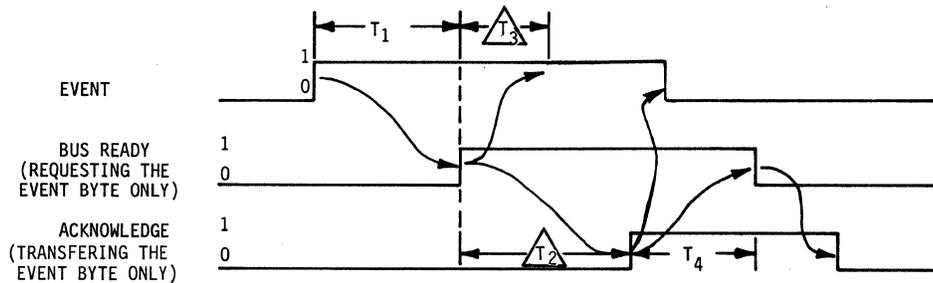
$T_1 \leq 200^*$ ms IF SEEK IN PROCESS

$T_1 \leq 500^*$ μs IF SEEK NOT IN PROCESS **

$\triangle T_2 \geq 0^*$ ns

$0 \leq \triangle T_3 \leq 1^*$ μs + T_2

$T_4 \geq 2^*$ μs

T_i INDICATES DRIVE CONTROLLED TIME WHERE i = 1 and 4

$\triangle T_i$ INDICATES ADAPTER CONTROLLED TIME WHERE i = 2 and 3
      REFER TO FIGURE 5 FOR DETAILED TIMING OF DATA TRANSFER

* PRELIMINARY VALUE

NOTE: LOGIC 0 $\geq$ 2.4 VOLTS AT THE DRIVE INTERFACE
         LOGIC 1 $\leq$ 0.4 VOLTS AT THE DRIVE INTERFACE

** THIS NUMBER ASSUMES NO OPERATOR INTERVENTION

(Z172b)

Figure 3.   Event Timing

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3.1.2   Receive From Adapter

The Receive From Adapter signal specifies the direction of
information transfer on the Bus lines. A logic 1 signifies
that information is to be transferred from the adapter to the
drive; a logic 0 signifies that information is to be trans-
ferred from the drive to the adapter.

See Figures 4, 5, and 6 for detailed timing of this signal.

The line may be used for a secondary function of signaling
when the drive can be deselected (when in the Interrupt mode)
following an event in which positioner movement occurs.
Receive From Adapter will switch states and be in the trans-
mit mode immediately following the transfer of the Event Byte
and complementary parameters.

$T_1 \leq 200$ ns T_x - DRIVE CONTROLLED TIME

$T_2 \geq 0$ T_y - ADAPTER CONTROLLED TIME

$T_3 \leq 1$ μs

"1" ⇒ 0.4 VOLTS MAX. AT INTERFACE
       WHICH IS ACTIVE STATE (TTL LOW).
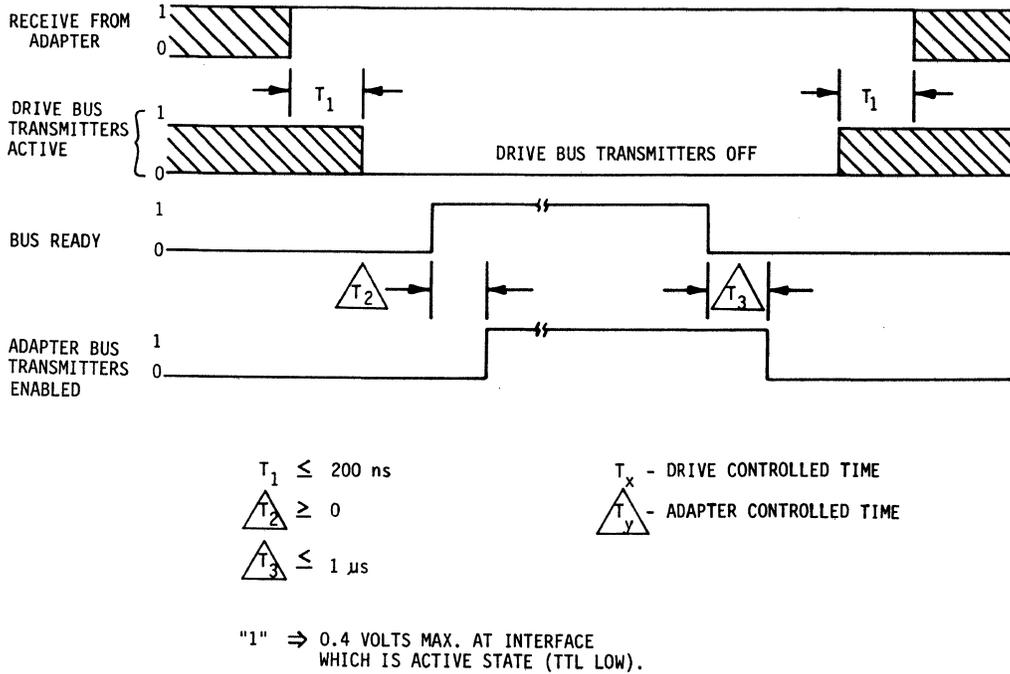
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Figure 4. Bus Transceiver Control

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3.1.3   Address

The three Address lines specify up to eight different interpretations of the information on the bidirectional Bus lines. The state of the Address lines is controlled by the LMU in response to the adapter-controlled Event request and are used in both directions of transfer.

The following Address Line configurations have been defined.

Bytes Received from the Adapter	
Address Bit (210)	Bus Byte
111	Event Byte
000	Escape Byte
110	Low Cylinder Byte
100	High Cylinder Byte
101	Head Byte
001	Reserved for future use
010	Reserved for future use
011	Reserved for future use
Bytes Sent to the Adapter	
Address Bit (210)	Bus Byte
111	Status Byte
001	MC Status Codes Byte
011	Auxiliary Byte
000	Device ID Byte
010	Detailed Status Byte
100	Reserved for future use
101	Reserved for future use
110	Reserved for future use

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3.1.4   Bus (Bidirectional)

The Bus signal is an 8-bit 3-state bidirectional bus used for
information transfers between the drive and the adapter. The
Bus dialogue is defined in Figures 5 and 6. When the Bus is
valid, the bit interpretations shown in Figure 10 are defined
by the state of the Address lines and the Receive from Adapter
signal levels. Refer to sections 4.0 and 5.0.

3.1.5   Bus Ready

Bus Ready is a handshaking line from the drive to the adapter
which initiates all Bus transfer requests.

For Bus transfers from the drive to the adapter, the leading
edge of the Bus Ready signal signifies that the contents of
the Address and Bus lines are valid and that the adapter may
accept the information. The trailing edge acknowledges the
acceptance of the Bus information by the adapter.

For Bus transfers from the adapter to the drive, the
leading edge of the Bus Ready signal signifies that the drive
is ready to accept a Bus byte from the adapter as specified
by the address lines. The trailing edge of Bus Ready signi-
fies that the drive has accepted the Bus byte from the
adapter.

Refer to Figure 5 for detailed timing of these lines.

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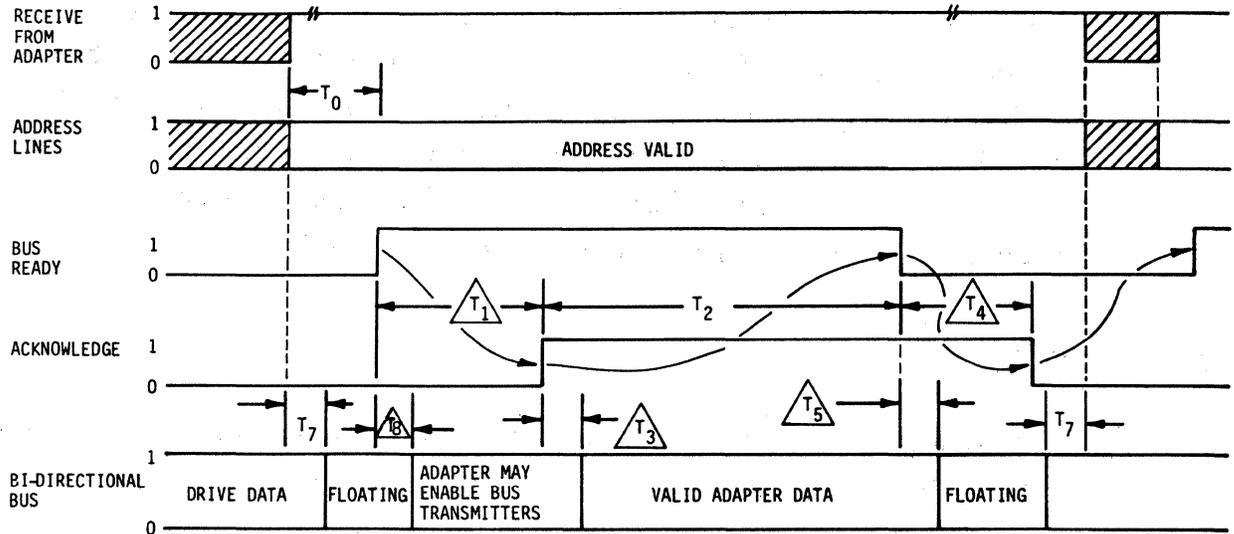
$*T_0 \geq$ 400 ns ADDRESS SETUP TIME

$0 \leq */T_1\backslash \leq$ 500 μs MAX

$T_2 \leq$ 100 μs MAX

$/T_3\backslash \leq$ 1 μs MAX ADAPTER DATA MUST BE VALID AT THE DRIVE CONNECTOR AFTER ACKNOWLEDGE

$0 \leq /T_4\backslash \leq$ 100 μs MAX

$/T_5\backslash \leq$ 1 μs MAX THE ADAPTER MUST CEASE DRIVING THE BUS WITHIN 1 μs AFTER
BUS-READY BECOMES INACTIVE

$T_7 \leq$ 200 ns MAX   THE DRIVE WILL CEASE DRIVING THE BUS A MAXIMUM OF 200 ns
AFTER RECEIVE-FROM-ADAPTER BECOMES ACTIVE

$/T_8\backslash \geq$ 0 MIN   THE ADAPTER MAY DRIVE THE BUS AFTER BUS-READY BECOMES ACTIVE

* ALL T_x TIMING CONTROLLED BY DRIVE.

* ALL /T_y\ TIMING CONTROLLED BY ADAPTER.

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Figure 5.   Read an Adapter Byte Timing

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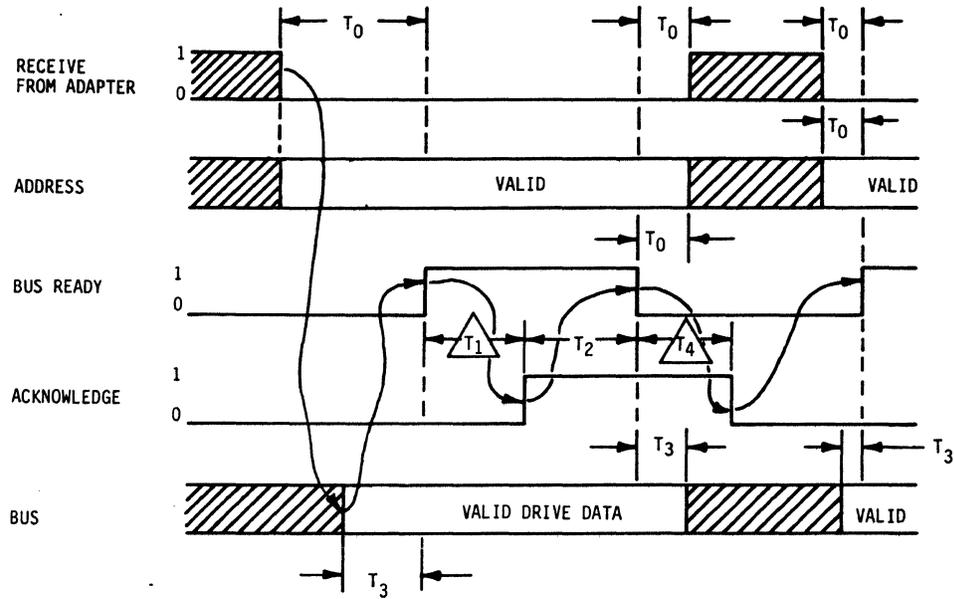
$T_0 \geq 400$ ns — THE ADDRESS IS VALID 400 ns BEFORE BUS READY BECOMES ACTIVE.

$0 \leq T_1 \leq 500$ μs MAX — THE ADAPTER MUST RESPOND TO BUS READY ACTIVATION WITHIN 500 ns.

$0 \leq T_2 \leq 100$ μs

$T_3 \geq 400$ ns — DRIVE DATA TO BUS READY SET UP AND HOLD TIME.

$0 \leq T_4 \leq 100$ μs MAX

NOTE: "1" ≥ 0.4 VOLTS MAX AT INTERFACE (TTL LOW)

T_i ≥ DRIVE CONTROLLED TIME

T_i (triangle) ≥ ADAPTER CONTROLLED TIME

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Figure 6.   Send a Byte to the Adapter Timing

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3.1.6   Acknowledge

Acknowledge is a handshaking line from the adapter to the drive which indicates acceptance of a Bus byte from the drive or the presence of a valid Bus byte to the drive.

For Bus transfers from the drive to the adapter, the leading edge of Acknowledge signifies that the adapter has accepted the Bus byte (the response to the leading edge of the drive's Bus Ready signal.) The trailing edge of Acknowledge signifies detection of the trailing edge of Bus Ready.

For Bus transfers from the adapter to the drive, the leading edge of Acknowledge signifies that the data requested by the leading edge of Bus Ready is available on the bus. The trailing edge of Acknowledge signifies detection of the trailing edge of the Bus Ready signal.

Refer to Figures 5 and 6 for detailed timing.

If the adapter decides to terminate a dialogue sequence by not responding to Bus Ready with Acknowlege, the drive will wait for approximately 500 microseconds, Fault, and then close the dialogue sequence. A micro-computer detected status code (MC Status Code) will be stored since the drive does not know that the "no response" condition was intentional. Commands for which processing has been completed before the dialogue is terminated will be executed; all others will be ignored.

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3.1.7   Read Gate

The Read Gate signal enables serial NRZ Read Data on the
radial Read Data lines. The leading edge of Read Gate
triggers the drive to synchronize on the PLO synchronization
pattern. (See Section 7.0 for application and timing
information.)

The Early Strobe or Late Strobe line may be enabled simul-
taneously with Read Gate as an aid in recovering marginal
data. (Refer to Sections 3.1.9 and 3.1.10.)

3.1.8   Write Gate

The Write Gate signal enables the drive to write the serial
NRZ write data defined by the data cable Write Data and
Write Clock signals. (See Section 7.0 for application and
timing information.)

3.1.9   Early Strobe

<u>NOTE</u>

The Early Strobe signal is intended to
be an aid in recovering marginal data
and is only valid when Read Gate is true.

When this line is true, the drive's PLO data separator will
strobe the data at a time earlier than nominal. Normal
strobe timing will be returned when the line is false.

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3.1.10 Late Strobe

NOTE

The Late Strobe signal is intended to
be an aid in recovering marginal data
and is only valid when Read Gate is
true.

When this line is true, the drive's PLO data separator will
strobe the data at a time later than nominal. Normal strobe
timing will be returned when the line is false.

3.1.11 Index Pulse

The Index Pulse (1.25 $\pm$ 0.2 microseconds) occurs once per
revolution; its leading edge is considered the sector pulse
for sector zero (see Figures 7 and 8). Index pulses may be
missed when a head change is performed. Index timing will
become valid (that is, accurately reflect the location of
sector zero) when On Cylinder is true after a head change.

If a head switch occurs during an Index Pulse, the pulse will
not be gated off, but will be allowed its full pulse width.

3.1.12 Sector Pulse

The Sector Pulse (1.25 $\pm$ 0.2 microseconds) is derived from
the embedded servo (see Figures 7 and 8). Sector Pulse
integrity is retained when Ready is active and throughout
seek operations in which no head change is effected. There
are 63 sector pulses available per revolution for the 64
sector-per-track format (see Figure 8). When combined with

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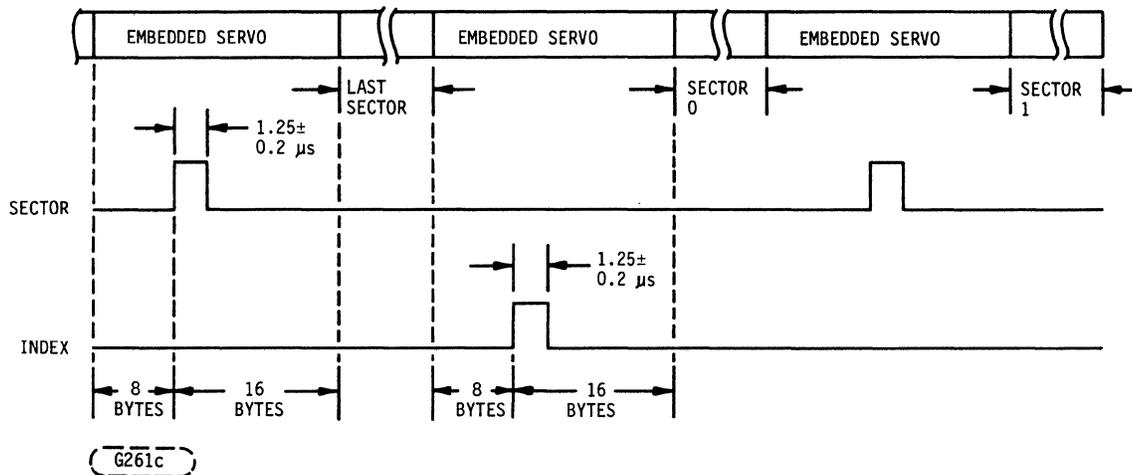
Figure 7. Relative Index and Sector Relationship

Index in the adapter, this divides the tracks into 64 equal-length sectors.

NOTE 1

Sector pulses will be missed as a consequence of a head change (Figure 8). If the adapter counts sector pulses to determine sector location, it should wait until the next Index pulse following the On Cylinder indication to establish rotational position orientation after a head change. Head changes occur due to Head Select or RTZ commands.

NOTE 2

The phase relationship of index/sector pulses to Servo Clock is not guaranteed.

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△1 INDEX/SECTOR PULSES BECOME INVALID AS A RESULT OF HEAD
    SELECT OR HEAD SELECT WITH SEEK OR RTZ.

△2 AFTER COMPLETION STATUS RETURN IN WHICH ON CYLINDER
    IS TRUE, SECTOR PULSES WILL DEFINE THE BEGINNING
    OF A SECTOR; HOWEVER, ANY ROTATIONAL POSITION
    SENSING MECHANISM IMPLEMENTED BY THE ADAPTER MAY
    NOT BE VALID UNTIL THE NEXT INDEX PULSE.

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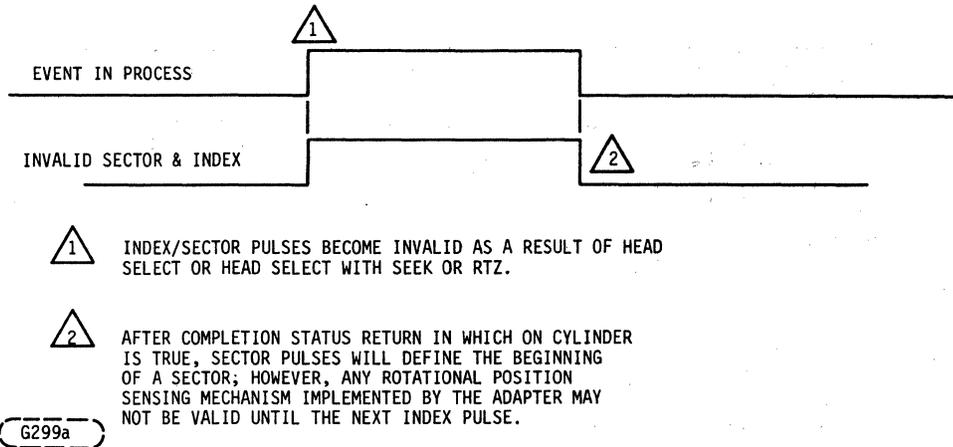
Figure 8. Index and Sector Pulse Validity
During Head Change

NOTE 3

Thirty-two equal-length sectors per
track are available via a different
device configuration (that is, dif-
ferent assembly number).

3.1.13 Read/Write Fault (R/W Fault)

The Read/Write Fault signal is a real time indicator of a
read or write fault. The adapter should monitor this sig-
nal to verify that a hardware write fault did not occur
during a read or a write function. The line is deactivated
following a Fault Reset Command bit in the Event Byte pro-
vided the fault no longer exists. Refer to Section 5.1.1,
Fault (Bit 0), which is also activated when a read/write fault
occurs.

NOTE

This signal is the only active high line
in the interface.

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3.2   DATA CABLE SIGNAL DEFINITION

The radial data cable contains real time Data and Clock lines, a Select line to enable or disable the command cable interface for daisy-chained operation, and an Interrupt Request line from the drive to signify a status change has occurred within the drive.

The data cable signals are a combination of single-ended and differential signal levels. The driver and receiver electrical characteristics are defined in Section 6.0.

3.2.1   Select

This single-ended signal from the adapter to the drive is used to enable or disable the command cable interface for daisy-chained operation. When a drive is deselected, all command cable inputs will be ignored and all command cable drivers will assume a high impedance state.

<u>NOTE</u>

The adapter need not request the current drive status when a new drive is selected unless that drive's Interrupt Request line is active.

In a daisy-chained configuration, the interface drivers and receivers will be enabled within 200 nanoseconds from the leading edge of the Select line. The interface transmitters and receivers will assume the high impedance state within 200 nanoseconds from the trailing edge of the Select line. Refer to Figure 8A.

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T1 ≤ 50 ns
T2 ≤ 40 ns
T3 ≤ 80 ns
T4 ≥ 400 ns

⚠ INDEX/SECTOR PULSE MAY BE
CLIPPED ON THE ENABLE/DISABLE
TRANSITION.
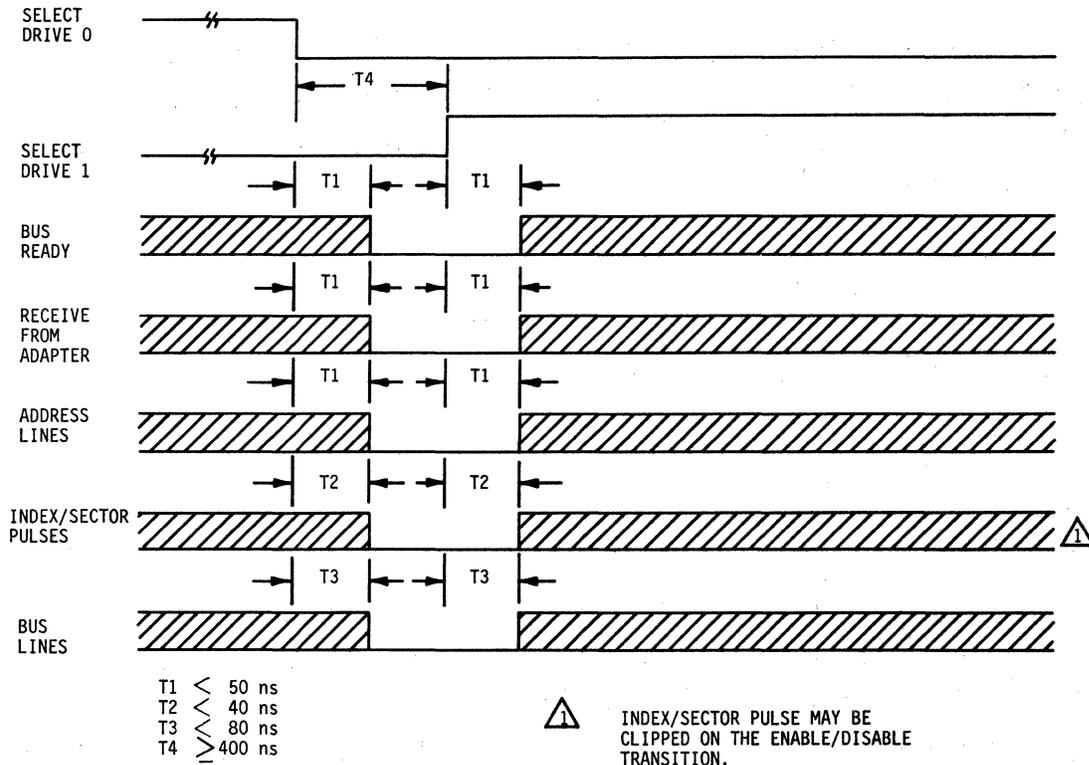
(GG108a)

Figure 8A. Deselect/Select Timing

3.2.2 Servo Clock

The differential Servo Clock (Figure 9) is a drive generated, con-
tinuously transmitted, phase-locked 9.677 MHz (nominal) clock
which must be used by the adapter to generate write clocks. Servo
Clock is not gated with Select. Servo Clock is frequently locked
to the disk rotational speed by sampling a field within the
embedded servo.

3.2.3 Read Clock

The differential Read Clock defines the beginning of a data cell.
It is an internally derived clock signal and is synchronous with
the detected data as specified in Figure 9. This signal is trans-
mitted continuously, but not in phase with data unless reading.

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Figure 9.   NRZ Data and Clock Timing
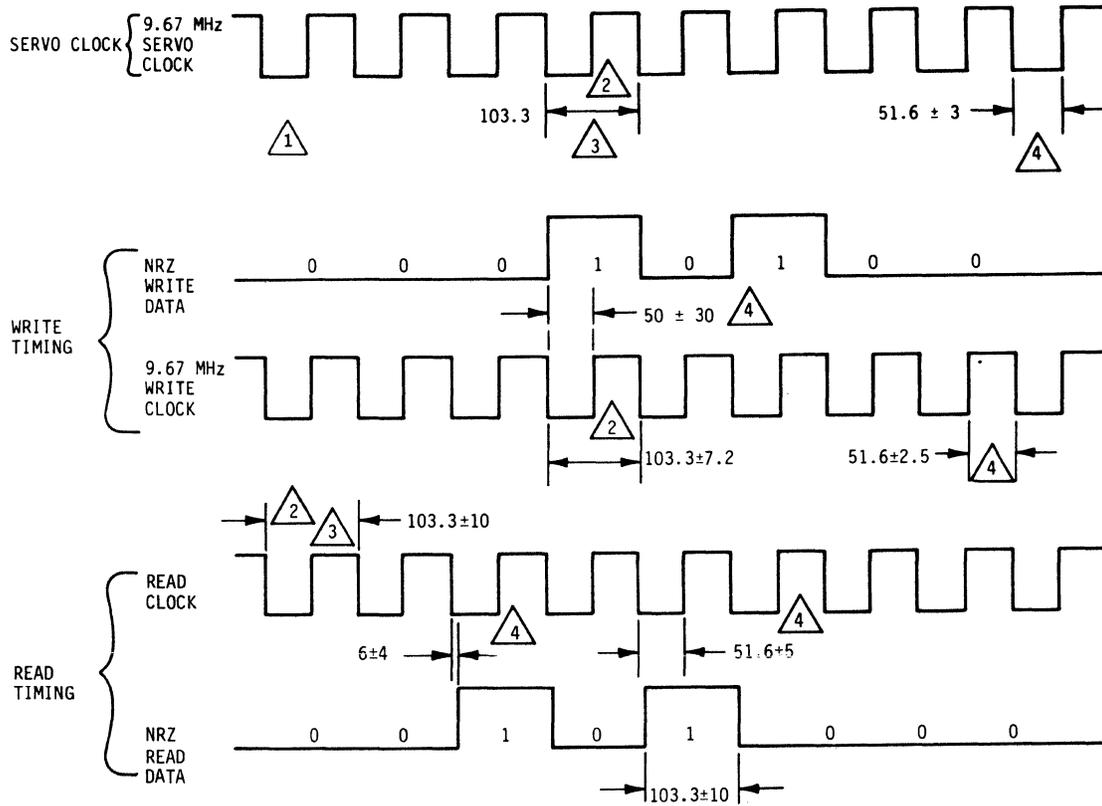
NOTES

1. ALL TIMES IN ns MEASURED AT I/O CONNECTOR OF THE DRIVE.

2. SIMILAR PERIOD SYMMETRY SHALL BE ±2 ns BETWEEN ANY TWO ADJACENT CYCLES DURING READING OR WRITING.

3. EXCEPT DURING A HEAD CHANGE OR PLO SYNCHRONIZATION THE CLOCK VARIANCES FOR SPINDLE SPEED AND CIRCUIT TOLERANCES SHALL NOT VARY MORE THAN -5.5% to +4%. PHASE RELATIONSHIP BETWEEN SERVO CLOCK AND NRZ WRITE DATA OR WRITE CLOCK IS NOT DEFINED.

4. TIMING APPLICABLE DURING READING OR WRITING.

When Read Gate in the command cable is true, Read Clock will begin phase synchronization at the end of the embedded servo zone and will be synchronized to data within 11 bytes of the PLO sync field.   Phase discontinuities may be present on Read Clock between the embedded servo field and the beginning of the PLO sync field.

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3.2.4   Read Data

This differential line transmits the recovered data in the NRZ
form (Figure 9). There is a 9-bit delay from detection of a
bit by the head until that bit is available on the Read Data
line at the drive connector. This delay results from the read
decoder circuits that convert the recorded flux reversals to
NRZ data.

3.2.5   Write Clock

This differential line transmits the Write Clock signal which
must be synchronized to the NRZ data as illustrated in Figure 9.
The Servo Clock (transmitted from the drive to the adapter) is
intended to be used by the adapter to generate the Write Clock
signal. Since the Servo Clock is synchronized to the servo
information, the Write Clock and Write Data will, therefore, be
timed precisely, irrespective of the variation in revolutions
per minute of disk speed.

The Write Clock need not be transmitted continuously, but must
be transmitted at least 250 nanoseconds prior to Write Gate.

3.2.6   Write Data

This differential line carries NRZ data which is to be recorded
on the disk pack (see Figure 9 for timing). A data bit received
at the drive connector is delayed 8-bit times before it is re-
corded. This delay results from the write encoder circuits that
convert the interface NRZ data to the coded pattern that is
written on the disk.

3.2.7   Interrupt Request

This single-ended signal signifies that a Status change has
occurred within the drive if deselected. Thus, in an interrupt-

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driven system, Interrupt Request can be used to signal seek complete with overlapping operations.

If the drive is selected, this line can be used in lieu of automatic Status returns. To use this feature, the Interrupt Mode bit within the Event Byte must be active. The adapter may respond to this line and request updated status at any time.

The Interrupt Request line will be deactivated after the adapter has activated Event and before the drive requests transmission of the Event Byte. Refer to Section 4.1.2.

4.0   BUS COMMAND DEFINITION

The Bus Commands are defined in Figure 10 and in the following paragraphs.

4.1   EVENT BYTE (ADDRESS 111)

The Event Byte (refer to Table 1 and Figure 11) consists of bit-encoded commands which are to be performed by the LMU. The drive will execute the command specified by each activated bit each time this byte is read by the drive. The adapter should deactivate all bits in the Event Byte after the drive has read the byte to prevent multiple executions of a single operation. In general, the descriptions are given as if only one command is given in the Event Byte; however, multiple commands may be given. Multiple commands that are contradictory (such as Spindle Power Off with Seek, RTZ, Head Select, or Spindle Power On) will generate a fault that can be identified by reading MC Status Codes. The normal Event Byte dialogue sequence will be ignored if contradictory commands are received. The illegal Event will cause the Interrupt Request line to become active if the Interrupt Mode had been set to a logic 1 on the last valid Event Byte transfer; otherwise, the drive will request to make a status transfer to signify the fault condition.

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BYTES RECEIVED FROM THE ADAPTER (RECEIVE FROM ADAPTER)

RECEIVE FROM ADAPTER	ADDRESS $(2^2, 2^1, 2^0)$		(MSB) ← BUS BIT → (LSB)							
			7	6	5	4	3	2	1	0
1	EVENT (111)	7	READ ESCAPE REG	SEEK	HEAD SELECT	RTZ	SPINDLE POWER ON	FAULT RESET	INTERRUPT MODE	SPINDLE POWER OFF
1	ESCAPE (000)	0	[△3]	[△3]	SERVO OFFSET MINUS	SERVO OFFSET PLUS	LOOP LOW CYL REG	SEND DEV ID	SEND MC STATUS CODE	SEND DETAILED STATUS
1	LOW CYL (110)	6	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
1	HIGH CYL (100)	4	[△3] ← RESERVED FOR HIGH CYLINDER EXPANSION →							
1	HEAD (101)	5	[△3] ← RESERVED FOR HEAD EXPANSION →						2^1	2^0

BYTES SENT TO THE ADAPTER

SENT TO ADAPTER			7	6	5	4	3	2	1	0
0	STATUS (111)	7	READY TO LOAD	WRITE PROTECTED	ON CYLINDER	UNIT READY	[△3]	SEEK ERROR	[△3]	FAULT
0	MC STATUS CODE (001)	1	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
0	DEV ID (000)	0	ID_3 [△1]	ID_2 [△1]	ID_1 [△1]	ID_0 [△1]	CB_3 [△2]	CB_2 [△2]	CB_1 [△2]	CB_0 [△2]
0	DETAILED STATUS (010)	2	STOP SWITCH	SPINDLE STOPPED	RPM OK	[△3]	[△3]	[△3]	FIXED PROTECT SWITCH	REMOVABLE PROTECT SWITCH
0	AUXILIARY (011) WHEN USED:	3	CONTENTS OF ADAPTER'S LOW CYLINDER ADDRESS (SENT BY LOOP LOW CYLINDER ADDRESS)							

[△1] DEVICE ID CODE FOR THE LMU IS 0001

[△2] DEVICE CONFIGURATION CODE
0001 = 64 SECTORS PER TRACK
0000 = 32 SECTORS PER TRACK

[△3] RESERVED - MUST BE ZERO

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Figure 10. Bus Definition

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Table 1. Valid Adapter Commands and Drive Responses

Event byte bit legend: 7 = RD ESC, 6 = SEEK, 5 = HDT SEL, 4 = RTZ, 3 = SPLIT NRS ON, 2 = FLT RS, 1 = INTER, 0 = SPIN OFF

Escape byte bit legend: 7 6 = 0 0, 5 = SV 00 OFF −, 4 = SV 00 OFF +, 3 = LOE ON PDCYL, 2 = SEND MC STSS, 1 0 = SEND MDT SS

	EVENT BYTE				ESCAPE BYTE			REQUESTED BYTES OTHER THAN ESCAPE BYTE	TRANSMISSION AT CONCLUSION OF EVENT
	7 6 / 5 4 / 3 2 / 1 0				7 6 / 5 4 / 3 2 / 1 0				
STATUS REQUEST	0 0	0 0	0 0	X 0				NONE	PRESENT STATUS [2]
ESCAPE	1 0	0 0	0 0	X 0	0 0	1 0	0 0	0 0	NONE	COMPLETION STATUS [1]
	1 0	0 0	0 0	X 0	0 0	0 1	0 0	0 0	NONE	COMPLETION STATUS [1]
	1 0	0 0	0 0	X 0	0 0	0 0	1 0	0 0	LOW CYL	AUXILIARY (LOOPED LOW CYL)
	1 0	0 0	0 0	X 0	0 0	0 0	0 1	0 0	NONE	DEVICE ID
	1 0	0 0	0 0	X 0	0 0	0 0	0 0	1 0	NONE	MC STATUS CODE
	1 0	0 0	0 0	X 0	0 0	0 0	0 0	0 1	NONE	DETAILED STATUS
	1 0	0 0	0 0	X 0	0 0	0 0	0 0	0 0	NONE	COMPLETION STATUS [1] [3]
POSITIONER EVENTS	0 1	0 0	0 0	X 0				LOW CYL	COMPLETION STATUS [1]
	0 0	1 1	0 0	X 0				HD ADDRESS	COMPLETION STATUS [1]
	0 1	1 0	0 0	X 0				1ST HD ADDR / 2ND LOW CYL	COMPLETION STATUS [1]
RTZ WITH POSITIONER EVENT	0 0	0 1	0 0	X 0				NONE	COMPLETION STATUS [1]
	0 0	1 0	0 0	X 0				HD ADDR	COMPLETION STATUS [1]
	0 1	0 1	0 0	X 0				LOW CYL	COMPLETION STATUS [1]
	0 1	1 1	0 0	X 0				1ST HD ADDR / 2ND LOW CYL	COMPLETION STATUS [1]
FLT RS WITH POSITIONER EVENT	0 0	0 0	0 1	X 0				NONE	COMPLETION STATUS [1]
	0 0	1 0	0 1	X 0				HD ADDR	COMPLETION STATUS [1]
	0 1	0 0	0 1	X 0				LOW CYL	COMPLETION STATUS [1]
	0 1	1 0	0 1	X 0				1ST HD ADDR / 2ND LOW CYL	COMPLETION STATUS [1]
FLT RS, RTZ AND POSITIONER EVENT	0 0	1 1	0 1	X 0				HD ADDR	COMPLETION STATUS [1]
	0 1	0 1	0 1	X 0				LOW CYL	COMPLETION STATUS [1]
	0 1	1 1	0 1	X 0				1ST HD ADDR / 2ND LOW CYL	COMPLETION STATUS [1]
	0 0	0 1	0 1	X 0				NONE	COMPLETION STATUS [1]
SPINDLE POWER ON	0 0	0 0	1 0	X 0				NONE	COMPLETION STATUS [1]
	0 0	1 0	1 0	X 0				HD ADDR	COMPLETION STATUS [1]
SPINDLE POWER OFF	0 0	0 0	0 0	X 1				NONE	COMPLETION STATUS [1]

NOTES

[1] COMPLETION STATUS IS AUTOMATICALLY SENT IF INTERRUPT MODE INACTIVE. IF ACTIVE, INTERRUPT REQUEST LINE IS ACTIVATED AND ADAPTER MUST REQUEST STATUS. INTERRUPT REQUEST IS RESET BY ANY EVENT.

[2] A STATUS IS RETURNED IMMEDIATELY WITHOUT SETTING INTERRUPT (INDEPENDENT OF THE INTERRUPT BIT). THE INTERRUPT BIT IN THE COMMAND SETS THE MODE FOR LATER STATUS CHANGES (I.E., DEFINES IF INTERRUPT REQUEST LINE IS SET OR STATUS IS SENT IF A FAULT OCCURS).

[3] SPECIAL CODE WHICH MAY BE USED TO TERMINATE OFFSET COMMANDS.

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SPECIFICATION FOR LARK MICRO INTERFACE
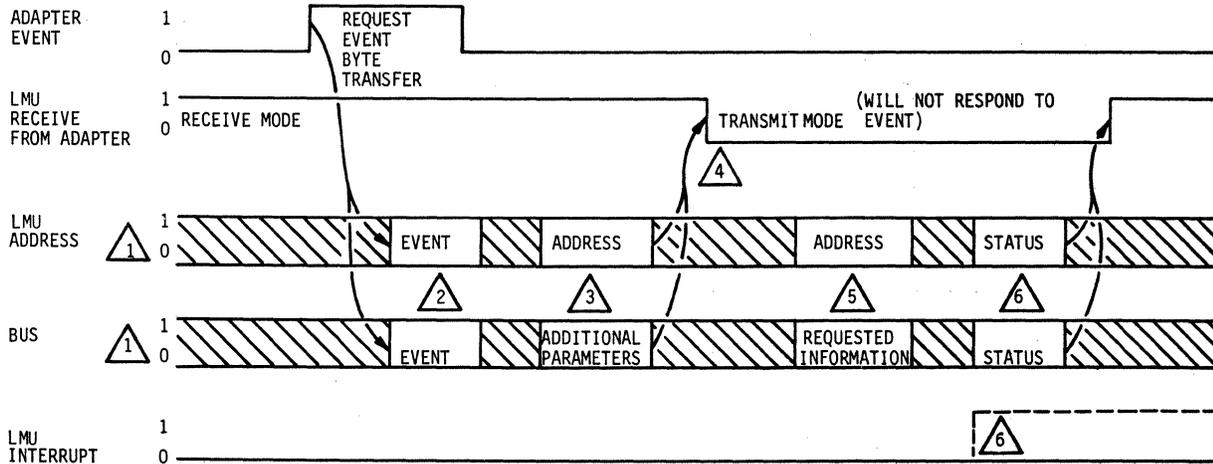
△1 ADDRESS AND BUS VALIDITY ARE DEFINED BY THE INTERLOCKED LMU BUS READY AND ADAPTER ACKNOWLEDGE SIGNALS.

△2 LMU RESPONDS TO THE ADAPTER EVENT LINE BY READING THE EVENT BYTE TO DETERMINE THE FUNCTION(S) TO BE PERFORMED.

△3 IF REQUIRED, THE LMU READS ADDITIONAL PARAMETERS FROM THE ADAPTER TO COMPLETE THE FUNCTION(S) DEFINED IN THE EVENT BYTE.

△4 LMU DEACTIVATES RECEIVE FROM ADAPTER SIGNIFYING THAT ALL REQUIRED PARAMETERS HAVE BEEN REQUESTED. ADAPTER MAY DESELECT.

△5 IF APPLICABLE(DEPENDENT ON COMMAND BITS ACTIVATED) LMU RESPONDS WITH REQUESTED INFORMATION (FOR EXAMPLE DEVICE ID).

△6 IF APPLICABLE, AND NOT IN THE INTERRUPT MODE, LMU RESPONDS WITH COMPLETION STATUS OF THE COMMAND. IF APPLICABLE AND IN INTERRUPT MODE, NO STATUS TRANSFER WILL BE REQUESTED AND THE INTERRUPT LINE WILL BE ACTIVATED.

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Figure 11. Generalized Lark Micro Interface Operation

SPECIFICATION FOR LARK MICRO INTERFACE

As a general rule, there will be one completion Status (Address 111) return for each Event or multiple Event when completed. An exception to this rule is when reading the Escape Byte (which can be viewed as an extension of the Event Byte), commands such as Loop Low Cylinder, Send Device ID, Send MC Status Codes, or Send Detailed Status will transfer the information requested without sending the customary completion Status (Address 111).

4.1.1   Spindle Power Off (Bus Bit 0)

This bit allows power to be removed from the spindle motor. If the spindle motor is up to speed, the activation of this bit should stop the spindle motor in less than 60 seconds. Completion Status will be available after the spindle has stopped.

4.1.2   Interrupt Mode (Bus Bit 1)

When inactive in the Event Byte, a transfer (usually completion Status, Table 1) will be requested by the drive at the completion of the Event, or before if Status changes due to an error condition. While in the non-Interrupt Mode, the drive should not be deselected. If the adapter cannot respond to this Status request by acknowledging Bus Ready within 500 microseconds, a Fault will be stored. Refer to Figure 6.

When active in the Event Byte, the Interrupt Request line is activated after the Event is complete, or Status changes due to an error condition. The Interrupt Request line will be reset with any new Event request.

SPECIFICATION FOR LARK MICRO INTERFACE

The Interrupt Mode, thus, provides two methods of handling Status returns: either automatically, or by request, as the user may choose.

There are, however, characteristics of each of these modes that should be considered by the user. The Auto Status mode (non-Interrupt Mode) does not require Status Request logic and is more efficient because a Status Request Event is not necessary. The adapter is expected to wait for Event completion and receive new Status.

On the other hand, the Interrupt Mode may simplify bus control logic by not allowing the drive to transmit Status without an Event. It also allows the adapter to perform overlapping operations and operate in an Interrupt-driven mode. A Status Request Event will be necessary to retrieve new Status.

When in the Auto Status mode, the user should be aware of a situation that could occur due to an unpredictable error condition within the LMU. If an error should occur before the Event dialogue sequence, the drive may request to send Status. The adapter must honor this request to avoid a subsequent Fault. After the error condition is cleared, the adapter may reinitiate the Event. In the Interrupt mode, when an error condition occurs before the Event dialogue sequence, the Interrupt Request line will be activated. The adapter should terminate the Event dialogue and honor the Interrupt Request line before attempting to complete the current Event.

4.1.3   Fault Reset (Bus Bit 2)

This bit will clear MC Status Codes and reset the fault bit in the Status Byte providing the fault condition no longer exists. Refer to section 5.1.8.

SPECIFICATION FOR LARK MICRO INTERFACE

4.1.4   Spindle Power On (Bus Bit 3)

This bit, when a logic 1, will command the drive to start the
spindle motor provided that DC power is on, AC power is on,
the control panel start/stop switch is in the start position,
and the access-door-closed and pack-in-place interlocks are
satisfied, and the Fault bit in Status is zero. To allow
operator control of the LMU via the front panel, the
default power-on condition of this bit is always considered
active. A Spindle Power Off command will disable operator
control and cause the drive to enter the remote spindle on/
off mode. The Spindle Power On command, unlike other Event
Bytes will be stored in the LMU's memory and does not
require the adapter to reissue this bit with every Event
Byte.

A single completion Status will be requested when the drive
is up to speed, heads loaded, and ready for operation.

4.1.5   Return to Zero (RTZ) (Bus Bit 4)

This bit will deactivate the seek error bit in Status, cause
the actuator to select head 0, and then seek to track 0.
Completion status as described for the Head Select and Seek
functions (sections 4.1.6 and 4.1.7) will be sent to the
adapter for this command. A head change operation will
always be performed even though head 0 may be previously
selected. Any Seek or Head Select request received in the
same Event with an RTZ will determine the cylinder or head
that will be selected after the RTZ. If the Fault status
bit is a logic 1, Status will not change and the RTZ will
not be performed if the Fault Reset bit is inactive in this
Event.

SPECIFICATION FOR LARK MICRO INTERFACE

4.1.6   Head Select (Bus Bit 5)

When this bit is a logic 1, the drive will read the Head Address Byte and perform the most appropriate action described below:

1. If the new head address is greater than 3, the drive will set the Seek Error bit in Status to a logic 1 and take no further action until an RTZ command is received from the adapter. If a valid head address other than 0 is desired, it may be issued with the RTZ Event Byte transfer as a multiple event execution. Refer to section 4.1.5.

2. If the new head address is the same as the head currently selected, there will be no action or change in Status although completion Status will be returned.

3. If a seek was requested with a valid Head Select, the following will happen: the Head and Cylinder Address Bytes will be requested from the adapter; Head Select will be performed followed by the seek operation; and at the completion of the seek, Status transmission will be requested.

4. If a valid Head Select is received without a seek in the same Event Byte, the head change will be performed immediately. On Cylinder timing will be identical to Case 3 above. In this case, the Cylinder Address Byte will not be read.

    If Seek Error or Fault is a logic 1, the Head Address Byte will be requested, but Status will not change and Head Select will not be performed although completion Status will be returned.

SPECIFICATION FOR LARK MICRO INTERFACE

4.1.7 Seek (Bus Bit 6)

This bit signifies that a seek function is to be performed.
The drive will request transmission of the adapter's Low
Cylinder Byte, and verify that the cylinder address specified
by this byte is 205 or less. If an invalid address (such as
206 or greater) is received, the drive will activate the Seek
Error bit in the Status Byte and request a Status transfer.
If the drive is unable to complete the seek within 500 milli-
seconds, the drive will activate the Fault bit in Status and
request a Status Byte transfer.

If the Seek Error bit in the Status Byte is a logic 1 or if
the Fault bit in Status is a logic 1, the cylinder address
will be requested, but Status will not change and the seek
will not be performed although completion Status will be
returned.

4.1.8 Read Escape Register (Bus Bit 7)

The drive will read the adapter's Escape Byte to determine
what additional command functions are to be executed.

4.2 ESCAPE BYTE (ADDRESS 000)

The Escape Byte consists of additional bit-encoded operations
which are to be performed by the LMU. The adapter should
deactivate all bits of the Escapte Byte after it is read by
the drive to prevent multiple executions of a single command.

The Servo Offset Plus and Servo Offset Minus commands are not
used in the LMU due to the embedded servo positioning system,
but are included for future products.

Refer to Figures 10 and 11 and Table 1.

SPECIFICATION FOR LARK MICRO INTERFACE

4.2.1   Send Detailed Status (Bus Bit 0)

This bit will command the drive to send the Detailed Status
Byte to the adapter.

4.2.2   Send MC Status Code (Bus Bit 1)

This bit commands the LMU to send one Micro-Computer (MC)
Status Code to the adapter. A memory containing up to 16
status codes is maintained within the drive as an aid in
isolating conditions that cause seek errors or faults.

The Status code byte has a double functionality providing a
detailed definition of the fault or seek error and providing
a history (trace) of the sequence of firmware activity which
lead to the fault/error condition. These codes are stored
whenever their defined Status condition occurs and a specific
descriptive code is stored for any fault or seek error. One
MC Status Code will be transferred per event beginning from
the earliest to the latest. The last Status code will be the
descriptive code for the fault or seek error and the earlier
codes can be used as a history (trace) of drive activity
leading to the fault. Each Status code that is transferred
across the interface will be cleared from memory.

All the MC Status Codes can be reset simultaneously by
issuing a Fault Reset command. Thus, if the user chooses
to issue a Fault Reset command in the Event Byte with the
normal multiple event combinations, all MC Status Codes are
cleared at the beginning of the event execution. By doing
this, only MC Status Codes will be stored relative to this
specific event (if a fault/error should occur).

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Since many of the MC Status Codes relate to drive activity
(specific firmware subroutine), the presence of codes without
a fault or seek error is normal. Thus, these codes only pro-
vide meaningful information after a fault/error condition
occurs. A skilled customer engineer can then analyze these
codes and isolate the fault cause very predictably. Refer
to section 5.2 for a definition of MC Status Code byte.

4.2.3   Send Device ID (Bus Bit 2)

This bit will command the drive to send the Device ID Byte
to the adapter.

4.2.4   Loop Low Cylinder Register (Bus Bit 3)

This bit allows an adapter-initiated loopback function to be
performed. This loopback function is intended as a diagnostic
aid in verifying operation of the Bus lines and the interface
control lines. When this command is detected, the drive will
request transmission of the adapter's Low Cylinder Byte and
then, automatically, request to send the byte to the Auxiliary
Byte Address in the adapter.

4.2.5   Servo Offset Plus (Bus Bit 4)

This bit is reserved for future drives which may require
actuator "offsets" to aid in recovering previously recorded
data which cannot be correctly read with nominal head posi-
tioning over a track. For the LMU, no actuator movement
will result from the activation of either Servo Offset Plus
or Servo Offset Minus; however, completion Status will be
sent.

SPECIFICATION FOR LARK MICRO INTERFACE

4.2.6   Servo Offset Minus (Bus Bit 5)

This bit is reserved for future drives which may require
actuator "offsets" to aid in recovering previously recorded
data which cannot be correctly read with nominal head posi-
tioning over a track. For the LMU, no actuator movement
will result from the activation of Servo Offset Minus or Servo
Offset Plus; however, completion Status will be sent.

4.2.7   Reserved (Bus Bit 6)

Because this bit is reserved for future use, it must be a
logic 0.

4.2.8   Reserved (Bus Bit 7)

Because this bit is reserved for future use, it must be a
logic 0.

4.3   LOW CYLINDER BYTE (ADDRESS 110)

This byte contains the lower eight bits of the cylinder address
for a seek command. The LSB (least significant bit) of the
cylinder address will be transmitted on Bus Bit 0; the MSB
(most significant bit) of the cylinder address will be trans-
mitted on Bus Bit 7. The drive will read this byte as a
result of receiving the seek command via the Event Byte.
(Refer to Section 4.1.7 for a definition of the Seek command.)

4.4   HIGH CYLINDER BYTE (ADDRESS 100)

This byte will contain the higher order cylinder address for
a seek command. This byte is not utilized by the LMU,
but is reserved for use in future drives.

SPECIFICATION FOR LARK MICRO INTERFACE

4.5   HEAD BYTE (ADDRESS 101)

This byte contains the new head address for a head select
command. The drive will read this byte as a result of
receiving the head select command via the Event Byte.

Head Byte Bits B7 — B0		Head Number	
00000000	0	Removable	(upper)
00000001	1	Removable	(lower)
00000010	2	Fixed	(upper)
00000011	3	Fixed	(lower)

(Refer to Section 4.1.6 for a definition of the head select
command.)

If the head byte has a value greater than 3, the Seek Error
bit in Status will become true and remain true until an RTZ
command is received.

5.0   BUS STATUS DEFINITION

5.1   STATUS BYTE (ADDRESS 111)

This byte contains the current drive status. The LMU
will request transmission of this byte as the final transfer
of any Event completion if in the Auto Status mode. If
in the Interrupt Mode, the Interrupt line will be acti-
vated and the adapter may receive the new status by trans-
mitting an all zeroes Event Byte. The Interrupt bit may be
activated or deactivated at this time. If an error condition
should occur in the LMU, a transfer of the Status Byte
will be attempted at any time either by a transfer request
(Auto Status) or by activating the Interrupt Request line.

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If the LMU is deselected and in the Auto Status mode, a Status change will be reflected by the activation of the Interrupt Request line.

5.1.1   Fault (Bus Bit 0)

This bit indicates that a fault has occurred over the interface or inside the LMU. Normal operation of the drive will not continue until this bit is reset. Prior to resetting this bit, the LMU will be internally write protected and the write protect switch LED on the operator panel will blink. This bit will be reset when a Fault Reset command is issued and the fault no longer exists. Cycling the operator panel write protect switch will generate a Fault Reset command only if the Fault bit is activ

A microprocessor within the LMU continuously monitors drive activity and checks for various fault conditions. An interface accessible section of memory is available to store pertinent information regarding these faults. Reading the MC Status Codes can identify the specific fault cause. Refer to section 5.2 for a definition of MC Status Code Byte.

5.1.2   Reserved (Bus Bit 1)

Because this bit is reserved for future use, it must be a logic 0.

5.1.3   Seek Error (Bus Bit 2)

When this bit is true, a seek error has occurred. The error bit may be deactivated only by commanding an RTZ. This bit, when true, indicates that the drive is unable to maintain track lock, or the drive has received an illegal track

SPECIFICATION FOR LARK MICRO INTERFACE

address. If an illegal cylinder address is received, the seek error bit will become a logic 1 and no positioner motion will occur. This bit will also become active for a head address greater than 3.

5.1.4   Reserved (Bus Bit 3)

Because this bit is reserved for future use, it must be a logic 0.

5.1.5   Unit Ready (Bus Bit 4)

When the drive is selected and Unit Ready is true, this bit indicates that the drive is up to speed and the heads are positioned over the recording tracks.

5.1.6   On Cylinder (Bus Bit 5)

This status bit, when true, indicates that the drive has positioned the desired head over the desired track. This status will be deactivated if the LMU detects that the selected head has failed to maintain track lock.

If the adapter should issue a seek to an invalid cylinder address, On Cylinder status will not be deactivated, the positioner will not be moved, and the seek error status bit will be set.

5.1.7   Write Protected (Bus Bit 6)

This bit, when active (logic 1), signifies that the currently addressed volume (fixed or removable) is write protected.

SPECIFICATION FOR LARK MICRO INTERFACE

It does not reflect internal write protection status (such as during faults, seeks, head selects, etc.).

<p align="center">NOTE</p>

The fixed and removable volumes may be
independently write protected. At power
turn on the removable volume is addressed.

5.1.8   Ready to Load (Bus Bit 7)

This bit indicates that the spindle has been rotating at the specified revolutions per minute for sufficient time to purge the disk chamber. If this bit remains activated after a fault condition causing a head retract, the Fault Reset command will initiate a head load sequence.

5.2   MC STATUS CODE   (ADDRESS 001)

This status code byte provides detailed information relative to micro-computer detected conditions. Sixteen bytes of wrap-around micro-computer memory are reserved for the storage of these status codes. They can be transferred across the interface (from the earliest to the latest) one byte per read MC Status Code command and then are cleared from micro-computer memory.

These codes are generally used to isolate fault or error conditions. Interpretation of most codes requires a thorough technical knowledge of the LMU and are intended to be used at a depot level maintenance activity. Definitions of these codes are beyond the scope of this specification and

SPECIFICATION FOR LARK MICRO INTERFACE

will be defined within the depot level maintenance support documentation for the LMU.

A Fault Reset command will clear all MC Status Codes.

Refer to section 4.2.2 for a definition of Send MC Status Codes.

5.3 DEVICE ID BYTE (ADDRESS 000)

This byte specifies a code to identify the LMU and also defines the number of sectors per track. The Device ID code is transmitted in bus bits 7, 6, 5, and 4 and is 0001 for the LMU. The drive configuration code is transmitted to bus bits 3, 2, 1, and 0. 0001 defines a 64-sector/track drive while 0000 defines a 32-sector/track drive. (Refer to Figure 10.) A request to send this byte to the adapter is made if commanded via the Send Drive ID bit in the adapter's Escapte Byte.

5.4 DETAILED STATUS BYTE (ADDRESS 010)

This byte is used to transmit additional hardware status information.

5.4.1 Removable Protect Switch (Bus Bit 0)

When active, the LMU will be write protected whenever the cartridge (head address 0 or 1) is selected. This line is activated via an operator changeable tab on the removable cartridge.

5.4.2 Fixed Protect Switch (Bus Bit 1)

When active, the LMU will be write protected whenever the fixed media (head address 2 or 3) is selected. This line is activated via the operator panel fixed write protect switch.

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5.4.3   Reserved (Bus Bit 2)

This bit is reserved for future products and will be a logic 0 with the LMU.

5.4.4   Reserved (Bus Bit 3)

This bit is reserved for future products and will be a logic 0 with the LMU.

5.4.5   Reserved (Bus Bit 4)

This bit is reserved for future products and will be a logic 0 with the LMU.

5.4.6   RPM OK (Bus Bit 5)

When this bit is activated, the spindle RPM is operating within the specified limits.

5.4.7   Spindle Stopped (Bus Bit 6)

When active, this bit indicates that the spindle has stopped rotating after a Spindle Power Off command or the start/stop switch has been placed in the stop position.

5.4.8   Stop Switch (Bus Bit 7)

When active, this bit indicates that one or more of the following conditions are true and the spindle will not be started:

1.   The start/stop switch on the operator panel is in the stop position.

SPECIFICATION FOR LARK MICRO INTERFACE

    2. The cartridge is not in place.

    3. The cartridge access door is not fully closed.

5.5   AUXILIARY BYTE (ADDRESS 011)

        This byte will contain the cylinder address sent from the
        adapter when a Loop Low Cylinder Address command is issued.

6.0   MICRO UNIT INTERFACE COMPONENTS

        Accessory items required, but not furnished with the drive,
        are the cables described in this section.

        All critical read/write signals are implemented using
        balanced, terminated, differential pair lines across a flat
        cable. All other signals are implemented using single-ended,
        LS TTL compatible lines. Signal lines are separated by ground
        lines to reduce crosstalk. (Refer to Figures 12 and 13 for
        pin assignments.) These ground lines must be grounded both
        at the adapter and the drive(s). Polarized connectors should
        be used on all cables to prevent reversal of ground and signal
        lines. (Refer to Figure 14.) Further component details are
        given in remaining sections.

        In order to ensure reliable interface operation and prevent
        damage to drivers or receivers, a DC ground should
        exist between the drive and the adapter. This ground should
        be carefully incorporated into the overall grounding system
        to prevent circulating ground currents. The ground connec-
        tion, while necessary, is not within the scope of this speci-
        fication.

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	Signal	Pin
⚠1	EVENT	1
	GROUND	21
⚠2	BUS BIT 0	2
⚠2	BUS BIT 1	22
⚠2	BUS BIT 2	3
⚠2	BUS BIT 3	23
⚠2	BUS BIT 4	4
⚠2	BUS BIT 5	24
⚠2	BUS BIT 6	5
⚠2	BUS BIT 7	25
	GROUND	6
⚠1	RECEIVE FROM ADAPTER	26
⚠1	ADDRESS BIT 0	7
⚠1	ADDRESS BIT 1	27
⚠1	ADDRESS BIT 2	8
	GROUND	28
⚠1	BUS READY	9
	GROUND	29
⚠1	ACKNOWLEDGE	10
	GROUND	30
⚠1	READ GATE	11
	GROUND	31
⚠1	WRITE GATE	12
	GROUND	32
⚠1	EARLY STROBE	13
	GROUND	33
⚠1	LATE STROBE	14
	GROUND	34
⚠1	INDEX	15
	GROUND	35
⚠1	SECTOR	16
	GROUND	36
⚠1	R/W FAULT	17
	GROUND	37
	GROUND	38,39,40
	SPARES	18,19,20

⚠3

DRIVE
COMMAND
CABLE
CONNECTOR

SIGNAL TYPE

⚠1 SINGLE ENDED

⚠2 BIDIRECTIONAL

⚠3 LINES ARE SHOWN IN THE ACTUAL SEQUENCE
THEY APPEAR IN THE FLAT CABLE.

(G260a)

Figure 12.   Command Cable Connector Assignments

SPECIFICATION FOR LARK MICRO INTERFACE

|			
	GROUND	01	⚠3
+	SERVO CLOCK ⚠2	14	
-	SERVO CLOCK ⚠2	02	
	GROUND	15	
-	READ DATA ⚠2	03	
+	READ DATA ⚠2	16	
	GROUND	04	
+	READ CLOCK ⚠2	17	
-	READ CLOCK ⚠2	05	
	GROUND	18	
-	WRITE CLOCK ⚠2	06	DRIVE
+	WRITE CLOCK ⚠2	19	CONNECTOR
	GROUND	07	
+	WRITE DATA ⚠2	20	
-	WRITE DATA ⚠2	08	
	GROUND	21	
	SPARE ⚠1	09	
	GROUND	22	
	SELECT ⚠1	10	
	GROUND	23	
	INTERRUPT REQUEST ⚠1	11	
	GROUND	24	
	SPARE	12	
	GROUND	25	
	SPARE	13	
	GROUND	26	
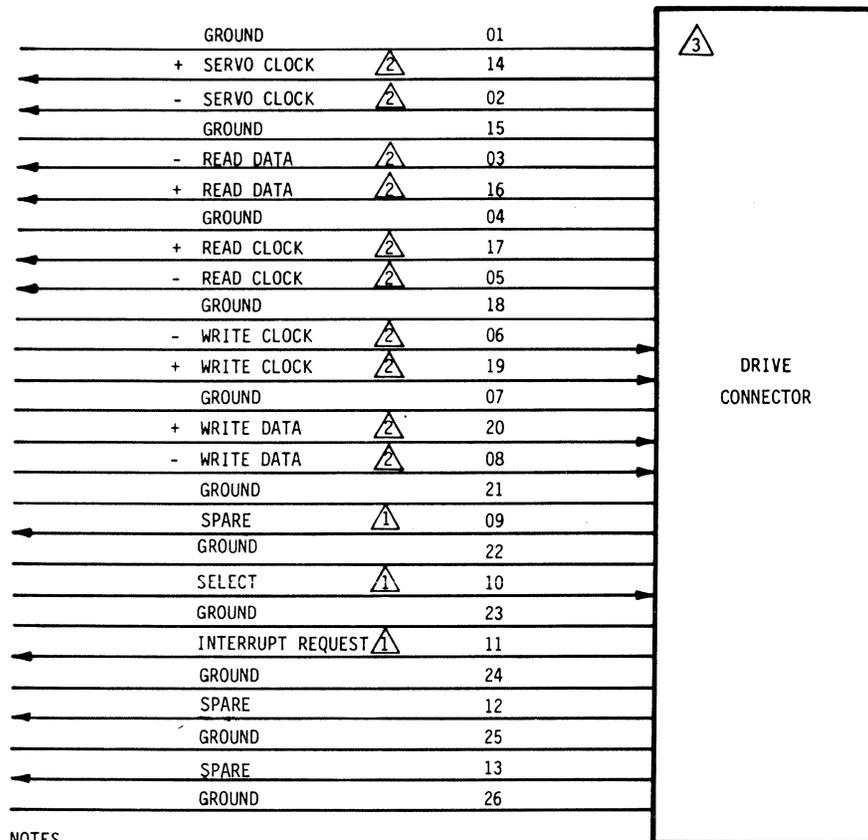
NOTES

⚠1 ACTIVE LOW, SINGLE ENDED LINES

⚠2 DIFFERENTIAL PAIR LINES

⚠3 LINES ARE SHOWN IN THE ACTUAL SEQUENCE THEY
APPEAR IN THE FLAT CABLE.

(G260b)

Figure 13. Data Cable Connector Assignments

SPECIFICATION FOR LARK MICRO INTERFACE

6.1 CABLE CHARACTERISTICS

The cables described in sections 6.1.1 and 6.1.2 may be used when cables are carefully routed and remain inside an RFI shielded enclosure. The shielded cables described in section 6.1.3 must be used to prevent RFI leakage where cables are used outside a shielded enclosure. The shield should be terminated to the outside skin of the enclosure.

6.1.1 Command Cable Characteristics

Type:	40 wire flat cable (not twisted)
Wire size:	28 AWG, 7 strand
Voltage:	300 V (maximum)
Length:	4 feet (maximum) [including all daisy chain]
Impedance:	100 Ohms
Wire spacing:	0.050 inch

6.1.2 Data Cable Characteristics

Type:	26 wire flat cable with ground plane and drain wire
Wire size:	28 AWG, 7 strand
Voltage:	300 V (maximum)
Length:	4 feet (maximum)
Impedance:	65 Ohms
Wire spacing:	0.050 inch

6.1.3 Shielded Command and Data Cable Characteristics

Type:	40/26 wire flat cables with shield and jacket
Wire size:	28 AWG, 7 strand
Voltage:	300 V (maximum)
Length:	4 feet (maximum)
Impedance:	TBD
Wire spacing:	0.050 inch

SPECIFICATION FOR LARK MICRO INTERFACE

6.2   CABLE/CONNECTOR PART NUMBERS

Following is a list of components to be used to interconnect the drive(s) to the adapter. Items 1 through 7 are heads and connectors which feature a center bar type of polarization. Refer to Figure 14.

Note that items 4 and 5 are three-sided headers which are used on the drive.
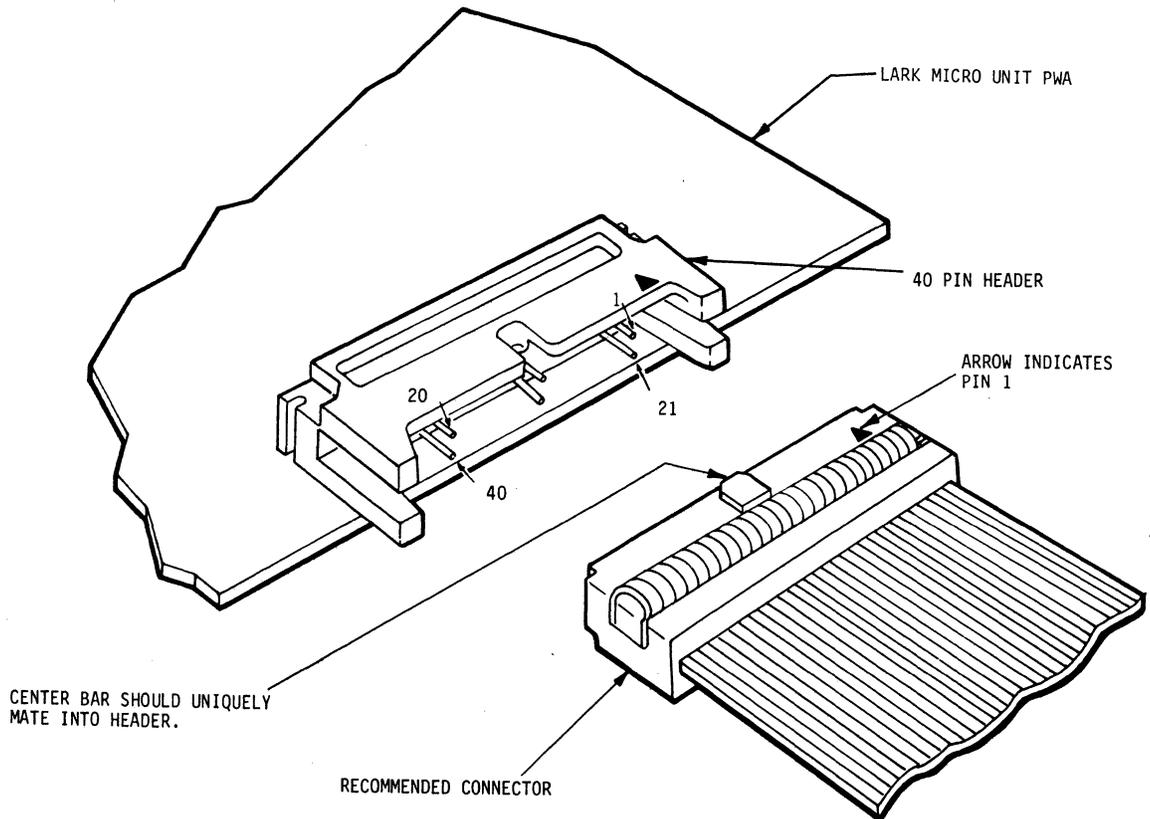
Figure 14.   Pictorial Representation of
Command Cable and Connector

SPECIFICATION FOR LARK MICRO INTERFACE

ITEM NO.	DESCRIPTION	CDC PART NUMBER	VENDOR/ PART NUMBER
1	Connector (40 conductor)	92014152-0/54-6	Berg 65948-440/640
2	Connector (40 conductor daisy chain)	92014153-8/55-3	Berg 65948-540/740
3	Connector (26 conductor)	92014136-3/38-9	Berg 65948-426/626
4	Right angle header (40 conductor)	51847515	Berg 65496-025
5	Right angle header (26 conductor)	51847513	Berg 65496-013
6	Vertical header (40 conductor)	95433303	AMP 102154-9
7	Vertical header (26 conductor)	95433301	AMP 102154-6
8	Cable (40 conductor)	65832230	3M 3365-40
9	Cable (26 conductor)	75884912-9	3M 3476-26
10	Shielded cable (40 conductor)	TBS	TBS
11	Shielded cable (26 conductor)	TBS	TBS

Items 1 and 3 are closed-end cover connectors to be used at the end of cables to prevent the cable from shorting with drive board runs. Item 2 is an open-end cover connector which can be used for daisy chaining. Items 8 through 11 are part numbers for the cables described in section 6.1.

SPECIFICATION FOR LARK MICRO INTERFACE

6.3 SINGLE ENDED TRANSMITTERS AND RECEIVERS

The true or logic 1 state of all interface signals at the drive connector is defined as a voltage level of ≤ 0.4 volts. A logic 0, a false condition, is defined as ≥ 2.4 volts. The only exception to these rules is the R/W Fault line where a logic 1 is defined as ≥ 2.4 volts and a logic 0 is defined as ≤ 0.4 volts. All times referred to within this specification are defined at the interface connector of the drive.

6.3.1 Single Ended Transmitters

All transmitters are LS TTL devices with high output current capability. All transmitters have an additional requirement of three state outputs (necessary for daisy chaining and power losses). Further requirements are given in Figure 15.

6.3.2 Single Ended Receivers

All receivers are LS TTL compatible with 200 mV (minimum) hysteresis. The clamping diode at the input of the receiver is used to terminate the line high-to-low transitions. All low-to-high transitions are slow enough that characteristic impedance termination should not be needed. The termination resistors shown in Figure 15 minimize induced current problems and hold the inputs high whenever lines are not being driven. Note that this automatically disables the interface whenever a cable is disconnected or power is lost on one side of the cable. Also note that a read/write fault is generated whenever the cable is open or power is lost at the drive. Further receiver characteristics are shown in Figure 15.

6.3.3 Single Ended Transceivers

Transmit and receive requirements for the bidirectional transceivers are identical to those discussed in sections 6.3.1 and 6.3.2. Thus, the transceiver function may be accomplished using components recommended in those sections. Other wiring information may be found in Figure 16.

SPECIFICATION FOR LARK MICRO INTERFACE
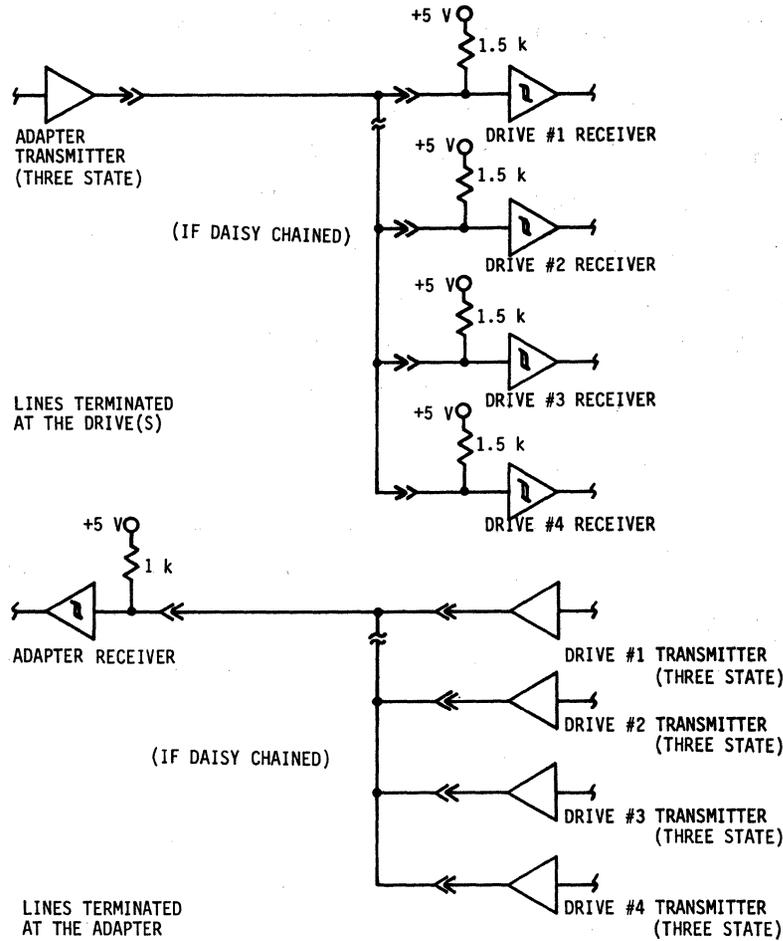
TRANSMITTER REQUIREMENTS

PARAMETER	CONDITION	MIN	MAX	UNIT
HIGH LEVEL OUTPUT VOLTAGE		2.4	5.3	V
LOW LEVEL OUTPUT VOLTAGE	I_{OUT} = 12 mA		0.4	V
LOW LEVEL OUTPUT VOLTAGE	I_{OUT} = 24 mA		0.5	V
THREE-STATE OUTPUT CURRENT			100	µA

RECOMMENDED LS TRANSMITTERS:
74LS240, 74LS244 or 74LS374

RECEIVER REQUIREMENTS

PARAMETER	CONDITION	MIN	MAX	UNIT
HIGH LEVEL INPUT VOLTAGE		2.0	7.0	V
LOW LEVEL OUTPUT CURRENT	V_{IN} =2.7 V		20.0	µA
LOW LEVEL INPUT VOLTAGE			0.8	V
LOW LEVEL INPUT CURRENT	V_{IN} =0.4 V		0.4	mA
INPUT HYSTERESIS		200		mV
MAX INPUT VOLTAGE			7.0	V
INPUT CLAMPING	I_{IN} = -18mA		-1.5	V

RECOMMENDED LS RECEIVERS:
74LS14, 74LS240 or 74LS244

NOTE: MULTIPLE DRIVES MAY ALSO BE CONNECTED BY RADIAL CABLES.

(G053)

Figure 15. Single Ended Transmitters/Receivers

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+5V 1.0k

ADAPTER TRANSCEIVER
(OR RECEIVER/TRANSMITTER)

(IF DAISY CHAINED)

+5V 1.5k   DRIVE #1

+5V 1.5k   DRIVE #2

+5V 1.5k   DRIVE #3

+5V 1.5k   DRIVE #4

1. TRANSMITTER AND RECEIVER
    ELECTRICAL REQUIREMENTS
    ARE THE SAME AS GIVEN IN
    FIGURE 15.

2. MULTIPLE DRIVES MAY ALSO
    BE CONNECTED BY RADIAL
    CABLES.

G028b
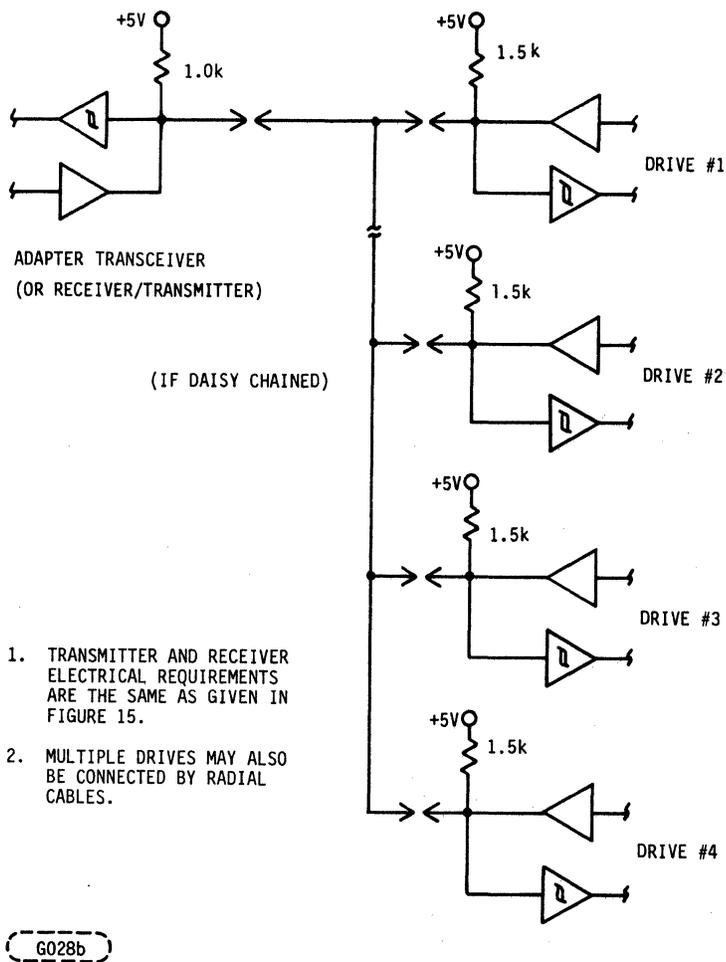
Figure 16.   Single Ended Transceivers
(Used on Bus Lines)

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6.4 DIFFERENTIAL SIGNAL CHARACTERISTICS

Transmitters and receivers of the industry standard types 75110A and 75107 or equivalent are used to provide a terminated, balanced transmission system.

6.4.1 Differential Transmitter Characteristics

The device controller line transmitters are compatible with the line receiver described in section 6.4.2.

Output signal levels are shown in Figure 17.

The transmitter is connected to the input/output line such that the output labeled "-" connects to the low order pin number of the data cable connector, and the output labeled "+" connects to the high order pin number of the data cable connector. Figure 13 contains connector pin assignments.

A logic 1 on the interface is defined when the "+" output is more positive than the "-" output.

6.4.2 Differential Receiver Characteristics

The device controller input amplifier is compatible with the transmitter described in section 6.4.1.

Input signal levels are shown in Figure 17.

The differential receiver is connected to the input/output line such that the input labeled "-" connects to the low order pin number of the data cable connector, and the output labeled "+" connects to the high order pin number of the data cable. Figure 13 contains connector pin assignments.

SPECIFICATION FOR LARK MICRO INTERFACE

A logic 1 on the interface is defined when the "+" is more positive than the "-" input line.

A terminator resistor as shown in Figure 17 is required at the receiver end of each transmission line of the data cable. This resistance is provided for the receivers located within the drive.

NOMINAL - LINE $\quad$ 0V

LOGIC 0 $\qquad$ LOGIC 1 $\begin{cases} 1.21 \text{ V (MAX)} \\ 0.623 \text{ V (MIN)} \end{cases}$

NOMINAL + LINE $\quad$ -0.715 V

$10 \text{ ns} \leq T_r \leq 35 \text{ ns}$, 10% to 90% LEVEL
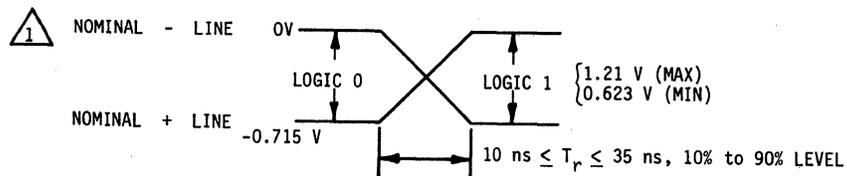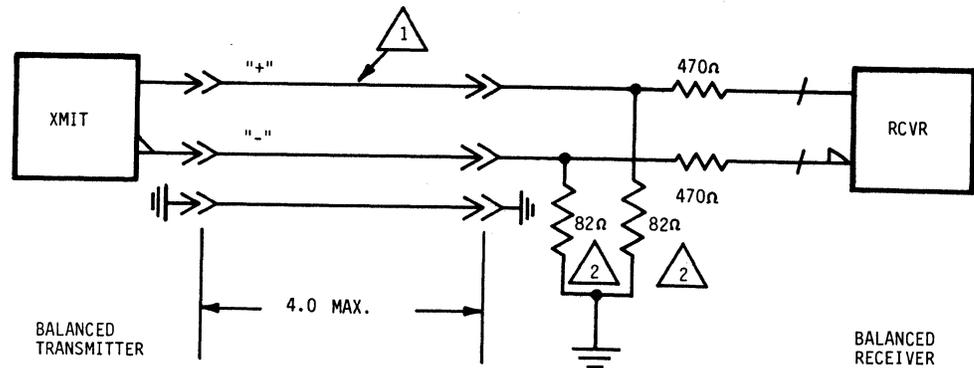
2. TERMINATOR RESISTORS ARE LOCATED AT THE RECEIVER END OF THE CABLE ON DRIVE LOGIC CARD OR IN ADAPTER. THESE SIGNALS MUST BE RADIALLY CABLED.

G028a

Figure 17. Differential Drivers/Receivers
(Used on Read/Write Lines)

SPECIFICATION FOR LARK MICRO INTERFACE

7.0   DATA FORMAT AND DATA CONTROL TIMING

7.1   FORMAT DEFINITION

The sector format on the disk is determined by the adapter
except for the Embedded Servo field. The Index and Sector
pulses are available for use by the adapter to indicate the
beginning of a track or sector. A suggested format for fixed
data records is shown in Figure 18.
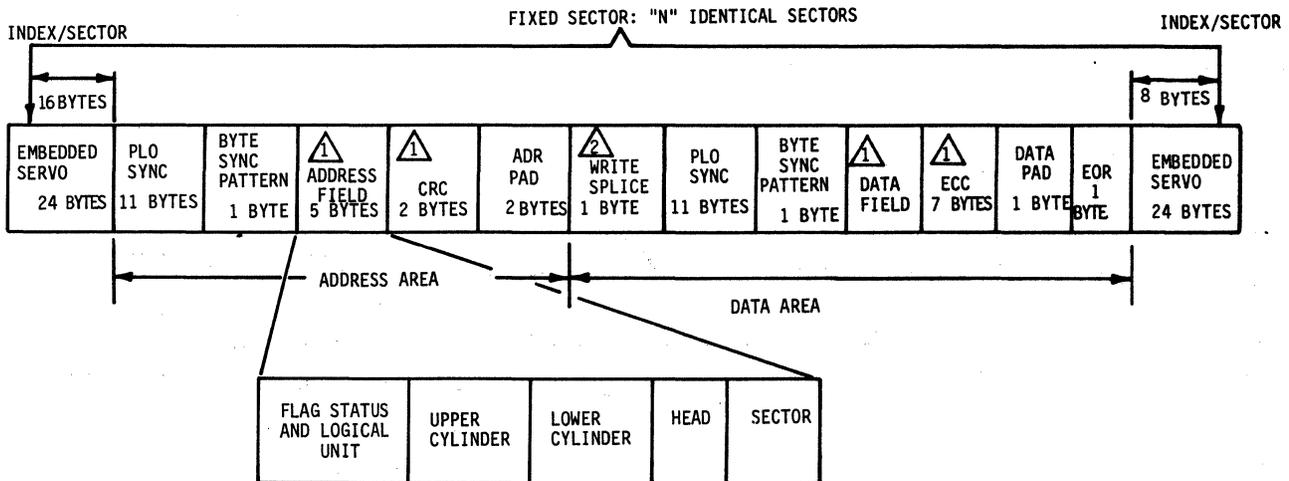
EXAMPLE NO. 1: DATA FIELD LENGTH USING 64 SECTORS

$$\text{DATA FIELD} = \frac{\text{TOTAL BYTES/TRACK}}{\text{NUMBER OF SECTORS/TRACK}} - (\text{SYNC FIELDS, TOLERANCE GAPS, AND ADDRESS})$$

$$\text{DATA FIELD} = \frac{20,672}{64} - 67$$

DATA = 256 BYTES/SECTOR

$$\% \text{ EFFICIENCY} = \frac{256 \times 64}{20,672} = 79\%$$

⚠1 THESE AREAS ARE EXAMPLES ONLY AND MAY BE STRUCTURED TO SUIT INDIVIDUAL CUSTOMER REQUIREMENTS.

⚠2 THIS WRITE SPLICE BYTE IS IN THIS LOCATION AS A RESULT OF A RECORD UPDATE, FOR FORMATTING CONSIDERATIONS
THIS BYTE MAY BE ALLOWED FOR AT THE END OF THE DATA SECTOR BY INCREASING THE NUMBER OF EOR (END OF RECORD)
BYTES FROM 1 TO 2.

(Z271a)

Figure 18.   Sector Format

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The format presented in Figure 18 consists of three functional areas: Embedded Servo, Address, and Data. The Data area is used to record the system's data files. The Address area is used to verify the track and sector location on the disk.

Figure 18 shows data as recorded on the disk. The adapter must allow for the delays in the encoder in order to maximize data storage.

7.1.1   Embedded Servo Area (Figure 18)

The Embedded Servo area is 24 bytes long and is permanently preformatted on each track. It contains information for the drive's positional servo electronics. This area is used solely by the drive and is not accessible by the adapter, although the adapter must allow for its existence.

NOTE

The LMU will internally ignore Read or Write Gate during the Embedded Servo area.

This area also serves as an interrecord gap between sectors to allow adapter decision-making time.

7.1.2   Address Area (Figure 18)

The Address area is used to provide a positive indication of the track and sector locations. The Address area is normally read by the adapter and the address bytes verified prior to a Data area read or write. The Address area is normally written

SPECIFICATION FOR LARK MICRO INTERFACE

by the adapter only during a format function (section 7.2) and, thereafter, only read. The Address area consists of the following bytes.

1. PLO Sync (11 bytes minimum). These 11 bytes of zeroes are required by the drive to allow the drive's read data phase locked oscillator (PLO) to become phase and frequency synchronized with the data.

2. Byte Sync Pattern (1 byte). This byte is user-defined; it indicates to the adapter the beginning of the address field information, and it establishes byte synchronization (ability to partition this ensuing serial bit stream into meaningful information groupings, such as bytes).

3. Address Field. These bytes are user-defined and interpreted by the adapter. A suggested format consists of five bytes, which allows one byte to define flag status bits or logical unit number, two bytes to define the cylinder address, one byte to define the head address and one byte to define the sector address. (Although one byte of cylinder address is sufficient for the current LMU cylinder address, two bytes are suggested for future enhancements and/or Micro Unit family compatibility.)

4. CRC (2 bytes recommended) - (Address Field Check Codes). Selection of an appropriate error detection mechanism, such as a Cyclic Redundancy Check code, is made by the user and written after the address during formatting. These codes are generated by the adapter and used to verify address integrity.

SPECIFICATION FOR LARK MICRO INTERFACE

5. <u>ADR Pad</u> (2 bytes) - (Address Field Pad). The address field pad must be written by the adapter to ensure that all of the address field will be recovered. This pad is necessary due to an eight-bit write encoder delay.

7.1.3   Data Area (Figure 18)

The Data area is used to record the user's data files. The contents of the data fields within the Data area are specified by the host computer system. The remaining fields of the Data area are specified and interpreted by the user's adapter to recover the data fields and ensure their integrity. The Data area consists of the following bytes:

1. <u>Write Splice</u> (1 byte). This byte is required by the drive to allow time for the write drivers to turn on and reach a recording amplitude sufficient to ensure data recovery. This byte should be allowed for in the format and is described in greater detail in section 7.2.

2. <u>PLO Sync</u> (11 bytes). These 11 bytes of zeroes are required when reading to allow the drive's phase locked oscillator (PLO) to become phase and frequency synchronized with the data bits recorded on the media.

3. <u>Byte Sync Pattern</u> (1 byte). This byte is user-defined and indicates to the adapter the beginning of the Data Field bytes and establishes byte synchronization for the Data Field.

4. <u>Data Field</u> (256 bytes with 64 sectors per track, or 512 bytes with 32 sectors per track). The Data Field contains the host system's data files.

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5. ECC (7 bytes maximum) - (Data Field Check Codes). Error Correction Codes (ECC) are user-defined and provide error detection and correction capability for the Data Field. The use of ECC is recommended but is not mandatory.

6. Data Pad (1 byte) - (Data Field Pad). The Data Pad byte must be included by the adapter and is required by the drive to ensure proper recording of the last bits of the Data Field Check Codes.

7. End of Range (EOR) (1 byte). This byte is required by the drive to account for electromechanical tolerances. It is not necessarily read or written, but must be allocated in the sector format design.

7.1.4   Read/Write Timing Considerations

1. All timing references are at the drive input/output connector.

2. Allowance for propagation delay of the interconnecting cables and adapter circuits is a critical element of adapter design and is outside the scope of this specification.

3. Because of encoder delay, interface write data is delayed by eight bits before it is recorded. Write Gate must remain active until the end of the pad after the Address area or Data area.

4. Because of decoder delay during a read operation, data will appear at the drive connector nine bits after being sensed by the head.

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7.2   WRITE FORMAT PROCEDURE

Provisions must be made within the adapter to format the disk. The sector format shown in Figure 19 has been defined to account for restrictions placed on the format by the drive as well as functionality required by the adapter.

The following procedure is recommended for fixed sector formats with separate Address and Data fields.

1.   Select the desired drive, cylinder, and head.

2.   The adapter must wait for On Cylinder before proceeding. This ensures that the drive will be ready to write when the leading edge of Index (or Sector) is detected.

3.   Search for the leading edge of the desired Index/Sector pulse.

NOTE

The Index pulse provides a common rotational reference for each track and is considered the sector pulse for sector zero.

4.   After detecting the leading edge of the selected Index/ Sector pulse, activate Write Gate and start transmitting zeroes.

Format 19. Format Timing
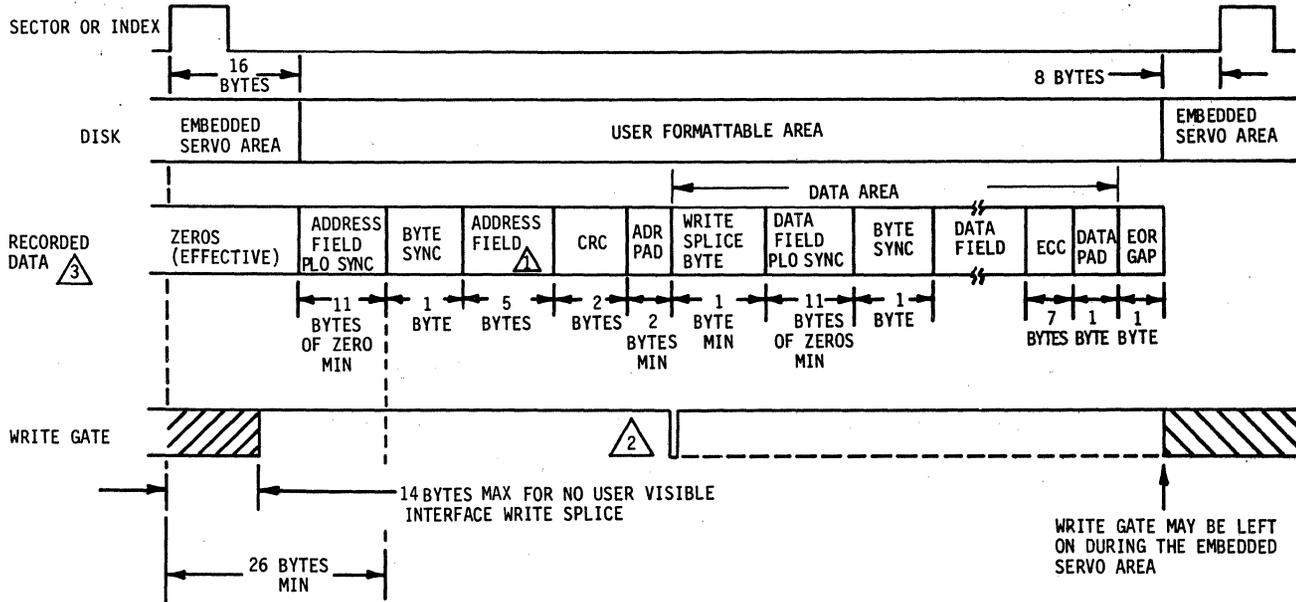
△1 THE ADDRESS FIELD INCLUDES THE CYLINDER HEAD AND SECTOR LOCATION.

△2 WRITING THE DATA AREAS ARE OPTIONAL. THESE AREAS ARE USEFUL TO VERIFY
THE INTEGRITY OF THE SECTOR IF THE ADAPTER READ VERIFIES THESE AREAS
AFTER A FORMAT OPERATION WHICH ALSO WRITES THE DATA AREAS. IF DATA
FIELDS ARE TO BE WRITTEN, WRITE GATE MUST BE DEACTIVATED FOR A MINIMUM
OF ONE BIT TIME AFTER THE ADDRESS PAD.

△3 SHOWS DATA AS RECORDED ON THE DISK. TRANSMISSION OF THIS DATA BEGINS
8 BITS EARLIER TO ALLOW FOR ENCODER DELAY.

△4 THIS FIGURE IS NOT DRAWN TO SCALE.

(G030a)

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NOTE

The Embedded Servo area is write protected
by the drive. Data transmitted to the
drive by the adapter during the Embedded
Servo time will not be written on the disk;
however, to control Write Splice timing be-
tween the Embedded Servo area and the
address PLO Sync field, it is recommended
that the adapter activate Write Gate and
begin transmitting all zeroes no later
than 14 byte times after the leading edge
of the Index/Sector pulse. If Write Gate
is activated within the recommended time,
Write Splice will be masked by the Embedded
Servo area.

5. Transmit all zeroes during the Embedded Servo area
   (beginning no later than 14 byte times after the leading
   edge of the sector pulse) and for the address PLO Sync
   field (11 bytes minimum). This is equivalent to trans-
   mitting a minimum of 26 bytes of zeroes from the leading
   edge of the sector pulse.

6. Transmit a Byte Sync pattern, the Address Field, and the
   CRC (address field check codes).

7. Transmit all zeroes for the Address Pad bytes and the
   Write Splice Byte. Terminate Write Gate during the last
   four bits of the Write Splice Byte.

8. If a Data Field is to be written, proceed to step 9; if
   no Data Field is to be written, proceed to step 11.

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9. Reinitiate Write Gate at the end of the Write Splice Byte of step 7. Transmit all zeroes for a Data Field PLO Sync (11 bytes minimum), transmit the Byte Sync pattern, the desired Data Field, and the ECC bytes.

10. Transmit all zeroes for the Data Pad and EOR Gap bytes (2 bytes minimum).

11. The adapter may now proceed to step 1 if the entire track has been formatted or proceed to step 3 if additional sectors on this track are to be formatted.

    If additional sectors on the track are to be formatted, the adapter may leave Write Gate turned on until the next Sector pulse is detected and then proceed to step 4. (If sequential sectors are to be formatted, Write Gate may be continuously left on, but the adapter timing must be re-initialized with each Sector pulse.)

This format procedure has allowed three bytes (Adr Pad and Write Splice Byte) between the last bit of the CRC and the first bit of the Data Field PLO Sync. However, if during formatting, Write Gate is enabled relative to the Sector pulses and the Address and Data areas are written consecutively (that is, no physical Write Splice is created between the Address and Data areas), then only the Adr Pad bytes are required provided that two EOR Gap bytes are inserted at the end of the Data Pad. Note that this format variation is still compatible with the recommended Write Format procedure since a splice will be created per Figure 20 when a record update function is performed, redistributing the 2-byte EOR to a 1-byte EOR field and generating the Write Splice Byte.

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7.3   READ/WRITE CONTROL TIMING (Figure 20)

The objective of this section is to specify the interrelation-
ship of the drive interface control leads necessary to recover
or record data fields on a formatted disk media. The format
of Figures 18 and 20 will be assumed; however, critical drive-
dependent parameters will be summarized to enable adapter
variations in the read/write timing.

To perform a Data Field read function, the Address area is
read and verified, then its Data area is read. To perform a
Data field write function, the Address area is read and veri-
fied, then the Data area is written. The following sections
will expand on these concepts.

7.3.1   Read Function

The read function consists of reading the Address field and
then the Data field. The critical interface lines associated
with a read function are the Sector (Index) pulses, Read Gate,
Read Clock, Read Data, and Servo Clock lines.

Address Field Read (Figure 20)

The location of the Address Field is defined relative to the
Sector (Index) pulse. To recover the Address Field the adapter
waits for the leading edge of a Sector (Index) pulse. Read
Gate must be activated within 128 maximum Servo Clock periods
after the leading edge of the Sector (or Index) pulse. The
leading edge of Read Gate forces the phase locked oscillator
to synchronize on the Address PLO Sync field. Read Gate also
enables the read data output of the data separator after fre-
quency and phase synchronization is established. Synchronization

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to the Address PLO Sync pattern will not begin until the end of the Embedded Servo area. If the adapter initiated a sector format function at least two bytes prior to the end of the Embedded Servo area, Read Gate may be activated during the Embedded Servo area with internal drive logic accounting for the write splice between the Embedded Servo area and the Address PLO Sync field.

Read Data will be valid within the 11 byte Address PLO Sync area after the concurrence of Read Gate and the PLO Sync field. Read Clocks are transmitted continuously and will be in phase and frequency synchronization with the Read Data within the 11 byte PLO Sync area after the concurrence of Read Gate and the PLO Sync field. The Read Data line will be a logic 0 until the first one bit of the Byte Sync Pattern is detected. It is then the adapter's responsibility to establish byte synchronization, perform the address field verification, and interpret the address field check codes (CRC). Read Gate may be deactivated after the last bit of the address CRC is received by the adapter and must be deactivated no later than one bit prior to a Write Splice Area.

For example, consider the format shown in Figure 20. This example has a Write Splice Area located on the disk two bytes after the Address CRC. (The creation of the Write Splice Area will be explained in section 7.3.2). An examination of the Interface Data (Read) timing signal reveals that the Interface Data (Read) is delayed by nine bit times from data recorded on the media. Thus, to meet the requirement that Read Gate must be deactivated at least one bit prior to a Write Splice area requires that, for the format shown in Figure 20, Read Gate must be deactivated within six bit times after the reception of the last bit of the Address CRC by the adapter.

SPECIFICATION FOR LARK MICRO INTERFACE
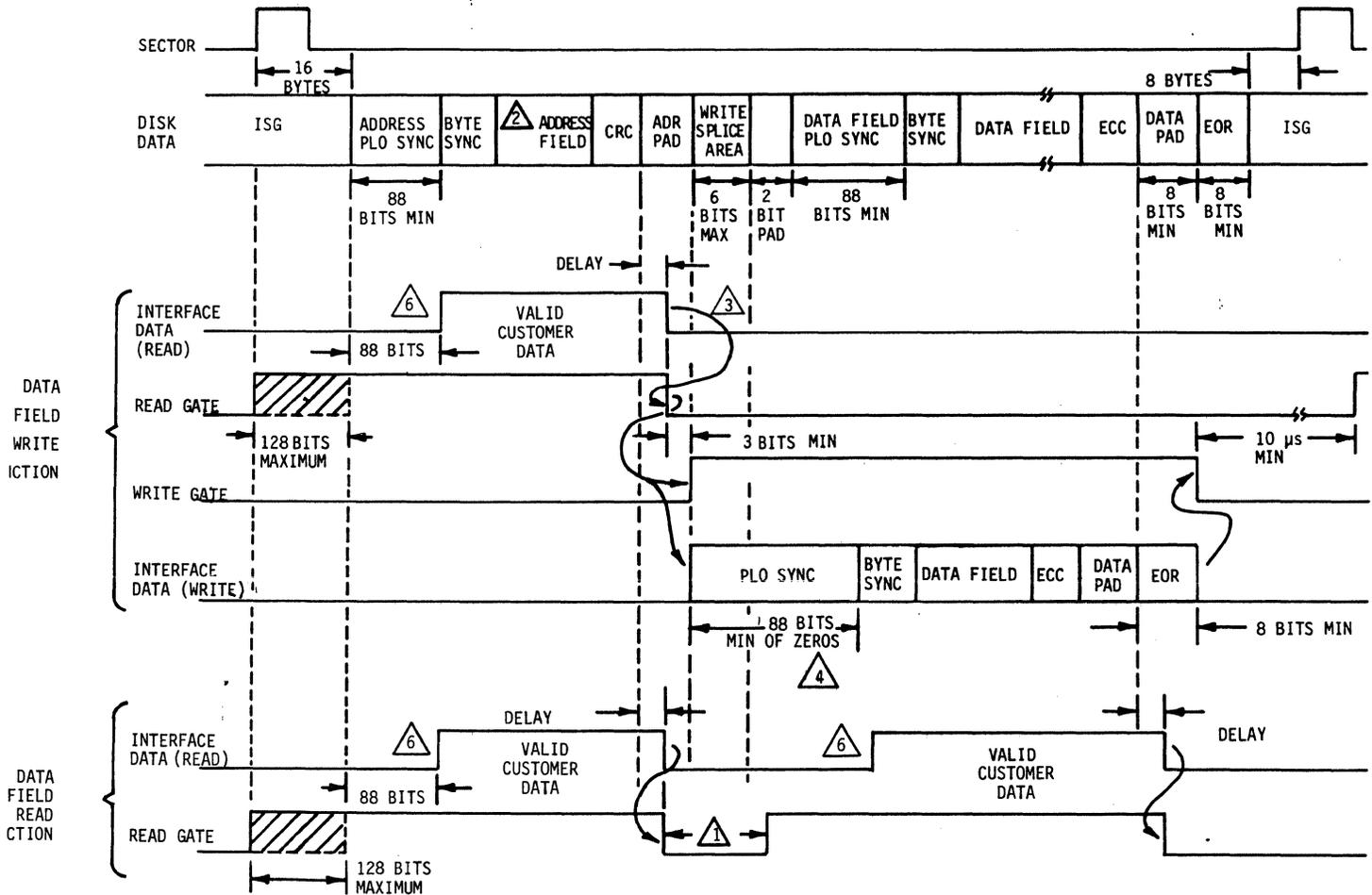
△1 READ GATE MUST BE DEACTIVATED PRIOR TO THE WRITE SPLICE. IT MUST BE REINITIATED AT LEAST ONE BIT AFTER THE WRITE SPLICE AND WITH AT LEAST 11 BYTES OF PLO SYNC REMAINING IN THE SYNC FIELD.

△2 THE ADDRESS FIELD INCLUDES THE TRACK, HEAD, AND SECTOR LOCATION.

△3 CABLE/ADAPTER DELAY NOT SHOWN.   ALL TIMING SPECIFIED AT THE DRIVE CONNECTOR.

△4 THE WRITE SPLICE BYTE WILL BE PROVIDED BY THE DRIVE ENCODER.

△5 THIS FIGURE IS NOT DRAWN TO SCALE.

△6 DATA IS VALID AND GUARANTEED TO BE ZEROS.

(G052a)

* VALUES ARE FOR THIS EXAMPLE.

Figure 20. Typical Read/Write Timing

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The adapter may compare the contents of the disk media recorded address field to the desired sector location as they are received from the drive. However, a valid comparison should not be assumed until the CRC bytes have been used to validate the Address Field. If the recorded and desired Address Fields compare and no check code error is detected, then the desired sector has been found.

Data Field Read (Figure 20)

After the desired sector location has been found, the Data Field may be read. When a Data Field is updated, a six-bit-wide Write Splice Area is created on the media. (See section 7.3.2.) Read Gate must be deactivated a minimum of one bit time preceding a Write Splice area and must be activated a minimum of one bit after a Write Splice Area.

For example, consider the format shown in Figure 20. To satisfy the Read Gate/Write Splice timing requirements, Read Gate could be deactivated as soon as the last bit of the Address CRC was received by the adapter and reactivated 14 bit times following deactivation. The example chose to deactivate Read Gate as soon as the last bit of the Address CRC was received (versus deactivating Read Gate six bit times after the last bit of the Address CRC) for timing compatibility with the Data Field update function (section 7.3.2) which assumed this timing relationship to enable Write Gate and create the Write Splice Area in the location shown in Figure 20.

Per Figure 20, if Read Gate is activated after Write Splice and at the beginning of the Data Field PLO Sync area, the interface Read Data lines will be valid within the 11 byte PLO Sync area. (The two-bit pad following the Write Splice area allows Read

SPECIFICATION FOR LARK MICRO INTERFACE

Gate to be activated a minimum of one bit time after the Write
Splice area and still ensures 11 bytes of Data Field PLO Sync
area. The adapter may then search for the Data Byte Sync
pattern, establish byte synchronization, and read the Data
field plus read and interpret the Data ECC. Read Gate may be
deactivated after the last bit of the data ECC is received. In
the example illustrated by Figure 20, Read Gate was reactivated
14 bit times after reception of the last bit of the address
check code to ensure that Read Gate would always be reactivated
after Write Splice under worst case tolerances.

Summary of Critical Read Function Timing Parameters

Adapter variations of the read timing are allowed if the
following drive-dependent parameters are met:

1. Read Initialization Time.

    A read or write may not be initiated until On Cylinder is
    true following a Seek command or a Head Select command.

2. Read Gate Timing

    Requesting the drive to establish synchronization (that is,
    enabling Read Gate) for the Address area should be done no
    later than 128 bits from the leading edge of a Sector (Index)
    pulse and at least 11 bytes prior to the Address field Byte
    Sync pattern.

    Read Gate may not be enabled or true during a Write Splice
    area. (Read Gate must be deactivated one bit time minimum

before a Write Splice Area and must be enabled one bit time
minimum after a Write Splice Area.)

NOTE

Data (Read) at the interface is delayed
by nine bit times from the data recorded
on the disk media.

7.3.2   Write Function (Figure 20)

The Write function consists of reading the Address field to
verify the sector location, and then writing the Data Field
PLO Sync characters, the Byte Sync pattern, the Data Field,
the Data Field ECC and a Data Pad byte. The critical inter-
face lines associated with the write function are the Write
Gate, Write Data, and Servo Clock lines.

Read Address Field Prior to Write

The Address Field and Address CRC should be read and verified
prior to writing the Data area, except while formatting.

Write Splice Creation

The last Interface Data (Read) bit of the Address CRC will be
delayed by nine bit times from the recorded disk location.
Thus, if the adapter deactivates Read Gate when the last bit
of the Address CRC is detected, the read/write head will be
located a maximum of nine bit times into the Adr Pad. When
Read Gate is deactivated, Write Clocks to the drive should be
enabled. (The LMU requires Write Clocks to precede Write Gate
a minimum of 250 nanoseconds.)

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The adapter must provide three Servo Clock periods (minimum) of delay (approximately 0.3 microsecond) between the trailing edge of the Read Gate signal and the leading edge of the Write Gate signal. This delay will allow for signal propagation tolerances and prevent a possible overlap of the Read and Write Gate in the drive.

Thus, from Figure 20, if the Read Gate was deactivated when the last Interface Data bit of the Address CRC was received by the adapter and the Write Gate was activated three Servo Clock periods after this last bit was received, a Write Splice Area would be created at the location shown in Figure 20 (that is, the Write Splice Area on the media would start 16 bit times from the last bit of the recorded Address CRC). In addition, if Write Clocks were enabled when Read Gate was deactivated, the drive requirement for Write Clocks to precede Write Gate by 250 nanoseconds would also be satisfied.

Since the write driver turn-on delay plus data encoder turn-on delay is six Servo Clock periods (maximum) from the leading edge of Write Gate, the width of the Write Splice area recorded on the media will be six Servo Clock periods (maximum).

PLO Sync Field Write

The PLO Sync field must consist of 11 valid and recoverable bytes of interface data zeroes. From Figure 20, a two-bit Pad area is shown between the six-bit Write Splice Area and the start of the Data Field PLO Sync. This two-bit Pad area

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allows Read Gate to be enabled one bit minimum after a Write
Splice and be valid at the drive interface prior to the Data
Field PLO Sync bytes. Since the Write Splice data is provided
by the encoder and the write data is delayed by eight bits in
the encoder, transmission of the 11 byte PLO Sync field will
begin as noted in Figure 20.

Byte Sync, Data Field, ECC, and Data Pad Write

After the Data Field PLO Sync field is written, a Byte Sync
character should be written to enable the adapter to establish
synchronization for the Data Field.

After the Data Field is written, the Data ECC should be
written followed by a one-byte Data Pad at the end of
the ECC field to ensure proper recording and recovery of
the ECC codes.

NOTE

In addition to these requirements, an
additional 1 byte End of Record (EOR)
field should be allowed for in the
format design to allow for overall
system tolerances.

After the Data Pad byte is written, Write Gate should be
deactivated and Read Gate should not be activated to read the
Address area of the next sector within 128 maximum Servo Clock
periods after the next Sector pulse is detected. This will
allow ample time for the write-to-read recovery time (that is,
the 10 microseconds minimum between the trailing edge of Write
Gate and the leading edge of Read Gate).

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Summary of Critical Write Function Parameters

Adapter timing variations in the record-update function are allowed if the following drive-dependent write (and inter-related read) timing parameters are met:

1. <u>Read-to-Write Time</u>. Assuming head selection is stabilized, the time lapse from disabling Read Gate to enabling Write Gate shall be three Servo Clock periods minimum.

2. <u>Write Clock-to-Write Gate Timing</u>. Write clocks must precede Write Gate by a minimum of 250 nanoseconds.

3. <u>Write Driver plus Data Encoder Turn-on from Write Gate</u>. The write driver plus data-encoder turn-on time (write splice width) is six Servo Clock periods maximum.

4. <u>Write Driver Turn-off from Write Gate</u>. To account for data encoding delays, Write Gate must be held on for at least one byte time after the last bit of the information to be recorded. (Refer to "Data Pad" in Figure 20.)

5. <u>Write-to-Read Recovery Time</u>. The time lapse before Read Gate can be enabled after disabling the Write Gate is 10 microseconds minimum.