# 3000 printed circuits

CONTROL DATA
EDUCATION INSTITUTES

CONTROL DATA
CORPORATION

# 3000 SERIES PRINTED CIRCUITS
# AND
# ELEMENTS OF LOGIC

FOR TRAINING PURPOSES ONLY

CONTROL DATA INSTITUTE
CONTROL DATA CORPORATION

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This manual was prepared for training purposes and does not contain all of the card types used in Control Data computers.

For a complete listing of printed circuits, refer to Printed Circuits Manual, Volumes I and II, publications number 60042900.

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## ELEMENTS OF CONTROL DATA LOGIC

The basic logic element in Control Data computers and peripheral devices is a transistor inverter circuit. A flip-flop (FF) is a combination of two inverters; a control delay is three inverters with clocked inputs. The major portion of a digital computer is built by interconnecting these circuits. Connections of inverters, flip-flops, and control delays form the various units of a digital computer, e.g., registers, counters, adders, complementers, and comparators. To facilitate the diagrammatic representation of these circuits the logic diagram technique is used. This technique emphasizes the functional aspect of a digital computer rather than the electronic aspect.

As a general rule, a digital computer has four main sections: Control, Arithmetic, Storage, and Input/Output. The Control and Arithmetic sections can be grouped under Logic section. Accordingly, the descriptions of the circuits in this manual are presented in four groups: Logic, Storage, Input/Output, and Special Purpose, (Chapters 2, 3, 4, and 5).

## PRINTED CIRCUIT CARDS

Control Data electronic circuits are mounted on printed circuit cards (frontispiece). Each card is equipped with a 15 pin male connector for plugging into the equipment chassis. The printed circuit card technique has the advantages of ease of design and maintenance, use of solid state components, greater reliability, and modular construction.

## INVERTER

The basic logic building block is an inverter circuit, represented by a rectangle as shown in figure 1-1. This circuit employs a $180^{o}$ electrical phase shift to produce an inversion; a "1" input results in a "0" output, and vice versa. In addition to use as an inverter, combinations of this basic logic element form bi-stable flip-flops and control delays.

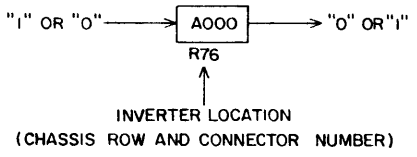



Figure 1-1. Conventional Inverter Symbol

## FLIP-FLOP (FF)

A FF is two inverter circuits interconnected as shown in figure 1-2. Each rectangle represents a single inverter. One of the inverters is the set side of the FF; the other, the clear side. The FF is placed in the "1" (set) state by a "1" signal on the set input. Conversely, it is placed in the "0" (cleared) state by a "1" signal on the clear input.

The storage capability of a FF means that the FF remains in the state in which it was placed by the last "1" input. Specifically, if a "1" signal is present at the set input, then the output of inverter K000 (figure 1-2) becomes "0". This output is applied as an input to K001 and its output then becomes "1". The output of K001 is fed back to K000. Thus, when the set input drops to "0", the feedback connection between K000 and K001 permits the storage of the state to which the "1" signal on the set input forced the FF. Should the clear input later receive a "1" signal the output of K001 becomes "0", and the feedback input to K000 is "0". Consequently, K000 furnishes a "1" output which is returned to K001 and replaces the "1" signal at the clear input.

When the FF is set, K001 has a "1" output and K000 has a "0" output. Conversely, when the FF is cleared, K001 has a "0" output, and K000 has a "1" output.

The conventional square or box symbol for a FF is used in figure 1-2 to show the relationship between it and the inverter configuration which forms the FF. The square which represents the FF encompasses the crossover of the outputs.

## CONTROL DELAY

The function of the control delay is to synchronize a sequence of logic operations within the computer with the two-phase master clock. Logical "1" inputs are received during one phase time, either odd or even, and "1" outputs are provided during the next phase time, either even or odd. The phase time of the output is opposite the phase time of the input.

### DEFINITION OF A CLOCK PHASE TIME

A clock phase time is the time during which an inverter driven by that phase has a "1" output. The input to the inverter is the raw clock signal received directly from the clock card. Thus during a clock phase time, the raw clock signal from that phase is a logical "0".

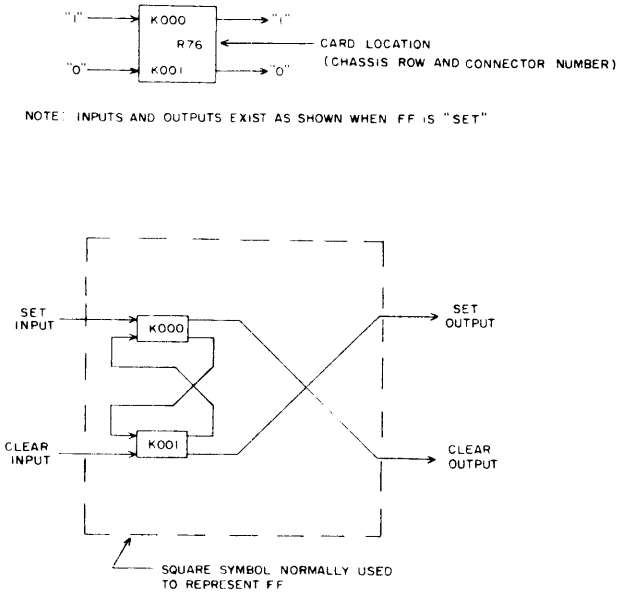



Figure 1-2. Conventional Flip-Flop Symbol

The response time of the inverter is approximately 1/4 to 1/2 a phase time. Thus the clock phase time always lags behind the raw clock signal, due to the delay of the inverter. However, this delay is not shown in the timing diagram of figure 1-4.

DESCRIPTION

The control delay consists of a FF having its feedback ANDed with a raw clock signal, and one or more inverters with two OR inputs each, which are driven by the A section of the FF and by a raw clock signal. The raw clock signal which enables the FF feedback is the phase opposite that which drives the inverter or inverters.

A diagram of a control delay symbol and the circuits encompassed by it is shown in figure 1-3. Figure 1-4 shows the timing of its operation.

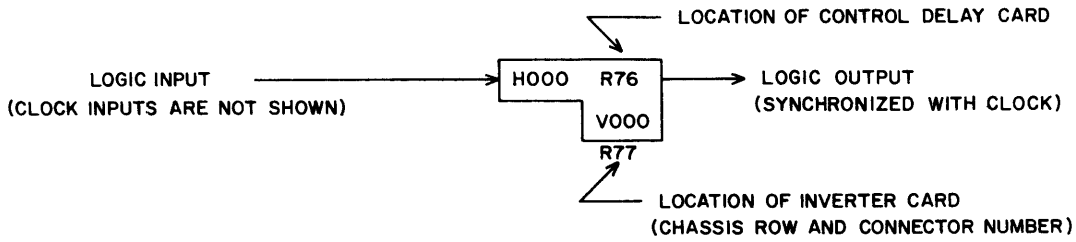
The clock inputs to a control delay are ordinarily not shown on a drawing. It is understood that the output occurs during the odd or even phase time, while the corresponding raw clock signal is a "0", depending upon whether the third superscript digit is odd or even. For example, control delay H100/V100 would have its output during an even clock phase time, while H101/V101 would have its output during an odd clock phase time.

The logic input to a control delay is gated by the external circuitry. Normally, the input drops to "0" shortly after the output appears, and is not repeated. If the input does not drop, then the output of the control delay is a series of pulses from the inverter, since it is driven by the raw clock signal.

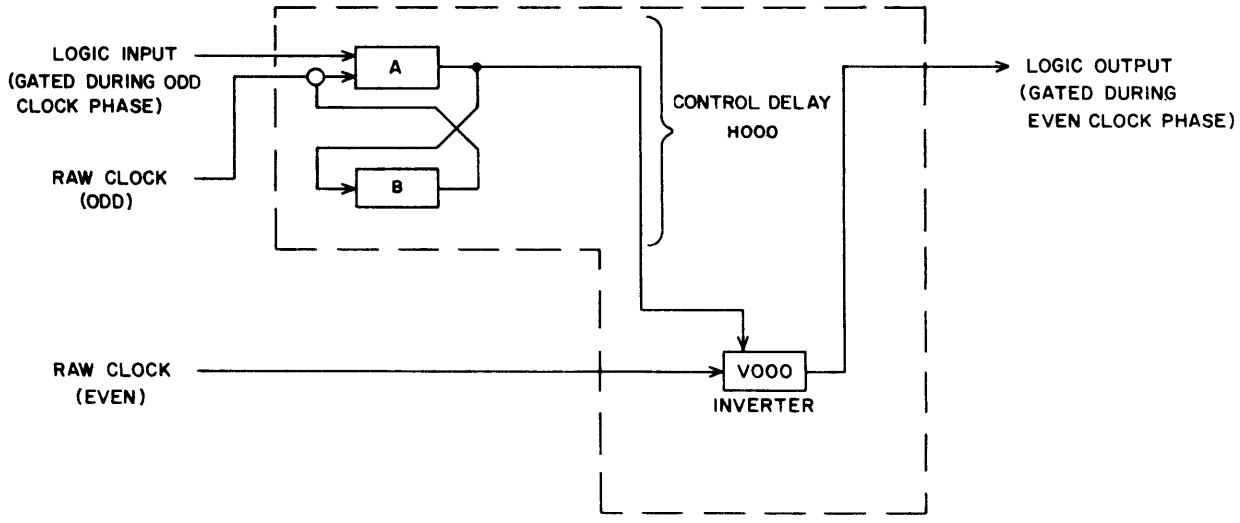
CIRCUIT OPERATION

Figure 1-3 shows that the gated logic input goes directly into the A section of H000. This forces the output of A to "0", resulting in a "1" output from B. The input to A is gated during the odd clock phase time; thus during this time, the odd raw clock signal is "0". When the odd raw clock signal becomes "1", the logic input to A drops, but the feedback path from B to A is enabled so that A continues to have a "0" output until the next odd clock phase time.

Inverter V000 is gated both by the output of A and by the even raw clock signal. With a "0" input from A, inverter V000 provides a "1" output during the even clock phase time, since the even raw clock signal is a "0". The "1" output from V000 continues until the next odd clock phase time disables the FF feedback, and the control delay returns to initial conditions.




NOTE:
INVERTER MAY BE REPRESENTED BY EITHER V---, N---, OR Y---.




NOTE:
LOGIC INPUT IS GATED INTO CONTROL DELAY WHILE ODD CLOCK PHASE IS "1".
THE INPUT DROPS WHEN ODD PHASE BECOMES "0" AND IS NOT REPEATED.

Figure 1-3. Conventional Control Delay Symbol

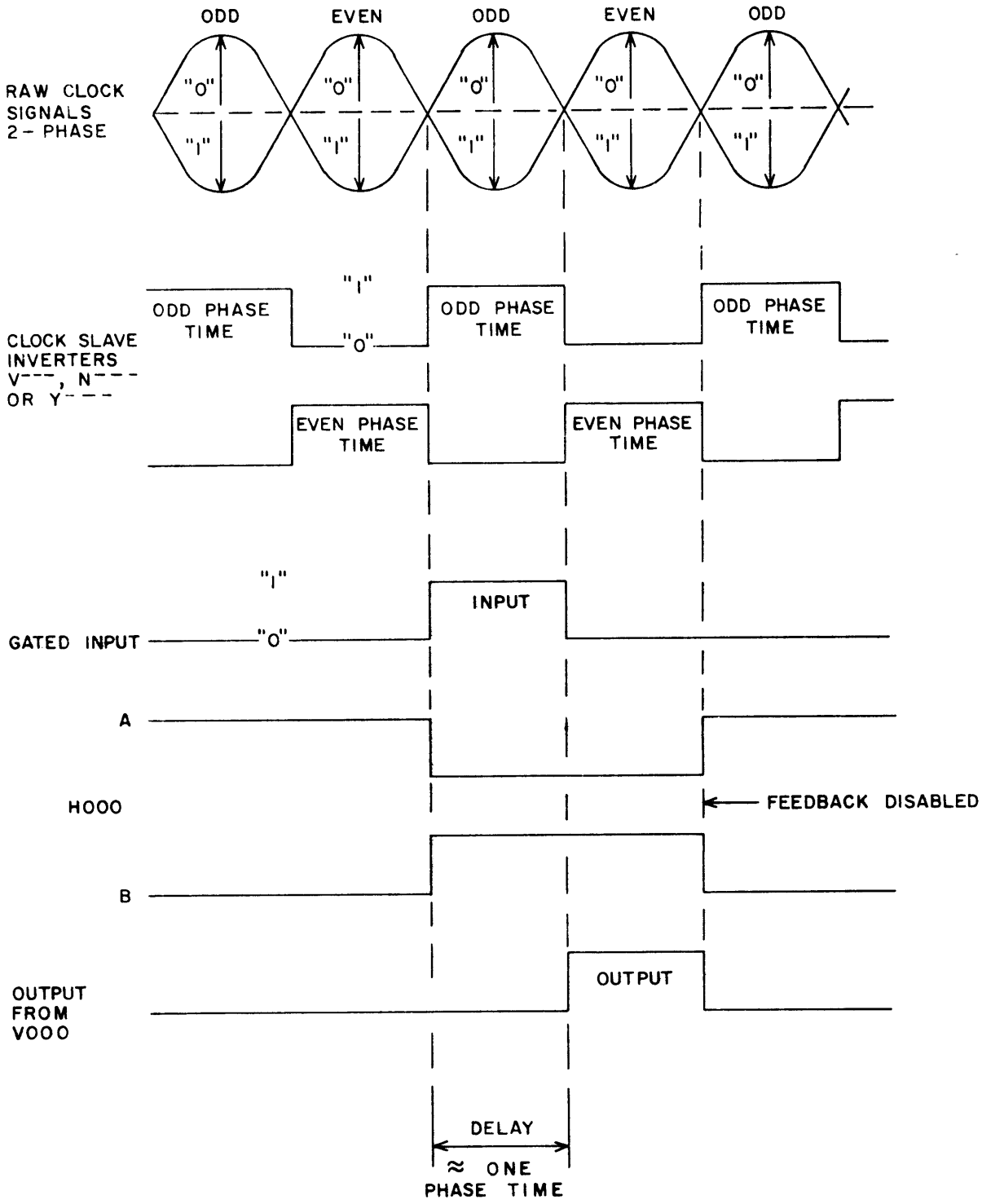



Figure 1-4. Control Delay Timing Diagram

LOGICAL EQUATIONS OF A CONTROL DELAY

A control delay may be represented by a minimum of two logical equations: one equation for the H--- term, and one equation for each V---, N---, or Y--- term. The symbol on the left of the equal sign is the subject term, and the expression on the right describes the configuration of its inputs.

All raw clock and gated logic inputs to a control delay are represented in its equations. The H--- term requires a logic input gated during a clock phase, and a raw clock signal which gates the FF feedback. The V--- term requires a raw clock signal to gate its output, and a logic input from the H--- term. These conditions are covered by the following basic rules:

1. Every input term of an H--- equation must contain one, and only one, clocked symbol such as V---, N---, or Y---.
2. The last term of an H--- equation must be a C--- (raw clock).
3. At least one input term of a V---, N---, or Y--- equation must contain an H--- symbol.
4. The last term of a V---, N---, or Y--- equation must be a C--- (raw clock) symbol.

A set of equations for control delay which would have an output during an even phase time could be written as follows:

H000 = Z024 W005 N001 + C001

V000 = H000 + C000

The symbols in the above equations refer to the following:

| | |
|---|---|
| H000 | A circuit on a control delay card which receives its input during an odd phase time, since the third superscript digit is even. |
| Z024 | A logic input. |
| W005 | A logic input. |
| N001 | A clock slave inverter which provides a "1" input enabling the 3-way AND during an odd clock phase time. |
| C001 | A raw clock signal which is a "0" during odd clock phase times; it is received at the control delay card and gates the FF feedback. |
| V000 | The inverter portion of the control delay which provides a "1" output during an even clock phase time only. |
| C000 | A raw clock signal which is "0" during even clock phase times and drives the control delay inverter. |

## LOGICAL "AND"

A three-input AND circuit is shown in figure 1-5. The small circle and connections used to represent this circuit on a logic diagram are also shown.

The AND gate requires that all inputs must be a "1" simultaneously. If any one of the AND inputs is a "0", then a "1" on another input is not sensed.

Thus, if the transistors A, B, and C are not conducting, their output diodes are biased in the reverse direction, and the resulting output signals are at the logical "1" level. This condition allows the -20v through the AND resistor to place a negative voltage on the base of transistor D, so that it conducts.

However, if any one of transistors A, B, or C is conducting, its collector goes to approximately ground potential. Its output diode is biased in the forward direction from the -20v through the AND resistor. This prevents the -20v source from applying drive current to transistor D, and transistor D is held in the non-conducting state.

## LOGICAL "OR"

A three-input OR circuit is shown in figure 1-6 (the conventional logic diagram representation is also shown). An OR gate allows a "1" signal on any input to be sensed, although a "0" signal may simultaneously appear on another input.

Figure 1-6 shows three single-input ANDs connected to produce three logical OR inputs to transistor D. The input lines are separated by diodes, so that a "1" signal is not nullified by a "0" signal on another input line. Thus, if any one of transistors A, B, or C is not conducting so that it has a "1" output, the -20v through the respective AND resistor applies a negative voltage to the base of transistor D, causing it to conduct.

## BASIC THREE-STAGE COUNTER

A counter is essentially a double rank register which increases or decreases the quantity stored, an increment at a time. The three-stage counter circuit shown in figure 1-7 is additive from binary 000 through 111.

A count is stored in two steps:

1. A "1" input on the Advance line sets a FF in rank 1. This occurs in consecutive order and when all three are set, the next

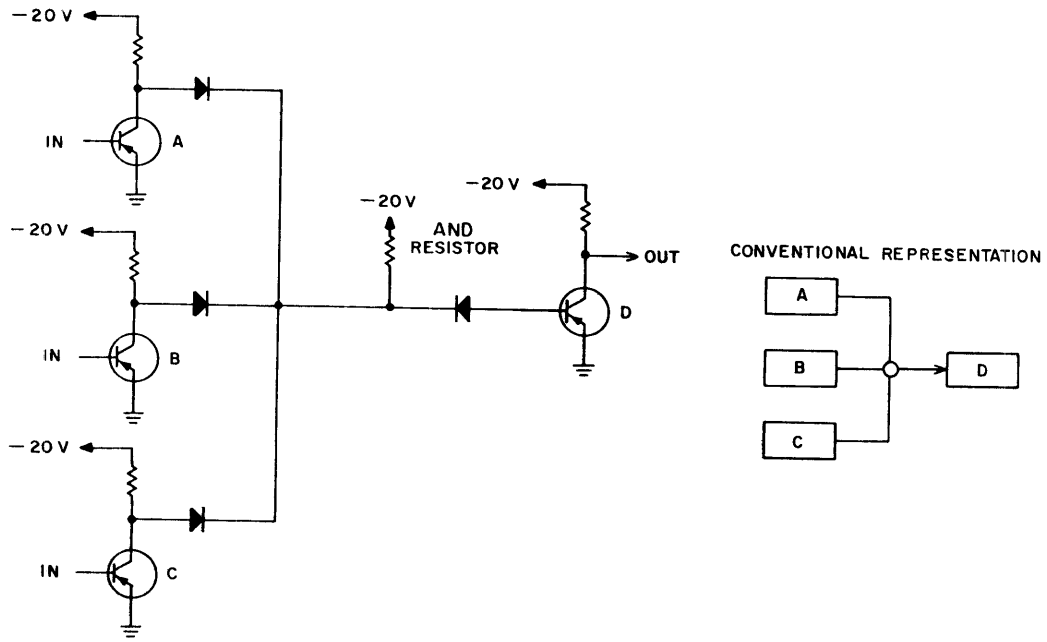



Figure 1-5. Logical AND

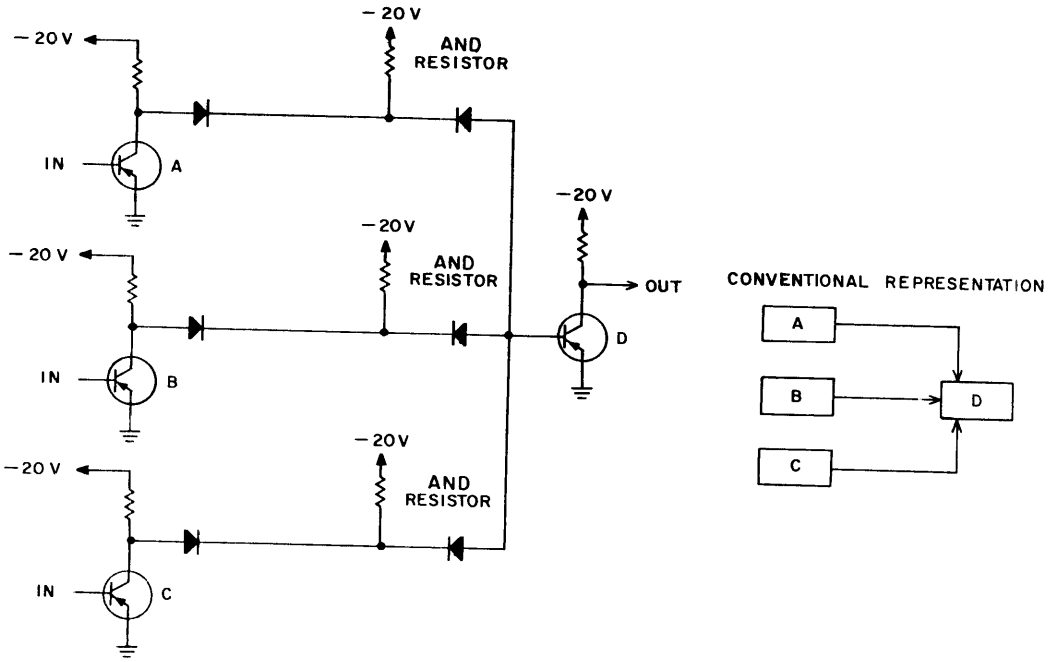



Figure 1-6. Logical OR

input clears them.

2. A "1" input on the Transfer line causes the FFs in rank two to assume the identical states as their corresponding FFs in rank 1.

To analyze the operation of the counter, assume that both ranks are initially cleared, so the count stored is zero. The first Advance command finds the AND gate to K000 enabled and therefore enters the count 001 (octal 1) into rank 1. This partially enables the AND gate to K002 so that the Transfer command enters the count 001 into rank two. The next Advance command finds the AND gate to K001 and K010 enabled and thus enters the count 010 (octal 2) into rank 1. The operation continues in this manner as shown in table 1-1 until the count reaches 111 (octal 7), which is the highest possible count in a three-stage counter. This is followed by a command sequence which returns both ranks to the count 000.

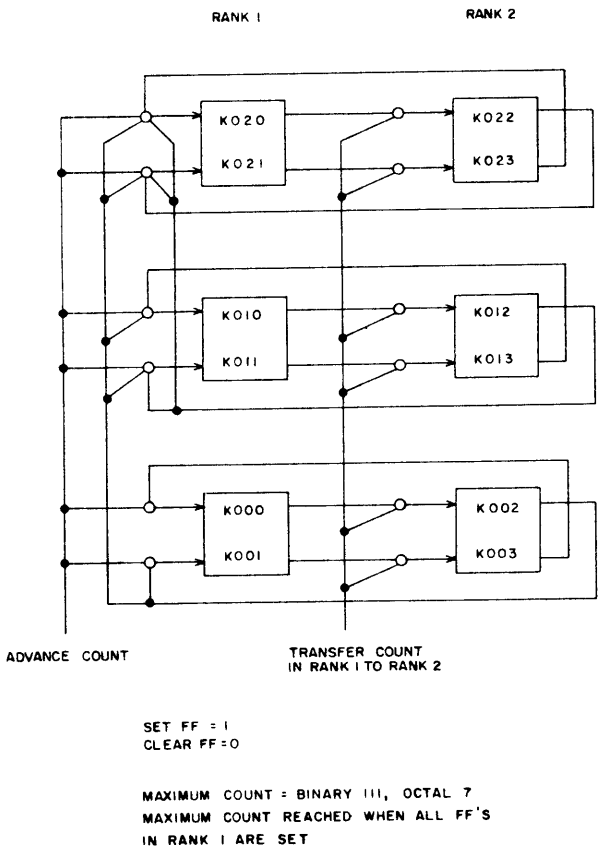



Figure 1-7. Basic Three-Stage Counter

TABLE 1-1. COUNTING SEQUENCE FOR THREE-STAGE COUNTER

| Command | Quantity Stored (Octal) | Rank 1 | | | Rank 2 | | |
|---|---|---|---|---|---|---|---|
| | | K02- | K01- | K00- | K02- | K01- | K00- |
| Initial conditions | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Advance | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| Transfer | | 0 | 0 | 1 | 0 | 0 | 1 |
| Advance | 2 | 0 | 1 | 0 | 0 | 0 | 1 |
| Transfer | | 0 | 1 | 0 | 0 | 1 | 0 |
| Advance | 3 | 0 | 1 | 1 | 0 | 1 | 0 |
| Transfer | | 0 | 1 | 1 | 0 | 1 | 1 |
| Advance | 4 | 1 | 0 | 0 | 0 | 1 | 1 |
| Transfer | | 1 | 0 | 0 | 1 | 0 | 0 |
| Advance | 5 | 1 | 0 | 1 | 1 | 0 | 0 |
| Transfer | | 1 | 0 | 1 | 1 | 0 | 1 |
| Advance | 6 | 1 | 1 | 0 | 1 | 0 | 1 |
| Transfer | | 1 | 1 | 0 | 1 | 1 | 0 |
| Advance | 7 | 1 | 1 | 1 | 1 | 1 | 0 |
| Transfer | | 1 | 1 | 1 | 1 | 1 | 1 |
| Advance | 0(or8) | 0 | 0 | 0 | 1 | 1 | 1 |
| Transfer | | 0 | 0 | 0 | 0 | 0 | 0 |

## CAPACITIVE DELAY

Capacitive delay circuits are constructed by placing a capacitor from the signal line to ground. The delay time is the time required to charge the capacitor when a "1" signal appears on the line. A "0" signal is delayed approximately one tenth as long as a "1". The method of connecting a delay between two logic cards, and the symbols used to represent this connection on a logic diagram are shown in figure 1-8.

Figure 1-8 shows that when the transistor on card A is conducting, its collector is almost at ground potential. Hence, the voltage across the delay capacitor is quite low and it contains very little charge. However, when the output of card A switches to "1" and its transistor stops conducting, the circuitry attempts to bias the input line at the "1" level. Initially this voltage is absorbed by the uncharged delay capacitor, which gradually obtains a charge as shown in figure 1-9.

Two factors govern the delay time: the size of the capacitor and the rate at which it receives charging current. Generally, the larger the capacitor, the longer the delay time. The delay time may be adjusted by varying the resistance in series with the capacitor. Increasing the resistance decreases current flow to the capacitor, increasing the delay time.

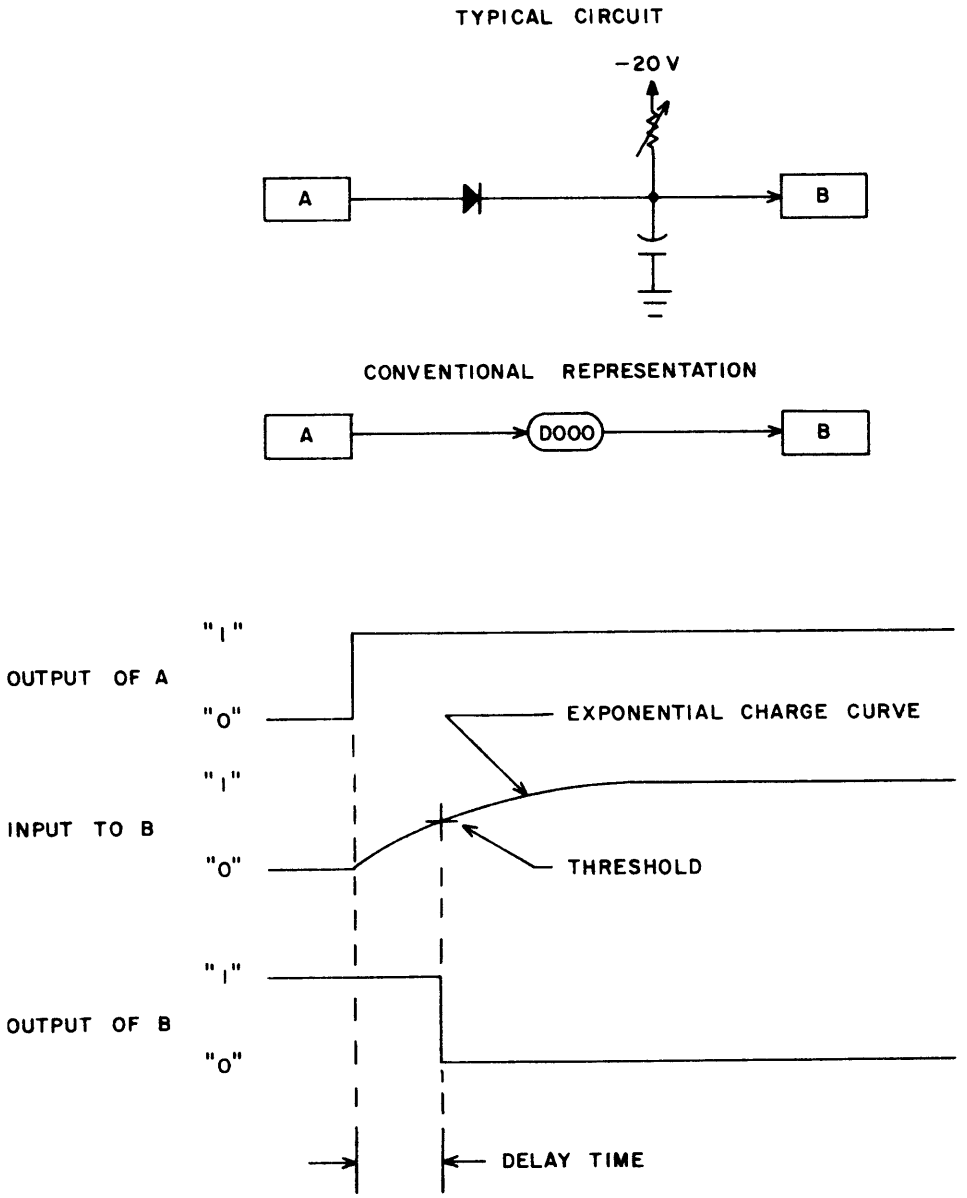
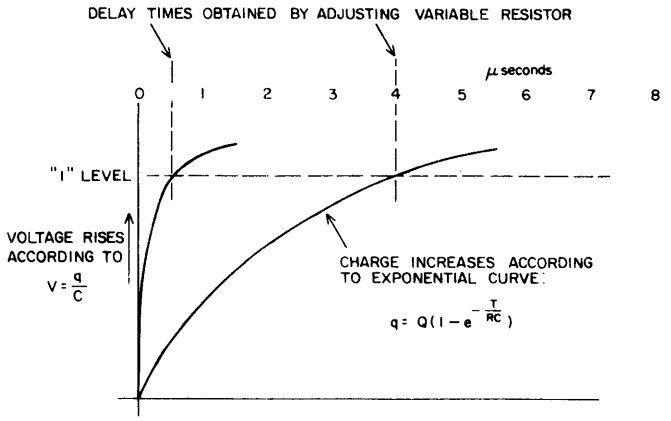



Figure 1-8. Capacitive Delay




NOTE:

| SYMBOL | REFERS TO: | UNITS |
|---|---|---|
| T | TIME | SECONDS |
| q | PARTIAL CAPACITOR CHARGE | COULOMBS |
| Q | FINAL CAPACITOR CHARGE | COULOMBS |
| R | SERIES RESISTANCE | OHMS |
| C | CAPACITANCE | FARADS |
| V | APPLIED POTENTIAL | VOLTS |
| e | NATURAL LOGARITHM BASE | PURE NUMBER 2.718, APPROX. |

Figure 1-9. Capacitor Charge Curve

## PULSE FORMING NETWORKS

Many circuits contain pulse forming networks, consisting of two inverters and a capacitive delay, for the purpose of reshaping a steady "1" signal into a short "1" pulse. There are two types: those which produce a pulse upon receipt of a "1" signal and those which produce a pulse when the "1" signal ends. These types are known respectively as "leading edge" and "trailing edge" networks, and are presented in figure 1-10.

When a "1" input is received by a leading edge network, an immediate double inversion occurs, producing a "1" output. However, as soon as the capacitor is sufficiently charged, a "1" is sent directly into A001, and the output of inverter A001 switches to "0".

In the case of a trailing edge network, the steady input signal is fed directly into both inverters. Thus, when this signal goes to "0", the output of both inverters switches to "1". However, the "1" output of A000 does not reach A001 until the capacitor has charged sufficiently; at that time the output of A001 switches to "0".

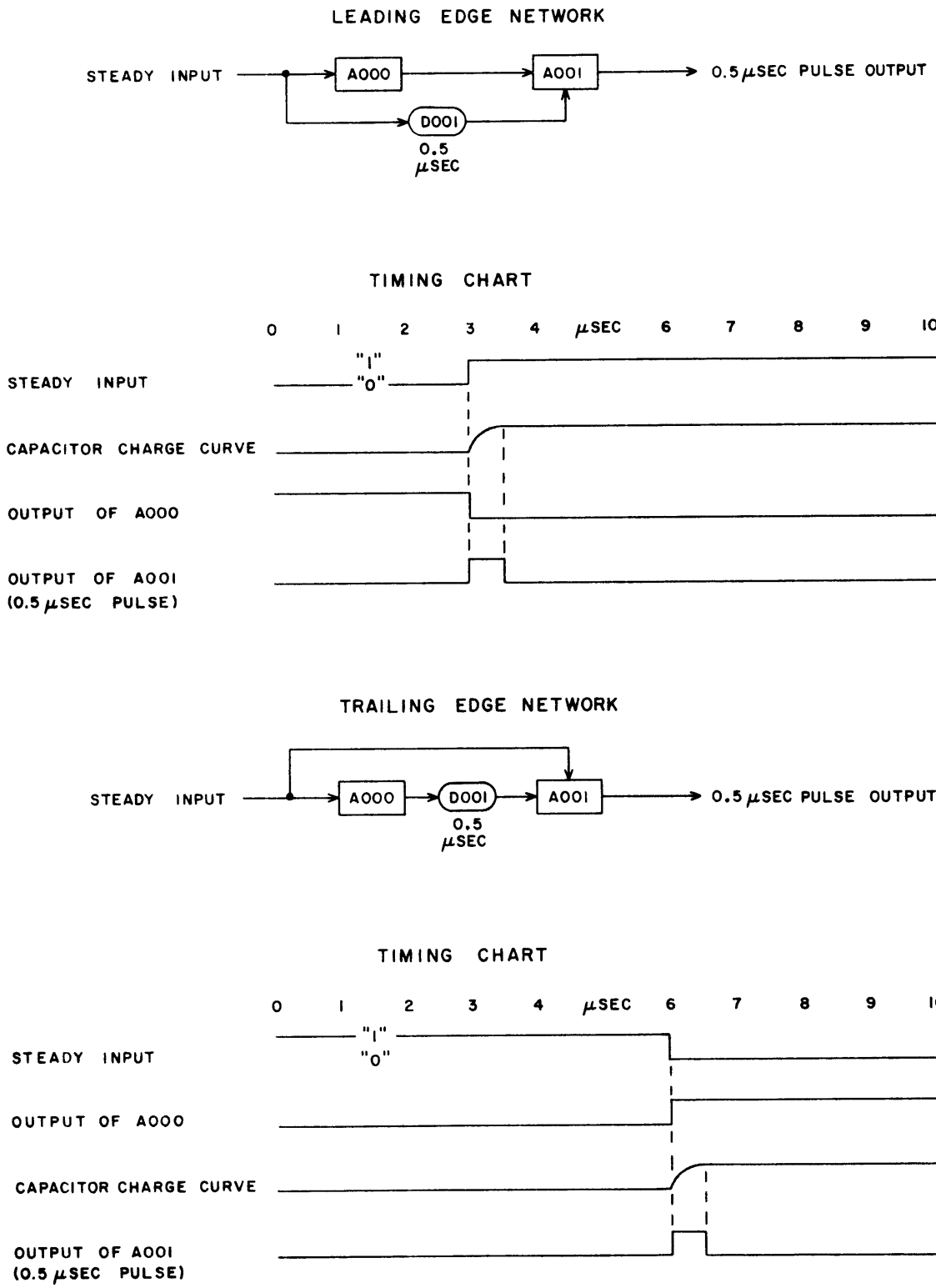



Figure 1-10. Pulse Forming Networks

## TIMING CHAIN PULSE GENERATOR

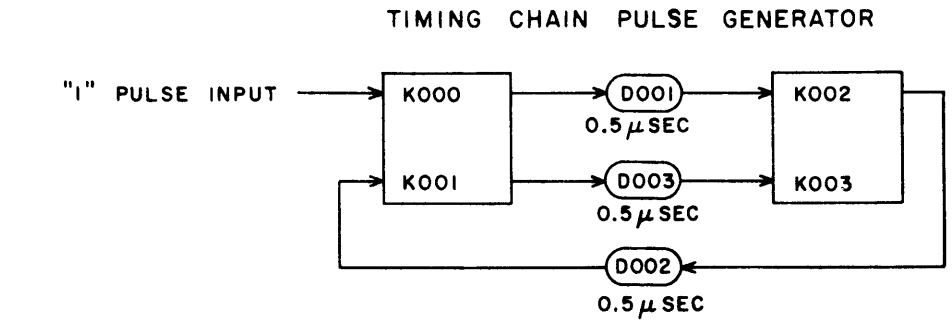
A convenient method of obtaining a series of sequential pulses using flip-flops and delays is shown in figure 1-11.

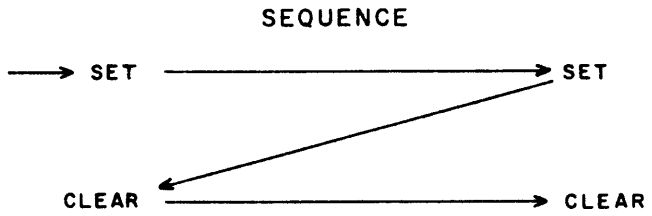
The two FFs exhibit four distinct sets of conditions at successive time intervals. Initially both are in the clear state. A "1" pulse input to K000 sets K000/001, so that K001 has a "1" output. After a brief delay, this signal sets K002/003. K003 then sends a "1" through a delay to K001, so that K000/001 is cleared. This causes K000 to send a "1" through the third delay to K003, so that K002/003 is also cleared and initial conditions prevail.

These four conditions and the times at which they occur are as follows:

| | K000/K001 | K002/K003 |
|---|---|---|
| Time 0 | Clear | Clear |
| Time 1 | Set | Clear |
| Time 2 | Set | Set |
| Time 3 | Clear | Set |
| Time 0 (or 4) | Clear | Clear |

The lengths of these time intervals are dependent upon the value of the capacitive delays. In the example shown, all of the times are 0.5 us. However, these may be varied in any manner desired.



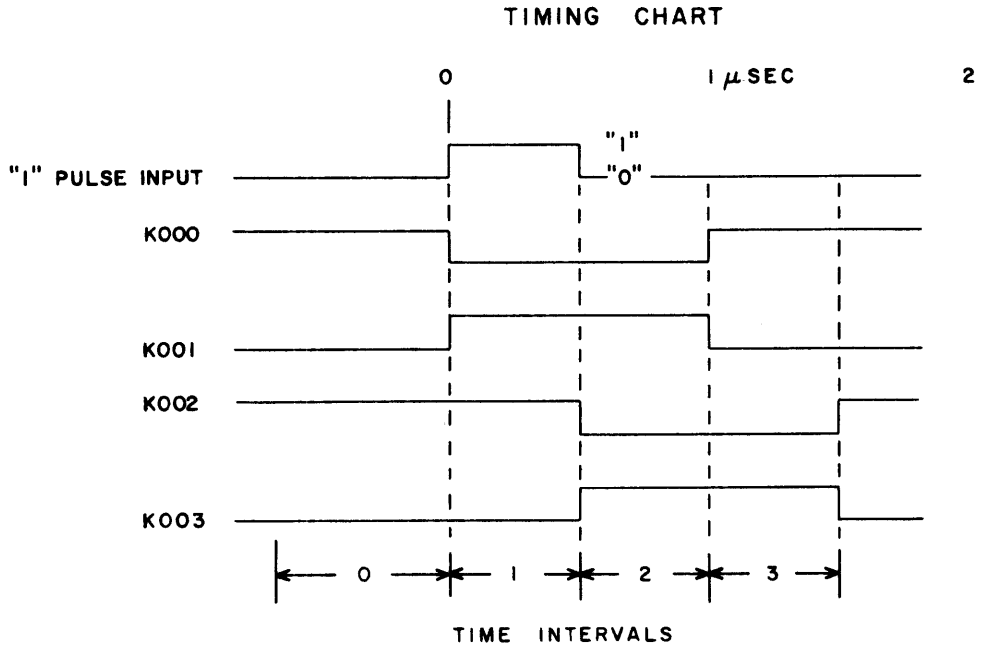




Figure 1-11. Timing Chain

## INVERTER CIRCUIT
## 1604 TYPE

The two signal levels in 1604 type logic are: -3.0v, logical "1", and -0.5v, logical "0". The single inverter inverts these signal levels: a -3.0v input becomes a -0.5v output, and vice versa.

In the standard inverter circuit shown, transistor Q01 is connected as an emitter-follower; Q02, as an amplifier. The collector circuits of the transistors have two feedback loops which prevent the transistors from being driven to cutoff or saturation. As a result, switching from one state to the other is accomplished in from 50 to 100 nanoseconds.

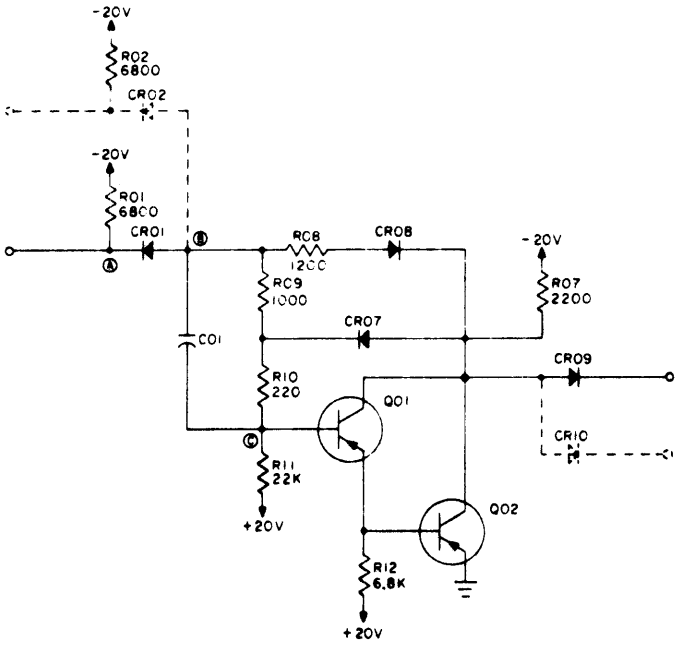
An input signal is applied via isolation diodes CR01 or CR02 to a voltage divider network composed of resistors R07, R08, R09, R10 and R11. An input signal of -0.5v (point A) results in -1.5v at point B and 0.8v at the base of Q01 (point C). CR01 is biased 1v in the backward direction to provide for noise suppression at the input of the inverter. Capacitor C01, between CR01 and the base of Q01, provides rapid coupling of input signal changes to Q01, improving the switching time of the circuit.

Transistors Q01 and Q02 each provide beta* current gains of approximately 100; loop gain of the two transistors is in the order of $10^4$. The collector current of Q01 and Q02 develops the output voltage across resistor R07. Output diode CR09 isolates the output line from the other output line connected to CR10.

Diodes CR07 and CR08 form the feedback loops which prevent transistors Q01 and Q02 from being driven to cutoff or saturation. The positive-going limit allows a maximum transistor conduction that is less than saturation; the negative-going limit fixes a minimum conduction for the transistors. When the transistors approach cutoff, their collectors approach -3.0v. The collector potential is coupled back to the base of Q01 through CR08, R09 and R10. As a consequence the base of Q01 always is held at a sufficiently negative voltage to permit some minimum conduction of Q01 and thus Q02.

*The beta current gain is the ratio of collector current to base current.

When the transistors approach saturation, the collectors approach 0v. The collector potential is coupled back to the base of Q01 through CR07 and R10. The base of Q01 is thus prevented from becoming so negative that saturation occurs.




Schematic Diagram of 1604 Type Inverter Circuit

GROUND RULES

The following ground rules for usage of the basic 1604 inverter circuit are intended as guidelines in obtaining optimum performance. They are not intended to be excessively restrictive, because it is often found that a circuit will operate satisfactorily in a configuration which may deviate considerably from one or more of the ground rules. Decisions as to when a ground rule may be violated must be based upon various electronic and timing considerations, and are the responsibility of the designer.

1) A maximum of eight outputs may be taken from a single inverter.

2) An inverter will drive a maximum of six simultaneously gated AND loads.

3) The total number of inputs and outputs of a single inverter must not exceed 12.

4) The number of OR inputs to an inverter is limited to a maximum of six.

5) For high speed operation, the number of AND connections which can be made to a single OR input should be limited to four. If timing is not critical, the maximum number of AND connections can be increased to six.

6) All unused input pins must be grounded.

7) The minimum switching time for a mesa transistor inverter driving one load is approximately 30 nanoseconds. This will increase to about 75 nanoseconds as additional loads are added.

8) The minimum switching time for a drift transistor inverter driving one load is approximately 50 nanoseconds. This will increase to about 100 nanoseconds as additional loads are added.

9) An inverter will drive a load having 0.015 uf of capacitance. This may be increased at the discretion of the designer; however, long capacitive delays (greater than 10 usec) should be constructed using card type 97.

10) A capacitive delay should not be driven directly by a flip-flop, especially a flip-flop using mesa transistors, unless the discharge time of the capacitance is appreciably shorter than the duration of the input to the flip-flop.

## 3600 INVERTER CIRCUIT

NOTE

Type CA cards having OR inputs have been discontinued and should not be used for new design.

### AVAILABLE CARD TYPES

Three series of printed circuit cards have been produced during development of the 3600 family of computing systems. The initial prototype series was designated Type C. Later, after the design had been approved, the physical size of the phenolic board was increased slightly and the cards went into production as the Type CA series. Except for the addition of more test points, there was no change in the circuit.

As shown in figure 1, logical OR inputs on Type CA inverters consist of only the OR diode without any connection to -20 volts. This was intended to eliminate the requirement for grounding unused OR inputs, since an open OR input will not drive the circuit output to "0". In actual practice, however, it was found that the distributed capacitance of large numbers of open OR inputs could result in a delay in switching time. In addition, since OR inputs did not provide the clamping action of AND inputs, the circuits tended to respond excessively to transients on the signal line. These conditions brought about the development of two new series of cards, called Type HA and Type K. Both of these have the same basic inverter circuit as the Type CA inverter, but the inputs are modified. The logical AND and OR input configuration of a Type K card is identical to the corresponding Type CA number, but all OR's have been converted to single-way AND's including the feedback of flip-flops. Cards in the Type HA series are built with a limited number of inputs, e.g., an HA 07 card contains two inverters with each having only one single-way AND input. Type CA cards have since been discontinued and should not be used in new design.

## BASIC INVERTER CIRCUIT

The basic inverter circuit consists of two transistor stages, as shown in figures 1 and 2. Transistor Q01 is a grounded emitter stage which supplies AND current to the load, and transistor Q02 is an emitter follower stage which supplies OR current to the load.

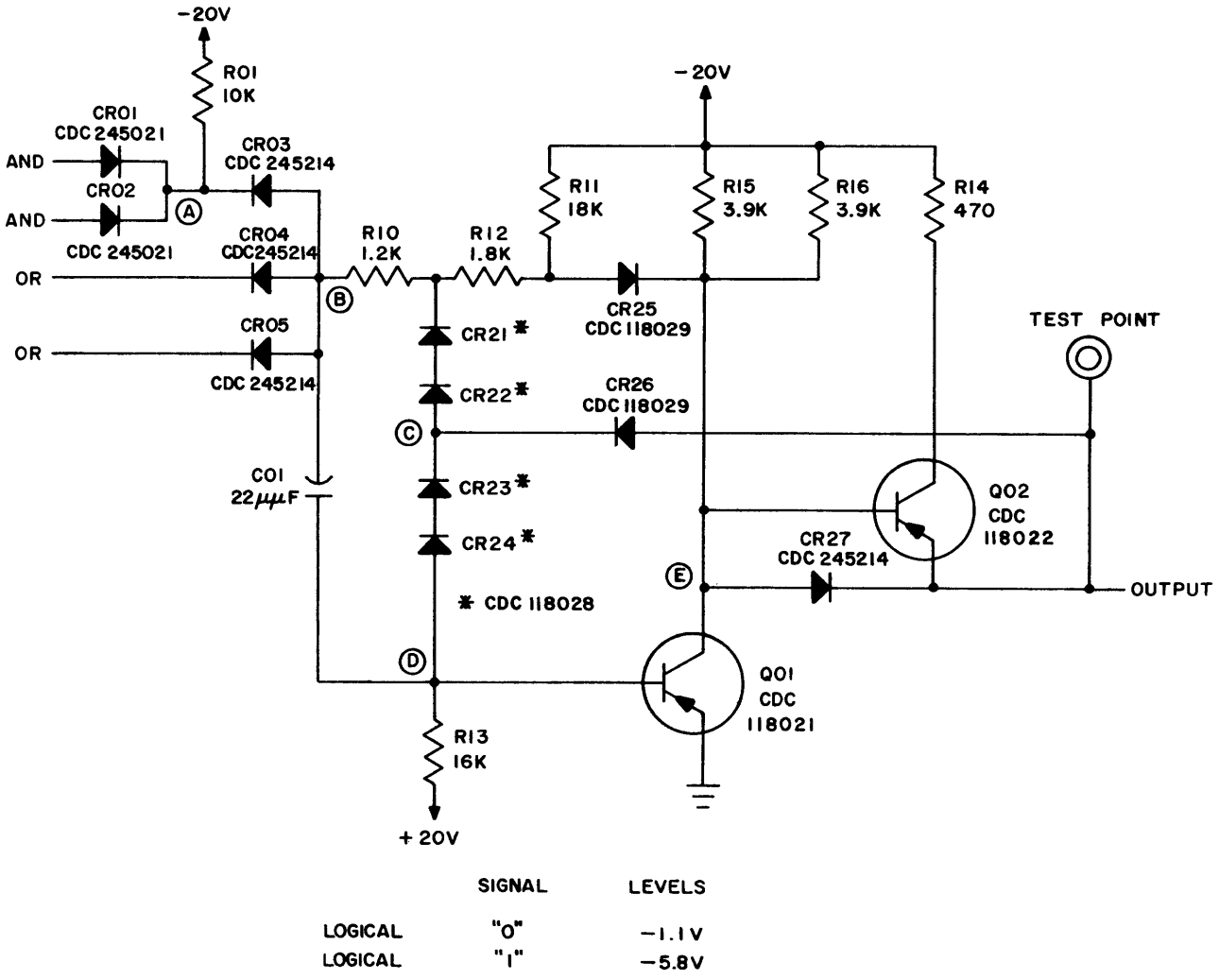



Figure 1. Schematic Diagram Type CA Inverter Circuit
(Not to be used for new design)

The input to the circuit consists of two levels of diode logic. The maximum number of inputs is limited by the number of available input pins on a circuit card; however, the maximum number of individual inputs to any single AND cannot exceed 6.

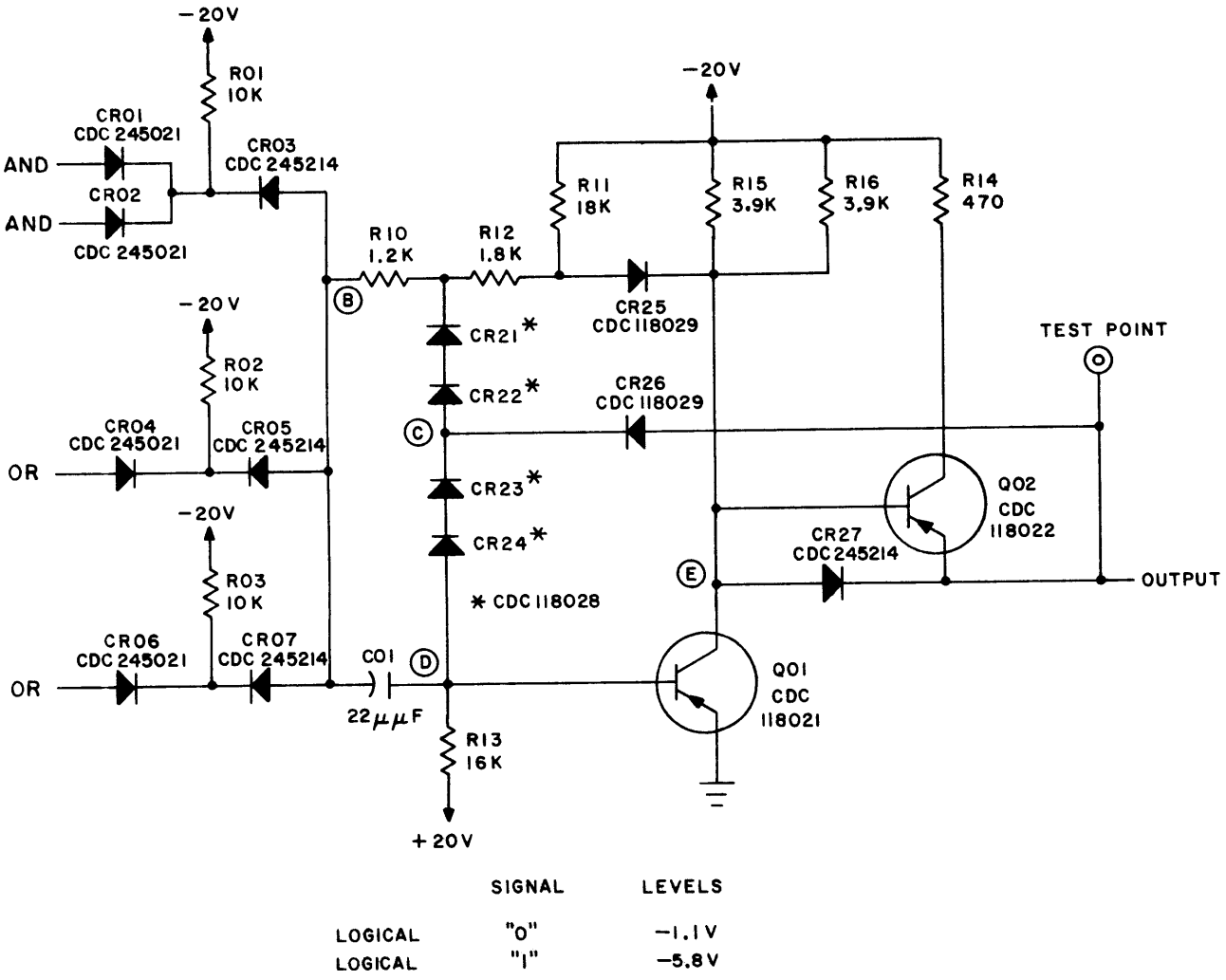



Figure 2. Schematic Diagram of Type K and Type HA Inverter Circuit

The input logic diodes are medium speed germanium devices. Initially, Hughes HD2969 diodes were used, and a set of graphs is included in this report which show the comparative recovery time of these diodes.

The response of an AND input is a function of the time constant of the AND resistor R01, shunt circuit capacitance at point (A) and the recovery speed of the input diodes. Because additional AND diode inputs increase the shunt capacitance, it is necessary to decrease the size of the AND resistor a proportionate amount as the number of inputs to the AND increases beyond 3.

The transition speed of the AND circuit varies inversely with the recovery speed of the AND diodes. Slow diodes allow additional recovery current to be drawn. This, in effect, allows a larger turn-on current in the first transistor stage.

The input resistor and diode network of transistor Q01 establishes the clamping levels for the output signal. This network also provides feedback to the base of Q01 which stabilizes the two quiescent values of the output voltage.

The input network establishes an input threshold level of approximately -3 volts. Thus, the input signal must be more negative than -3 volts before transistor Q01 turn-on current is allowed to flow. Silicon forward drop diodes CR21 through CR24 are used in the input network to obtain a constant d-c level for signal threshold. These diodes also have a low dynamic impedance which causes little attenuation of the input signal current.

The 22 uuf speed-up capacitor C01 on the input of the first stage bypasses the 1.2 k resistor R10 and the diode network during the initial rise or fall of the input signal. This provides additional drive to the base of Q01 during the input signal transition, thereby speeding the switching of this stage.

Feedback is accomplished through two high speed silicon diodes, CR25 and CR26, which have very low stored charge characteristics. If these diodes were capable of storing excessive charge, there would be additional delay in switching. By using diodes with very low storage, the initial switching speed is greatly improved.

When the grounded emitter stage Q01 is turned on, collector current flows out of the circuit through the series diode CR27. In this state, Q01 can supply current to 8 AND loads. Transistor Q01 is clamped out of saturation by the silicon feedback diode CR26, and the output voltage settles at a nominal value of -1.1 volt. The voltage drop across diode CR27 insures a back bias being applied to the base-emitter junction of Q02, thereby keeping this stage turned off.

When Q01 turns off, the collector voltage starts to rise toward -20 volts. Since the voltage across the load cannot change as quickly as the collector voltage of Q01, the series output diode CR27 is back biased and the output emitter follower stage Q02 is turned on.

The turn-on current is applied to the base of Q02 at the rate at which Q01 turns off. The turn-on current is the current that is drawn through the first stage collector resistors R15 and R16. This current is available to turn on the output stage only as fast as it is turned off in the first stage.

Transistor Q02 in the on state proceeds to drive the output voltage negative. At about -5.8 volts, the output is fed back to the input of the first stage by diode CR25 to start the clamping action. Since this process has delay associated with it, the output signal overshoots the -5.8 volt mark and may carry as far as -8 volts. The circuit then settles the voltage back to the -5.8 volt level. In this state, transistor Q02 provides a low impedance path to the -20 volt supply.

## GROUND RULES

(Effective November 21, 1963)

The following ground rules for usage of the basic 3600 inverter circuit are the result of tests performed by the Special Projects Department, Government Systems Division of Control Data Corporation. Inquiries concerning these ground rules should be addressed to the above department.

The ground rules are intended as guidelines in obtaining optimum circuit performance. They should not be considered as being excessively restrictive, because it is often found that a circuit will operate satisfactorily in a less than optimum configuration which may deviate considerably from one or more of the ground rules. Decisions as to when a ground rule may be violated must be based upon various electronic considerations, and are the responsibility of the designer.

Definition: Minimum Usage Inverter

The minimum usage inverter referred to in the following rules is defined to be an inverter driving one load and having one input. The inverter which drives the minimum usage inverter must drive no other loads. All wire lengths are kept as short as possible, voltages are adjusted to proper levels, and temperatures are allowed to stabilize.

LOADING

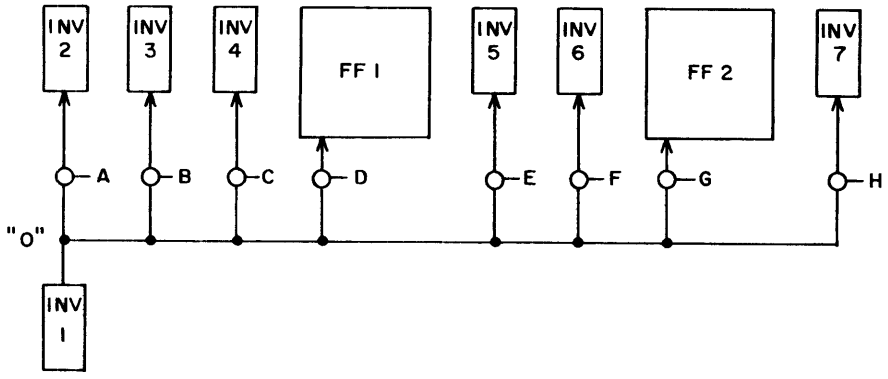
Any single input to a recipient inverter, regardless of whether it is a part of a 1, 2, 3, 4, 5, or 6 input AND or an OR input, is considered to be one load.

1) An inverter may simultaneously drive eight AND loads, eight OR loads, or any combination up to eight loads total.

2) A flip-flop or a control delay may drive only seven loads, because it is required to provide its own feedback which constitutes one load.

Exception to Rule

Inverter 1 is normally capable of maintaining a logical "0" on eight input AND gates. However, there is one exception when all the points, A through H, are driven to a "1" simultaneously. The current demand on inverter 1 is of such magnitude that the "0" condition is lost momentarily, allowing runt pulses to occasionally set a flip-flop or be amplified through an inverter. This condition can be avoided by limiting the inverter to a total of six loads as opposed to the usual eight loads.



UNUSED INPUTS

3) In case an entire AND input group is unused, at least one of the inputs must be grounded.

4) All unused OR inputs must be grounded, if using type C or CA cards.

5) All unused single-way AND inputs must be grounded.

NOISE SUPPRESSION

6) When a noise condition cannot be alleviated by the following suggestions or if an interconnecting lead is over 80 inches in length use logic level clamp card CA02.

   a) Maintain wire runs as short as possible.

   b) When possible, drive heavily loaded inverters from a lightly loaded source.

   c) When possible, use cards with 1, 2, 3, or 4 input AND gates as opposed to 5 and 6 input AND gates.

   d) Avoid using OR inputs unless the OR is a single-way AND.

7) All drive lines from H--- terms to N---, V---, and Y--- terms must be clamped, regardless of length, and must enter the recipient N---, V---, and Y--- terms through AND inputs.

8) N---, V---, and Y--- terms having a clock signal on an AND input must use one of the special card types numbered K72, CA73, K74, K92, K93, and HA06.

The clock input must be on the following pins:

| Card Type | Inverter A | Inverter B |
|---|---|---|
| CA72 | 5 or 6 | 13 or 14 |
| K72 | 2, 5, or 6 | 10, 13, or 14 |
| CA73 | 2 or 3 | 10 or 11 |
| CA74 | 5 or 6 | 13 or 14 |
| K74 | 5 or 6 | 13 or 14 |
| K92 | 2 | |
| K93 | 2 or 3 | |
| HA06 | 5 or 6 | 13 or 14 |

Exception to Rule

a) A clock input must come in on an AND; if the listed pins do not lend themselves to conditions, another AND input can be used.

b) The restriction of using only the above card types may be violated in applications where the logic circuits are heavily loaded.

PROPAGATION DELAYS AND TIMING ALLOWANCES

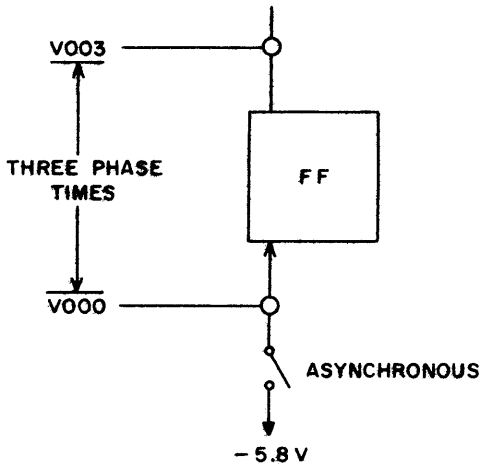
| | | |
|---|---|---|
| 9) | Allow $17 \times 10^{-9}$ seconds | To switch from "0" to "1" any minimum usage inverter using any type input. |
| 10) | Allow $11 \times 10^{-9}$ seconds | To switch from "1" to "0" any minimum usage inverter using a 1, 2, 3, or 4-way AND input. |
| 11) | Allow $8 \times 10^{-9}$ seconds | To switch from "1" to "0" minimum usage inverters where equal numbers of AND and OR inputs are involved in a string of inverters. |
| 12) | Allow $6 \times 10^{-9}$ seconds | To switch from "1" to "0" any minimum usage inverters using a 5 or 6-way AND input. |
| 13) | Allow $5 \times 10^{-9}$ seconds | To switch from "1" to "0" any minimum usage inverters using OR inputs. |
| 14) | Allow $2 \times 10^{-9}$ seconds per foot | For propagation time from point to point through all lengths of wire. |
| 15) | Add $1 \times 10^{-9}$ seconds | To each inverter switching time for each additional load beyond one. |
| 16) | Add $2 \times 10^{-9}$ seconds | To each inverter switching time for each foot of wire attached to the output. |

17) The transition times from -1.1v "0" to -5.8v "1" and from -5.8v "1" to -1.1v "0" range from $20 \times 10^{-9}$ to $50 \times 10^{-9}$ seconds and $15 \times 10^{-9}$ to $35 \times 10^{-9}$ seconds, respectively. These times are highly influenced by loading effects.

18) If two inverters are cross coupled to perform as a flip-flop and the load on either side of the flip-flop is two loads or less, the cross-coupling must come into AND inputs.

19) The length of cross-coupling leads of inverters to be used as a flip-flop must not exceed six inches.

20) In applications where an asynchronous signal forms an AND gate with an N---, V---, or Y--- term, allow a minimum of three clock-phase times ($187.5 \times 10^{-9}$ sec) before probing the flip-flop output for reliable information.



EVEN PLANE
INHIBIT DRIVER
Card Type C00

FUNCTION

The function of the circuits on this card is to allow a 340 ma inhibit current to flow from the +40v source at pin 6 to the inhibit winding at pin 1 or pin 15. This occurs whenever all inputs to the respective circuit are at the logical "1" level of -5.8v. The inhibit circuit contains a series 120-ohm resistor so that the resulting current is approximately 340 ma.

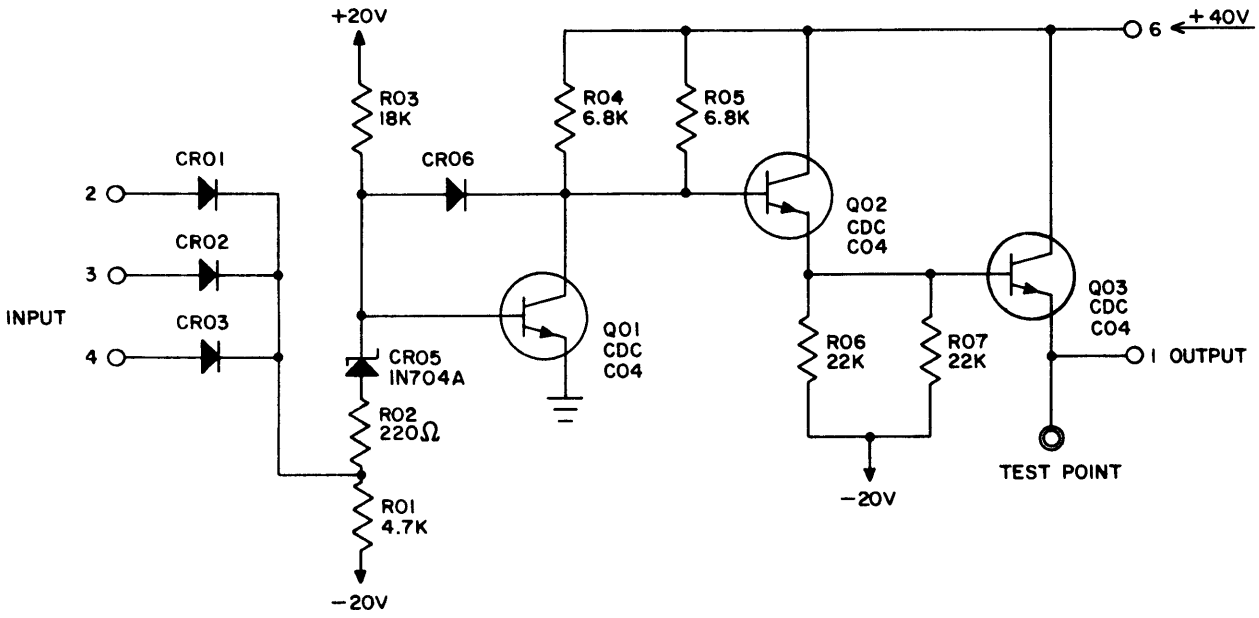
OPERATION

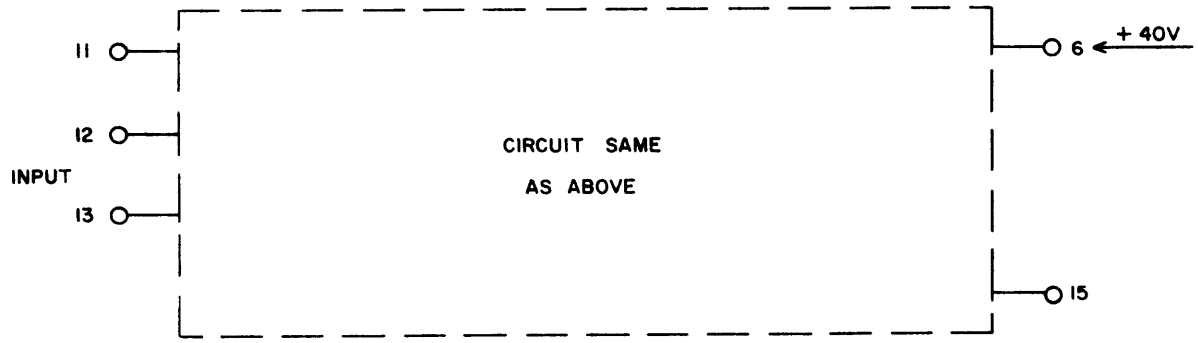
Each circuit has a three-way logical AND input, meaning that all inputs must be at the -5.8v "1" level in order for an input to be sensed. A -1.1v "0" signal on any input disables the AND. An unused input acts as a steady "1" if left open, or as a steady "0" if grounded.

A level-shifting action is provided to the base of Q01 by resistors R01, R02, R03, and the 4.1v zener diode CR05. The zener diode CR05 is reverse biased so that its operating point is beyond the knee of the breakdown region; thus the cathode remains approximately 4.1v positive with respect to the anode, regardless of current fluctuations.

When a -1.1v "0" signal appears at an input, the zener diode CR05 places a forward bias on the base of Q01. Transistor Q01 then switches to a state of heavy conduction. It is held out of saturation by the feedback diode CR06 and its collector voltage is approximately +0.4v. The low collector voltage of Q01 is also the base voltage of Q02, which is connected as an emitter follower. The emitter voltage of Q02 is equal to its +0.4v base voltage minus its base-emitter junction drop, and is approximately -0.3v. This provides sufficient forward bias so that a minimum conduction is maintained through Q02. Transistor Q03 is connected as an emitter follower with the inhibit winding load in series with the emitter. The emitter of Q03 is connected to ground through the inhibit line. The base-emitter junction is therefore reverse biased by the -0.3v input, so that Q03 is cut off. This disables the current path from the +40v supply to the inhibit winding.

With the AND input satisfied by -5.8v "1" signals, the base of Q01 is biased at approximately -1.5v and Q01 is cut off. The collector voltage of Q01 rises to approximately +38.5v (40v minus the IR drop across R03 and R04). This provides drive to the




NOTES:

1. EACH CIRCUIT HAS THREE "AND" INPUTS.
2. TRANSISTORS Q02 & Q03 CONDUCT WHEN ALL INPUTS ARE -5.8V "1".
3. ALL DIODES ARE HD2969 UNLESS OTHERWISE INDICATED.

# EVEN PLANE

Inhibit Driver C00

base-emitter junction of Q02. Transistor Q02 is connected as an emitter follower; thus its emitter voltage becomes approximately +38v. This provides a strong forward bias to the base of Q03, causing Q03 to conduct heavily. The voltage applied to the inhibit line is the emitter voltage of Q03 and is approximately +37.5v. The 340 ma inhibit current is also the emitter current of Q03, and is allowed to flow when Q03 switches to the conduction state.

## CLOCK OSCILLATOR-AMPLIFIER
Card Type C01

### GENERAL
The clock oscillator-amplifier shown on page 33 is essentially a tank circuit which may be tuned through a small range around 8 megacycles, with drive provided to the tank by two transistor amplifiers. The transistors are connected in a push-pull configuration, with the two circuit inputs directly connected to their bases. When the transistor inputs are provided with cross-coupled feedback from the oscillator transformer secondary, a continuous self-oscillation is maintained.

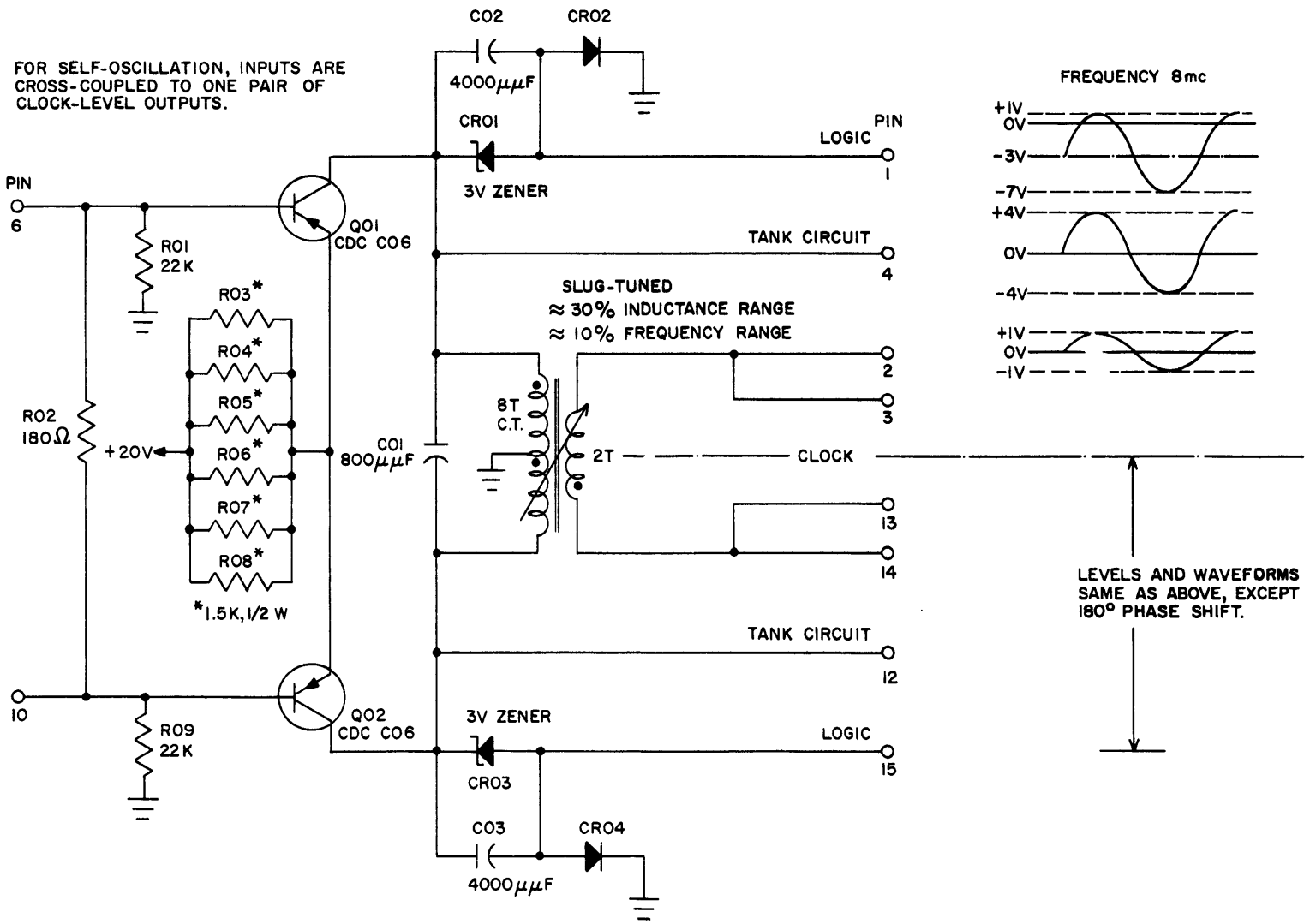
The circuit is designed so that, if external drive is provided to the inputs, the two transistors will operate as sine wave amplifiers, providing a two-phase output at the tank frequency.

### PYRAMID CONNECTION
The computer timing configuration for which this circuit is designed is an oscillator-amplifier pyramid, as shown on page 34 The master oscillator is a clock circuit connected as a feedback oscillator. To avoid undue loading effects, the master oscillator is permitted to drive only 2 amplifiers.

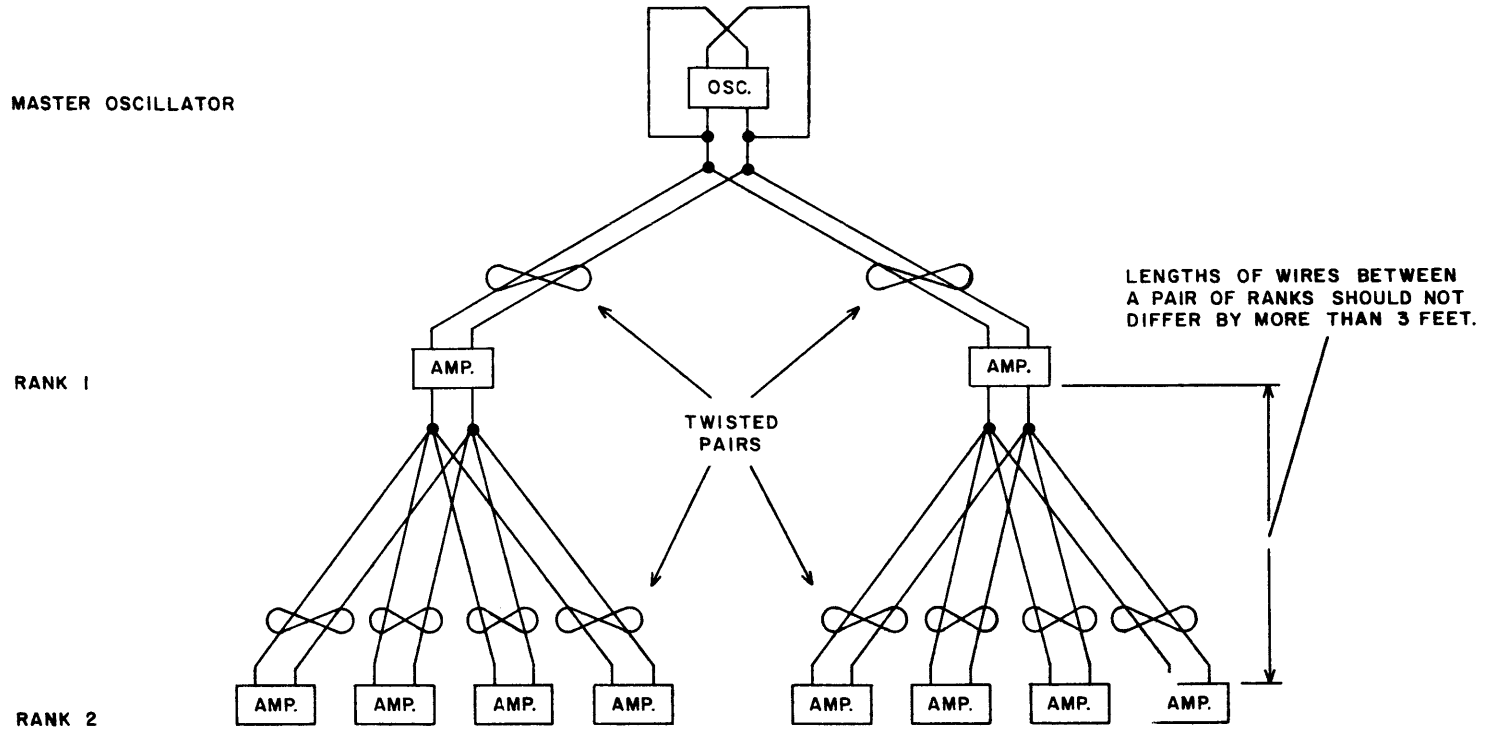
The ranks of amplifiers are clock circuits which receive external inputs and function as push-pull sine wave amplifiers. Each amplifier is capable of driving 4 others; thus, the pyramid effect is produced. Each amplifier in a rank must be in phase with every other amplifier in that same rank, although it is not necessary for the ranks to be in phase with each other or with the master oscillator. Outputs to the logic are taken only from the final rank of amplifiers.

### CIRCUIT OPERATION
The driving transistors Q01 and Q02 are CDC C06's and are connected in a push-pull configuration. Only one transistor is necessary to sustain oscillation; however, two transistors greatly increase the ability of the circuit to drive an unsymmetrical load.

Clock amplifier logic outputs are restricted to driving AND loads only. Through jumpered connections, an amplifier may drive up to 10 loads. Ideally, this is distributed




Clock Oscillator-Amplifier C01




NOTE:

1. MASTER OSCILLATOR MAY DRIVE 2 AMPLIFIERS.
2. EACH AMPLIFIER MAY DRIVE 4 FOLLOWING AMPLIFIERS.
3. ALL AMPLIFIERS IN THE SAME RANK ARE IN PHASE WITH EACH OTHER, BUT NOT NECESSARILY IN PHASE WITH ANY OTHER RANK OR WITH THE MASTER OSCILLATOR.

with 5 loads on each output phase; however, the loading may be unbalanced to 8 and 2, if necessary.

The characteristics of transistors Q01 and Q02 are such that they have a power handling capability of 150 mw at 25°C ambient. The average transistor dissipation in an oscillator circuit is of the order of 60 mw.

An 800 uuf silver-mica capacitor C01 having a low temperature coefficient and good stability is used in the tank circuit to resonate with the transformer inductance at a center frequency of 8 megacycles. The transformer inductance may be tuned through a range of approximately 30 percent by means of a low permeability ferrite slug. This has the effect of shifting the tank frequency through a range of approximately 10 percent.

The peak-to-peak signal develped across the tank is restricted to approximately 8v by the clamp diodes CR01 and CR04. The printed circuit card provides outputs at pins 4 and 12 at which this sine wave appears. If necessary, all tanks in a rank of amplifiers may be locked in phase with one another by connecting these outputs in parallel.

A logic-level signal is a sine wave about -3v, with peaks at +1v and -7v. It is produced by using a zener diode to shift the d-c reference level of the tank output. Logic-level outputs are taken only from the last rank of the clock pyramid and are available at pins 1 and 15.

The circuit on page 33 provides a clock-level output at pins 2, 3, 13, and 14, which is taken from the secondary of the tank transformer. The secondary winding consists of 2 turns, while the primary winding is 8 turns, center-tapped; therefore the clock-level output is a sine wave about ground with a peak-to-peak amplitude of approximately 2v.

The clock-level signals are used as drive signals throughout the clock pyramid, as shown on page 34. All wires used to transmit clock-level signals must be twisted pair, and the distance over which the signal is transmitted should be less than 15 feet. In addition, there should be less than a 3 foot variation in the lengths of wire used to transmit drive signals between a given pair of ranks.

PROCEDURE FOR TUNING A CLOCK PYRAMID

A scope equipped with a differential or dual-trace preamplifier, such as a Tektronix type CA, may be used for tuning the pyramid. The probe leads should be equal in length and must be grounded at the cards. The scope should be externally synchronized during step 3. Use the master oscillator for this.

Step 1.

Adjust the transformer of the master oscillator to the correct computer frequency. This may be done by setting the horizontal sweep at 0. 1 usec/ cm and adjusting until 8 peaks are seen across the 10 cm scope grid, if the desired frequency is 8 megacycles.

Step 2.

With the scope on a sensitive range, adjust one of the amplifiers in Rank 1 for maximum amplitude.

Step 3.

Using external sync, adjust the remaining amplifiers in Rank 1 to be in phase with the reference amplifier tuned in step 2. This may be done with a differential preamplifier, by inverting one signal and adding algebraically, and adjusting for minimum deflection with the scope on a sensitive range.

Other ranks are tuned according to steps 2 and 3.

GROUND RULES

A. Clock-level outputs.

1. The oscillator may drive 2 amplifiers in addition to providing its own feedback.
2. Each amplifier may drive 4 other amplifiers.
3. Interconnecting wires between ranks of amplifiers and from the master oscillator to rank 1 must be twisted pair.
4. Signals may be transmitted up to 15 feet.
5. There should be no more than a 3-foot difference in the lengths of interconnecting wires between a given pair of ranks.

B. Tank circuit output.

1. This is used only to phase-lock the tanks within a single rank of amplifiers, if necessary.

C. Logic-level outputs.

1. Clock outputs must always connect to logic card AND inputs.
2. A maximum of 10 loads may be driven.
3. A maximum of 8 loads may be driven by any single output; with 8 loads on one output, the opposite-phase output of that amplifier may drive only 2 loads, so that the total number does not exceed 10.

## CLAMP

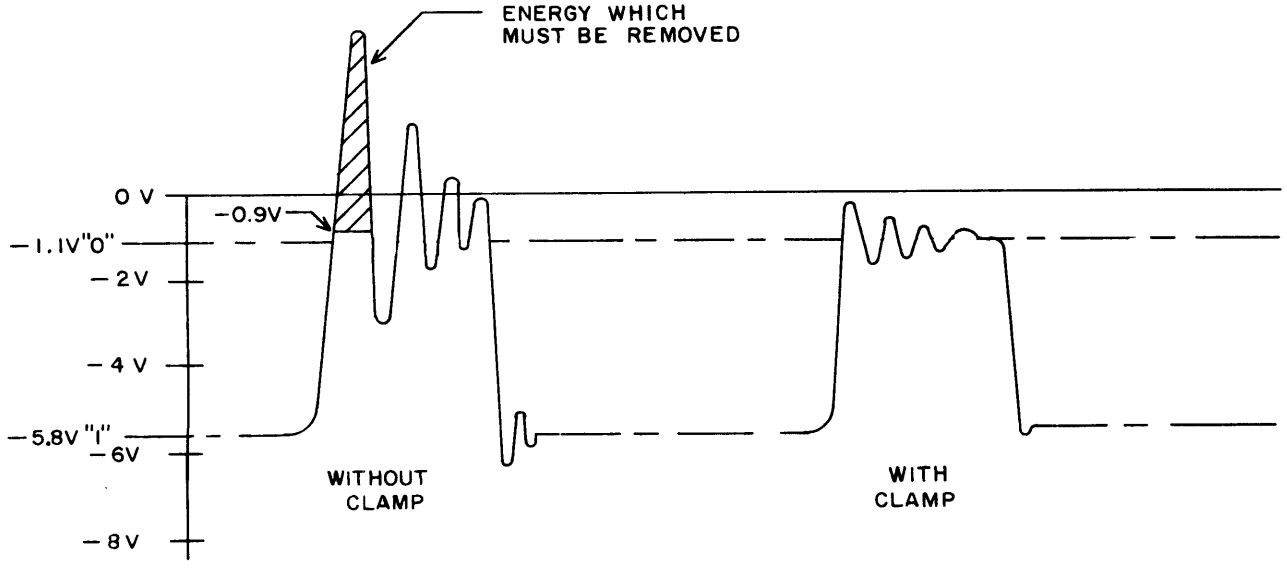
### Card Type C02

This circuit provides a clamp for logic circuit connecting lines, so that ringing is minimized. If sufficient energy is removed from the first overshoot, the remainder of the ringing has an amplitude less than the logic circuit threshold. A schematic of the clamp circuit is presented on page 39, with typical waveforms showing its effect on a line having excessive ringing.

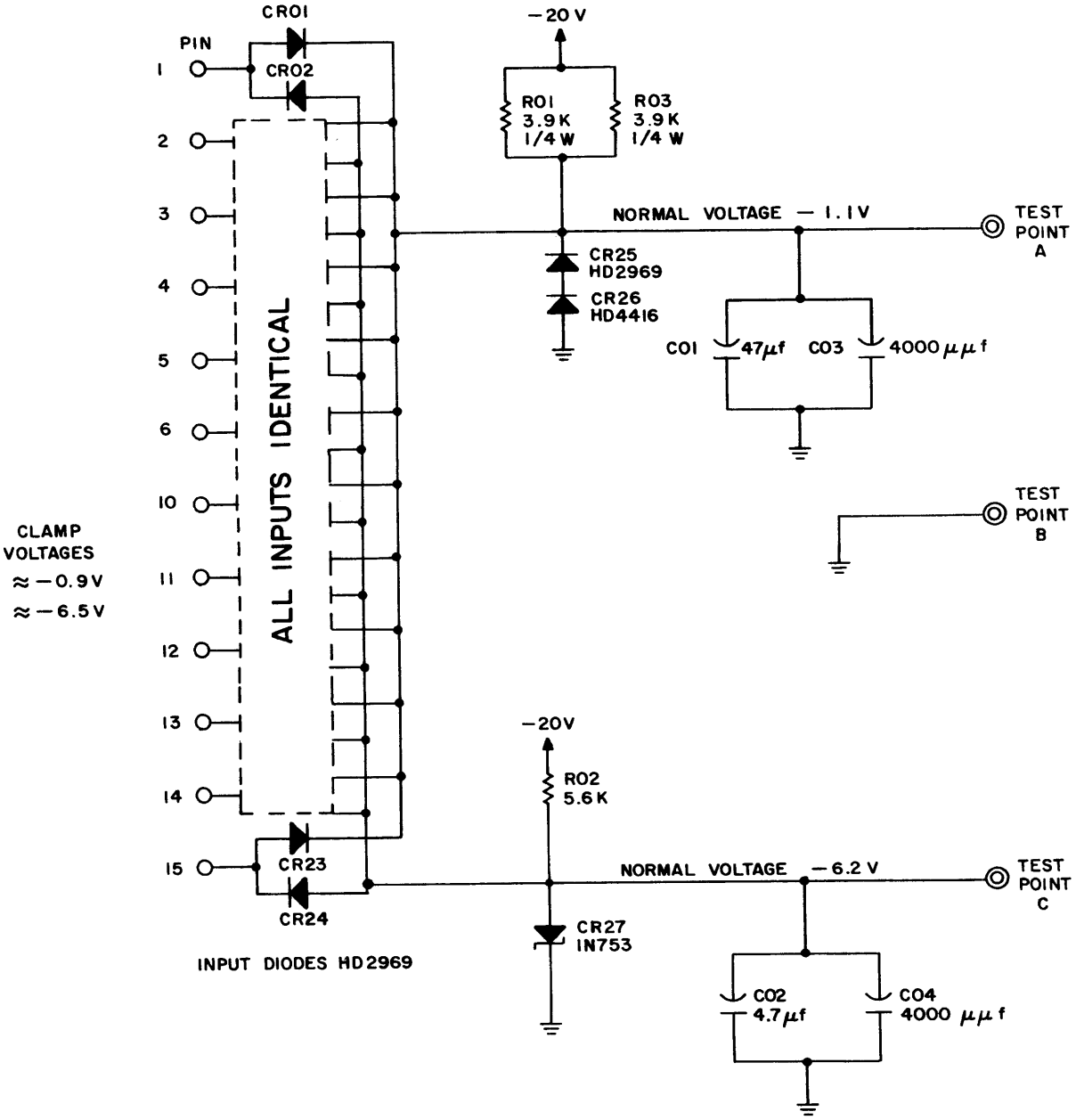
The clamp voltage in the positive direction is the sum of the forward drops across diodes CR25 and CR26, less the drop across the input diodes. It is approximately -0.9v.

The clamp voltage in the negative direction is the sum of the drop across zener diode CR27 plus the drop across the input diodes. It is approximately -6.5v.

Filtering is provided by capacitors C01, C02, C03, and C04. Due to their large area C01 and C02 present an appreciable amount of inductive reactance. It is therefore necessary to include the small capacitors C03 and C04 in order to filter out high-frequency spikes.




Typical Logic Line Voltage, 3600

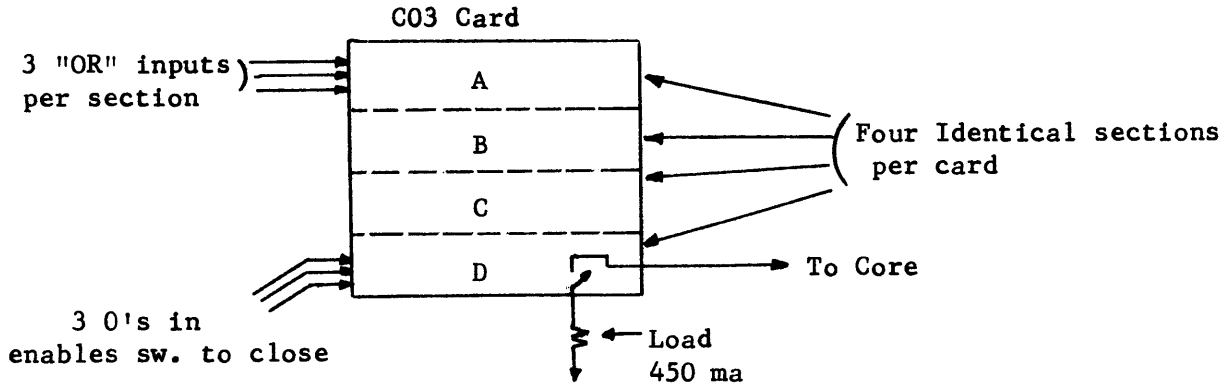

CR01
PIN
1
CR02
2
3
4
5
6
10
11
12
13
14
15
CR23
CR24
ALL INPUTS IDENTICAL
INPUT DIODES HD2969
CLAMP VOLTAGES
≈ −0.9 V
≈ −6.5 V
−20 V
R01 3.9K 1/4 W
R03 3.9K 1/4 W
NORMAL VOLTAGE — 1.1 V
TEST POINT A
CR25 HD2969
CR26 HD4416
C01 47μf
C03 4000 μμf
TEST POINT B
−20V
R02 5.6K
NORMAL VOLTAGE −6.2 V
TEST POINT C
CR27 IN753
C02 4.7μf
C04 4000 μμf

Clamp C02

LINE DRIVER

Card Type C03

This page will give you a big picture of the C03 Card. You can also use it for a quick reminder of the Card.




NOTE: The C03 Card supplies ground to C10 cards when all the inputs to a C03 section are "0's".

LINE DRIVER

Card Type C03

FUNCTION

The function of the circuits on this card is to enable 450 ma of positive current to flow from the output pins 1 or 15 to ground, whenever all inputs to the respective circuit are at the logical "0" level of -1.1v. Pins 1 and 15 connect to the two ends of the primary windings of eight memory driver transformers. During the memory cycle, one transformer will be center-tapped to +20v; thus current flow in either direction may be obtained by selecting one of the circuits on the C03 card.

The output pins 1 and 15 are connected as shown on page 42 by capacitor C03 and resistor R06, which form a series differentiating network. This connection transmits only those signals having a high rate of change, such as a sharp noise spike, and blocks entirely a steady d-c voltage. Thus, a noise spike appearing at pin 1 also appears at pin 15, and their total effect is to cancel each other. However, the d-c levels of pins 1 and 15 are completely separated if either circuit switches to the conduction state while the other remains cut off.

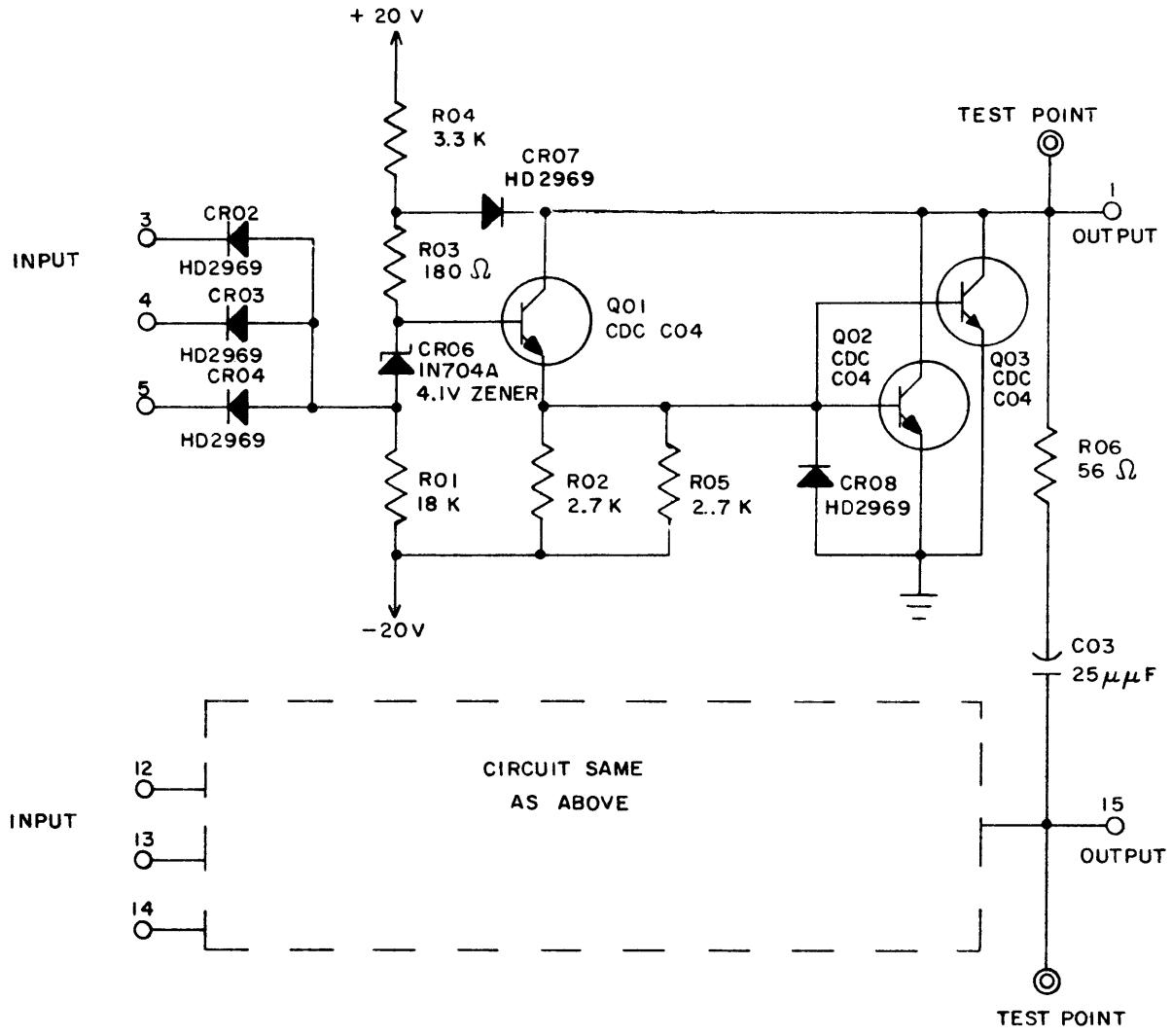
OPERATION

The two circuits on the card are identical and are labeled A and B. The following discussion of operation applies to either circuit; however, the component numbers mentioned are those appearing in circuit A.

A level shifting action is provided to the base and emitter of Q01 by resistors R01, R03, R04, and the 4.1v zener diode CR06. The zener diode CR06 is reverse biased so that its operating point is beyond the knee of the breakdown region; thus the cathode remains approximately 4.1v positive with respect to the anode, regardless of current fluctuations.

Each circuit has three logical OR inputs, meaning that a -5.8v "1" signal on any input is sensed, although a -1.1v "0" signal may be present simultaneously at another input. Any unused input acts as a steady "0", regardless whether it is grounded or left open.

When a -5.8v "1" signal appears at an input, the base of Q01 is biased at about -1v and it is cut off. The bases of Q02 and Q03 are held at approximately -0.3v by the forward drop of diode CR08, and they are likewise cut off. Thus, except for negligible leakage effects, pin 1 is completely isolated from ground and rises to a high positive voltage. Diode CR07 therefore provides a blocking action, preventing current from flowing




NOTES:

1. EACH CIRCUIT HAS 3 "OR" INPUTS.
2. TRANSISTORS SWITCH TO CONDUCTION STATE WHEN ALL INPUTS ARE −1.1 V "0".

Line Driver C03

through the transformer primary into pin 1.

If all of the circuit inputs are at the -1. 1v "0" level, zener diode CR06 holds the base of Q01 at a positive voltage. This forward bias is sufficient so that Q01 conducts heavily, but it is held out of deep saturation by diode CR07 and resistor R03. Transistor Q01 in its conduction state allows the +20v source, which connects to pin 1 through the transformer primary, to bias the bases of Q02 and Q03 at a positive potential. Thus they also conduct heavily, and positive current is allowed to flow from pin 1 to ground with only a drop of approximately 1v across Q02 and Q03.

Transistors Q02 and Q03 are grounded emitter stages driven by the emitter follower stage Q01. Their base drive is taken directly from the emitter of Q01; thus the input to Q02 and Q03 follows the input to Q01 and is increased by the gain of Q01. When Q01 switches on, it attempts to bias the bases of Q02 and Q03 well into the positive voltage domain, so that they also switch on and conduct heavily. Likewise, when Q01 switches off, Q02 and Q03 also switch off, and the voltage drop across diode CR08 applies a reverse bias of approximately 0. 3v to the base-emitter junctions of Q02 and Q03 so that they are well into the cut off region.

ODD PLANE
INHIBIT DRIVER
Card Type C04

FUNCTION

The function of the circuits on this card is to allow a 340 ma inhibit current to flow from pin 1 or 15 to ground, whenever all inputs to the respective circuit are at the logical "0" level of -1.1v. The inhibit wires are energized by a source of +40v, and each inhibit circuit contains a series 120-ohm resistor so the resulting current is approximately 340 ma. The odd plane inhibit wires terminate at either pin 1 or pin 15 of a C04 card, and the path is completed to ground allowing current to flow, if the respective inhibit generator circuit switches to its conduction state.

OPERATION

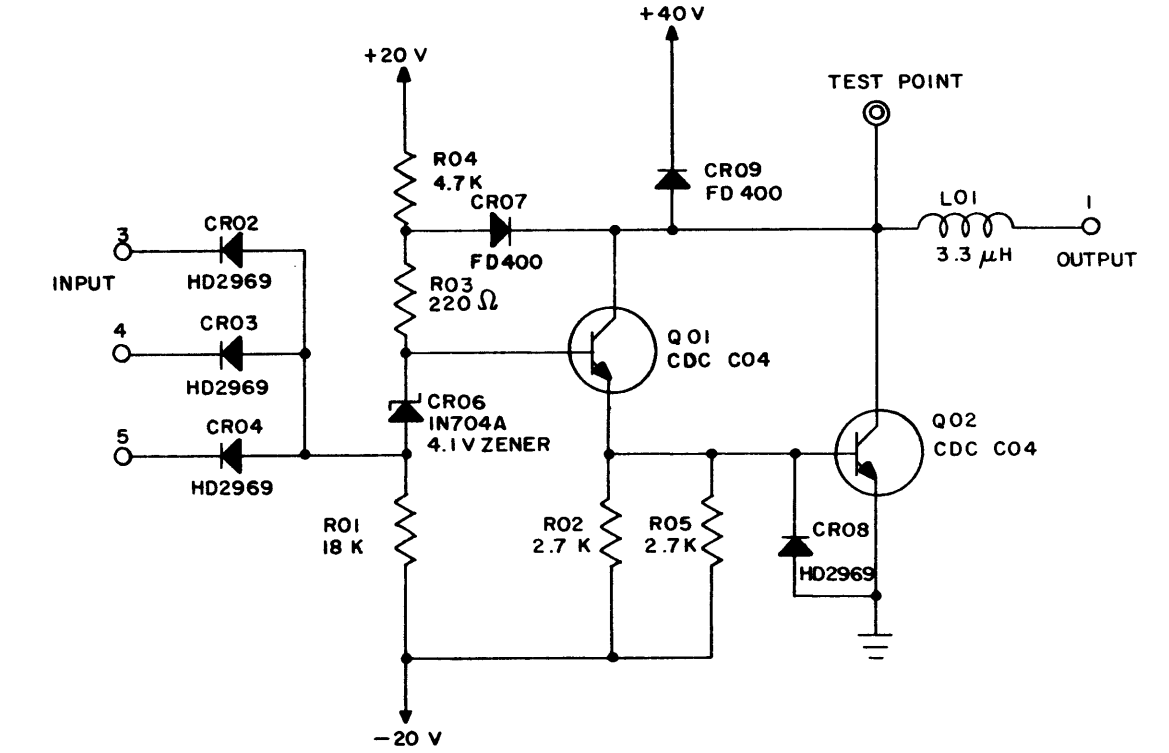
The two circuits contained on the card are identical and are labeled A and B. The following discussion of operation applies to either circuit but the component numbers mentioned are those appearing in circuit A.

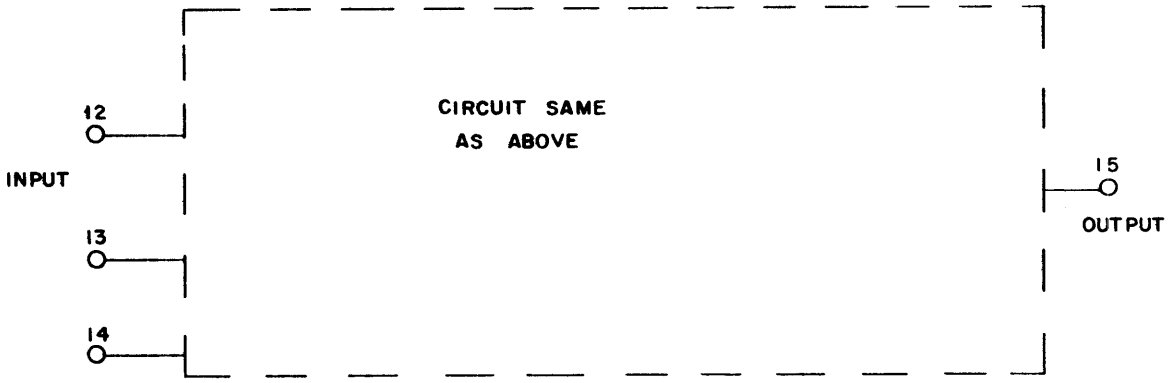
A level-shifting action is provided to the base and emitter of Q01 by resistors R01, R03, R04, and the 4.1v zener diode CR06. The zener diode CR06 is reverse biased so its operating point is beyond the knee of the breakdown region; thus the cathode remains approximately 4.1v positive with respect to the anode, regardless of current fluctuations.

Each circuit has three logical OR inputs, meaning that a -5.8v "1" signal on any input is sensed, although a -1.1v "0" signal may be present simultaneously at another input. Any unused input acts as a steady "0", regardless whether it is grounded or left open.

When a -5.8v "1" signal appears at an input, the base of Q01 is biased at about -1v and Q01 is cut off. The base of Q02 is held at approximately -0.3v by the forward drop of diode CR08, and Q02 is also cut off. Thus, except for negligible leakage effects, pin 1 is completely isolated from ground and rises to a high positive voltage. Diode CR07 therefore provides a blocking action, preventing current from flowing through the inhibit wire into pin 1.

If all of the circuit inputs are at the -1.1v "0" level, zener diode CR06 holds the base of Q01 at a sufficiently positive voltage so Q01 conducts heavily. In this state, diode




NOTES:

1. EACH CIRCUIT HAS THREE "OR" INPUTS.
2. A CIRCUIT WILL SWITCH TO ITS CONDUCTION STATE WHEN ALL INPUTS ARE −1.1 V "0".

## ODD PLANE

Inhibit Driver C04

CR07 holds Q01 out of saturation. Transistor Q01 in its conduction state allows the +40v source, which connects through the inhibit wire to pin 1, to bias the base of Q02 at a positive level. Thus transistor Q02 also conducts heavily, and positive current is allowed to flow from pin 1 to ground with only a drop of 1v across Q02.

Transistor Q02 is a grounded emitter stage driven by the emitter follower stage Q01. The base drive for Q02 is taken directly from the emitter of Q01; thus the input to Q02 follows the input to Q01 and is increased by the gain of Q01. When Q01 switches on, it attempts to bias the base of Q02 well into the positive voltage domain, so Q02 also switches on and conducts heavily. Likewise, when Q01 switches off, Q02 also switches off, and the voltage drop across diode CR08 applies a reverse bias of approximately 0.3v to the base-emitter junction of Q02 so it is well into the cut off region.

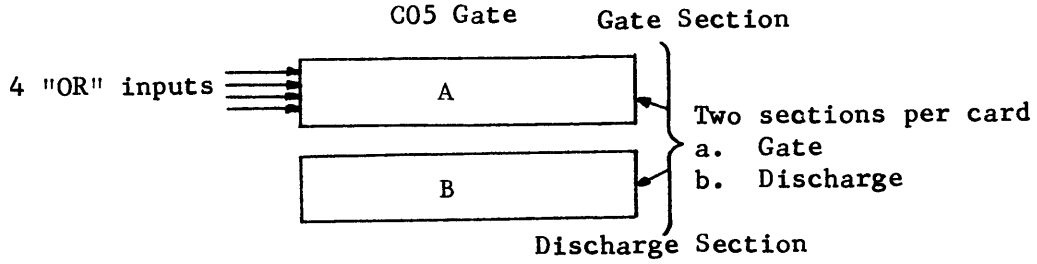
The connection of diode CR07 and the +40v source provides a clamp for the collector voltage of the transistors. When the transistors switch to the non-conducting state, the inductance of the inhibit wire tends to induce high-voltage transients; however, these inductive transients are clamped at +40v plus the drop across the silicon diode.

The 3.3 uh inductor in series with the output pin is for reducing ringing on the inhibit wire. The inductor increases the current rise time and hence reduces the overshoot.

GATE

Card Type C05

Here is a block diagram of the gate "C05" card. The detailed explanation is on the following pages.

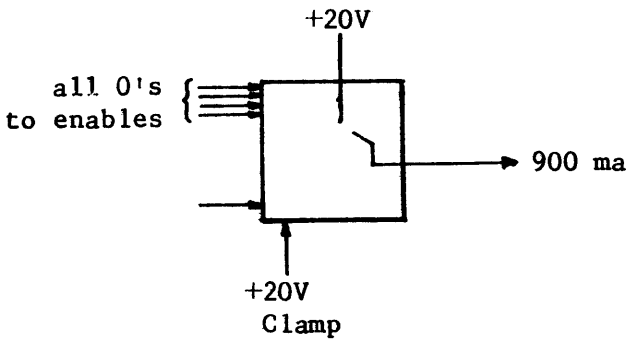



The gate section supplies +20V to C10 when turned on (needs all 0's in)

When the gate is turned on the discharger must be turned off.

Discharge section grounds C10 (transformer) when turned on by a "0" input.

Another way to look at this card is shown below:



FUNCTION

The function of the Gate circuit is to enable a current path from a +20v source through which current of the order of 900 ma flows to the primary windings of two memory driver transformers. Pin 4 connects to +20v and pins 1, 2, and 3 provide the output. The path from pin 4 to the output is enabled only when all inputs to the Gate circuit are at the logical "0" level of -1.1v.

The function of the Discharger circuit is to ground the primary windings of the two memory driver transformers previously energized. This removes stored charge from the windings and neutralizes the transformers. The Discharger circuit is enabled by a -1.1v "0" input.

OPERATION

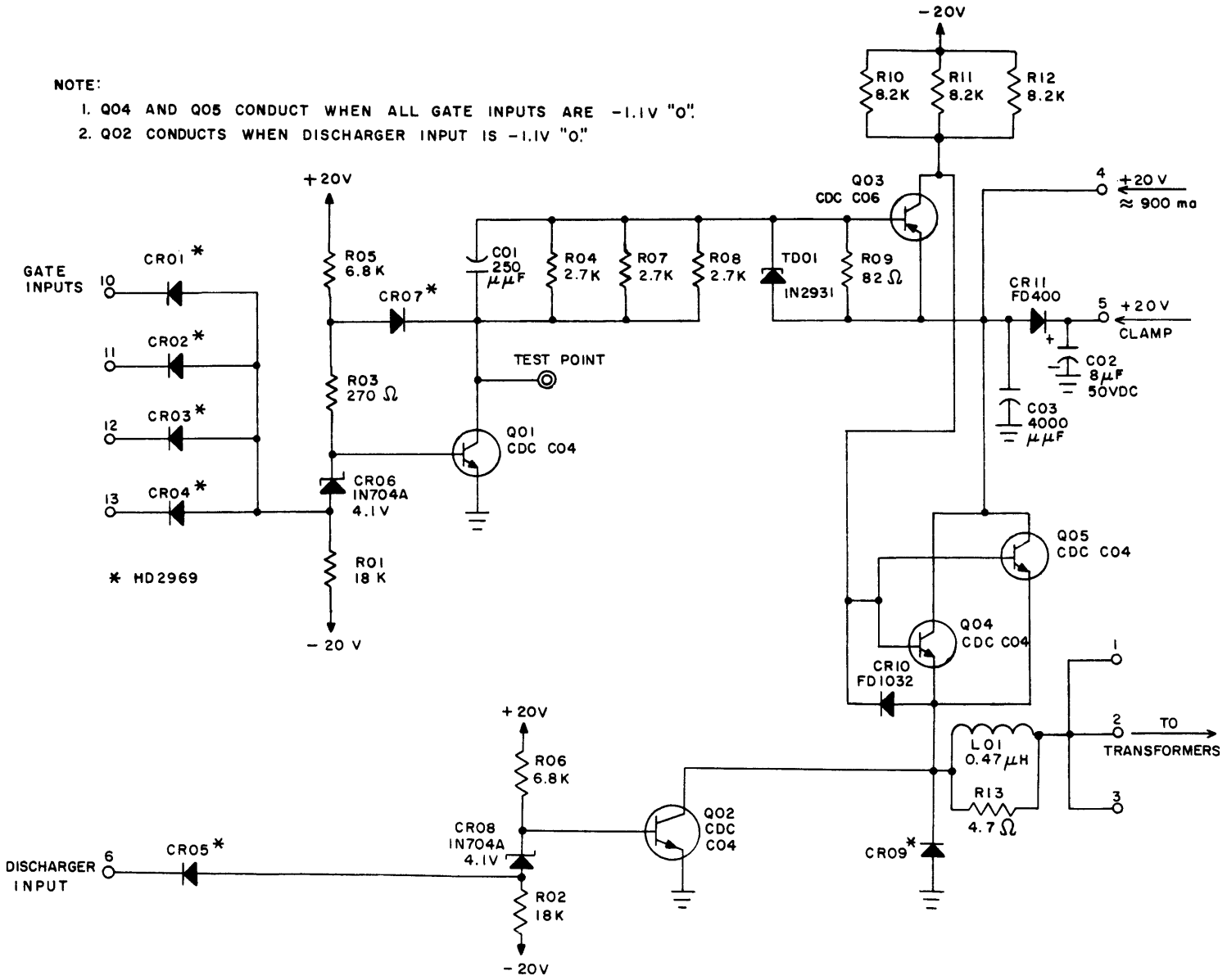
Pins 10 through 13 provide four logical OR inputs to the Gate circuit, and pin 6 provides an OR input to the Discharger. An unused input is interpreted as a steady "0", regardless whether it is grounded or left open.

A level-shifting action for the Gate inputs is performed by resistors R01, R03, R05, and the 4.1v zener diode CR06. The zener diode CR06 is reverse biased so its operating point is beyond the knee of the breakdown region; thus the cathode remains approximately 4.1v positive with respect to the anode, regardless of current fluctuations. Resistors R02, R06, and zener diode CR08 perform the level-shifting action for the Discharger.

With open circuits or logical "0" signals on all Gate inputs, the base of Q01 is at an approximate potential of +0.7v. It is prevented from going more positive by the low forward base-emitter impedance of Q01. During this time, Q01 is in the conduction state. However, if any input receives a -5.8v "1", the zener diode CR06 holds the base of Q01 at approximately -1.7v and Q01 is cut off.

During the time that Q01 is cut off by a "1" signal, its collector potential is raised to a high positive value by the +20v source attached to pin 4. Since no appreciable current now flows through the 82-ohm resistor and tunnel diode between base and emitter of Q03, it is also essentially cut off.

Gate C05


NOTE:
1. Q04 AND Q05 CONDUCT WHEN ALL GATE INPUTS ARE -1.1V "0".
2. Q02 CONDUCTS WHEN DISCHARGER INPUT IS -1.1V "0."
-20V
R10 8.2K
R11 8.2K
R12 8.2K
+20V
Q03 CDC C06
4 +20V ≈ 900 ma
GATE INPUTS
10
11
12
13
CR01 *
CR02 *
CR03 *
CR04 *
R05 6.8K
CR07 *
C01 250 μμF
R04 2.7K
R07 2.7K
R08 2.7K
TD01 IN2931
R09 82 Ω
CR11 FD400
5 +20V CLAMP
C02 8μF 50VDC
C03 4000 μμF
TEST POINT
R03 270 Ω
Q01 CDC C04
CR06 IN704A 4.1V
R01 18 K
* MD2969
-20 V
Q05 CDC C04
Q04 CDC C04
CR10 FD1032
1
2 TO TRANSFORMERS
3
L01 0.47μH
R13 4.7 Ω
CR09 *
+20V
R06 6.8K
CR08 IN704A 4.1V
Q02 CDC C04
DISCHARGER INPUT
6
CR05 *
R02 18K
-20V

When Q01 switches to its conducting state, current is allowed to flow from the +20v source at pin 4 through the tunnel diode and 82-ohm resistor between emitter and base of Q03, through the three parallel 2.7k resistors, and through Q01 to ground. A threshold level is provided by the tunnel diode, since in its low-voltage state, it does not allow Q03 to conduct. However, when current through the tunnel diode increases to 10 ma, it switches to its high-voltage state. This places approximately 0.8v forward potential on the base of Q03 causing it to switch to its conduction state. This enables the series circuit from +20v at pin 4 through Q03 and through the three parallel 2.7k resistors to -20v. The base drive for Q04 and Q05 is taken from the collector of Q03, and when Q03 conducts, turn-on current is provided for Q04 and Q05 so that they switch to the conduction state. Thus the circuit is completed, allowing positive current to flow from pin 4 to the output. When Q03 switches off, the voltage drop across diode CR10 applies a reverse bias of approximately 0.6v to the base-emitter junctions of Q04 and Q05, cutting them off.

Transistors Q04 and Q05 control a current of the order of 900 ma flowing in a highly inductive load. Diode CR09 is therefore provided so that when Q04 and Q05 interrupt the current, the induced high-voltage transient is dissipated with no effect on other transistors.

Diode CR11 acts as a clamp against positive voltage surges at the collectors of Q04 and Q05 when current is interrupted. Pin 5 connects to a separate +20v bus and prevents pin 4 from becoming more positive than +20.6v, taking into account the 0.6v drop across the silicon diode.

Capacitors C02 and C03 provide a smoothing filter for spikes and ripple in the +20v sources at pins 4 and 5. The 8 microfarad capacitor C02 is sufficient for ripple and low frequency fluctuations; however, it exhibits a certain amount of inductive reactance due to its large area. For this reason, it is necessary to include C03 which has negligible inductive reactance and is therefore effective in filtering high frequency spikes.

The Discharger circuit is enabled by a -1.1v "0" input on pin 6. This causes zener diode CR08 to apply sufficient forward bias to the base of Q02 so that Q02 switches to its maximum conduction state. Transistor Q02 thus provides a low impedance path to ground for any stored charge remaining in the primary windings of the two memory driver transformers.

## SENSE AMPLIFIER
### Card Type C06

This card amplifies and detects the pulses induced in a sense winding when a magnetic memory core switches polarity. The two ends of the sense winding are connected to pins 4 and 5, and when a core switches its magnetic state, the circuit produces a logical "0" output on pin 15.

The circuit may be conveniently divided into two sections: a differential voltage amplifier having a gain of approximately 100, and a discriminator having an output of approximately -13.6v. The output of -13.6v represents a logical "1" which changes to a logical "0" when a memory core switches its magnetic state. The following logic card interprets any signal more positive than -3v as a logical "0", however the discriminator output approaches -1.6v when a core switches.

AMPLIFIER

The differential voltage amplifier is the symmetrical portion of the circuit to the left of the diode bridge, as shown in the accompanying diagram. Input signals from the sense winding are received on pins 4 and 5. The ends of the sense winding are connected to these two pins, forming a series loop which threads all memory cores in a plane quadrant. The only ground reference to this loop is through the 1000-ohm resistor R02, thus the nominal 30 mv potential induced in the sense winding by the switching of a core is applied equally and oppositely to both input pins. This is amplified into a 3v signal which appears across the diode bridge.

The amplifier circuit is sensitive only to the difference in potential between pins 4 and 5, which is produced by the application of a double-ended signal from the sense winding. A simultaneous shift of the d-c reference level of both input pins produces only a negligible effect. It is possible for both inputs to fluctuate simultaneously by as much as 2v without producing more than 0.2v fluctuations at the diode bridge.

"Common mode rejection ratio" refers to the number used to represent the degree of sensitivity exhibited by a differential amplifier to potential differences between its inputs and simultaneous shifts of both inputs in the common mode. The number for this circuit is of the order of 40,000.

Resistors R01 and R03 are connected in series across the two inputs as shown. This relatively low resistance is in parallel with the input impedance of the amplifier, so that the total terminating impedance across the sense line is reduced. This has the effect of making the amplifier less sensitive to noise induced by the flow of inhibit current.

The 3.3 uh inductors in the emitter circuits of Q02 and Q03 determine the high frequency roll-off of the amplifier. This inductance reduces the gain at high frequencies and prevents the amplifier from responding to noise spikes.

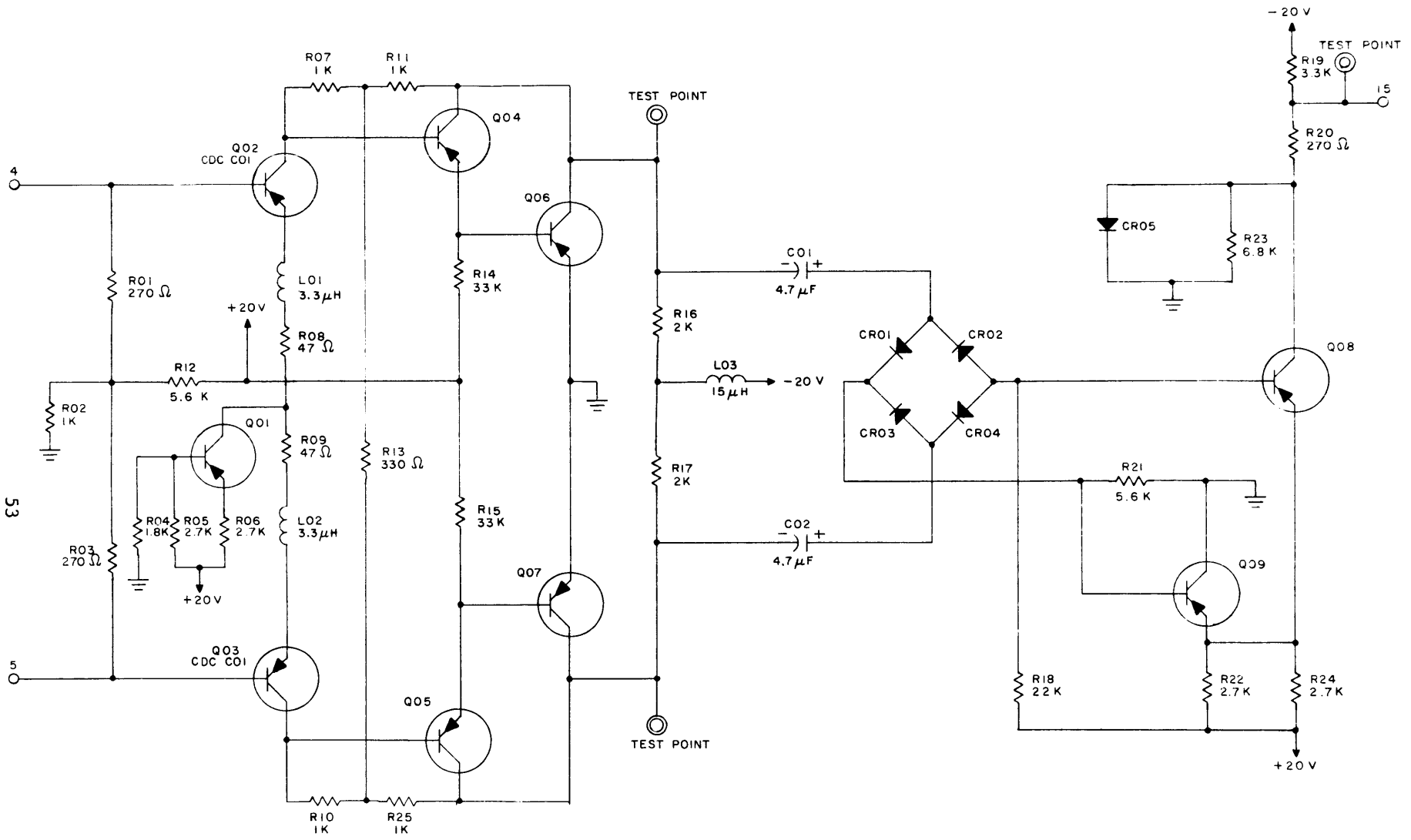
The signals produced by the memory cores are received and amplified in the double-ended fashion. As an example of operation, assume that the 30 mv potential from the memory core is in a direction so that pin 4 shifts negative 15 mv and pin 5 shifts positive 15 mv from the rest state. These potentials are applied to the bases of Q02 and Q03, causing Q02 to conduct more heavily while conduction through Q03 decreases. This action is further regulated by the constant-current source through Q01, so an emitter current increase in Q02 must be accompanied by a decrease in Q03.

Due to the action described above the collector of Q02 becomes more positive and the collector of Q03 becomes more negative. This, in turn, causes transistors Q04 and Q06 to conduct less heavily while conduction through Q05 and Q07 increases. The collectors of Q04 and Q06 therefore shift approximately 1.5v in the negative direction and the collectors of Q05 and Q07 shift a similar amount in the positive direction. A potential difference of 3v then exists across the diode bridge.

The signals from the collectors of Q02 and Q03 are amplified by a factor of 100 by Q04 and Q06, and by Q05 and Q07, respectively, which are connected as an emitter follower and a grounded emitter amplifier. Depending upon their particular characteristics, the two transistors are capable of providing a maximum available gain of the order of 1000. To insure stable operation, this is reduced to around 30 by the negative feedback connection of the two 1000-ohm resistors from collector to base. A portion of this negative feedback, however, is nullified by the 330-ohm resistor connecting the two feedback lines, so the over-all voltage gain of each of the stages is approximately 100.

DISCRIMINATOR

The discriminator is the portion of the circuit to the right of the diode bridge. Its function is to provide outputs at voltage levels suitable for use by logic circuits. The




NOTE:
1. ALL DIODES FD 1032.
2. ALL TRANSISTORS CDC C02, UNLESS OTHERWISE INDICATED.

Sense Amplifier C06

output of the discriminator is from pin 15 and is approximately -13.6v during the rest state. However, when a voltage appears across the diode bridge, the output at pin 15 approaches -1.6v which is interpreted as a logical "0".

The diodes used in the bridge are high speed silicon devices having a forward voltage drop of the order of 0.6v. Therefore, during the rest state a voltage-dividing action is provided from +20v to ground through the 22,000-ohm resistor R18, the diode bridge, and the 5600-ohm resistor R21. Due to the forward drop of the diodes, the base of Q08 is held at around 1.2v higher positive potential than the base of Q09. Transistor Q09 thus conducts quite heavily while Q08 conducts very little. Under these conditions the output at pin 15 is around -13.6v, due to the voltage dividing action of R19, R20, and R23. Transistor Q09 provides a low impedance path to ground, so the emitter of Q08 cannot rise to a high positive potential when it is in a state of low conduction.

The diode bridge rectifies the potential across it, so an input of either polarity results in a negative input to the base of Q08 and a positive input to the base of Q09. This has the effect of causing Q08 to conduct heavily while Q09, in turn, conducts very little. Transistor Q08 thus enables a low impedance path from +20v to ground through diode CR05, which is a silicon diode having a forward drop of approximately 0.6v. The anode of CR05 is therefore at approximately +0.6v, so that pin 15 is biased at approximately -1.6v by resistors R20, R19, and the -20v source. This output voltage level is interpreted as a logical "0".

## EMITTER FOLLOWER
### Card Type C07C

FUNCTION

The function of this circuit is to convert inputs received from a terminated 200-ohm delay line into outputs suitable for driving a logic card load. This circuit provides a high impedance load for the delay line, avoiding excessive current drain which affects its operating characteristics.

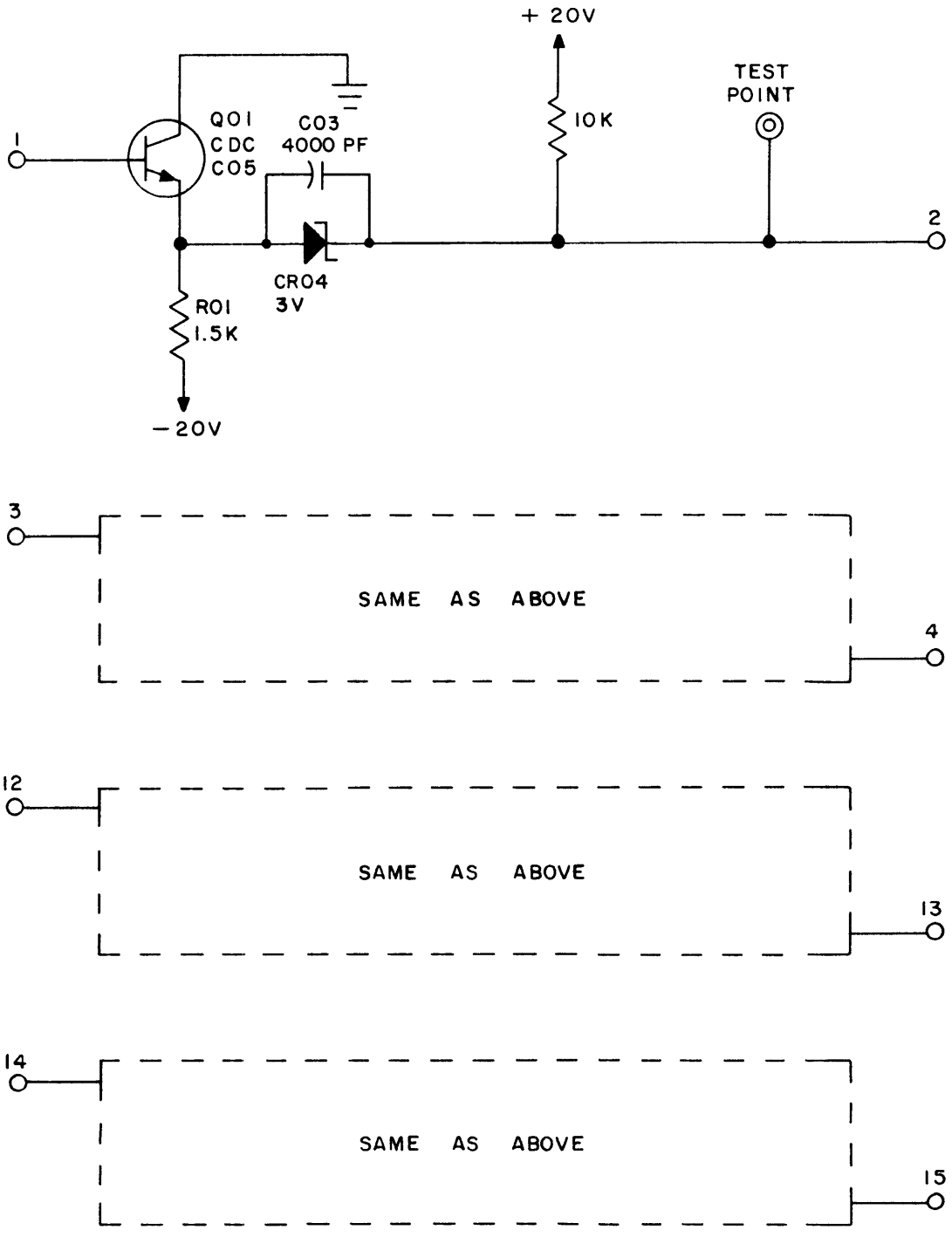
OPERATION

The delay line is driven by the circuit on card type C08; thus its input signal levels are approximately -0.3v and -10v. However, due to integrating characteristics and attenuation, the peak voltage levels tend to diminish slightly as the signal travels down the delay line. The input signal levels of the emitter follower circuit are therefore of the order of -0.3v and -10v, depending upon the point of the delay line from which the signal is taken.

A -0.3v input results in an output near ground which is interpreted as a logical "0".
A -10v input results in an output of approximately -9.3v which is interpreted as a logical "1".

Transistor Q01 is an NPN silicon type CDC C05. It is connected as an emitter follower; thus its emitter voltage is always approximately 0.7v more negative than the circuit input.

CR04 is a zener diode having a voltage drop of approximately 3v. This holds the circuit output 3v more positive than the emitter of Q01.




Emitter Follower C07C

## DELAY LINE DRIVER
Card Type C08

### FUNCTION
The function of this circuit is to provide an output suitable for driving a terminated 200-ohm delay line. With a 200-ohm load at pin 1 and the circuit in its quiescent state, the output voltage level is approximately -10v. Upon receipt of a -5.8v "1" input, both transistors switch to a state of heavy conduction and the output voltage becomes approximately -0.3v.

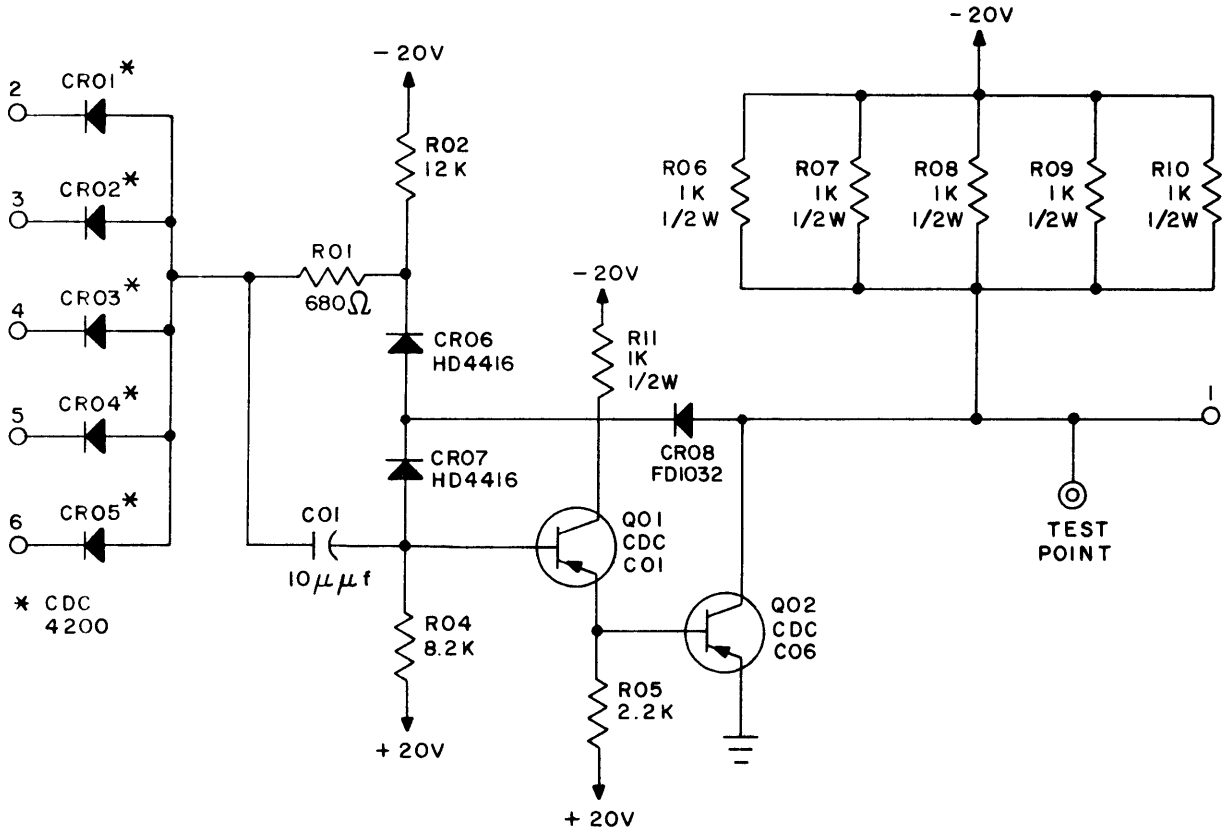
### OPERATION
The circuit has 5 logical OR inputs; thus a -5.8v "1" on any input activates the circuit. An unused input is effectively a steady "0", regardless whether it is grounded or left open.

An input level-shifting action is provided by the two forward-drop diodes CR06 and CR07. These are silicon diodes having a forward voltage drop of approximately 0.7v. The two diodes in series provide a voltage shift of +1.4v from the cathode of CR06 to the anode of CR07.

With -1.1v "0" inputs, the base of Q01 is held at approximately +1.3v by the level-shifting diodes. Transistor Q01 is connected as an emitter follower; thus its emitter voltage is equal to the base voltage plus the base-emitter junction drop, and is approximately +1.6v. This provides sufficient forward bias so that minimum conduction is maintained through Q01. The emitter voltage of Q01 drives the base of Q02, which is a grounded emitter stage. The base-emitter junction of Q02 is therefore back-biased by the +1.6v input, and Q02 is cut off.

A -5.8v "1" input holds the base of Q01 at approximately -0.6v causing Q01 to conduct heavily. The emitter voltage of Q01 goes to approximately -0.3v, which causes Q02 to switch on and conduct heavily. In this state, the circuit output is clamped at approximately -0.6v by CR08.

With Q02 in the cut off state, its collector voltage tends to rise toward -20v. However, the 200-ohm load acts as a voltage divider with the equivalent 200-ohm resistance of the five 1000-ohm resistors, and the output stabilizes at -10v.




NOTES:

1. CIRCUIT HAS 5 "OR" INPUTS.
2. A -5.8V "1" INPUT CAUSES TRANSISTORS TO CONDUCT.

Delay Line Driver C08

## INHIBIT COMPENSATOR
### Card Type C09

FUNCTION

The function of the circuits on this card is to enable a 340 ma current to flow from pin 1 or 15 to ground, whenever at least one input to the respective circuit is a -1.1v "0". The inhibit compensator circuits are energized by a +40v supply. Each circuit contains a series 133-ohm resistor external to the circuit on the card. Each inhibit compensator circuit terminates at either pin 1 or pin 15 of a C09 card, and the path is completed to ground allowing current to flow if the respective circuit attached to that pin switches to its conduction state.

OPERATION

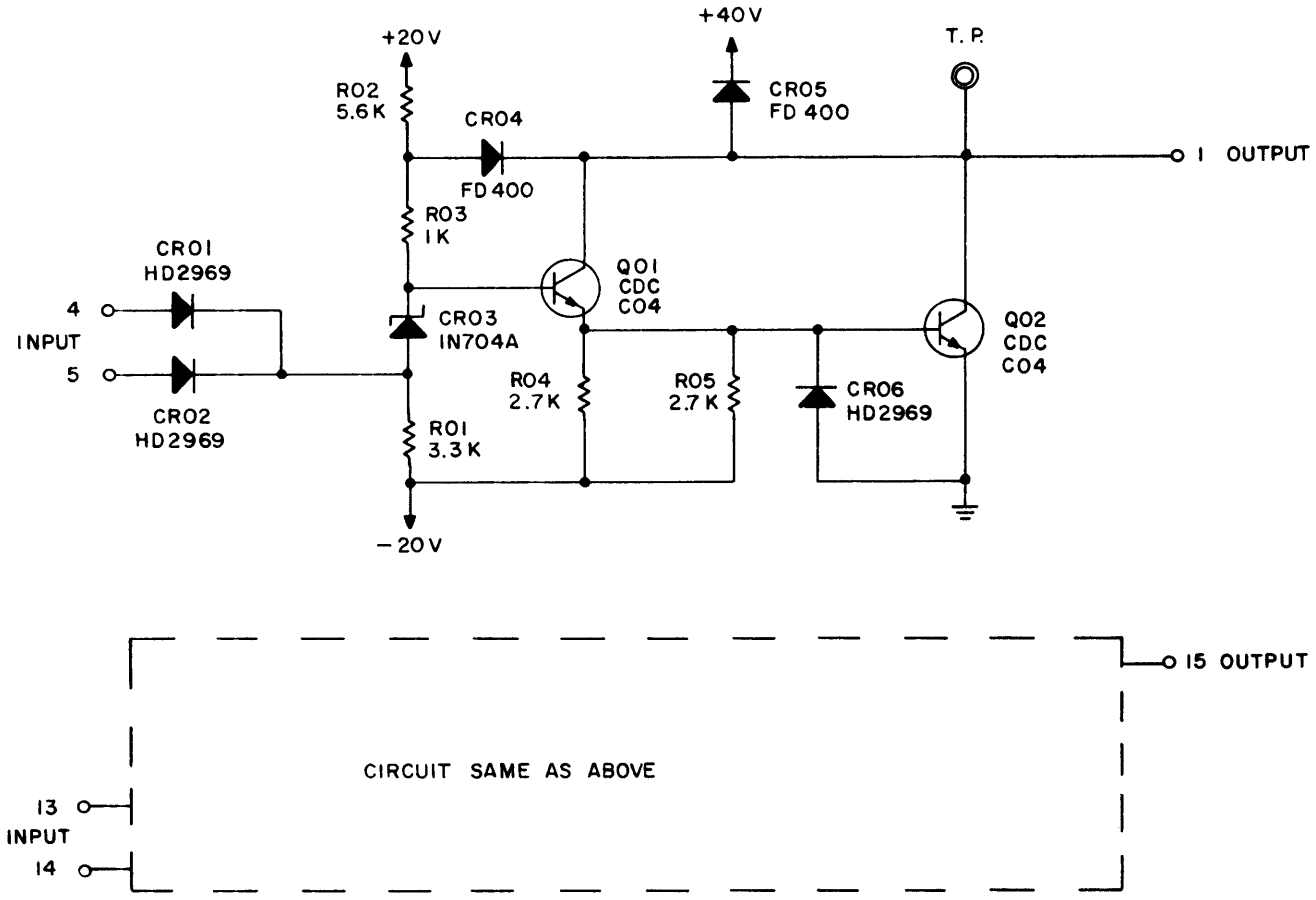
Each circuit has a two-way logical AND input, meaning that both inputs must be at the -5.8v "1" level for an input to be sensed. A -1.1v "0" signal on either input disables the AND. An unused input acts as a steady "1" if left open, or as a steady "0" if grounded.

The transistors are disabled if the AND is satisfied by two -5.8v "1" inputs, preventing current from flowing. If either input receives a -1.1v "0", the transistors switch to the conduction state and current is allowed to flow from the output pin to ground.

A level-shifting action is provided by the 4.1v zener diode CR03. This diode is reverse biased so its operating point is beyond the knee of the breakdown region; thus the cathode remains approximately 4.1v positive with respect to the anode, regardless of current fluctuations.

When the AND is satisfied by -5.8v "1" inputs, this voltage level plus the forward drop of diodes CR01 and CR02 holds the anode of CR03 at approximately -6.1v. The base of Q01 is therefore at approximately -2v. The emitter of Q01 is held at approximately -0.3v by the forward drop of CR06. This places a reverse bias of 1.7v across the base-emitter junction of Q01, so it is well into the cut off region. In addition, the 0.3v drop of CR06 reverse biases the base-emitter junction of Q02, so that it is also cut off. Thus, except for negligible leakage effects, the output pin is completely isolated from ground.

When either input receives a -1.1v "0", the anode of CR03 is held at approximately -1.4v. The 4.1v voltage differential across the zener diode CR03 attempts to hold the




NOTES:

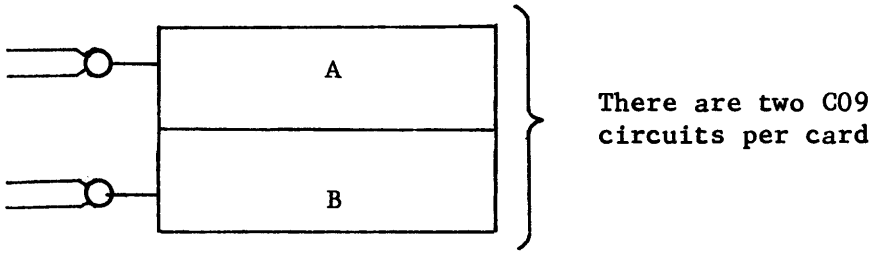
1. EACH CIRCUIT HAS A TWO-WAY "AND" INPUT.
2. A -1.1V "0" ON EITHER INPUT ENABLES CIRCUIT TO CONDUCT.
3. -5.8V "1'S" ON BOTH INPUTS PREVENT CIRCUIT FROM CONDUCTING.

Inhibit Compensator C09

base of Q01 at approximately +2.7v. This causes Q01 to switch on and conduct heavily, but it is clamped out of saturation of CR04. The emitter voltage of Q01 rises to approximately +2.2v, providing drive to the base of Q02. Transistor Q02 thus switches to the conduction state, allowing current to flow from the output pin to ground.

The connection of diode CR05 and the +40v supply provides a clamp for the collector voltage of the transistors. When the transistors switch to the nonconducting state, the inductance of the load tends to induce high-voltage transients; however, these inductive transients are clamped at +40v plus the drop across the silicon diode CR05.

Here is a more basic diagram of the Inhibit Compensator C09.



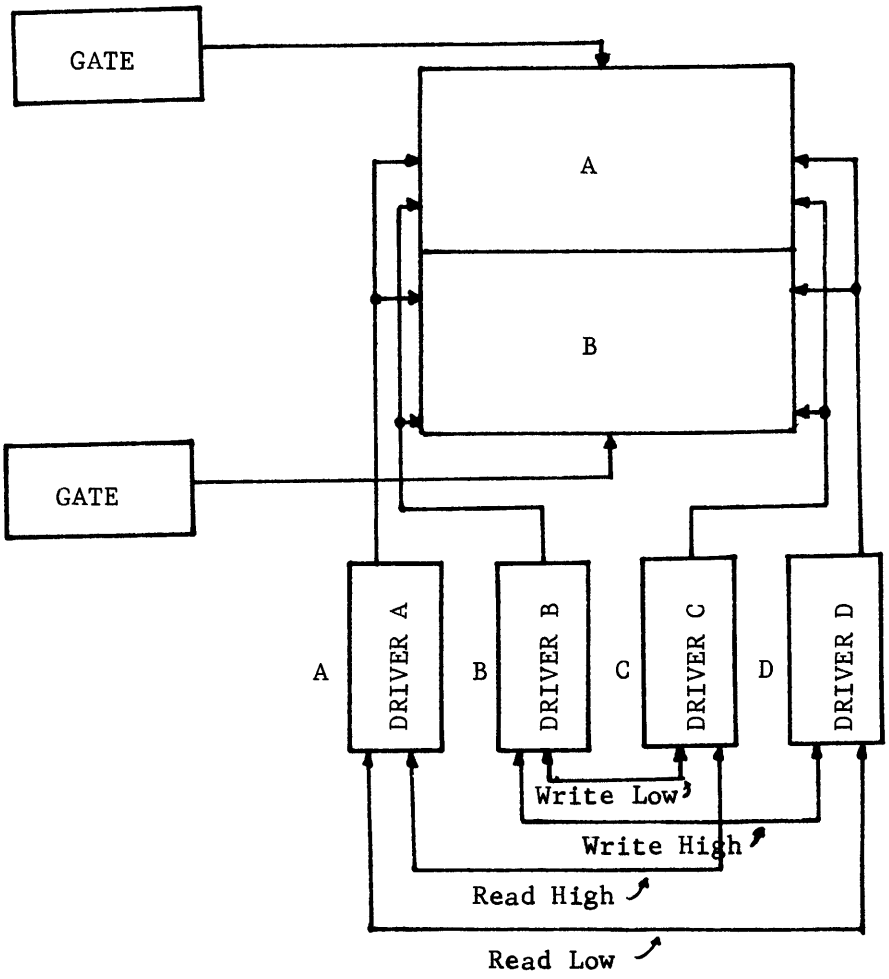

Remember that this card enables 340 ma to flow from the 40v supply with a "0" input. This card turns on when the associated inhibit drivers are off. This keeps a constant load on the 40v supply.

DRIVE LINE TRANSFORMER

C10

(BLOCK DIAGRAM)

The diagram below is so you can see how (in a Block Diagram fashion) the GATE, and DRIVER cards are connected to the transformer.




This card supplies half current (340 ma at 44v) to one of 4 driver lines. Each section supplies 2 drive lines. To turn on a drive line, 1 gate (C03) must be turned on.

## DRIVE LINE TRANSFORMER
### Card Type C10

FUNCTION

The function of this card is to provide half-currents of 340 ma at approximately 44v to the memory stack when supplied with primary power at the +20v level. The card contains four 3:4 voltage step-up transformers, each having two secondary windings of 32 turns and a center-tapped primary of 48 turns. The transformers are connected so that two operate simultaneously with their primary windings energized in parallel from +20v and their secondaries connected in series. The output voltages are therefore additive, resulting in levels of approximately 44v.

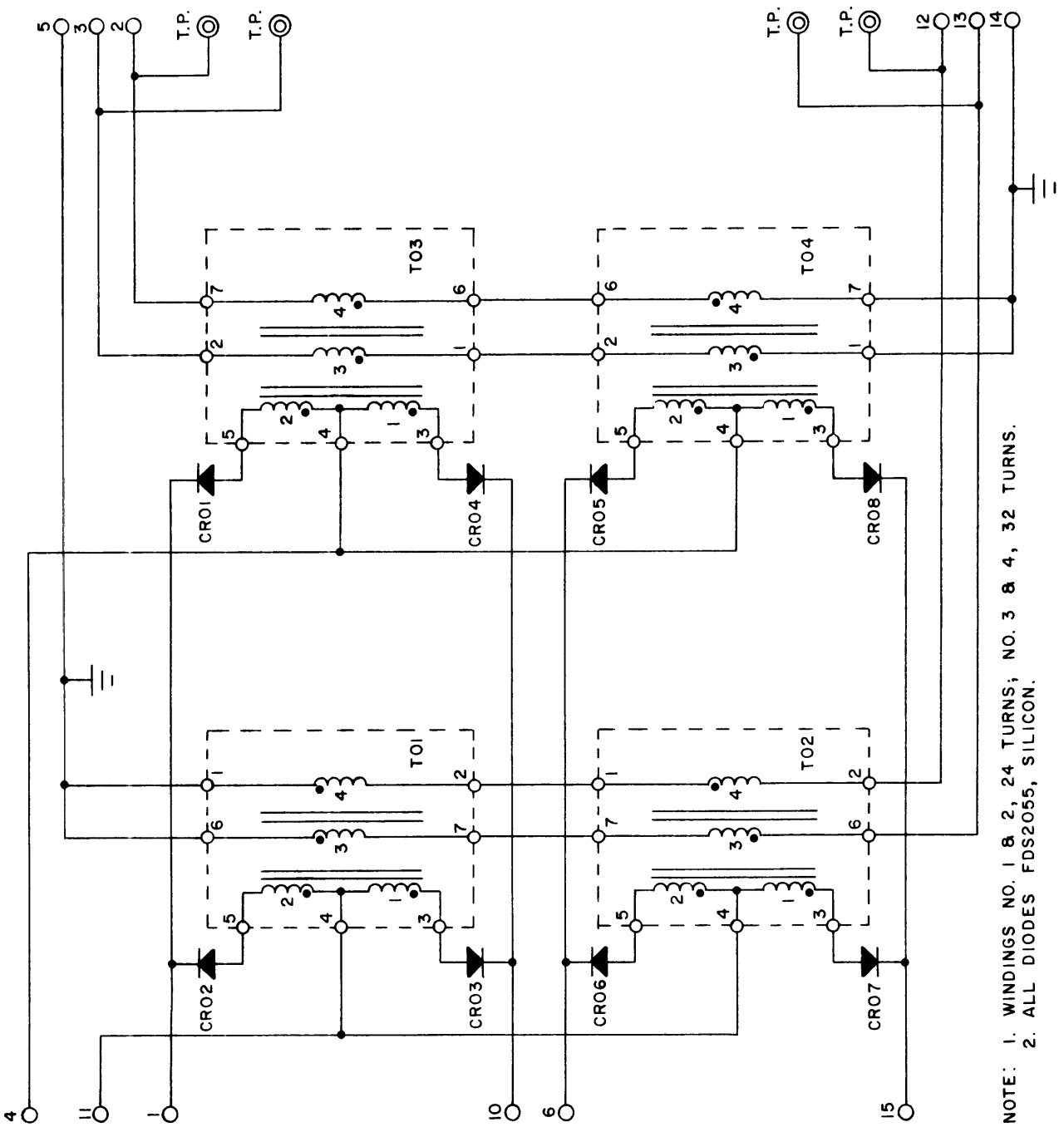
This card operates in conjunction with three other cards; a gate card which switches a source of +20v into the center taps of the transformer primaries, and with two transformer driver cards which allow current to flow from one of the primary windings to ground.

OPERATION

A schematic of the circuit contained on card type C10 is presented in the accompanying diagram, with the transformers indicated by dashed outlines. The transformers are identical, each having four windings and seven connecting pins as shown. Silicon diodes at transformer pins 3 and 5 provide isolation so current cannot flow through a primary winding in the wrong direction and prevent interaction between transformers.

The dots on the transformer windings indicate polarities according to the usual convention. For example, if current flows into the dotted end of the primary winding, current must flow out of the dotted end of the secondary winding. If a voltage is impressed across the primary winding so that the dotted end is positive, the dotted end of the secondary will also be positive.

As an example of operation, assume that card pin 11 is energized from a source of +20v. This is fed to the center tap of the primary windings of transformers T01 and T02. Then, by connecting card pins 1 or 10, and 6 or 15 to ground, it is possible to produce either +44v or -44v at either pin 12 or pin 13 while the other pin remains at essentially zero potential. The positive and negative potentials correspond to the memory cycle, in which a current of one polarity is used to read and the other to write.




Memory Drive Line Transformer C10

To produce +44v at pin 12, the external circuitry would connect card pins 10 and 15 to ground, allowing 450 ma to flow through windings # 1 of T01 and T02. The primary voltage is of the order of +18v, due to the drop across the silicon diode and external circuitry; however, the 3:4 transformer step-up produces a secondary voltage of approximately +22v.

It is seen that windings # 4 of T01 and T02 are connected in series so the voltages are additive, resulting in +44v at pin 12. It is further seen that windings # 3 are connected oppositely, so the voltages cancel and only a negligible effect is produced at pin 13. However, +44v appears at pin 13 with negligible voltage at pin 12 if the external circuitry grounds pin 6 instead of pin 15.

If it is desired to produce -44v at pin 12, then pins 1 and 6 are grounded; and if the -44v is to appear at pin 13, pins 1 and 15 are grounded.

Under the preceding sets of conditions, the voltages appearing on pins 12 and 13 appear on pins 2 and 3, if the source of +20v is gated into pin 4 instead of pin 11.

The various outputs available at pins 2, 3, 12, and 13 and the conditions necessary to produce them, are listed below. Pin 5 provides a common return for pins 12 and 13, and pin 14 provides a common return for pins 2 and 3.

| Gate +20v into: | Enable Ground Connection From: | Resulting Voltages at: Pin 2 | Pin 3 | Pin 12 | Pin 13 |
|---|---|---|---|---|---|
| Pin 4 | Pins 6 and 10 | +44v | | | |
| Pin 4 | Pins 1 and 15 | -44v | | | |
| Pin 4 | Pins 10 and 15 | | +44v | | |
| Pin 4 | Pins 1 and 6 | | -44v | | |
| Pin 11 | Pins 10 and 15 | | | +44v | |
| Pin 11 | Pins 1 and 6 | | | -44v | |
| Pin 11 | Pins 6 and 10 | | | | +44v |
| Pin 11 | Pins 1 and 15 | | | | -44v |

## TRANSMITTER AND RECEIVER
## Card Types C62A, C61, and C61B

GENERAL

The circuit configuration shown on page 68 performs high speed transmission of digital information from one module to another. Inputs to the transmitter circuit are logical "1's" and "0's" of -5.8v and -1.1v, respectively. The transmitter converts these single-ended inputs to double-ended outputs suitable for transmission over a balanced transmission line. Tests using an 8-megacycle bit rate input have shown that 1 transmitter satisfactorily drives 20 receivers and 19 unused transmitters located at any point along a 200 foot transmission line.

The transmission line is twisted-pair having a characteristic surge impedance of approximately 110 ohms and is terminated at each end in its characteristic impedance. Transmission signal levels are approximately 0.5v line-to-line, and a "1" is distinguished from a "0" by a full voltage reversal.

The line voltage levels which represent a "0" are established by current flow from the +20v to the -20v source at the terminating resistors. Each of these currents is of the order of 5 ma, so that the total voltage developed across the terminating resistors is approximately 0.5v.

When the 3-way AND input to the transmitter is disabled by a "0", transistor Q01 is turned on and current is shunted around the two constant current drivers Q02 and Q03. With the AND enabled by "1" inputs, Q01 is turned off, thus allowing Q02 and Q03 to drive a constant 20 ma into the transmission line. Originally, the bias networks on the line were producing a 5 ma current flow in one direction through the terminating resistors, but when the transmitter switches on, the direction of net current flow through the terminating resistors effectively reverses. The current from the transmitter divides into two 10 ma currents which flow through each line termination. This current is in the opposite direction to the 5 ma bias current; thus the net current flow is 5 ma in the opposite direction, producing a voltage drop equal and opposite to the original voltage. This results in a full voltage reversal for separating a "1" from a "0", although the signal level remains of the order of 0.5v line-to-line.

TRANSMITTER, Card Type C62A

The printed circuit card contains two identical transmitter circuits designated A and B. A typical circuit is shown on page 68.

The logic input circuitry consists of a 3-way AND. The output of a standard logic card constitutes a proper input to a transmitter. A logical "1" input causes transistor Q01 to turn off and Q02 and Q03 to turn on, while a "0" input has the opposite effect.

A -1.1v "0" input causes the emitter-base junction of Q01 to be forward biased, fully turning on Q01. When Q01 is turned on, a shunt path for current is provided around Q02 and Q03. Since Q02 and Q03 no longer have a source of current, no current is injected into the transmission line.

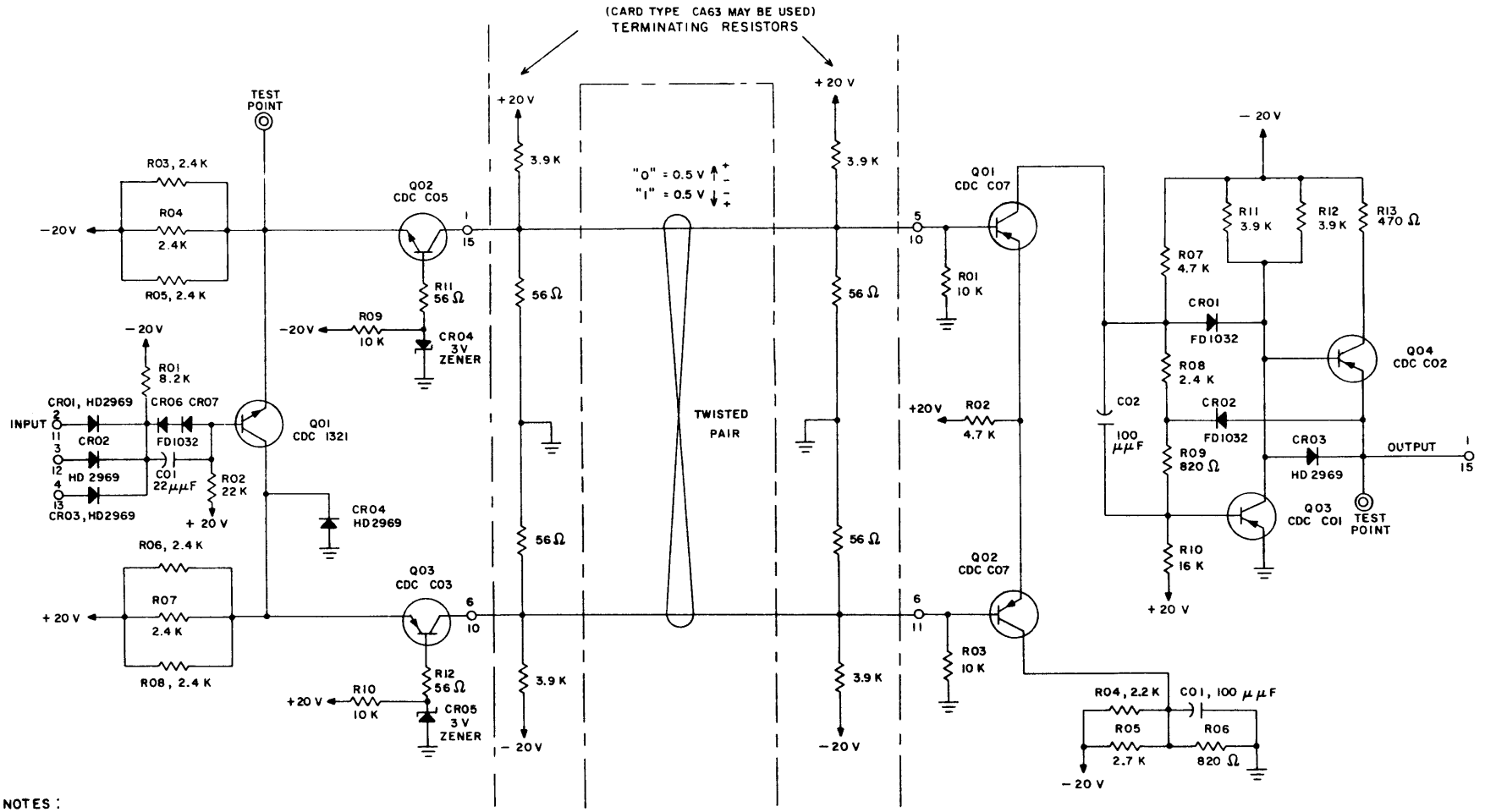
When the AND input is satisfied, the base of Q01 is held at approximately -5 volts. This reverse biases the emitter-base junction by approximately 3 volts and causes Q01 to be turned off. Since the shunt path for current around Q02 and Q03 no longer exists, they become constant current generators of opposite polarities. Q03 injects a current of approximately 20 ma into the line and a like amount of current flows out of the line into Q02.

The base networks of Q02 and Q03 each contain a 3v zener diode which performs two functions. In the first case, the zener diode sets the voltage level at which the emitters of Q02 and Q03 reach their turned-on state. This, in turn, sets the threshold that must be overcome at the base of Q01, since its emitter is at the same potential as the emitter of Q02. In the second case, the zener diodes set the base voltages of Q02 and Q03 which determine how much noise voltage is allowed at the collectors before the collector-base junctions become forward biased. This value of noise voltage is something over 3 volts since the forward drop of the collector-base junctions adds to the zener diode voltage. This means that the transmitter operates satisfactorily with up to 3 volts of random noise on the transmission line.

The transmitter must be connected to the line in only one polarity, as shown on page 68. This is necessary to provide current through the terminating resistors in a direction opposite the bias current.

TRANSMISSION LINE

A terminated balanced twisted-pair transmission line carries digital information from the transmitter to the receiver. This information is in the form of line-to-line




NOTES :

1. THE CONNECTION SHOWN DOES NOT PROVIDE A LOGICAL INVERSION; A "1" INPUT RESULTS IN A "1" OUTPUT.
2. TO PRODUCE AN OVER-ALL LOGICAL INVERSION, THE TRANSMISSION LINE CONNECTION AT THE RECEIVER WOULD BE REVERSED.
3. THE TRANSMISSION LINE CONNECTION AT THE TRANSMITTER CAN NOT BE REVERSED, BECAUSE OF VOLTAGE POLARITIES.

Transmitter and Receiver C62 and C61

differential voltages of the order of 0.5v, with a complete voltage reversal distinguishing a "1" from a "0".

The surge impedance of the transmission line is 100 to 120 ohms. The line is terminated at each end with a 112-ohm resistive load, consisting of two 56-ohm resistors in series across the line with an optional center ground reference. This provides very good impedance matching and, as a result, reflections and standing waves are minimized.

The line is biased at each end by means of 3.9k resistors to +20v and -20v to achieve a 5 ma bias current through the terminating resistors. This holds the "0" state signal level at 0.5v line-to-line.

The length of a transmission line may be up to 200 feet, with as many as 20 transmitters and 20 receivers placed in parallel along its length.

Bit rates of 8 mc or greater are possible on a 200 foot line. Low bit rates over longer distances are limited by the d-c line losses; however transmitters may be paralleled for longer distances to overcome these losses.

The velocity of signal propagation along the line is approximately 50 percent to 60 percent of the velocity of light. This results in a time delay per foot of the order of 1.6 to 1.8 nanoseconds.

The balanced system using differential receiving techniques allows a difference in noise levels up to 3v to be tolerated between the transmitter ground reference and the receiver ground reference.

RECEIVER, Card Type C61B

The printed circuit card contains two identical receiver circuits designated A and B. A Typical example is presented on page 68. This portion of the circuit connected to the collector of Q01 is similar to a logical inverter, which is discussed elsewhere in this report.

This circuit functions as both a differential amplifier and a discriminator. It provides a logic output of either "1" or "0", according to the polarity of the differential 0.5v signal which the two input terminals receive from the transmission line.

The circuit inputs are connected directly into the bases of Q01 and Q02. The 0.5v differential input is centered about ground, so one input shifts approximately 0.25v positive while the other input shifts negative a similar amount. The two input transistors Q01 and Q02 are PNP type CDC C07's; thus the transistor which receives the negative input conducts more heavily while the one receiving the positive input conducts less heavily.

The circuit is such that a negative input to the base of Q01 and a positive input to the base of Q02 results in a logical "1" at the receiver output. Under the opposite conditions of a positive input to Q01 and a negative input to Q02, the output is a logical "0". Thus, by reversing the connections at the receiver inputs, it is possible for a given set of conditions on the transmission line to produce either a "1" or a "0" at the receiver output.

The circuit shown on page 68 does not produce an inversion between input to the transmitter and output from the receiver. A "1" input to the transmitter produces a transmission line signal of approximately 0.5v line-to-line with the polarity as shown. This allows transistor Q01 to apply approximately 5 ma of collector current to the junction of R07, R08, and the anode of CR01, which causes Q03 to switch off and Q04 to switch on, providing a "1" output. In this state, transistor Q04 can drive 8 OR loads. With opposite conditions at the receiver input, the output can drive 8 AND loads.

GROUND RULES, using Receiver Card Type C61B

1. The output of a logic card constitutes a proper input to a transmitter.
2. The output of a receiver constitutes a proper input to a logic card.
3. A receiver may drive 8 OR loads, 8 AND loads, or any combination resulting in 8 loads total.
4. The transmission line is twisted-pair, having a surge impedance of 100 to 120 ohms.
5. The transmission line may be any length up to 200 feet.
6. The transmission line is terminated at each end in a resistive load approximately equal to its surge impedance.
7. A logical inversion between input to transmitter and output from receiver may or may not occur, depending upon the transmission line connections at the receiver.
8. The transmission line connections at the transmitter can not be reversed, due to the polarity of the line bias voltage.

9. Up to 20 transmitters and 20 receivers may be connected along a transmission line.
10. A transmitter having an 8 megacycle bit rate input will drive 20 receivers at the end of a 200 foot transmission line, with 19 inactive transmitters also connected to the line.
11. Inactive transmitters and receivers do not load a transmission line and do not have to be disconnected from it.
12. No more than 8 transmitters should be driven by an inverter and no more than 7 should be driven by a flip-flop.

GROUND RULES, using Receiver Card Type C61

2. The output of a receiver constitutes a proper input to a logic card. However, when the output of the receiver is used with other terms to perform a logical function at the input of a logic circuit, the receiver output comes in on an AND input. This automatically implies that a receiver driving a flip-flop or control delay must feed an AND input. The above restriction may be violated when the output at the "1" level exceeds 0.6 usec duration.

All Ground Rules, other than number 2, for Card Type C61 are the same as for C61B.

# RESYNC CIRCUIT
## Card Types C64A, C65A, C66A

### GENERAL

The resync circuit shown on page 74 is contained on three printed circuit cards, the type numbers being C64, C65, and C66. The logical operation of this circuit is presented on page 73 and a timing diagram is shown on page 75.

The function of a resync circuit is to synchronize an asynchronous signal of random length with the computer clock. Upon receipt of a logical "1" input signal, the resync circuit produces a "1" output during a clock phase. This output is 62.5 nanoseconds long and is not repeated, regardless of the duration of the input.

The delay time through the resync circuit is approximately 40 nanoseconds. The clock which drives the resync circuit must be phase-shifted so that the resync output coincides with the computer clock.

The average time required for resynchronization is 2 clock phase times, taking into account the 40-nanosecond circuit delay. It is possible, however, for this to occur during 1 phase time, and it never requires more than 3. A simplified timing diagram of the resync circuit is shown on page 75. The best case and worst case conditions refer to the length of time required for synchronization.

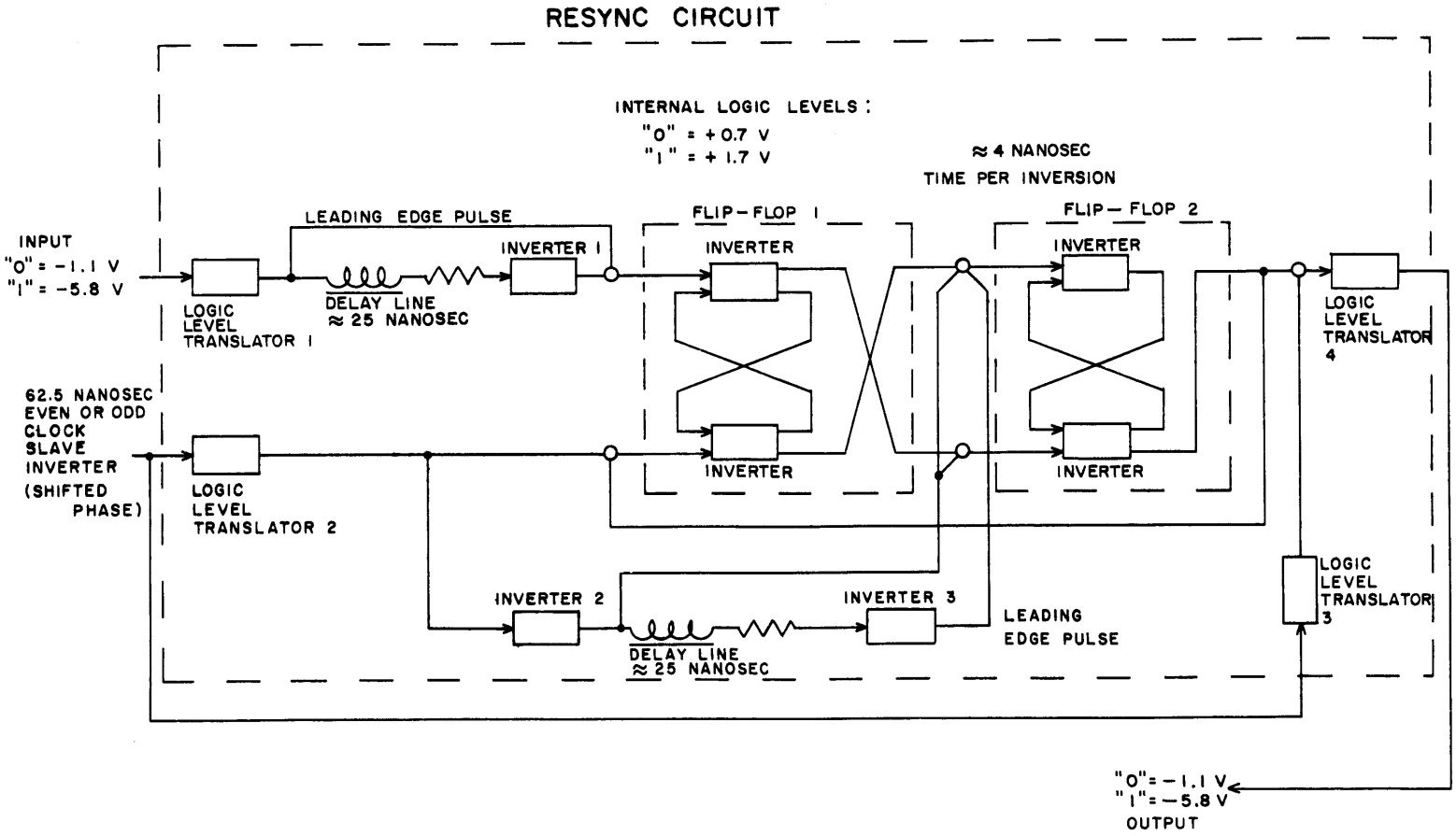
Logic levels within the resync circuit are in the positive voltage domain. A "0" is represented by +0.7v and a "1" by +1.7v.

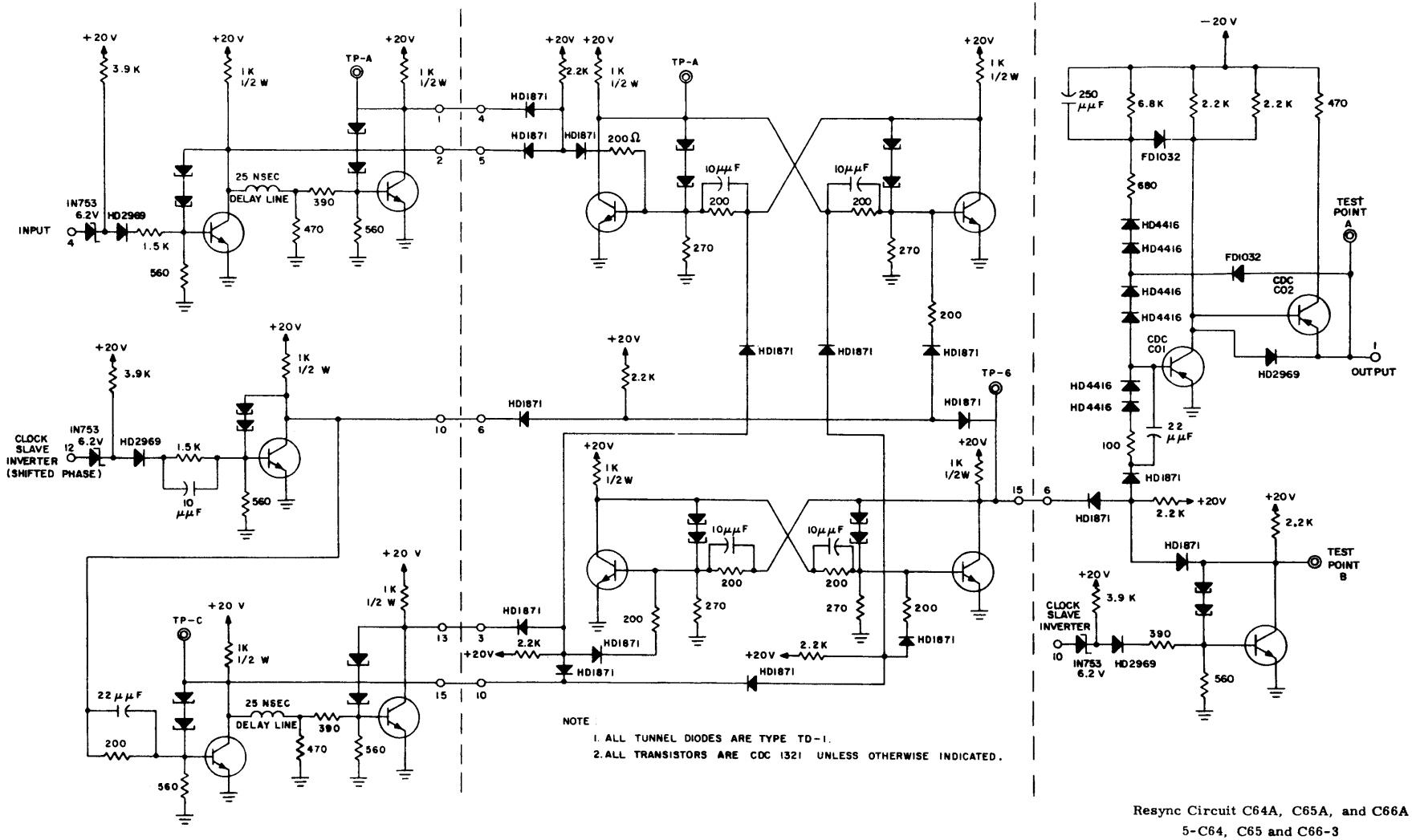
### LOGICAL FUNCTIONING

With initial conditions prevailing, the input to the circuit is a steady "0" and the output of inverter 1 is a steady "1". When a "1" input is received by the circuit, the delay line allows the output of inverter 1 to remain a "1" for approximately 25 nanoseconds. During this time FF 1 is set.

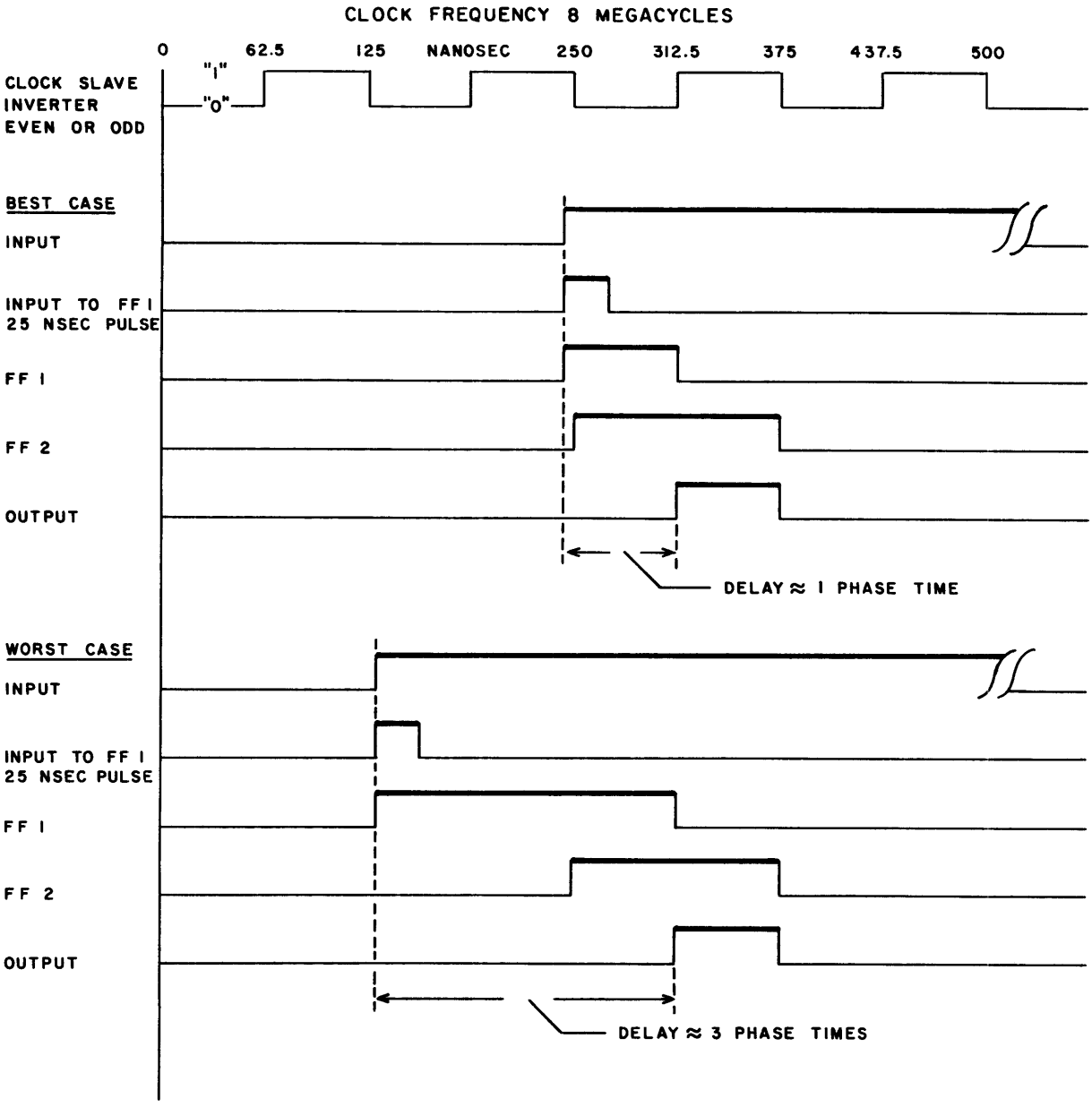
Next, FF 2 is set by the ANDed outputs of inverters 2 and 3. When the clock input goes to "0", the output of inverter 2 goes to "1". The delay line allows the output of inverter 3 to remain a "1" for 25 nanoseconds, setting FF 2.

With FF 2 set, the "1" is gated out of the circuit by a full 62.5 nanosecond clock phase, which also clears FF 1. Following this, the clock input clears FF 2, and initial conditions prevail.


RESYNC CIRCUIT
INTERNAL LOGIC LEVELS :
"0" = +0.7 V
"1" = +1.7 V
≈ 4 NANOSEC
TIME PER INVERSION
INPUT
"0" = -1.1 V
"1" = -5.8 V
LOGIC LEVEL TRANSLATOR 1
LEADING EDGE PULSE
DELAY LINE ≈ 25 NANOSEC
INVERTER 1
FLIP-FLOP 1
INVERTER
INVERTER
FLIP-FLOP 2
INVERTER
INVERTER
LOGIC LEVEL TRANSLATOR 4
62.5 NANOSEC EVEN OR ODD CLOCK SLAVE INVERTER (SHIFTED PHASE)
LOGIC LEVEL TRANSLATOR 2
INVERTER 2
DELAY LINE ≈ 25 NANOSEC
INVERTER 3
LEADING EDGE PULSE
LOGIC LEVEL TRANSLATOR 3
"0" = -1.1 V
"1" = -5.8 V
OUTPUT




Resync Circuit C64A, C65A, and C66A
5-C64, C65 and C66-3




NOTES:

1. BEST CASE — INPUT RECEIVED JUST BEFORE CLOCK PHASE GOES TO "0."
2. WORST CASE — INPUT RECEIVED JUST AFTER CLOCK PHASE GOES TO "0."

Resync Circuit Timing Diagram

CIRCUIT OPERATION

As shown on page 74, except for the transistors in the output logic level translator, all of the resync circuit transistors are CDC 1321. This is a high speed silicon NPN type, having a gain-bandwidth of 1 kmc, which provides a time per inversion of approximately 4 nanoseconds, as used in this circuit. All of the CDC 1321 transistors have a base-to-collector tunnel diode network. This network establishes an input threshold level and holds the output voltage at the sum of the tunnel diode drops and the base-emitter junction drop.

The tunnel diodes are type TD-1. This is an axial tunnel diode having an $I_p$ = 1 ma and a $V_{fp}$ = 500 mv. Assuming an ideal case, two tunnel diodes in series would switch at 1 ma with a composite $V_{fp}$ = 1v. Due to slight individual differences, no two tunnel diodes switch at exactly the same point, but the difference is negligible in this high speed circuit.

Logic level translators 1, 2, and 3 perform the function of changing a -5.8v "1" to a +1.7v "1", and a -1.1v "0" to a +0.7v "0". Upon receipt of a -1.1v "0" input, the tunnel diodes are back biased and they are in the low voltage state. Thus the collector potential is held at the potential of the base, which is approximately +0.7v, being a grounded emitter silicon transistor. However, upon receipt of a -5.8v "1" input, the 6.2v drop across the zener diode causes tunnel diode current to increase to approximately 1.2 ma, so they switch to the high voltage state. This causes transistor conduction to decrease, and the collector voltage becomes equal to the sum of the tunnel diode voltages and the base-emitter voltage, a total of +1.7v.

The inverter circuits change a +1.7v "1" input to a +0.7v "0" output, and vice versa. Again, the output levels are taken from the collector, and the collector potential is equal to the sum of the tunnel diode voltages plus the base-emitter voltage of the silicon transistor. The time required for a transition from one state to the other is approximately 4 nanoseconds.

As shown on page 74, the two flip-flops are each constructed of two inverter circuits provided with cross-coupled feedback from collector to base. These flip-flops are bistable circuits and are therefore capable of storing information.

The output logic level translator is quite similar to a logical inverter circuit, which is discussed elsewhere. This circuit converts a +0.7v "0" into a -1.1v "0", and a

+1.7v "1" into a -5.8v "1". It is capable of driving up to 8 logic cards, all of which may be either AND or OR, or any combination resulting in 8 loads total. The input to this translator consists of the set output of FF 2, ANDed with the output of logic level translator 3. This produces an output pulse width of 62.5 nanoseconds, since the input from the clock slave inverter is a -5.8v "1" for this length of time. There is a delay of approximately 40 nanoseconds from this input to the resync circuit output.

The grounded emitter transistor is a PNP type CDC C01. The base bias is such that a +0.7v "0" allows it to switch on, producing a -1.1v "0" output, while a +1.7v "1" input causes it to switch off, producing a -5.8v "1" output.

GROUND RULES

1. The clock slave inverter input to pin 12 of the C64 card and pin 10 of the C66 card should be phaseshifted so that the resync output coincides with the computer clock.
2. There is a delay of approximately 40 nanoseconds from the clock slave inverter input at pin 10 of the C66 card to the resync circuit output.
3. The resync circuit may drive 8 AND loads, 8 OR loads, or any combination up to 8 loads total.

## CAPACITIVE DELAY
### Card Types C67, K67, C68, C69, C70, C71, K71

FUNCTION

The function of a capacitive delay is to provide an interval of time delay between successive logical operations. This is done by regulating the length of time required for a logical "1" to pass through the delay circuit. The delay time for a logical "0" is approximately one-tenth of the delay time for a logical "1".

The circuits contained on card types C67, C68, C69, C70, and C71 provide delay times ranging from 20 nanoseconds to 40 ms, and are shown on pages 83 through 87. In addition, the delays on card types C68 and C69 may be varied through a range of approximately ±15 percent by means of the variable resistor R02.

OPERATION, Card Types C67, C71, and K71

A delay circuit configuration is shown on page 82 with typical waveforms. It consists of a capacitor from the signal line to ground, having a source of charging current through a series resistance with the voltage regulated by a 15v zener diode. The delay time from A to B is the time required to charge the capacitor to the input threshold level of inverter B when the output of inverter A switches to a -5.8v "1".

The charging voltage is stabilized at a constant 15 volts by a zener diode. The delay time is therefore proportional only to the RC time constant of the series resistance and the capacitance, and is not affected by small line voltage variations. On card types K67, C68, and C69, the series resistance is variable by means of a 2k potentiometer. This provides a close adjustment of the delay times through a range of approximately ±15%.

The AND input contains FD 1032 silicon diodes having a voltage drop of approximately 0.6v; thus point ① on page 82 is always 0.6v more negative than the logic-level input. The voltage across the capacitor is controlled by the level of the input signal. With a -1.1v "0" input, this voltage is approximately -1.7v. When the input from A switches to a -5.8v "1", the voltage at point ① approaches -6.4v in an exponential curve according to the rate at which charging current flows into the capacitor. At the threshold level of approximately -3v, inverter B switches state.

OPERATION, Card Types K67, C68, and C69

The circuit contained on these cards is designed to provide stable delay times of relatively long duration. It consists of a capacitive delay followed by a double inverting network such that the circuit does not produce an over-all logical inversion.

The circuit output characteristics are similar to those of a logic card, and it drives a maximum of 8 logic card loads. These may be 8 AND loads, 8 OR loads, or any combination up to 8 loads total.

As discussed in the previous section, the delay time is the time required to charge the capacitor to the threshold level of the following inverter when the circuit input switches to the -5.8v "1" level. The threshold level at which the inverter switches state is approximately -3v, but often varies slightly from card to card. From an examination of the exponential charge curve of the capacitor, it is seen that a small variation of the threshold level makes an appreciable difference in the delay time. This variation can be eliminated by always using the same inverter with a given capacitive delay. Mounting the inverter on the same card ensures that the capacitive delay always drives the same inverter and the threshold remains essentially constant.

As discussed previously, the input logic diodes are high speed devices having a voltage drop of approximately 0.6v. This holds the anode of zener diode CR05 at a potential 0.6v more negative than the logic-level input.

Zener diode CR05 functions as a threshold-setting device. The breakdown voltage of CR05 is approximately 4.9v; thus with its anode held at -6.4v by "1" inputs, CR05 applies approximately 1.3v of forward drive to the base of Q01. As the circuit input goes negative, conduction increases through CR05 and resistor R05. When current flow through R05 reaches approximately 0.36 ma, the negative-going input starts to draw turn-on current from transistor Q01. The input continues moving negative to the -5.8v "1" level, causing Q01 to conduct heavily.

A -1.1v "0" input holds the anode of CR05 at approximately -1.7v. In this state, CR05 does not have sufficient bias to hold it in the zener breakdown region. The base of Q01 is therefore held at a low positive voltage by resistors R05 and R06, and Q01 is cut off.

Base drive for transistor Q02 is taken from the collector of Q01. When -5.8v "1" inputs cause Q01 to conduct heavily, its collector holds the base of Q02 at approximately -0.5v, so that Q02 is in a state of minimum conduction. The collector voltage of Q02 is clamped

at approximately -6v by resistors R07, R08, and diode CR06.

The -6v level is applied to the base of Q03 and its emitter is isolated by CR07. Transistor Q03 is connected as an emitter follower, and in this state, it can supply OR current for 8 logic card loads.

A -1.1v "0" input causes Q01 to cut off and its collector voltage rises toward -20v, causing transistor Q02 to conduct heavily. The collector voltage of Q02 approaches -0.5v, and the circuit output becomes a logical "0". In this state, transistor Q03 is cut off and Q02 can supply AND current for 8 logic card loads.

Positive feedback is provided from the collector of Q02 to the base of Q01 by resistors R05, R06, and capacitor C09. This produces a regenerative effect which speeds the switching action.

OPERATION, Card Type C70C

This circuit is designed to provide an approximate linear delay, requiring 120 to 150 nanoseconds for the output to change from "0" to "1", and requiring 60 to 75 nanoseconds to change from "0" to the -3v threshold. The delay time from "1" to "0" is approximately one-tenth as long, or 10 to 15 nanoseconds.

With a -1.1v "0" input, the cathode of CR01 is near -1.3v. The two forward-drop diodes CR02 and CR04 hold the base of Q03 near ground. Transistor Q03 is connected as an emitter follower; thus the circuit output is equal to the base voltage less the base-emitter junction drop and in this state is approximately -0.8v.

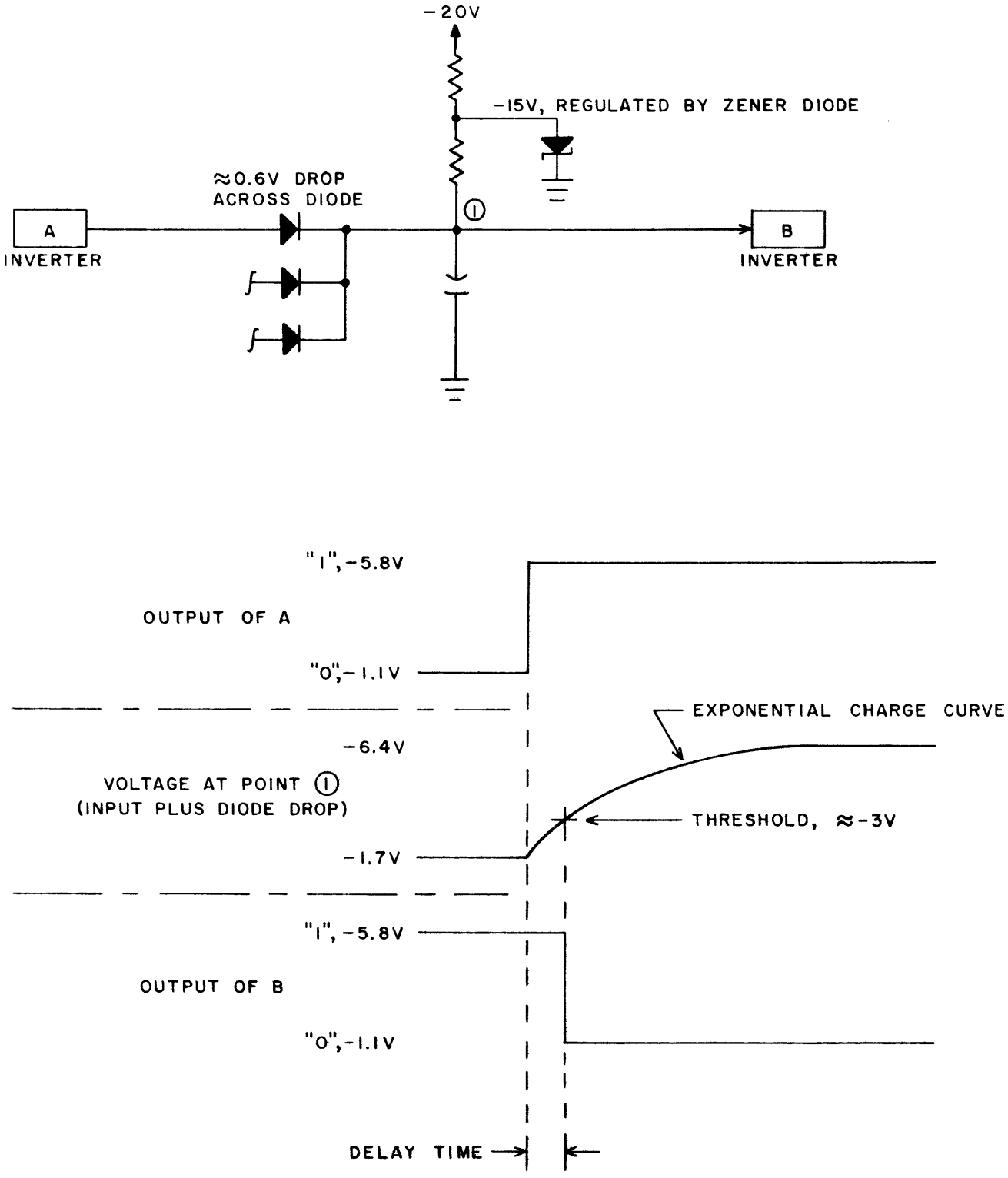
When the input switches to a -5.8v "1", capacitor C01 begins charging toward -6v. This causes conduction through Q01 to decrease so that the circuit output moves negative. However, the negative-going output is coupled back by the "bootstrap" connection of CR03, which is a 3v zener diode. This results in a nearly constant current of about 3.5 ma through resistor R02. Capacitor C03 is therefore charged at a nearly constant rate, resulting in a highly linear output.

GROUND RULES

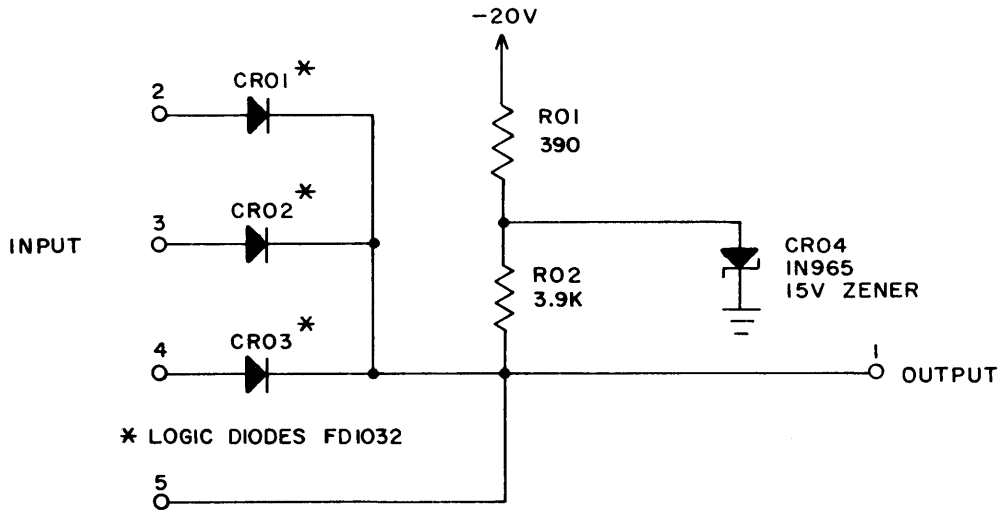
1. Each delay circuit contained on card types C67 and C71 may drive only one logic circuit.
2. The outputs of delay circuits contained on card types C67 and C71 must always connect to logic circuit OR inputs, while the circuit on Card Type K71

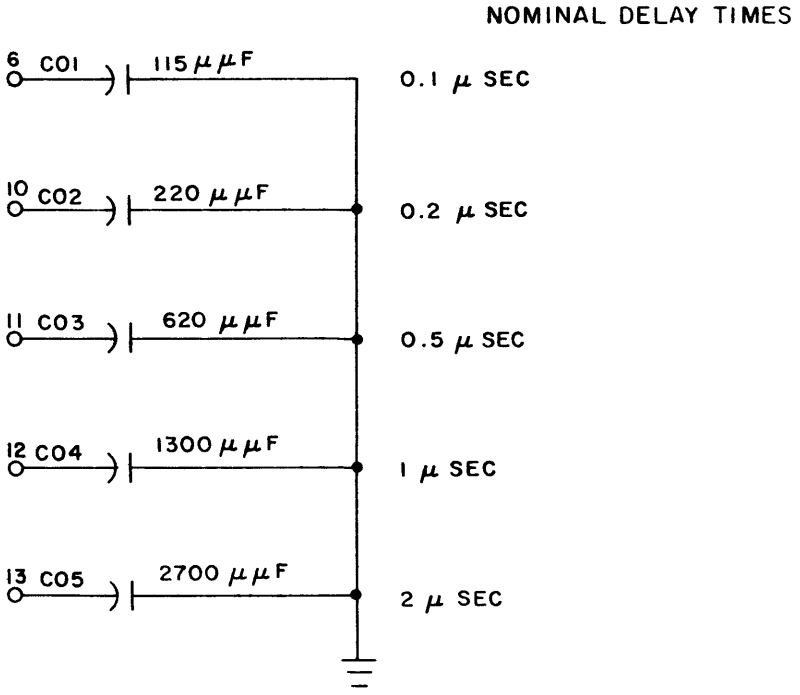
must drive AND inputs.

3. The delay circuits contained on card types K67, C68, and C69 may drive 8 AND loads, 8 OR loads, or any combination up to 8 loads total.
4. The nominal delay times pertain to a logical "1".
5. The delay time for a logical "0" is approximately one-tenth of the corresponding delay time for a logical "1".




Typical Circuit Configuration

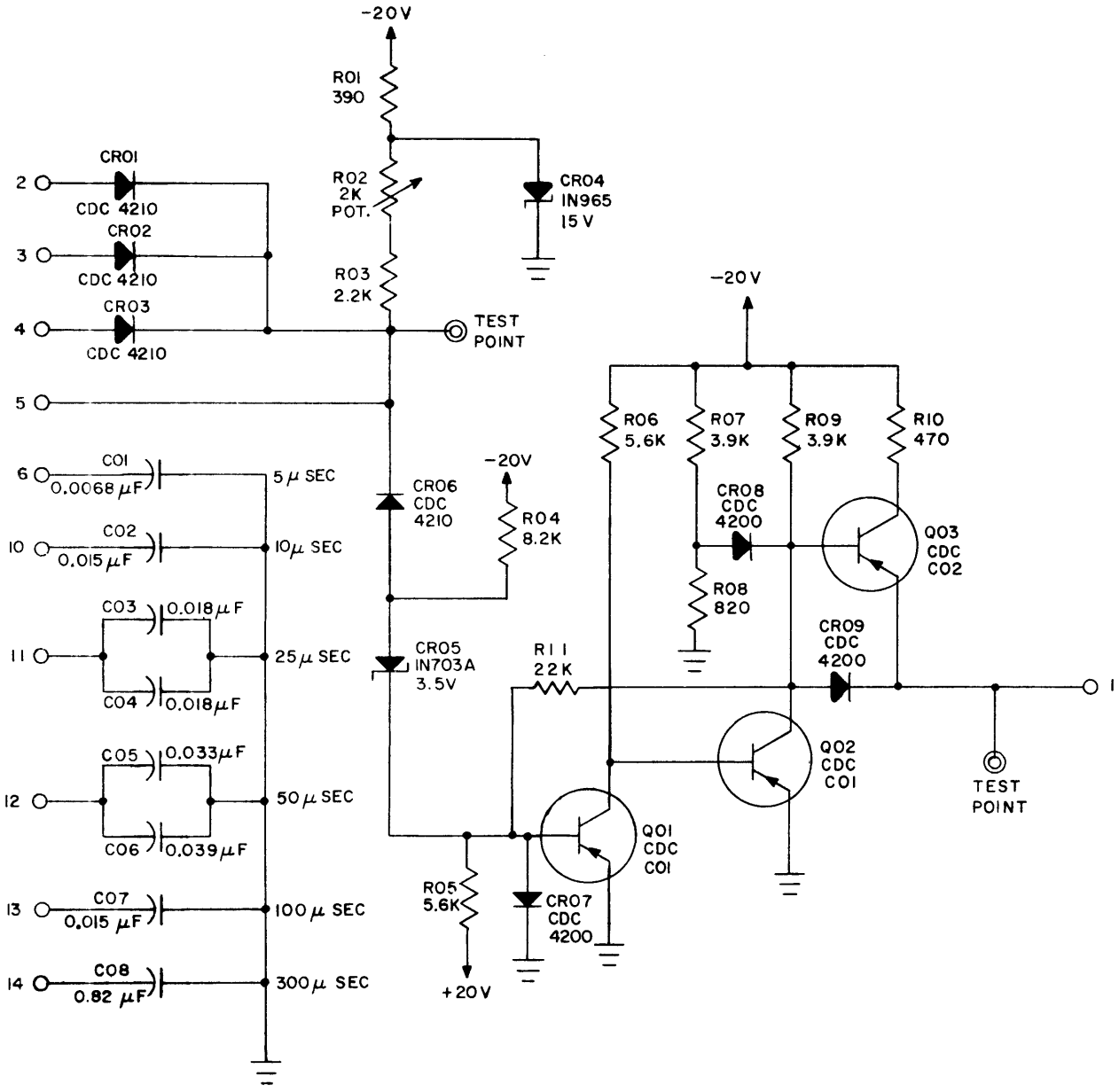



NOTE:

1. AN EXTERNAL JUMPER CONNECTS PIN 5 TO THE DESIRED DELAY.
2. CARD TYPE K67 GIVES SAME DELAY TIMES, BUT CIRCUIT IS SIMILAR TO C68 AND C69.

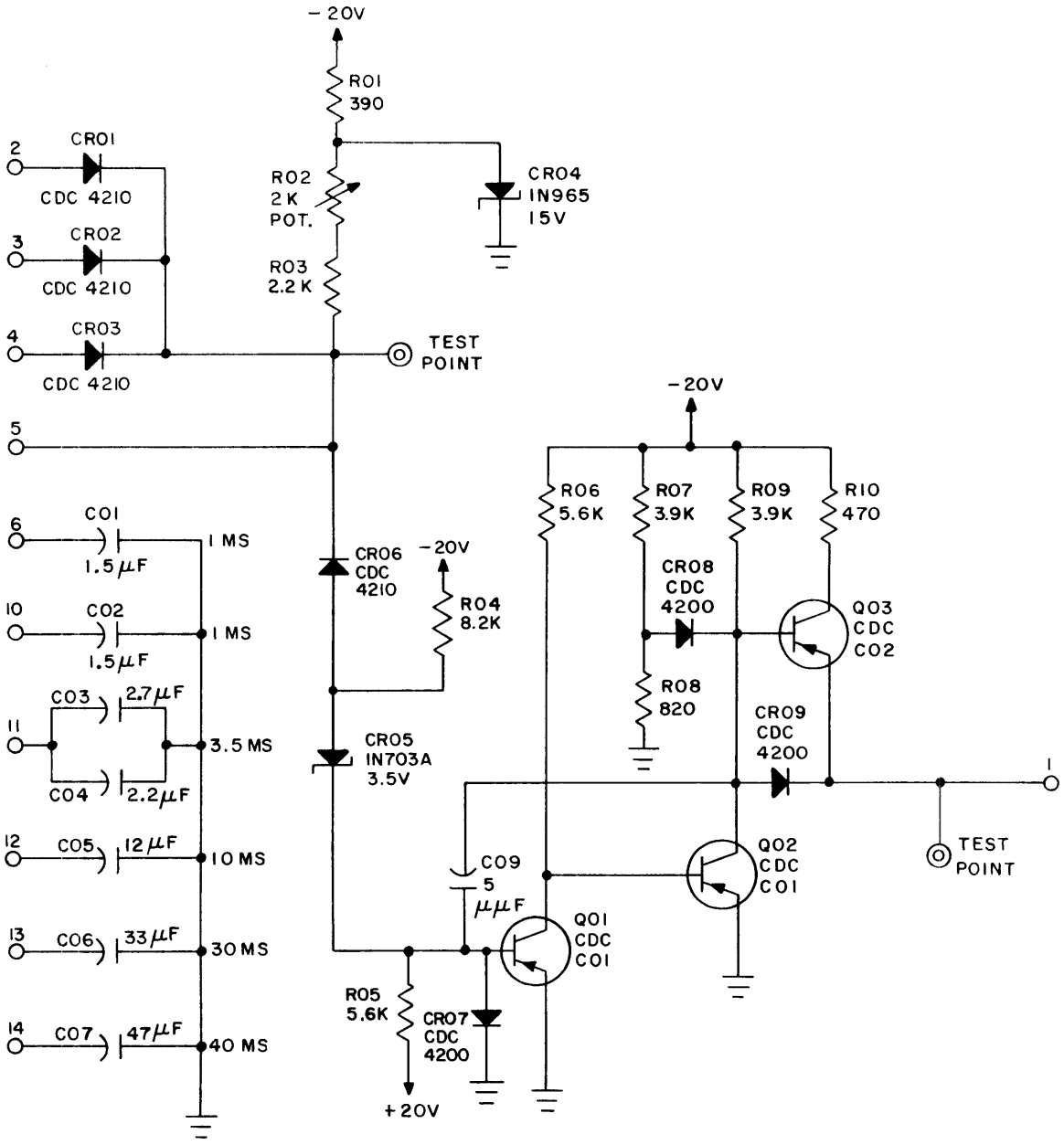
Capacitive Delay, Fixed C67




NOTES:

1. EXTERNAL JUMPER CONNECTS PIN 5 TO DESIRED DELAY.
2. NOMINAL DELAY TIMES VARIABLE ± 15% BY ADJUSTING R02.
3. THE CIRCUIT DOES NOT PRODUCE AN OVER-ALL INVERSION.

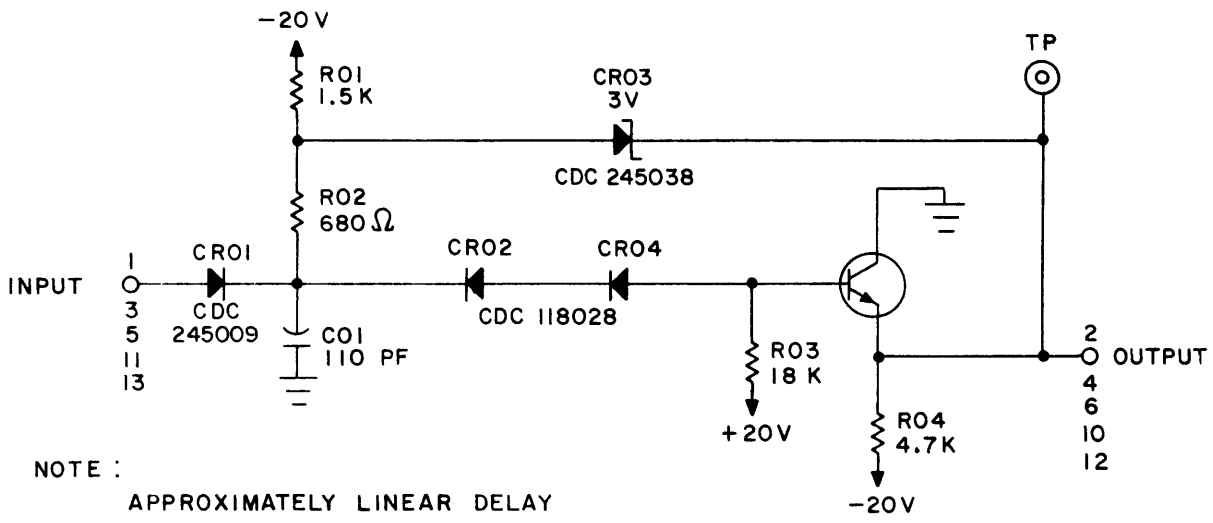
Capacitive Delay, Variable C68




NOTES:

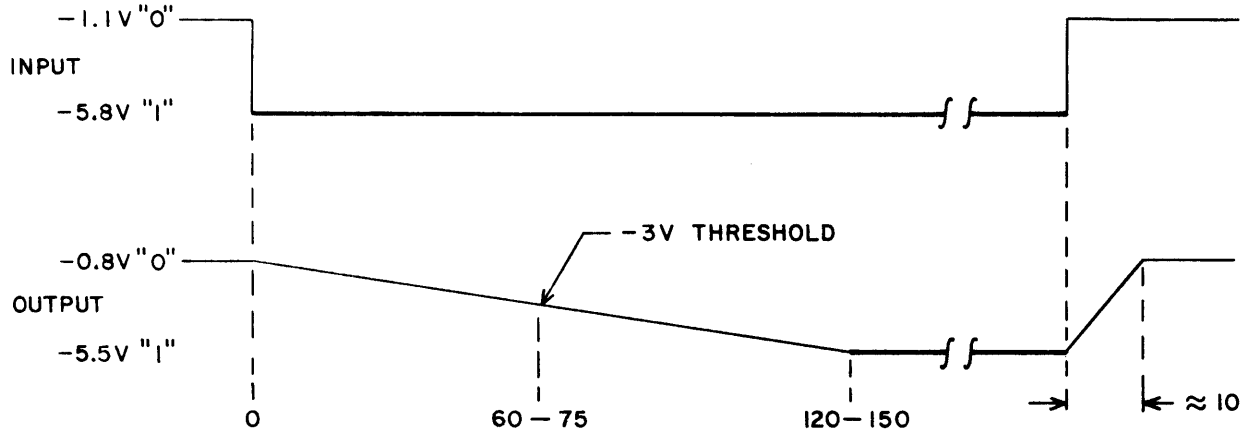
1. EXTERNAL JUMPER CONNECTS PIN 5 TO DESIRED DELAY.
2. NOMINAL DELAY TIMES VARIABLE ± 15 % BY ADJUSTING R02.
3. THE CIRCUIT DOES NOT PRODUCE AN OVER-ALL INVERSION.

Capacitive Delay, Variable C69




NOTE :

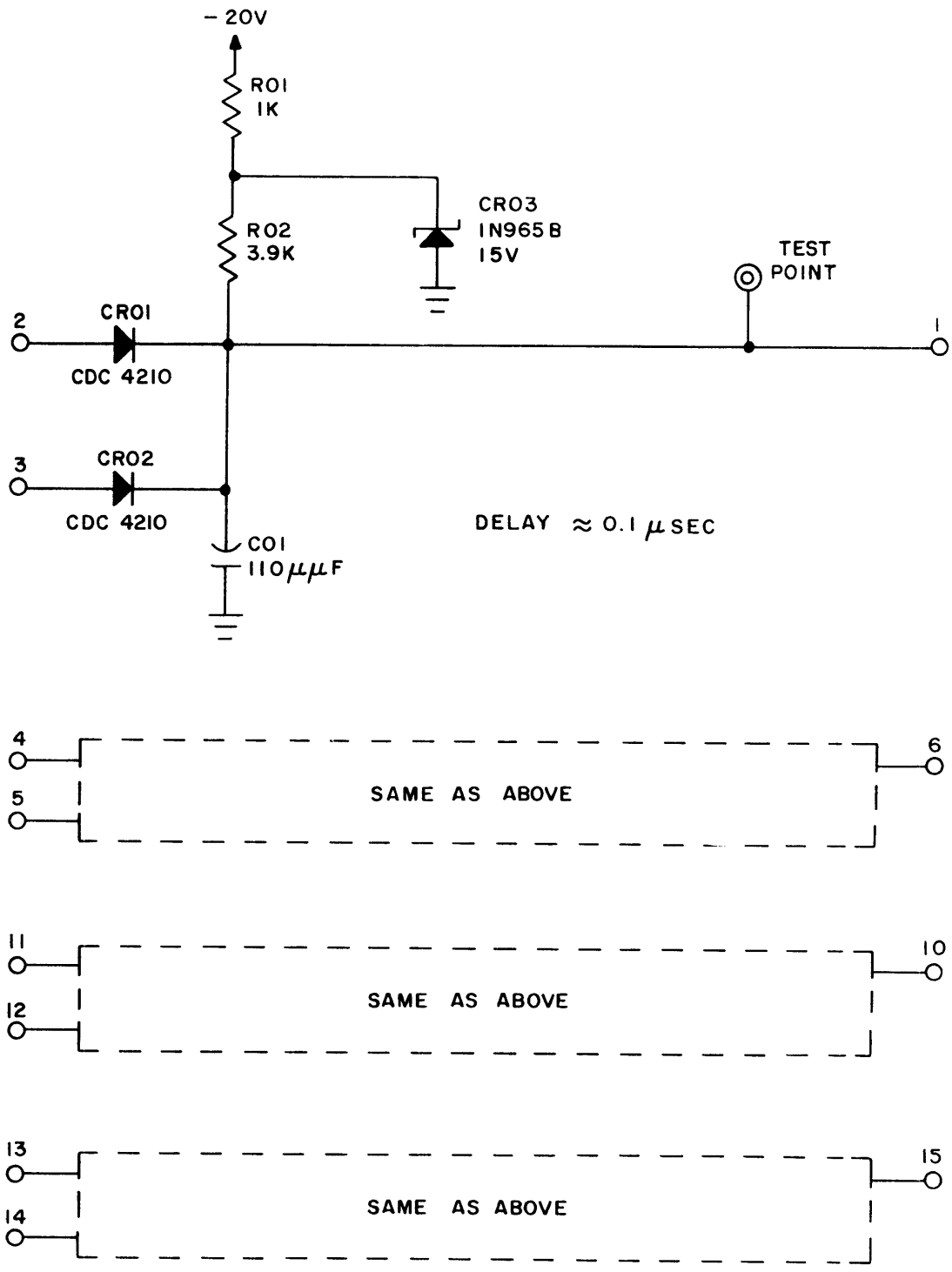
APPROXIMATELY LINEAR DELAY




NOTE :

ALL TIMES ARE IN NANOSECONDS.

Adder Network Delay C70C




Capacitive Delay, 0.1 usec C71

## PRIORITY CIRCUIT

Card Types C77, C78B, C79A

(See Pub No. 60042000 3609 Diagrams, drawing number 311518)

### GENERAL

The priority circuit shown on page 90 is contained on three printed circuit cards, the type numbers being C77, C78, and C79. The logical operation of this circuit is presented on page 89 and a timing diagram is shown on page 91.

The function of the priority circuit is to enable a storage module to honor its five access channels on a first-come, first-serve basis, without interference from any other access channel. Priority circuits are contained in the input logic of each of the five access channels, and when one of them receives a "1" input, it disables the priority circuits in the remaining four channels. Thus a request on any of the remaining channels is not honored until the first channel is released.

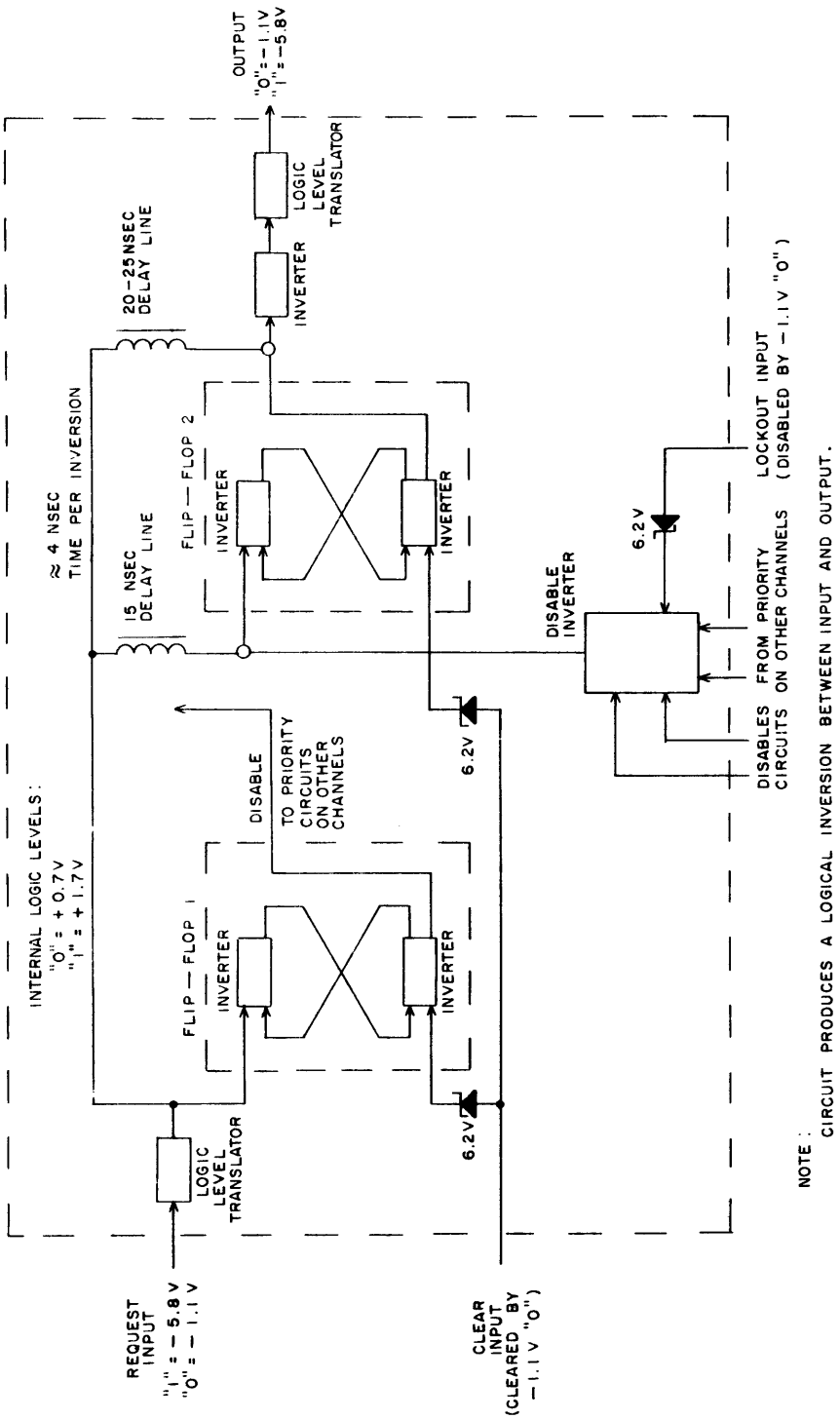
The priority circuits differentiate between access channel requests spaced down to approximately 7 to 8 nanoseconds. Requests arriving more closely than this are considered to have arrived simultaneously, and factors such as supply voltage and wire length determine which channel is honored. If two requests arrive simultaneously and all other factors are equal, then neither is honored.

With card type C79A, the delay time through a priority circuit is 30 to 40 nanoseconds. The 20-nanosecond delay line accounts for the majority of this, since the transistor and tunnel diode logic provides a time per inversion of approximately 3 to 4 nanoseconds. A priority circuit timing diagram is presented on page 91.

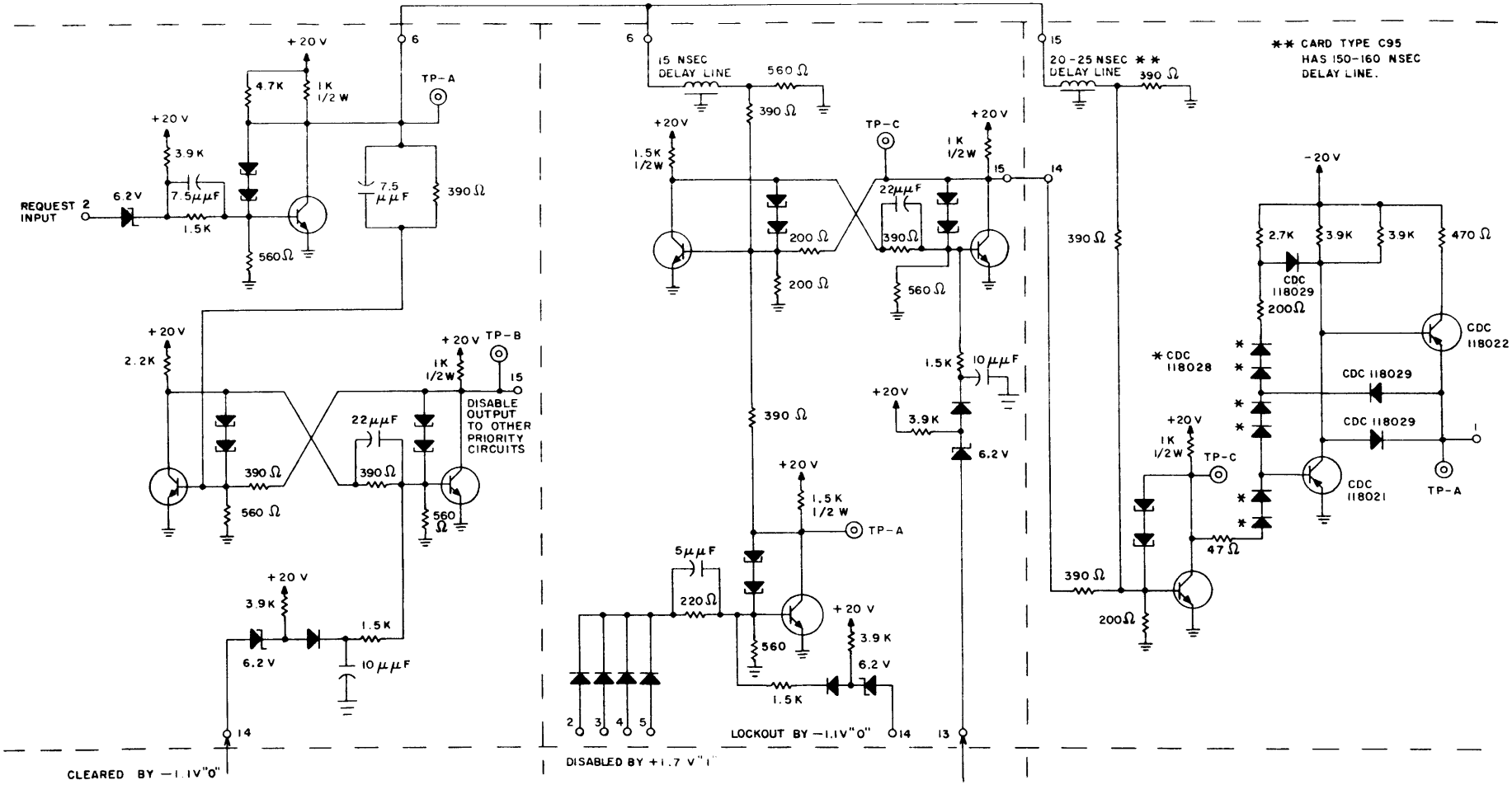
Logic levels within the priority circuit are in the positive voltage domain. A "0" is represented by +0.7v and a "1" by +1.7v. The disable signal sent from one priority circuit to the other four is the set output of FF1, and is a +1.7v "1".

NOTE

Card type C95 is similar to C79A, except that the delay line is 150-160 nanoseconds.



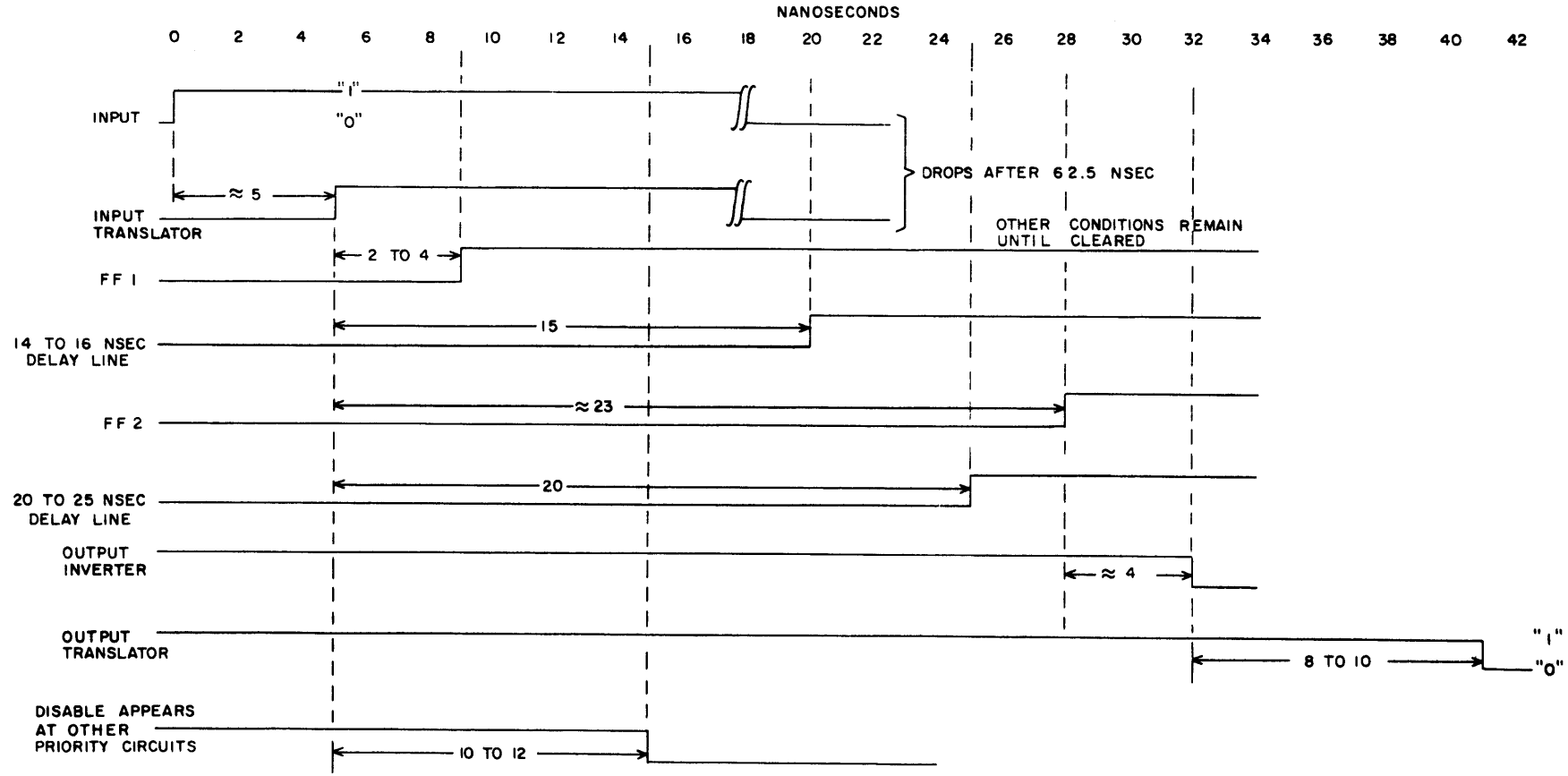

Priority Circuit




NOTES :

1. ALL TUNNEL DIODES ARE TYPE TD−1, CDC 245011.
2. ALL ZENER DIODES ARE TYPE 1N753, 6.2 V, CDC 245039.
3. ALL TRANSISTORS ARE CDC245010 UNLESS OTHERWISE INDICATED.
4. ALL DIODES ARE CDC 245009 UNLESS OTHERWISE INDICATED.

Priority Circuit C77B, C78B and C79A




NOTE: OVER—ALL INVERSION BETWEEN INPUT AND OUTPUT

Priority Circuit Timing Diagram

LOGICAL FUNCTIONING

As shown on page 89, the portions of the priority circuit are: an input logic level translator; flip-flop 1 which produces the signal disabling the other priority circuits; an inverter which disables flip-flop 2 if another access channel has priority; flip-flop 2; an output inverter; and an output logic level translator.

In addition, the priority circuit contains four 6.2v zener diodes, three of which function both as logic level translators and inverters. A -5.8v "1" input to a zener diode becomes a +0.4v output, and a -1.1v "0" input becomes a +5.1v output. These outputs act as "0" and "1", respectively, in the priority circuit logic. The remaining zener diode performs a level-shifting action in the input logic level translator.

A Request signal on an access channel results in a -5.8v "1" input, which is converted by the input logic level translator to a +1.7v "1". This sets FF1, which, in turn, disables the other priority circuits.

After a delay of 15 nanoseconds, the "1" reaches the AND into FF2. If a disable input is not being received, the output of the disable inverter is also a "1", so that FF2 is set. Then, after an additional 5-nanosecond delay, the "1" is ANDed with the set output of FF2 into the output inverter, where it becomes a +0.7v "0". This is converted by the output logic level translator to a -1.1v "0". The priority circuit therefore produces a logical inversion between input and output.

As soon as the access channel has been honored, the priority circuit is cleared by a -1.1v "0" input, which is converted by zener diodes to +5.1v, and is applied to the clear inputs of FF1 and FF2. This removes the disable from the other priority circuits so that a request on another channel may be honored.

CIRCUIT OPERATION

As shown on page 90 except for the transistors in the output logic level translator, all of the priority circuit transistors are CDC 245010. This is a high speed silicon NPN type, having a typical gain bandwidth of 1 kmc, which provides a time per inversion of approximately 2 to 4 nanoseconds, depending upon the loading.

All of the CDC 245010 transistors have a base-to-collector tunnel diode network. This establishes an input current threshold level and holds the output voltages at the sum of the tunnel diode drops and the base-emitter junction drop.

The tunnel diodes used are CDC 245011. This is an axial tunnel diode having an $I_p$ = 1 ma and a $V_{fp}$ = 500 mv. Assuming an ideal case, two tunnel diodes in series would switch at 1 ma with a composite $V_{fp}$ = 1v. Due to slight individual differences, no two tunnel diodes ever switch at exactly the same point, but the difference is negligible in this high speed circuit.

The input logic level translator performs the function of changing a -5.8v "1" into a +1.7v "1", and a -1.1v "0" to a +0.7v "0". Upon receipt of a -1.1v "0" input, the tunnel diodes are back biased and they are in the low voltage state. Thus the collector potential is held at the potential of the base, which is approximately +0.7v, being a grounded emitter silicon transistor. However, a -5.8v "1" input causes tunnel diode current to increase to a value in excess of 1 ma, so that they switch to the high voltage state. This causes transistor conduction to decrease, and the collector voltage becomes equal to the sum of the tunnel diode voltages and the base-emitter voltage, a total of +1.7v.

The disable inverter and the output inverter circuits are for changing a +1.7v "1" to a +0.7v "0", and vice versa. In addition, the disable inverter also changes the +5.1v signal received through the zener diode to a +0.7v "0". Again, the output levels are taken from the collector, and the collector potential equals the sum of the tunnel diode voltages plus the base-emitter voltage of the silicon transistor. The time required for a transition from one state to the other is approximately 4 nanoseconds.

The amount of speed-up capacitance used on inverters of this type is dependent upon the particular input. A single OR input may have a fairly large speed-up capacitor; however, the speed-up capacitance on the OR inputs to the disable inverter must be kept small. This is because FF 1 on each priority circuit must drive four disable inverter inputs and is loaded too heavily if too much speed-up capacitance is used. Also, the speed-up capacitance on AND inputs must be small in order to prevent runt pulses and partial enables from satisfying the AND.

As shown on page 90, the two flip-flops are each constructed of two inverter circuits provided with cross-coupled feedback from collector to base. These flip-flops are bi-stable circuits and are therefore capable of storing information.

The output logic level translator is quite similar to a logical inverter circuit, which is

discussed elsewhere. This circuit converts a +0.7v "0" to a -1.1v "0", and a +1.7v "1" to a -5.8v "1". It is capable of driving up to 8 logic cards, all of which may be either AND or OR, or any combination resulting in 8 loads total. The grounded emitter transistor is a PNP type CDC118021.The base bias is such that a +0.7v input allows it to switch on, producing a -1.1v "0" output, while a +1.7v input causes it to switch off, producing a -5.8v "1" output.

GROUND RULES

1. The priority circuit may drive 8 AND loads, 8 OR loads, or any combination up to 8 loads total.
2. Lead length from FF 1 to the disable inverters on the other priority circuits must be less than 5 inches.
3. Only one priority circuit may be cleared by any one inverter, because a priority circuit requires approximately 15 ma of current for clearing.
4. One inverter may drive the lockout inputs of 4 priority circuits, because a lockout input requires approximately 4 ma.

## STROBE SHAPER
### Card Type C85

FUNCTION

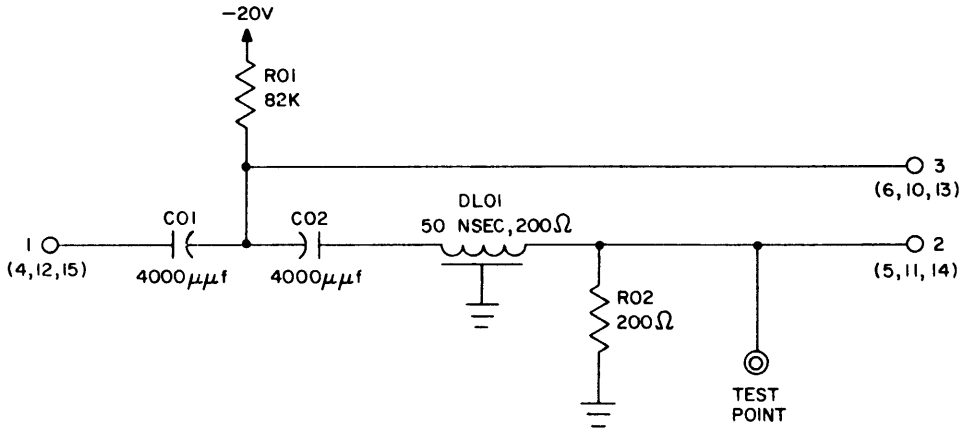
This circuit operates with a Receiver circuit contained on card type C61. Their function is to convert a delay line output (received via an Emitter Follower circuit on card type C07) into a -1.1v "0" pulse 50 nanoseconds in length.

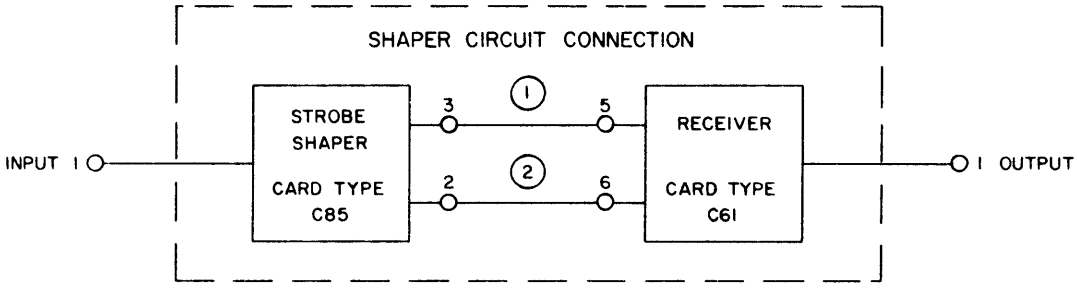
OPERATION

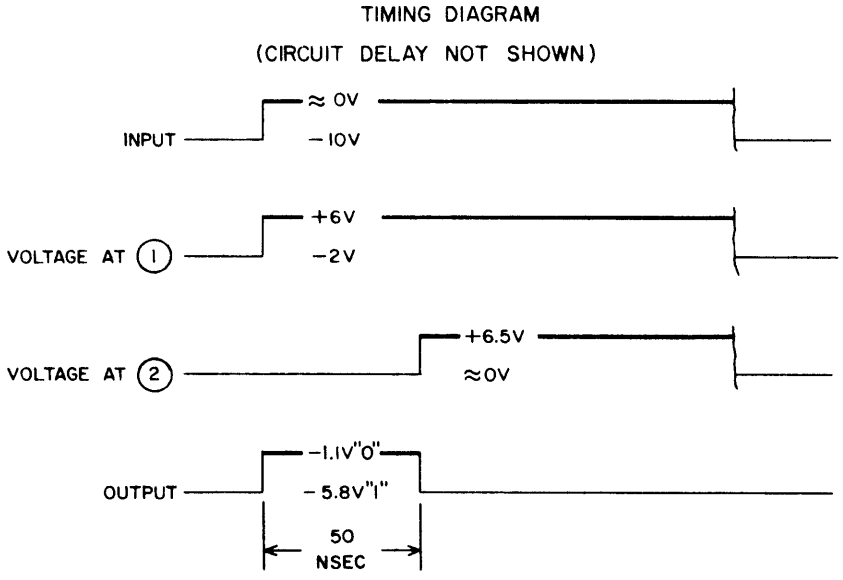
As shown on the accompanying diagram, the input from the Emitter Follower circuit is a positive-going pulse with a swing from -10v to ground, approximately. This input is received by the Strobe Shaper circuit and immediately appears on one of the outputs, causing the Receiver output to switch to -1.1v "0". After a delay of 50 nanoseconds, the input signal appears on the other output, causing the Receiver output to return to -5.8v "1". When the input signal drops, the bias from -20v through R01 holds the Receiver output at -5.8v "1".

Capacitors C01 and C02 isolate the input and the delay line output from the -20v bias voltage. The d-c levels of the input and output are approximately the values shown in the timing diagram.

The delay line is 50 nanoseconds, with a 200-ohm characteristic impedance. The 200 ohm resistor R02 provides impedance matching between the delay line and the Receiver input.




Strobe Shaper C85
(Four Circuits per card)

## OVERLOAD PROTECTOR
Card Type C94

### FUNCTION
This circuit provides protection from excessive current flow in the memory drive lines (labeled X and Y in the 3600 system). In addition, it monitors the drive and inhibit voltages and disables the logic if any of these voltages fall below operating level. As shown in the accompanying diagram, the circuit contained on card type C94 operates in conjunction with other power supply components which are mounted elsewhere. The memory drive power supply system is disconnected if the type C94 card is removed from its connector.

Typical external connections to a C94 card are shown on page 99. For the actual wiring of the Overload Protector circuit in the 3609 Storage Module, see the 3609 Diagrams manual, Pub. No. 60042000.

### OPERATION, Over-Current Protectors
The card contains two identical circuits for dropping power if a current overload occurs in the X or Y drive scheme. This is shown with the principal current paths indicated by heavy lines. Normal current flow to the X or Y gate circuits is of the order of 900 ma. If this should increase to approximately 1.4 amperes, the voltage drop across the 18-ohm resistor causes the transistor to switch to its conduction state, firing the silicon controlled rectifier.

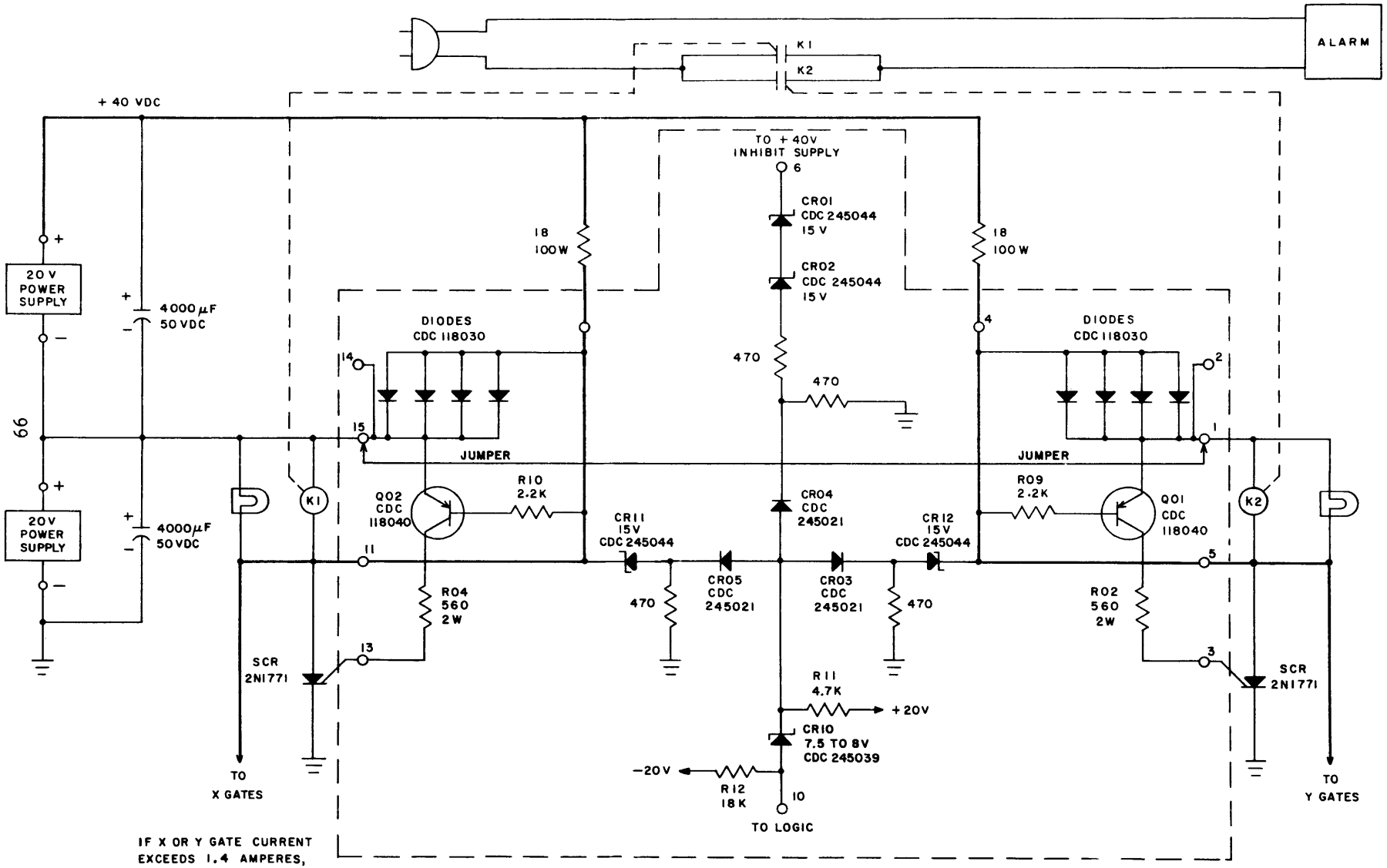
During normal operation, the rank of four CDC 118030 diodes are in a state of heavy forward conduction and the drop across the 18-ohm resistor is very close to 19.3v. The output supplied to the gate circuits is the voltage at the anodes of the diodes and is around 20.7 volts (20v plus 0.7v forward diode drop). A heavier output current results in a greater drop across the 18-ohm resistor, and when the current reaches approximately 1.4 amperes, the diodes cut off. A further increase in current draws turn-on current through the transistor causing it to switch on, which fires the silicon controlled rectifier (SCR).

As shown in the diagram, the SCR in its high conduction state grounds the output to the gate circuits, lights an indicator, and closes a relay to sound an alarm. The SCR may be returned to its OFF state by lowering the power supply voltages to zero.

OPERATION, Voltage Monitor

This portion of the circuit monitors the +20v gate supplies and the +40v inhibit supply. If these three voltages are present, a "0" output of approximately -0.7v appears at pin 10. If the inhibit supply falls below +30v, or if either gate supply falls below +15v, this output switches to a "1" of approximately -6.5v, disabling the operation of the memory logic.

A 3-way AND connection is provided by diodes CR03, CR04, and CR05, so that a low input voltage to any diode results in a "1" output. A level-shifting action is provided by the zener diode CR10. This diode is back biased sufficiently so that the voltage across it is a constant 7.5 to 8v.




IF X OR Y GATE CURRENT EXCEEDS 1.4 AMPERES, SCR FIRES.
(CURRENT PATHS SHOWN BY HEAVY LINES.)

"0" IF VOLTAGES ARE PRESENT.
"1" IF X OR Y GATE SUPPLY DROPS BELOW +15V OR INHIBIT SUPPLY DROPS BELOW + 30V.

Overload Protector C94

## CONSOLE INTERFACE
### Card Type HA10A

FUNCTION

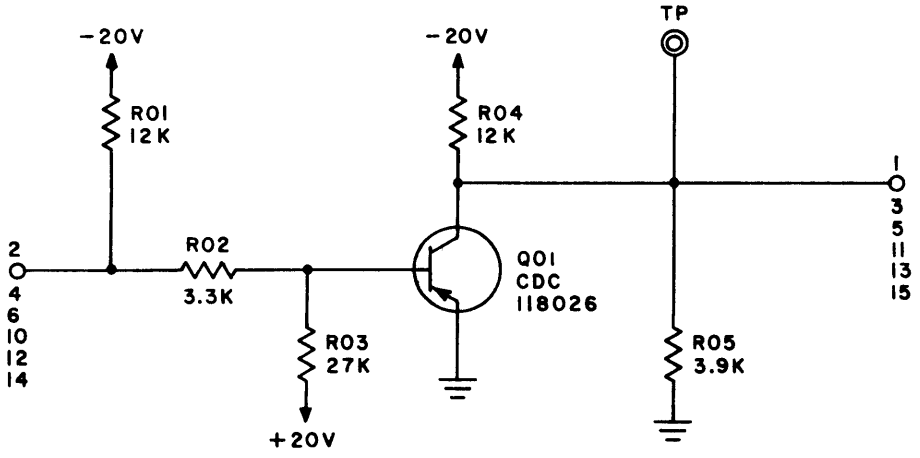
This circuit converts the signals received from either logical inverters or manual switches into outputs suitable for driving a high-current load such as a 5v light. This circuit can also function as a logical inverter since its output voltages are approximately those required for "1's" and "0's".

OPERATION

Transistor Q01 is capable of handling a current of the order of 200 ma. A -5.8 v "1" (or open) input causes Q01 to conduct, while a -1.1 v "0" (or ground) input causes Q01 to cut off.

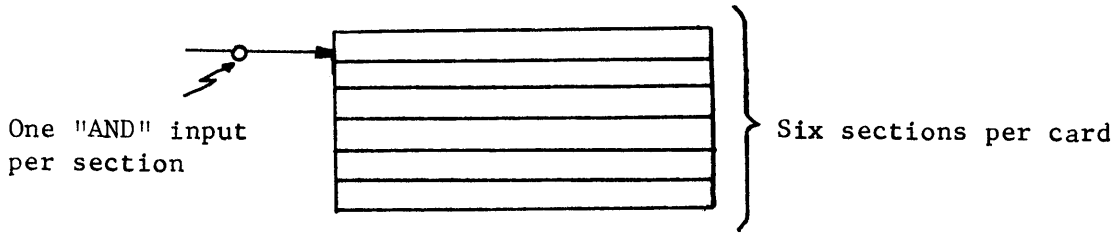
A -1.1 v "0" or ground input allows the +20 v through resistor R03 to reverse-bias the emitter-base junction of Q01, so that Q01 is cut off. In this state, the test point voltage will be approximately -5.6 v. This is produced by the voltage divider action of R04 and R05.

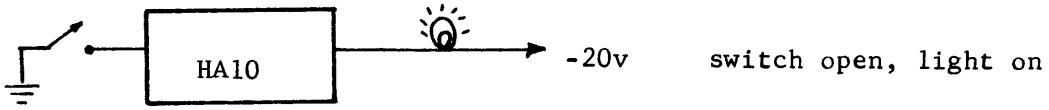
A -5.8 v "1" or an open input will cause Q01 to switch on and conduct heavily. A negative-going input causes current flow to increase through R02. Initially this current is supplied by the +20 v source through R03, however the voltage drop across R03 is limited by the base-emitter junction drop of Q01. A further increase in current flow will draw turn-on current through Q01, causing it to switch to its conduction state.

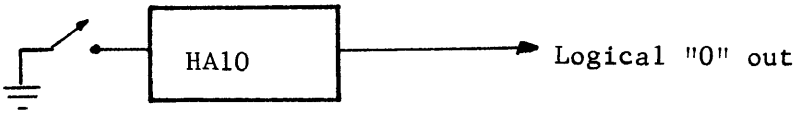


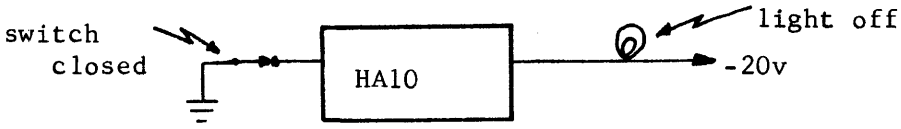

NOTE: SIX CIRCUITS PER CARD.

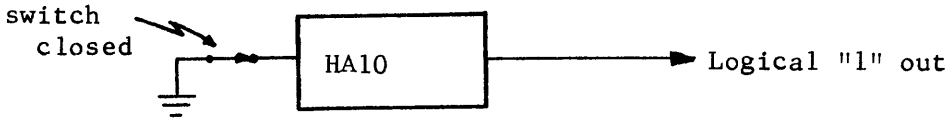
Here are four possible conditions of the Console Interface (HA10) card.




NOTE: When switch is closed we have ⏚ input which is effectively a logical "0" input.

When switch is open we have an effective logical "1" input.

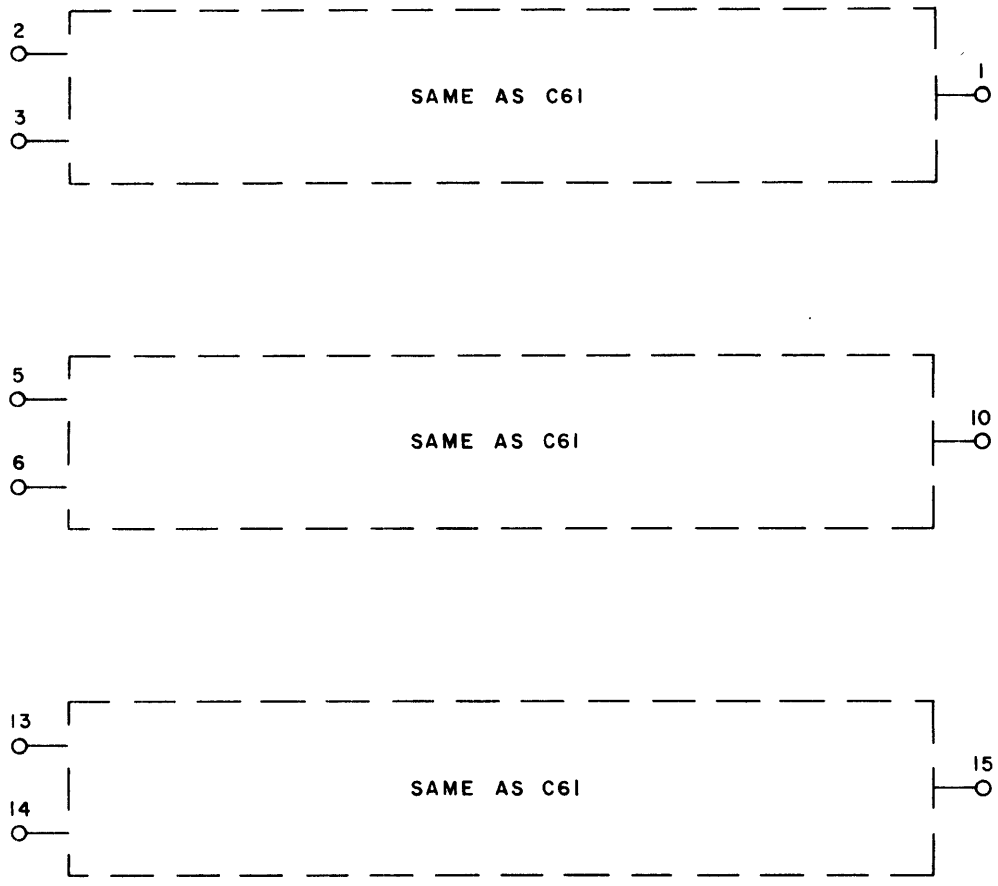
## RECEIVER
## Card Type HA11A

This card contains three receiver circuits, having the pin connections shown in the accompanying diagram. The circuits operate the same as card type C61, which is discussed elsewhere.

The circuit functions as both a differential amplifier and a discriminator. It provides a logic output of either a -5.8 v "1" or a -1.1 v "0", according to the polarity of the differential 0.5 v signal which the two input terminals receive from the transmission line.

The transmission line is balanced, terminated, twisted-pair, and the signals are centered about ground. As an example, if pin 2 goes to +0.25 v and pin 3 goes to -0.25 v, pin 1 will go to -1.1 v "0". If the inputs are reversed, the output will be -5.8 v "1".

The receiver circuit will drive 8 loads, and the ground rules are the same as for card type C61.




NOTES: 1. CIRCUITS OPERATE SAME AS C61.
2. 3 RECEIVER CIRCUITS PER CARD.

Receiver HA11A

## DELAY LINE AMPLIFIER
### Card Type HA12

FUNCTION

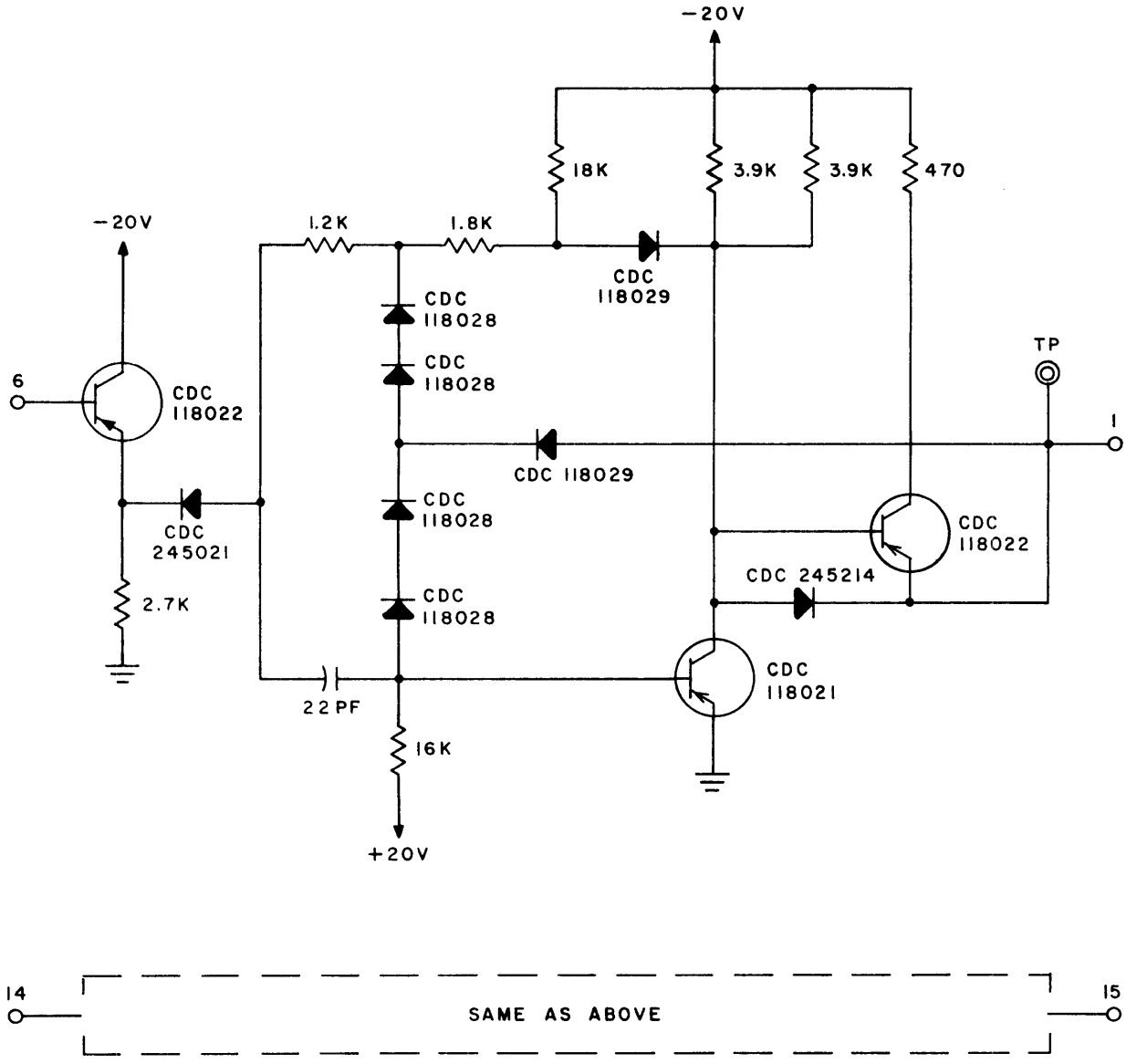
The function of this circuit is to convert inputs received from a terminated, 200-ohm delay line into logic outputs. The circuit provides a high-impedance load for the delay line, avoiding excessive current drain. The circuit output is a -1.1 v "0" which goes to -5.8 v "1" upon receipt of a positive-going pulse from the delay line. It is capable of driving eight loads, and its output characteristics are identical to a logical inverter.

OPERATION

The circuit consists of an emitter follower feeding an inverter through an OR diode. Inputs are received by tapping from the delay line. The quiescent value of the input signal is about -10 v, with pulses going to ground.

The input transistor is an emitter follower current amplifier, which provides a high impedance load with little current drain for the delay line. It is coupled directly into the inverter by means of an OR diode. With a -10 v input, the emitter of the input transistor is held at approximately -9.3 v. This holds the output of the inverter at -1.1 v "0". A positive-going input is effectively the same as a logical "0" and will cause the inverter to have a -5.8 v "1" output.

The inverter portion of the circuit is similar to a logical inverter, which is discussed elsewhere.




Delay Line Amplifier HA12

## DIGIT DRIVER
### Card Type HA14

FUNCTION

The function of this circuit is to provide bi-directional 400 ma drive currents through a digit winding in a word organized memory. The two ends of the winding connect to pins 14 and 15. Pin 13 connects through a power resistor to +20 v.

The circuits are activated by -1.1v "0" inputs. Each circuit has a 2-way AND input and pin 12 acts as a gate. The receipt of -1.1 v "0" inputs at pins 10 and 12 will cause pin 15 to go positive and 14 to go negative; with "0" inputs at pins 11 and 12, pin 14 will go positive and 15 will go negative.

OPERATION

The filter network consisting of L01, L02, and C04-C08 performs a decoupling function. The current carried by pins 14 and 15 is of the order of 400 ma. The decoupling network prevents voltage surges and fluctuations on the circuit input which could result from heavy current switching at the output.

The two input circuits are identical, as shown in the accompanying diagram. The components mentioned here are those associated with test point A.

The input of each circuit is a 2-way AND, and -1.1 v "0" inputs allow transistor Q01 to conduct. A level-shifting action is provided by the 4.1 v zener diode CR05. A -5.8 v "1" input at either pin 10 or 12 will result in approximately -1.2 v at the base of Q01, so that Q01 is cut off. With both inputs at the -1.1 v "0" level, zener diode CR05 will bias the base of Q01 well into the conduction region.

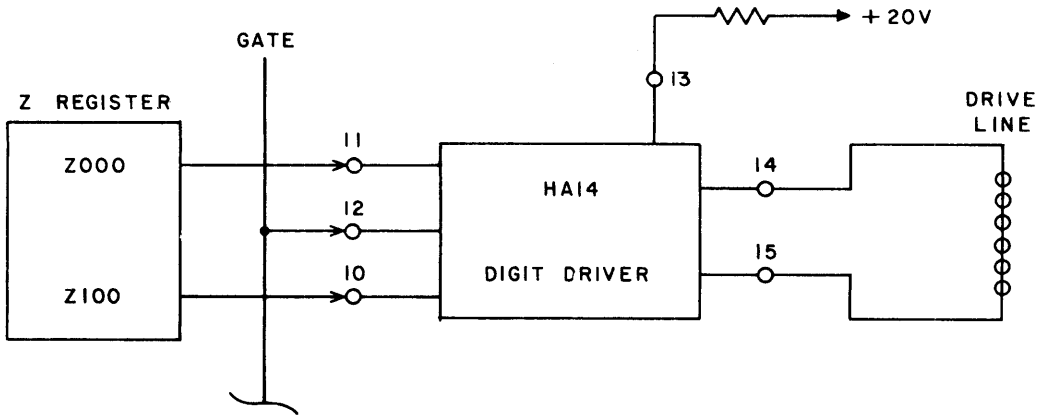
Transistor Q01 in its conduction state allows current flow to increase through the primary winding of transformer T1. In this state, current through the 16-turn primary of T1 will be approximately 2 ma. This results in about 8 ma in each of the 4-turn secondaries and provides forward drive current for Q03 and Q06, causing them to switch.

Transistors Q03 and Q06 in their conduction state cause pin 15 to go positive and 14 to go negative. The 100-ohm resistor R15 provides a blocking action, causing practically all of the current from Q03 to flow out of pin 15, through the 2-ohm drive line resistance, back into pin 14, and through Q06 to -20 v.

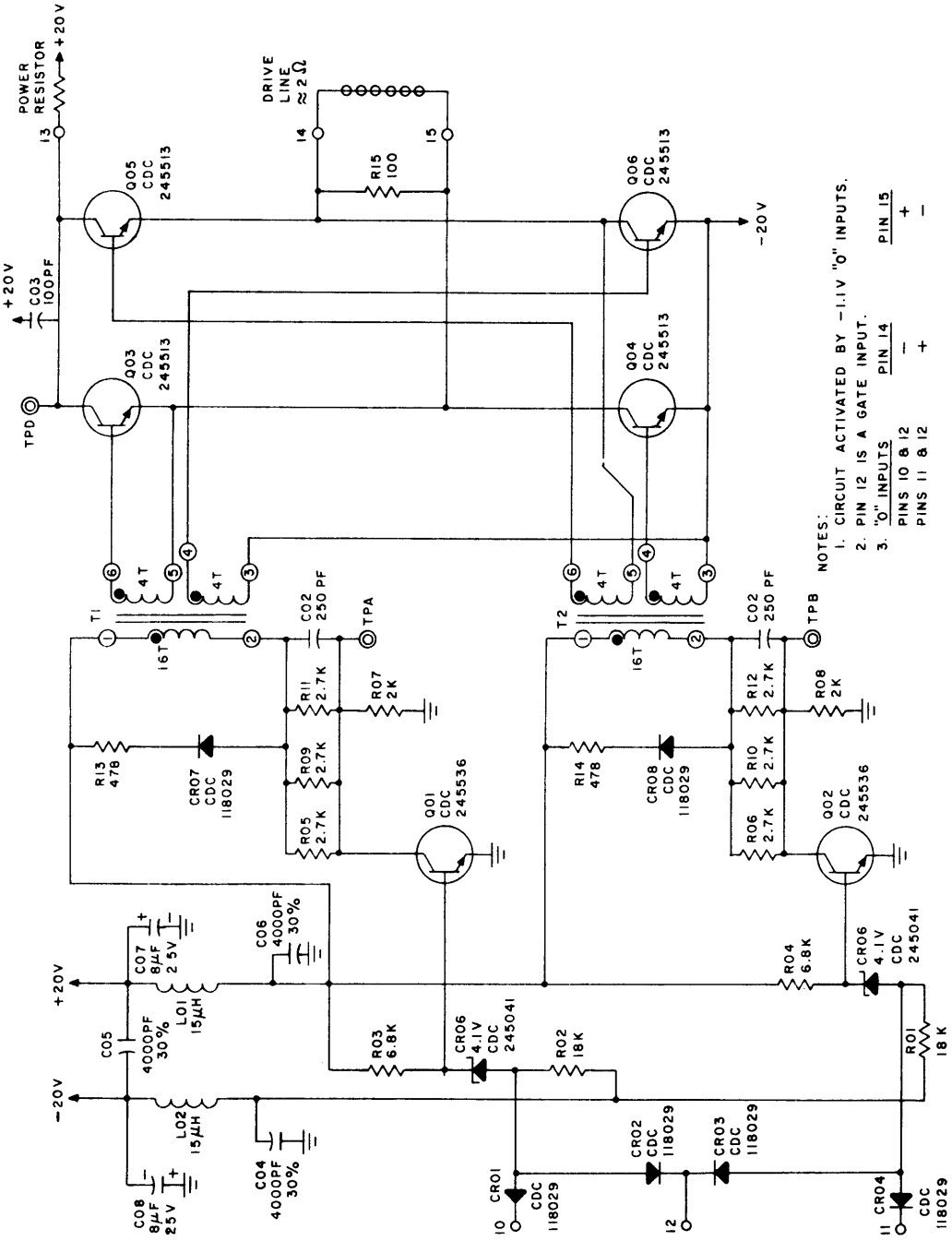
(Note that with "0" inputs at pins 11 and 12, transistors Q04 and Q05 will conduct producing an output current of the opposite polarity.)

Capacitor C03 performs a speed-up function, providing an initial surge of high current when the transistors switch on. This gives a sharper leading edge to the output waveform.

The connection of R13 and CR07 provides a clamp for the transformer primary This dissipates any inductive transient which could result when Q01 switches off.




TYPICAL APPLICATION




Digit Driver HA14

## DIGIT COMPENSATOR
### Card Type HA15

FUNCTION

This circuit operates in conjunction with the drive hardware of a word-organized memory. Its purpose is to provide a constant load for the -20v power supply by driving a 400 ma current through a load resistor during times when no drive lines are energized.

The load resistors are external to the circuits on the card and are connected in series from pins 1 and 15 to -20v. Current is allowed to flow whenever at least one of the inputs to the respective circuit is a -5.8v "1".

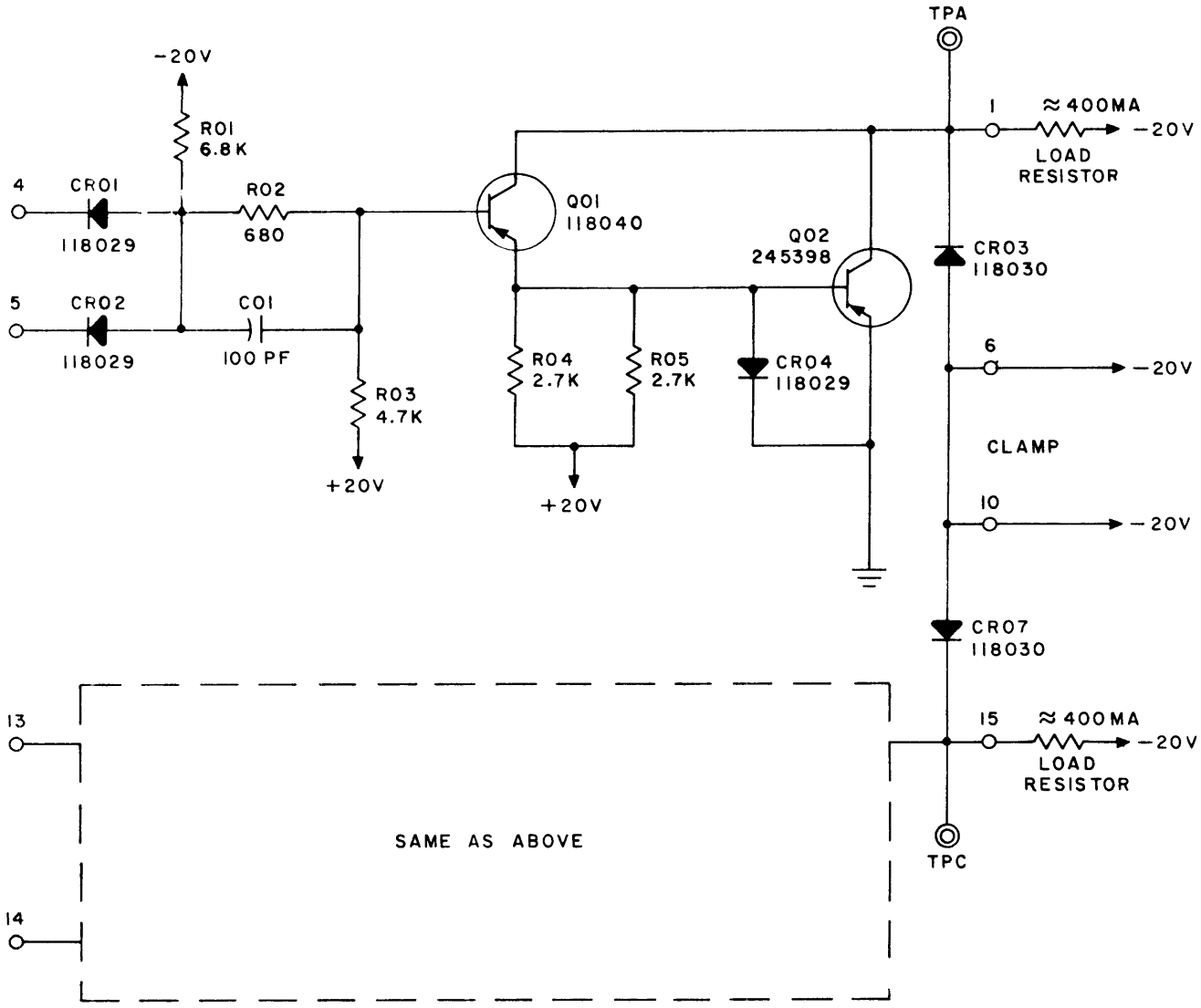
OPERATION

Each circuit has two OR inputs, and a -5.8v "1" on either input will cause the circuit to conduct. If both inputs are left open, the base of Q01 will rise toward approximately +4.5v and the circuit will be cut off.

A -1.1v "0" on both input will hold the circuit in the OFF state. This results in approximately +2v at the base of Q01. The emitter of Q01 and the base of Q02 are held at +0.5v by the forward drop across CR04, so that both transistors are cut off.

A -5.8v "1" on either input holds the base of Q01 at approximately -2v. The base drive for Q02 is taken from the emitter of Q01. A negative-going input to Q01 causes it emitter current to increase. Initially, this current is supplied from the +20v source through R04 and R05. However, the voltage drop across R04 and R05 is clamped at about 0.3v by the base-emitter junction drop of Q02. Resistors R04 and R05 are therefore able to supply only about 0.22 ma, and a further increase in the emitter current of Q01 will draw drive current through Q02, causing it to switch to its conduction state.

Diodes CR03 and CR07 provide clamps for the collector voltage of the transistors. This clamp connection should be used when driving an inductive load.




NOTES: 1. EACH CIRCUIT HAS TWO "OR" INPUTS.
2. TRANSISTORS CONDUCT WHEN EITHER INPUT RECEIVES A −5.8V "1".

Digit Compensator HA15

## SENSE AMPLIFIER
### Card Type HA16

FUNCTION

This card is designed for use as a sense amplifier in a word-organized memory. It consists of a differential amplifier driving a discriminator with a strobe input. Pins 4 and 5 connect to the two ends of the sense line, pin 15 provides the output, and pin 12 is the input for the -1.1v "0" strobe pulse. In the quiescent state, the output at pin 15 is about +0.3v which is interpreted as a logical "0".

The polarity of the differential 0.1 v input signal determines whether the output at pin 15 will be "1" or "0". If pin 4 goes positive with respect to pin 5, the strobed output at pin 15 will be a "1" of approximately -5.8 v. If pin 4 goes negative with respect to pin 5, the output at pin 15 remains at a +0.3 v. "0".

The strobe input at pin 12 is a -1.1 v "0" pulse. This input must be present in order to allow the circuit to produce a -5.8 v "1" output. If pin 12 is held at -5.8 v "1", the output at pin 15 will be held at +0.3 v "0".

OPERATION

Since this circuit is a direct coupled amplifier, regulated voltages must be used. A connection to -18 volts is made at pin 2 and a connection to -6.8 v is made at pin 13. The -18 v may be obtained from an 18-volt zener diode and a 4.5-ohm resistor in series to -20 v, and the -6.8 v may be obtained using a 6.8-volt zener diode and a 30-ohm resistor in series to -20 v.

The 200-ohm resistors R01 and R04 terminate the sense line, while R02 and R03 provide bias for Q01 and Q02. The 100 mh inductor in the emitter circuit of Q01 and Q02 greatly increases the emitter impedance and improves the common mode characteristics.

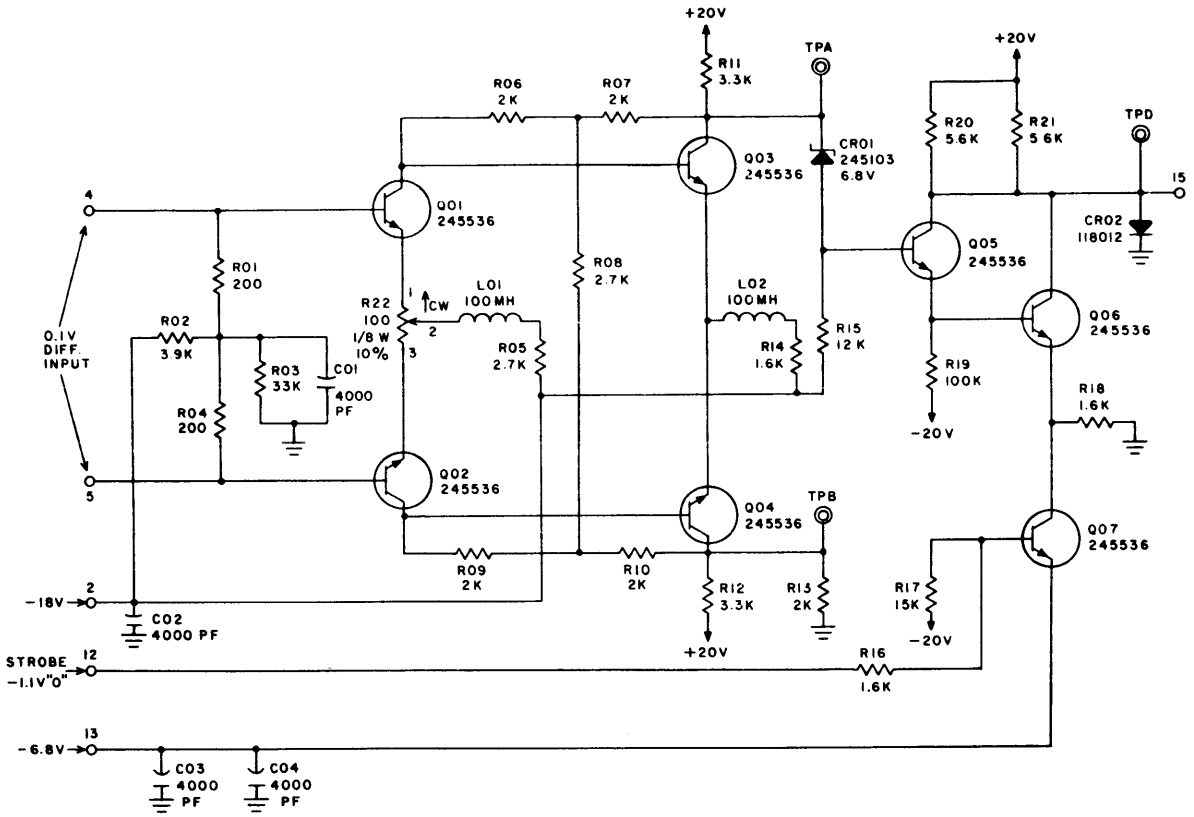
The 2K resistors in the collector circuits of the amplifier provide negative feedback. A portion of this is nullified by the positive feedback connection of R08.

The load resistances of Q01 and Q02 consist of the two 2K resistors plus the 3.3 K resistor. The load of Q03 is the 3.3 K resistor in parallel with the output circuit, while the load of Q04 is the 3.3 K resistor and the 2 K resistor in parallel.

Level translation is performed by the 6.8v zener diode CR01, which drives the input of the Darlington amplifier consisting of Q05 and Q06.

Transistors Q06 and Q07 perform an AND function. If both conduct at the same time, the -6.8v at pin 13 will produce approximately -5.8v at pin 15, allowing for voltage drop across the transistors. Transistor Q06 is driven to its conduction state by a differential input which causes pin 4 to become positive with respect to pin 5. Transistor Q07 is driven to conduction by a -1.1v "0" strobe pulse at pin 13.

If the AND condition of simultaneous conduction by Q06 and Q07 is not met, the voltage at pin 15 will be a logical "0" at approximately +0.3v. This is produced by the forward drop across CR02.




NOTE:

THE POLARITY OF THE DIFFERENTIAL INPUT DETERMINES WHETHER THE STROBED OUTPUT AT PIN 15 IS "1" OR "0", AS FOLLOWS.

| PIN 4 | PIN 5 | PIN 15 | |
|---|---|---|---|
| + | − | "1" | −5.8V |
| − | + | "0" | +0.3V |

Sense Amplifier

## SENSE AMPLIFIER
## Card Type HA18

### FUNCTION

This card amplifies and detects the pulses induced in a sense winding when a magnetic memory core switches polarity. The two ends of the sense winding are connected to pins 4 and 5, and when a core switches its magnetic state, the circuit produces a logical "1" output at pin 15.

The circuit may be conveniently divided into two sections; a differential voltage amplifier having a gain of approximately 100, and a discriminator having an output of approximately -1.6v. The output of -1.6v represents a logical "0" which changes to a logical "1" when a core switches. The following logic card interprets any signal more negative than -3v as a logical "1", however the circuit output approaches -14.6v when a core switches.

### AMPLIFIER

The differential voltage amplifier portion of the circuit is similar to card type C06, which is discussed elsewhere. However, the overall gain is approximately 100 so that the nominal 30 ma induced in the sense winding by the switching of a core results in approximately 3v at the diode bridge.

### DISCRIMINATOR

The discriminator is the portion of the circuit to the right of the diode bridge. Its function is to provide outputs at voltage levels suitable for use by logic circuits. The output of the discriminator is from pin 15 and is approximately -1.6v during the rest state. However, when a voltage appears across the diode bridge, the output at pin 15 approaches -14.6v which is interpreted as a logical "1".

The diodes used in the bridge are high speed silicon devices having a forward voltage drop of the order of 0.6v. Therefore, during the rest state, a voltage-dividing action is provided from +20v to ground through the 22,000-ohm resistor R18, the diode bridge, and the 5600-ohm resistor R21. Due to the forward drop of the diodes, the base of Q09 is held at around 1.2v higher positive potential than the base of Q08. Transistor Q08 thus conducts quite heavily while Q09

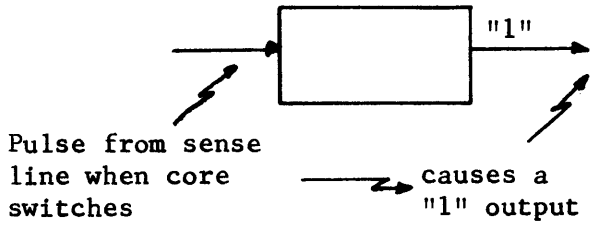
conducts very little. Under these conditions the output at pin 15 is around -1.6 v, due to the voltage dividing action of R20, R21, and the -20 v source. Diode CR05 is in a state of heavy forward conduction, being forward-biased by the +20 v source through R25 and Q08. In this state, the anode of CR05 is at approximately +0.6 v.

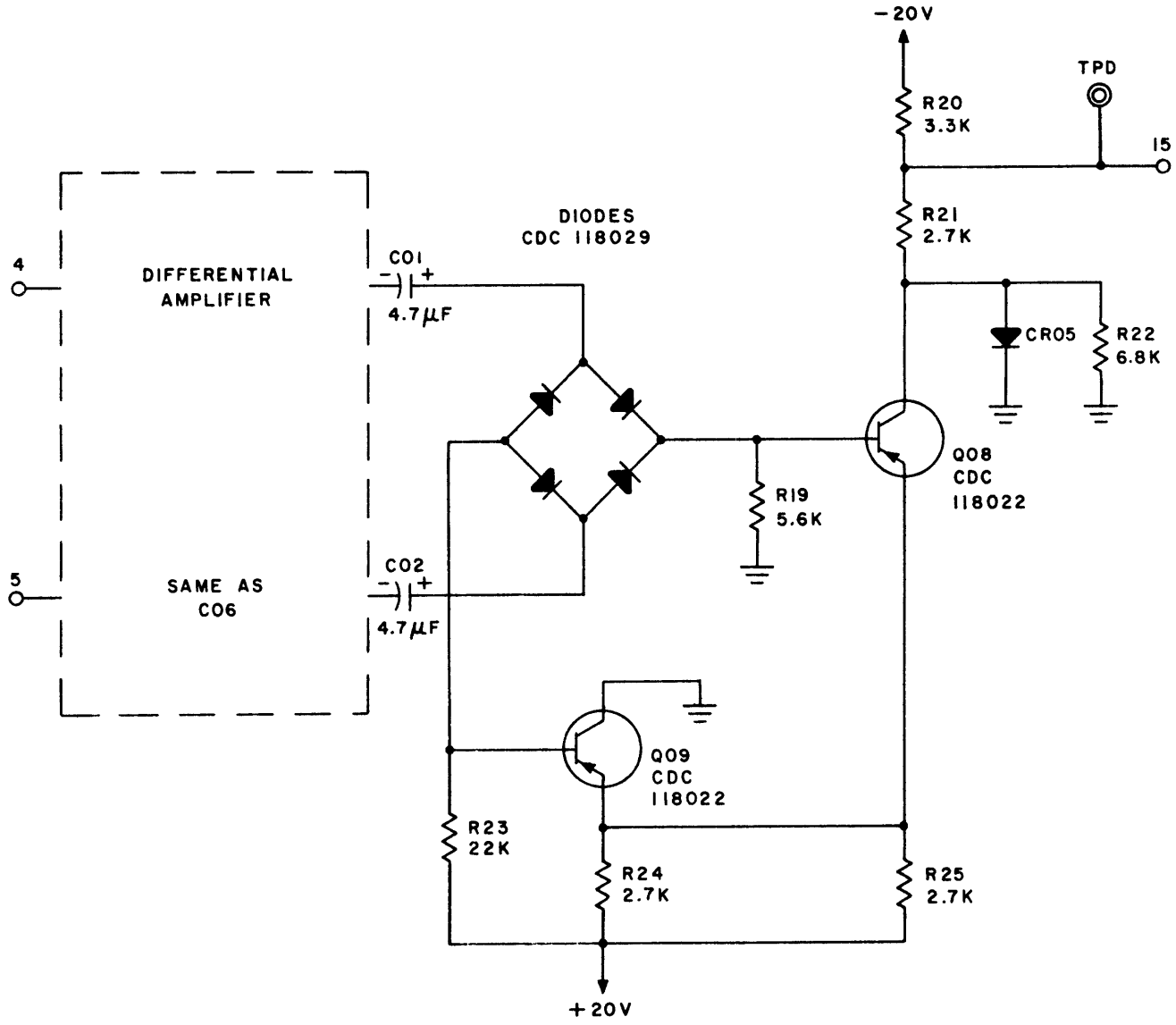
The diode bridge rectifies the potential across it, so an input of either polarity results in a positive input to the base of Q08 and a negative input to the base of Q09. This has the effect of causing Q09 to conduct heavily while Q08, in turn, conducts very little.

The output of -14.6 v is established by the voltage-divider action of R20, R21, and R22. Transistor Q09 provides a low impedance path to ground, so that the emitter of Q08 cannot rise to a high positive potential.

SENSE AMP

HA18 (Block Diagram)



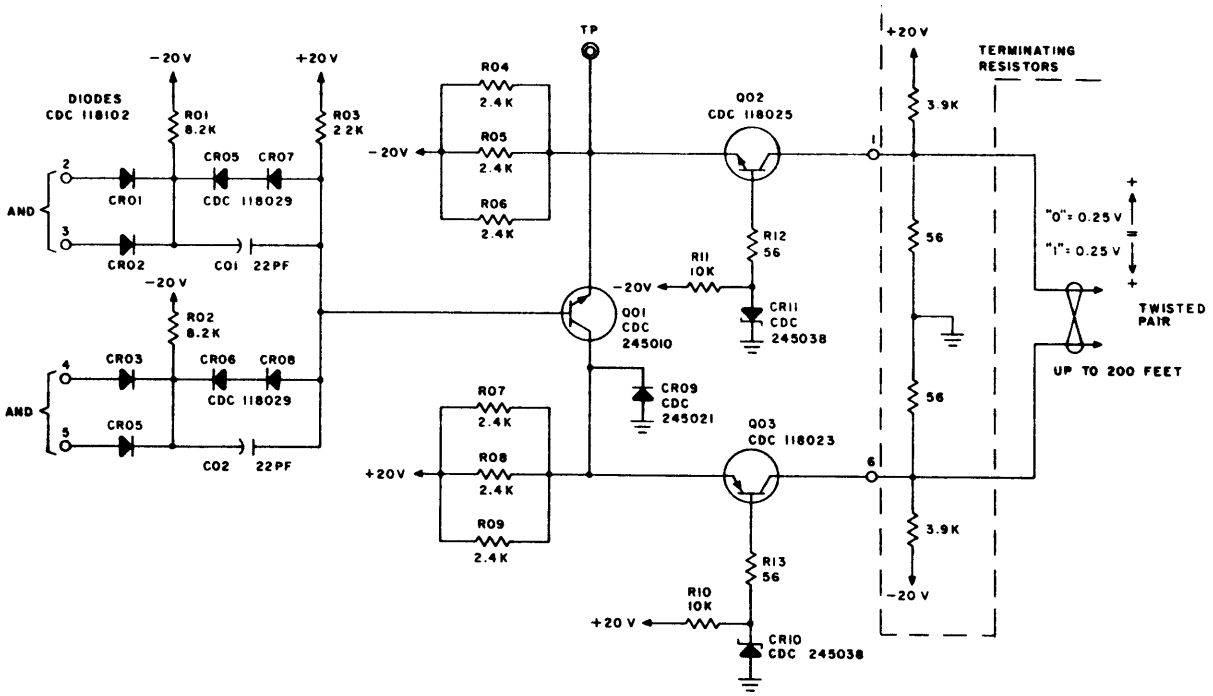



NOTE: PRODUCES "1" OUTPUT WHEN CORE SWITCHES.

Sense Amplifier HA18

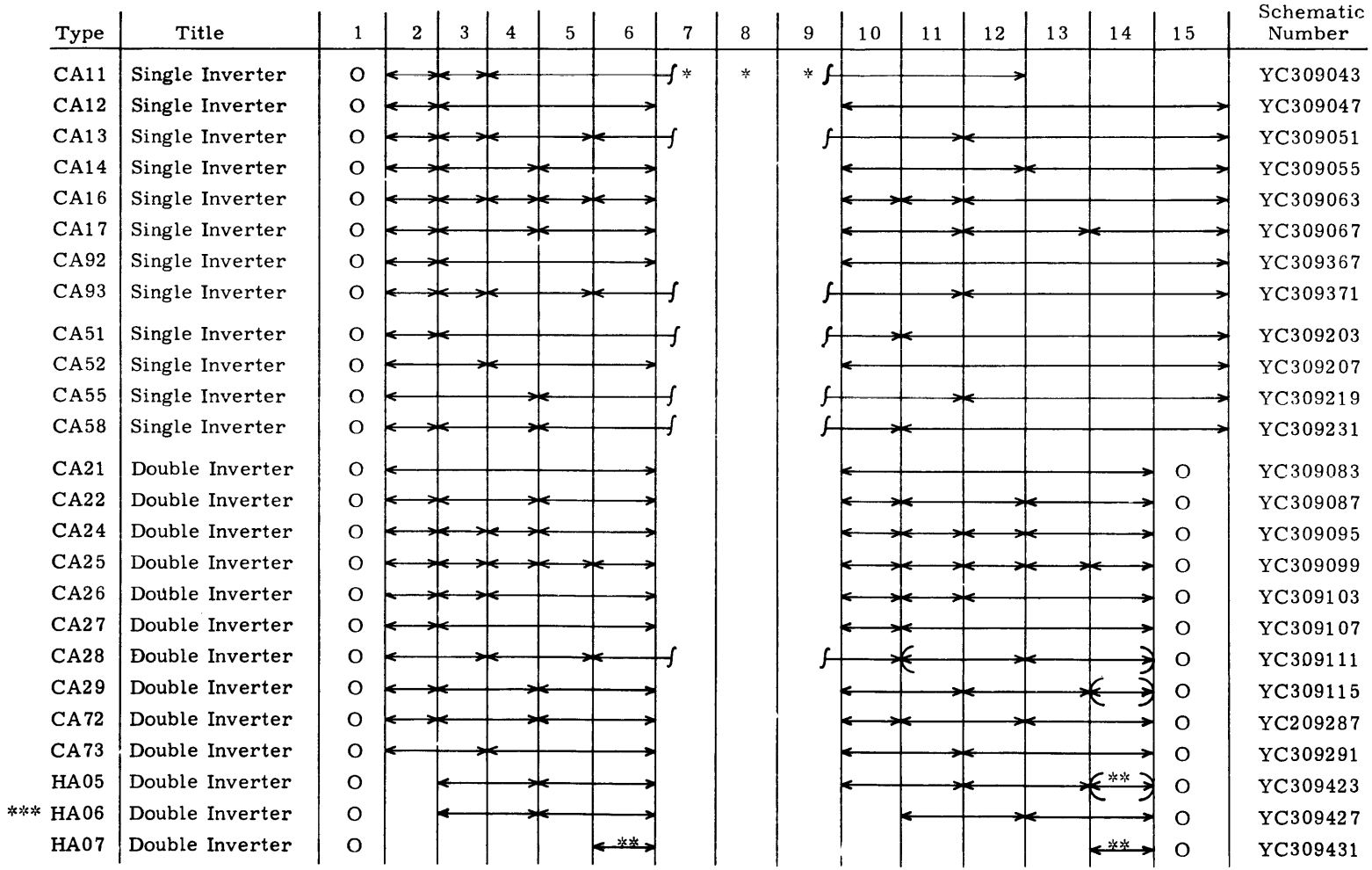
## TRANSMITTER
### Card Type HA 19

The function of the circuits on this card is to convert logic signals into outputs suitable for transmission over a balanced, terminated, twisted-pair transmission line up to 200 feet in length. Each circuit has two 2-way AND inputs. The remainder of the circuit is identical to card type C62 and the same ground rules apply.




NOTE: CIRCUIT OPERATES SAME AS CARD TYPE C62

Transmitter HA19



| Type | Title | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | Schematic Number |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CA11 | Single Inverter | O | ← | ← | ← | | | ∫ * | * | * ∫ | → | | | | | | YC309043 |
| CA12 | Single Inverter | O | ← | ← | | | | → | | | ← | | | | | → | YC309047 |
| CA13 | Single Inverter | O | ← | ← | ← | | ← | ∫ | | ∫ | | → | ← | | | → | YC309051 |
| CA14 | Single Inverter | O | ← | ← | | ← | | → | | | ← | | → | ← | | → | YC309055 |
| CA16 | Single Inverter | O | ← | ← | ← | ← | ← | → | | | ← | ← | → | | | → | YC309063 |
| CA17 | Single Inverter | O | ← | ← | | ← | | → | | | ← | → | ← | | → | → | YC309067 |
| CA92 | Single Inverter | O | ← | ← | | | | → | | | ← | | | | | → | YC309367 |
| CA93 | Single Inverter | O | ← | ← | ← | | ← | ∫ | | ∫ | | → | ← | | | → | YC309371 |
| CA51 | Single Inverter | O | ← | ← | | | | ∫ | | ∫ | → | | | | | → | YC309203 |
| CA52 | Single Inverter | O | ← | | ← | | | → | | | ← | | | | | → | YC309207 |
| CA55 | Single Inverter | O | ← | | | ← | | ∫ | | ∫ | | → | ← | | | → | YC309219 |
| CA58 | Single Inverter | O | ← | ← | | ← | | ∫ | | ∫ | → | | | | | → | YC309231 |
| CA21 | Double Inverter | O | ← | | | | | → | | | ← | | | | | O | YC309083 |
| CA22 | Double Inverter | O | ← | ← | | ← | | → | | | ← | ← | ← | | | O | YC309087 |
| CA24 | Double Inverter | O | ← | ← | ← | ← | | → | | | ← | ← | ← | ← | | O | YC309095 |
| CA25 | Double Inverter | O | ← | ← | ← | ← | ← | → | | | ← | ← | ← | ← | ← | O | YC309099 |
| CA26 | Double Inverter | O | ← | ← | ← | | | → | | | ← | ← | ← | | | O | YC309103 |
| CA27 | Double Inverter | O | ← | ← | | | | → | | | ← | | | | | O | YC309107 |
| CA28 | Double Inverter | O | ← | | ← | | ← | ∫ | | ∫ | ← | | ← | ← | | O | YC309111 |
| CA29 | Double Inverter | O | ← | ← | | ← | | → | | | ← | ← | ← | | ← | O | YC309115 |
| CA72 | Double Inverter | O | ← | ← | | ← | | → | | | ← | ← | ← | | | O | YC209287 |
| CA73 | Double Inverter | O | ← | | ← | | | → | | | ← | → | | | | O | YC309291 |
| HA05 | Double Inverter | O | | ← | | ← | | → | | | ← | → | | | ** | O | YC309423 |
| *** HA06 | Double Inverter | O | | ← | | ← | | → | | | | ← | ← | | | O | YC309427 |
| HA07 | Double Inverter | O | | | | | ** | → | | | | | | | ** | O | YC309431 |

* Unless otherwise noted: pin 7 equals +20v; pin 8 equals ground; pin 9 equals -20v.
** One way AND.
*** 10 pf speed-up capacitor.

| Type | Title | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | Schematic Number |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| HA08 | Double Inverter | O | | | | ** | ** | * | * | * | | | | ** | ** | O | YC309435 |
| HA09 | Double Inverter | O | | | ** | | | | | | | | ** | | | O | YC309439 |
| CA31 | Flip Flop | | | | | | | | | | | | | | | | YC309123 |
| CA32 | Flip Flop | | | | | | | | | | | | | | | | YC309127 |
| CA33 | Flip Flop | | | | | | | | | | | | | | | | YC309131 |
| CA34 | Flip Flop | | | | | | | | | | | | | | | | YC309135 |
| CA35 | Flip Flop | | | | | | | | | | | | | | | | YC309139 |
| CA36 | Flip Flop | | | | | | | | | | | | | | | | YC309143 |
| CA37 | Flip Flop | | | | | | | | | | | | | | | | YC309147 |
| CA40 | Control Delay | | | | | | | | | | | | | | | | YC309159 |
| CA44 | Control Delay | | | | | | | | | | | | | | | | YC309175 |
| CA46 | Control Delay | | | | | | | | | | | | | | | | YC309183 |
| CA47 | Control Delay | | | | | | | | | | | | | | | | YC309187 |
| CA48 | Control Delay | | | | | | | | | | | | | | | | YC309191 |

Output

Output

Clock

* Unless otherwise noted: pin 7 equals +20v; pin 8 equals ground; pin 9 equals -20v.
**One way AND.

| Type | Title | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | Schematic Number |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CA00 | Even Inhibit Driver | $O_A$ | ← | $I_A$ | → | | +40 | ** | ** | ** | GND | ← | $I_B$ | → | | $O_B$ | YC309399 |
| CA01 | Clock Oscillator Amplifier | Dr. O | Trans. Sec. O ← | → | Tank O | | I | | | | I | | Tank O | Trans. Sec. O ← | → | Dr. O | YC309003 |
| CA02 | Line Clamp | I | I | I | I | I | I | | | | I | I | I | I | I | I | YC309007 |
| CA03 | Line Driver | $O_A$ | | ← | → | ← | → | | | | | | ← | → | ← | → $O_B$ | YC309011 |
| CA04 | Odd Inhibit Driver | $O_A$ | | ← | → | ← | +40 | | | | +40 O Term. R. | | ← | → | ← | → $O_B$ | YC309015 |
| CA05 | Gate | O | O | O | +20 I Protcd | +20 Ret. Mem. | Dchg. ← → I | | | | ← | ← | ← | → | | | YC309019 |
| CA06 | Sense Amplifier | | | | I | I | | | | | | | | | | O | YC309023 |
| CA07 | Emitter Follcwer | $I_A$ | $O_A$ | $I_B$ | $O_B$ | | | | | | | | $I_C$ | $O_C$ | $I_D$ | $O_D$ | YC309027 |
| CA08 | Delay Line Driver | O | ← | → | ← | → | → | | | | | | | | | | YC309031 |
| CA09 | Inhibit Compensator | O | | | ← | → | +40 | | | | +40 O Term. R. | | | → | → | O | YC309035 |
| CA10 | Drive Line Transformer | Dr. I | O | O | Gt. I | GND | Dr. I | | | | Dr. I | Gt. I | O | O | GND | Dr. I | YC309039 |
| CA60 | Switch Card | $O_A$ | $I_A$ | $I_A$ | $I_B$ | $I_B$ | $O_B$ | | | | $O_C$ | $I_C$ | $I_C$ | $I_D$ | $I_D$ | $O_D$ | YC309239 |
| CA61 | Receiver | $O_A$ | | | | $+I_A$ | $-I_A$ | | | | $+I_B$ | $-I_B$ | | | | $O_B$ | YC309243 |
| CA62 | Transmitter | $+O_A$ | ← | $I_A$ | → | | $-O_A$ | | | | $-O_B$ | ← | $I_B$ | → | | $+O_B$ | YC309247 |
| CA63 | Transmission Line Termination | +A | -A | +B | -B | +C | -C | | | | +D | -D | +E | -E | +F | -F | YC309251 |
| CA64 | Resync | O* | O* | | I | | | | | | O* | | I | O* | | O* | YC309255 |
| CA65 | Resync | | | I* | I* | I* | I* | | | | I* | | | | | O* | YC309259 |
| CA66 | Resync | $O_A$ | | | | * ← | → * | | | | * ← | → * | | | | $O_B$ | YC309263 |
| CA67 | Cap. Delay, Var. | O | ← | → | ← | → Jpr. | 0.1μs | | | | 0.2μs | 0.5μs | 1.0μs | 2.0μs | | | YC309267 |
| CA68 | Cap. Delay, Var. | O | ← | → | ← | → Jpr. | 5.0μs | | | | 10μs | 25μs | 50μs | 100μs | 300μs | | YC309271 |

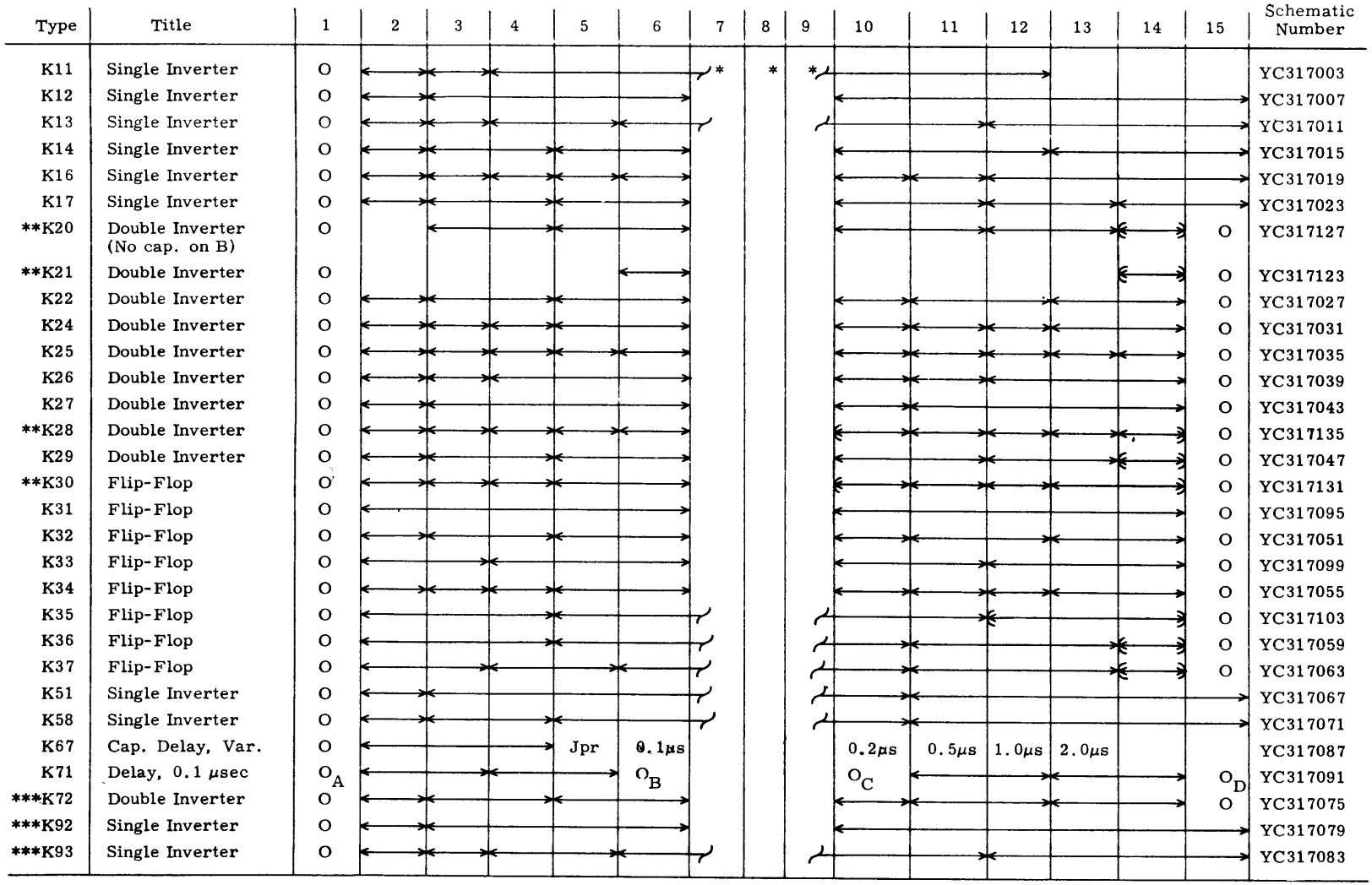
* Indicates +1.8v and +0.8v levels for a "1" and "0" respectively.
**Unless otherwise noted: pin 7 equals +20v; pin 8 equals ground; pin 9 equals -20v.

| Type | Title | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | Schematic Number |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CA69 | Cap. Delay, Var. | O | ← | ← | ← | Jpr. | 1.0mś | ** | ** | ** | 1.0ms | 3.5ms | 10ms | 30ms | 40ms | | YC309275 |
| CA70 | Adder Network Delay | $I_A$ | $O_A$ | $I_B$ | $O_B$ | $I_C$ | $O_C$ | | | | $O_D$ | $I_D$ | $O_E$ | $I_E$ | $O_F$ | $I_F$ | YC309279 |
| CA71 | Cap. Delay, 0.1 usec | $O_A$ | ← | ← | ← | ← | $O_B$ | | | | $O_C$ | ← | ← | ← | ← | $O_D$ | YC309283 |
| *** CA72 | Double Inverter | O | ← | ← | ← | ← | ← | | | | ← | ← | ← | ← | ← | O | YC309288 |
| *** CA73 | Double Inverter | O | ← | ← | ← | ← | ← | | | | ← | ← | ← | ← | ← | O | YC309292 |
| *** CA74 | Double Inverter | O | ← | ← | ← | ← | ← | | | | ← | ← | ← | ← | ← | O | YC309295 |
| CA75 | Modified M | $O_A$ | | | | | $I_A$ | | | | | | | | $I_B$ | $O_B$ | YC309299 |
| CA76 | Modified L | $O_A$ | ← | ← | ← | ← | | | | | ← | ← | ← | ← | | $O_B$ | YC309303 |
| CA77 | Priority | | I | | | | O* | | | | | | | | Clr. | O* | YC309307 |
| CA78 | Priority | | * | * | * | * | I* | | | | | | | Clr. | Ext. Lck. Out | O* | YC309311 |
| | | | ← | ← Lockout | ← | ← | | | | | | | | | | | |
| CA79 | Priority | O | | | | | | | | | | | | | * | * | YC309315 |
| CA80 | Delay, 1 usec | $I_A$ | $O_A$ | $I_B$ | $O_B$ | | | | | | | $I_C$ | $O_C$ | $I_D$ | $O_D$ | | YC309319 |
| CA81 | Crystal Osc. | $O_{LO}$ | $O_{HI}$ | | | | | | | | | | | | | | YC309323 |
| CA82 | Crystal Osc. | $O_{LO}$ | $O_{HI}$ | | | | | | | | | | | | | | YC30327 |
| CA83 | Crystal Osc. | $O_{LO}$ | $O_{HI}$ | | | | | | | | | | | | | | YC309331 |
| CA84 | Relay Driver | $O_A$ | Clmp | ← | ← | ← | ← | | | | ← | ← | ← | ← | Clmp | $O_B$ | YC309335 |
| CA85 | Strobe Shaper | $I_A$ | $O_{A2}$ | $O_{A1}$ | $I_B$ | $O_{B2}$ | $O_{B1}$ | | | | $O_{C1}$ | $O_{C2}$ | $I_C$ | $O_{D1}$ | $O_{D2}$ | $I_D$ | YC309339 |
| CA86 | Sense Amplifier | $O_A$ | $+I_A$ | $-I_A$ | $+I_B$ | $-I_B$ | $O_B$ | | | | $+I_C$ | $-I_C$ | $O_C$ | $+I_D$ | $-I_D$ | $O_D$ | YC309343 |
| CA87 | Driver | ← | ← | ← | ← | | | | | | Cap. GND | | | | | | YC309347 |
| CA88 | Diverter | ← | ← | ← | ← | O | O | | | | O | O | O | O | O | O | YC309351 |
| CA89 | Amplifier Shaper | I | | | | | | | | | | | | | | O | YC309355 |
| CA90 | Emitter Follower | $O_A$ | $I_A$ | $O_B$ | $I_B$ | | | | | | | | $I_C$ | $O_C$ | $I_D$ | $O_D$ | YC309359 |

* Indicates +1.8v and +0.8v levels for a "1" and "0" respectively.
** Unless otherwise noted: pin 7 equals +20v; pin 8 equals ground; pin 9 equals -20v.
*** 10 pf speed-up capacitors.

| Type | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | Schematic Number |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| HA10A | Console Interface | $O_A$ | $I_A$ | $O_B$ | $I_B$ | $O_C$ | $I_C$ | * | * | * | $I_D$ | $O_D$ | $I_E$ | $O_E$ | $I_F$ | $O_F$ | YC 309443 |
| HA11A | Receiver | $O_A$ | $+I_A$ | $-I_A$ | | $+I_B$ | $-I_B$ | | | | $O_B$ | | | $+I_C$ | $-I_C$ | $O_C$ | YC 309447 |
| HA12 | Delay Line Amplifier | $O_A$ | | | | | $I_A$ | | | | | | | | $I_B$ | $O_B$ | YC 309451 |
| HA14 | Digit Driver | | | | | | | | | | ← | ← | G → | +20 | O | O | YC 309459 |
| HA15 | Digit Compensator | $O_A$ | | | ← | ← | -20 | | | | -20 | | | ← | ← | $O_B$ | YC 309463 |
| HA16 | Sense Amplifier | | -18 | | I | I | | | | | | | str. → | -6.8 | | O | YC 309467 |
| HA17 | Filter | $O_A$ | $I_A$ | $O_B$ | $I_B$ | $O_C$ | $I_C$ | | | | $I_D$ | $O_D$ | $I_E$ | $O_E$ | $I_F$ | $O_F$ | YC 309471 |
| HA18 | Sense Amplifier | | | | | I | I | | | | | | | | | O | YC 309475 |
| HA19 | Transmitter | $+O_A$ | ← | | ← | | $-O_A$ | | | | $-O_B$ | ← | | ← | ← | $+O_B$ | YC 309479 |
| HA20 | Light Driver | $O_A$ | ← | | $O_B$ | ← | ← | | | | ← | ← | $O_C$ | ← | ← | $O_D$ | YC 309483 |
| **HA21 | Single Inverter | O | ← | ← | | | ← | | | | ← | | | | | ← | YC 309487 |
| **HA22 | Single Inverter | O | ← | ← | ← | ← | ← | ) | | ( | | | ← | | | ← | YC 309491 |
| **HA23 | Double Inverter | $O_A$ | ← | ← | | ← | ← | | | | ← | ← | ← | ← | ← | $O_B$ | YC 309495 |
| **HA24 | Double Inverter | $O_A$ | | ← | ← | ← | ← | | | | | ← | ← | ← | ← | $O_B$ | YC 309499 |
| **HA25 | Double Inverter | $O_A$ | ← | ← | ← | | ← | | | | ← | | ← | ← | ← | $O_B$ | YC 309503 |
| HA26 | Long Line Receiver | $O_A$ | | | | | $I_A$ | | | | | | | | $I_B$ | $O_B$ | YC 309507 |
| HA27 | Keyboard Translator | O | I | I | | O | | | | | O | | | | | | YC 309511 |
| HA28 | Keyboard Translator | I | I | I | I | I | I | | | | I | I | O | O | O | O | YC 309515 |
| HA29 | Ground | ← All Inputs | | | | | | ) | | ( | | | Grounded | | | → | YC 309519 |
| HA30 | Double Inverter | $O_A$ | ← | | ← | | ← | | | | | | | | ← | $O_B$ | YC 309523 |
| HA31 | Level Translator | $I_A$ | $O_A$ | $I_B$ | $O_B$ | $I_C$ | $O_C$ | | | | $I_D$ | $O_D$ | $I_E$ | $O_E$ | $I_F$ | $O_F$ | YC 309527 |
| HA32A | Line Driver | O | O | ← | ← | ← | ← | ) | | ( | | | ← | | | → | YC 309531 |
| HA33A | Low Speed Oscillator | O | | | | I | | | | | | | | | | O | YC 309535 |
| HA35 | 0.1 Usec Delay | $O_A$ | $I_A$ | | $I_B$ | | $O_B$ | | | | $O_C$ | $I_C$ | | $I_D$ | | $O_D$ | YC 309543 |
| HA37 | Transmitter, 1000-foot | $+O_A$ | ← | | ← | | $-O_A$ | | | | $-O_B$ | ← | | ← | | $+O_B$ | YC 309551 |
| HA38 | Diode | $I_A$ | $O_A$ | $I_B$ | $O_B$ | $I_C$ | $O_C$ | | | | $I_D$ | $O_D$ | $I_E$ | $O_E$ | $I_F$ | $O_F$ | YC 309555 |
| HA39 | Line Terminator | I | I | I | I | I | I | | | | I | I | I | I | I | I | YC 309559 |
| HA43 | Transmitter, 1000-foot | $+O_A$ | ← | | ← | | $-O_A$ | | | | $-O_B$ | ← | | ← | | $+O_B$ | YC 309592 |
| HA46 | Double Flip-Flop | $O_A$ | | | | | $O_B$ | | | | $O_C$ | | | | | $O_D$ | YC 309579 |
| HA47 | Quadruple Inverter | $O_A$ | | | | | $O_B$ | | | | $O_C$ | | | | | $O_D$ | YC 309583 |
| ***HA48 | Quadruple Inverter | $O_A$ | | | | | $O_B$ | | | | $O_C$ | | | | | $O_D$ | YC 309587 |

* Unless otherwise noted, pin 7 equals +20v; pin 8 equals ground; pin 9 equals -20v.
** No speed-up capacitor.
*** 10 pf speed-up capacitor.



| Type | Title | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | Schematic Number |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| K11 | Single Inverter | O | | | | | | * | * | * | | | | | | | YC317003 |
| K12 | Single Inverter | O | | | | | | | | | | | | | | | YC317007 |
| K13 | Single Inverter | O | | | | | | | | | | | | | | | YC317011 |
| K14 | Single Inverter | O | | | | | | | | | | | | | | | YC317015 |
| K16 | Single Inverter | O | | | | | | | | | | | | | | | YC317019 |
| K17 | Single Inverter | O | | | | | | | | | | | | | | | YC317023 |
| **K20 | Double Inverter (No cap. on B) | O | | | | | | | | | | | | | | O | YC317127 |
| **K21 | Double Inverter | O | | | | | | | | | | | | | | O | YC317123 |
| K22 | Double Inverter | O | | | | | | | | | | | | | | O | YC317027 |
| K24 | Double Inverter | O | | | | | | | | | | | | | | O | YC317031 |
| K25 | Double Inverter | O | | | | | | | | | | | | | | O | YC317035 |
| K26 | Double Inverter | O | | | | | | | | | | | | | | O | YC317039 |
| K27 | Double Inverter | O | | | | | | | | | | | | | | O | YC317043 |
| **K28 | Double Inverter | O | | | | | | | | | | | | | | O | YC317135 |
| K29 | Double Inverter | O | | | | | | | | | | | | | | O | YC317047 |
| **K30 | Flip-Flop | O | | | | | | | | | | | | | | O | YC317131 |
| K31 | Flip-Flop | O | | | | | | | | | | | | | | O | YC317095 |
| K32 | Flip-Flop | O | | | | | | | | | | | | | | O | YC317051 |
| K33 | Flip-Flop | O | | | | | | | | | | | | | | O | YC317099 |
| K34 | Flip-Flop | O | | | | | | | | | | | | | | O | YC317055 |
| K35 | Flip-Flop | O | | | | | | | | | | | | | | O | YC317103 |
| K36 | Flip-Flop | O | | | | | | | | | | | | | | O | YC317059 |
| K37 | Flip-Flop | O | | | | | | | | | | | | | | O | YC317063 |
| K51 | Single Inverter | O | | | | | | | | | | | | | | | YC317067 |
| K58 | Single Inverter | O | | | | | | | | | | | | | | | YC317071 |
| K67 | Cap. Delay, Var. | O | | | | Jpr | 0.1μs | | | | 0.2μs | 0.5μs | 1.0μs | 2.0μs | | | YC317087 |
| K71 | Delay, 0.1 μsec | $O_A$ | | | | | $O_B$ | | | | $O_C$ | | | | | $O_D$ | YC317091 |
| ***K72 | Double Inverter | O | | | | | | | | | | | | | | O | YC317075 |
| ***K92 | Single Inverter | O | | | | | | | | | | | | | | | YC317079 |
| ***K93 | Single Inverter | O | | | | | | | | | | | | | | | YC317083 |

* Unless otherwise noted: pin 7 equals +20v; pin 8 equals ground; pin 9 equals -20v.
** No speed-up capacitor.
*** 10 pf speed-up capacitor.