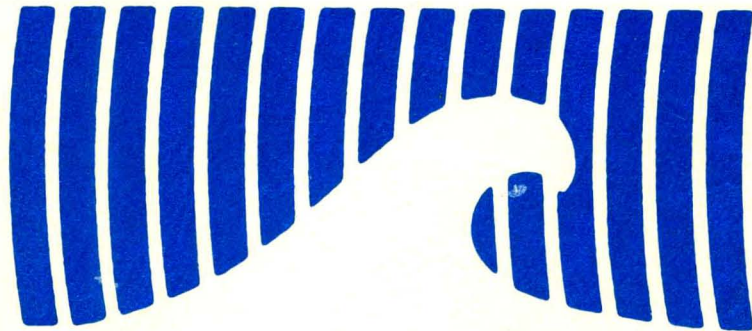


QTIMER™
USER'S MANUAL



**CODAR
TECHNOLOGY
INC.**

Q-TIMER™

USER'S MANUAL

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INTRODUCTION

The Q-Timer is a dual-wide module that is fully compatible with the LSI-11 bus (Q-Bus). It provides the following functions: calendar clock, non-volatile 2KW CMOS RAM, Line Time Clock generation, Line Time Clock control register, 4KW EPROM memory, 8-bit output port, 8-bit input port, watchdog timer and bus termination. Included in the EPROM memory is a monitor program that will read and set the time, boot from a number of different devices, run a system memory test, run a Q-Timer self-test, and down-load a program from a remote computer. This manual contains complete instructions for integrating the Q-Timer into the RSX-11M and the RT-11 operating systems.

All memory and device addresses appear in the I/O page. EPROM memory appears as 16 pages of 256 words and CMOS RAM memory appears as 8 pages of 256 words. The calendar clock provides time information from tenths of seconds through months with the year being stored in CMOS RAM. The Q-Timer may either generate a 60 HZ Line Time Clock signal or it may turn on or off an existing Line Time Clock signal depending on how it is jumpered. The Watchdog Timer function, which must be enabled by jumper, will automatically do a RESTART operation after a certain time interval if a specific memory location is not read. The bus termination function may be removed by pulling the three terminating resistor networks from their sockets. The operation of all of these features is explained in detail in this manual.

Paragraphs enclosed by these asterisks are to be noted as items of interest.

Q-TIMER CONFIGURATIONS

STANDARD (STD) configuration:

All Q-Timer addresses are in the I/O page. The Q-Timer, as shipped standard from the factory, has the CMOS RAM at address 766000 octal, the Software Monitor (including boot routines, diagnostic routines and Calendar Clock format/read routines) at address 773000, and the Line Time Clock (LTC) and the LTC Software Control Register enabled.

MOVE BOOT (MB) configuration:

If your system currently has an operating boot routine in the DEC I/O page at address 773000 octal, then you must either disable your current boot routine at that address or order the Q-Timer Configuration MOVE BOOT which moves the Q-Timer Software Monitor (including boot code, diagnostic routines and Q-Timer Calendar Clock format/read routines) to address 771000 octal.

This situation of boot conflict often occurs due to the fact that some micro-processor based disk and tape controllers contain their own on-board boot code which responds to the address 773000. It is preferred that you disable your current boot to resolve this conflict, so that the Q-Timer boot features can be implemented at the standard start-up address of 773000. If however, you choose to move the Q-Timer Software Monitor via the MB configuration to address 771000, the Software Monitor will implement all its features but must be entered at address 771000.

LTC DISABLE (LD) configuration:

If your system currently has an operating Line Time Clock (LTC) and you do not wish to use the Q-Timer LTC, then the Q-Timer requires the LTC DISABLE configuration which disables the Q-Timer LTC and the Q-Timer LTC Software Control Register. A complete discussion of the LTC function is provided in the LINE TIME CLOCK section of this manual.

FALCON (FAL) configuration:

If your system currently has RAM (or any other device) residing in the I/O page at address 766000 octal, then the Q-Timer requires the FALCON configuration which moves the Q-Timer CMOS RAM to address 775000 octal. (Note this configuration is required for Falcon implementations to avoid conflict with the Falcon RAM.)

FALCON WITH DEC ODT (FDO) configuration:

If your FALCON has the optional ODT chip set, then your Q-Timer requires this configuration which moves the Q-Timer CMOS RAM to 775000 octal and moves the Q-Timer Software Monitor to 774000 octal. Again, the Software Monitor will implement all its features but must be entered at address 774000.

SPECIAL (SP) configuration:

These are special configurations for custom applications or for test purposes.

NOTE: A version of the Q-Timer Monitor is available which includes console ODT for FALCON SBC 11/21 systems. With this feature, you can have ODT without tying up the 11/21's on-board memory sockets which otherwise must be used for the Macro-ODT chips. Call CTI for further information.

Following is a graphical presentation of the labeled EPROM's that are shipped with each of the Q-Timer configurations. Thus, a user can ascertain their Q-Timer configuration via inspection of the EPROM set on a given board.

STANDARD (STD)	----- STD D V_.__ -----	----- STD LB V_.__ -----	----- STD HB V_.__ -----
MOVE BOOT (MB)	----- MB D V_.__ -----	----- MB LB V_.__ -----	----- MB HB V_.__ -----
LTC DISABLE (LD)	----- LD D V_.__ -----	----- LD LB V_.__ -----	----- LD HB V_.__ -----
FALCON (FAL)	----- FAL D V_.__ -----	----- FAL LB V_.__ -----	----- FAL HB V_.__ -----
FALCON WITH ODT (FDO)	----- FDO D V_.__ -----	----- FDO LB V_.__ -----	----- FDO HB V_.__ -----

The upper left corner designates the configuration or option.

The lower left corner designates the PROM as an Address Decoder, Data lo-byte, or Data hi-byte chip.

The lower right corner designates the version of the EPROM code.

If an EPROM set is configured with two options, the second option will appear in the upper right corner, i.e.:

```

-----
| MB            LD|
| D            V_.__|
-----

```

designates the MOVE BOOT and the LTC DISABLE option.

TABLE & FIGURES

Module Size :	5.2 x 8.9 inches dual-wide
Operating Power :	5V +/- 5% 1.2 Amp with bus terminators 0.7 Amp without bus terminators
Operating Temperature :	0 deg. to 50 deg. C
Relative Humidity :	5% to 95% noncondensing
Bus Loading :	1 LSI-11 bus load per I/O line
Batteries :	3 x 1.2 Volt Ni-Cad, 180 ma hours
Battery Back-up :	60 days minimum, 75 days typical
Battery Life :	3 to 5 years typical
Clock Accuracy :	8 sec/month typical error, 15 deg. to 40 deg. C
Address EPROM :	4096 x 8-bit, one 2732, 450 ns max access time
Boot EPROM :	4096 x 16-bit, two 2732's, 450 ns max access
CMOS Memory :	2048 x 16-bit static CMOS RAM
I/O Cycle Time :	6 micro-sec maximum for DATI and DATO 9 micro-sec maximum for DATIO
60 Hz LTC Phase Jitter :	0.2% maximum (33 micro sec), non-accumulating
Parallel I/O :	TTL compatible, 120 ohm input termination

Table 1 "Q-TIMER SPECIFICATIONS"

			Q-Timer Config.
CMOS RAM Memory	256 locations	766000-766777 775000-775777	STD,MB,LD FAL,FDO
EPROM Memory (holds the Q-Timer Software Monitor)	256 locations	773000-773777 771000-771777 774000-774777	STD,LD,FAL MB FDO
8-Bit Output Ports	16 ports	777200-777236	all
8-Bit Input Ports	16 ports	777240-777276	all
Calendar Clock	16 registers	777300-777336	all
EPROM Page Register & Watchdog timer reset	1 location	777340	all
CMOS RAM Page Register	1 location	777342	all
Line Time Clock (LTC) Software Control Reg.	1 location	777546	all

Table 2 "Q-TIMER DEVICE ADDRESSES"

HARDWARE DEVICE ABBREVIATIONS

DD	-	TU58 cartridge tape
DK	-	RK05 disk
DL	-	RL01 or RL02 disk
DM	-	RK06/RK07 disk
DP	-	RP02/RP03 disk
DR	-	RM02 disk
DX	-	RX01 or RX02 diskette
MT	-	TM11 magnetic tape

SOFTWARE FEATURE ABBREVIATIONS

MDO	-	LSI-11 Main Memory Test 16-bit or 18-bit systems
MD1	-	LSI-11 Main Memeory Test 22-bit system
OB	-	Other Boot
SLO	-	Serial Downline Loader "Intellec" format & Terminal Emulator
SL1	-	Serial Downline Loader "Intellec" format
SL2	-	Serial Downline Loader "abs loader" format & Terminal Emululator
SL3	-	Serial Downline Loader "abs loader" format
ST	-	Q-Timer Self-Test
TT	-	Terminal Emulator

Table 3 "SOFTWARE MONITOR BOOT COMMANDS"

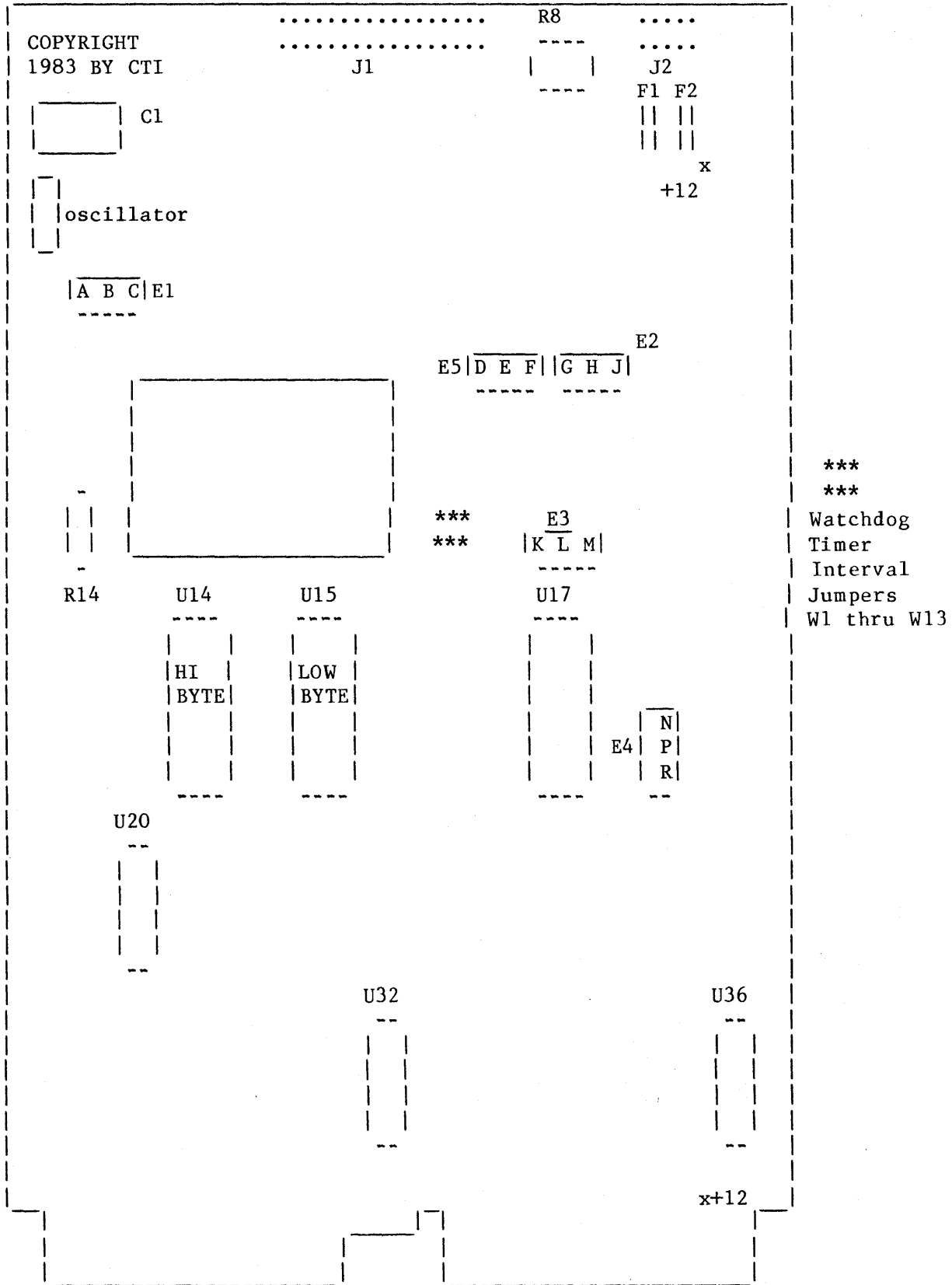


Figure 1 "Q-TIMER COMPONENT LOCATIONS"

PIN	FUNCTION	PIN	FUNCTION
1	GND	18	GND
2	/OUTADR	19	IN 0
3	GND	20	IN 1
4	OUTSTB	21	IN 2
5	GND	22	IN 3
6	OUT 0	23	IN 4
7	OUT 1	24	IN 5
8	OUT 2	25	IN 6
9	OUT 3	26	IN 7
10	OUT 4	27	GND
11	OUT 5	28	ADR 1
12	OUT 6	29	ADR 2
13	OUT 7	30	ADR 3
14	GND	31	ADR 4
15	/INADR	32	GND
16	GND	33	GND
17	INSTB	34	GND

Table 4 "34-PIN CONNECTOR (J1) PINOUT"

PIN	FUNCTION
1	GND
2	32,768 Hz output, TTL levels, 5 unit loads
3	+5 volt output (F1 must be fused at 0.5 amp)
4	32,768 Hz input, +5 volt CMOS levels ($V_{il} < 1.5$ volts, $V_{ih} > 3.5$ volts)
5	+12 volt output (F2 must be fused at 0.5 amp)
6	External LTC signal input, TTL levels, 1/4 unit load
7	External battery input (5.25 volt maximum)
8	32,768 Hz output, CMOS level, 150 Kohm output impedance
9	Q-Timer logic clock output, TTL levels, 5 unit loads (1 MHz + or - 5%)
10	GND

Table 5 "10-PIN CONNECTOR (J2) PINOUT"

Jumper	Time-Out Interval	Jumper	Time-Out Interval	Jumper	Time-Out Interval
1-D	0.133 sec	8-D	17.07 sec	12-D	273.1 sec
4-D	1.067 sec	9-D	34.13 sec	13-D	546.1 sec
5-D	2.133 sec	10-D	68.27 sec	14-D	1092.0 sec
6-D	4.267 sec	E-D	136.50 sec	F-D	disabled
7-D	8.533 sec				

Table 6 "WATCHDOG TIMER JUMPERS"

Q-TIMER INSTALLATION

includes: Calendar Clock Software Routine Integration (Step 4)

CAUTION : Do not discard any shipping materials until the Q-Timer has been inspected for damage. Notify CODAR Technology and the shipping carrier immediately if any damage is evident. Various time limits, depending on the carrier, may apply concerning the reporting of physical damage.

This section provides a 6-step procedure to permit a quick installation of the Q-Timer.

STEP (1) BUS TERMINATION CHECK

If the Q-Timer is to be used as a bus terminator, the resistor DIP packs U20, U32, and U36 must be installed. If not, they must be removed. If the Q-Timer is to be used as a bus terminator, it must be placed in the slot in which the bus lines end. In most backplanes this is the slot directly to the right of the CPU. If not, it can be placed in any vacant board slot (i.e. it does not require bus continuity). The power should always be off when removing or installing boards. See Section III, Figure 1, for the DIP pack locations.

STEP (2) LINE TIME CLOCK (LTC) CHECK

Proper configuration of the LTC function is crucial to the correct operation of the LSI-11 system. Each processor and system provides various implementations of these functions. The LTC must be provided by either the system or the Q-Timer (in which case it will be a good crystal-controlled LTC). Multiple LTC registers or LTC signals will cause improper system operation. See Section IX, LINE TIME CLOCK, for an explanation of the LTC function and implementation.

STEP (3) ADDRESS CONFLICT CHECK

Before installing the Q-Timer, verify that there will be no address conflicts. To do this you must be in ODT. ODT may be entered on most systems by placing the RUN/HALT switch in the HALT position. When you are in ODT you will receive an "@" prompt on your console terminal. After the prompt you may type the octal memory address you wish to examine followed by a "/". If the memory address is nonexistent, which is the response you are looking for, ODT will type "?"; otherwise it will type the contents of the location.

If you obtain any response from these address checks other than "?" (i.e. ODT shows contents at one of the locations), you must decide whether to disable the function residing at the conflicting address on your present system, or to disable or move the device residing at the conflicting address on the Q-Timer. Changing any of the Q-Timer addresses will necessitate changes in the Q-Timer Software Monitor program (EPROM) as well. Contact CTI

for additional information. Q-Timer Addresses have been chosen which are either used identically for equivalent DEC functions, or are listed as unused in the current DEC Q-BUS address map.

Verify that there is no conflict with the CMOS RAM address space:

@766000/ ? with STD, MB, LD configuration
@766776/ ?
@

@775000/ ? with FAL, FDO configuration
@775777/ ?
@

This procedure checks the first and last locations of CMOS RAM. It is possible that there are address conflicts between the two limits. If you are so concerned, you should test every location between.

Falcon installations will experience an address conflict at address 766000 due to the Falcon on-board CMOS RAM. Additionally, if the DEC FALCON ODT is in use, conflict will also occur at address 773000 (see below). This can be solved by ordering the Q-Timer with configuration FAL or FDO. See the Q-TIMER CONFIGURATIONS section of this manual.

Verify that there is no conflict with the EPROM address space:

@773000/ ? with STD, LD, FAL configuration
@773777/ ?
@

@771000/ ? with MB configuration
@771777/ ?
@

@774000/ ? with FDO configuration
@774777/ ?

Again, this procedure checks only the first and last location of the address space.

Any existing boot board such as the DEC BDV11 will produce a conflict at address 773000. Additionally, many of the new generation LSI-11 system disk controllers contain on-board boots which are addressed at 773000. The controller boot must be disabled, or the Q-Timer boot address must be moved via the Q-Timer MB configuration. See the Q-TIMER CONFIGURATIONS section of this manual.

Verify that there is no conflict with the 8-bit Output Port address space:

@777200/ ?
@777202/ ?
.
.
.
@777236/ ?
@

Verify that there is no conflict with the 8-bit Input Port address space:

@777240/ ?
@777242/ ?
.
.
.
@777276/ ?
@

Verify that there is no conflict with the Calendar Clock address space:

@777300/ ?
@777302/ ?
.
.
.
@777336/ ?

Verify that there is no conflict with the EPROM Page Register, the CMOS RAM Page Register, or the Line Time Clock Software Control Register address space:

@777340/ ?
@777342/ ?
@777546/ ?
@

STEP (4) CALENDAR CLOCK SOFTWARE INTEGRATION

The following contains software routines to integrate the Calendar Clock into RSX-11M version 3.2, RSX-11M version 4.0, or RT-11, to allow automatic setting of date and time in your operating system.

BEGINNING OF SOFTWARE INTEGRATION

FOR INTEGRATION into RSX-11M, version 3.2 :

Included in this section are the source and command file listings used to build a program (QTIME.TSK) which will read the calendar clock, and then set the RSX11M/S system time. Note that this program must be built with the privileged (/PR) attribute. This program illustrates one technique by which a program can execute Q-Timer EPROM subroutines. It does not link to the resident library shown below because, as a task with privileged mapping, it will already be mapped to the I/O page.

We suggest that you put QTIME.TSK into SY:[sysuic], and insert the line:

RUN \$QTIME

in your startup command file (SY:[1,2]STARTUP.CMD). This will ensure that your system loads the proper date and time every time it boots.

```
;  
; QTIME.MAC  
;  
; Copyright (C) 1983 Codar Technology, Inc.  
; The following listing is provided for tutorial purposes only.  
;  
; Note that this program does not check for "busy" status of the EPROM RTIME  
; subroutine.  
;  
; Note that if you have chosen the MOVE BOOT configuration, change $QROM  
; below from 173000 to 171000 to reflect the new EPROM Software Monitor  
; starting address.  
;
```

.MCALL EXIT\$\$

```
$QROM = 173000 ; Starting address of EPROM  
RTIME = $QROM+062 ; RTIME subroutine entry (in page 0)  
$QRPAG = 177340 ; EPROM page select register  
  
BEGIN: MOV #ARGS,R5 ; R1 --> date/time buffer  
CLR $QRPAG  
JSR PC,RTIME ; Call RTIME routine in EPROM  
EMT 376 ; Switch to system state, with  
.WORD EXIT ; return to user state at "EXIT:"  
MOV # $TTNS-14,R0 ; R0 --> RSX time locations  
MOV (R1)+,(R0)+ ; Year since 1900 (TTNS-14)  
MOV (R1)+,(R0)+ ; Month ($TTNS-12)  
MOV #MTBL-2,R2 ; R2 --> days per month table  
ADD -(R1),R2 ;  
ADD (R1)+,R2 ; R2 --> this month in days per month table  
MOV (R2),R2 ; R2 := max days in this month plus one  
CMP -2(R1),#2 ; February?  
BNE 10$ ; If NE no  
BIT #3,-4(R1) ; Yes -- leap year?  
BNE 10$ ; If NE no  
INC R2 ; Yes -- add one for leap day  
10$: MOV R2,$TKPS-10 ; Set RSX days per month parameter  
MOV (R1)+,(R0)+ ; Day ($TTNS-10)  
MOV (R1)+,(R0)+ ; Hour ($TTNS-6)  
MOV (R1)+,(R0)+ ; Minute ($TTNS-4)  
MOV (R1)+,(R0)+ ; Second ($TTNS-2)  
CLR (R0)+ ; Clear RSX clock ticks  
RTS PC ; Return to user state  
EXIT: EXIT$$  
  
MTBL: .WORD 32. ; January  
.WORD 29. ; February (non leap years)  
.WORD 32. ; March  
.WORD 31. ; April
```

continued on next page

```

        .WORD 32.          ; May
        .WORD 31.          ; June
        .WORD 32.          ; July
        .WORD 32.          ; August
        .WORD 31.          ; September
        .WORD 32.          ; October
        .WORD 31.          ; November
        .WORD 32.          ; December

ARGS:  .BYTE 1,0          ; Argument list for "CALL RTIME"
        .WORD DATIME      ;
DATIME: .BLKW 9.          ;

        .END BEGIN

```

The following command file will assemble and link the QTIME task. You must ensure that the file RSX11M.STB (or RSX11S.STB, if you are building QTIME to run under an RSX-11S system) is in the directory LB:[sysuic] during the task-build. This is the file that defines the locations within the RSX executive that contain the date and time information.

The STB file will have been left in the proper directory by SYSGEN.

```

.;
.; Copyright(C) 1983 Codar Technology, Inc.
.; The following listing is provided for tutorial purposes only.
.;

.ENABLE SUBSTITUTION
MAC QTIME=QTIME
.OPEN BUILD.CMD
.ENABLE DATA
QTIME/PR=QTIME,LB:~<SYSUIC>~RSX11M.STB/SS
/
PRI=148
STACK=32
UNITS=0
//
.DISABLE DATA
.CLOSE
TKB @BUILD
PIP BUILD.CMD;*/DE,QTIME.OBJ;*
PIP QTIME.*/PU

*****
                END OF RSX-11M version 3.2 INTEGRATION
                BEGINNING OF RSX-11M version 4.0 INTEGRATION
*****

```

FOR INTEGRATION into RSX-11M, version 4.0 :

The following program will set the date and time for RSX-11M version 4.0.

```

.ENABLE LC
.TITLE QTIME Set RSX11M/S V4.0 system date/time
.MCALL STIM$C,EXIT$S
.IDENT /02.02/

```

```

;
; The program shown previously for RSX-11M version 3.2, will actually work under
; any version of RSX11M or RSX11S.
;
; However, the shorter program shown here can be used specifically under version
; 4.0, if the STIM$ directive was included during system generation.
;

```

```

$QROM = 173000          ; Starting address of EPROM
RTIME = $QROM+062      ; RTIME subroutine entry (in page 0)
$QRPAG = 177340        ; EPROM page select register

```

```

BEGIN:  MOV    #ARGS,R5      ; R5 --> argument list
        CLR    $QRPAG        ; Select EPROM page 0

        JSR    PC,RTIME      ; Call RTIME routine in EPROM
        MOV    #-1,DATIME+S.TICP ; Use sysgen ticks/second parameter
        STIM$C DATIME        ; Set RSX system time
        EXIT$$

```

```

ARGS:   .BYTE  1,0          ; FORTRAN compatible arg list for CALL RTIME
        .WORD  DATIME        ;
DATIME: .REPT   9.          ; Buffer for date/time
        .WORD  -1           ; (Init to "default")
        .ENDR
        .END   BEGIN

```

```

*****
                END OF RSX-11M version 4.0 INTEGRATION
                BEGINNING OF RT-11 INTEGRATION
*****

```

FOR INTEGRATION into RT-11 :

The following program will set the date and time for RT-11 version 4. Include the command "RUN QTIME" in the file STARTS.COM . Information regarding older RT-11 versions 2 and 3 is available on request.

```

;
; Copyright 1983, Codar Technology Inc.
;
; Note that if you have chosen the MOVE BOOT configuration, change $QROM below
; from 173000 to 171000 to reflect the new EPROM Software Monitor starting
; address.
;

```

```

        .MCALL    .EXIT,.SDTTM
        .GLOBL   JTIME

```

```

$QROM=173000          ; Starting address of EPROM
RTIME=$QROM+062      ; RTIME subroutine entry (in page 0)
$MUL=$QROM+040       ; $MUL subroutine
$QRPAG=177340

```

```

BEGIN:  MOV    #ARGS,R5      ; R5 --> argument list
        CLR    $QRPAG        ;
        JSR    PC,RTIME      ; Call RTIME subroutine in EPROM

```

continued on next page


```

MOV R1,R5           ; Copy pointer
MOV (R5)+,R2       ; Get year since 1972 in <04:00>
SUB #72.,R2        ;
MOV (R5)+,R0       ; plus month of year in <13:10>
MOV #2000,R1       ;
JSR PC,$MUL        ;
BIS R1,R2          ;
MOV (R5)+,R0       ; plus day of month in <09:05>
MOV #40,R1         ;
JSR PC,$MUL        ;
BIS R1,R2          ;
MOV R2,RTDTM       ; Date is 1st word in RT list
MOV #JHR,R0        ;
MOV (R5)+,(R0)+    ; Copy hours for CALL JTIME
MOV (R5)+,(R0)+    ; Copy minutes
MOV (R5)+,(R0)+    ; Copy seconds
CLR (R0)+          ; No ticks for now
MOV #JARGS,R5      ;
JSR PC,JTIME       ; Convert to RT-style 32-bit integer
.SDTM #AREA,#RTDTM ;
.EXIT

```

```

AREA:  .BLKW      2
ARGS:  .BYTE      1,0
       .WORD      DATIME
DATIME: .BLKW      9.
JARGS: .BYTE      5,0
       .WORD      JHR
       .WORD      JMI
       .WORD      JSE
       .WORD      JTI
       .WORD      RTDTM+2
JHR:   .BLKW      1
JMI:   .BLKW      1
JSE:   .BLKW      1
JTI:   .BLKW      1
RTDTM: .BLKW      3

.END      BEGIN

```

```

*****
                        END OF SOFTWARE INTEGRATION
*****

```

STEP (5) SYSTEM STARTUP

Once the board is in place and the power restored, the system should be started at location 773000. This may happen automatically on power-up if your LSI-11 has been so configured, or it may be done from ODT by typing "773000G" for STD, LD, and FAL configurations; "771000G" for MB configuration; or "774000G" for FDO configuration.

STEP (6) Q-TIMER SOFTWARE MONITOR OPERATION

The Q-Timer Software Monitor (as delivered) should type the time and date and a prompt "*" (if the Q-Timer has previously been configured to auto-boot a device, it will attempt to do so after printing the date and time). The following section of this manual explains the use of the Software Monitor.

Q-TIMER SOFTWARE MONITOR OPERATION

**includes: Boot Commands
Setting the Calendar Clock Time
EPROM Page Register Function**

Please note that a version of the Q-Timer is available which includes console ODT for FALCON SBC 11/21 systems. With this feature, you can have ODT without tying up the 11/21's on-board memory sockets which otherwise must be used for the DEC Macro-ODT chips. Call CTI for further information.

The EPROM Q-Timer Software Monitor code resides at the standard LSI-11 restart address of 773000 octal with Q-Timer configurations STD, LD, or FAL; at address 771000 octal with Q-Timer configuration MB; or at address 774000 with Q-Timer configuration FDO. If your LSI-11 CPU is configured for automatic boot on power-up, it will automatically go to 773000 and, if the Q-Timer has configuration STD, LD, or FAL, enter the Q-Timer Software Monitor. If the LSI-11 is configured for ODT mode on power-up (i.e. gives you an "@" prompt), the user should type 773000G or 771000G or 774000G to enter the Software Monitor routine.

If you have set the Q-Timer to auto-boot a designated hardware device (using the "S" command as explained later in this section), it will print the date and time as shown below and then attempt to boot the selected device. You can abort this auto bootstrap operation by typing two or three <CTRL C>'s immediately after the date/time message is printed.

If you have not set the Q-Timer to auto-boot, the Software Monitor will print to the system console device the day/date/time and the version number and the processor type, followed by a prompt. For example:

```
MON 24-MAY-82 16:28:31 V03.00 11/23
```

```
*
```

If you have the LED/Switch Panel (Test Plug) plugged onto the Q-Timer's 34-pin Connector (I/O Port), the LED's will flash briefly during power-up. The LED's are turned on (i.e. the parallel outputs are set to 1), a read/write check of the Q-Timer's CMOS RAM is performed, and if it succeeds the LED's are then turned off (i.e. the parallel outputs are cleared to 0). If the system hangs with the LED's illuminated a CMOS RAM failure is indicated. Note this is an actual RAM error, and is not caused by loss of battery backup power. Installation of the LED/Switch Panel is not mandatory.

The user may next enter (in response to the Q-Timer's "*" prompt) one of eight commands: "E", "T", "J", "S", "B", "1", "2", or "A" followed by a carriage return.

EXITING THE Q-TIMER MONITOR: "E"

The "E" command may be entered in response to the Q-Timer's "*" prompt to cause an exit to console ODT. This is useful in some systems on which the BREAK feature is disabled. Q-Timer execution can be resumed via the ODT "P" command if relevant system status is not changed (e.g. PC, PS, registers, EPROM and CMOS RAM pages etc.).

SETTING THE CALENDAR CLOCK TIME: "T"

Typing "T" yields:

* DDD DD-MM-YY HH:MM

Thus the Software Monitor indicates the exact format for time information entry ("- " is the prompt). Leading zeros must be typed or the format will not be accepted.

Typing a RETURN without entering all time information will cause the current Calendar Clock date and time to be printed. To set the time, however, the user should type the format indicated. For example, the user may enter:

TUE 05-MAY-82 16:42

Seconds are cleared when you type <RETURN>.

NOTE: to handle leap year correctly, the Q-Timer's date and time must be set (using the Q-Timer monitor's "T" command) during the interval between 1-JAN 00:00:00.0 and 28-FEB 23:59:59.9 of each leap year.

JUMP COMMAND: "J"

"J" is the jump command and can be used to transfer control to any location in the EPROM (by PDP-11 convention control must be to a word address, not a byte address). "J" must be followed by the octal jump address which can range from 00000 to 17776. This command allows implementation of customer generated programs, diagnostics, etc.

AUTOMATIC BOOT: "S"

"S" is the set automatic boot command and is used to specify a device for automatic boot when the Software Monitor is entered (this automatic device specification is stored in the last page of the CMOS memory). "S" must be followed by one of the same device abbreviations as given for the "B" boot command explained below. The automatic boot is cancelled by typing S<RETURN>.

If a device is selected for automatic boot, the question arises as to how one may obtain the Q-Timer Software Monitor prompt since every time the Software Monitor is entered, it automatically boots the device. There are two methods: take the current boot device off-line, or type two or three <CTRL C>'s immediately after the Q-Timer prints out the initial date/time (upon power up).

The "S" command is very powerful, as it eliminates the need to remove a board and change jumpers or DIP switches to select a different boot device. The selected boot device is protected with a series of check bits in CMOS RAM. If an invalid boot device is detected, control returns automatically to the Q-Timer Monitor. This virtually eliminates the possibility of an attempted boot from an erroneous device due to corruption of the Q-Timer CMOS RAM.

BOOT COMMANDS: "B"

"B" is the boot command, and must be followed by one of the two or three-character abbreviations listed in Table 3, Section III.

HARDWARE DEVICES

With the 2-character device abbreviations listed in the top half of Table 3, one can add an optional unit designator. As an example, "B MT2" will attempt to boot from unit 2 of the system tape drive. The space after the B is automatically echoed.

SOFTWARE FEATURES

"MDO for 16 or 18-bit systems; MD1 for 22-bit systems."

This performs a test of the LSI-11 main memory. On unmapped systems, memory will be tested up to the limit of 56 KB. If the processor has memory management hardware, it will be employed to test memory up to the limit of 248 KB on 18-bit systems, or 4088 KB on 22-bit systems.

A message in the format

"[mmmmmm] aaaaaa ccccc vvvvv" (all values are octal)

will be printed for each failing word of memory encountered. "vvvvv" is the incorrect value actually read from the faulty cell, while "cccccc" is the value which should have been returned. For unmapped systems, "aaaaaa" is the physical address (0 - 157776) of the bad cell. For 18-bit or 22-bit mapped systems, "mmmmmm" is the content of the MMU page address register (0 - 177600) and "aaaaaa" is the virtual address (1 - 17776), mapping the bad cell. The physical address (P) can be computed as follows:

$P = (\text{mmmmmm} * 100) + \text{aaaaaa}$ (all values are octal)

For example, the line

17400 7746 0 2

indicates that physical location 1740000 + 7746, or 1747746, read back as 2, when it should have contained a 0.

"OB"

Other Boot provides a means of transferring control to other locations in memory. If you have a Q-Timer with an alternate EPROM address, then "B OB" will transfer control to 773000 octal. It may also be used in conjunction with the "A" command to transfer control to anywhere in the lower 56KB of main memory.

"TT"

"B TT" executes a program which allows the local computer to act as a "terminal emulator" (or "virtual terminal") for a remote computer. In this terminal emulator mode, the local computer is transparent to the local (user) terminal/console. Thus the local terminal interacts in a direct manner with the remote computer. In this mode the transparent local computer maintains a

64-character buffer for characters received from the remote computer for transmission to the local terminal. If the buffer is about to overflow, an X-off character is sent to the remote computer. When the buffer is almost empty an X-on character is sent. If the remote computer responds to these control characters, then it is not necessary to match the baud rates between the local terminal and the remote computer. Otherwise the remote computer baud rate must be less than or equal to the local terminal baud rate to prevent data loss from the remote computer.

"SL"

All SL commands and the TT command use the serial line interface at addresses 776500-776507.

"SL1"

"B SL1" executes a program which allows the local computer to accept, as a down-line device, code or data in the INTEL INTELLEC FORMAT from a remote computer. The user is seated at the local computer. This INTELLEC serial format breaks the data into small blocks, each with a start character, a header, data and a checksum. All numbers are encoded in ASCII hex. The following is an example of the format:

:BBAAAATTDDDD...DDCC	BB is the two-character data byte count.
:BBAAAATTDDDD...DDCC	AAAA is the four-character destination byte address.
.	DD is a data byte.
.	CC is a one-byte checksum formed by summing the record into an 8-bit register and taking the 2's complement.
.	
.	
.:BBAAAATTDDDD...DDCC	TT is the data type. 00 indicates data, 01 indicates end of transmission.

After typing "B SL1" to prepare the local computer for receipt of INTEL format data, the user must next command the remote computer (in whatever manner is dictated by the user installation) to send the INTEL format data down-line. The last item in the down-line data transfer must be a starting-address record (type 01). This will cause control to immediately transfer to the address given in the address field of that record. If this starting-address record is absent from the down-line data transfer, the program hangs while waiting for more data. If the address is even, control is transferred to that address; if it is odd, exit is made to the Q-Timer monitor.

"SLO"

"B SLO" implements both the Serial Downline Loader "Intellec" feature and the Terminal Emulator feature.

Typing "B SLO" executes a program which sets up the local computer for receipt of INTEL-format data (acceptor mode), and also implements the Terminal Emulator mode. The user is seated at the local computer console. The user can next type the appropriate command (but no RETURN) to instruct the remote computer to begin sending the INTEL-FORMAT data down-line to the transparent local computer (acceptor), and a null character (control-space on some terminals, control-@ on others) and then the RETURN. Following is an example of this for a DEC LSI-11 system:

B SLO

<command line to remote computer><null character><RETURN>

This command sequence allows the local (user) terminal to command the remote computer to start the down-loading of data to the local transparent computer. The null character (which is not sent to the remote computer) indicates to the local transparent computer that one more character will be sent to the remote computer (usually a RETURN) and that the local transparent computer shall then switch into the INTEL-format acceptor mode.

The last item in the down-line data transfer can be a record to transfer control to the starting address of the down-loaded program (this starting address would be encoded in the address field of the record). If this last record/command transfers control back to the Q-Timer Monitor, which it can do by encoding any odd starting address, the Terminal Emulator mode will then not be in effect.

"SL2" or "SL3"

SL2 and SL3 are the implementation in "abs loader" format, of SLO and SL1 respectively. With the abs loader format as created by the RT11 linker, the data is un-coded. It runs about twice as fast as "Intellec", but requires that the serial ports at each end be configured for 8-data-bit operation. The abs loader does not support loading of the Q-Timer CMOS RAM -- if you wish to do so, you must use the "Intellec" loader SLO or SL1.

"ST"

"B ST" runs the Q-Timer self-test. Selecting "ST" with the "S" command self-test, is not generally useful to the Q-Timer user, as it is meant for factory testing.

"1" or "2" (FALCON only)

For FALCON 11/21 systems, you can set the baud rate on either of the Falcon Serial Line Units (SLU's) prior to implementation of the Serial Downline Loader features. It is recommended that you read the previous discussion (this section, under BOOT COMMANDS) regarding the SLO/1/2/3 software features.

"1 x2<CR>" selects baud rate x for SLU1.

"2 x2<CR>" selects baud rate x for SLU2.

"1 <CR>" enables autobaud for SLU1.

Baud rates 0 thru 7 (typed in place of x) are:

0	300 baud	3	2400 baud	6	19200 baud
1	600 baud	4	4800 baud	7	38400 baud
2	1200 baud	5	9600 baud		

For example, to select 9600 baud before implementing SL2, type;

"2 52<CR>"

"A"

By typing in the "A" command, one can specify an address which will be stored in CMOS RAM. This address will be used in ANY subsequent bootstrap instead of the normal device address. The syntax of the "A" command is:

A xxxxxx<CR> where "xxxxxx" is an octal address up to 6 digits long.
 The carriage return is needed only if "xxxxxx" is shorter
 than 6 digits.

A <CR> to clear the alternate address and resume use of the
 default addresses.

ANY bootstrap which is invoked while the alternate address (set with the "A" command) is in effect will use the alternate address. To return to normal operation, you must clear the alternate address.

No alternate address can be specified for the console terminal, nor for Q-Timer on-board devices.

The "Intellec" format serial line loader (SL0 and SL1) does not support the alternate device feature, while the "abs loader" format (SL2 and SL3) does.

Uses of the "A" alternate device address include:

Powering up to any location in the lower 56 KB of main memory, or to any address in the I/O page (accessible via the "OB" boot command, see the previous discussion of "OB" under BOOT COMMANDS, this section). For example, to configure the Q-Timer to go to location 1000 for bootstrap:

A 1000<CR> sets alternate address to 1000
S OB<CR> selects "OB" for Auto-Boot on power up (see SET AUTO-BOOT, this
 section)

Bootstrapping from a disk or tape controller at other than the standard addresses (when you have more than one such controller):

A 172420 sets an alternate tape controller address
B MT1 boots unit 1 on the alternate controller (see BOOT COMMANDS,
 this section)

Using a serial port other than the one at 776500 for "TT" or "SL2/3" (see BOOT COMMANDS, this section):

A 176510 sets an alternate Serial Line address
B TT<CR> implements the Terminal Emulator

EPROM PAGE REGISTER FUNCTION:

The EPROM read-only memory is 4K words long X 16 bits wide, and is fully byte addressable. Two 2732 EPROM's (each 4K X 8), one for the high byte (U14) and one for the low byte (U15), are concatenated to yield the 16 bit word length. The EPROM memory is divided into 16 pages (0 through 15) of 256 words each, and utilizes a 4-bit page offset register. Thus the EPROM uses a 256-word block of the I/O page plus 1 word for the page offset register. The EPROM memory is supplied from the factory pre-programmed with the Q-Timer Software Monitor. The EPROM address assignment is 773000 or 771000 or 774000 octal, depending on the Q-Timer conguration as explained in Section II (see also Section III, Table 2).

The EPROM Page Offset Register is used by the Q-Timer Monitor to access the EPROM memory pages. The EPROM Page Offset Register address assignment is 777340 octal. Only bits 9, 10, 11 and 12 are used to set the page offset register. Bit 9 is the LSB and bit 12 is the MSB. The EPROM page offset register is write-only and is cleared to 0 (page 0) on power-up or by a RESET instruction.

The EPROM's are supplied with an opaque label which should not be removed. This label prevents accidental erasure due to exposure to sources of strong ultraviolet radiation. The label also contains information regarding the revision level of the Q-Timer Software Monitor.

CALENDAR CLOCK

CAUTION :

THE Q-TIMER CMOS clock oscillator is a high-impedance device; hence care should be exercised when handling the Q-Timer board if the time is to be preserved while the board is out of the computer. Placing fingers on the oscillator circuitry may cause it to stop oscillating. While this will not harm the circuitry, it will result in the loss of time (the oscillator is located in the upper left hand corner of the board directly behind the handle). Setting the board on a conductive surface may short the Ni-Cad battery supply and cause a complete loss of calendar time (as well as the contents of CMOS RAM). The plastic sheet on the back of the board is designed to eliminate the possibility of a short.

If the plastic sheet is removed, it must be re-glued with RTV non-corrosive adhesive (i.e. does not contain acetic acid which will corrode the board). Note that corrosive RTV can usually be identified by a strong vinegar-like acetic acid smell.

The Calendar Clock function occupies 16 consecutive word addresses within the I/O page.

A 32,768 Hz oscillator is used to drive the Calendar Clock (and the LTC circuitry under normal jumper configuration). The output of this on-board oscillator can be monitored on pin 8 of the Q-Timer Auxiliary Connector; the oscillator frequency can be adjusted via capacitor C1 (use a non-metal screwdriver/device to adjust the capacitor; 1/8 turn corresponds to approximately 0.1 Hz). The location of these components is shown in Section III, Figure 1. Note that a 0.1 Hz error in oscillator frequency translates to a timekeeping error of 0.26 seconds per day, or approximately 7.9 seconds per month. An accurate frequency counter must be used !

The year, as output by the Q-Timer Software Monitor, is stored in the Q-Timer CMOS memory and is updated whenever the SET TIME COMMAND is used. The algorithm that maintains the year functions as follows. Whenever the time is read and the date is in the last half of the year, a flag is set in CMOS RAM. Whenever the time is read and the date is in the first half of the year, the flag is checked: if it is set the year is incremented and the flag is cleared. This algorithm will properly maintain the year provided you read the time at least once in the first half of the year, and at least once in the second half of the year.

Information regarding the Calendar Clock registers is printed in the Codar Technology "Q-TIMER TECHNICAL ADDENDUM", available at no charge from CTI.

WATCHDOG TIMER

The Q-Timer is shipped with the Watchdog Timer disabled. In order to enable it, the wire-wrap jumper between D and F in Jumper Area E5 must be removed. Connecting a jumper between D and E in Jumper Area E5 will result in a time-out interval of 136.5 seconds. Other time-out intervals are available by installing a jumper from D to the numbered holes around U38. The time-out intervals that may be obtained are shown in the table below.

When the Watchdog Timer is enabled, location 777340 must be read periodically to prevent it from timing out. Each read of 777340 or RESET instruction clears the Watchdog Timer so that the full time-out interval must elapse before the CPU is restarted. If the Watchdog Timer times out, bus line DCOKH is toggled. This produces the same effect as pressing the RESTART button on the front panel.

The Q-Timer Software Monitor reads the Q-Timer EPROM Page Select Register periodically to guarantee that the Watchdog Timer does not "bark" during terminal input and other delays.

The Watchdog Timer will be muzzled while the Q-Timer Monitor waits for input from the console, during execution of the Memory Test "MD0/1", Serial Line Loader "SL0/1/2/3", Self-Test "ST", and Terminal Emulator "TT" (see Section V), and during bootstrap operations up to the point at which the secondary boot begins execution.

If the Watchdog Timer is enabled, it is the user's responsibility to ensure that the delay is long enough to permit the system bootstrap to complete, or that the secondary boot contains code to control the Watchdog Timer during the operation.

On FALCON 11/21 systems, the Q-Timer console ODT muzzles the Watchdog Timer during console input if ODT entry was the result of the Q-Timer "E" command (see Section V), or a BREAK. ODT entries that result from power-up, HALT execution, or references to non-existent memory by a program are allowed to timeout in order to ensure a system restart after software errors.

Jumper	Time-Out Interval	Jumper	Time-Out Interval	Jumper	Time-Out Interval
1-D	0.133 sec	8-D	17.07 sec	12-D	273.1 sec
4-D	1.067 sec	9-D	34.13 sec	13-D	546.1 sec
5-D	2.133 sec	10-D	68.27 sec	14-D	1092.0 sec
6-D	4.267 sec	E-D	136.50 sec	F-D	disabled
7-D	8.533 sec				

"WATCHDOG TIMER JUMPERS"

CMOS RAM

The CMOS read/write memory is 2048 words long X 16 bits wide, and fully byte addressable. It is divided into 8 pages (0 through 7) of 256 words each, and utilizes a 3-bit page offset register. The memory uses a 256-word block of the I/O page plus 1 word for the Page Offset Register. Thus, at any given time only 256 words of the 2048 total appear in the I/O page. The desired 256 word "page" is selected by writing to the Q-Timer Page Offset Register (location 777342 in the I/O page) using bits 10, 11, and 12. Bit 10 is the LSB and bit 12 the MSB. The Page Select Register is write-only and is cleared to 0 (page 0) on power-up or by a RESET instruction. The Q-Timer CMOS RAM page 7 is reserved for use by the Q-Timer Software Monitor, thus the user can use pages 0 thru 6.

The CMOS RAM may be used as standard program memory. Due to the paging technique, the programmer has access to only 256 words without changing the Page Offset Register. The Page Offset Register needs to be written only once to select a given page, and the selected page will remain selected until either a reset instruction is executed, a power up sequence occurs, or the Page Offset Register is rewritten.

Programs that use the CMOS RAM for data or parameter storage require no unusual programming techniques other than ensuring that the Page Offset Register is properly incremented at the end of a 256 word page (the Page Offset Register does not autoincrement on overflow). Programs, such as device hardware boots, that execute program instructions from CMOS RAM or EPROM require some amount of planning. The program should be optimized to eliminate any unnecessary jumps between 256 word pages. When a new page is selected by writing to the Page Offset Register, the address selected within the page does not change. Thus, if location 140 in page "0" contains an instruction that selects page "5", the next instruction executed will be in location 142 in page "5". This situation is best handled by using reserved locations at the end of a page for transferring control between pages.

CAUTION :

As discussed in this Section , Ni-Cad battery backup is provided to make the CMOS RAM and Calendar Clock non-volatile. If the DEC specified power-down sequence is followed, Q-Timer CMOS memory corruption will not occur. If, however, the DEC protocol is not followed there may be adverse consequences. If bus signal BDCOK is not implemented, corruption of the CMOS memory and/or the Calendar Clock may occur during power-up or power-down. If the signal BPOK is not implemented and a CMOS memory location is being written at the time the +5 volt power fails, there is a chance that the single location being accessed will be corrupted. Other locations in the CMOS RAM will be unaffected.

This potential problem may be eliminated by proper implementation of the BPOK signal. The system power supply should assert BPOK at least 4 msec prior to actual power failure. Assertion of BPOK will cause the CPU to trap to the standard power-fail address at 24 octal. The user/programmer is responsible for generating software to insure orderly shutdown as a result of this trap. Specifically, all write operations to either the CMOS RAM or Calendar Clock should be terminated. It is recommended that the customer verify that his LSI-11 chassis does in fact properly implement the DEC power sequencing protocol including both BPOK and BDCOK. Proper implementation is fortunately the rule and not the exception.

LINE TIME CLOCK

includes: LTC Jumper Configurations

Experience has shown that system designers do run into problems with the LTC. Many systems generate the 60 HZ LTC directly from the system power supply. You may find it necessary to remove wires from your LSI-11 backplane to disable the chassis-generated LTC on your system, if you choose to use the Q-Timer LTC.

Note that jumper W4 on the DEC LSI-11/23 CPU, must be removed to enable BEVENT and to allow the use of an LTC.

The Q-Timer LTC (Line Time Clock) circuitry drives the LSI-11 bus line BEVENT at a 60 Hz rate. BEVENT is a hardwired LSI-11 interrupt which is normally used by RT-11 and RSX-11 as the operating system clock. The 60 Hz LTC signal is synthesized from the Q-Timer's on-board 32,768 Hz oscillator using a 15/16 pulse-swallowing technique. The same 32,768 Hz oscillator is used to drive the Calendar Clock, thus allowing the use of the LTC and the Calendar Clock in applications requiring the synchronous timing of both functions. The pulse-swallowing synthesis technique results in an extremely small "phase jitter" of about 33us. This is not an inaccuracy or a drift but rather a short term fluctuation which averages to zero. This "phase jitter" is actually insignificant when compared to fluctuations inherent in 60 Hz clocks derived from the A.C. power line.

The Q-Timer LTC Software Control register responds to the standard DEC address of 777546 octal. The LTC Software Control register (and address) is supported by both RT-11 and RSX-11 operating systems. The LTC Software Control register is a single-bit write-only device which is set by writing either "1" or "0" in bit location 6. Writing a "0" disables the LTC interrupts by clamping the BEVENT line to ground. The LTC interrupts are enabled by writing a "1" which releases the clamp on BEVENT. The LTC Software Control register does not actually generate a LTC clock signal; it only controls (clamps) whatever signal is present on the BEVENT line. Note that the DEC power-up protocol and/or the RESET instruction will clear the LTC Software Control register, thus clamping the BEVENT line and disabling interrupts.

Following are brief descriptions of the STD and LD factory-available "configurations". Alternatively, one can implement one of the following user-installed "alternatives". The jumper and pin locations are shown in Section III, Figure I.

The STANDARD (STD) configuration and the three "LTC alternatives" (which are not given as available "configurations" from the factory) can be field installed. The LTC DISABLE (LD) configuration requires the use of an EPROM programmer to modify the Q-Timer Address Decoder EPROM to insure a null response by the Q-Timer at the LTC software control address (and thus is given as a factory installed configuration).

STANDARD (STD) configuration:

In the standard configuration, the on-board 32,768 Hz oscillator is used to generate the 60 Hz LTC signal, which drives BEVNT, which in turn is enabled/disabled by the LTC Software Control register.

LTC with External 32,768 Hz alternative:

The 60 Hz LTC signal can alternatively be obtained from an external 32,768 Hz oscillator via pin 4 of the Q-Timer Auxiliary Connector. This allows the use of an extremely high accuracy clock if required in the application. This option is jumper selectable (shown later in this section); the external oscillator is not supplied with the Q-Timer.

LTC with External LTC alternative:

An external LTC signal may be brought in via pin 6 of the Q-timer Auxiliary Connector. This does not have to be 60 Hz and can be any frequency desired (with suitable modifications to the operating system). The signal must be at standard TTL levels, and loading is 1/4 unit load. This option is also jumper selectable (shown later in this section). The functioning of the LTC Software Control register is unchanged.

LTC Clamp but no LTC alternative:

This alternative disables the 60 Hz LTC signal generated on the Q-Timer, but maintains the LTC Software Control register. The LTC Software Control register will (under software control) clamp/release the LSI-11 backplane BEVNT line. This alternative is typically used in systems that generate the 60 Hz LTC signal in the system power supply or by other means. One consequence of this configuration is that the time as maintained by the Calendar Clock chip will not be exactly synchronized with the system time derived from the 60 Hz power line (system power supply).

LTC DISABLE (LD) configuration:

The Q-Timer 60 Hz LTC and the Q-Timer LTC Software Control register can be completely disconnected from the LSI-11 BEVNT line. This is achieved by a two part modification. First the 60 Hz LTC function on the Q-Timer is disabled via jumper configuration (shown later in this section). Next the LTC Software Control register is disabled from responding to its I/O page address. This is accomplished at the factory by modifying the Q-Timer Address Decoder EPROM to insure a null response (by the Q-Timer) at the LTC software control address.

Proper configuration of the various LTC functions is crucial to the correct operation of the LSI-11 system. Each DEC processor and system provides various combinations of these functions. Multiple LTC registers or LTC signals will cause improper system operation.

The following LTC Jumper representation is provided to allow the user to accomplish configuration quickly with minimal description. Each jumper, on the Q-Timer board, consists of 3 pins, and in each case the center pin must be jumpered to one of the pins on either side. See Section III, Figure 1 for jumper locations.

LTC JUMPERS

STANDARD (STD) configuration: On-board generation of 60 Hz, and LTC Software Control Register ENABLED.

E1: PINS (A-B) E2: PINS (J-H) E3: PINS (K-L) E4: PINS (N-P)

LTC with External 32,768 Hz alternative: External 32,768 Hz oscillator via pin 4 of the Q-Timer Auxiliary Connector.

E1: PINS (B-C) E2: PINS (J-H) E3: PINS (K-L) E4: PINS (N-P)

LTC with External LTC alternative: External signal via pin 6 of the Q-Timer Auxiliary Connector drives the BEVNT line.

E1: PINS (A-B) E2: PINS (H-G) E3: PINS (K-L) E4: PINS (N-P)

LTC Clamp but no LTC alternative: LTC Software Control Register only, used to clamp or release BEVNT line.

E1: PINS (A-B) E2: don't care E3: PINS (L-M) E4: PINS (N-P)

LTC DISABLE (LD) configuration: Disable any interaction with BEVNT (Address Decoder EPROM must be changed to disable BRPLY).

E1: PINS (A-B) E2: don't care E3: don't care E4: PINS (P-R)

I/O PORTS & OTHER ITEMS

includes: 34-Pin I/O Port Configuration & Timing
10-Pin Auxiliary Connector Configuration
Bus Termination By The Q-Timer
LED/Switch Panel (Test Plug) Use
On-Board Rechargeable Batteries

34-PIN I/O PORT CONFIGURATION & TIMING:

See Section III, Table 4, "34-PIN CONNECTOR (J1) PINOUT", for the pinout of this port.

The latched 8-bit Parallel Output Port is write-only. Of the data word sent to the port, only bits 0 through 7 are used for data output; the remaining 8 bits are ignored. The Output Port occupies 16 consecutive word addresses within the I/O page. All 16 bus addresses result in a write operation to the same physical port; however, bits 1, 2, 3 and 4 of the bus address are made available on the parallel port connector so that external logic may decode up to 16 different external destination addresses.

The 8-bit Parallel Input Port is read-only and is terminated in 120 ohms at 3.4 volts by SIP resistors R5 and R6. The Input Port also responds to 16 bus addresses and can be expanded to 16 input ports using the address bits 1-4 (and external decoding logic). Detailed interface and timing information is provided later in this section.

The Parallel Port connector (J1) is a standard 34-pin male ribbon connector with "long" latching hardware. A mating connector is not supplied with the Q-Timer; the proper 3M connector number (any equivalent will also work) is # 3414-7034 socket connector, closed end cover with strain relief.

There are two control lines associated with the Input Port, /INADR and INSTB, and 2 lines associated with the Output Port, /OUTADR and OUTSTB. All four control lines are outputs. If one is not attempting to decode port addresses, the 4 address lines (ADR 1-4) and the /INADR and /OUTADR control lines can be disregarded.

All voltage levels are TTL. Output control signals are driven by a 74LS244 octal buffer, and output data lines (OUT 0-7) are driven by a 74LS374 buffer register. Thus, data written to the output port remains latched and stable until the port is written again. Timing information is provided in the following figure.

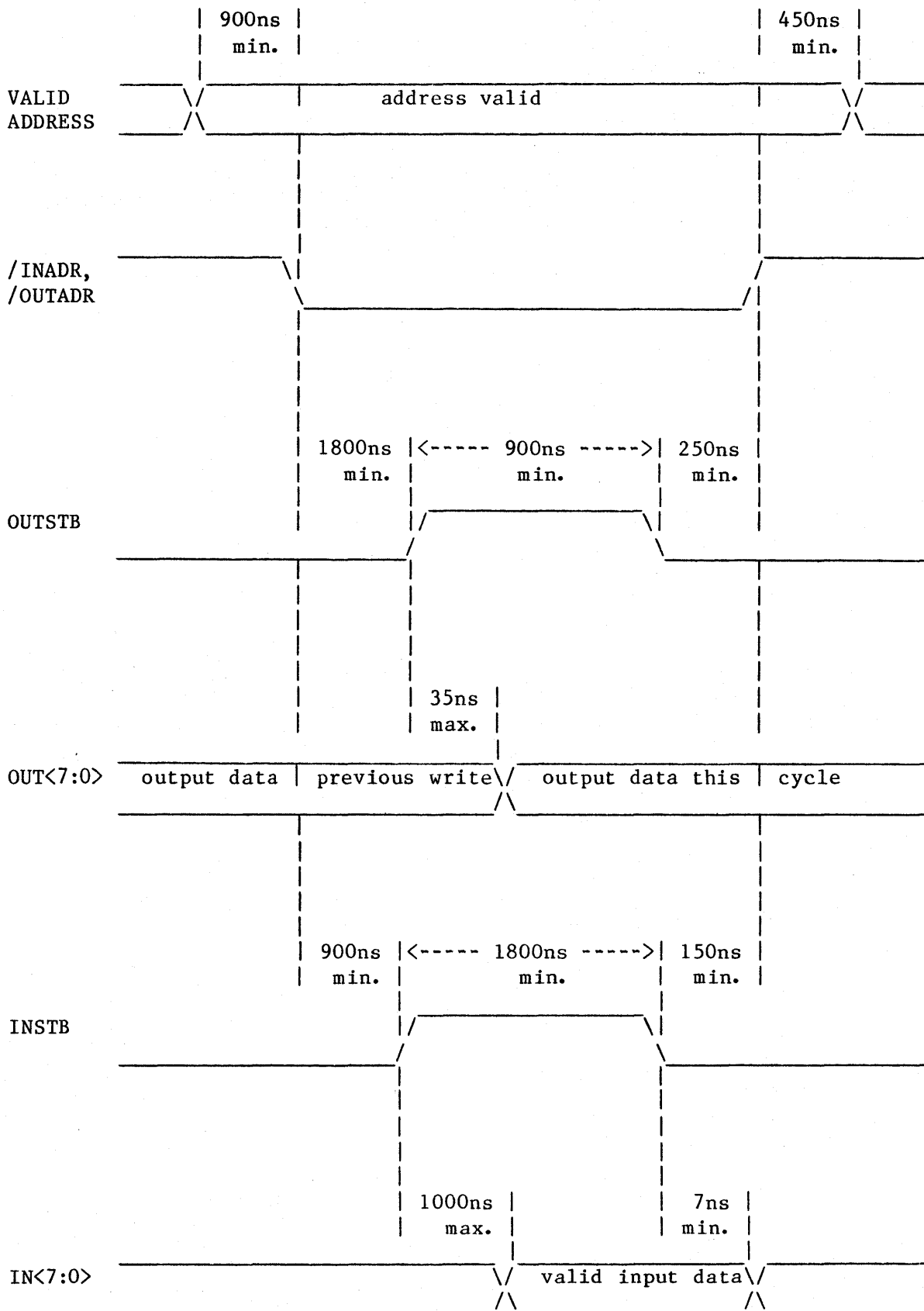


Figure 2 34-PIN CONNECTOR. PARALLEL I/O PORT TIMING DIAGRAM

10-PIN AUXILIARY CONNECTOR CONFIGURATION:

See Section III, Table 5, "10-PIN CONNECTOR (J2) PINOUT, for the pinout of this connector.

The Auxiliary Connector (J2) is a 10-pin connector with 0.1 inch pin spacing. Most standard 10-pin cable/ribbon connectors will mate properly; AMP connectors as used by DEC on the DLV11 (serial line interface boards) are suitable as well as 3M type ribbon connectors. Viewed from the front of the connector (i.e. looking at the handle end of the board), pin 1 is the upper right corner, pin 2 the lower right, pin 9 the upper left and pin 10 the lower left corner.

The 32,768 Hz signal on pin 2 is present only when the primary +5 volt board power is present.

Pins 3 and 5 provide system supply +5 volts and +12 volts for use by external devices such as oscillators and displays. These power sources are not implemented in factory configurations. The customer may implement these voltages by inserting two 0.5 amp Pico fuses on the Q-Timer board (F1 and F2 as shown in the Section III, Figure 1, and adding a single jumper on the +12 volt line (also shown in Figure 4; jumper the +12x to the x+12). The Pico fuses are available on request from CODAR Technology. An external 32,768 HZ signal can be supplied by the customer on pin 4 (a jumper change on the board is required - see the LINE TIME CLOCK section of this manual). This allows the use of an extremely stable reference if required. This signal must track the Q-Timer power supply voltages in amplitude. Contact CTI engineering for assistance if required.

Pin 6 can be used for a customer-supplied (customer-desired frequency) LTC BEVNT signal. This function must be implemented in conjunction with jumper changes as discussed in the LINE TIME CLOCK section of this manual.

The clock signal on pin 8 is a CMOS level which will vary in amplitude with the power source which normally runs at +5 volts; 3.9 volts when on battery backup. A 150 Kohm series resistor prevents excessive loading or power consumption. This signal is normally used for measuring and setting the frequency of the CMOS oscillator which drives the Q-Timer Calendar Clock and, under the STANDARD configuration, the LTC function. Pin 8 is driven from a CMOS gate with on-board battery backup, thus this signal is present even when the board does not have primary power.

Pin 9 is the 1.0 MHz logic clock signal. This provides a convenient means for setting the correct frequency. As this oscillator will not normally require adjustment, pin 9 should be considered a factory test point only.

BUS TERMINATION BY THE Q-TIMER:

The Q-Timer provides removable line terminating resistors which may be used for terminating the Q-Bus in a 120 ohm impedance. The terminating resistors are contained in three socketed DIP packages, U20, U32, and U36 and are fully interchangeable with each other. See Section III, Figure 1, for their location.

The Q-Timer is normally shipped with the three DIP terminating resistors installed. The customer should either verify that no other terminating resistors are present on the Q-Bus or remove the three Q-Timer terminating packs. The Q-Bus must not be double terminated! A double bus termination will typically cause the system either not to function or to behave in a very erratic fashion.

For proper bus termination, the Q-Timer should be placed in the slot at which the bus lines end. On most backplanes this is the slot directly to the right of the CPU. (If the terminating function is not implemented, the Q-Timer can be placed in any available Q-Bus system slot.) The two LSI-11 bus serial priority lines are jumpered through the Q-Timer board thus insuring proper operation of the Q-Bus interrupt structure regardless of Q-Timer placement. (The Q-Timer will not function in the C-D backplane slots which were implemented on earlier DEC backplanes in support of the RL disk controller).

LED/SWITCH PANEL (TEST PLUG) USE:

This miniature display / switch board plugs directly onto the Parallel Port (34-Pin Connector). It contains 8 LED's for binary readout of data written to the port, and an 8-position DIP switch for manual entry of binary data to be read from the port.

Each LED corresponds to a single bit in the parallel port 8-bit output word. Writing a "1" to a bit will cause the appropriate LED to light. As the output port is latched, the bit will remain illuminated until a "0" is written to the appropriate bit.

The DIP switch settings may be read by accessing the Parallel Input Port.

The test plug does not differentiate among the 16 possible input or output addresses. Thus, LED #0 will light regardless of which of the 16 possible output addresses a logic "1" is written to in bit position "0". The same applies for reading the input switch. Bit "0" for both the LED's and the DIP switch is on the right side of the test plug when viewing the test plug. Bit "7" is on the far left.

ON-BOARD RECHARGEABLE BATTERIES:

The CMOS Calendar Clock and CMOS RAM are backed up by an on-board rechargeable Ni-Cad battery pack. When the primary LSI-11 +5 volt supply drops, the CMOS devices are automatically connected to the Ni-Cad power without interruption or loss of data. The Ni-Cad's are automatically recharged when the LSI-11 +5 volt power is present. The batteries require 17 hours to fully recharge from a completely discharged condition. The batteries are fully charged during manufacturing of the Q-Timer; due to shipping delays however, some self-discharge may occur prior to delivery to the customer.

When fully charged, the batteries will maintain the CMOS devices in an operational state for a minimum of 60 days without primary board power (typical battery backup life is in excess of 75 days). The Q-Timer Ni-cad's are special high temperature devices designed specifically for low current

float charge applications and can be expected to provide a service life of 3 to 5 years.

The Q-Timer batteries will not be damaged by long periods in a discharged condition or by continuous float charging. The primary factor in shortening the battery life is high temperature. The batteries do not suffer from many of the problems, including short life, associated with flat button cells which are frequently used in CMOS applications. It is not recommended that spare battery packs be purchased (until needed) as the total battery life starts at the time of battery manufacture.

The Q-Timer Ni-Cad battery pack consists of three cells connected in series. Each cell is normally rated at +1.2 volts. After extended charging, the cell voltage will approach +1.3 volts resulting in a pack voltage of approximately +3.9 volts; each cell is considered discharged at +1.1 volts (+3.3 volts for a pack). Any "fully charged" battery pack measuring in the vicinity of +2.6 volts should be considered suspect for a dead cell. The Q-Timer CMOS Clock, oscillator, and RAM will function with voltages as low as +3.1 volts worst-case, +2.4 volts typical.

An external battery may be connected via the 10-Pin Auxiliary Connector J2. The external battery voltage should not exceed +5.25 volts, since at that point the external battery will simply discharge into the LSI-11 +5 volt power supply. Additionally, the current consumption of the CMOS devices increases very rapidly in the power-down mode with increasing battery voltage. Thus high backup voltages may be self-defeating.

The Q-Timer current consumption in the battery back-up mode is approximately 45 microamps. This current consumption is best measured using a DVM to measure the voltage across the 68 ohm resistor, R14. See Section III, Figure 1, for component locations.

WARRANTY

Document # 130-0104-00

Codar Technology Inc. (hereinafer referred to as "CTI"), warrants the "Q-Timer" to be free from defective material or workmanship for a period of 6 months from the date of shipment from Longmont, Colorado, USA. This Warranty applies to the original Purchaser only and may not be transferred without the written permission of CTI. CTI under this Warranty is limited to repairing or replacing the defective product components which, in CTI's judgment, shall have been originally defective or to have failed in normal operation during the warranty period. Disposable items, such as batteries, fuses, etc., are not covered by this Warranty.

The CTI Equipment must be returned to the factory (Longmont, Colorado, USA) with a Return Material Authorization (RMA) number telephonically obtained from CTI, within 6 months from the date of original shipment from Longmont, Colorado, USA. The Purchaser shall prepay shipping charges to CTI and CTI shall pay shipping charges to return the product to Purchaser. However, Purchaser shall pay all shipping charges, duties, and taxes for Equipment returned to CTI from another country.

CTI warrants that its software and firmware designated by CTI for use with or on a piece of equipment, will execute its programming instructions when properly installed on that piece of equipment. CTI does not warrant that the operation of the piece of equipment, or software, or firmware will be uninterrupted or completely error free.

This Warranty shall not apply to any damage or defect caused by injuries received in shipment, or any defects or failure resulting from accident, misuse, improper or inadequate maintenance by Purchaser, Purchaser-supplied software or firmware or interfacing, modifications or connections or installations or adjustments contrary to instructions furnished by CTI in writing, unauthorized repairs, operation outside of the environmental specifications for the Equipment, or exposure to corrosive environments.

This Warranty does not apply to, nor does CTI assume any liability for, the use of the Equipment in any life support application.

CTI shall not be liable for any direct, indirect, special, incidental, or consequential damages, whether based on contract, tort, or any other legal theory.

No other warranty is expressed or implied. CTI specifically disclaims the implied warranties of merchantability and fitness for a particular purpose.

This Warranty is in lieu of all other representations or warranties expressed or implied and no agent or representative of CTI is authorized to assume any other obligations in connection with the sale and purchase of this Equipment.

ERRATA SHEET
