COLEX

68000

FEATURES

- ☐ Powerful 68000 Processor
- ☐ 32-bit Data Registers
- ☐ 56 Instruction Types
- ☐ Operations on Five Main Data Types
- ☐ 14 Addressing Modes
- ☐ 16 Mbyte Direct Addressing
- ☐ STD-68K Bus Compatible
- ☐ Supports STD-Z80 Peripherals
- ☐ USER/SUPERVISOR Mode Supported
- ☐ 256 Vectored Interrupts Available
- ☐ 2K/4K x 8 EPROM Socket
- ☐ STD-Z80 Memory REFRESH Timing Provided
- ☐ STD-Z80 Vectored Interrupts Supported
- ☐ STD-Z80 DMA's Supported
- ☐ 4 MHz or 8 MHz Operation
- ☐ +5 Volt Only Required
- ☐ 1 Year Warranty

DESCRIPTION

The Colex STD-68000 is a high performance, 16-bit 68000 CPU designed to interface with the STD-Z80 or STD-68K Bus. Systems integrators requiring 16-bit power on the STD Bus while retaining STD-Z80 interrupt compatibility need this card. While it is fully Z80 STD Bus compatible, the 68K CPU does not restrict the user to limited 8-bit processing capabilities.

STD-Z80 COMPATIBILITY

The STD-68000 card contains an on-board microsequencer that translates the 68000 processors' signals to STD-68K and STD-Z80 levels. The sequencer provides resolution of byte high, byte low, full word and long word memory data access. It generates the

STD-68000

extended (24-bit) addresses and bank select scheme. Furthermore, it emulates Z80 interrupt timing and is STD-Z80 memory compatible which allows use of STD-Z80 dynamic RAM cards.

DIRECT MEMORY ADDRESSING

Direct memory addressing to 16 megabytes is possible. The last 2 megabytes are set aside for the I/O page by the CPU. The STD address bus is a 16-bit, 3-state, high level active bus. It is extended to 24 bits for a 16 megabyte address space by using the data bus during Memory Fetch Operations. The upper 8 bits (A16 through A23) are asserted and latched onto memory cards by the rising edge of MCSYNC*. The

COLEX STD-256DRAM is compatible with this direct addressing scheme. For memory cards that don't decode these upper 8 bits, the addressing mode is transparent and limited to a 64K byte memory page.

An 8-bit memory REFRESH* is provided by the STD-68000 card. This allows support of STD-68K and STD-Z80 type dynamic RAM memory cards. The REFRESH* addressing is supplied on the lower 8 address bus lines. The REFRESH* occurs after the first 8-bit fetch of any 16-bit word.

SUPERVISOR/USER STATE

The STD-68000 card can operate in either of two states: USER or SUPERVISOR. The USER mode prevents the execution of certain instructions or processes. The SUPERVISOR mode has control over the execution of all instructions. The SUPERVISOR/USER bit, signal FC2, from the Processor Status Word is buffered and output on MEMEX to the STD Bus. The signal is active high whenever the processor is in the SUPERVISOR mode and low in the USER mode. The COLEX STD-256DRAM board uses this signal. When USER mode is decoded, a hardware lockout is generated preventing access to the lower 128K bytes of memory. In SUPERVISOR mode, all the memory is accessible.

Note: If MEMEX is grounded on the motherboard, the ground strap should be removed to enable this function.

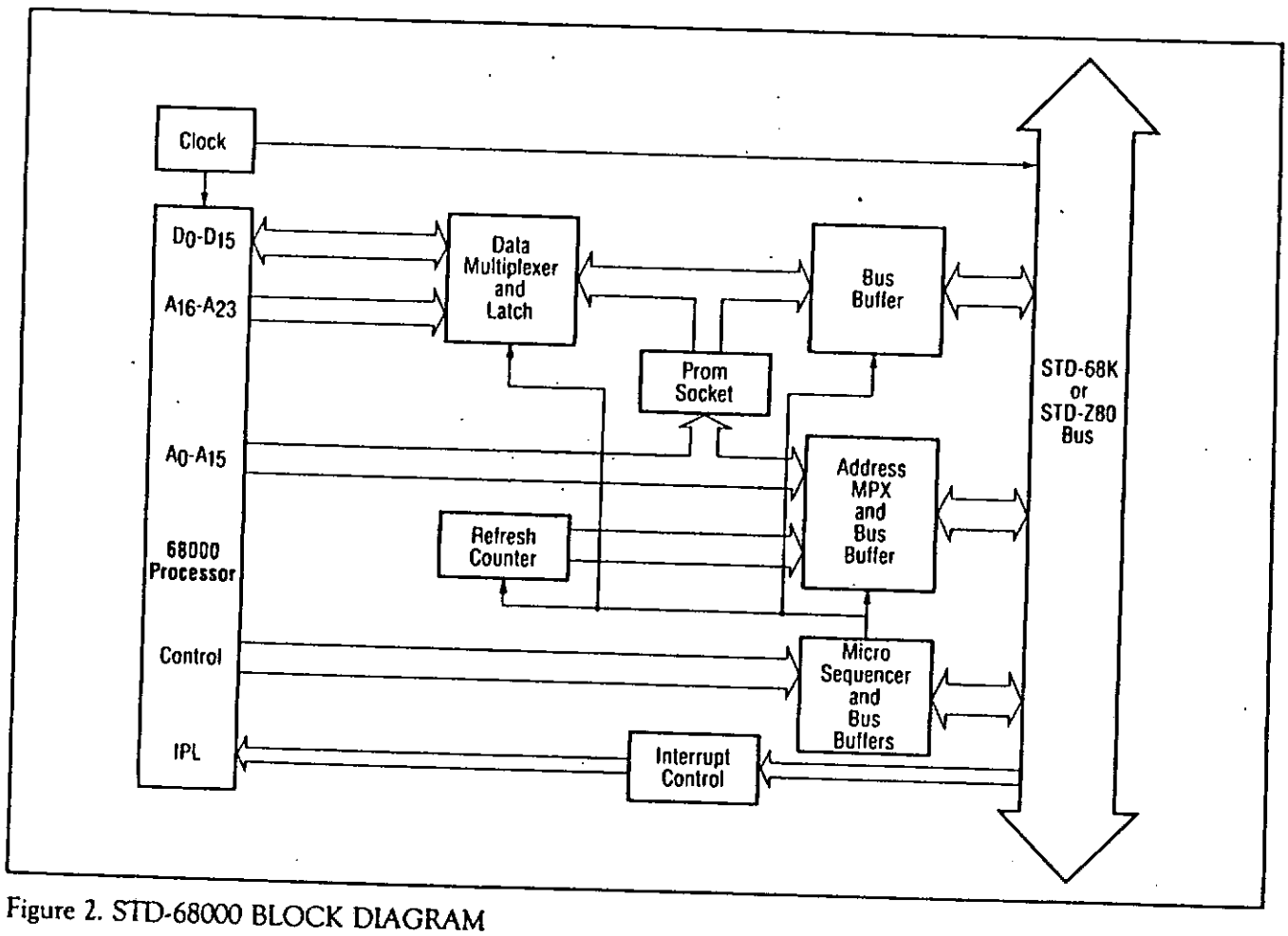


Figure 2. STD-68000 BLOCK DIAGRAM

I/O ADDRESSING

I/O addressing only occurs during the I/O page memory operation. The I/O page is defined as processor addresses between the ranges of E00000 and FFFFFF hexadecimal. STD-Z80 compatible I/O timing is used for memory locations E00000 through EFFFFF hexadecimal. STD-6800 I/O timing is used for memory locations F00000 through FFFFFF hexadecimal. The STD-68000 can support vectored STD-Z80 interrupts from up to 128 I/O devices. Mapping STD-Z80 peripherals to the STD-68000 requires matching the card's I/O address with the lower address byte of the 68000 I/O address.

For example, the 68000 I/O address of E000A8 would support an 8-bit peripheral card with an I/O address $A8_H$. The upper bytes (A9 through A24) are decoded by the microsequencer to differentiate between a memory or I/O operation. The lower address bytes are continuously decoded within the Z80 memory map. The Z80 and other I/O cards will ignore the upper addresses and the ports will appear every 256 bytes in the I/O page. Therefore, an address of E000A8, E001A8, E002A8, etc., would all generate a valid I/O address for I/O port address $A8_H$.

The STD-68000 card emulates the correct M1* and IORQ* signals to completely support the Z80 interrupt structure. The software must issue the ED 4D command to clear interrupt flag in the interrupting Z80 peripheral chip. It can also support STD-6800 nonvectored interrupts; however, this requires a terminated backplane.

PROM SOCKET

One socket is provided to support a 2716/2732 type EPROM for bootstrap or diagnostics operations, and is designed to phantom out of the memory map. It is selected by a RESET instruction, a bus SYSRESET*, or PBRESET and is deselected upon the first I/O request cycle. This is generated by issuing any memory reference to the I/O page. The socket is only used by memory read cycles. The first sequence of instructions should copy the RAM by reading and writing each memory location until the program is copied to RAM. Any subsequent instruction referencing the I/O page will phantom the EPROM from the memory map.

The STD-68000 is configured from the factory to accept a 2716 2Kx8 +5 volt only EPROM. This is enabled by a jumper between pin pair 1 and 2 of J2. A 2732 4Kx8 EPROM will also be accepted in the socket by jumpering pin pair 3 and 4 of J2. The logic table is below.

Pin Pair 1-2	Pin Pair 3-4	Comments
Jumper	No Jumper	2716 Support: Shipped in this configuration
No Jumper	Jumper	2732 Support

Figure 3. J2 Jumper Configuration

PROGRAMMING CONSIDERATIONS

The 68000 has a 32-bit internal structure. When using the 8-bit STD-Z80 Bus special program considerations are required. This is caused primarily by the way the STD-Z80 Bus handles interrupts. The 68000 has 7 different interrupt levels, and the STD-Z80 Bus only handles two. The STD-68000 uses 2 interrupt levels. Level 1 is for maskable interrupts (INTRQ*) and level 7 (the highest) is for nonmaskable (NMIRQ*) interrupts. The 68000 CPU will process any interrupt with priorities equal to or higher than the current interrupt mask.

If Z80 peripheral devices such as the SIO, CTC, PIO, or DMA are used, then particular attention must be given to the return from interrupt sequence. Z80 peripheral devices require that they decode an ED 4D instruction being fetched from memory when M1* is asserted. The peripheral then acknowledges the interrupt and internally resets the request flag.

This is simply done by issuing the following command after an interrupt:

LSL.W #6,D5 : Issue an ED4D command to acknowledge an interrupt request.

The Z80, SIO, PIO, DMA, SCC and CIO peripheral chips contain a bit that generates a Return from Interrupt. These peripherals respond to the bit in the same manner as the ED 4D instruction sequence. This

can be used as an alternative method for clearing an interrupt request. Refer to their respective technical manuals for operational details.

One should be careful in accessing the I/O pages with 8-bit instructions such as BSET, BCLR or any that do a read-modify-write operation should be avoided. This is due to the fact that some peripheral devices do not have a readback on the bits. Issuing these instructions will yield erroneous results. The @(An) addressing mode is useful for byte operations on an odd memory boundary, and may be used for I/O operations on 1-, 8-, 16- or 32-bit I/O devices occupying consecutive physical addresses.

REFRESH

The 68000 STOP instruction will inhibit the REFRESH from occuring and will cause the loss of dynamic RAM. This is unlike the Z80 microprocessor HALT instruction. This instruction should be avoided when using dynamic RAM cards that require refresh generated from the CPU card.

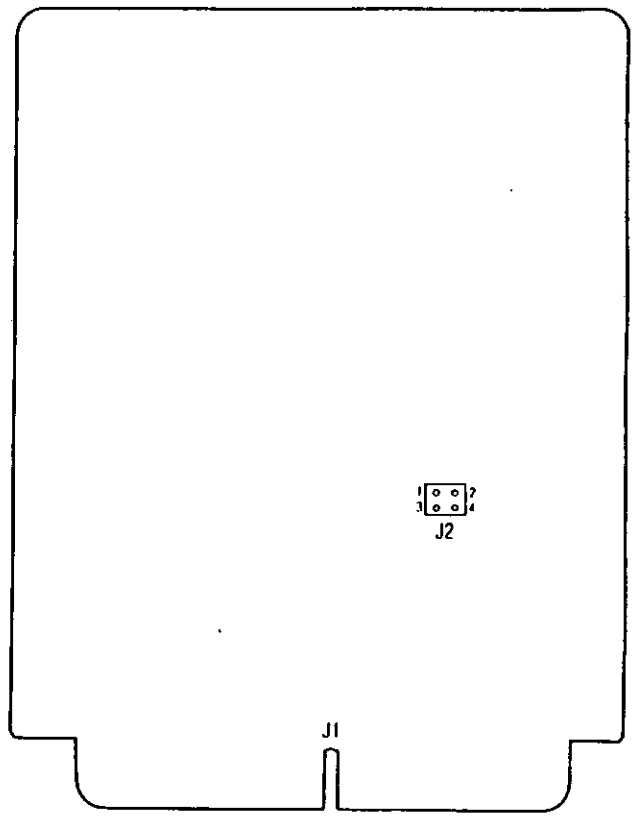


Figure 4. STD-68000 Header Positions

STD-68000 OPERATING AT 8 MHz

The STD-68000 internal clock runs at 8.0 MHz for the processor; however, the STD Bus System CLOCK* runs at a 4.0 MHz rate. This allows 4 MHz STD cards to work directly with the STD-68000 card with no modification required. The on-board PROM socket must have a device capable of 300ns access time for proper operation.

STD BUS CONNECTOR

J1 The STD Bus pins are buffered and brought out to a 56-pin edge connector as shown.

Signal Name	J1 Pins		Signal Name
+5 V	1	2	+5 V
Ground	3	4	Ground
N.C.	5	6	N.C.
D3/A19	7	8	D7/A23
D2/A18	9	10	D6/A22
D1/A17	11	12	D5/A21
D0/A16	13	14	D4/A20
A7	15	16	A15
A6	17	18	A14
A5	19	20	A13
A4	21	22	A12
A3	23	24	A11
A2	25	26	A10
A1	27	28	A9
A0	29	30	A8
WR*	31	32	RD*
IORQ*	33	34	MEMRQ*
N.C.	35	36	MEMEX
REFRESH*	37	38	MCSYNC*
STATUS 1*	39	40	STATUS 0*
BUSAK*	41	42	BUSRQ*
INTAK*	43	44	INTRQ*
WAITRQ*	45	46	NMIRQ*
SYSRESET*	47	48	PBRESET*
CLOCK*	49	50	CNTRL*
PCO	51	52	PCI
N.C.	53	54	N.C.
N.C.	55	56	N.C.

N.C. = No connection on the STD 68000 card

Figure 5. STD-68000 STD Bus Connector

NOTE: If MEMEX* is grounded on the motherboard, the ground strap should be removed.

SPECIFICATIONS

- ☐ Processor: 68000
- ☐ System Bus: STD-68K, STD-Z80
- ☐ Internal Clock: 4.0 MHz or 8.0 MHz
- ☐ System Clock: 4 MHz
- ☐ Data Bus: 8 bits, bi-directional
- ☐ Address Bus: 16 bits standard wit 8 bits extended (data bus)
- ☐ Signal Loading: Inputs: One 74LS maximum
  Outputs: I_{OH}=+3mA min @ 2.4 volts
  I_{OL}=24mA min @ 0.5 volts
- ☐ Operating Temperature: 0°C to 60°C
- ☐ System Interrupt Units: 0 SIU's
- ☐ EPROM Timing Requirements: 525ns from Address
  @ 4.0 MHz internal clock: 300ns from Output Enable
- ☐ Power Requirements: @ 25°C

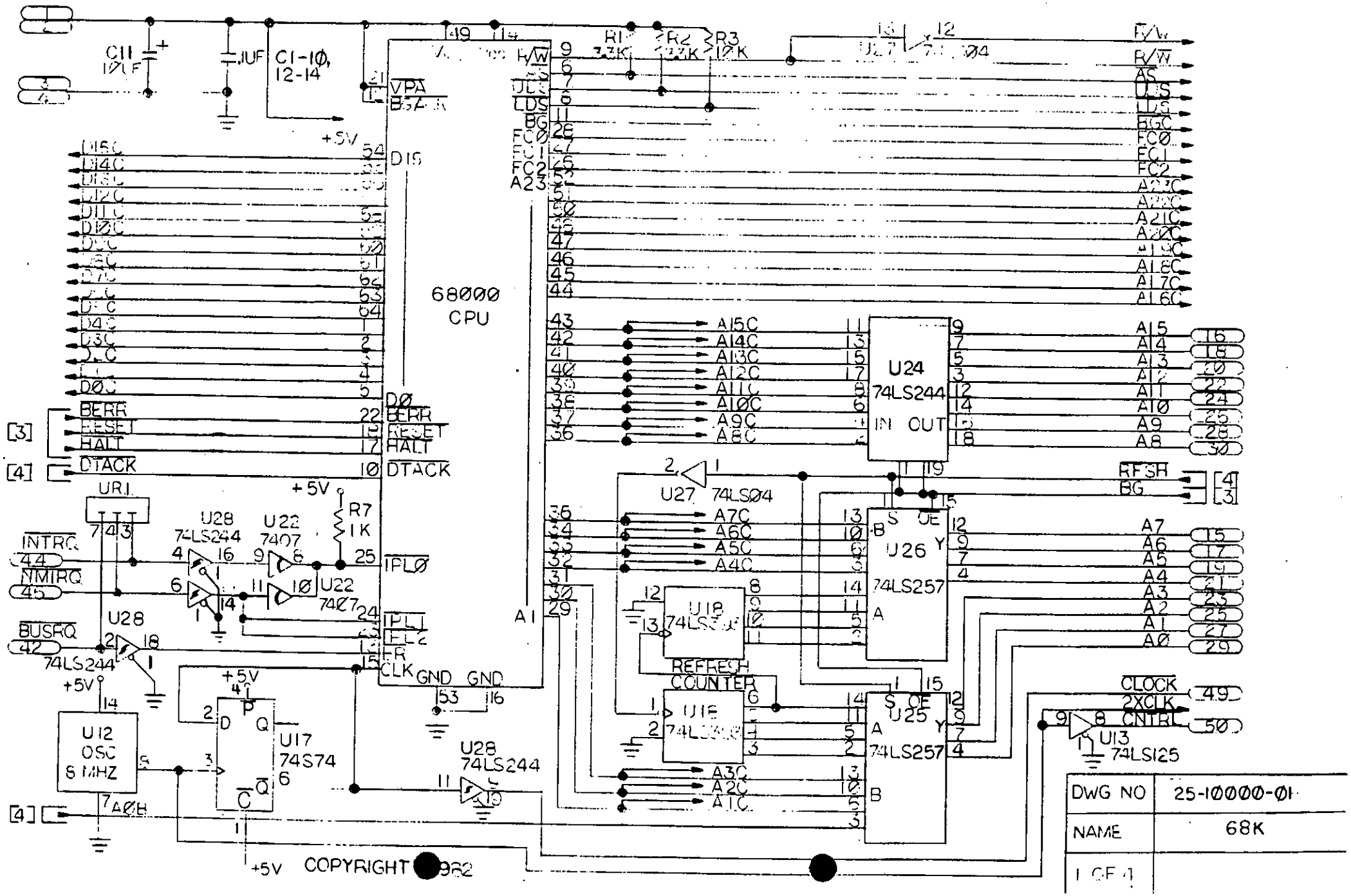
Parameter	Condition	Min.	Typ.	Max	Units
V_{cc}	–	4.75	5.0	5.25	Volts
I_{cc}	@ 5V	–	800	1600	mA

MECHANICAL

- ☐ Card Dimensions:

Form Factor	H	W	L	Units
STD-Bus	0.60	4.5	6.5	inches

- ☐ PC Board Thickness: 0.062 inches
- ☐ Connector: STD Bus (J1): 56-pin dual readout; 0.125 inch centers



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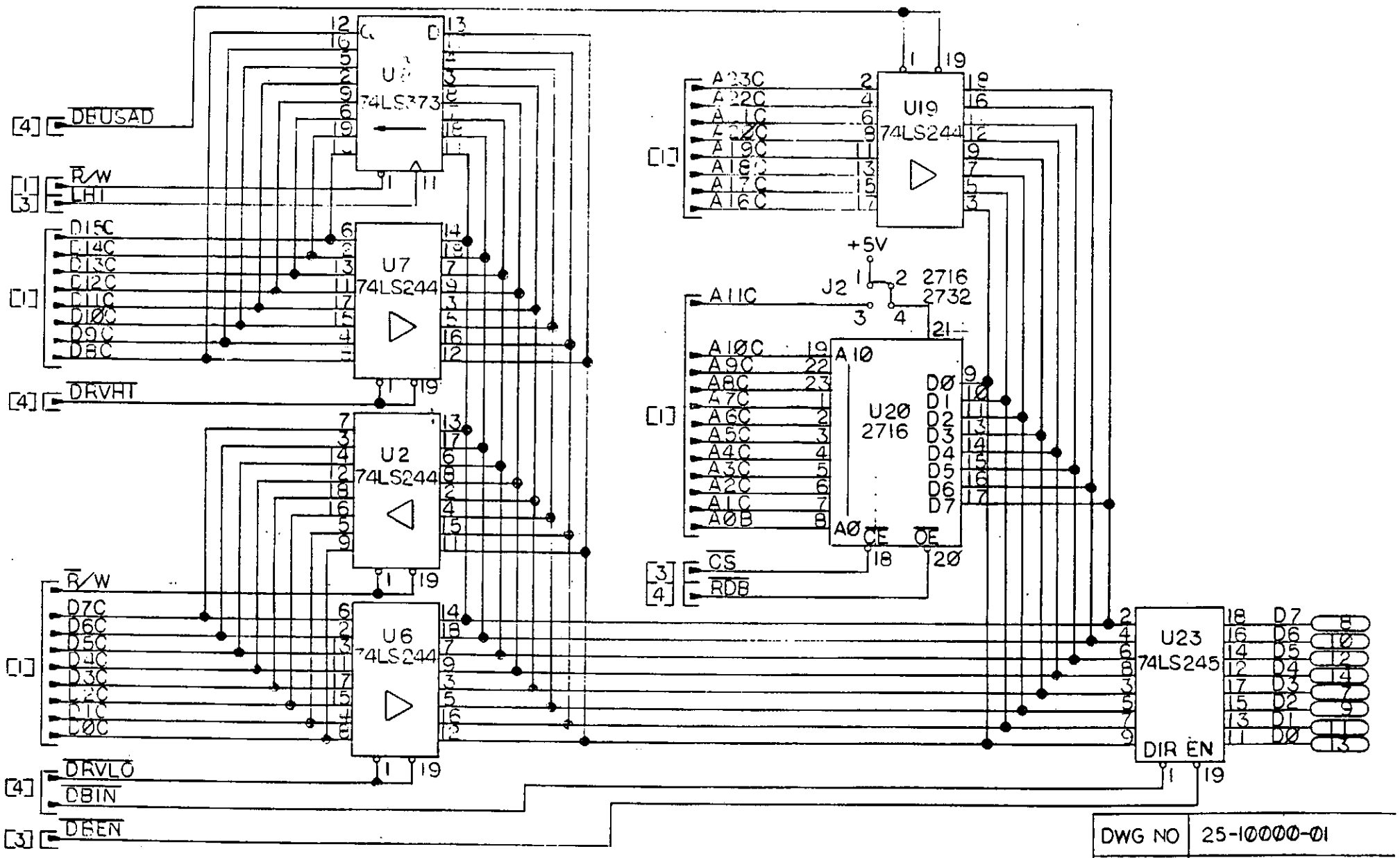
NAME	68K



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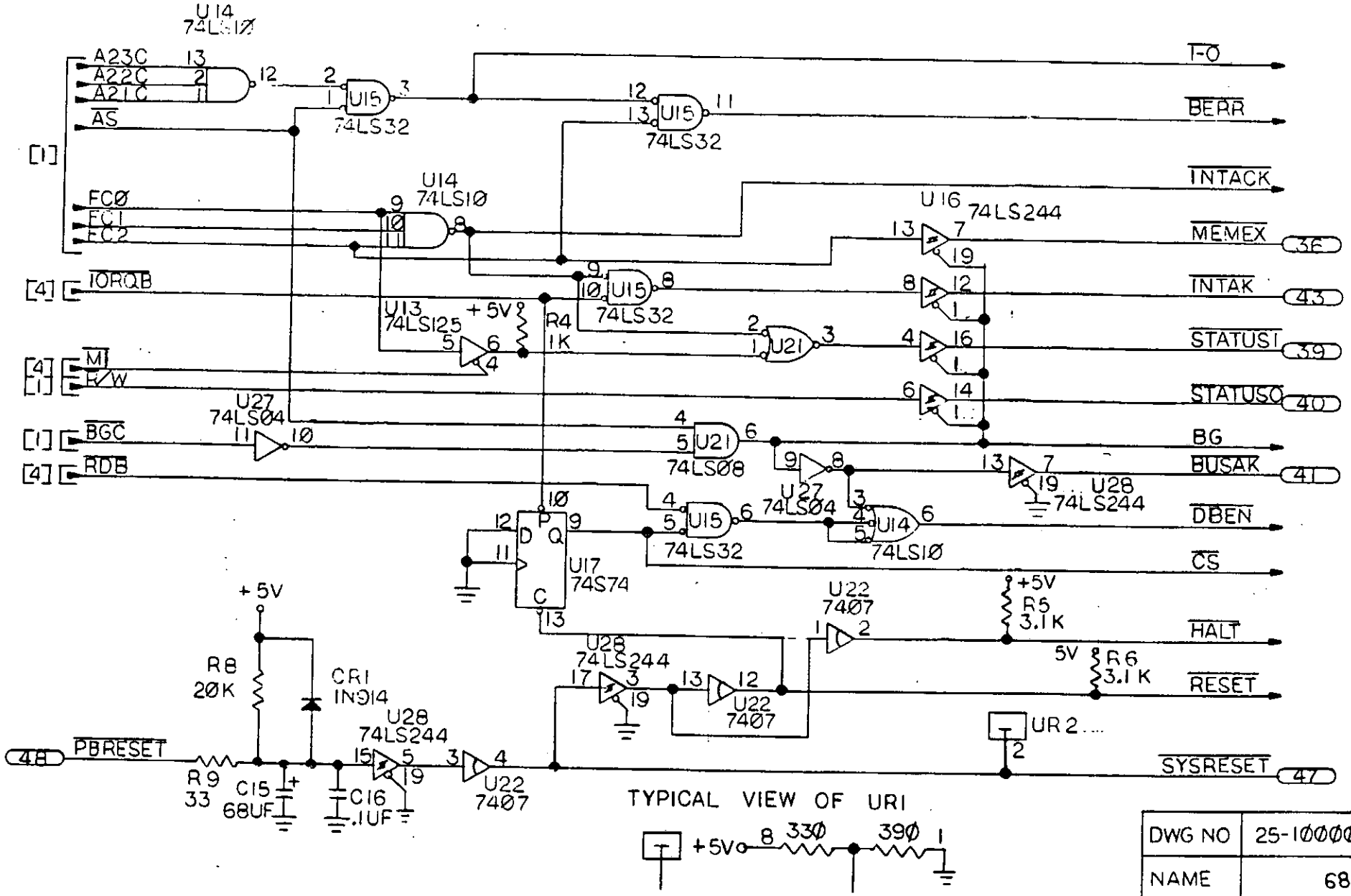
NAME	68K
2 OF 4	



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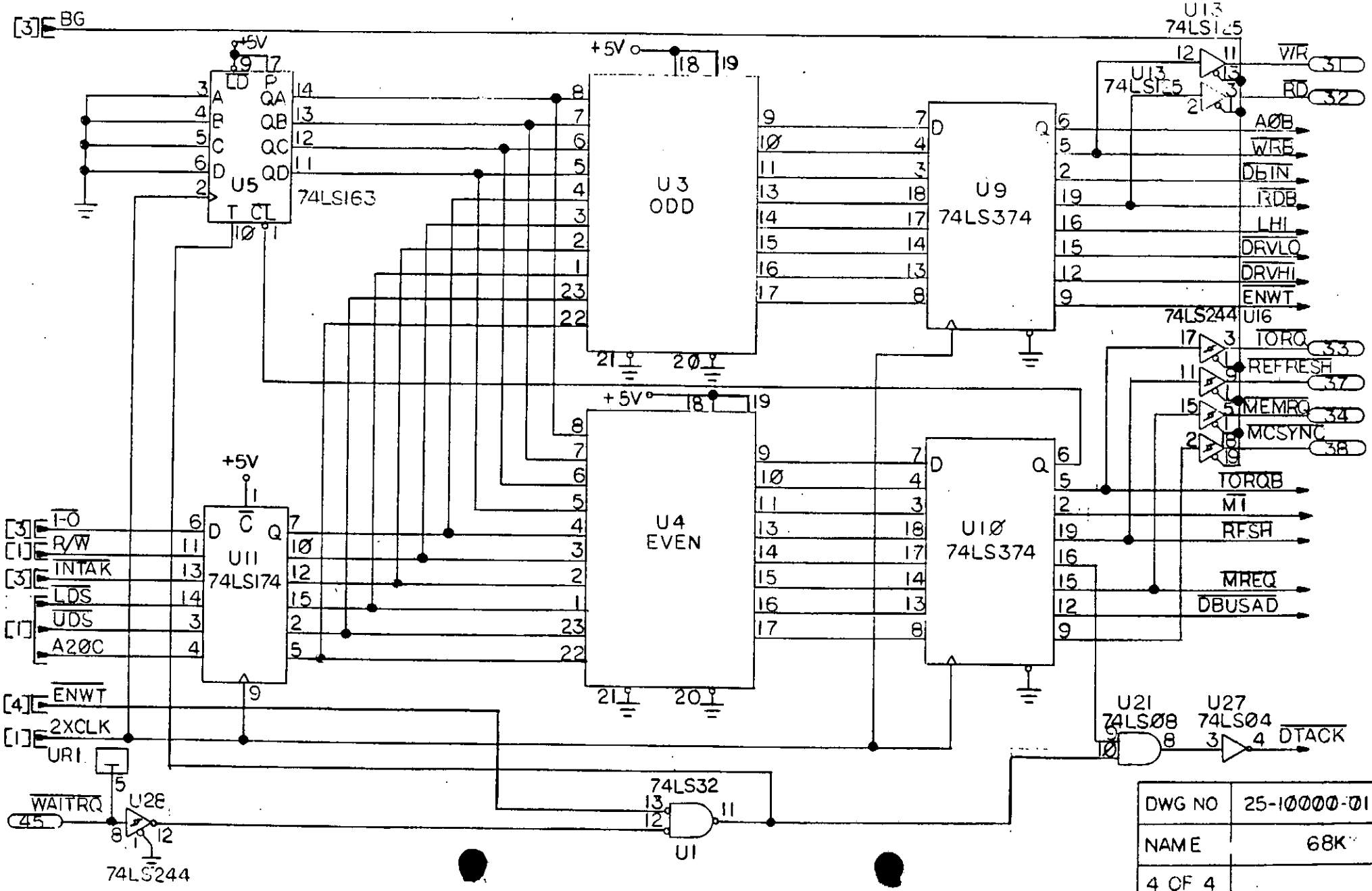
NAME	68K
3 OF 4	


[3] BG
U5
74LS163
U3
ODD
U4
EVEN
U9
74LS374
U10
74LS374
U11
74LS174
U13
74LS125
74LS244
U16
U21
74LS08
U27
74LS04
74LS32
U1
U28
74LS244
WR
RD
AØB
WRB
DBIN
RDB
LHI
DRVLO
DRVHI
ENWT
IORQ
REFRESH
MEMRQ
MCSYNC
IORQB
M1
RFSH
MREQ
DBUSAD
DTACK
I-O
R/W
INTAK
LDS
UDS
A20C
ENWT
2XCLK
UR1
WAITRQ
+5V
DWG NO 25-10000-01
NAME 68K
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