NCR 9800 System

PRODUCT DESCRIPTION

After a long period of silence, NCR finally announced in April a long rumored new mainframe, the 9800 System. The new system is a radical departure from the previous V8500 and V8600 system architecture. The 9800 uses a modular, incremental architecture based on loosely coupled, multiple function-specific processors. The new hardware design and the new VRX/E operating system supporting several fault tolerant features should open the door for NCR to enter the fast growing transaction processing market.

A 9800 system contains at least two processors, one application processor and one data storage processor, a dual-channel interprocessor bus, and related peripheral components all located in the same cabinet. The system can be expanded by adding new processors. Up to eight application processors and up to four data storage processors may be combined for the high-end system 9884. When two or more application processors are present in a system they are loosely coupled, with each application processor using its own copy of the operating system software and running independently of the other application processors in the system. All application processors and data storage processors are interconnected over the interprocessor bus. Each interprocessor bus channel is implemented as a star, with two interprocessor buses and star couplers in all 9800 models. Traffic is normally shared by the two interprocessor buses, but in the event of the failure of one bus, all application processors and data storage processors can communicate over the remaining interprocessor bus.

Multiple processor architecture results in a system that is inherently fault tolerant, assuring a high availability of all computerized functions for business operations. Since fault tolerance is achieved with all system components actively contributing to processing the workload, no part of the

PRODUCT ANNOUNCED: The NCR 9800 System is an incremental-architecture system designed for on-line transaction processing. The modular 9800 System consists of a series of function-specific processors, the application processors and the data storage processors. A system can contain from one to eight application processors and one to four data storage processors. The application processor and storage processor each have from two to four megabytes of memory, up to a total of 48 megabytes. The NCR 9800 is available in seven different configurations and operates under the new operating system, VRX/E.

COMPETITION: Burroughs A 3, A 9; Digital Equipment Corporation 8200, 8300; IBM 4300.

DATE ANNOUNCED: April 22, 1986.

SCHEDULED DELIVERY: Volume shipments of the NCR 9800 will start in the third quarter of 1986.

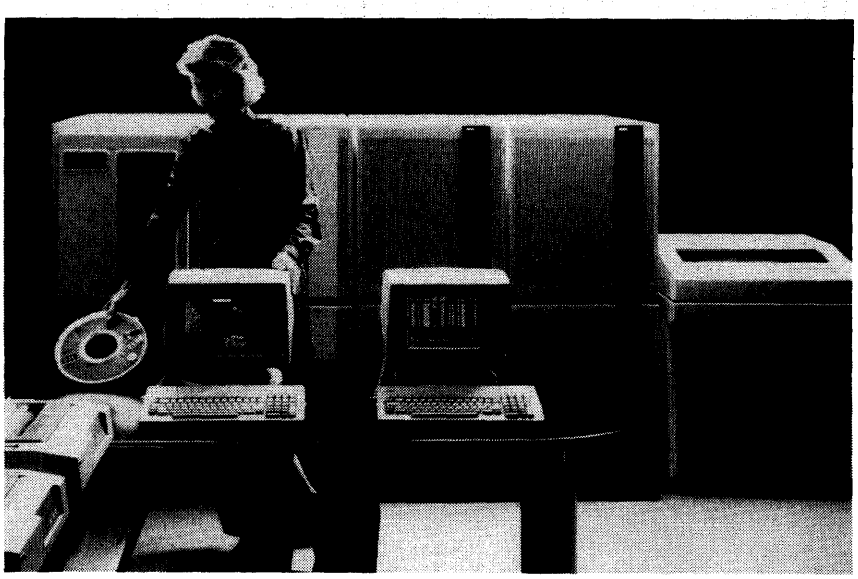
BASIC SPECIFICATIONS

MANUFACTURER: NCR Corporation, 1700 South Patterson Boulevard, Dayton, Ohio 45479. Telephone (513) 445-5000. In Canada: NCR Canada Limited, 117 Eglington Avenue East, Toronto, Ontario M4P 1J1.

MODELS: NCR 9811, 9821, 9832, 9842, 9863, 9884.

CONFIGURATION

The NCR 9800 system architecture comprises multiple, loosely coupled processors interconnected in a network by an interprocessor bus subsystem. System size may vary from a small Model 9811 with one application processor (AP) and one data storage processor (DSP) system to a large Model 9884 with eight applications



The NCR 9800 is an on-line transaction processing system, based on multiple function-specific processors. The 9842 model is a mid-range configuration consisting of four application processors and two data storage processors. Each processor can contain up to 4 megabytes of memory.

NCR 9800 System

system waits unproductively to provide backup in the event of component failure. To further ensure high system availability, the new feature "file mirroring" assures that operation of critical applications can continue despite disk or data storage processor failures. The system automatically maintains exact copies of selected files.

A single console is used to control the entire system, regardless of the configuration size. On-line or batch applications are automatically routed to the proper processor element.

RELATIONSHIP TO CURRENT PRODUCT LINE: The 9800 system is compatible on the object level with the V8500 and V8600 systems. The upward-compatible and highly configurable 9800 system will provide an attractive migration path for V8500 and V8600 users. The 9800 system offers a more attractive price/performance factor than these current systems. Fault tolerance, dynamic load balancing, and the VRX/E operating system, including an IBM SQL/DS-compatible relational data base, might also tempt the current user base to migrate to the new system. According to the vendor, the 9800 system will replace the V8500 and will eventually be positioned as a top-end member of the V8000 family.

COMPETITIVE POSITION: The 9800 system will compete with the A 3 and A 9 system from Burroughs in the banking and medical fields where both vendors have traditional strongholds. NCR gives a power range of 0.6 to 4.0 batch processing MIPS (Millions of Instructions per Second) or 1.0 to 8.0 transaction MIPS depending on the number of processors in each configuration. Estimated batch MIPS ratings for the A 3 are 0.6 to 0.9, and 1.9 to 2.5 for the A 9.

As usual, IBM is present in all market sectors and the 9800 system will have the IBM 4300 as a competitor. The main memory capacity of the IBM 4300 ranges from 2 to 32 megabytes, compared to the maximum 48 megabytes of memory for the 9800. And only the 4381 dual-processor systems use multiprocessing with shared storage. Batch MIPS ratings for the 4361 range from 0.3 to 1.1.

The new 8200 and 8300 systems from Digital Equipment have a main memory ranging from 4 to 16 megabytes and are designed for general-purpose business applications. The 8200 system, with a 4-megabyte memory, is priced at $79,000. The 9811 model, with a 4-megabyte memory, costs $41,220. NCR definitely has the price advantage here.

Because of the multiprocessing hardware and software support of several fault tolerant features, the 9800 system will face competition with the fault tolerant vendors Tandem and Stratus. □

PROCESSORS AND MEMORY

APPLICATION PROCESSOR: The Application Processor (AP) is the main transaction processor for the NCR 9800 system. The AP is responsible for instruction execution, internal interrupt handling, and unit I/O operations from both the interprocessor bus and peripherals. The AP supports all system I/O peripherals other than the disks and magnetic tapes containing system memory. Peripherals available for the application processor include fixed and removable disks, printers, magnetic tapes, and communications processors.

The application processor consists of the following components: the processor element board, the system bus adapter/star coupler board, the writable control store board, the trace board, the no-match assist board, and the memory board. The processor element board contains a 155-nanosecond VLSI chip set, a 32-bit processor-to-memory bus, maintenance registers, and related logic circuits. The system bus adapter provides the circuits to transmit and receive the interprocessor communications. The star coupler circuitry receives, repowers, and retransmits these messages to all the processors on the bus. The writable control store board, with 128K-bit RAM memory, stores the firmware microcode as an instruction storage unit. A 16K-bit PROM memory provides the initial power-on load boot and level 0 diagnostics firmware. The trace board is an optional feature providing firmware control register tracing for unit servicing. The no-match assist board services the dynamic address translation 16-entry associative memory register. Each memory board provides 2 megabytes of memory in 64K-bit RAM integrated circuit (IC) packs. Memory access time on a 32-bit boundary is 360 nanoseconds. Memory cycle time is 120 nanoseconds. Each application processor contains one or two memory boards.

DATA STORAGE PROCESSOR: The Data Storage Processor (DSP) is the data file controller processor for system memory. It can support one or two bit-serial disk controllers with up to four fixed disk drives, each for program library and data file storage. The data storage processor firmware runs object instructions, maintains the various task tables, provides call/return routines, services internal and external I/O interrupts including those of the interprocessor bus, and provides a unit interval timer facility and system time-of-day (TOD) clock. Under software control, the DSP maintains file queues and locks, and a one- or three-megabyte cache memory for temporary file storage in local memory. The data storage processor performs all memory addressing in realtime, with the majority of the operating system residing in that portion of local memory not dedicated to the cache. Overlays are called from disk virtual memory to provide software for exception conditions.

The data storage processor hardware construction is similar to that of the application processor, and contains the following components: the processor element board, the system bus adapter/time-of-day board, the writable control store board, the trace board, and the memory board. The processor element board is identical to the one in the application processor. The system bus adapter provides the circuits to transmit and receive the interprocessor communications. The time-of-day circuit portion of the board contains a realtime clock and lithium battery for back-up clock power. The writable control store board and the trace board are also identical to the boards in the application processor. Each memory board provides 2 megabytes of memory in 64K-bit RAM integrated circuit (IC) packs. Memory access time on a 32-bit boundary is 450 nanoseconds. Memory cycle time is 150 nanoseconds. Each data storage processor contains one or two memory boards.

INTERPROCESSOR BUS: The Interprocessor Bus Subsystem (IB) provides intelligent intrasystem communications between processors through a dual-channel serial connection with broadcast capabilities. Each channel of the interprocessor bus subsystem, channel A and channel B, operates independently of the other. Both carry high-speed, bit-serial data between the various units of the system, operating in the full-duplex mode. The interprocessor bus subsystem is composed of two full-duplex, twisted-pair cables to each processor, one or two electrical star coupler boards, each housed in separate application processors, and a system bus adapter board with I/O controller microcode and object code. A 6-

processors and four data storage processors. The last two digits of the model number signify the number of processors in the system. For example, Model 9842 has four APs and two DSPs. Each of the application processors and data storage processors contain from two to four megabytes of memory, for a total of 48 megabytes in a fully configured system with twelve processors.

NCR 9800 System

megabyte bandwidth is achieved for the dual-channel bus through an individual channel transfer rate of three megabytes per second, transmitting at 24 megahertz.

COMMUNICATIONS

The Link Level Communications Subsystem (LLCS) is the integrated communications controller for the 9800 system. A single link level communications subsystem can support up to 18 lines of NCR ISO Async, Bisync, or Data Link Control (DLC) lines, or up to 36 lines for teletype (TTY)-compatible terminals. These lines are interfaced to a single low-speed bit-serial, one-megabit serial line from the processor. The LLCS connects to an application processor through a low-speed link, and handles an aggregate transmission rate of 120K bytes for all its lines. The link level communications subsystem is housed in a communications module, and consists of up to two subsystem control modules, 18 individual line interface boards, and its own power supply and cooling fan.

The link level communications subsystem includes five line module types and two features, including the console line module, the base mode communications line module (BMC), the DLC common carrier secondary line module, the teletype (TTY) line module, the X.25 line module, the backup interface feature, and the line status display feature.

SOFTWARE

The new operating system, the Virtual Resource Executive/Extended (VRX/E), supports object code compatibility from the V8500 and 8600 systems. It maintains the same process and management disciplines as in the VRX. Interprocess management is new and is carried out over the interprocessor bus, using locks and queues in system memory. New capabilities in VRX/E include transparent interhost, interprocess communications, interhost file sharing, interhost communications support, and the synchronization and message handling provided by the interprocessor bus protocols and the system memory mechanism.

The Record Management System (RMS) is a new component of the VRX/E and executes each application processor. RMS provides Cobol 74 sequential, relative, and indexed access methods, and supports the V8500, V8600 CAM (Criterion Access Method). File interleaving, mirroring, and write-through options are specified via a file control language, and are supported by RMS. File sharing among multiple applications processors is supported by page-level locking in system memory.

The System Telecommunications Access Method (STAM) is also a new component of the VRX/E. STAM allows terminals to access applications in application processors they are not connected to, by creating links through data storage processors. Applications communicate with STAM via Cobol Enable/Disable, Send/Receive primitives.

Multi-Tran (MT) is a new transaction monitor for the 9800 system architecture. MT supports transaction distribution and load leveling; and also offers walk-through screen menus, security and validation checking, debugging tools, and utilities. Multi-Tran consists of a terminal manager job (TMJ) and an applications manager job (AMJ). The AMJ is a multithreaded monitor serving multiple terminals.

The new DBSR/SQL relational query/update access system provides an SQL/DS IBM-compatible interface. The DBSR kernel, which contains the relational table management, can be linked with a Multi-Tran AMJ, or to any user application. In addition to data management/definition languages, NCR supports a data control language for defining security and a data dictionary.

VRX/E supports SNA and X.25. Systems running under VRX/E support SNA and non-SNA terminals, and can participate as host in an SNA network.

Among the high-level programming languages supported by the VRX/E are Cobol, NEATVS, C, and IVS Basic.

PRICING

The basic NCR 9811 two-processor system includes one application processor, one data storage processor, two megabytes of memory in each processor, the VRX/E operating system software, and a system console. The purchase price for this system is $41,220. The high-end system NCR 9884 is priced at $340,508, and includes eight application processors, four data storage processors, four megabytes of memory in each processor, the VRX/E operating system software, and two system consoles. ■