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SECTION 1   TECHNICAL DESCRIPTION

1.1 GENERAL DESCRIPTION

The RL01/RL02 Disk Drive is a random access mass storage device. Both drives utilize a removable, single platter top-loading disk cartridge. The RL01K cartridge provides five million bytes of storage, and the RL02K cartridge will hold ten million bytes. Up to four RL01 or RL02 Disk Drives may be used per controller to provide up to 40 million bytes of storage for PDP-8, PDP-11, and LSI-11 computer system applications.

The RL01/RL02 Disk Drive (Figure 1-1) is mounted on slides and is 26.6 cm (10.5 in) high, 63.5 cm (25 in) deep (compatible in width to a 19 inch RETMA rack) and weighs 34 kg (75 lbs).

Operating controls and indicators plus a removable air filter are located at the front of the drive. Access to the cartridge is provided by a lift-up cover incorporating a safety interlock. All servicing can be achieved from the top of the drive or front or rear of the corporate cabinet.

RL01/RL02 Disk Drives are shipped from the factory as 115 Vac/60 Hertz units. Field change to 230 Vac/50 or 60 Hertz is accomplished by reversing either of two terminal block covers located externally at the rear of the drive. The line cord plug may be cut and replaced with an applicable 230 Vac line plug. The RL01/RL02 Disk Drive is UL listed and CSA certified.

Interlocks are provided where the potential exists for damage to the drive, media, operators, or service personnel.

The RL01/RL02 Disk Drive provides high field performance and maintainability. The drive is designed for easy removal and replacement of logic and electromechanical subassemblies to result in an average replacement time of not more than 15 minutes. Special tools and alignment packs or fixtures are not required for on-site maintenance. Only two adjustments are required under normal service conditions. All logic modules are placed so that they may be accessed without the use of extenders.

1.1.1 Servo-In-Data Concept

Key to the performance of the RL01/RL02 is the servo-in-data concept. The concept allows the derivation of head positioning and track counting information from pulses imbedded within the data track. Each read/write head seeking to a desired track becomes its own servo transducer. Data tracks could conceivably be located within a band anywhere on the recordable disk surface as long asthe positioner does not run out of travel limits. Since the heads seek and center on data tracks, environmental problems related to mechanical drift and tolerances become practically nonexistent. Precise head alignment requiring the use of special fixtures is unnecessary.
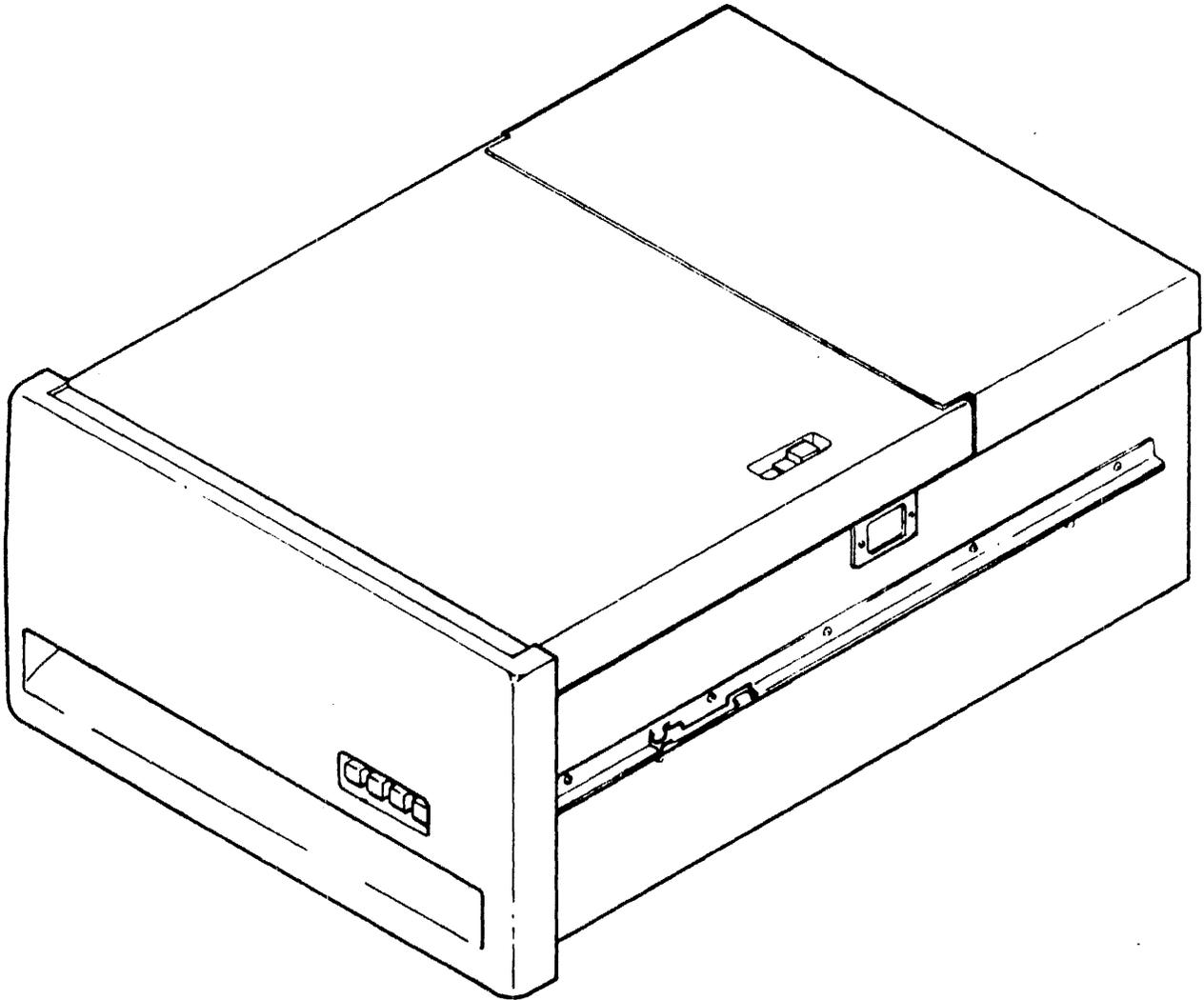
MA-0592

Figure 1-1 Typical Disk Drive

1.1.2 Storage Medium

The RLØ1K or RLØ2K Disk Cartridge is a modified 5440 type removable, top-loading, single platter cartridge with 256 discrete data tracks on each of the two recording surfaces. The cartridge armature plate contains 40 sector slots, defining 40 sectors per track. Servo information (servo-in-data) from which sector and track determinations are made is prerecorded on the cartridge at the factory and cannot be reformatted in the field. Bad sector information is contained on the last data track.

RLØ1K and RLØ2K cartridges are intended as a means of data interchange between computer systems. Data written on one RLØ1 Disk Drive will be readable on any other RLØ1 drive, and the same is true for any two RLØ2 drives, provided that both drives have been properly maintained and that the computer systems and controllers are compatible with respect to word length. Note, however, that an RLØ1K cartridge cannot be used on an RLØ2 drive, nor can an RLØ2K cartridge be used on an RLØ1 drive. While either cartridge will physically fit into either drive, the results of using the wrong cartridge are unpredictable. The cartridge are color keyed and labeled to help prevent incorrect use.

1.1.3 Mechanical Partitioning

Figure 1-2 shows location of the major drive subassemblies and air flow through the drive chassis.

1.1.3.1 Air Flow System – The RLØ1/RLØ2 Disk Drive is designed to achieve maximum protection of the head/disk interface even in a contaminated environment. The air flow system (Figure 1-2) is separated into a recirculating clean air supply and a cooling air supply. The cooling air is drawn in through the bezel and is exhausted out the rear of the drive by a muffin fan. The recirculating clean air is moved through the duct system by an impeller attached to the spindle drive motor. Before the clean air is recirculated to the disk cartridge, the duct system routes it through a high efficiency filter and a heat exchanger. The heat exchanger is cooled by the cooling air supply.

1.1.3.2 Air Filter – The absolute air filter is a self-contained throwaway unit. Because of the two air systems, replacement of the absolute filter is only required on a yearly basis.

1.1.3.3 Positioner Assembly – The positioner assembly consists of a carriage, servo motor with capstan and tension cable, linear tachometer, head load cam, and home switch. The magnetic read/write heads are mounted on the carriage. Figure 1-3 illustrates the principle components of the positioner assembly. The positioner subplate can be moved laterally to align head access radially to the disk.

SPINDLE MOTOR

POSITIONER

DC SERVO BOARD

POWER PANEL

COOLING AIR FLOW

SPINDLE

BASEPLATE AND SHEET METAL CHASSIS

CLEAN AIR SEAL

CLEAN AIR FLOW

DUCTING OF COOLING AIR INTAKE IN BEZEL

CABLE TO OPERATOR PANEL
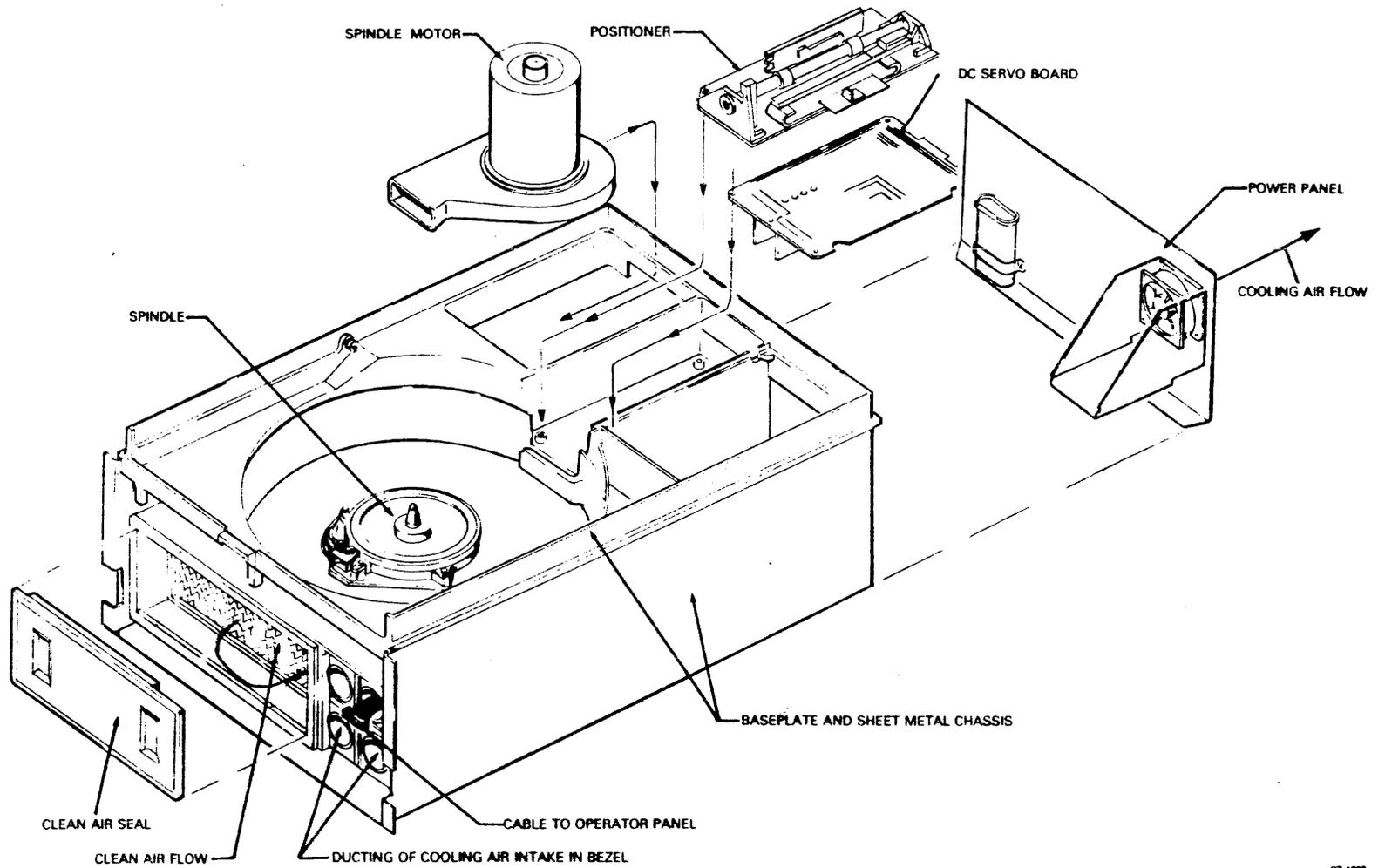
CZ-1000

Figure 1-2 Major Subassemblies and Air Flow

THESE 2 SCREWS ARE
NEAREST THE MOTOR
SHAFT AND ARE THE LONGEST
OF THE SIX MOUNTING
SCREWS.

HEADS HOME SWITCH
ADJUSTING SCREW

POSITIONER
ADJUSTING
SLOT

POSITIONER
ADJUSTING SLOT

CZ-1079
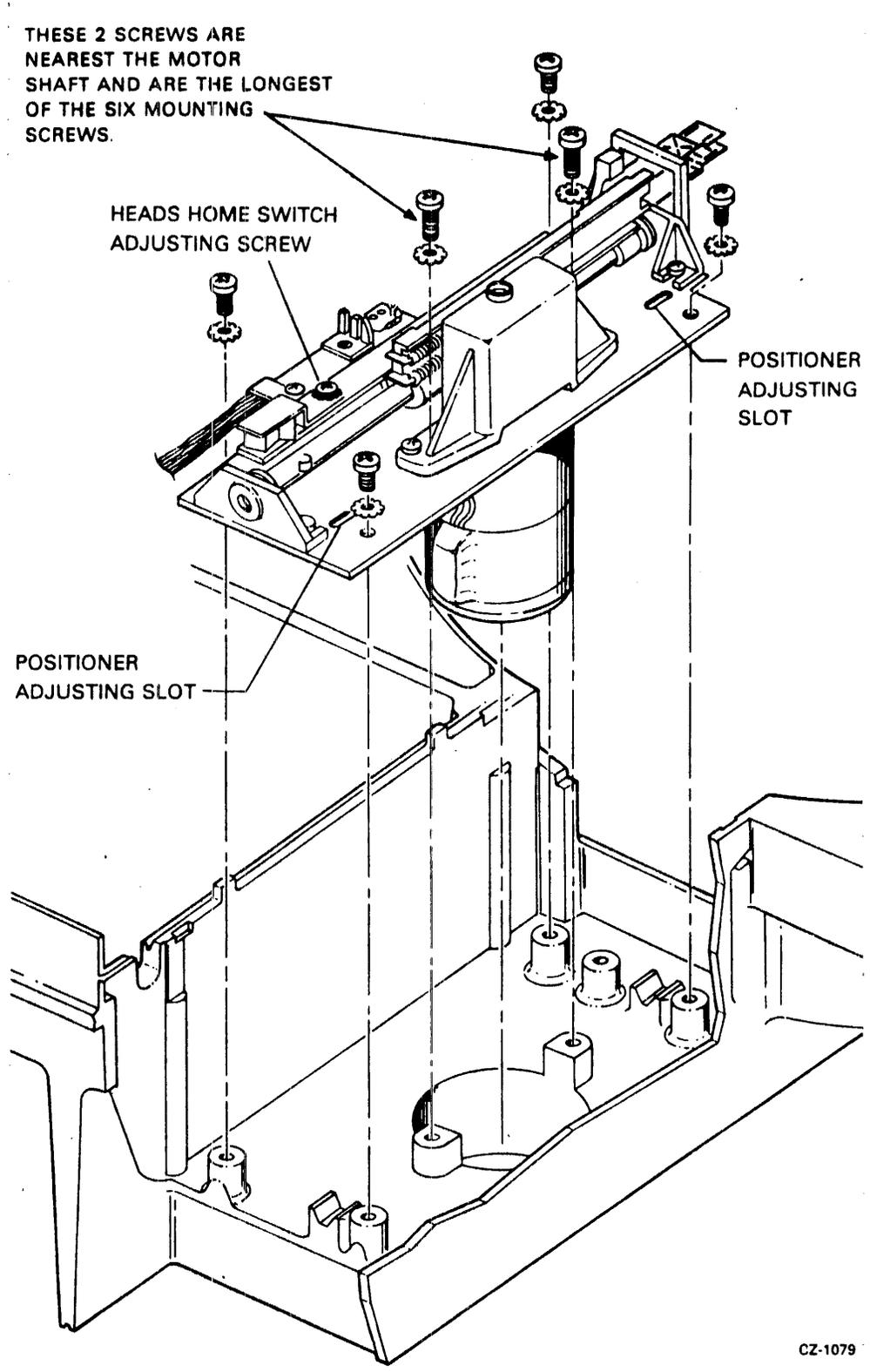
Figure 1-3 Positioner Assembly

I/1-5

1.1.3.4   Spindle Assembly - The Spindle Assembly comprises a
housing, the rotating cartridge interface hub, the spindle ground
button, and the drive belt.   Figure 1-4 shows the Spindle
Assembly.

The sector transducer mounts and aligns itself on the spindle
housing.

The disk cartridge interfaces the spindle via a cone located in
the center of the spindle, a 14.0 cm (5.5 in) diameter stabilizing
hub, and a hold-down magnet.

1.1.3.5   Brush Drive Assembly - The RL01/RL02 Disk Drive has
motor-driven cleaning brushes (refer to Figure 1-5) which
automatically sweep across the disk surfaces each time the spindle
drive motor is started. The brush cycle must be completed and the
brushes retracted before the heads will load. In order to prevent
damage to the read/write heads and cartridge, the cartridge access
cover remains interlocked so that the cartridge cannot be removed
in the event that the brushes fail to return to their home
position. The brush holder assembly is a field replaceable unit.

1.1.3.6   Read/Write Heads - Each head (Figure 1-6) is made up of
a magnetic core structure mounted in a ceramic slider pad and is
supported on an arm. Each head is also provided with a flexible
cable that terminates with a connector. When both heads are
loaded and positioned with the disk rotating at 2400 | 2% rpm,
each head is supported by a boundary layer of air approximately 50
microinches thick. The "up" head is used for reading and writing
data on the bottom surface (surface 1) of the disk and the "down"
head is used for reading and writing data on the top surface
(surface 0) of the disk. Each head is loaded and unloaded from
the rotating disk by the force of a cam against the 30 degree ramp
in the head arm.

The heads operate at 4.1 megaflux-reversals per second maximum
using the Modified Frequency Modulation (MFM) method for encoding
or decoding data. This corresponds to a maximum density of 3725
bits per inch on the inner track (track 255, decimal).

1.1.3.7   Read/Write Board - The read/write board is contained in
a subchassis to provide shielding for the logic.

1.1.3.8   Power Panel - The removable rear panel of the drive
contains a muffin type fan, I/O connectors, an ac circuit breaker,
an RFI filter, the spindle motor capacitor, the ac terminal
assembly block and the ac servo module chassis. Refer to Figure
1-7. The ac circuit breaker provides power ON/OFF control for the
drive and is normally left in the ON position.

SCREW
3 PLACES

LOCKWASHER
3 PLACES
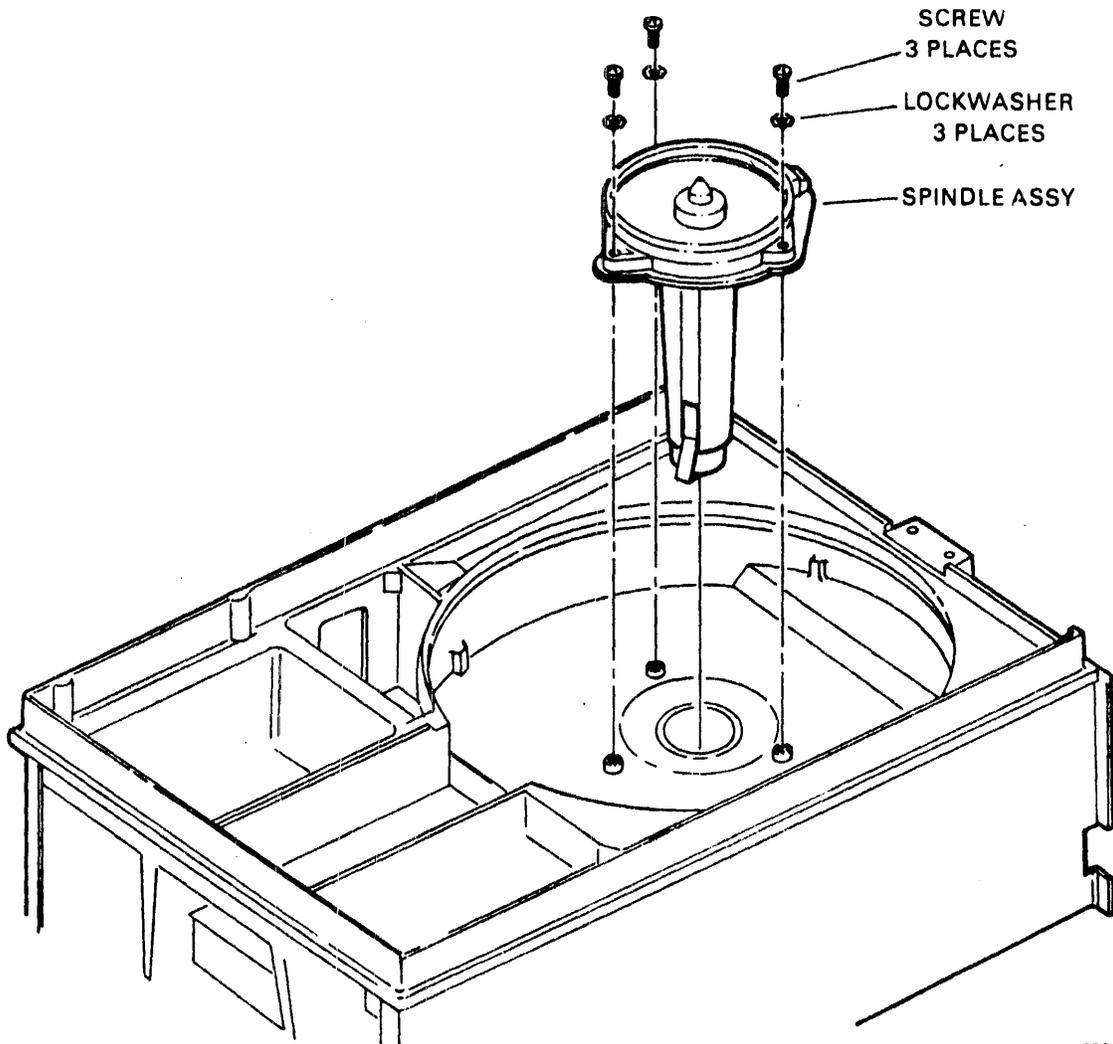
SPINDLE ASSY

MA-1588

Figure 1-4   Spindle Assembly

I/1-7
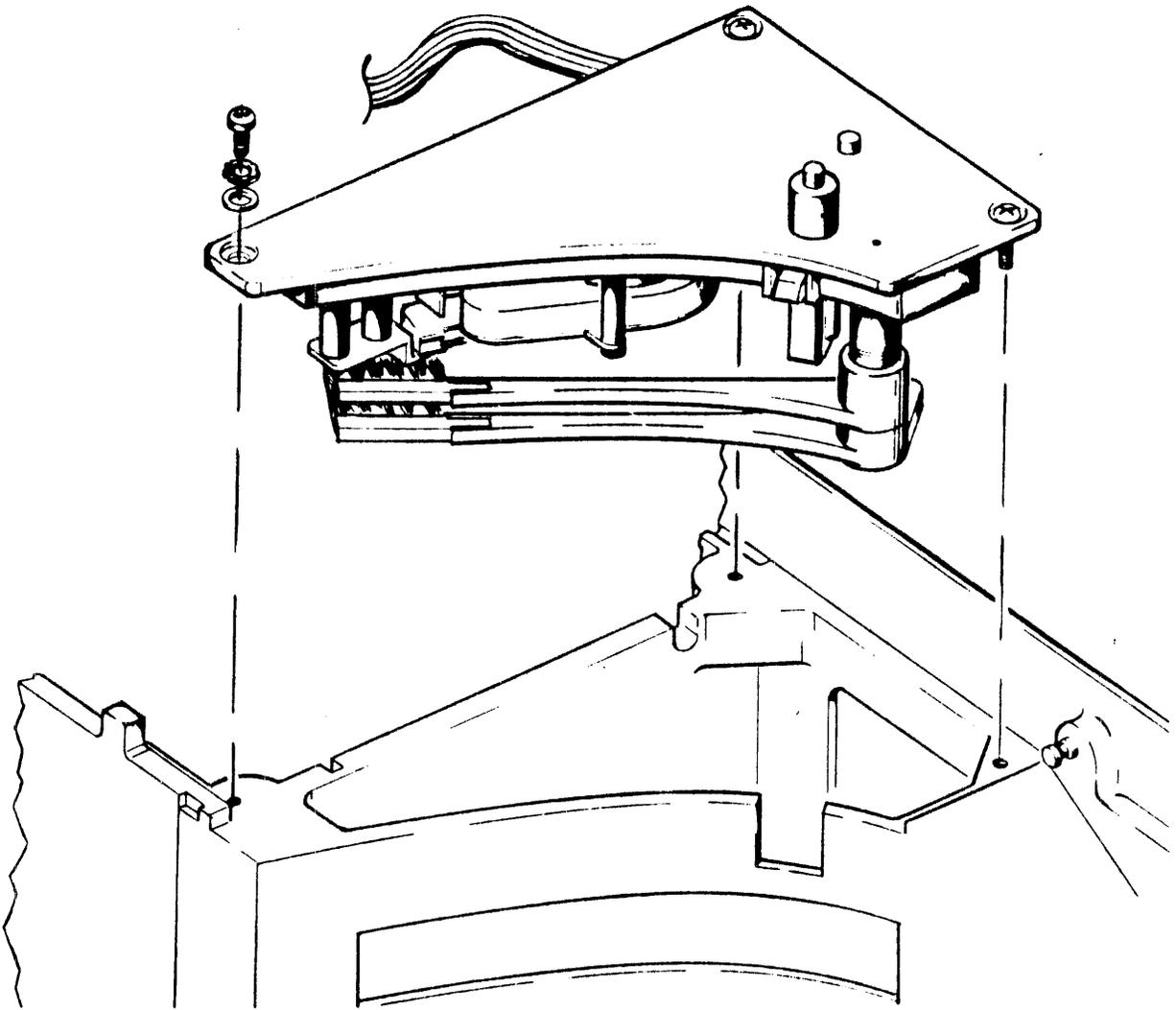
CZ-1002

Figure 1-5 Brush Assembly

LOWER
HEAD

UPPER
HEAD

PLASTIC
EXTENSION

LOWER HEAD LOCATING PIN

CARRIAGE
ASSEMBLY
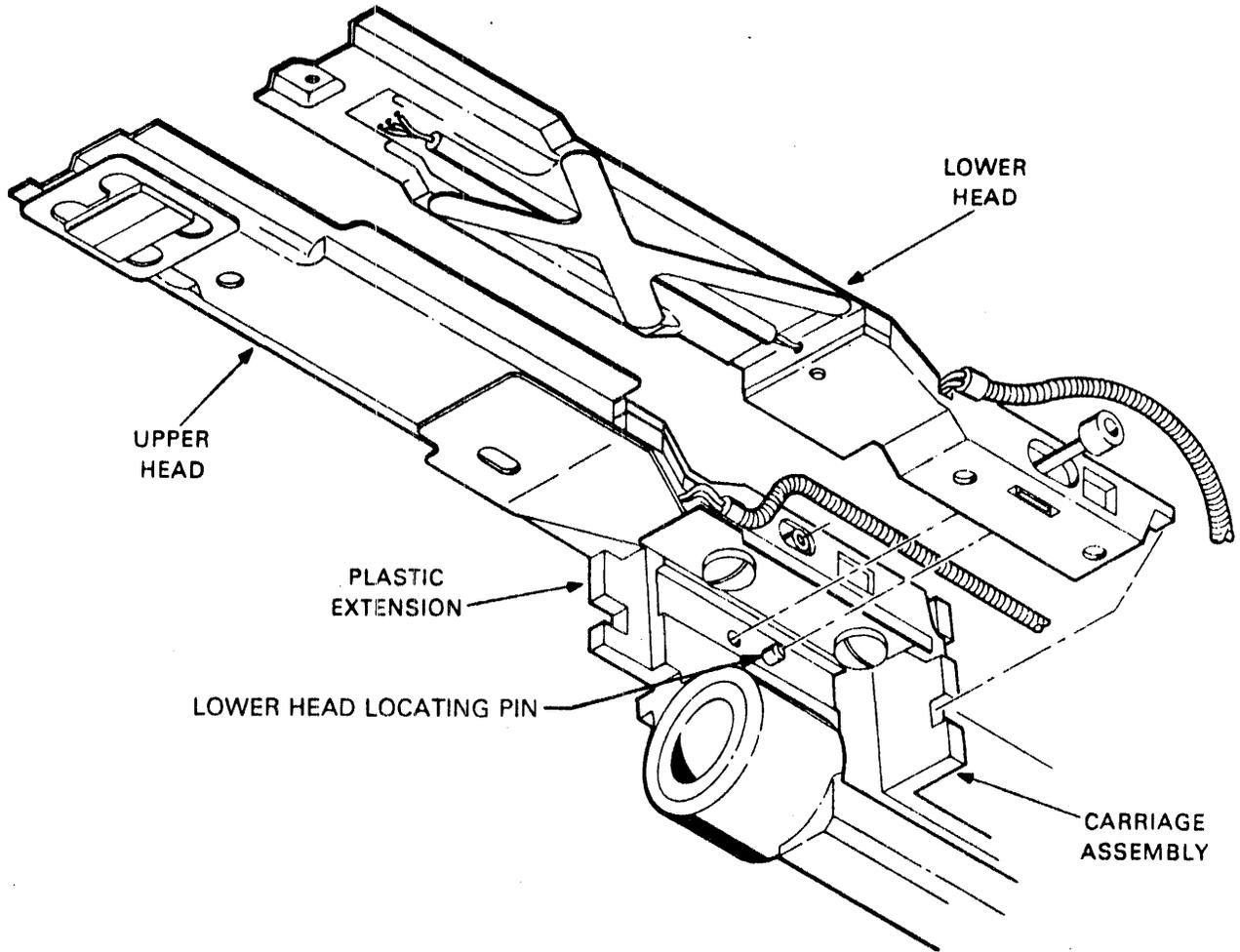
CZ-1003

Figure 1-6   Read/Write Heads

1

2

MOUNTING
SCREWS (6)

REAR POWER PANEL ASSEMBLY
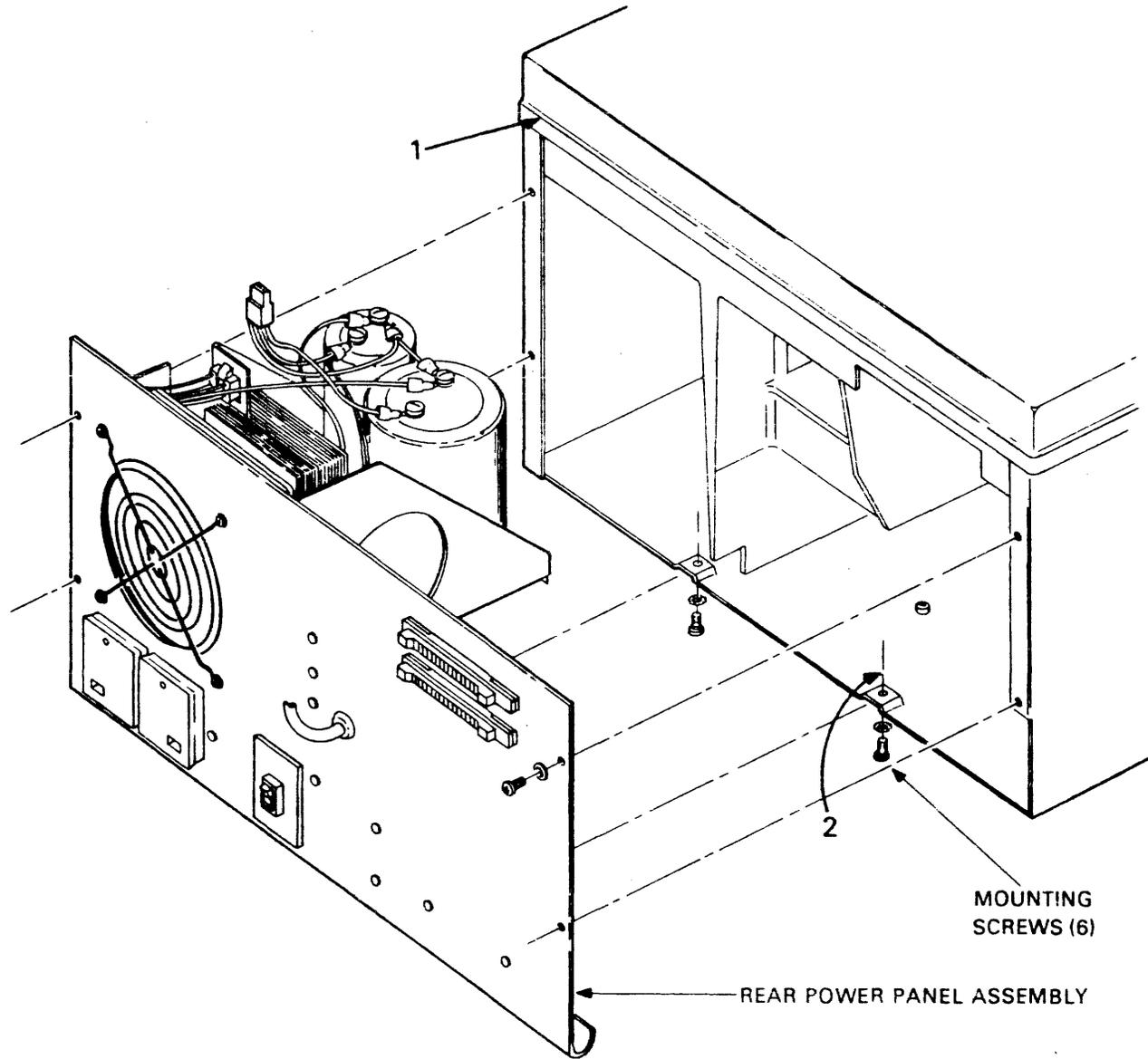
CZ-0015

Figure 1-7   Rear Panel Assembly

1.1.3.9   Control Panel – The operator's control panel is located at the front of the drive.   The following push on/push off alternating action switches and indicators are located on the drive control panel (Figure 1-8):

- Run/Load switch with LOAD indicator

- Unit Select switch with READY indicator

- FAULT indicator

- Write Protect switch with WRITE PROTect indicator

Run/Load Switch with LOAD Indicator

This push on/push off alternating action switch, when depressed, energizes the spindle motor providing the following conditions have been met:

- The disk cartridge has been installed

- The cartridge protection cover is in place and the cartridge access cover is closed and latched

- All ac and dc voltages are within specifications

- The read/write heads are home

- The brushes are home

When this switch is released (depressed a second time), the spindle drive motor is deenergized if the read/write heads are not loaded.   If the heads are loaded, they are retracted before the spindle drive motor is deenergized.   In the event of a main power interrupt and subsequent power restoration, the drive will cycle up again if the switch is depressed since it contains mechanical memory.

The LOAD enable indicator is illuminated whenever:

- The spindle is stopped

- The read/write heads are home

- The brushes are home

- The spindle drive motor is at rest

LOAD SWITCH
AND INDICATOR

UNIT SELECT PLUG
AND READY INDICATOR

FAULT
INDICATOR

WRITE PROTECT SWITCH
AND INDICATOR
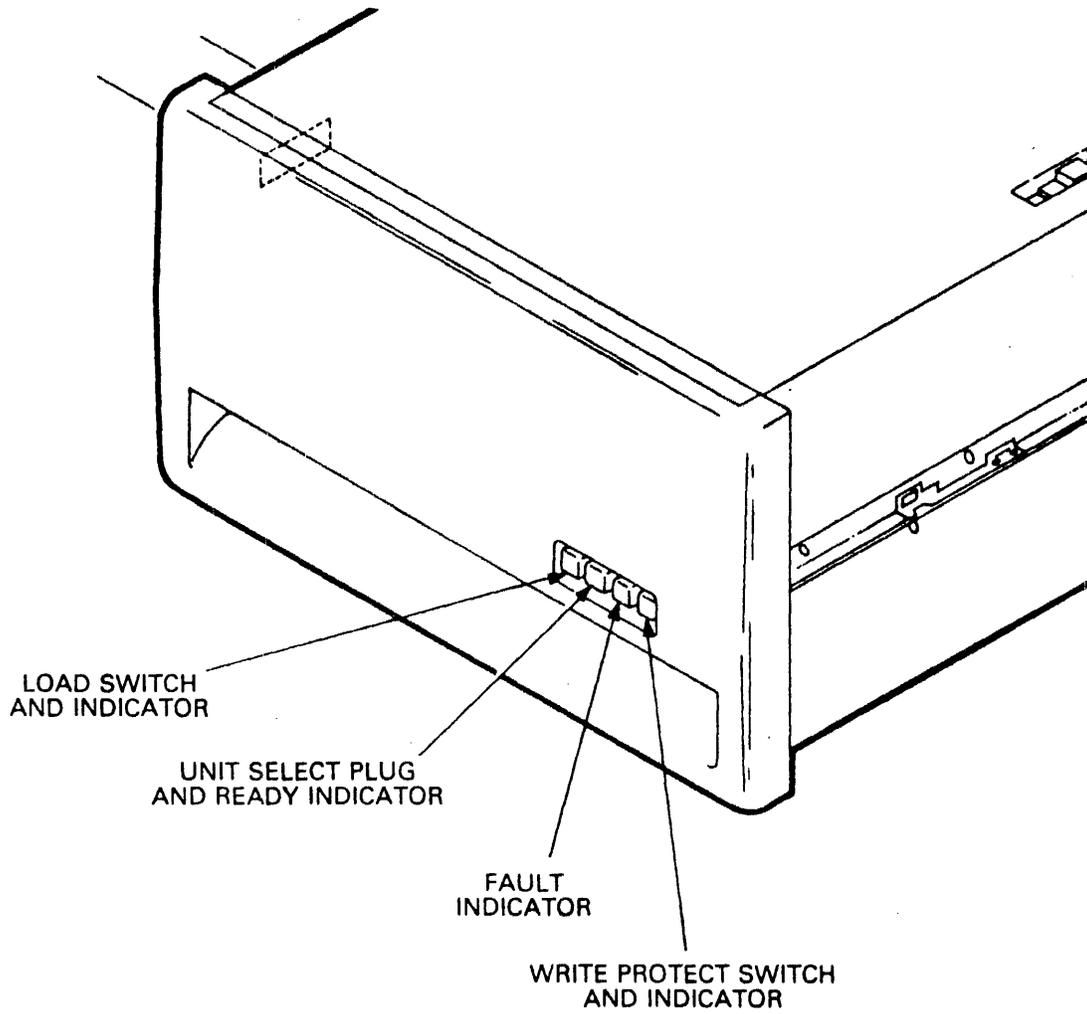
CZ-1005

Figure 1-8   Control Panel

I/1-12

Unit Select (0, 1, 2, 3) Switch with READY Indicator

The unit select switch is a cam operated switch which is actuated by inserting a numbered, selectively cammed button. The switch contacts are binary encoded so the drive interface logic recognizes the matching controller generated drive address code and the corresponding unit select number (0, 1, 2 or 3).

The numbered indicator, when lit, indicates a drive READY condition. This condition exists when:

- The spindle is up to speed

- The brushes are home

- The read/write heads are loaded

- The heads are detented on a specific track

FAULT Indicator

The FAULT indicator is lit whenever the following fault or error conditions develop in the disk drive:

- Drive Select Error

- Seek Time Out Error

- Write Current in Heads During Sector Time Error

- Loss of System Clock

- Write Protect Error

- Write Data Error

- Spin Error

WRITE PROTect Switch and Indicator

This alternating action push on/push off switch, when de-pressed, sets the drive in write protect mode whether or not the Write Gate line is asserted (refer to interface line descriptions). If the Write Gate line is asserted when WRITE PROTect is on, the drive will generate a Write Gate error (which will light FAULT). The write protect mode will be immediately removed upon release of the switch.

1.1.4   Drive Electronics Partitioning

A large percentage of the drive electronics is contained on the drive logic module. Additional electronics are on these modules:

- The dc servo module

- The ac servo module

- The read/write module

This design concept enhances the module-swap maintenance philosophy.

The drive logic module, mounted inside the rear cover at the top of the drive, is a single hex-sized board. The rear cover can be detached and positioned vertically on the rear edge of the base plate. Refer to Figure 1-9.

Opening the rear cover exposes the read/write module and the dc servo module. Both the read/write module and dc servo module can be placed on their sides to allow easy access to the positioner assembly, module chips and test points. Refer to Figure 1-9. The ac servo module is located on the removable power panel. Refer to Figure 1-9.

1.1.4.1   Drive Logic Module – The drive logic module provides the drive with the following functions:

- Interface to the controller via a 40 pin PC-mounted connector and flat ribbon cable

- Interface enabling and control circuits

- State control logic (load/run sequencing)

- Seek control and track counting logic

- Device command/status register

- Positioner velocity command generation

- Disk drive motor speed control

- Error detection and status data generation

- Servo data detection logic

1.1.4.2   DC Servo Module – The dc servo module contains the positioner servo amplifier and dc voltage regulators. The voltage regulators are mounted on a U-shaped heat sink which faces down into the cooling air chamber. This module also serves a mechanical function in that it seals a portion of the cooling air system from the clean air system.

DRIVE LOGIC
MODULE

A.C.
SERVO MODULE

R/W
MODULE

D.C. SERVO MODULE
AND TEMPLATE
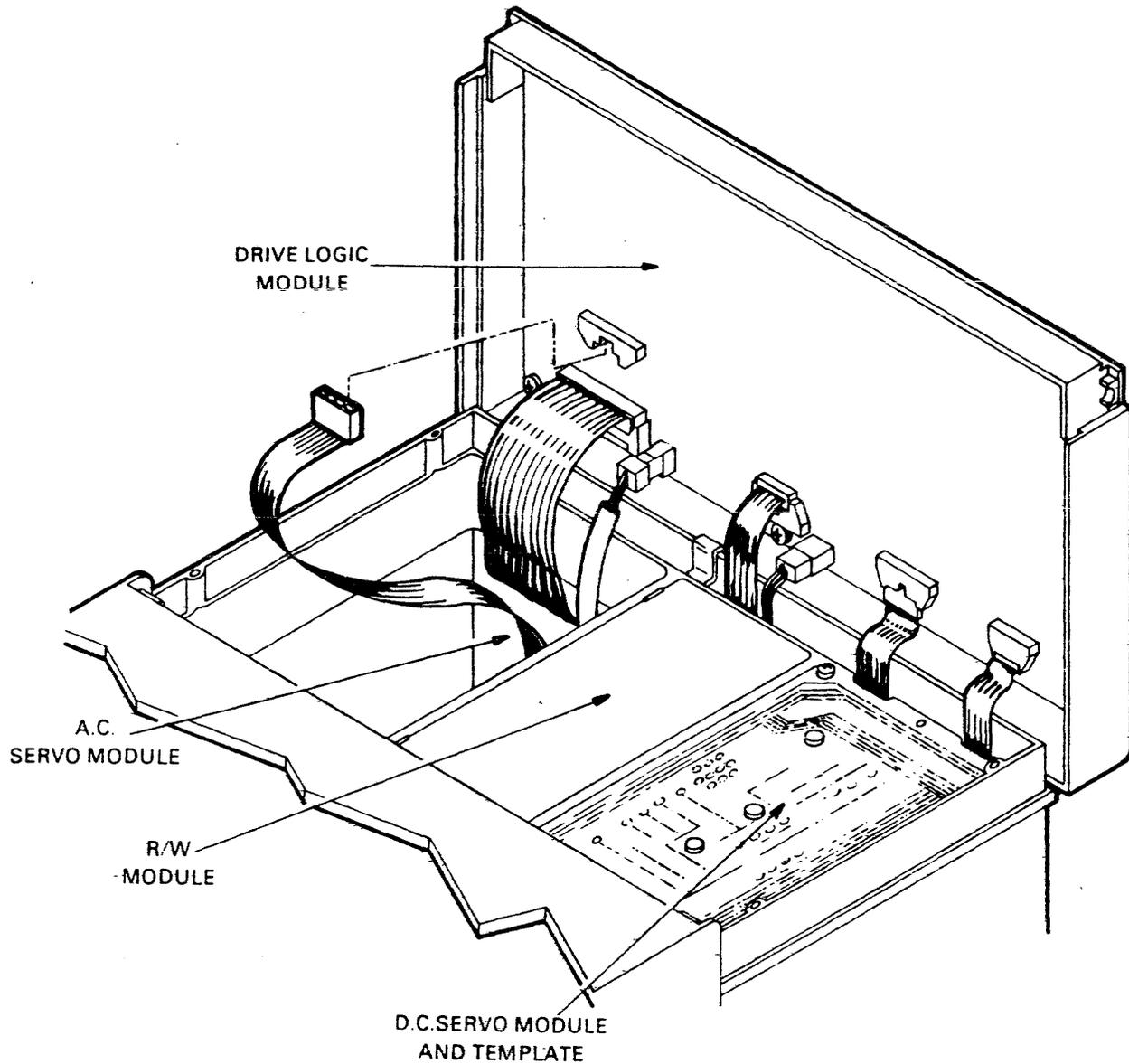
CZ-0011

Figure 1-9   Logic Modules

1.1.4.3.   AC Servo Module - The ac servo module provides the following functions:

- Control circuits for the brush motor

- Control circuits for the spindle drive motor

- Cover solenoid drive circuit

1.1.4.4   Read/Write Module - The functions provided by the read/write module are:

- Servo and read data preamplifier, filters, differentiator and limiter

- Head selection

- Write drivers and write current sensing

- Write error sensing

1.1.5   Documentation
Table 1-1 lists the documents that will be available to describe the RL01/RL02 Subsystem.

Hard copy user documentation consisting of the RL01/RL02 Disk Subsystem User's Guide (which contains operation and installation information) will ship with each subsystem.

Table 1-1   RL01/RL02 Subsystem Documentation

Title	Microfiche Number	Hard Copy Number
RLV11 Controller Technical Description Manual	EP-RLV11-TD	EK-RLV11-TD
RL11 Controller Technical Description Manual	EP-0RL11-TD	EK-0RL11-TD
RL8A Omnibus Controller Technical Manual	EP-0RL8A-TM	EK-0RL8A-RM
RL01/RL02 Preventive Maintenance Procedures	EP-00008-PM	EK-RL012-PM
RL01 Illustrated Parts Breakdown	EP-00016-IP	EK-0RL01-IP
RL02 Illustrated Parts Breakdown	EP-00016-IP	EK-0RL02-IP
RL01/RL02 Disk Subsystem User's Guide	N/A	EK-RL012-UG
RL01/RL02 Pocket Service Guide	N/A	EK-RL012-PG

1.2   SUBSYSTEM SPECIFICATIONS

This section provides the following specificataion for the RLØ1 and RLØ2 Disk Subsystem:

- Table 1-2:   RLØ1/RLØ2 Disk Drive Physical and Environmental Specifications

- Table 1-3:   RLØ1/RLØ2 Disk Drive Operational Specifications

- Table 1-4:   RLØ1K/RLØ2K Disk Cartridge Operational Specifications

Table 1-2   RL01 Disk Drive Physical and Environmental Specifications

Width	Compatible with 19 inch RETMA rack
Depth	63.5 cm (25 in) behind bezel
Height	26.5 cm (10.5 in)
Weight	34 kg (75 lbs)
Mounting	The drive mounts on chassis slides.
Power Sources	90-127 Vac (47.5-63 Hz)
	180-254 Vac (47.5-63 Hz) (Manually selectable)
Input Power	200 watts maximum at 115 Vac, 60 Hz
Power Factor	Greater than 0.85
Starting Current	3.5 amps RMS maximum @ 90 Vac/47.5-63 Hz
	5.0 amps RMS maximum @ 127 Vac/47.5-63 Hz
	1.75 amps RMS maximum @ 180 Vac/47.5-63 Hz
	2.5 amps RMS maximum @ 254 Vac/47.5-63 Hz
Power Cord and Connector:	A molded line cord compatible with the drive operating voltage and the 861 Power Control for 120 Vac is attached to the drive.
	The power cord is 2.74 m (9 ft) long and the plug is NEMA 5-15P.
	The 230 Vac plug to be attached to high voltage drives is NEMA 6-15P.
Safety	The RL01/RL02 Disk Drive is UL listed and CSA certified.
Interlocks	Interlocks are used where potential exists for damage to drive, media, operators or service personnel.

Temperature/Humidity

Operating:

Temperature: 10° C (50° F) to 40° C (104° F).

Derate Temperature 5.9° C/1000 m (1.8° C/1000 ft)

Relative Humidity: 10% to 90% with maximum wet bulb 28° C (82° F) and minimum dew point 2° C (36° F).

Non-Operating:

Temperature: -40° C (-40° F) to 66° C (151° F)

Relative Humidity: 10% to 95%

Altitude

Operating: 2440 m (8,000 f) maximum.

Non-Operating: 9.1 km (30,000 f) maximum.

Shock

Operating: Half sine shock pulse of 10 Gpk and 10 +3 msec duration applied once in either direction of three orthagonal axes (3 pulses total).

Non-Operating: Half sine shock pulses of 40 Gpk and 30 +10 ms duration perpendicular to each of six package surfaces.

Vibration

Operating:

Sinusoidal vibration (sweep rate 1 octave/min)

5-50 Hz   0.002" DA
50-500 Hz   0.25 Gpk
500-50 Hz   0.25 Gpk
50-5 Hz   0.002" DA

Non-Operating:

Vertical Axis Excitation - 1.40 Grms overall from 10 to 300 Hz. Power spectral density 0.029 g/Hz from 10 to 50 Hz with 8 dB/octave rolloff from 50-300 Hz.

	Longitudinal and Lateral Axis Excitation - 0.68 Grms Overall from 10 to 200 Hz. Power spectral density 0.007 g/Hz from 10 - 50 Hz with 8 dB/octave rolloff from 50 to 200 Hz.
Dust	The drive will operate in an ambient atmosphere of less than 5 million particles 0.5 microns or larger per cubic foot of air. The drive is intended to run in a light industry (or cleaner) environment.
Attitude	Maximum pitch: +5 degrees Maximum roll: +5 degrees
Heat Dissipation	546 BTU/hour maximum

Table 1-3   RL01/RL02 Disk Drive Operational Specifications

General	Linear bit density: 147 bits/mm (3725 bits/in) at innermost track
	16 bit words per sector: 128
	Number of sectors: 40/track
	Track density: 4.9/mm (125/in) for RL01K, 9.8/mm (250/in) for RL02K
	Number of recording tracks: 256/surface for RL01K, 512/surface for RL02K
	Number of surfaces: 2
	Formatted capacity (megabytes): 5.2 for RL01K, 10.4 for RL02K
	Encoding method: MFM
Transfer Rate Bit Rate: (unbuffered values)	4.1 megabits/sec $\pm$1%
	Bit Cell Width: 244 nsec $\pm$1%
	Words (16 bit): 256 kilowords/sec $\pm$1%
Latency	Rotational Frequency: 2400 rpm $\pm$0.25%
	Average latency: 12.5 msec $\pm$0.25%
	Maximum latency 25.0 msec $\pm$0.25%
Seek Time	Average seek time — 55 msec max (85 tracks for RL01, 120 tracks for RL02)
	One cylinder track seek time — 5 msec max
	Maximum seek time — 100 msec max (256 tracks for RL01, 512 tracks for RL02)
	Head switch time — 8 msec
Start/Stop Time	Start time: 45 seconds
	Stop time: 30 seconds
Data Format	Refer to Figure 1-10
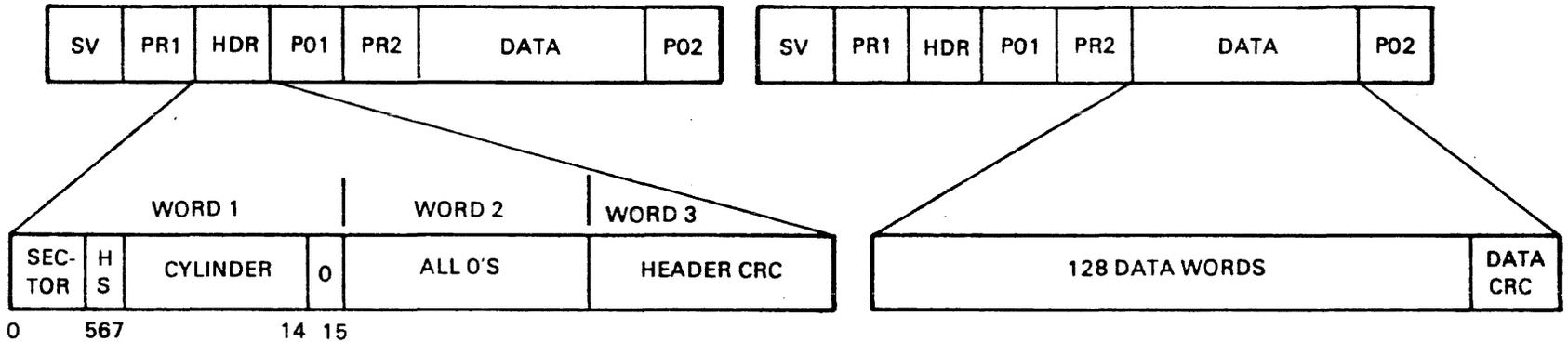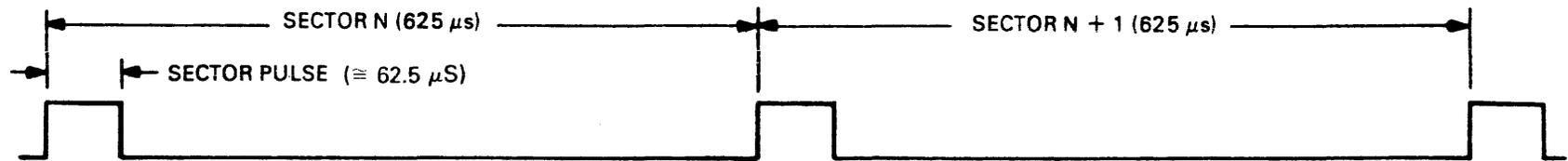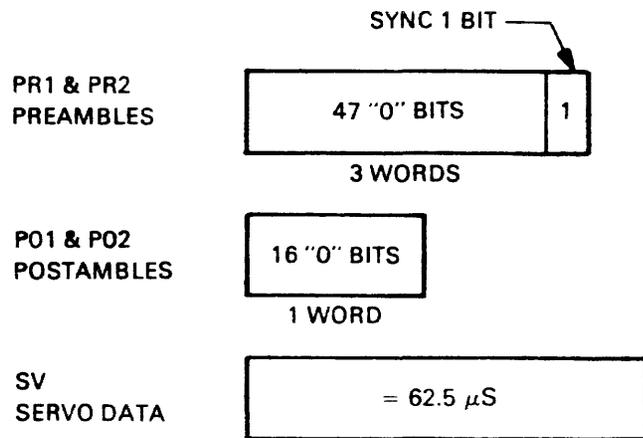
Figure 1-10   Data Format

CZ-1006

Table 1-4   RLØ1K/RLØ2K Disk Cartridge Specifications

Operating Environment	The cartridge will operate in air whose temperature lies between 40° C to 48° C (40° F to 120° F) at a relative humidity of 8 to 80%. The wet bulb reading shall not exceed 25° C (78° F). Before a cartridge is placed into operation, it shall be conditioned within its cover for a minimum of two hours in the same environment as that in which the disk drive is operating. The above specified range does not necessarily apply to the disk drive.
Storage	The cartridge must be stored at a temperature Environment between $- 40^\circ$ C to 65° C (-40° F to 150° F). The wet bulb reading not exceeding 29° C (85° F). For wet bulb temperatures between 0.56° C and 29° C (33° F and 85° F) the disk cartridge shall be able to withstand a relative humidity (non-condensing) of 8 to 80%. The stray magnetic field intensity shall not exceed 50 oersteds.
Dimensions (Cartridge)	External Diameter The external diameter of the top cover is 38.35 cm (15.1 in). The external diameter of the protection cover is 37.03 cm (14.58 in). The external height of the cartridge when resting on its bottom surface is 6.19 cm (2.44 in).
Maximum Speed	The rotating parts of the disk cartridge are capable of withstanding the effect of stress at the speed of 2,500 rev/min.
Track Geometry	Number of Tracks – There are 256 discrete concentric tracks per data surface for the RLØ1K, 512 tracks per data surface for the RLØ2K.

**Identification
of Data Tracks**

Data Track Identification – Data track iden-
tification is a three digit decimal number
(000 – 255, RL01K, 000 – 511, RL02K) that
numbers data tracks consecutively starting
at the outermost data track of each data
surface.

Data Surface Identification – The data sur-
faces are numbered 0 and 1 starting with the
uppermost surface and corresponding with the
head numbers.

Cylinder Address – A cylinder is defined as
the data tracks on the data surface with a
common data track identification.

Data Track Address – A 16-bit word, where
bits 0 – 5 define a binary sector number,
bit 6 defines surface, and bits 7 – 15
define a binary cylinder address. This
information is in word 1 of each sector's
header.

2.1   RLØ1RLØ2 MASS STORAGE SUBSYSTEM

The RLØ1/RLØ2 Mass Storage Subsystem consists of up to four drives in a daisy-chain configuration, and a controller (RL11, RLV11 or RL8A). Additional drives, if required, necessitate a second controller. Figure 2-1 illustrates a typical subsystem.

2.2   DISK CARTRIDGE FORMAT

Figure 2-2 shows servo, header, sector and data formatting for the RLØ1K/RLØ2K Disk cartridge.

Servo and header information for each sector is prerecorded at the factory and cannot be modified or rewritten in the field. Accidental overwriting or destruction of the servo information is prevented by logic within the drive.

Each RLØ1K disk recording surface has a total of 256 data tracks (numbered Ø to 255) and each RLØ2K surface has 512 tracks (numbered Ø to 511). Thus, there are 256 cylinders on an RLØ1K cartridge and 512 clinders on an RLØ2K.

2.2.1   Data Format

Each track on the recording surface is divided into 4Ø equal-length sectors which are further subdivided into fields. The six fields in each sector contain a total of 14Ø words of 16 bits each. One hundred twenty eight of the 14Ø words contain data.

Header Preamble (PR1) — These three words precede the header information and contain 47 "Ø" bits followed by a marker "1" (Sync Bit) to indicate the start of valid information.

Header — This field contains three words of 16 bits each. The first word identifies the disk surface (upper or lower), the cylinder address (1 of 256, RLØ1; 1 of 512, RLØ2), and the sector address (1 of 4Ø).

The second header word is all Øs. The third word is the header CRC word. This check word is prerecorded on the track, as are the other two header words. During a read operation, the header is checked for errors. If one is detected, an error flag is raised.

Header Postamble (PO1) — This field contains 16 "Ø" bits. It separates the header and data fields to allow for mechanical tolerances between drives.

Data Preamble (PR2) — This field contains 47 "Ø" bits followed by a marker "1" (Sync Bit) to indicate the start of the data field and is written in conjunction with the data.
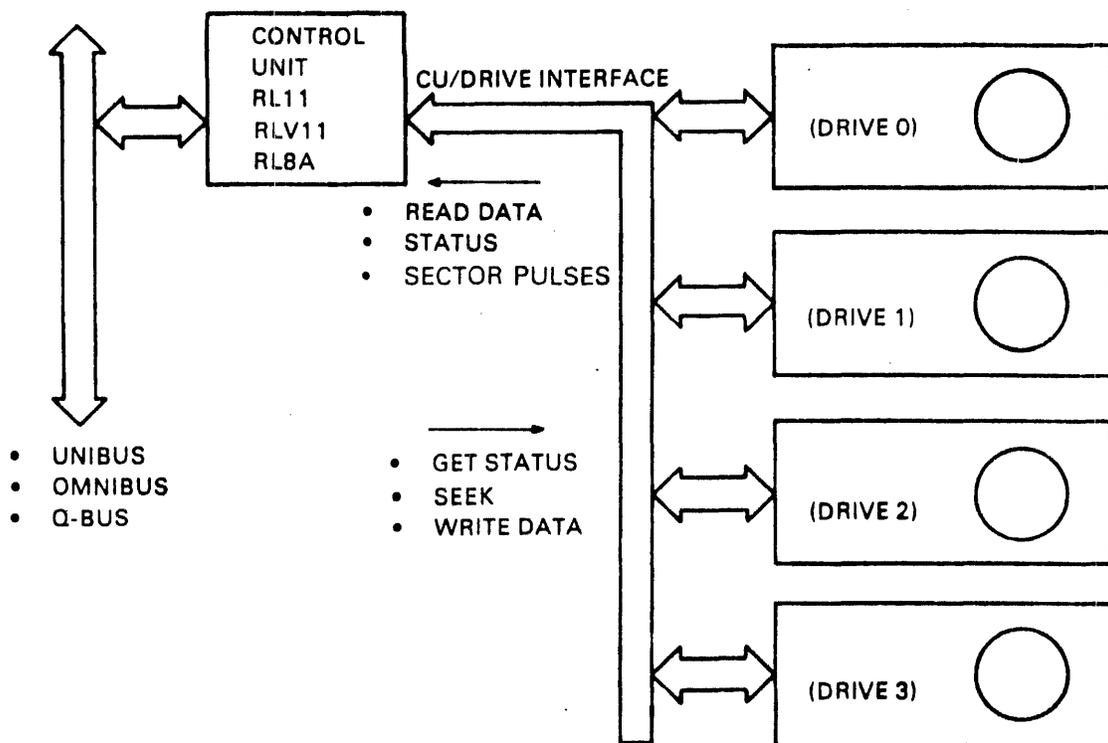
CZ-1007

Figure 2-1   Typical RL01/RL02 Mass Storage Subsystem

625µs

62.5µs

SECTOR PULSE

>0

| SERVO BURSTS | HEADER | DATA |
| | | |

| SERVO BURSTS | HEADER | DATA |
| | | |

| HEADER PREAMBLE | | ADDRESS | ZEROES | CRC | HEADER POSTAMBLE |
| 47 ZERO BITS | 1 | 16 BITS | 16 ZERO BITS | 16 BITS | 16 ZERO BITS |

| DATA PREAMBLE | | DATA | CRC | DATA POSTAMBLE |
| 47 ZERO BITS | 1 | 2048 BITS | 16 BITS | 16 ZERO BITS |

| SECTOR | HEAD | CYLINDER |
| SIX BITS | ONE BIT | NINE BITS |

LSB   MSB

| | WORD 0 | WORD 1 | | WORD 126 | WORD 127 |
| 16 BIT WORD MODE | 16 BITS | 16 BITS | | 16 BITS | 16 BITS |

| | BYTE 0 | BYTE 1 | | BYTE 254 | BYTE 255 |
| 8 BIT BYTE MODE | 8 BITS | 8 BITS | | 8 BITS | 8 BITS |

| | WORD 0 | WORD 1 | | WORD 168 | WORD 169 | UN-USED |
| 12 BIT WORD MODE | 12 BITS | 12 BITS | | 12 BITS | 12 BITS | 8 BITS |

MSB
LSB

NAME	MNEMONIC	LENGTH
SERVO BURSTS	SV	—
HEADER PREAMBLE	PR1	3 WORDS
HEADER	HDR	3 WORDS
HEADER POSTAMBLE	PO1	1 WORD
DATA PREAMBLE	PR2	3 WORDS
DATA	—	2048 BITS
DATA POSTAMBLE	PO2	1 WORD

CZ-2027

Figure 2-2   RL01K/RL02K Disk Cartridge Characteristics

Data - This field accommodates a block of 128 16-bit data words (2048 bits) followed by a 16-bit data CRC word. When writing data, a data CRC word is generated by the controller and appended to the 128-word data block. The contents of the CRC word vary with the contents of the data block. When reading the data from the drive, the data block and CRC word are checked in the controller. Detection of a data reading error results in a data CRC flag.

Data Postamble (PO2) - This field consists of 16 "0" bits. Write current is turned off at the end of this field so that data CRC information will not be destroyed.

2.2.2   Servo Data

2.2.2.1   Introduction - One of the features of the servo-in-data design approach for track counting and carriage positioning is the fact that it shares read/write heads and circuitry. This is different from IBM 3330 technology which, in general, requires a dedicated servo head and servo track. While 3330-type servo information is monitored continuously as the disk is spinning, the RL01 or RL02 only takes servo samples (much like snapshots) during each sector pulse.

The servo data bursts are prerecorded on the disk surface during a certain time period within the sector pulse. The sector pulse is generated by a separate magnetic transducer mounted on the spindle which senses each of the 40 sector slots in the cartridge armature plate.

Since the cartridge disk spins at 2400 rpm and there are 40 sector slots, the drive takes servo samples for positioning and track counting every 625 microseconds.

2.2.2.2   Modes of Operation - While the heads are flying, the drive operates in either of two modes:

● Velocity (seek and track counting) mode, or

● Position (track following) mode

In velocity mode, the drive logic counts track crossings by using servo information recorded on the disk surface and converting this information into binary format. This information is used in conjunction with carriage velocity (sensed by the tachometer) to decrement a track difference counter and ultimately to control the velocity of the positioner. This process is described in Paragraph 2.2.2.4.

The drive does not enter position mode until the track difference counter has been decremented (while the drive is in velocity mode) to zero. In positioning mode, the drive locks on to the required track. Position mode operation is described in Paragraph 2.2.2.5.

2.2.2.3   Generation of Servo Signals - There are two bursts of servo data that are prerecorded on the disk surface during a sector pulse. They are identified as servo samples S1 and S2 and are approximately 15 microseconds in length. Each servo sample is made up of two square wave components, S and $\overline{S}$ (i.e., S1 and $\overline{S1}$; S2 and $\overline{S2}$). These components are offset radially by .004 inches or half a data track. They are also 180 degrees out of phase (see Figure 2-3).

If the read/write head is centered directly over the centerline of the S and $\overline{S}$ components a pure sine wave (50% duty cycle) is output from the head. See Figure 2-4A. If the head is moved slightly off center, a wave shape with greater than a 50% duty cycle results (i.e., more S than $\overline{S}$ is sensed or vice-versa). This is shown in Figure 2-4B.

Because the S2 samples are 180 degrees out of phase from the S1 samples, a perfect sine wave (from S1) will alternate with an imperfect wave (from S2) as the head detects alternating S1 and S2 samples. See Figure 2-4A.

2.2.2.4   Velocity Mode Operation - As stated before, the servo information is converted to binary format as part of the control process for the positioner velocity. The first part of this process is the integration of the composite S and $\overline{S}$ signal. The integration is shown graphically in Figure 2-5. When the head is on a data track centerline, the S1 - $\overline{S1}$ signal will be a perfect sine wave. The integral of this, a signal called E1, is the sawtoothed wave shown below it. With the head still on the data track centerline, the S2 - $\overline{S2}$ signal is not a perfect sine wave, and its integral therefore, will not be a perfect sawtooth wave. Rather, it will be the jagged line shown in Figure 2-5. This signal is called E2.

The conversion of E1 and E2 to binary format is simple. If E1 or E2 is a perfect sawtooth, it is converted to a digital 0; if it is not a perfect sawtooth, it becomes a digital 1. The logic first samples E1 and a flip-flop sets or resets depending on whether E1 is 0 or 1. The same thing happens to E2. These two values become the signals E1 Held and E2 Held as a new E1 and a new E2 are determined.

These four signals (E1, E1 Held, E2 and E2 Held) are part of an address to the Count ROM. Another bit of the ROM address comes from a signal indicating the direction of head motion (sign forward) and the remaining three bits come from the velocity signal from the transducer (after conversion to digital form). The output of this ROM goes to the Count ROM Decoder, which is used to decrement the track difference counter.

SECTOR PULSE

PREVIOUS DATA RECORD

TRACK ₵

S₁

S̄₁

S₂

S̄₂

S₂

HEADER   DATA RECORD

TRACK ₵

DATA TRACK
₵

S₁

S̄₁

S₂

S̄₂

S₁, S̄₁ SERVO BURST AS PRERECORDED ON DISK

S₂, S̄₂ SERVO BURST AS PRERECORDED ON DISK

CZ-1009
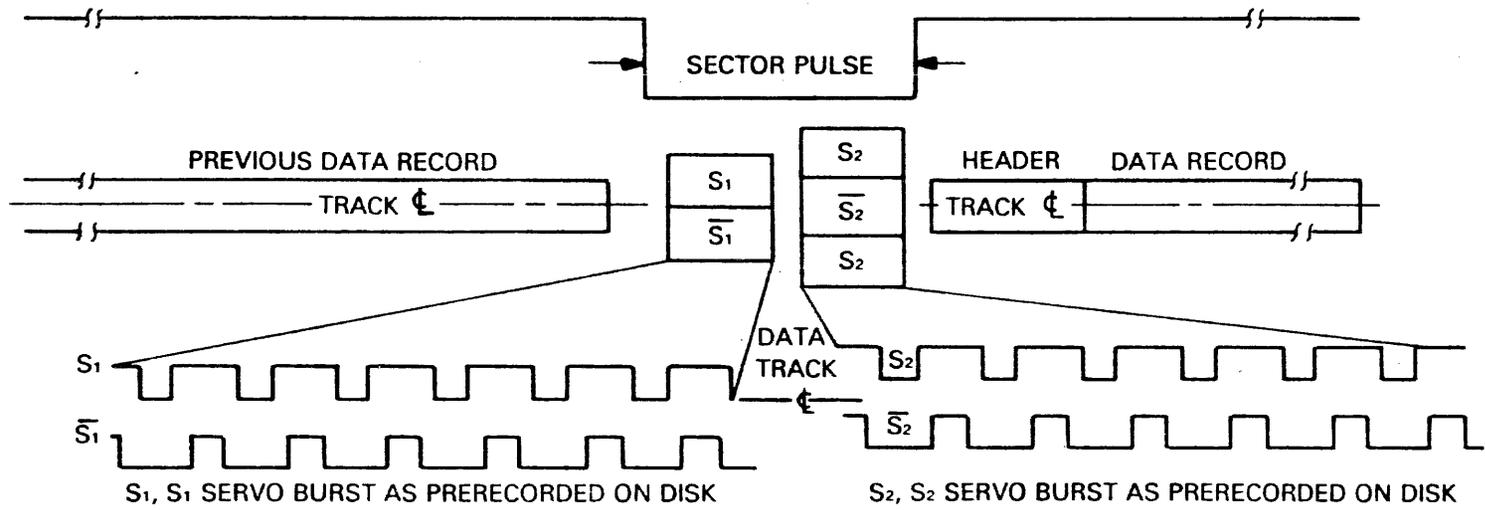
Figure 2-3   Servo Sample Generation
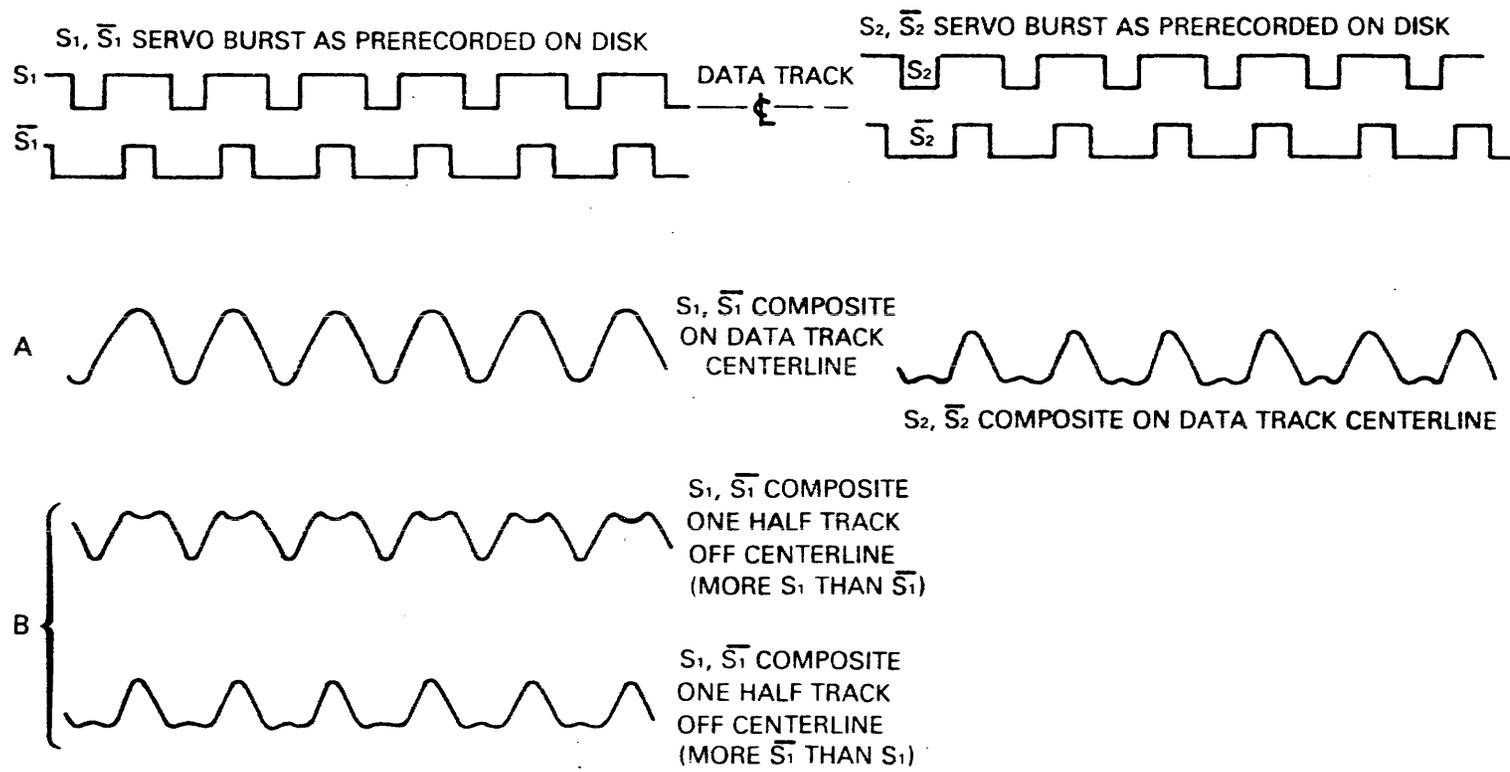
Figure 2-4 Servo Data Waveforms

$S_1, \overline{S}_1$ COMPOSITE ON DATA TRACK CENTERLINE

$S_2, \overline{S}_2$ COMPOSITE ON DATA TRACK CENTERLINE

0 VOLTS — E1 INTEGRATED

0 VOLTS — E2 INTEGRATED

CZ-1011

I/2-8
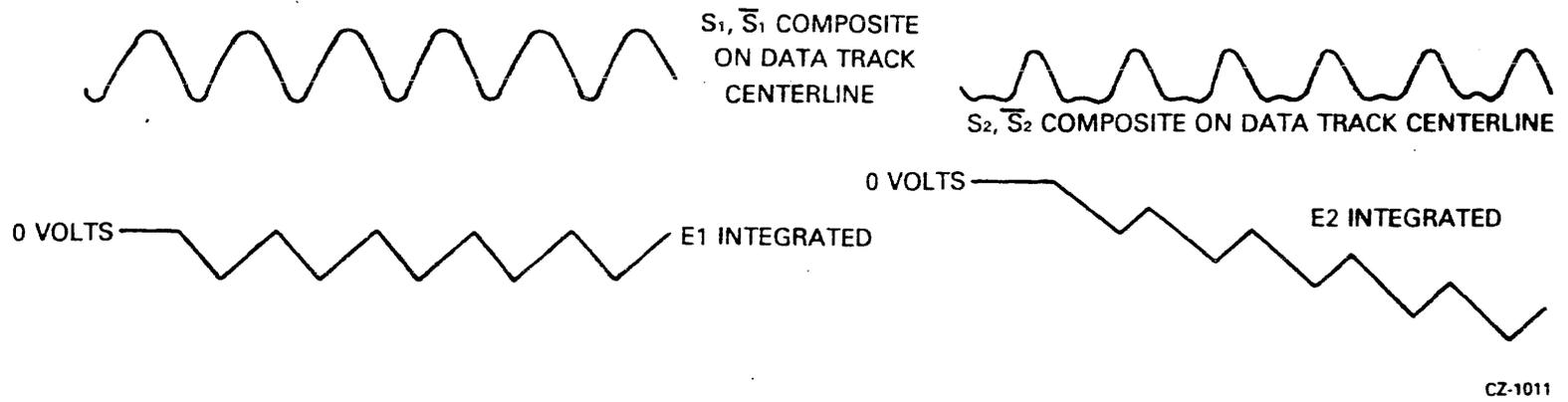
Figure 2-5   Generation of E1 and E2

2.2.2.5 Position Mode - The drive enters this mode of operation when the count in the track difference counter is zero, indicating that the head is over the centerline of the desired data track. At this point, the S1 - $\overline{S1}$ composite signal will be a perfect sine wave, and its integral, E1, will be the sawtooth wave shown in Figure 2-5. The average of the E1 signal will be zero, and the logic will send a zero signal (positioner signal) to the positioner, indicating that the positioner should not move. If the head drifts off the centerline, the signal E1 will no longer be a sawtooth wave and will no longer average out to zero. Thus, positioner signal will be an analog value that represents the error (the amount the head is away from the data track centerline) in the positioner, and this signal will move the positioner so the head returns to the centerline.

When positioner signal is nominally zero for 6.5 milliseconds (|20%), indicating the head has locked on the centerline, the signal READY TO R/W will be asserted, so that the drive can read or write.

2.2.2.6   Guard Band - The Servo bursts are not only used for locating data tracks. A special format at the far outer and far inner formatter tracks is used to identify "inner" and "outer" guardbands.   An absence of S_2 bursts and the recording of contiguous tracks of S_1 bursts identifies the "outer guard band" or the portion of the recording surface closest to the edge of the disk.   An absence of S1 bursts and the recording of contiguous tracks of S_2 bursts identifies the "inner guard band" or the portion of the recording surface closest to the spindle. See Figure 2-6.

2.2.3   MFM Encoding and Precompensation
The disk drive utilizes a Modified Frequency Modulation (MFM) encoding technique to magnetically record digital data on the disk surfaces (Figure 2-7).   With this technique, each logical one produces a flux reversal in the center of its bit cell.   Two successive logical zeros produce a flux reversal in a bit cell containing a logical zero following a logical one. This method of recording has the advantage of putting at least one flux reversal on the disk for every two bit cells, thereby making it feasible to use phase-locked loop techniques to form a self-clocking data recovery system. Phase-locked loop circuitry maintains a constant bit density despite minor variations in disk speed.

One of the problems associated with magnetic recording is a phenomenon called peak shift, wherein flux reversals written on the disk tend to repel one another. Because of this, the flux reversals appear displaced from where they were written. This can cause pattern-sensitive data recovery problems.
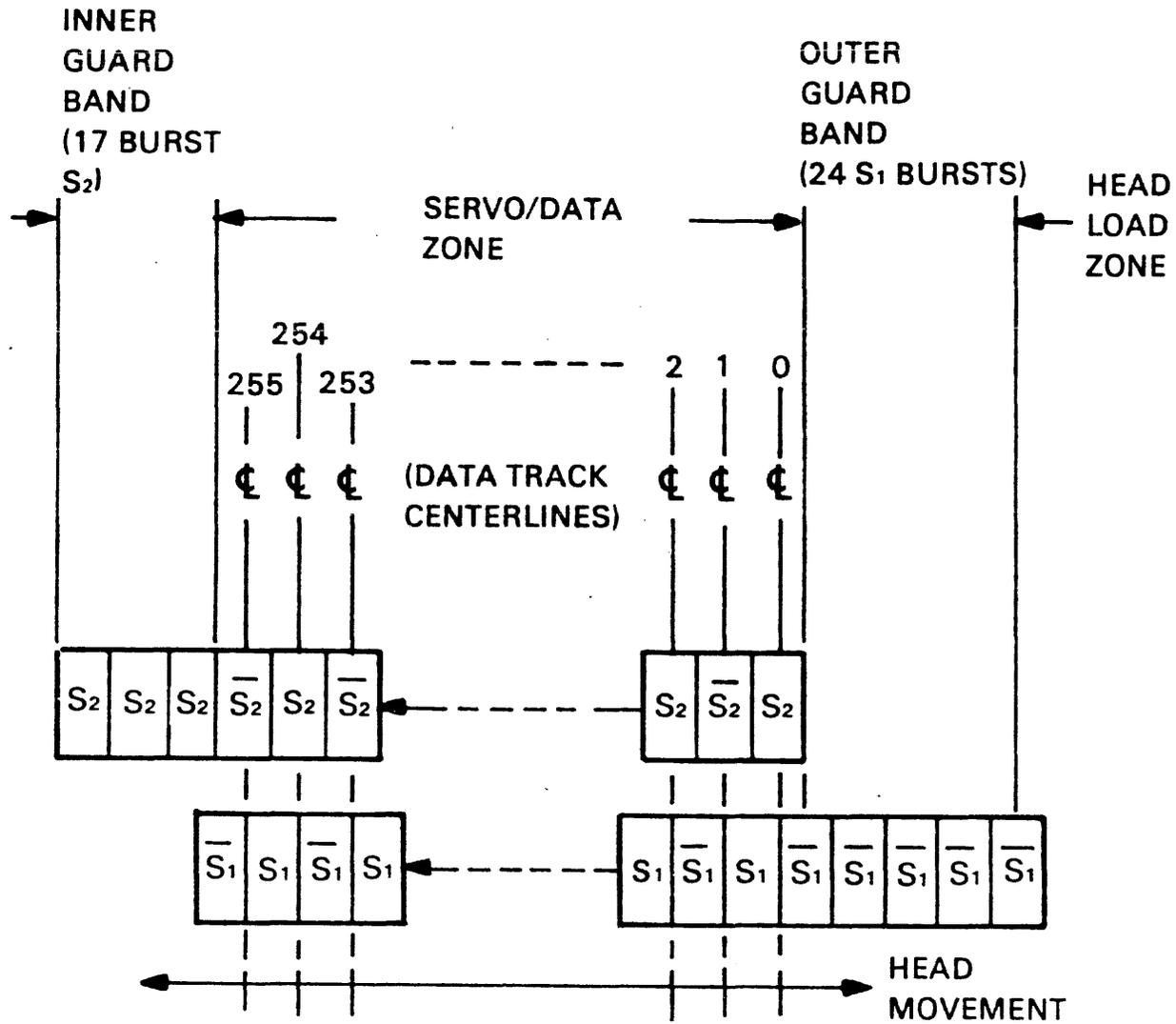
Figure 2-6 Servo Data Pattern
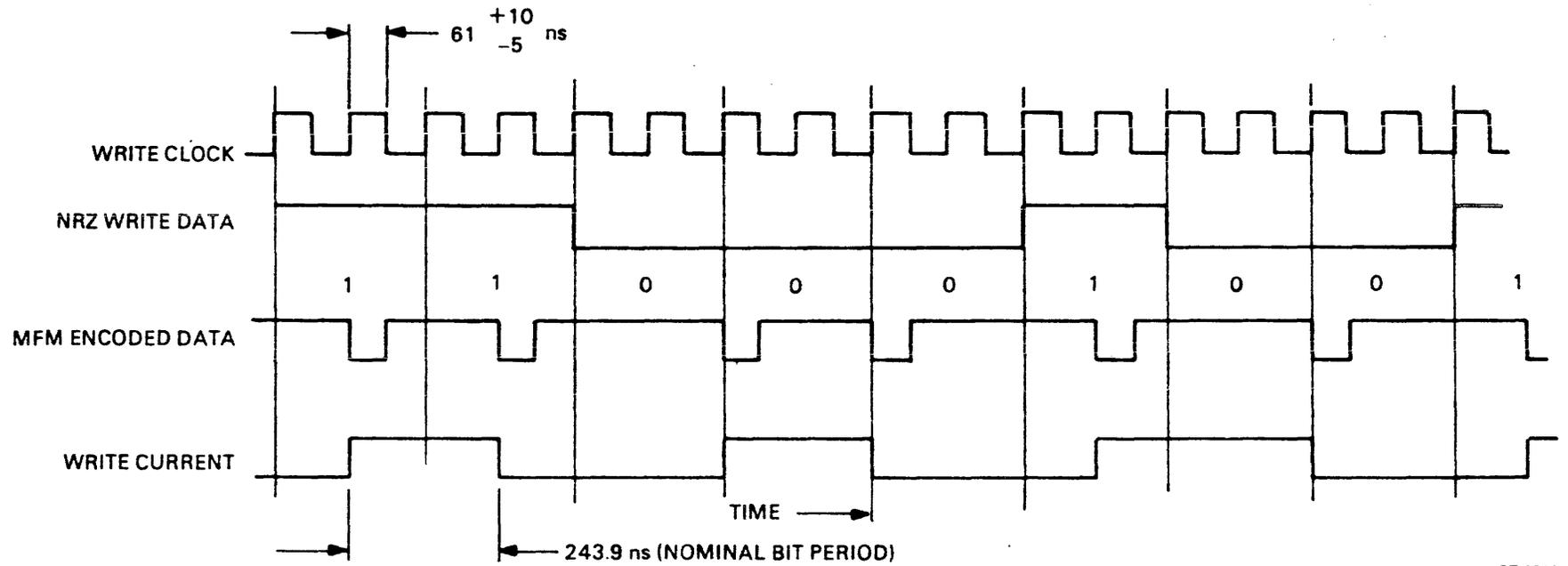
CZ-1012

Figure 2-7 Modified Frequency Modulation (MFM) Encoding

To offset the deleterious effect of peak shift, precompensation logic is included in the controller. This logic displaces certain encoded data pulses by 15 ns in one direction or the other before they are written on the disk so that the peak shift phenomenon displaces the flux reversals written on the disk to the desired positions.

To determine if an encoded data pulse is to be displaced from its nominal position, the following rule may be used: A pulse will be preshifted only if:

1. It is bounded on one side by a pulse that is not more than 1 bit cell away; and

2. It is bounded on the other side by a pulse that is greater than 1 bit cell away (for example, 1.5 or 2 bit cells away).

The direction of the preshift depends on the combination of ones and zeros that precede and/or follow the bit to be preshifted.

The controller precompensation algorithm is only concerned with the four conditions illustrated in Figure 2-8. Any other combination of serial data bits does not require preshifting. The algorithm consists of continuously examining a 4-bit pattern (the bit to be written in the current interval; the bit to be written next; and the two immediately preceding bits) and, based on that pattern, either leaving the pulse to be written in its nominal position or advancing or delaying the pulse by 15 nanoseconds.

Thus, for the bit pattern 1000 shown in Figure 2-8, the third bit must be preshifted 15 nanoseconds to the right (delayed) to compensate for a peak shift to the left. For the bit pattern 0001, the third bit must be preshifted 15 nanoseconds to the left (advanced) to compensate for a peak shift to the right, and so forth.

2.2.4   Bad Sector File

The Bad Sector File is a list of all bad sectors found on an RLØ1K or RLØ2K Disk Cartridge. The file also stores the cartridge serial number. This information is used by the operating system to avoid allocating user data to a bad sector.

The criteria for determining that a sector is bad are as follows:

● Inability to read a sector header

● 16 consecutive read/write errors within one sector.

This file is recorded on surface "1" of the last (innermost) cylinder. This track contains 40 sectors of 128 words each. The contents of the file are shown in Figure 2-9.
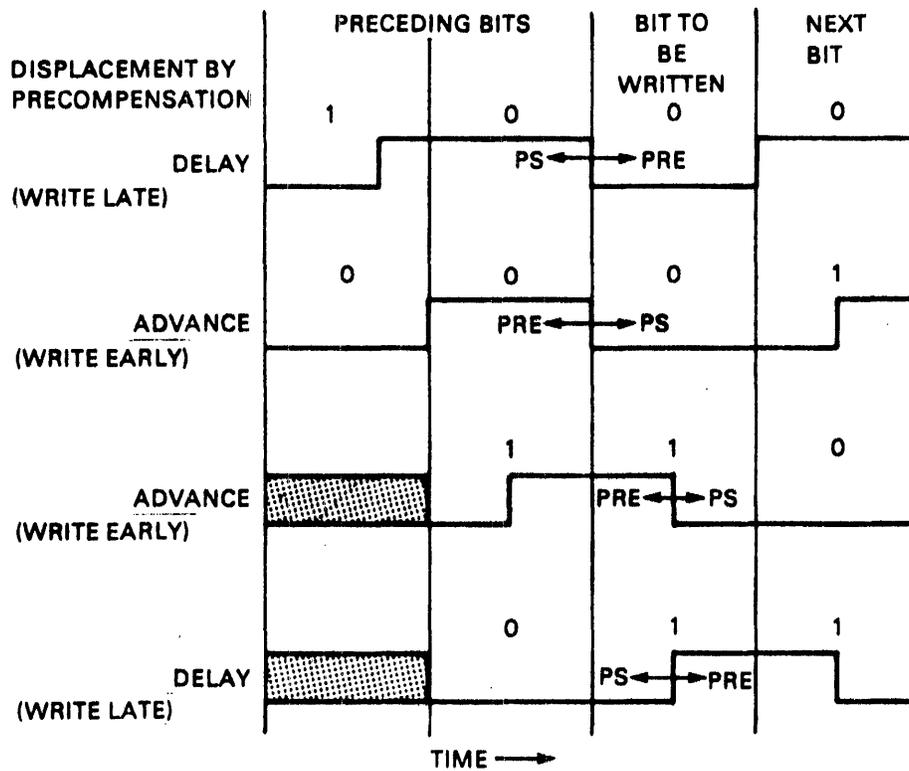
Figure 2-8   MFM Precompensation

BAD SECTOR FILE

SEC TOR	CONTENTS
0 / 1	FACTORY WRITTEN BAD SECTOR INFO
2 / 3	ALL ONES
4 / 5	DUPLICATE OF SECTORS 0, 1
6 / 7	ALL ONES
8 / 9	DUPLICATE OF SECTORS 0, 1
10 / 11	ALL ONES
12 / 13	DUPLICATE OF SECTORS 0, 1
14 / 15	ALL ONES
16 / 17	DUPLICATE OF SECTORS 0, 1
18 / 19	ALL ONES
20 / 21	FIELD WRITTEN BAD SECTOR INFO
22 / 23	ALL ONES
24 / 25	DUPLICATE OF SECTORS 20, 21
26 / 27	ALL ONES
28 / 29	DUPLICATE OF SECTORS 20, 21
30 / 31	ALL ONES
32 / 33	DUPLICATE OF SECTORS 20, 21
34 / 35	ALL ONES
36 / 37	DUPLICATE OF SECTORS 20, 21
38 / 39	ALL ONES

LAST CYLINDER
LAST SURFACE

TWO SECTORS

256 16 BIT WORDS

125 ENTRIES

WORD	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
0	ZERO	5 MOST SIGNIFICANT OCTAL DIGITS OF CARTRIDGE SERIAL NUMBER														
1	ZERO	5 LEAST SIGNIFICANT OCTAL DIGITS OF CARTRIDGE SERIAL NUMBER														
2	ZEROES															
3	ZEROES															
4	ZEROES								CYLINDER ADDRESS							
5	ZEROES							HEAD	ZEROES		SECTOR ADDRESS					
6	SAME FORMAT AS FIRST BAD SECTOR ENTRY															
7																
252	SAME FORMAT AS FIRST BAD SECTOR ENTRY															
253																
254	ALL ONES															
255	ALL ONES															

FIRST BAD SECTOR ENTRY (words 4, 5)

SECOND BAD SECTOR ENTRY (words 6, 7)

125th BAD SECTOR ENTRY (words 252, 253)

NOTE: UNUSED BAD SECTOR ENTRIES ARE ALL ONES

CZ-2020

Figure 2-9   Bad Sector File Format

3.1 Controller/Drive Interface Line Descriptions

The Control Unit/Drive Interface Bus comprises twelve differential signal lines and one single ended power fail line. Figure 3-1 shows the Control Unit/Drive Interface Lines. A maximum of four RL01 and/or RL02 Disk Drives may be daisy-chained to the controller via this bus.

Drives are selected by means of two binary encoded select lines. The selected drive indicates that it is ready to receive commands by asserting the Drive Ready line.

When the drive is ready, Seek, Head Select and Read Status commands can be transmitted serially. Drive status is transmitted to the controller as a serial word when requested by the Get Status Command.

Read or write data is encoded in serial MFM format.

During the absence of any command and whenever the disk drive is selected and ready, it is transmitting serial read data to the controller.

Table 3-1 describes the Drive Bus Interface Lines in detail.

DRIVE SELECT 0 (DR SEL 0)

DRIVE SELECT 1 (DR SEL 1)

WRITE GATE (WR GATE)

WRITE DATA (WR DATA)

SYSTEM CLOCK (SYS CLK)

DRIVE COMMAND (DR CMD)

POWER FAIL (PWR FAIL)

DRIVE READY (DR RDY)

STATUS CLOCK (STATUS CLK)

SECTOR PULSE (SEC PLS)

READ DATA (RD DATA)

DRIVE ERROR (DR ERR)

STATUS (STATUS)
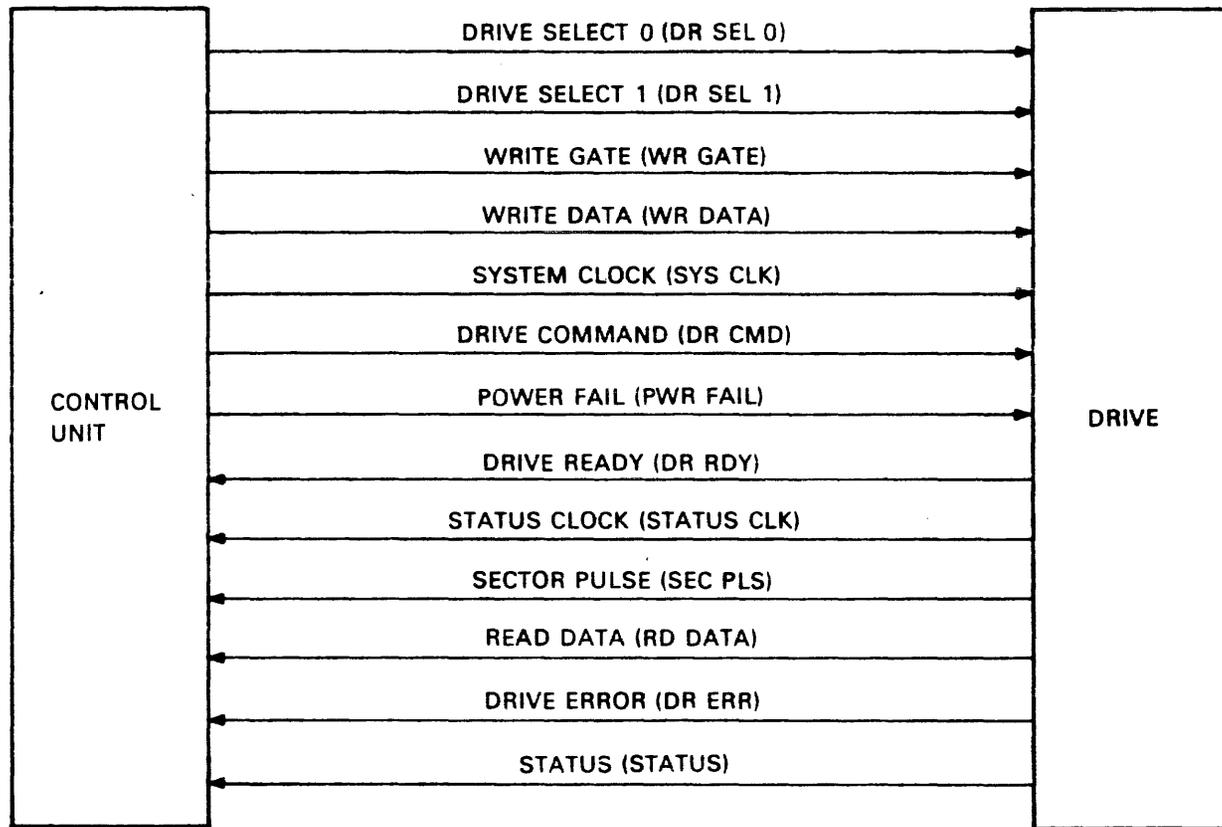
CONTROL
UNIT

DRIVE

MA-0580

Figure 3-1 Control Unit/Drive Interface Lines

Table 3-1   Drive Bus Interface Lines

Signal Name

Function

Drive Select 0,
Drive Select 1
(DR SEL 0, DR SEL 1)

These two lines select one of four disk drives. The drive must be selected 500 ns +10% before a Write Gate or Serial Drive command word is sent to the drive. One drive is always selected even though the controller is idle. Only the selected drive asserts the drive-to-controller interface lines, and these lines are valid 500 nanoseconds after the drive has been selected. A drive will inhibit transmission of a partial sector pulse if it is selected while its sector pulse is asserted.

Write Gate
(WR GATE)

This line enables the write circuits in the selected drive. It must be asserted at the start of Preamble PR2, and must precede the first bit of write data by 0 to 250 nanoseconds. Write Gate must not be asserted during a sector pulse; otherwise, a Write Gate Error will be asserted by the drive (bit 10 of status word) and operation terminated. Write Gate is removed at the end of Postamble PO2 (0 to 250 nanoseconds).

Write Data
(RW DATA)

This line contains the serial data, encoded in Modified Frequency Modulation (MFM) pulse form, that is to be written on the disk.

System Clock
(SYS CLK)

This clock shifts the Drive Command word to the drive and also operates the disk motor servo. Clock frequency is 4.1 Megabits/second +0.1%.

Drive Command
(DR CMD)

This line is used to transfer control and cylinder address difference information serially to the drive. It is enabled during Seek, Get Status or commands.

Power Fail
(PWR FAIL)

This signal is received by all drives at all times, regardless of which drive is selected. When the subsystem is first powered up, Power Fail is negated high. If AC power in the controller is subsequently lost or out of tolerance, Power Fail is asserted low, in which case the drives unload heads and cycle down. Return of power causes the drives to cycle up and load heads over track 0.

Drive Ready

When asserted high, this signal indicates that the selected head is centered on the track, and the drive is ready to receive a command. The signal goes low: (1) after the last bit of a cylinder address difference word has been shifted to the selected drive; (2) when a new head select is transfered to the drive, even though the address difference is zero; and (3) when there is an address difference of zero and no head select change is shifted to the drive.

Drive ready will go low when a drive error occurs. There are two exceptions to this. The first is when an attempt has been made to write on a write protected drive. In that case, only drive error will be asserted high. The second exception is that whenever the heads are loaded, for whatever reason, the volume check bit will be set and drive error will be asserted high.

Status Clock
(STATUS CLK)

This clock is the System Clock delayed through drive logic and returned to the controller when a status word is requested. The clock is turned on in sync with the first bit of the status word and remains in sync until: (1) a new Drive Command marker is received at the input to the drive command shift register, or (2) the drive is de-selected.

Sector Pulse

This 625 microsecond pulse is asserted high (SEC PLS) and occurs every 625 microsecond +1%, 40 times per disk revolution. When a drive is initially selected, it must wait until the next full sector pulse is detected before sending the sector pulse to the controller.

The sector pulse received by the controller is generated by a magnetic reluctance sensor. The leading edge of the sector pulse has a tolerance of +13 microsecond relative to the recorded data. This tolerance is required for head gap and positioner alignment relative to the sector pulse.

Read Data
(RD DATA)

This line transfers MFM encoded data from the drive read circuits to the controller. During the absence of any command and whenever a drive is selected and Drive Ready is asserted, Read Data appears on this line.

The drive senses the amplitude of the header preamble and sends Read Data over the Read Data line 2.5 +0.5 microsecond downstream from where the preamble actually starts.

For reading headers, the VFO loop is phaselocked with the arrival of Read Data after the end of the sector pulse.

For the data preamble, the VFO locks 32 read pulses after the header CRC to avoid transmitting erroneous sync pulses to the clock at the transition between the pre-recorded header and the data preamble. Detection of the preamble marker commences after the VFO has had time to phase lock.

Drive Error
(DR ERR)

This signal is asserted high on certain drive errors. Any attempt to write on a write protected drive also causes this signal to be asserted high. Asserting Drive Error causes bits 14 and 15 of the CS register to be set. The particular error involved can then be determined by initiating a Get Status command and reading bits 10, 11, 12, 14, and 15 of the status word.

The Drive Error latch can be reset by:

1. Manual disk power down/power up

2. Setting bit 3 of the serial Drive
    Command (bit 3 of the Disk Address
    register during a Get Status command)

3. Removing the Write lock condition via
    the drive front panel.

3.2   DRIVE COMMAND WORD
Figure 3-2 shows the Drive Command Word configuration.

The drive command word is sent to the drive serially over the
drive command line. After the drive has received a command word
(16 bits) without the Get Status bit set, the cylinder difference
address is loaded into a cylinder difference counter and the head
select bit is latched in a separate register.   The drive
immediately drops Drive Ready for a minimum of 6.5 milliseconds.
This delay allows the selected head to reposition in case the
cylinder difference address was zero and only a new head select
bit was sent.   Any cylinder difference count other than zero
causes the head to move to a different track location indicated by
the count and the sign bit (bit 2). As soon as the selected head
reaches the new cylinder location, the 6.5 milliseconds timeout is
again initiated. The selected head must stay positioned within a
tolerance band during the timeout. Only then, and at the end of
the 6.5 milliseconds period, will Drive Ready again be asserted
high. A Seek Timeout error (bit 12 of status word) will occur if
the selected head fails to lock back on a track within 1.5
seconds. This is the method by which the drive is commanded to do
a seek.

Marker (Sync) - When received at the drive, the Marker bit enables
the drive command shift register to receive the drive command.
When the Marker bit has shifted to the end of the drive command
shift register, it indicates that the drive has received the full
command word.

Get Status - When the drive receives the Get Status bit, it knows
that the controller is requesting the drive to send its status.
It will then shift the drive status word to the controller. Bits
15:04 of the command are ignored during this operation.

Sign - The Sign bit indicates the direction in which the heads
will move. A one in the sign position moves the heads toward the
spindle (i.e., to a higher cylinder address); a zero moves the
heads away from the spindle.

Reset - When asserted, the Reset bit clears all error sense bits in the drive. If the error condition that set the error sense bits has been removed, the error sense bits will remain cleared. However, if the error condition persists, the error sense bits will remain set after the appropriate timeout.

Head Select - When this bit is cleared, the head on the upper surface of the disk is selected (head 0). When this bit is set, the head on the lower surface of the disk is selected (head 1).

Cylinder Address Difference - The cylinder address difference is the magnitude of the programmed seek (i.e., the number of tracks the heads are to move). Transmission of zero difference and no change in head selection should be avoided, since a 6.5 msec timeout will occur before the drive again becomes ready. The relationship between the System Clock and the Drive Command bits is shown in Figure 3-3. If the Reset bit (bit 3) is asserted together with the Get Status bit, (bit 1) the drive will first reset all drive error latches and then send status back to the controller.

3.3 GET STATUS COMMAND AND RESPONSE
In response to a Get Status command, the drive enables Status Clock and sends the status word (Figure 3-4) to the controller via the Status line. This function can be performed even though Drive Ready is not present (i.e., during power up or a seek). Contents of the status word are as listed in Table 3-2 and placed into the Multi-Purpose Register (MPR) of the controller.

```
 15  14  13  12  11  10   9   8   7   6   5   4    3    2    1   0
┌───┬───┬───┬───┬───┬───┬───┬───┬───┬───┬───┬────┬────┬────┬────┬───┐
│ 0 │128│64 │32 │16 │ 8 │ 4 │ 2 │ 1 │ 0 │ 0 │ HS │RST │ SN │ GS │ M │
└───┴───┴───┴───┴───┴───┴───┴───┴───┴───┴───┴────┴────┴────┴────┴───┘
```

CYLINDER ADDRESS
DIFFERENCE (2_8 = 256)

HEAD SELECT
(0 = UPPER, 1 = LOWER)

RESET

SIGN
((1 = MOVE HEADS TOWARD SPINDLE
  0 = MOVE HEADS AWAY FROM SPINDLE))

GET STATUS

MARKER (SYNC)
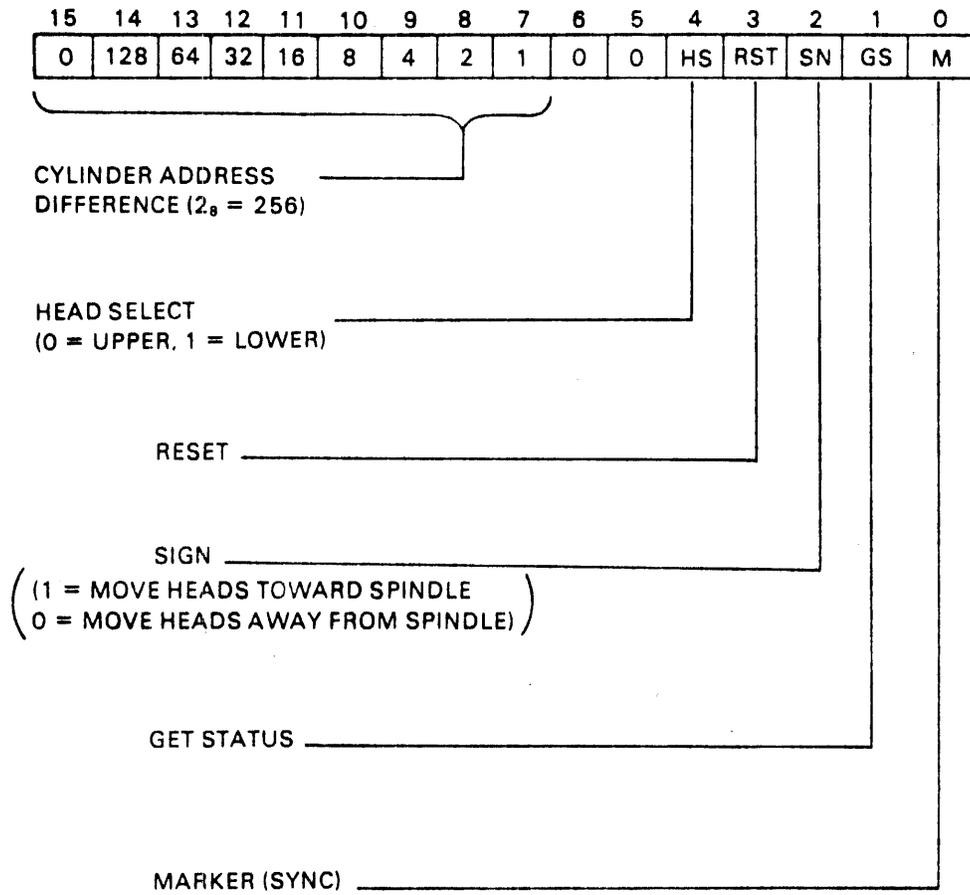
CZ-1038

Figure 3-2   Drive Command Word Configuration

IF DRIVE COMMAND IS NOT
"GET STATUS", THIS TIME MUST BE 0 TO 4 μSEC.

SECTOR
PULSE

DRIVE
COMMAND   BIT 0 | BIT 1 | BIT 2 |
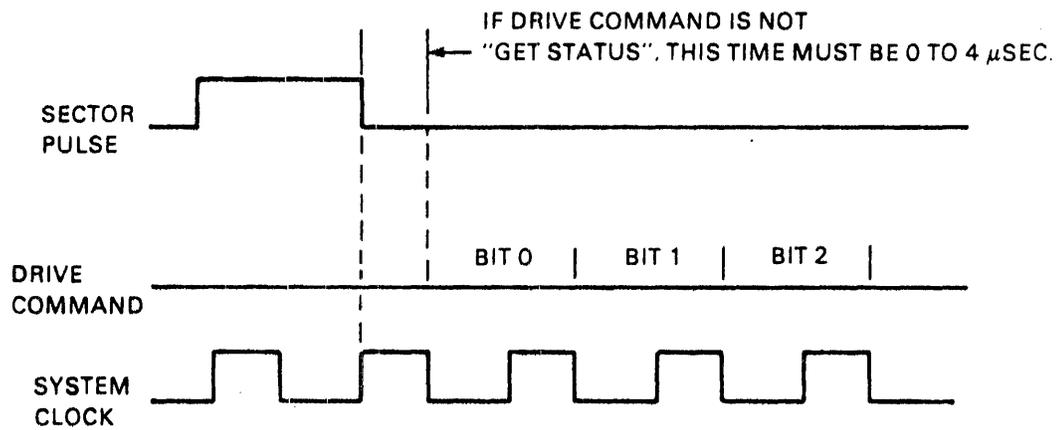
SYSTEM
CLOCK

CZ-1018

Figure 3-3   Relationship Between System Clock
and Drive Command Word Bits

I/3-9

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WDE	CHE	WLS		SPE	WGE	VC	DSE	0	HS	CO	HO	BH	STC	STB	STA

SKTO

DRIVE ERRORS   DRIVE STATUS   DRIVE STATE

STATUS CLOCK

| STATUS WORD | BIT 0 | BIT 1 | BIT 2 | BIT 3 | BIT 13 | BIT 14 | BIT 15 | 0 |
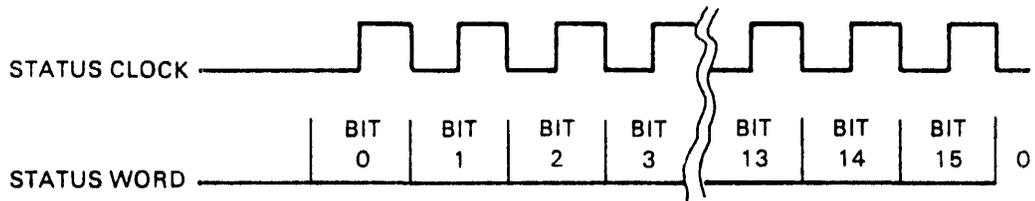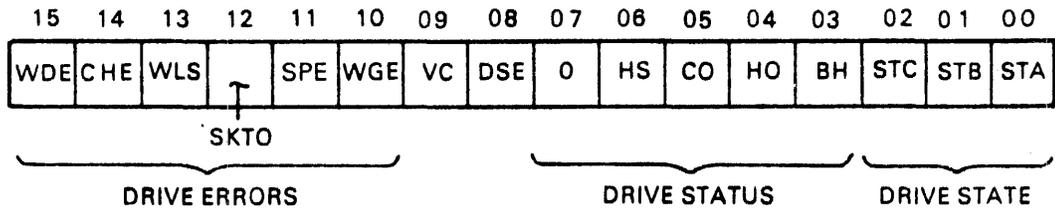
CZ-1019

Figure 3-4   Drive Status Word

I/3-10

Table 3-2   Drive Status Word

Bit(s)   **Function**

Bits 0-2   These bits define the state of the drive:

STC	STB	STA	
0	0	0	Load Cartridge State
0	0	1	Spin Up
0	1	0	Brush Cycle
0	1	1	Load Heads
1	0	0	Seek-Track Counting
1	0	1	Seek-Linear Mode (Lock On)
1	1	0	Unload Heads
1	1	1	Spin Down

Bit 3   Brush Home (BH). Asserted high when the brushes are not over the disk.

Bit 4   Heads Out (HO). Asserted high when the heads are over the disk, and low when positioner is retracted to home position.

Bit 5   Cover Open (CO). Asserted high when the cover is open or the dust cover is not in place.

Bit 6   Head Selected (HS). Identifies the currently selected head. This bit is zero to indicate the upper head (head 0).

Bit 7   Reserved. Must be a zero.

Bit 8   Drive Select Error (DSE). Asserted high by drive that first senses a multiple select.

Bit 9   Volume Check (VC). When high it indicates the heads have been unloaded since the last drive dialogue.

Bit 10   Write Gate Error (WGE). Indicates that the drive
            sensed a Write Gate when the Sector Pulse was asserted.
            Asserted high if the Write Gate remains asserted at the
            arrival of the next sector pulse, or after 625 micro-
            seconds have elapsed since the previous sector pulse.
            If Write Gate is asserted during the Sector Pulse, the
            drive will negate the Write Gate, and set an error
            flag.

Bit 11   Spin Error (SPE). Indicates the spindle did not reach
            speed in 40 seconds or is overspeeding by ±15 micro-
            seconds per 625 microseconds sector.

Bit 12   Seek Time Out (SKTO). Indicates the heads did not come
            on track in the required time during a Seek Command (15
            seconds) or have gone off track (no seek) for 1.5
            seconds.

Bit 13   Drive Write Locked. This is interpreted in two ways:

            1.   Status bit. Indicates to the system user that the
                 selected drive is in Write Lock Status (WLS).

            2.   An attempt to write on a write protected drive
                 (protected via front panel switch) causes the
                 Drive Error line to get asserted high. Since
                 Drive Ready will not drop for this particular
                 error, the controller may report a Write Lock
                 Error at that instant. From a subsequent Get
                 Status command, the diagnostic may verify that, in
                 fact, the drive was Write Locked.

Bit 14   Head Current Error (HCE). Indicates write current was
            detected in the heads even though Write Gate was not
            asserted.

Bit 15   Write Data Error (WDE). Indicates Write Gate was
            asserted but no transitions were detected on the Write
            Data line.

4.1 DEVICE OPERATIONS

The RLØ1/RLØ2 Disk Drive can be functionally divided into two different areas: internal functions (or internal machine cycles) and external functions (or responses to controller commands). The internal machine cycles are listed below.

- Load Cartridge
- Spin Up
- Brush
- Load Heads
- Seek
- Lock On
- Unload Heads
- Spin Down

The four external functions or controller commands that the drive functionally reacts to are Get Status, Seek, Read Data and Write Data. The other controller commands are invisible to the Disk Drive and are functionally handled in the controller.

4.2 INTERNAL MACHINE CYCLES

The RLØ1/RLØ2 Disk Drive, once power is applied, will be in one and only one of the eight machines states listed above at any time. This is accomplished by the State Control Logic, and primarily by the state ROM. This device monitors internal conditions and external inputs to control the state of the drive. The state ROM controls the sequencing through the states as well as protecting the drive during error conditions. The responses to error conditions and drive failures are explained in the description of each cycle.

Functional block diagrams and timing diagrams are presented to show what happens in each cycle and during the transition into and out of each cycle. Each function block is treated as a "black box". Control signals and data paths are emphasized to show their relationship to the device operations. Details of the "black boxes" are found in Chapter 5. The functional block diagrams and timing diagrams use signal mnemonics and Field Maintenance Print Set references.

Figure 4-1 is a block diagram of the RLØ1/RLØ2 Disk Drive. The detailed logic has been broken down into functional blocks and is keyed to the structure of the RLØ1 and RLØ2 Print Sets. The Drive Logic Module, which represents most of the drive electronics, comprises the areas in the block diagram that are listed below.

- State Control Logic (DL1)
- Velocity Command Status Data Control Logic (DL2)
- Count Logic (DL3)
- Disk Speed Control Logic (DL4)
- Error Logic (DL5)

- Interface Logic (DL6 and DL8)
- Integrator Logic (DL7)

The remaining drive electronics are contained on the separate modules listed below.

- DC Servo and Power Supply Module
- AC Servo Module
- Read/Write Board
- Front Panel Board
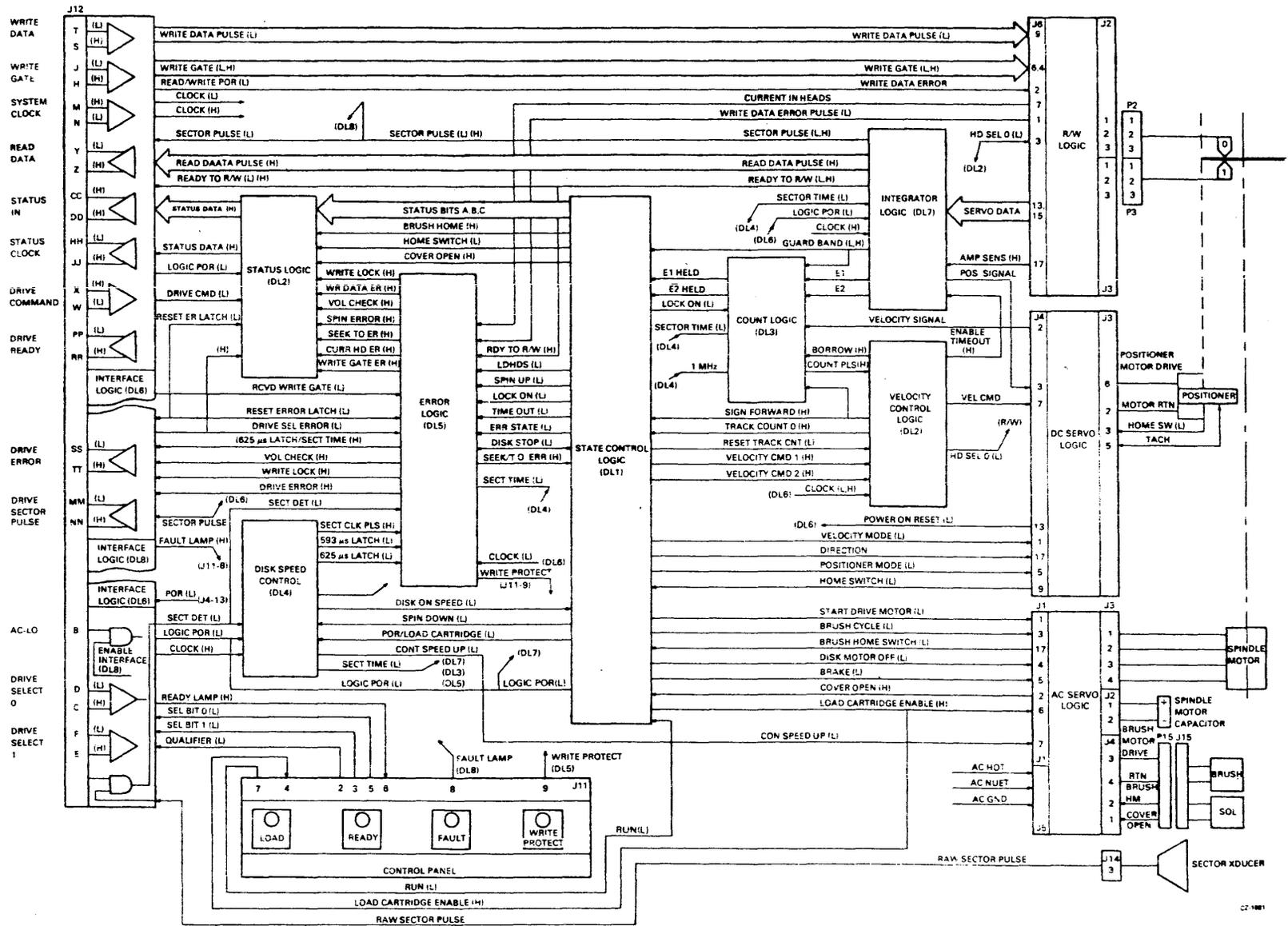
Figure 4-1 Disk Drive Detailed Block Diagram

The electromechanical assemblies and subassemblies listed below
are represented by the detailed block diagram.

- Positioner Assembly

    - Tachometer Signal

    - Read/Write Heads

    - Positioner Drive Motor

- Spindle Assembly

    - Spindle Drive Motor

    - Drive Motor Capacitor

    - Sector Transducer

- Brush Motor

- Cartridge Access Cover Locking Solenoid

All drive control signals, data paths and connector pin numbers
are defined by the detailed block diagram.

4.2.1 Power Up
Power Up is not considered here as a machine state, but is treated
as a special situation, as well as a convenient entry into the
machine cycle descriptions. When power is applied to the drive
the signal Power On Reset is generated. This signal resets
internal functions and therefore goes to much of the circuitry.
At this time the machine is forced to a special case of the "Spin
Down" state. (See Figure 4-16 of Spin Down.) While in this state
the spindle is energized but in brake mode (turning slowly) and
waiting for the disk stopped timer to time out. Notice the LOAD
light is not yet energized (by LOAD CART EN (H)). When the timer
times out (after approximately 15 seconds), transition into the
Load Cartridge cycle should happen. A detailed explaination of
Load Cartridge is found in Paragraph 4.2.2.

4.2.2 Load Cartridge Cycle - Figure 4-2 is a functional diagram
showing control signals and data paths which are enabled during
the Load Cartridge cycle of Device Startup. Figure 4-3 is a
timing diagram which shows the sequence of events which start and
end this cycle.
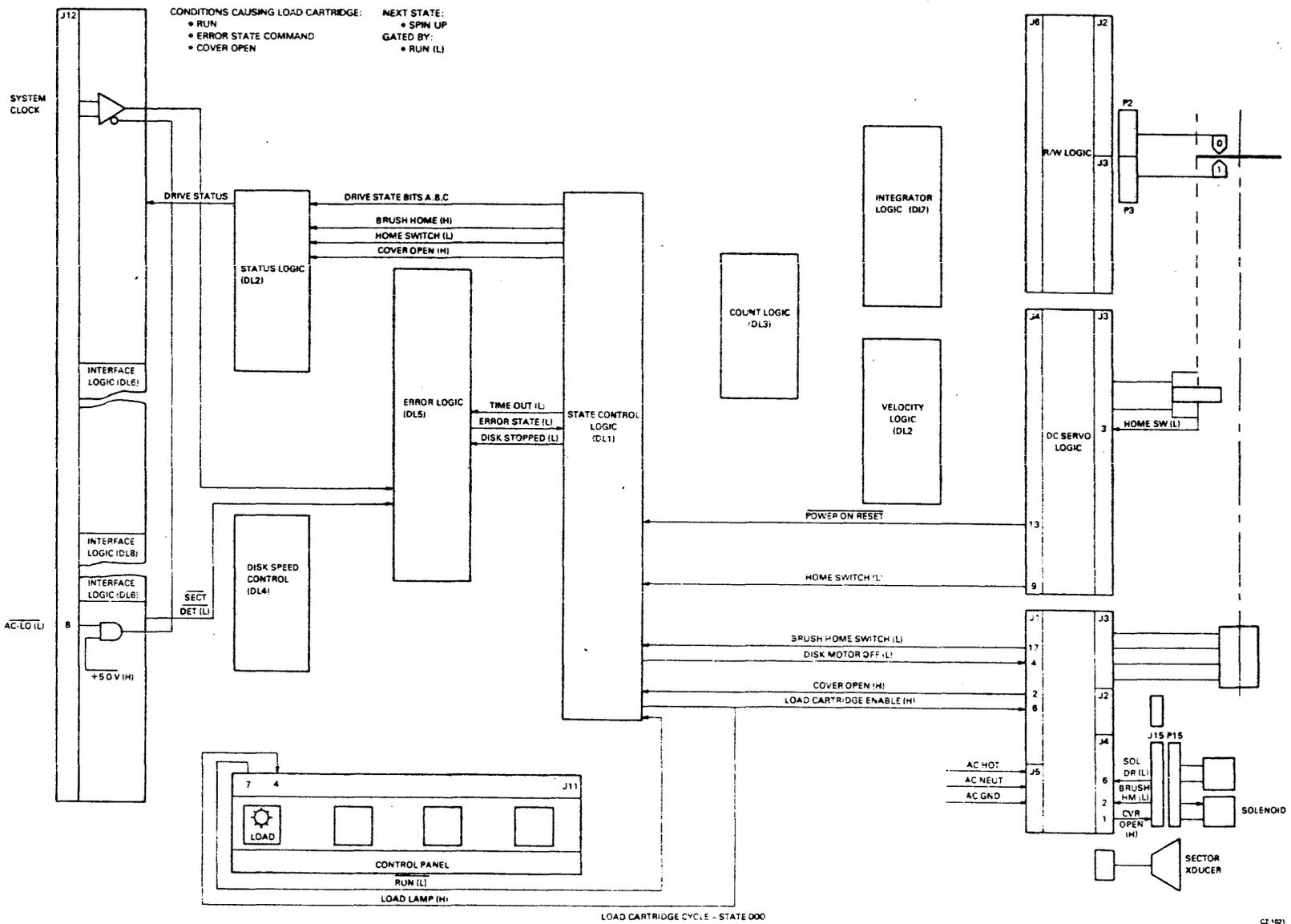
Figure 4-2 Device Startup - Load Cartridge Cycle
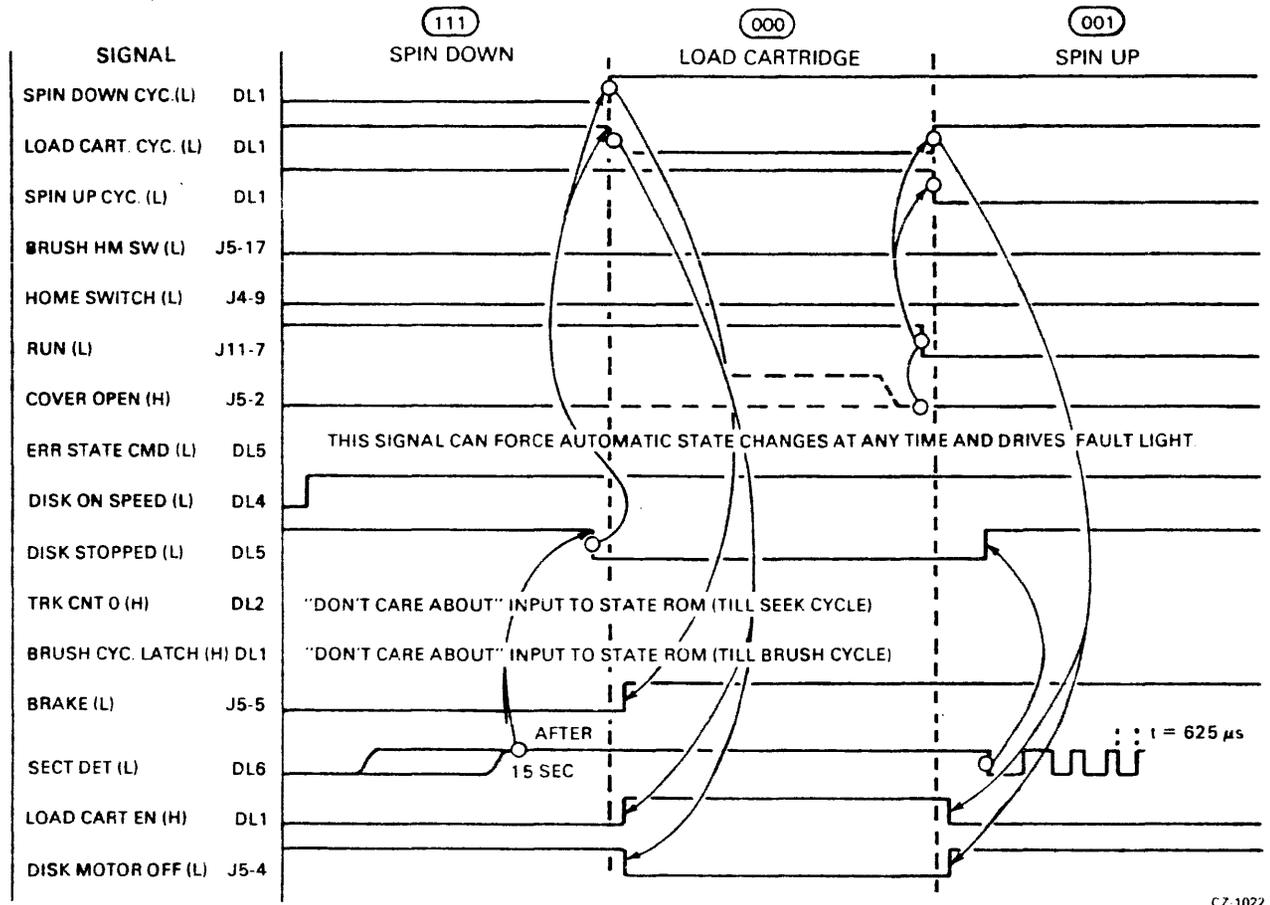
Figure 4-3 Device Startup - Load Cartridge Timing

These are the preconditions for the Load Cartridge cycle.

- The Cartridge Access Cover Solenoid has sensed that the cover is open and the RUN switch has not been depressed

- The brushes are in the home position

- The Read/Write heads are home

- No sectors are being detected (i.e., the spindle is stopped).

If these conditions have been met, the LOAD indicator on the Control Panel will be illuminated.

When the cartridge is loaded and the cover is closed, the next cycle for Device Start up is "spin-up". This cycle is started by depressing the RUN pushbutton.

It is possible that the controller may be requesting status during this cycle. In this case, the drive state bits (A, B, and C) would signify 0_8 or "load cartridge".

4.2.3 Spinup Cycle - Figure 4-4 is a functional diagram showing control signals and data paths which are enabled during the Spinup cycle of Device Startup. Figure 4-5 is a timing diagram which shows the sequence of events which start and end this cycle.

These are the preconditions for the spin-up cycle.

- The cartridge must be loaded with dust cover in place and the cover closed

- The brushes must be in the home position

- The heads must be in the home position

- The disk must be stopped

- The drive must be selected

If these conditions have been met, the spinup cycle will begin when the RUN switch is depressed. At this time, Start Drive Motor (L) will be asserted. Power will be applied to the Spindle Drive Motor and it will begin to rotate the spindle. As the disk turns, the sector slots located on the cartridge armature plate will be sensed by the sector transducer. As each sector slot is sensed, the Sector Detected (L) signal will be asserted. As soon as the time between sector pulses is between 594 and 624 microseconds, the disk speed control logic (DL4) will send Disk On Speed (L) to the State Control Logic (DL1). This signal begins Brush Cycle.

I/4-8

REQUIRED PRECONDITIONS FOR SPIN UP STATE:
- COVER CLOSED
- BRUSHES HOME
- HEADS HOME
- ON SPEED
- ERROR STATE COMMAND
- RUN

NEXT STATE:
- BRUSH CYCLE
GATED BY:
- DISK ON SPEED (L)

J12

J8   J2
R/W LOGIC
J3
P2
P3
0
1

INTEGRATOR LOGIC (DI7)

DRIVE STATUS   DRIVE STATE BITS A,B,C
                      BRUSHES HOME (H)
                      HOME SWITCH (L)
                      COVER OPEN (H)

STATUS LOGIC (DL2)

CLOCK (H)

COUNT LOGIC (DL3)

INTERFACE LOGIC (DL8)

ERROR LOGIC (DL5)   TIME OUT (L)
                       ERROR STATE (L)
STATE CONTROL LOGIC (DL1)

VELOCITY LOGIC (DL2)

J4   J3
DC SERVO LOGIC

RESET TRACK COUNT (L)

SECT DETECTOR (L)

INTERFACE LOGIC (DL8)

DISK SPEED CONTROL (DL4)

INTERFACE LOGIC (DL8)

HEADS HOME SWITCH (L)

DISK MOTOR OFF (L)

BRUSH HOME SWITCH (L)

J1
1
17

J3
1
2
3
4

SPINDLE MOTOR

AC SERVO LOGIC
J2
J4

AC HOT
AC NEUT   J5
AC GND

J12

7   J11
RUN
CONTROL PANEL
RUN (L)

RAW SECTOR PULSE

SECTOR XDUCER

SPIN UP CYCLE STATE (001)

CZ 1023

Figure 4-4   Device Startup – Spin-up Cycle
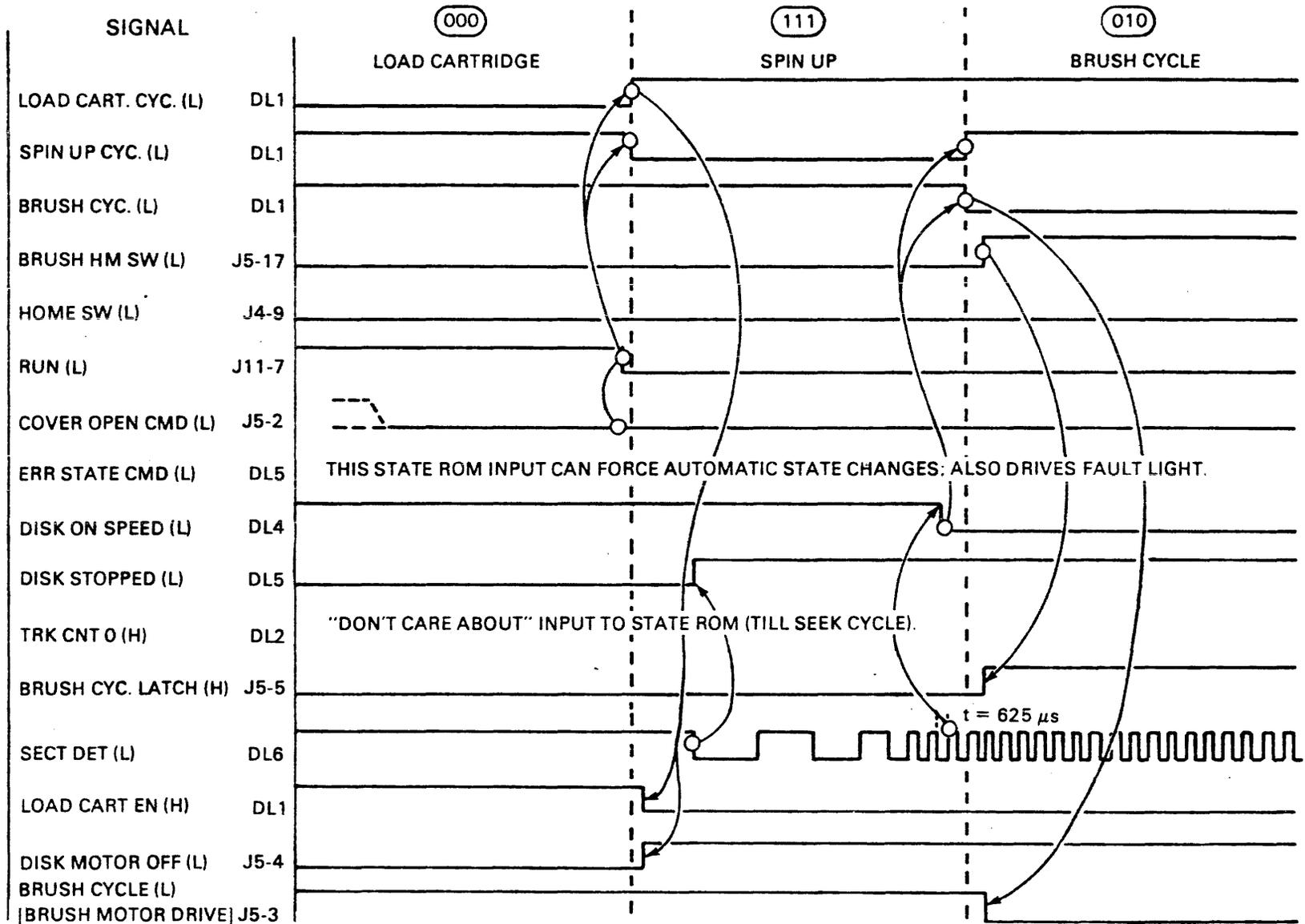
Figure 4-5 Device Startup - Spin-up Cycle Timing

CZ-1024

I/4-9

4.2.4   Brush Cycle – Figure 4-6 is a functional diagram showing control signals and data paths which are enabled during the Brush Cycle of Device Startup. Figure 4-7 is a timing diagram which shows the sequence of events which start and end this cycle.

The brush cycle is entered when the disk speed control (DL4) detects the spindle is up to speed. When the drive is in the Brush cycle, the following conditions exist.

●   This disk is spinning up to speed (Control Circuit active)

●   The brush drive is energized (brushes sweeping out over the disk).

The cycle is provided to allow the brushes to clean any debris that may be out on the disk surface prior to loading heads. The next cycle after Brush Cycle is Load Heads and the transition occurs when the brushes return to the home position. The signal Brush Home SW (L) resets the Brush latch forcing the state ROM change.

4.2.5   Load Heads Cycle – Figure 4-8 is a functional diagram showing control signals and data paths which are active during the Load Heads Cycle of device startup. Figure 4-9 is a timing diagram showing the sequence of events which start and end this cycle.

These are the preconditions for the Load Heads cycle.

●   The cover must be closed
●   The heads must be home
●   The brushes must be home and have completed a brush cycle
●   No drive errors are sensed
●   The disk must be on speed

As soon as the brush cycle is completed, the drive begins the Load Heads Cycle. The State Control Logic (DL1) sends a binary velocity command (10) to the DC Servo Logic which, in turn, initiates a six ips velocity command to the positioner drive motor.

REQUIRED PRECONDITIONS FOR BRUSH CYCLE: NEXT STATE:
- COVER CLOSED   • LOAD HEADS
- BRUSHES HOME   GATED BY:
- HEADS HOME   • BRUSH CYCLE LATCH (F
- DISK STOPPED
- ON SPEED

DRIVE STATUS

DRIVE STATE BITS (A,B,C)
BRUSHES HOME (L,H)
HOME SWITCH (L)
COVER OPEN (H)

STATUS LOGIC (DL2)

INTERFACE LOGIC (DL8)

INTERFACE LOGIC (DL8)

INTERFACE LOGIC (DL6)

ERROR LOGIC (DL5)

TIME OUT (L)
ERROR STATE (L)
DISK STOPPED (L)

STATE CONTROL LOGIC (DL1)

RESET TRACK COUNT (L)

COUNT LOGIC (DL3)

INTEGRATOR LOGIC (DL7)

VELOCITY CONTROL LOGIC (DL2)

R/W LOGIC

DC SERVO LOGIC

DISK SPEED CONTROL (DL4)

DISK ON SPEED (L)

BRUSH CYCLE (L)
BRUSH HOME SWITCH (L,H)

AC HOT
AC NEUT
AC GND

DRIVE
RTN
BRUSH
HM (L)

SECTOR XDUCER

CONTROL PANEL

BRUSH CYCLE - STATE 010

CZ 1025

Figure 4-6 Device Start-up - Brush Cycle
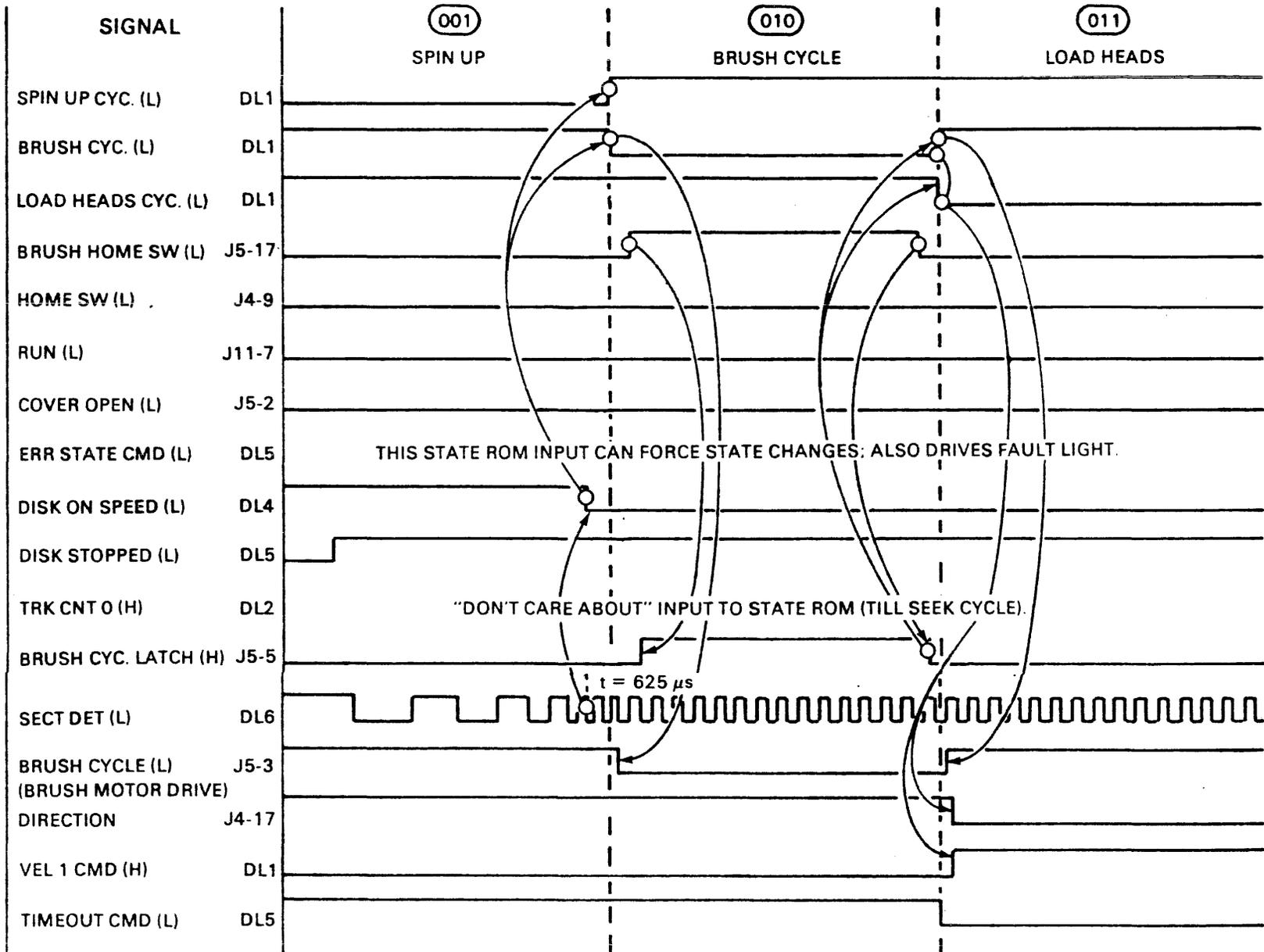
Figure 4-7 Device Start-up – Brush Cycle Timing
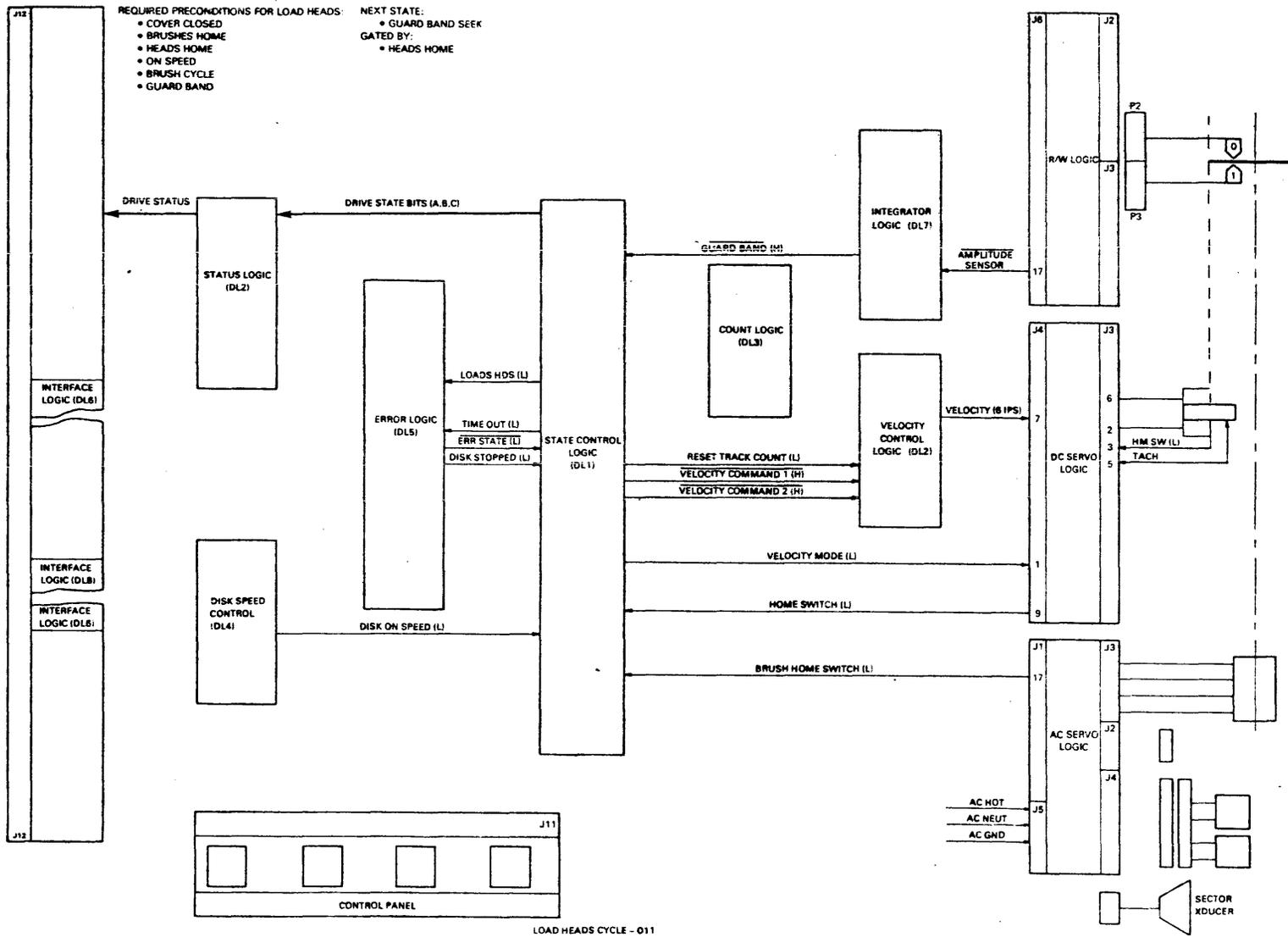
Figure 4-8   Device Start-up - Load Heads Cycle
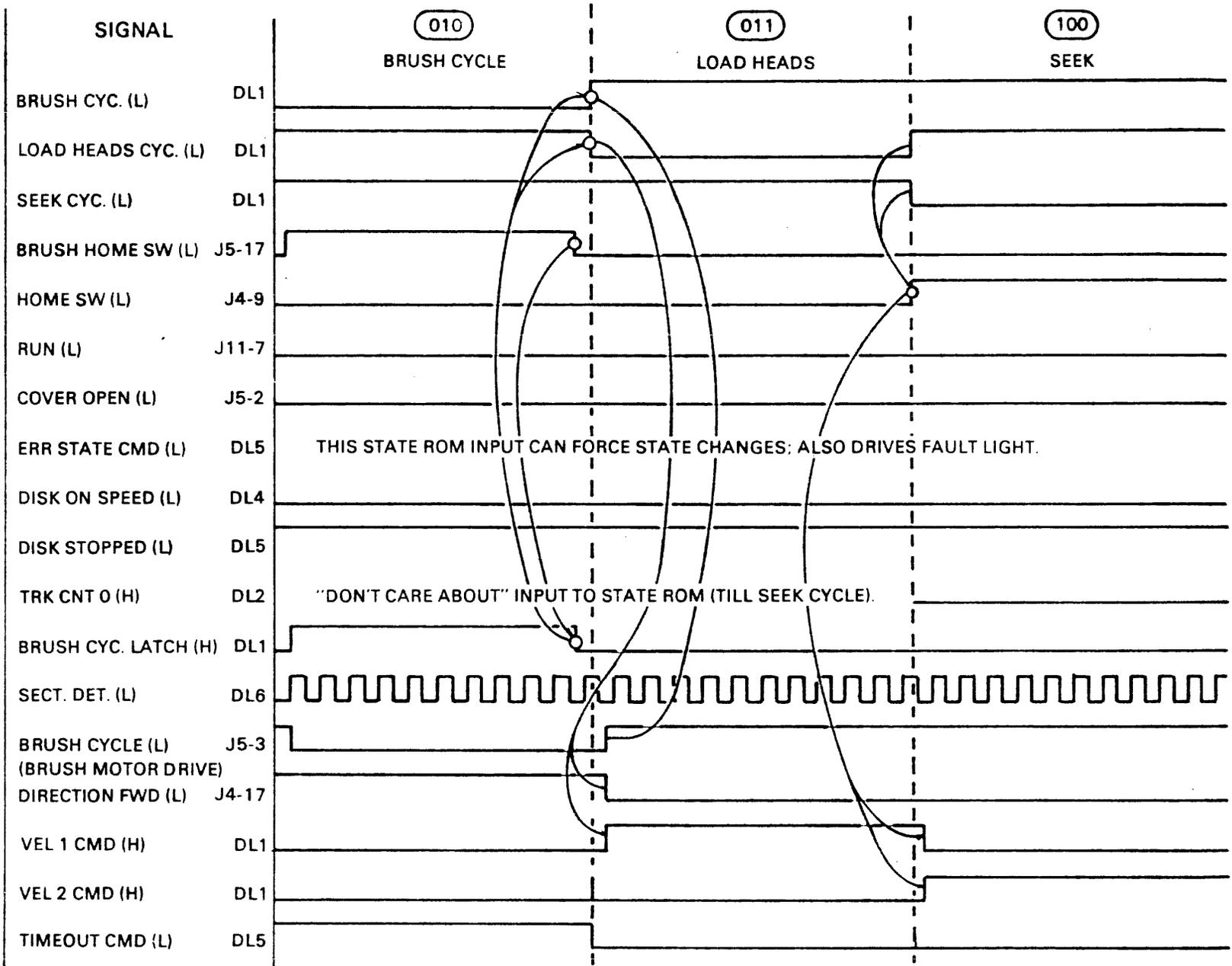
Figure 4-9 Device Start-up - Load Heads Cycle Timing

I/4-14

CZ-1028

The State Control Logic also produces the control signals listed below.

- Direction Forward (L) which instructs the positioner to move the heads toward the spindle

- Velocity Mode (L) which instructs the DC Servo Logic to accept a velocity command

- Reset Track Count (L) which clears the track counter

- Load Heads (L) is sent to the Error Logic (DL5) to produce Volume Check (H) which signifies that the cartridge may have been changed

The read/write heads are driven off the head loading ramp at six ips and out over the head loading portion of the disk surface. The drive enters the seek cycle as soon as the heads leave their home position.

4.2.6 Guard Band Seek Cycle - Figure 4-10 is a functional diagram showing control signals and data paths which are active during the Guard Bank Seek cycle of device startup. Figure 4-11 is a timing diagram showing the sequence of events which start and end this cycle.

These are the preconditions for the Guard Band Seek cycle.

- The cover must be closed
- The brushes must be home
- The heads must be loaded and moving
- No drive errors are being sensed
- The disk must be up to speed

As soon as the heads leave their home position, the drive enters seek mode. However, it must determine if it is performing a normal or a guard band seek.

As the read/write heads move across the head loading zone of the disk and into the outer guard band, the preformatted servo data is sensed. This produces the signal Amplitude Sensor (H) which simply acknowledges that some form of data is being read. Servo Data 1, Servo Data 2 and Amplitude Sensor (H) are sent to the Integrator Logic (DL7) where they are processed and decoded into servo sample signals E1 and E2.

The Integrator Logic determines that only one of the two guard band zones is being crossed due to the special prerecorded servo burst format (refer to Paragraph 2.2.3) and produces Guard Band (H).
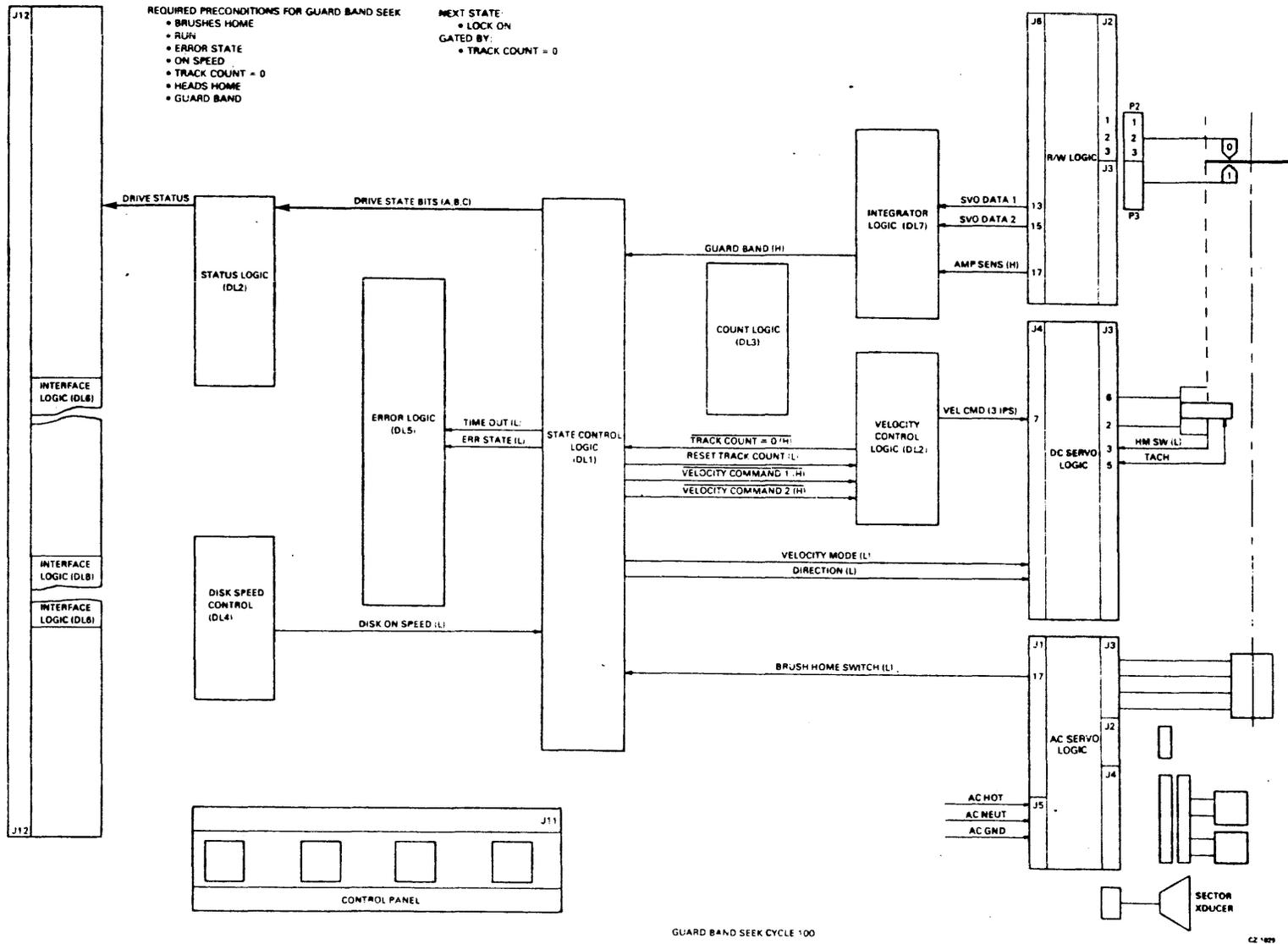
Figure 4-10 Device Start-up - Seek Cycle
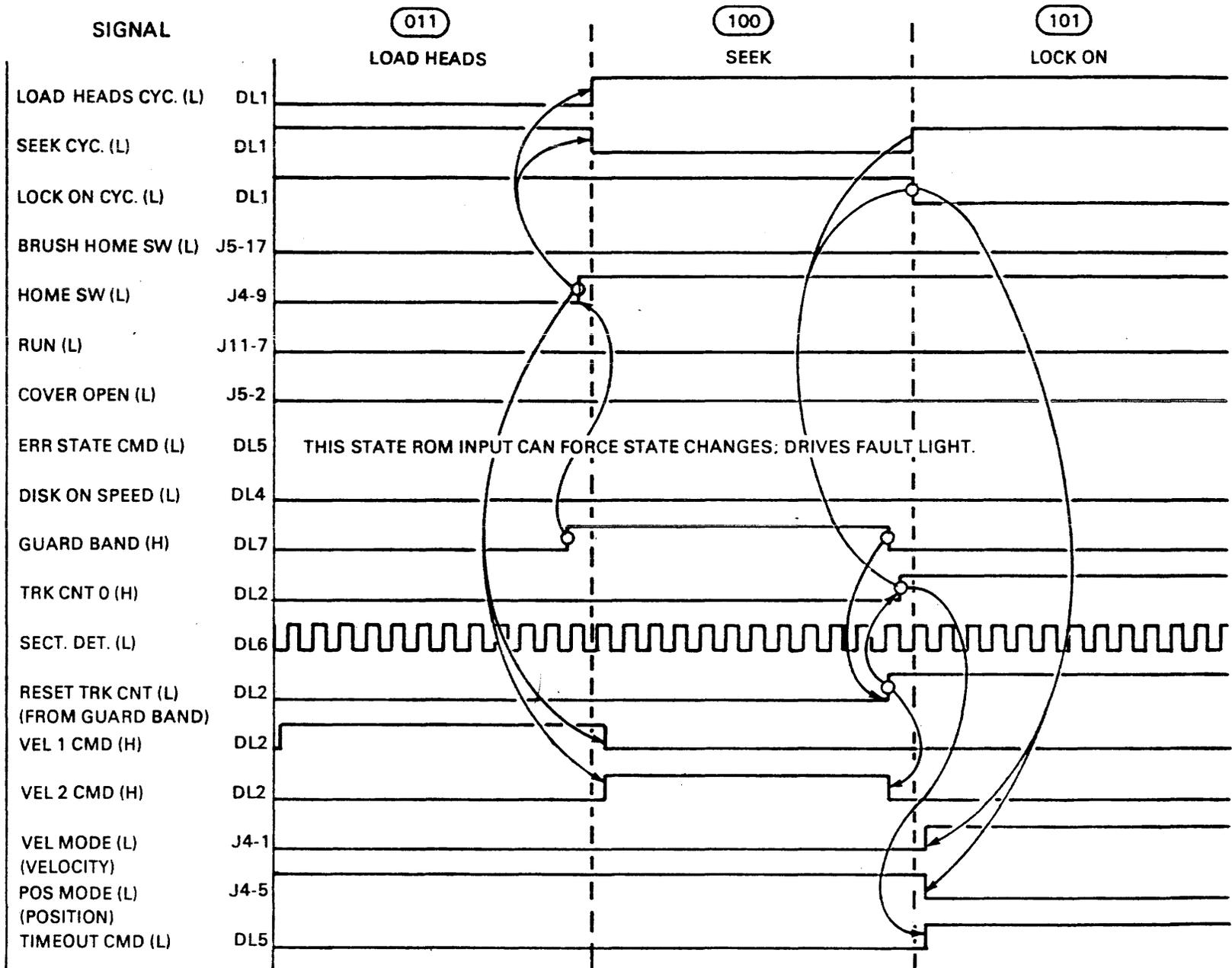
Figure 4-11 Device Start-up – Seek Timing

Again, due to the special servo format, the signal E1 Held is produced. This signal, in conjunction with Guard Band (H), allows the State Control Logic to determine that the positioner is crossing the outer Guard Band.

At this time, the Velocity Command changes to a binary 01. The Velocity Control Logic (DL2) reduces the previous Load Heads velocity command of six ips to three ips.

4.2.7   Lock on (Device Ready) - Figure 4-12 is a functional diagram showing the control signals and data paths which are active during the Lock On Track 0 cycle of Device Startup. Figure 4-13 is a timing diagram showing the sequence of events which start and end this cycle.

These are the preconditions for the Lock On Track 0 cycle.

● The cover must be closed

● The brushes must be home

● The heads must be loaded and traveling across the outer guard band

● No drive errors are being sensed

● The disk must be on speed

While the positioner is traveling across the outer Guardband zone, the read/write heads are only detecting S_1 servo bursts, due to the guard band servo format. As soon as S_2 bursts are detected, the intergrator logic (DL7) determines that the positioner is no longer within the guardband and causes the signal Guardband (H) to go low. This, in turn, causes Track Count = 0 (H) to be enabled which allows the State Control Logic (DL1) to change from Velocity Mode to Position Mode.

The signal Position Mode (L) instructs the DC Servo Logic to begin accepting incremental positioning signals from the Integrator Logic and to lock on to the negative slope of the positioner signal.

At the same time, a ready to read/write timeout is set which allows 6.5 milliseconds for the positioner to settle into place on data track 0. After the 6.5 millisecond timeout, the signal Ready to Read/Write (L) is enabled. This signal illuminates the Ready Lamp on the Control Panel and sends Drive Ready and Read Data to the controller.

The drive is now ready to receive controller write and seek commands.
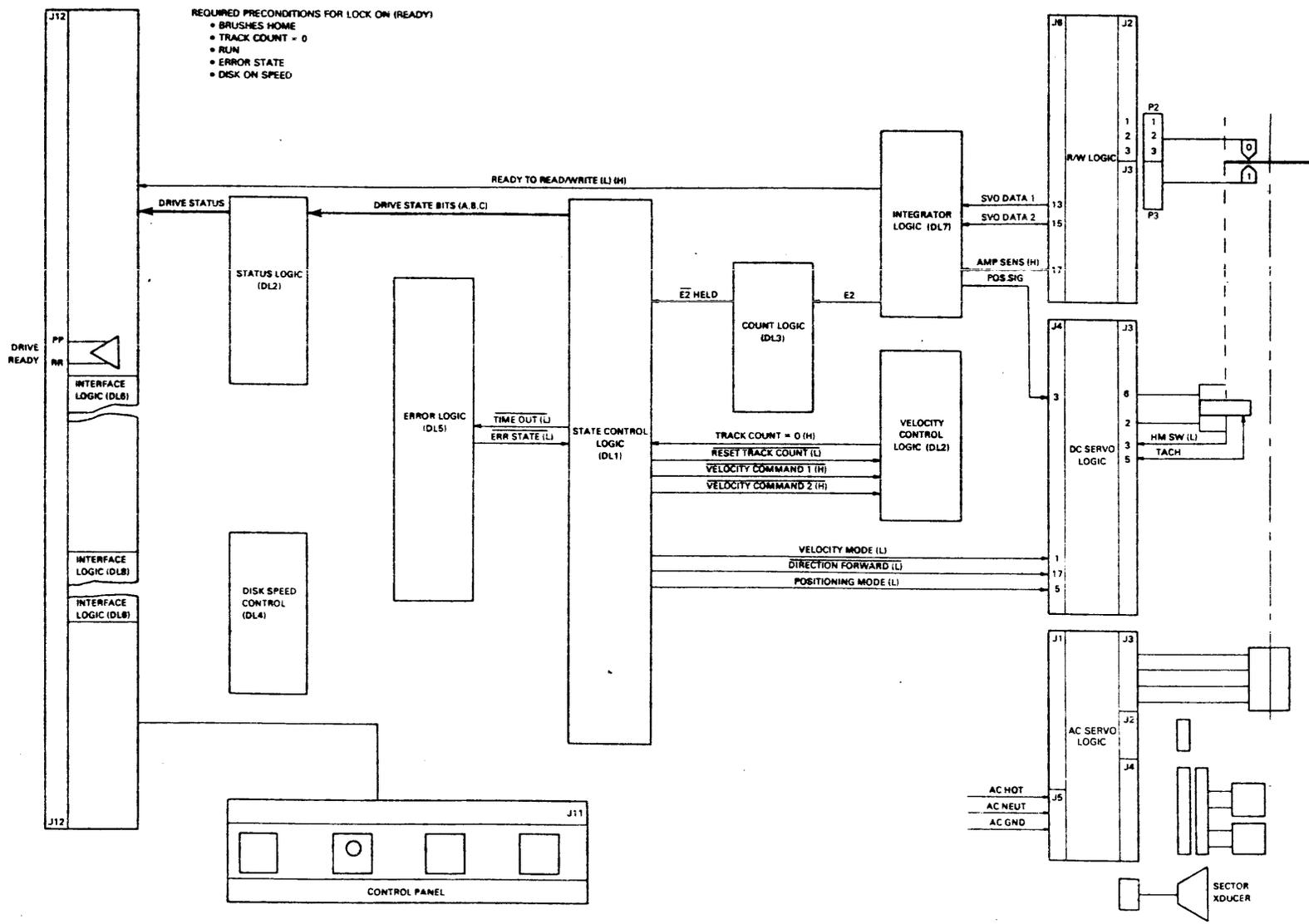
Figure 4-12 Device Startup - Lock on Track 0
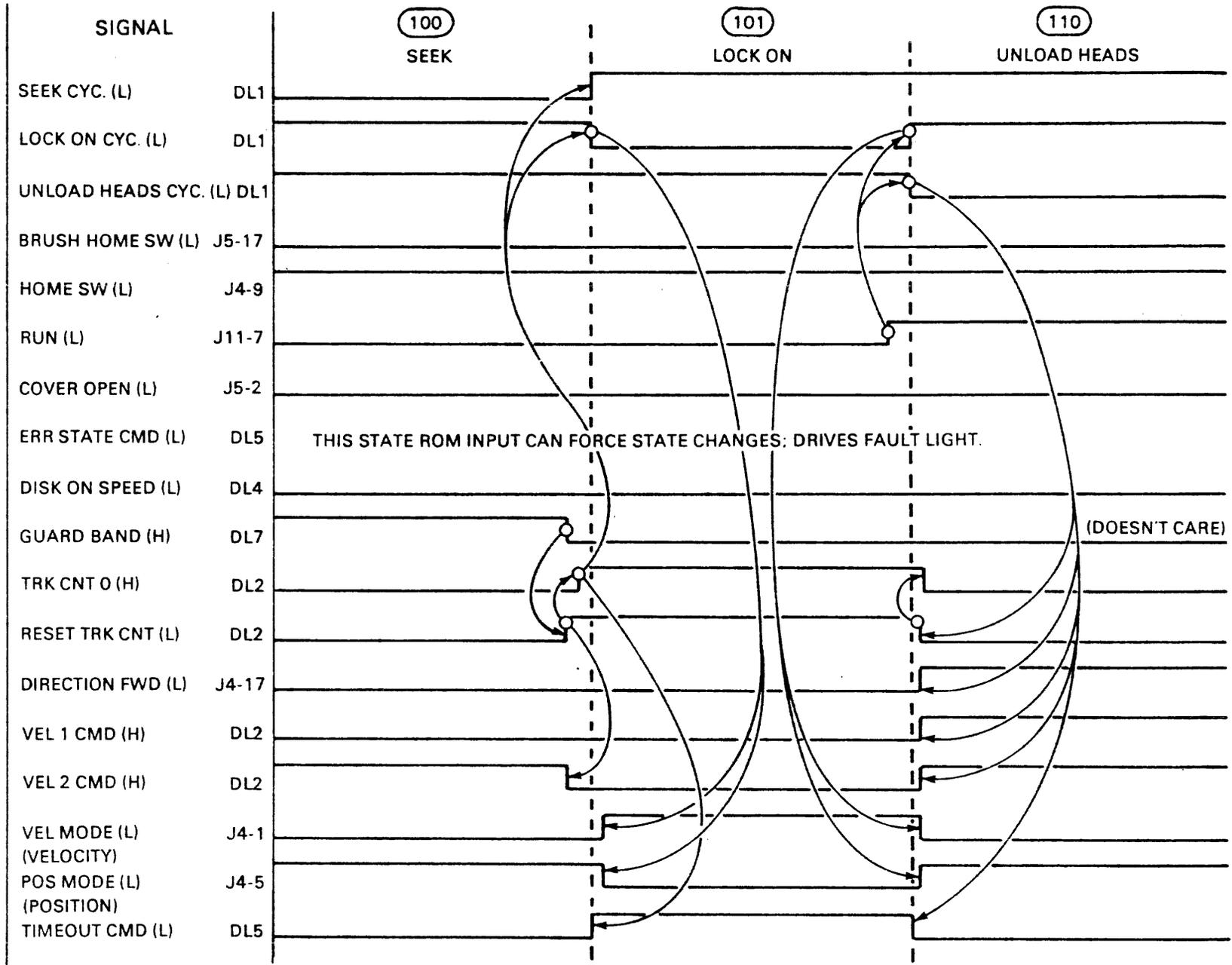
Figure 4-13   Device Startup - Lock on Track 0 Timing

CZ-1032

I/4-20

4.2.8 Unload Heads

Figure 4-14 is a functional diagram showing control signals and data paths which are active during the Unload Heads cycle and the emergency retract function.

Figure 4-15 is a timing diagram which shows the sequence of events which occur during these device operations.

These are the preconditions for the Unload Heads cycle.

- The cover must be closed

- The brushes must be home

- The disk must be on speed

- The positioner is to travel toward the home position.

The Unload Heads cycle is initiated by depressing the RUN switch on a drive that was ready (up to speed, on track, no errors etc.). Depressing the RUN switch immediately forces a state ROM change. The State Control Logic sends a binary velocity command of 11 to the DC Servo Logic which initiates a 15 ips velocity command to drive the positioner towards the home position and tell it is completely off the disk surface. When the positioner reaches the home position, transition into Spin Down cycle occurs.

The error conditions below will cause the positioner to unload the read/write heads under control of the State Control Logic (DL1) as described above.

- The drive senses Write Gate and Sector Pulse simultaneously (Status Word, Bit 10)

- The drive senses Write Current without Write Gate asserted (Status Word, Bit 14), or position threshold during write gate

- No transitions are detected on the Write Data Line but Write Gate is asserted (Status Word, Bit 15).

In the event of an ac power failure, the positioner will immediately unload the read/write heads by discharging a capacitor into the DC Servo Motor control circuitry.

4.2.9 Spin Down

Figure 4-16 is a functional diagram showing control signals and data paths which are enabled during the Spin Down Cycle. Figure 4-17 is a timing diagram which shows the sequence of events which start and end this cycle.
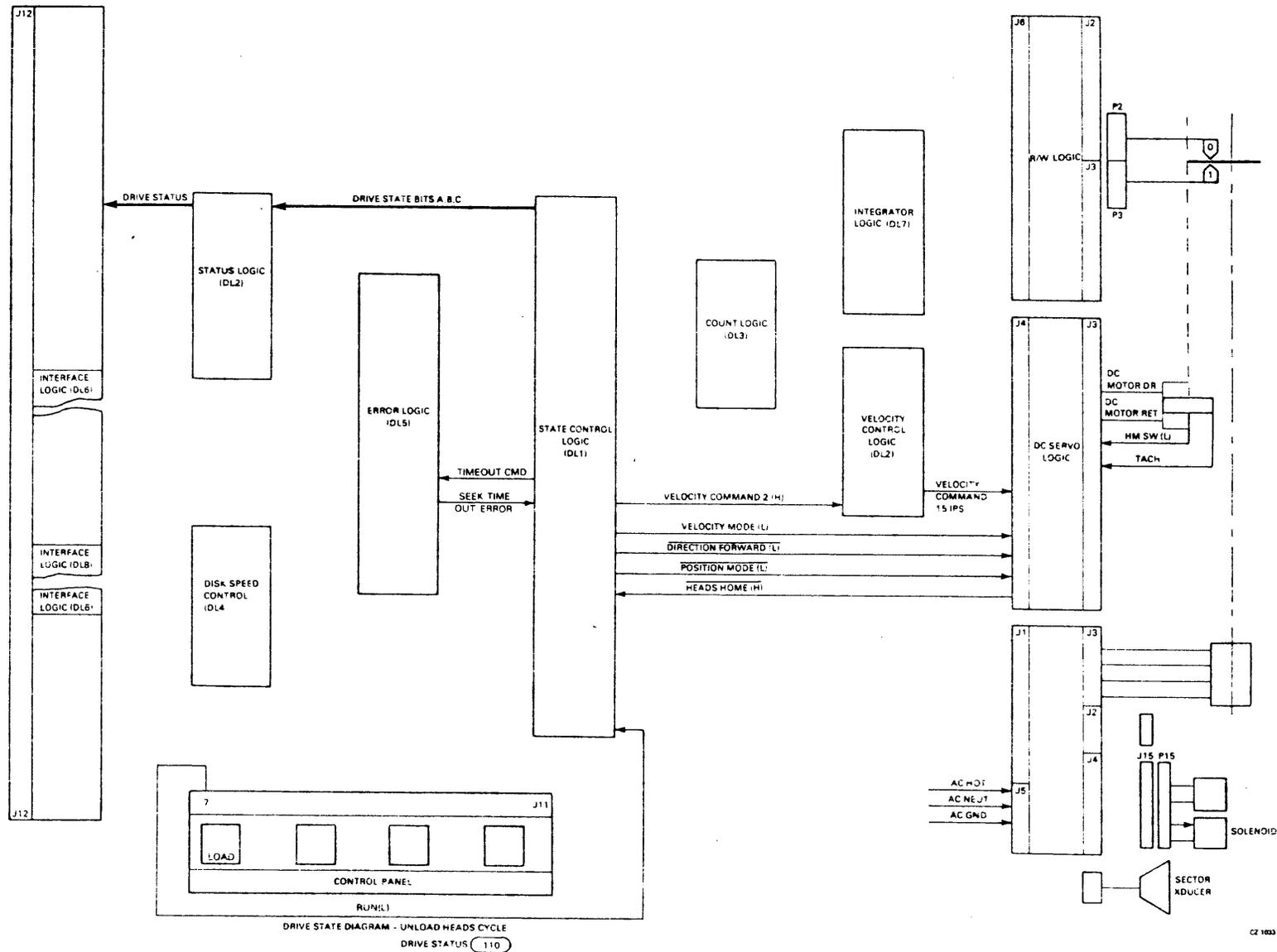
Figure 4-14   Device Startup - Unload Heads
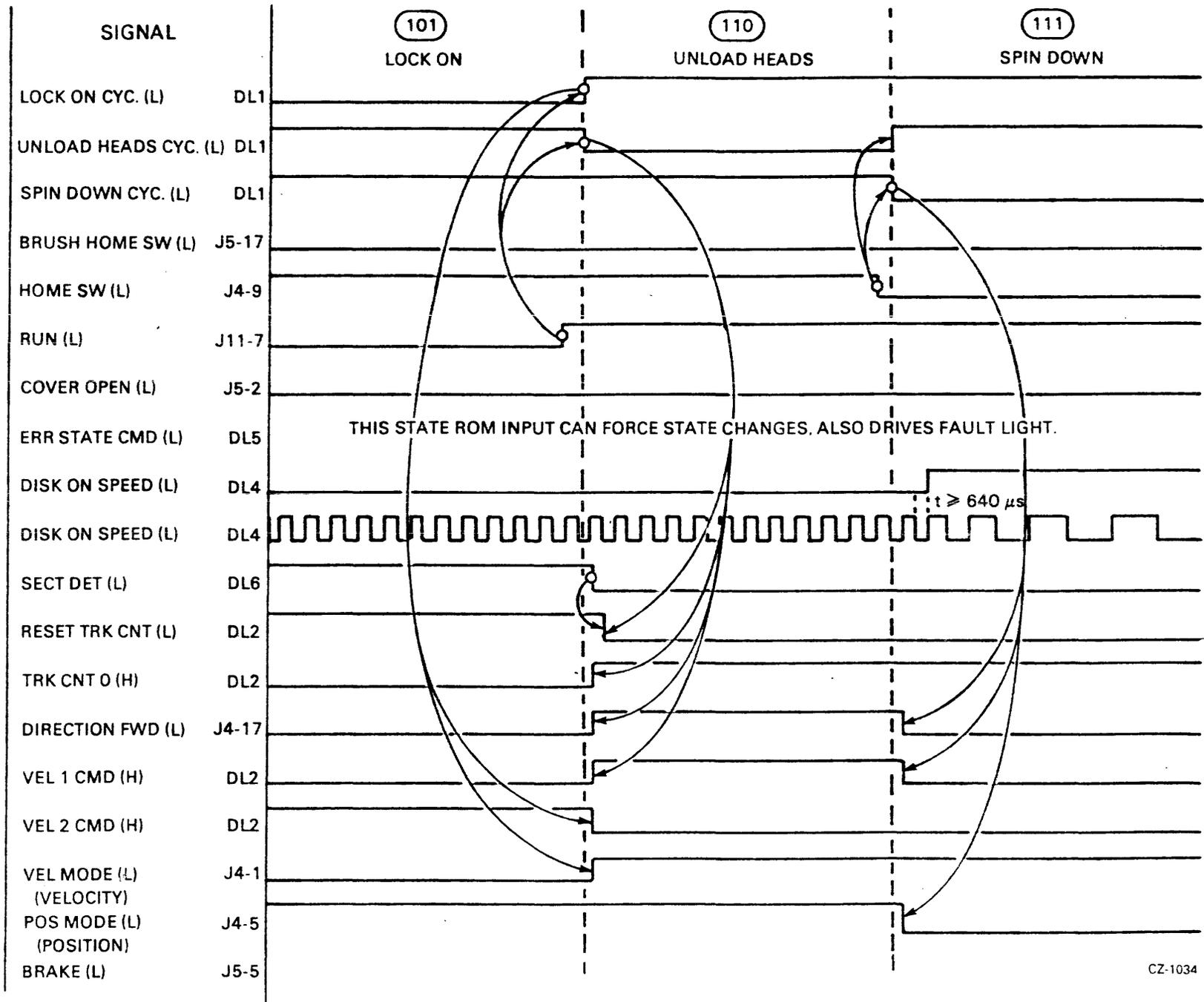
Figure 4-15 Device Startup - Unload Heads Timing

I/4-23
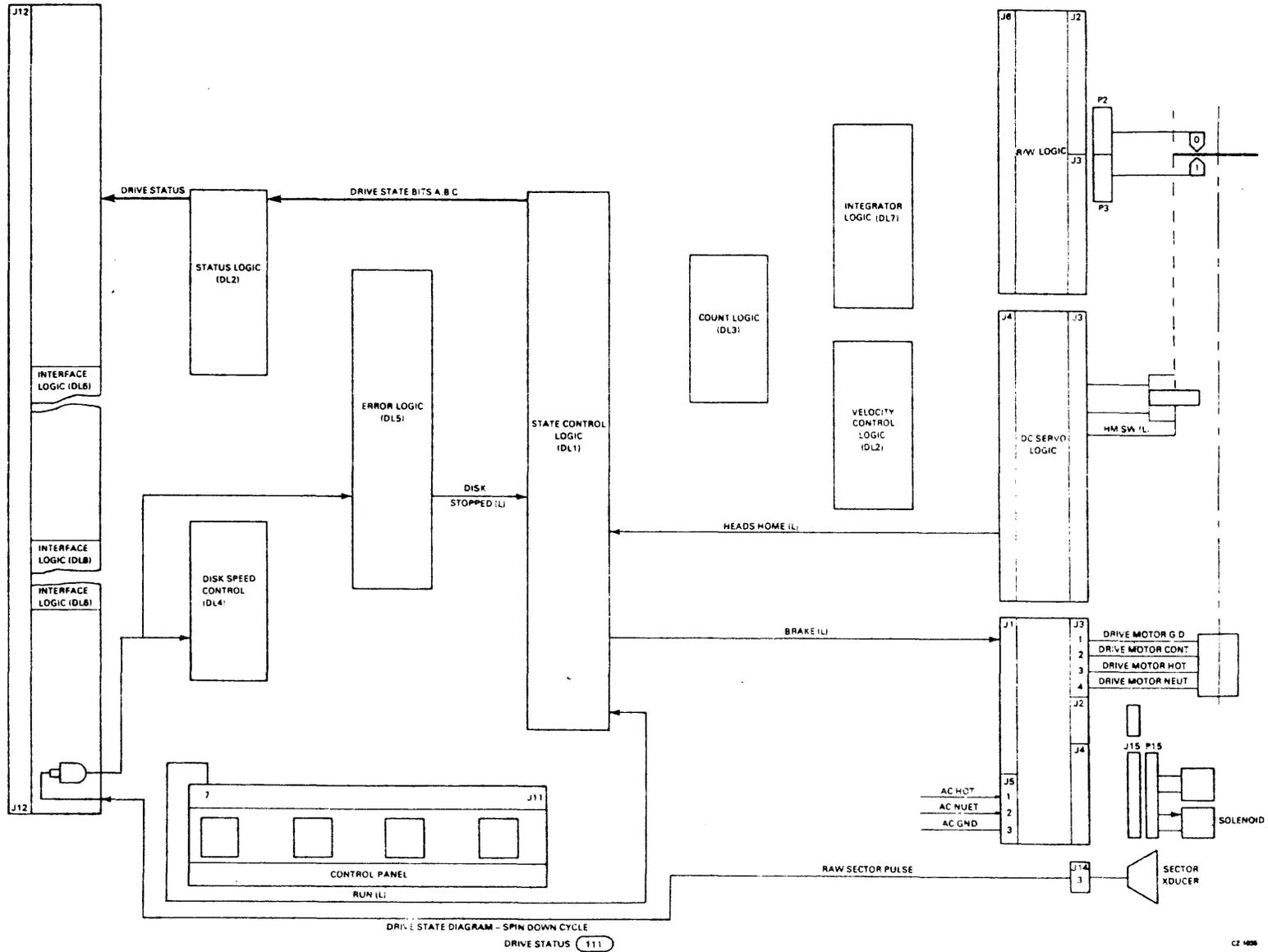
CZ-1034

Figure 4-16 Device Startup - Spin Down

I/4-24
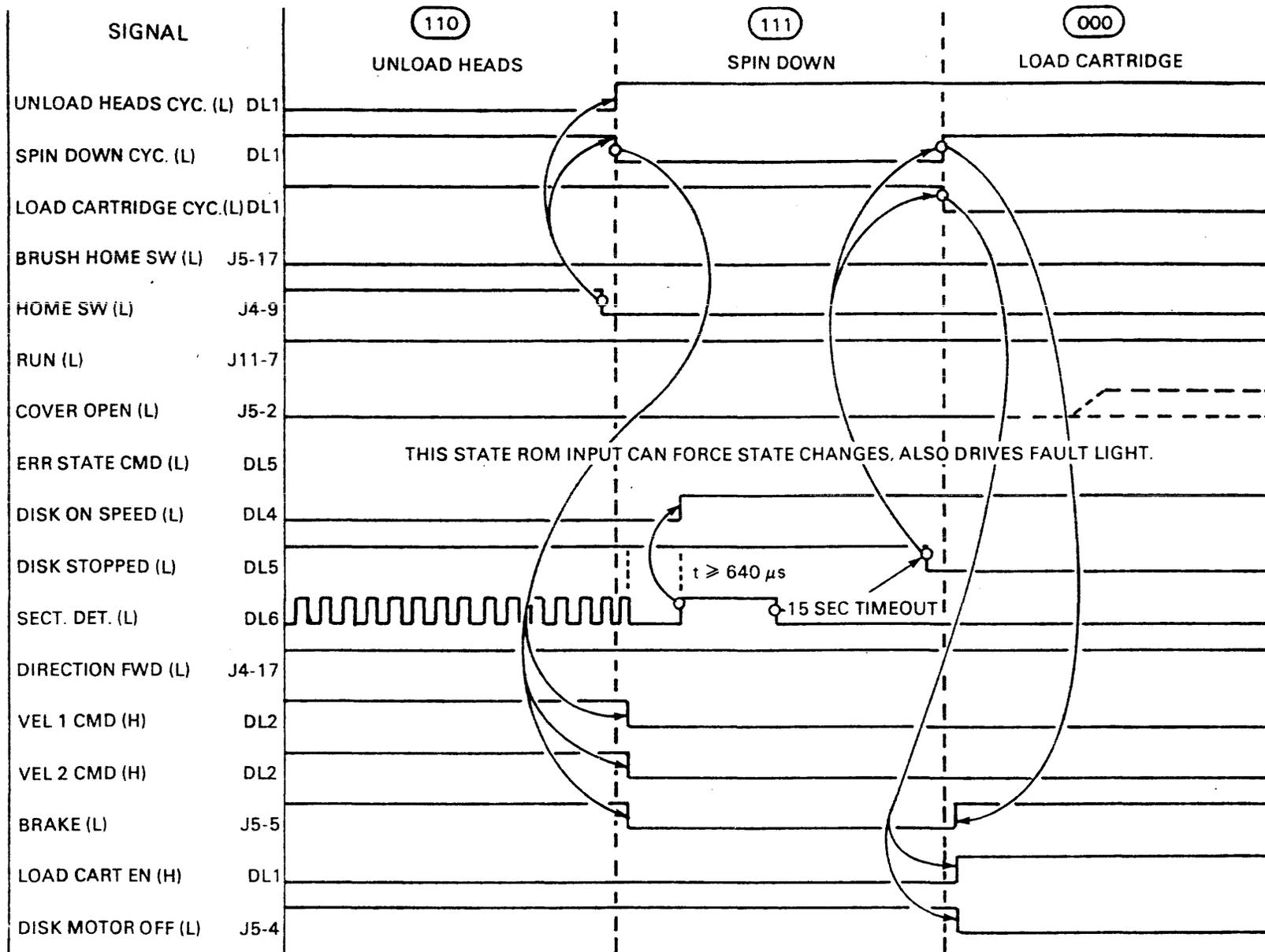
Figure 4-17 Device Startup - Spin Down Timing

I/4-25

CZ-1036

These are the preconditions for the Spin Down cycle.

- Brushes must be home

- Cover must be closed

- Run switch must not be depressed

- Heads must be home.

The transition into Spin Down cycle is made when the positioner reaches home position. The State Control Logic then disables the velocity command to the DC Servo Logic and enables the brake signal to the AC Servo Logic. The speed detection circuits of the Disk Speed Control Logic detect the spindle has stopped and initiates a 15 second timeout. When the timer times out the transition in Load Cartridge state occurs and disables the brake signal.

4.3 EXTERNAL DRIVE FUNCTIONS
To completely understand the functionality of the drive requires a knowledge of the responses to the commands from the controller. The four responses or functions the drive perform are Get Status, Seek, Read Data and Write Data. The three commands NO-OP, Read Data Without Header Check and Write Check do nothing more than read data. The functional differences are performed in the controller.

Functional block diagrams and flow charts are used to show the relationship of control signals and data paths to the device operations. They utilize signal mnemonics and Field Maintenance Print Set References.

4.3.1   Get Status
Figure 4-18 is a functional diagram showing control signals and data paths which are active when the drive receives a Get Status Command from the Controller and returns a Drive Status Word.

The drive receives the command word from the controller as shown in Figure 4-19.

To perform a Get Status both the Marker and Get Status bits must be set in the Drive Command Word. The Reset bit is optional. When set it causes all drive error latches to be reset once, before loading the drive status register. The signal Reset Error Latches (L) from DL2 performs this function. When reset, it does not reset the drive error latches. When the Get Status and Marker bits are decoded the remaining bits 15:04 are ignored.
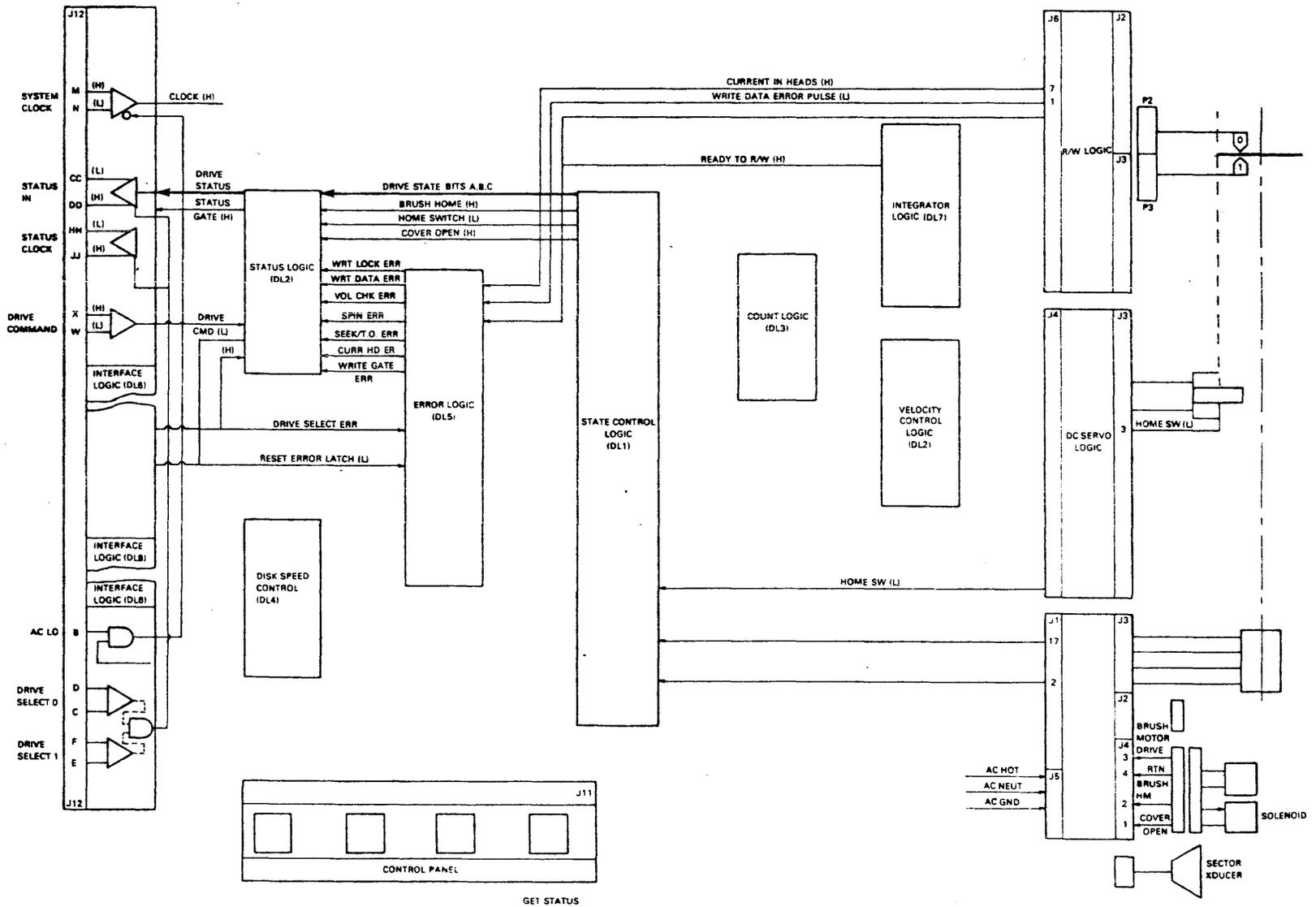
Figure 4-18 Get Status - Functional Block Diagram

```
 15   14   13   12   11   10   9    8    7    6    5    4    3    2    1    0
┌────┬────┬────┬────┬────┬────┬────┬────┬────┬────┬────┬────┬────┬────┬────┬────┐
│ 0  │128 │ 64 │ 32 │ 16 │ 8  │ 4  │ 2  │ 1  │ 0  │ 0  │ HS │RST │ SN │ GS │ M  │
└────┴────┴────┴────┴────┴────┴────┴────┴────┴────┴────┴────┴────┴────┴────┴────┘
```

CYLINDER ADDRESS
DIFFERENCE $(2_8 = 256)$

HEAD SELECT
(0 = UPPER, 1 = LOWER)

RESET

SIGN
(1 = MOVE HEADS TOWARD SPINDLE
0 = MOVE HEADS AWAY FROM SPINDLE)

GET STATUS

MARKER (SYNC)
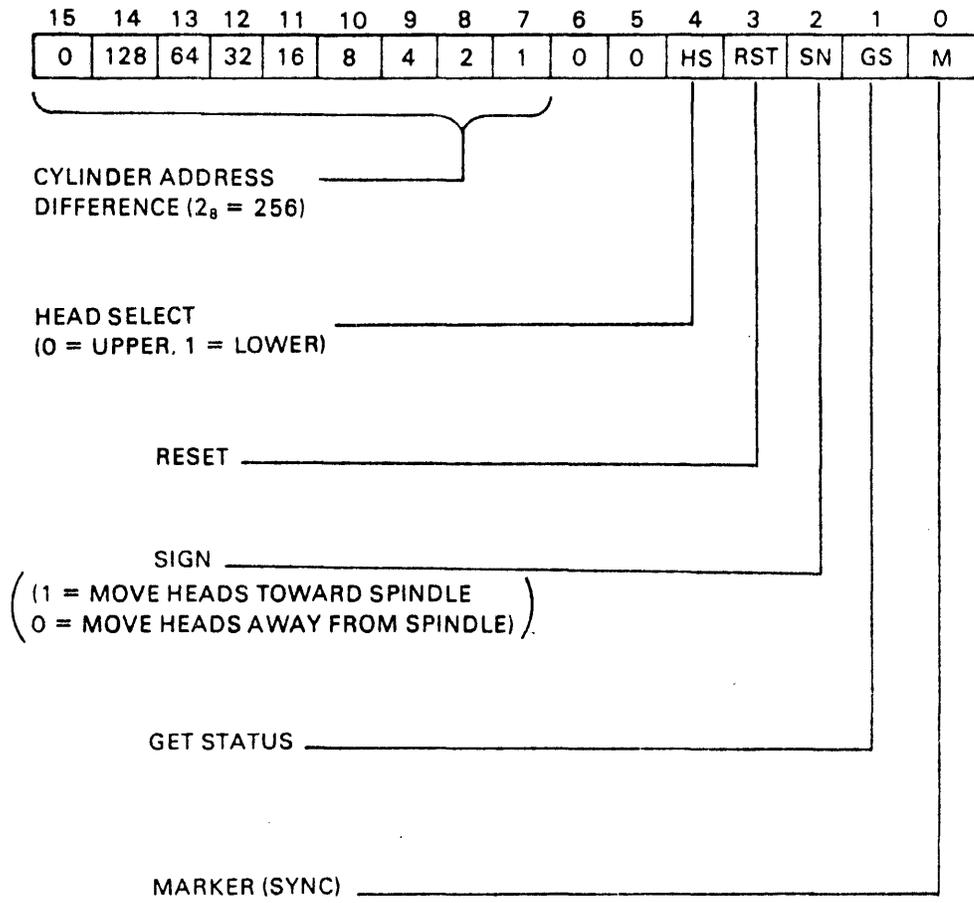
CZ-1038

Figure 4-19   Drive Command Word

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The Command Word and System clock are first received by the Interface Logic (DL6) and then sent to the Status and Control Logic (DL2). The command is then decoded, and since it is a Get Status Command, the status clock gate is enabled. Any drive errors, including status bits A, B, and C from the State Control Logic (DL1), are returned to the Interface Logic where they are transmitted to the controller in sync with the Status Clock.

Note that this function can be performed even if the drive is not ready.

Refer to Paragraph 3.3 for a detailed definition of the Drive Status Word contents.

4.3.2   Seek
Figure 4-20 is a functional diagram showing control signals and data paths which are active when the drive receives a Seek Command from the controller.

Figure 4-21 shows the Drive Command word during a seek as it is received by the Interface Logic (DL6). Note that the absence of the Get Status bit denotes that the command is indeed a seek.

The serial command word is sent to Status and Control Logic (DL2). As soon as the Marker bit is sensed, this logic realizes that it has the entire 16 bit word.

The following preconditions must be met before the seek is initiated.

- The brushes are in the Home position

- The heads are loaded

- The drive is in RUN mode, i.e.,

  - The drive is selected

  - The interface is enabled

  - Power is OK

- No drive errors are being detected

- The disk is up to speed

I/4-30
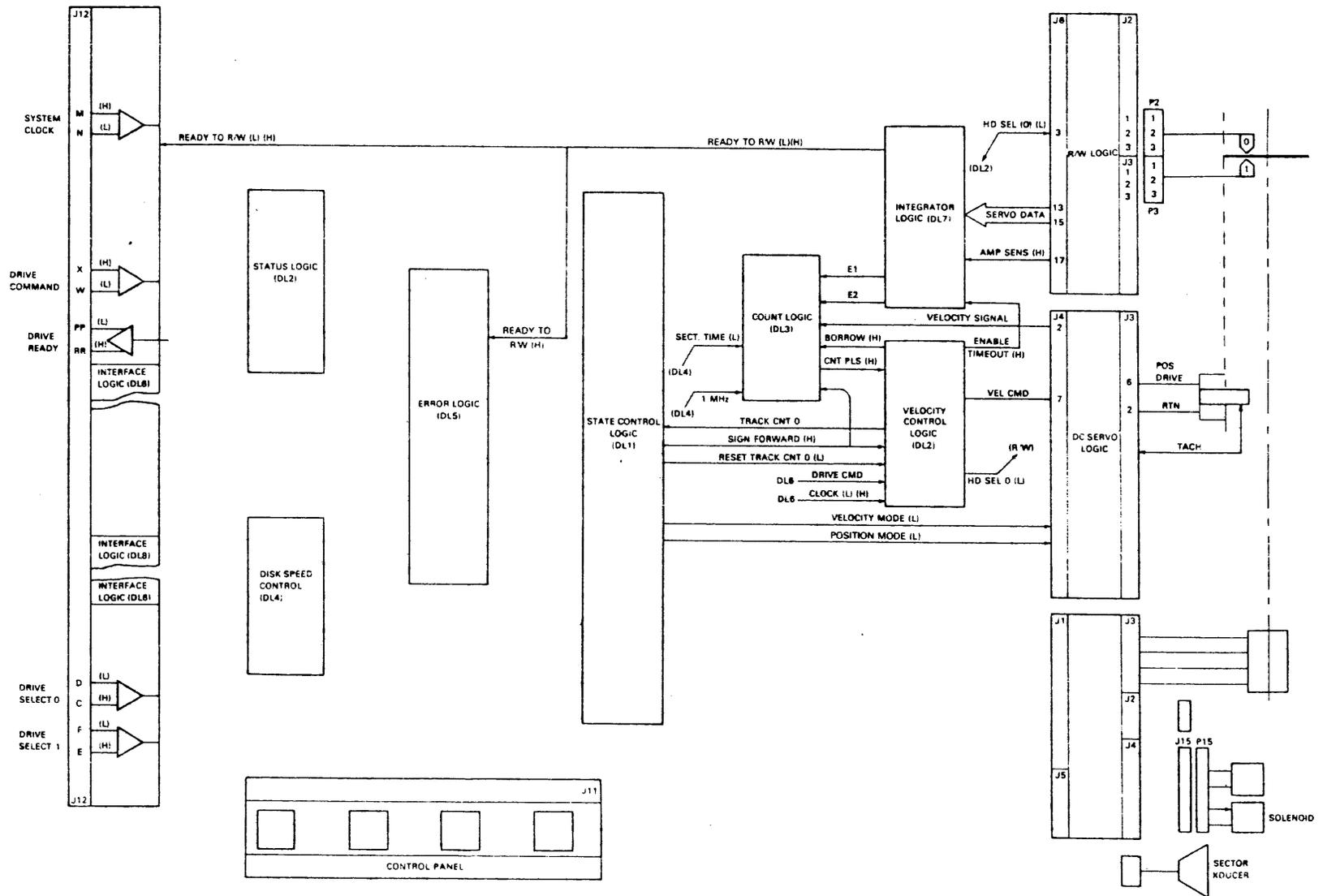
Figure 4-20 Seek Functional Block Diagram
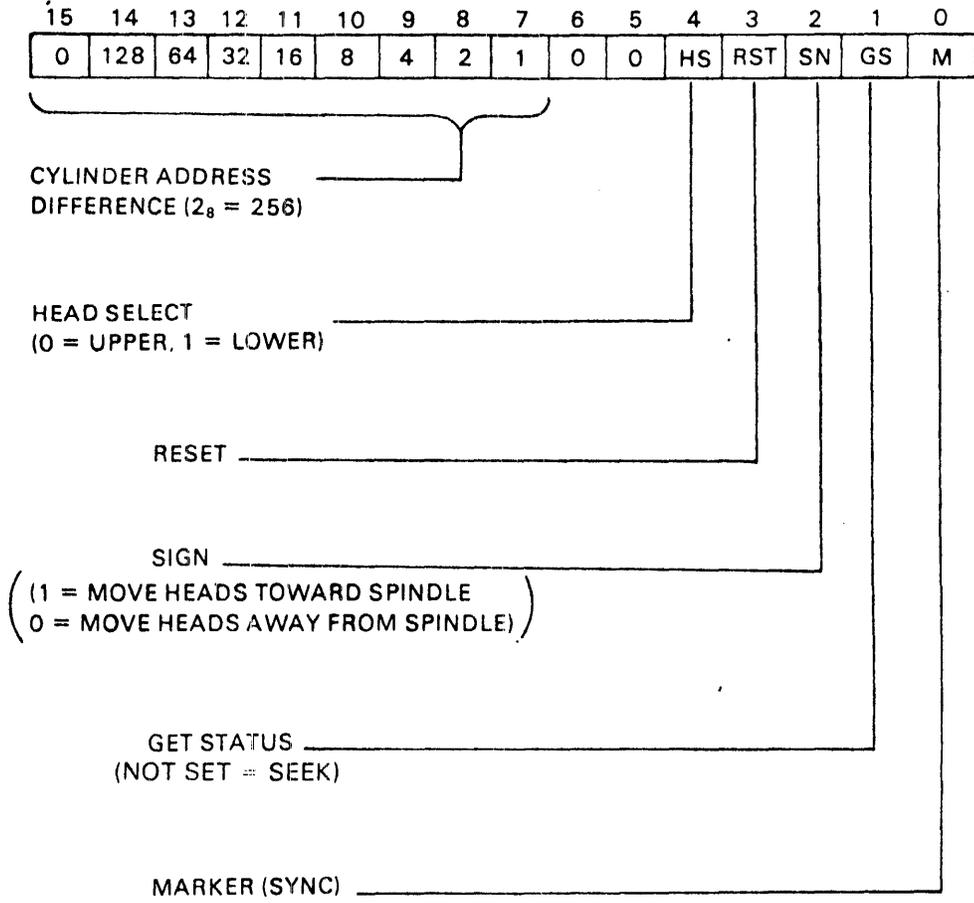
Figure 4-21   Drive Command Word During Seek

I/4-31

As soon as the Marker, Sign (direction) and Track Difference bits have been decoded by the Track Difference Counter (DL2), an initial velocity command is sent to the DC Servo Logic. The State Control Logic is in Seek (or Position) Mode. Servo samples for the Read/Write Logic and velocity feedback from the Positioner Tachometer are used by the Count Logic (DL3) to decrement the Track Difference Counter. As the distance to the target track decreases, the velocity command also decreases. As soon as the track difference counter has counted down to zero, the signal Track Count = 0 (H) is enabled.

The signal Position Mode (L) instructs the DC Servo Logic to accept incremental positioning signals from the Integrator Logic (DL7) and to lock on the negative or positive slope (depending upon the direction of the seek) of the positioner signal.

At the same time, a Ready to Read/Write timeout is set which allows 6.5 milliseconds for the positioner to settle into place on the designated track. After the 6.5 millisecond timeout, the signal Ready to Read/Write (L) is enabled. This signal illuminates the READY lamp on the Control Panel and sends Drive Ready and Read Data to the controller.

4.3.3 Read Data

Figure 4-22 is a functional diagram showing control signals and data paths which are active during Read Data.

The preconditions for reading valid data arelisted below.

- The drive has been selected by the controller

- Heads are locked on a data track (either track 0 immediately following a Guard Band Seek, or the track number specified) during a previous seek

- No drive errors are being sensed

- The spindle is on speed

- The 6.5 millisecond Ready to Read/Write timeout cycle has been completed, which occurs:

  - After the last bit of a cylinder address difference word has been shifted to the selected drive

  - When a new read/write head has been selected, even though the difference address for a seek is zero

  - When a seek difference address is zero and no change in head selection has occurred.

When these preconditions have been met, Modified Frequency
Modulation (MFM) encoded read data (see Paragraph 2.2.3) is
transferred from the drive to the controller via the Read Data
interface line. Note that whenever a drive is selected there is
some form of information on this line. Only when the above
conditions are met will legitimate data be transferred to the
controller.

The Sector Pulse is transmitted to the controller by the drive to
signify the beginning of a sector. The beginning of the sector
pulse corresponds with the sensing of the sector slot on the
cartridge armature by the sector transducer. The end of sector
pulse signifies the end of servo data.

After detection of the servo information and the header preamble,
read data goes to the controller.

In order to read headers, the controller VFO loop is phase-locked
with read data after the end of the drive sector pulse.
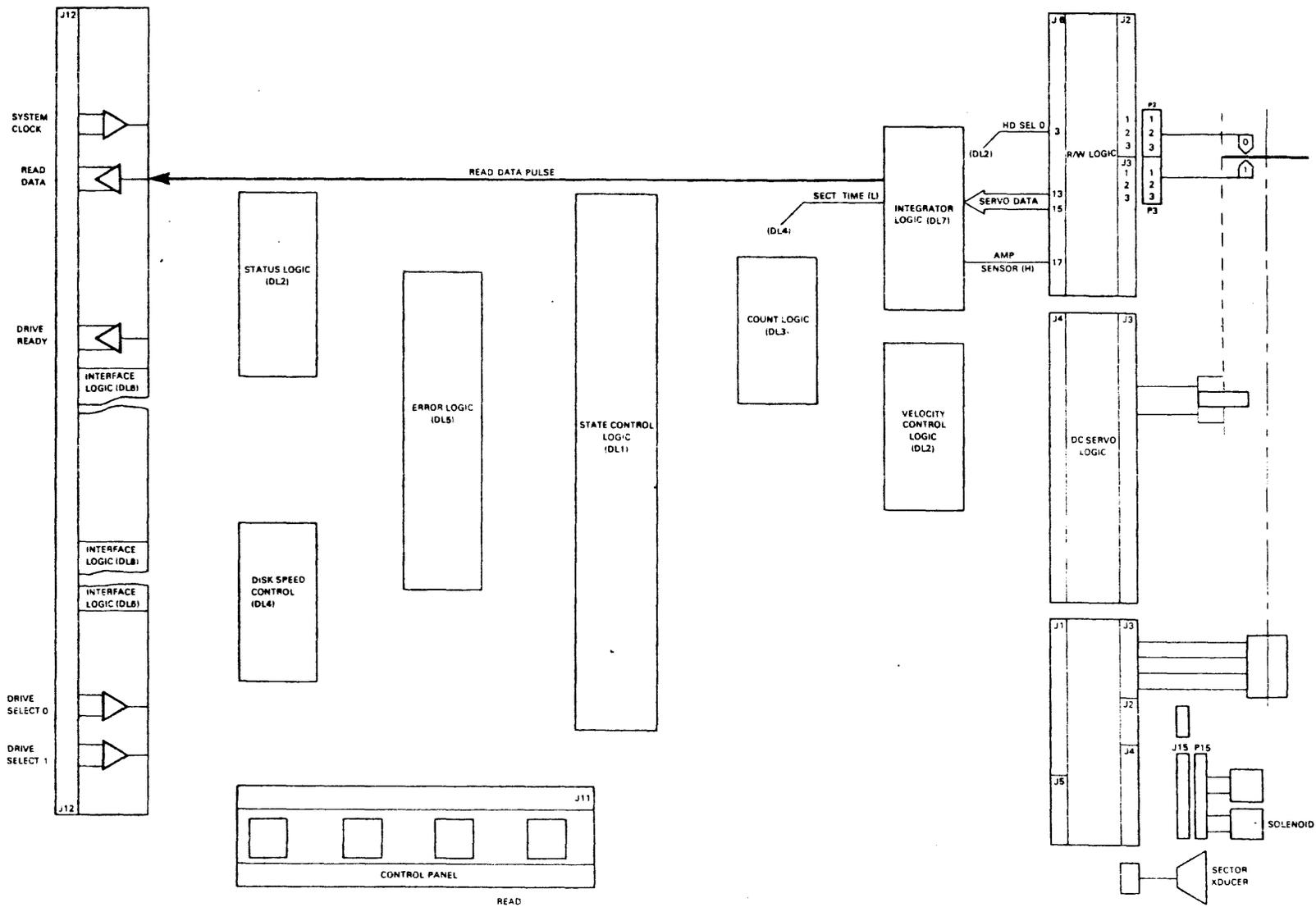
Figure 4-22 Read Data - Functional Block Diagram

4.3.4   Write Data
Figure 4-23 is a functional diagram showing control signals and data paths which are active during Write Data.

These are the preconditions required for Write Data.

- The drive has been selected by the controller

- Heads are locked on to a data track (either track 0 immediately following a Guard Band Seek, or the track number specified) during a previous Seek

- No drive errors are being sensed

- The 6.5 millisecond Read to Read/Write timeout cycle has been completed, which occurs

    - After the last bit of a cylinder address difference word has been shifted to the selected drive

    - When a new Read/Write head has been selected even though the difference address for a Seek is zero

    - When a seek difference address is zero and no change in head selection has occurred

- The end of the drive Sector Pulse has been detected

- A Header Compare has been detected by the controller

- The Header CRC checks

When these conditions have been met, and the Write Gate line has been asserted, Modified Frequency Modulation (MFM) encoded Write Data (see Paragraph 2.2.3) is transferred from the controller to the drive via the Write Data interface line.

The write data stream contains the three data preamble words (47 bits of zeros and the Marker Bit), 128 data words, the data CRC word, and the data postamble word (16 bits of zeros).

The Write Gate enables write circuits in the drive. It must be asserted at the start of the Data Preamble (PR2). The actual data to be written will occur 16 bit periods after the Header CRC; i.e., after the Header Postamble.

The control unit transmits write pulses which are compensated to reduce peak-shift introduced by the recording process (refer to Paragraph 2.2.3 on MFM Encoding and Precompensation).

WRITE DATA PULSE (L)

WRITE GATE (L) (H)

WRITE DATA

WRITE GATE

SYSTEM CLOCK

DRIVE READY

DRIVE SECTOR PULSE

DRIVE SELECT 0

DRIVE SELECT 1

INTERFACE LOGIC (DL6)

INTERFACE LOGIC (DL8)

INTERFACE LOGIC (DL6)

STATUS LOGIC (DL2)

DISK SPEED CONTROL (DL4)

ERROR LOGIC (DL5)

STATE CONTROL LOGIC (DL1)

COUNT LOGIC (DL3)

INTEGRATOR LOGIC (DL7)

VELOCITY CONTROL LOGIC (DL2)

R/W LOGIC

DC SERVO LOGIC

SOLENOID

CONTROL PANEL

RAW SECTOR PULSE

SECTOR XDUCER

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Figure 4-23 Write Data - Functional Block Diagram

5.1 DRIVE LOGIC MODULE THEORY OF OPERATION
This section describes in detail the operation of the Drive Logic Module.

For simplicity, the Drive Module Logic has been broken down into the functional areas listed below.

- State Control Logic (Sheet DL1 of the Field Maintenance Print Set)

- Velocity Command and Status Data Control Logic (DL2)

- Count Logic (DL3)

- Disk Speed Control Logic (DL4)

- Error Logic (DL5)

- Interface Logic (DL6, DL8)

- Integrator Logic (DL7).

5.1.1 State Control Logic (DL1)
The State Control Logic (shown on Sheet DL1 of the Field Maintenance Print Set) is the portion of the Drive Logic Module which both monitors and controls drive Start Up functions such as Spinup, Brush Cycle, Load Heads, etc. It comprises two Read-Only Memories (ROMs), the State ROM and the Seek Control ROM, a State Counter, the Brush Cycle Latch, and the control panel LOAD lamp driver.

5.1.1.1 State ROM - The State ROM is a 256 X 4 Bit Programmable Read-Only Memory. Its purpose is to generate a four bit binary encoded (BCD) word which denotes drive status and provides control for other decision-making logic within the drive. Its outputs are listed below.

- Status Bit A

- Status Bit B

- Status Bit C

- Time Out Command

The status bits A, B, and C are sent to the Status Control Logic (DL2) where they are used to make up the Drive Status Word resulting from a controller Get Status Command. They are also used as inputs to the Seek Control ROM and the State ROM Decoder.

The Time Out Command signal is sent to the Error Logic (DL5) where it is used to start the Seek Error Timer for moving positioner functions (i.e., Load Heads, Seek, and Unload Heads).

The address inputs to the State ROM are derived from eight signals which sense drive conditions at any given time. These address bits comprise the following:

● Brush Home Switch

● Heads Home Gate

● Run

● Error State Command

● Disk On Speed

● Disk Stopped

● Track Count = 0

● Brush Cycle Latch.

The State Control ROM is preprogrammed (burned-in) at the factory so that specific address combinations yield specific output words. Figure 5-1 shows the addressing scheme for the State Control ROM. The value "1" denotes a "true" input or output. The value "0" denotes a "false" input or output. The value "X" denotes a "don't care" situation.

5.1.1.2   State ROM Decoder - The State ROM Decoder is an SN7442 BCD-to-Decimal Decoder. It decodes the State ROM output (status bits A, B, and C) and provides an output corresponding to the drive state. Figure 5-2 shows the decoding scheme.

5.1.1.3   Seek Control ROM - The Seek Control ROM is a 256 X 4 Bit Programmable Read-Only Memory. Its purpose is to provide the Velocity Command Control Logic (DL2) with information pertaining to positioner location and drive status. Its outputs are listed below.

● Direction Forward

● Velocity Commands 1 and 2

● Reset Track Count.

Veloctiy Commands 1 and 2 are sent to the Velocity Command and Control Logic (DL2) where they used address bits for the Velocity ROM. These commands apply only when the Positioner is in Velocity Mode. Figure 5-3 shows the decoding for Velocity Commands 1 and 2.

	STATE ROM INPUTS								OUTPUT				

BRUSH HOME (H)	HEADS HOME GATE (H)	RUN (H)	ERROR STATE COMD (L)	DISK ON SPEED (L)	DISK STOPPED (L)	TRACK COUNT 0 (H)	BRUSH CYCLE LATCH (H)	TIME OUT COMD (L)	STATUS BIT C	STATUS BIT B	STATUS BIT A	
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Y_4	Y_3	Y_2	Y_1	FUNCTION
1	1	0	X	X	0	X	X	1	0	0	0	LOAD CARTRIDGE
1	1	1	1	1	X	X	X	1	0	0	1	SPIN UP
1	1	1	1	0	1	X	1	1	0	1	0	BRUSH CYCLE
1	1	1	1	0	1	X	0	0	0	1	1	LOAD HEADS
1	0	1	1	0	1	0	X	0	1	0	0	SEEK
1	0	1	1	0	1	1	X	1	1	0	1	LOCK ON
1	0	0	X	X	X	X	X	0	1	1	0	UNLOAD
1	1	0	X	X	1	X	X	1	1	1	1	SPIN DOWN

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Figure 5-1   State Control ROM Addressing

STATUS A	STATUS B	STATUS C		LOAD CART	SPIN UP	BRUSH	LOAD HDS	SEEK	LOCK ON	UNLOAD	SPIN DOWN
0	0	0		0	1	1	1	1	1	1	1
1	0	0		1	0	1	1	1	1	1	1
0	1	0		1	1	0	1	1	1	1	1
1	1	0		1	1	1	0	1	1	1	1
0	0	1		1	1	1	1	0	1	1	1
1	0	1		1	1	1	1	1	0	1	1
0	1	1		1	1	1	1	1	1	0	1
1	1	1		1	1	1	1	1	1	1	0

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Figure 5-2 State ROM Command Decoding Scheme

VELOCITY CMD 1	VELOCITY CMD 2		VELOCITY	MODE
0	0		0	OFF
1	0		3 I.P.S.	GUARD BAND
0	1		6 I.P.S.	HEAD LOAD
1	1		15 I.P.S.	HEAD UNLOAD

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Figure 5-3   Velocity Commands 1 & 2 Decoding Scheme

The address input to the Seek Control ROM are derived from eight signals which sense drive and positioner conditions at any given time. These address bits consists of the signals below.

- Status Bits A, B, and C

- Guard Band

- E1 Held (Previous E1 Servo Data Sample)

- E2 Held (Previous E2 Servo Data Sample)

- Sign Forward (Direction)

- Seek Timeout Error (Disables a Seek)

The Seek Control ROM is preprogrammed at the factory so that specific address combinations yield specific output words. Figure 5-4 shows the addressing scheme for the Seek Control ROM. The value "1" denotes a "true" input or output. The value "0" denotes a "false" input or output. The value "X" denotes a "don't care" situation.

5.1.1.4   Brush Cycle Latch - The Brush Cycle Latch monitors and controls the Brush Drive Assembly. It also provides an address input to the State Control ROM.

Input:

Set   = Power On Reset (L) or

           Load Cartridge State (L) from

           the State Control ROM

Reset   = Brush Home Switch (L).

Output:

Brush Cycle Latch (H).

When the Brush Cycle Latch is set, the State Control ROM starts the Brush Cycle. This produces the Signal Brush Cycle (L) which energizes the brush drive motor. As the brushes move out over the disk, the Signal Brush Home Switch (L) goes high, resetting the latch. The State Control ROM remains in the Brush Cycle State until the brushes, driven by a cam, return to their home position. The combination of the signals Brush Home Switch (L) and Brush Cycle Latch reset causes the state ROM to advance to the Load Heads State.

	SEEK CONTROL ROM INPUTS								OUTPUTS				
	SEEK TIME OUT ERROR (H)	STATUS BIT C (L)	STATUS BIT B (L)	STATUS BIT A (L)	GUARD BAND (H)	E1 HELD	SIGN FWD (H)	E2 HELD	RESET TRACK COUNT (L)	VELOCITY CMD 2 (H)	VELOCITY CMD 1 (H)	DIRECTION FWD (H)	
	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Y_4	Y_3	Y_2	Y_1	FUNCTION
									0	0	0	0	ILLEGAL
	1	X	X	X	X	X	X	X	0	0	0	1	SERVO OFF
	0	1	0	0	1	0	X	X	0	0	1	0	INNER GUARD BAND
	0	1	0	0	1	1	X	X	0	0	1	1	OUTER GUARD BAND
	0	0	1	1	X	X	X	X	0	1	0	0	LOAD HEADS
	0	1	1	0	X	X	X	X	0	1	1	1	UNLOAD HEADS
	0	1	0	0	0	X	1	X	1	0	0	0	SEEK FWD
	0	1	0	1	0	X	X	1					LOCK ON NEG. SLOPE
	0	1	0	0	0	X	0	X	1	0	0	1	SEEK REV
	0	1	0	1	0	X	X	0					LOCK ON POS. SLOPE

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Figure 5-4   Seek Control ROM Addressing

5.1.2 Velocity Command and Status Data Control Logic (DL2)
The Velocity Command and Status Data Control Logic is the portion
of the Drive Logic Module which receives the Drive Command Word
from the controller, decodes the Track Difference Count and
Direction for seek purposes, and develops the necessary velocity
command to drive the positioner.

If the Command Word is decoded as a Get Status Command, this logic
collects drive status and error information to make up the Drive
Status Word, which is transmitted to the controller in sync with
the Status Clock.

This logic comprises the circuitry listed below.

- Device Command/Status Register, Shift/Load, and Clear
  Gates

- Marker Flip-Flop and Latch

- Track Difference Counter and Load Latch

- Head Select/Sign Bit Holding Register

- Load Registers Gate

- Get Status Latch

- Reset Error Latches Gate

- Track Count = 0 Gate

- Enable Timeout Gate

- Velocity ROM

5.1.2.1   Device Command/Status Register — The Device
Command/Status Register is a sixteen bit register that may be
operated in two modes, shift or load. This register operates in
load mode only after it has decoded a Get Status Command from the
controller. Otherwise, it operates in Shift Mode, allowing the
drive command to ripple through under control of the system clock
and the Marker flip-flop.

Normally, the Marker bit is not followed by a Get Status bit. If
there is no Get Status bit, the Command Register is cleared on the
third transition of the system clock. This is done to ensure that
other pulses in the Drive Command are not mistaken as marker bits
as the command is shifted through.

Figure 5-5 shows Drive Command and Status Control Timing.

DRIVE COMMAND (GET STATUS)

DRIVE COMMAND (GET STATUS)

CLOCK (H)
DL2 E62-4

DRIVE COMMAND (H)
DL2 E30-2

MARKER FLOP (H)
DL2 E48-5

GET STATUS LATCH (H)
DL2 E29-13

MARKER LATCH (L)
DL2 E18-4

CLEAR FLIP-FLOP (L)
DL2 E20-9

CLEAR LATCH (L)
DL2 E24-6

SHIFT/LOAD (L)
DL2 E24-8

GET STATUS (H)
DL2 E27-12

CLOCK (L)
DL2 E18-9

HEAD SELECT/SIGN BITS AT HOLDING REG
DL2 E38-6,7

LOAD HOLDING REG. (H)
DL2 E33-10

HOLDING REG. OUT (HD SEL/SIGN BITS)
DL2 E38-13,12

BORROW (L)
DL2 E18-10

TRACK DIFFENCE CNTR LOAD LATCH (L)
DL2 E18-9

GET STATUS
BIT

GET STATUS (L)
DL2 E27-11

STATUS CLOCK GATE (H)
DL2 E26-11

STATUS CLOCK (H)
DL6 E50-4

STATUS DATA INPUT
TI CMD REG (H)

STATUS DATA (H)
DL2 E27-12

STATUS IN (TO CPU) (H)
DL6 E54-4

BIT 0   BIT 1   BIT 2

MARKER LATCH. COMMAND REGISTER CLEAR. HOLDING
REGISTER AND TRACK DIFFERENCE COUNTER LOAD

LEGEND   —O— ENABLE
          —☐— INHIBIT

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Figure 5-5   Drive Command and Status Control Timing

5.1.2.2   Marker Flip-Flop – The Marker flip-flop is used to detect the Marker bit; the first bit in a device command word. When set, it signifies that the entire 16 bit command is present in the Drive Command/Status Register.

Input:

       Data   = Serial Command Word from Drive Command/Status
               Register

       Clock   = System Clock (H), Load Track Difference Counter.

Output:

       Q   = Marker Bit (H) to Marker Latch.

5.1.2.3   Marker Latch – When set, the Marker Latch signifies that the Marker flip-flop has sensed the marker bit and that the device command word is available for decoding.

Input:
       Set   = Marker Flip-Flop (H), Clock (negative-going
               edge)

       Reset   = Next Clock Transition.

Output:

   • If Get Status, set Clear Flip-Flop, load holding registers

   • If Get Status, set Shift/Load Gate.

5.1.2.4   Clear Latch – The purpose of the Clear Latch is to clear all bits in the Device Command/Status register so that they will not appear as Marker Bits.

Input:

       Data   = Marker Latch (L)

       Clock   = 3rd half of System Clock Cycle going low.

Output:

       Q   = Clear (L).

5.1.2.5   Load Registers Gate - During a normal command (i.e., Get Status), the Load Registers Gate allows the Head Select/Sign Bit Holding register and the Track Difference Counter to be loaded with data from the Device Command/Status register. Data is loaded when the Marker Latch is set.

Input:

     Get Status, Marker Latch (L).

Output:

     Load Registers (H).

5.1.2.6   Shift/Load Gate - During a normal command (i.e., Get Status), the output from the Shift/Load Gate is high, which allows the Drive Command Word to shift through the Device Command/Status register.

Input:

     Get Status (L), Q output of Command Register, Marker Latch (L).

Output:

     Shift/Load (L) to Command register and Get Status Latch.

5.1.2.7   Get Status Latch - The Get Status latch is set when a Get Status Command is detected and the Shift/Load Gate requests Load. It also enables the Status Clock Gate.

Input:

     Set   = Shift/Load (L)

     Reset   = Next Drive Command.

Output:

     Enable Status Clock Gate (H).

5.1.2.8   Status Clock Gate - The output of the Status Clock Gate is sent to the Interface Logic (DL6) to enable the Status Clock for transmission of the Drive Status Word to the controller.

5.1.2.9   Track Difference Counter - During a device command (e.g., Get Status), the Track Difference Counter is loaded with the Track Difference value designated by the controller.

Outputs from the counter are used as address input to the Velocity ROM which determines the positioner velocity.

The counter is decremented one count (or track) at a time by the Count Logic (DL3).

Load Enable is provided by the Track Difference Counter Load Latch.

5.1.2.10   Track Difference Counter Load Latch - This latch allows the Track Difference Counter to be loaded with the difference address derived from the Device Command Word.

Loading of the Track Difference Counter is disabled if its contents are not equal to zero. This prevents loading new seek information into the Counter while a seek is being performed.

Input:

        Set   = Load Register Enable (H), System Clock going
                  high

        Reset   = Borrow (L).

Output:

        Load Track Difference Counter (L), Enable Time Out Gate

        Enable Device Command/Status Register Clock.

5.1.2.11   Head Select/Sign Bit Holding Register - This register holds Head Select and Positioner direction data from the Device Command Word. Loading is enabled by the Load Register Gate at the same time that the Track Difference Counter Load Latch is set. It is cleared by Power On Reset or when the drive is in the load cartridge state.

Input:

        Data   = Head Ø (L)

                  Sign Forward (H)

        Clock   = Load Registers (H).

Output:

        Data   = Head Select Ø (L)

                  Sign Forward (H).

5.1.2.12   Track Count = Ø Gate - The output from this gate [Track Count = Ø (H)] indicates that the Track Difference Counter has been decremented to zero and that the positioner should be on the track specified by a previous seek. This prevents the Count Logic from attempting to decrement the Difference Counter any further.

5.1.2.13 Reset Error Latches Gate – When the Reset bit is sensed during a Get Status decode of the Drive Command Word or a Power On Reset is received from the controller, the output from this gate is sent to the Interface Logic (DL8) and the Error Logic (DL5) to reset Drive Error Latches.

Inputs:

>   Reset Bit (H) or Marker (L) and Power On Rest (L) (Drive Command Word).

Output:
>   Reset Error Latches (L).

5.1.2.14   Velocity ROM – The Velocity ROM is a 256 X 4 Bit Programmable Read-Only Memory. Its purpose is to generate binary encoded current levels to drive the positioner servo.   The combination of ROM output (current levels) is a square root function of the track difference value presented by the track difference counter as address bits A through F and ME1 and ME2. In addition, the binary equivalent of the velocity commands for Load Heads, Unload, Guardband and Off as generated by the State ROM (DL1) are entered as address bits G and H.

Figure 5-6 is a simplified logic diagram showing the generation of the servo velocity command. Table 5-1 shows the ROM addressing scheme and resulting binary encoded outputs.

Any ROM output, when high, allows current to flow through diode D5.   Combinatorial selection of the ROM outputs is derived from track difference inputs.   The binary encoded outputs are then added, determining total drive current and the corresponding velocity command.   The series diodes reduce leakage current, allowing accurate low velocity command levels.   Current output from D5 is fed directly to the input of the servo summing amplifier (DC Servo Logic Module).

5.1.3   Count Logic (DL3) – The Count Logic comprises the E1 and E2 Servo Sample Holding flip-flops, Tachometer Feedback Velocity Level Detectors and the Count ROM and its associated logic.

5.1.3.1   Count ROM – The Count ROM is a 256 X 4 Bit Programmable Read-Only Memory.   Its purpose is to decrement the Track Difference Counter (DL2) by values of 0, 1, 2 or 3.   Figure 5-7 is a simplified logic diagram showing the count ROM and its associated logic.
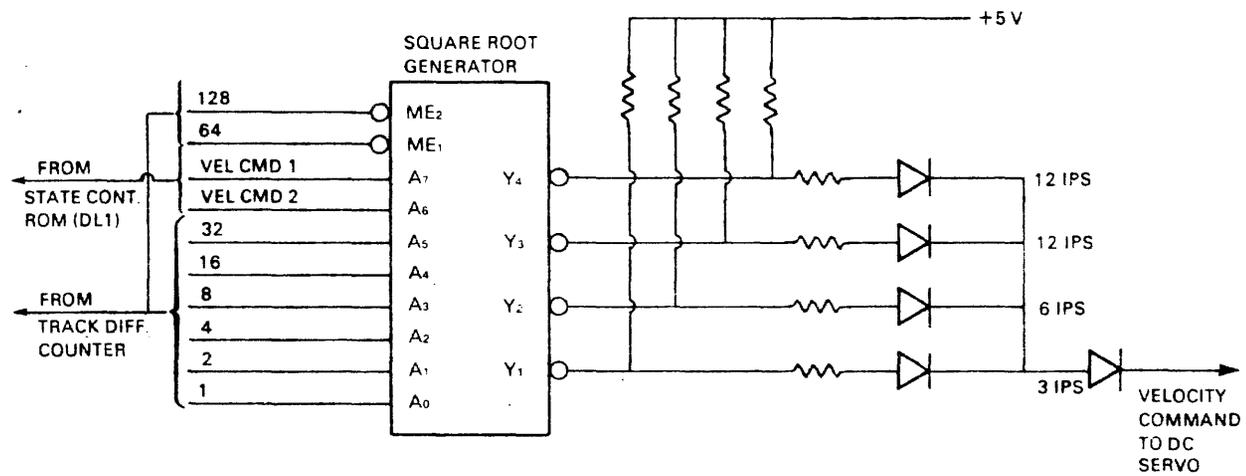
Figure 5-6   Velocity ROM and Velocity Command Generation

Table 5-1 Velocity ROM Addressing

Zeros mean a low logic level, ones mean high and Xs mean "don't care"

COMMAND	VEL CMD 2	VEL CMD 1	TRK CNT 32	TRK CNT 16	TRK CNT 8	TRK CNT 4	TRK CNT 2	TRK CNT 1	12 IPS	12 IPS	6 IPS	3 IPS
BIT	A7	A6	A5	A4	A3	A2	A1	A0	04	03	02	01
E43 PIN NO:	15	1	2	3	4	7	6	5	9	10	11	12
0 IPS (TRK 0)	0	0	0	0	0	0	0	0	0	0	0	0
3 IPS (TRK 1,	0	0	0	0	0	0	0	1	0	0	0	1
2 AND GUARD	0	0	0	0	0	0	1	0	0	0	0	1
BAND)	0	1	X	X	X	X	X	X	0	0	0	1
6 IPS (TRK 3,	0	0	0	0	0	0	1	1	0	0	1	0
4 AND LOAD	0	0	0	0	0	1	0	0	0	0	1	0
HEADS)	1	0	X	X	X	X	X	X	0	0	1	0
9 IPS (TRK 5	0	0	0	0	0	1	0	1	0	0	1	1
AND 6)	0	0	0	0	0	1	1	0	0	0	1	1
12 IPS (TRK 7,	0	0	0	0	0	1	1	1	0	1	0	0
8 AND 9)	0	0	0	0	1	0	0	X	0	1	0	0
15 IPS (TRK 10,	0	0	0	0	1	0	1	X	0	1	0	1
11, 12 AND	0	0	0	0	1	1	0	0	0	1	0	1
UNLD HEADS)	1	1	X	X	X	X	X	X	0	1	0	1
18 IPS (TRKS	0	0	0	0	1	1	0	1	0	1	1	0
13 TO 17)	0	0	0	0	1	1	1	X	0	1	1	0
	0	0	0	1	0	0	0	X	0	1	1	0
21 IPS (TRKS	0	0	0	1	0	0	1	X	0	1	1	1
18 TO 22)	0	0	0	1	0	1	0	X	0	1	1	1
	0	0	0	1	0	1	1	0	0	1	1	1
24 IPS (TRKS	0	0	0	1	0	1	1	1	1	1	0	0
23 TO 27)	0	0	0	1	1	0	X	X	1	1	0	0
27 IPS (TRKS	0	0	0	1	1	1	X	X	1	1	0	1
28 TO 34)	0	0	1	0	0	0	0	X	1	1	0	1
	0	0	1	0	0	0	1	0	1	1	0	1
30 IPS (TRKS	0	0	1	0	0	0	1	1	1	1	1	0
35 TO 41)	0	0	1	0	0	1	X	X	1	1	1	0
	0	0	1	0	1	0	0	X	1	1	1	0
33 IPS (TRKS	0	0	1	0	1	0	1	X	1	1	1	1
42 TO 255)	0	0	1	0	1	1	X	X	1	1	1	1
	0	0	1	1	X	X	X	X	1	1	1	1

Figure 5-7 Count ROM Logic

The eight address bits (A_0 through A_7) provide address-word information which determine binary outputs $\emptyset_1$ through $\emptyset_4$ ($\emptyset-3_{10}$). Information contained in the bits A_0 through A_7 is as follows:

- Velocity Range (A_0, A_1, A_2)

- Previous and present servo samples E_1 and E_2 (A_3, A_4, A_5, A_6)

- Direction (A_7)

The Count ROM Address bits and the count algorithm are defined in Figure 5-7. Note that the Count ROM microcoding is permanently burned in at the factory and is not field programmable.

The Count ROM output word ($\emptyset_1$ through $\emptyset_4$) is programmed so that the LS197 chip counts up until overflow occurs (Q_D goes low). The Q output (least significant bit) provides the count pulses which decrement the Track Difference Counter (DL2).

5.1.3.2   El Held Flip-Flop – This flip-flop stores the previous El servo sample. When the drive is in velocity mode, the El Held flip-flop is used to determine whether the positioner is crossing the inner or outer guard band.

Input:

       Data   = El sample from DL7

       Clock   = Sector time (L) from DL4.

Output:

       Q   = Address Bit 6 (A_6) of the Count ROM

       $\overline{Q}$ Address Bit 2 (A_2) of the Seek Control ROM

Table 5-2 is a truth table which defines Count ROM address bits A_3 through A_6. These bit values are derived from all possible combinations of present and previous servo samples (E_1 and E_2).

Table 5-3 is a truth table which defines count ROM address bits A_0 through A_2. These bit values are derived from distance and tachometer velocity thresholds during 625 microsecond servo sample periods.

Table 5-4 is the complete Count ROM map and algorithm.

Table 5-2   Track Count vs. Servo Samples and Direction

DEC	PREVIOUS		PRESENT		FORWARD				BACKWARD			
	E1	E2	E1	E2	MILS	CNT	MILS	CNT	MILS	CNT	MILS	CNT
Ø	Ø	Ø	Ø	Ø	Ø-4	Ø	12-2Ø	2	Ø-4	Ø	12-2Ø	2
1	Ø	Ø	Ø	1	Ø-8	1	15-24	3	8-16	1	24-32	3
2	Ø	Ø	1	Ø	8-16	2	24-32	4	Ø-8	Ø	16-24	2
3	Ø	Ø	1	1	4-12	1	20-28	3	4-12	1	20-28	3
4	Ø	1	Ø	Ø	8-16	1	24-32	3	Ø-8	1	16-24	3
5	Ø	1	Ø	1	Ø-4	Ø	12-2Ø	2	Ø-4	Ø	12-2Ø	2
6	Ø	1	1	Ø	4-12	1	20-28	3	4-12	1	20-28	3
7	Ø	1	1	1	Ø-8	Ø	16-24	2	8-16	2	24-32	4
8	1	Ø	Ø	Ø	Ø-8	Ø	16-24	2	8-16	2	24-32	4
9	1	Ø	Ø	1	4-12	1	20-28	3	4-12	1	20-28	3
1Ø	1	Ø	1	Ø	Ø-4	Ø	12-2Ø	2	Ø-4	Ø	12-2Ø	2
11	1	Ø	1	1	8-16	1	24-32	3	Ø-8	1	16-24	3
12	1	1	Ø	Ø	4-12	1	20-28	3	4-12	1	2Ø-28	3
13	1	1	Ø	1	8-16	2	24-32	4	Ø-8	Ø	16-24	2
14	1	1	1	Ø	Ø-8	1	16-24	3	8-16	1	24-32	3
15	1	1	1	1	Ø-4	Ø	12-2Ø	2	Ø-4	Ø	12-2Ø	2

Table 5-3   Distance and Velocity Thresholds

Index i	Distance X (MILS)	Velocity V (ips)	Velocity A2	Level A1	Detectors AØ
1	8 (2Q's)	12.8	Ø	Ø	1
2	12 (3Q's)	19.2	Ø	1	1
3	16 (4Q's)	25.6	1	1	1
4	2Ø (5Q's)	32.Ø	N.A.		

Table 5-4   Count ROM Map

DIR FWD =H	SERVO PREVIOUS		SAMPLES PRESENT		VELOCITY SENSE LEVELS (1) (A_2, A_1, A_0)								VEL THRESH
	E_1	E_2	E_1	E_2	A_0 <V_1	>V_1	(2)	>V_2	(2)	(2)	(2),(4)	>V_3	
A7	A6	A5	A4	A3	000	001	010	011	100	101	110	111	
	Ø	Ø	Ø	Ø	0001,	1101,	1101,	1101,	1101,	1101,	1101,	1101	V_1
					1111,	1111,	1111,	1111,	1111,	1111,	1111,	1111	V_4 (3)
					0001,	0001,	0001,	1101,	1101,	1101,	1101,	1101	V_2
					1111,	1111,	1111,	1111,	1111,	1111,	1111,	1011	V_3 (4)
					1111,	1111,	1111,	1011,	1011,	1011,	1011,	1011	V_2
					0001,	1101,	1101,	1101,	1101,	1101,	1101,	1101	V_1
					1111,	1111,	1111,	1111,	1111,	1111,	1011,	1011	V_3
Ø	Ø	1	1	1	1101,	1101,	1101,	1101,	1101,	1101,	1101,	1101	V_4 (3)
BWD	1	Ø	Ø	Ø	1101,	1101,	1101,	1101,	1101,	1101,	1101,	1101	V_4 (3)
					1111,	1111,	1111,	1111,	1111,	1111,	1111,	1111	V_3
					0001,	1101,	1101,	1101,	1101,	1101,	1101,	1101	V_1
					1111,	1111,	1111,	1011,	1011,	1011,	1011,	1011	V_2
					1111,	1111,	1111,	1111,	1111,	1111	1011,	1011	V_3
					0001,	0001,	0001,	1101,	1101,	1101,	1101,	1101	V_2
					1111,	1111,	1111,	1111,	1111,	1111,	1111,	1111	V_4 (3)
	1	1	1	1	0001,	1101,	1101,	1101,	1101,	1101,	1101,	1101	V_1
	Ø	Ø	Ø	Ø	0001,	1101,	1101,	1101,	1101,	1101,	1101,	1101	V_1
					1111,	1111,	1111	1011,	1011,	1011,	1011,	1011	V_2
					1101,	1101,	1101,	1101,	1101,	1101,	1101,	1101	V_4 (3)
					1111,	1111,	1111,	1111,	1111,	1111,	1011,	1011	V_3
					1111,	1111,	1111,	1111,	1111,	1111,	1111,	1111	V_4 (3)
					0001,	1101,	1101,	1101,	1101,	1101,	1101,	1101	V_1
					1111,	1111,	1111,	1111,	1111,	1111	1011,	1011	V_3
1	Ø	1	1	1	0001,	0001,	0001,	1101,	1101,	1101,	1101,	1101	V_2
FWD	1	Ø	Ø	Ø	0001,	0001,	0001,	1101,	1101,	1101,	1101,	1101	V_2
					1111,	1111,	1111,	1111,	1111,	1111,	1011,	1011	V_3
					0001,	1101,	1101,	1101,	1101,	1101,	1101,	1101	V_1
					1111,	1111,	1111,	1111,	1111,	1111,	1111,	1111	V_4 (3)
					1111,	1111,	1111,	1111,	1111,	1111,	1011,	1011	V_3 (3)
					1101,	1101,	1101,	1101,	1101,	1101,	1101,	1101	V_4 (3)
					1111,	1111,	1111,	1011,	1011,	1011,	1011,	1011	V_2
	1	1	1	1	0001,	1101,	1101,	1101,	1101,	1101,	1101,	1101	V_1

NOTES: (1) V_1 = 12.8 ips; V_2 = 19.2 ips; V_3 = 25.6 ips; V_4 = 32 ips

(2)   These address combinations should not occur. Velocity sense levels increment 001, 011, 111.
V_1 V_2 V_3

(3)   Detection level V_4 = 32 ips is important for moves in excess of six quadrants (38.4 ips).

(4)   Address 110 interpreted as 111 (Majority Logic).

5.1.3.3   E2 Held Flip-Flop – This flip-flop stores the previous E2 servo sample. When the drive is in positioner, or "Lock On" mode, the E2 Held flip-flop is used to determine the slope of the Lock On bit (A of the Seek Control ROM – DL1).

Input:

Data   = E2 sample from DL7

Clock   = Sector time (L) (from DL4) or Borrow (M) (from DL2, indicating a new address in the track difference counter)

Set   = Inner Guard Band [Guard Band (L) ^ E1 Held]

Reset   = Outer Guard Band [Guard Band (H) ^ E1 Held (H)].

Output:

Q   = Address Bit 5 (A_5) of the Count ROM

$\overline{Q}$ = Address Bit 0 (A_0) of the Seek Control ROM (DL1).

5.1.3.4   Velocity Level Detectors – These three comparators are used to convert the velocity feedback signal from the positioner tachometer to three binary encoded address inputs to the Count ROM.

The velocity input signal is first rectified by a full-wave rectifier and then distributed to the level detectors.

Input: Refer to Table 5-3.

Output: Refer to Table 5-3.

5.1.3.5   Disable Count 2 Latch – The Disable Count 2 latch prevents extraneous noise and glitches from causing the LS197 counter to count "2" before it has counted "1."

5.1.4   Disk Speed Control Logic (DL4)
This portion of the Drive Logic Module contains the following functional elements:

- Sector Detection Timer

- Disk On Speed Latch

- Sector Time Latch

- Disk Overspeed Latch

- Control Spinup Gate

- Timer and Latch Reset Flip-Flop

Figure 5-8 is a timing diagram for sector detection and spindle speed control.

5.1.4.1   Sector Detection Timer – After the Sector Pulse has been detected, the Sector Detection Timer counts down System clock pulses to provide timing reference for the spindle speed latches. It is reset by the Timer and Latch Reset One-Shot.

5.1.4.2   Disk On Speed Latch – If the time between Sector Pulses is between 594 and 639 microseconds, this latch is set. Its output is sent to the State Control Logic (DL1) to indicate that the disk is on speed.

5.1.4.3   Sector Time Latch – This latch is set by the Sector Pulse and remains set for 62.5 microseconds. Its output, Sector Time (L) is sent to the Count Logic (DL3), the Error Logic (DL5), an the Integrator Logic (DL7) to indicate that a sector has been detected. This latch is reset by the Timer and Latch Reset One-Shot.

5.1.4.4   593 Microsecond Latch – When this latch outputs the signal 593 microseconds LT (L) as true during a sector pulse, a disk over-speed indication is produced, i.e. the time between sector pulses was less than or equal to 593 microseconds. This condition sets the Spin Error flip-flop (on DL5), as well as a bit in the Drive Status Word.

5.1.4.5   Control Speed Up Gate – The signal Control Speedup (L) is generated when the time between sector pulses is longer than 625 microseconds, indicating that the speed of the Spindle Drive Motor is too slow. This gate is disabled by Disk on Speed or the Spin Down command from the State Control Logic (DL1). Control Speed up is sent to the AC Servo Module where it provides more ac power to the Drive Motor.

5.1.4.6   Timer and Latch Reset Flip-Flop – This flip-flop is essentially a one-shot producing a one clock cycle pulse which resets the Sector Detection Timer and Speed Latches. It is set when the zero crossing of the Raw Sector Pulse (from the Sector Transducer) is detected as the signal Sector Detected (L) goes high.

SECTOR DETECTED (L)
DL4 E4-1

~75 μSEC

TIMER AND LATCH RESET (H)
DL4 E4-5

ONE CLOCK CYCLE WIDE

SECTOR TIME (L)
DL4 TP9

62.5 μSEC

PERIOD BETWEEN SECTOR PULSES >640 μs ── PERIOD ≤ 625 μs ── PERIOD ≤ 593 μs

SECTOR DETECTED (L)
DL 4 E4-1

CONTROL SPIN. UP (L)
DI4 E58-8 (AC SERVO J5-7)

DISK ON SPEED (L)
DL 4 E7-4

593 μSEC LATCH (L)
(DISK OVERSPEED) DL4 E13-9

640 – 594 μSEC • DISK ON SPEED

RAN SECTOR PULSE
DL6 E8-8 (J14-5)

SECTOR DETECTED (L)
DL4 E4-1

CZ 1051

Figure 5-8   Sector Detection and Speed Control Timing

5.1.5   Error Logic (DL5) – The error logic portion of the drive logic module contains the logic elements listed below.

- Disk Stopped Timer

- Disk Spinup Timer and Error Latch

- Write Protect Detection and Error Latch

- Clock Error Detector

- Write Gate Error Flip-Flop

5.1.5.1   Disk Stopped Timer – If the drive is not in spinup state (from the State Control ROM), the Disk Stopped Timer will timeout 15 seconds after the last Sector Pulse is detected, generating the signal Disk Stopped (L).   This signal is sent to the AC Servo Module to disable the Spindle Drive Motor.

5.1.5.2   Disk Spinup Timer and Error Latch – The Disk Spinup Timer is started by the Spinup command from the State Control ROM (DL1).   If the Spinup Command is not removed (i.e., disk is not up to speed) within 39 seconds, the Spinup Error Latch and Spin Error flip-flop will be set.

5.1.5.3   Write Protect Detection and Error Latch – A Write Protect condition is sensed when the Write Protect switch on the control panel is depressed.   If this condition exists, one leg of the Write Protect Error Latch is enabled.   If Write Gate from the Controller is detected, the Error Latch is set, producing the signal Write Protect Error (L).

5.1.5.4   Clock Error Detector – Continuous System Clock pulses keep capacitors C_{10} or C_{22} of the Clock Error Detector discharged. If the Clock pulses should stop, one or both of these capacitors will charge up and cause a high level at the inverter.   This will produce the signal Clock Error (L).

5.1.5.5   Write Gate Error Flip-Flop – If Write Gate from the controller is enabled during Sector Time, the Write Gate Error Flip-Flop is set.   This produces the signal Write Gate Error (L), which prevents overwriting of prerecorded servo and header data.

5.1.6   Interface Logic (DL6 and DL8) - The Interface Logic portion of the Drive Logic Module contains the logic elements listed below.

- Interface Line Receivers

- Interface Line Drivers

- Line Receiver Power Supply

- Multiple Drive Selection Error Detector

- Drive Select Logic

- Interface Enable/Disable Logic

- FAULT Lamp Driver

- READY Lamp Driver

5.1.6.1   Sector Pulse Detector - The raw sector pulse, originating from the Sector Detector, is an analog signal. The Sector Pulse Detector shapes the analog signal into a square wave or logic pulse producing the signal Sector Detected (L). Refer to Figure 5-8. This signal is used to generate the 625 microsecond timeout for the Speed Control Logic (DL4).

5.1.6.2   Enable/Disable Interface Controls - Power On Reset (L) is a -8 volt signal from the controller which performs the functions listed below.

- Keeps the drive deselected from the interface bus if DC power is not within tolerances

- When dc power comes up to tolerance, the signal ensures that all drive latches, flip-flops, and counters have been cleared prior to device startup

If the signal AC LO (L) from the controller is enabled, the drive interface bus is disabled.

5.1.7   Integrator Logic (DL7)
The Integrator Logic portion of the Drive Logic Module produces
the E1 and E2 Servo Sample signals, and Positioner signal, and the
Ready to Read/Write signal. The logic elements used to produce
these signals are listed below.·

- E1 and E2 Servo Sample Generation and Integration Logic

  - Servo Data Latch

  - Integrate Circuit Enable/Disable Latches

  - Servo Data Cycle Counter

  - Integrate Enable Flip-Flop

  - E1/E2 Integrator Selector

  - E1 and E2 Integrators and Polarity Detectors

  - Guard Band Detector

- Positioner Signal and Ready to Read/Write Signal Logic

  - Sample one-shot and Driver

  - Position Signal Sample and Hold Circuit

  - Position Null Detector

  - Retrigger Disable Latch

  - Ready to R/W Timeout.

5.1.7.1   E1 and E2 Servo Sample Generation and Integration -
Servo Data, generated by the Read/Write Logic as Servo Data 1 and
2, is distributed to the Integrator Logic by the Servo Data Latch.

Integration Circuit Enable/Disable Latches - These two latches are
used to enable the integration logic during sector time and to
disable the integration logic after two integrations (E1 and E2)
have been performed.

The second latch must be set before the first latch is set. The
first latch must be reset before the second latch is set again.

The second latch is set by Sector Time (L) and Amplitude Sensor
(H), which means no data has been sensed as yet by the Read Logic.
As soon as data is sensed, Amplitude Sensor (L) is enabled. This
allows integrations to be performed. The first latch then counts
two integrations and resets. The second latch will disallow any
further integrations until the next sector time.

Servo Data Cycle Start Flip-Flop - This flip-flop is set when the Integration Circuit is enabled and allows the Servo Data Cycle Counter to be loaded.

Servo Data Cycle Counter - This counter is used to count the ten S_1 and S_2 servo data pulses which are to be integrated by either the E1 or E2 Integrators.

Integrate Enable Flip-Flop - As soon as Servo Data pulses are sensed by the Servo Data Latch and the Servo Data Cycle Counter has started counting the pulses, the Integrate Enable flip-flop is set. This enables either the E1 or E2 Integrators, depending upon which has been selected by the E1/E2 Integrator Selector flip-flop.

Figure 5-9 is a set of scope waveforms showing the Servo Data as sensed by the Read Logic, the output from the Servo Data Latch, the Integrate Enable flip-flop and the resulting output of the integrator.

E1/E2 Integrator Selector - As S_1 or S_2 servo sample bursts are detected, the E1/E2 Integrator flip-flop toggles, selecting either the E1 or E2 Integrator circuits. This flip-flop is held reset if Sector Time is not being sensed.

E1 and E2 Integrators - Ten servo data pulses are integrated by this logic to produce either E1 or E2 sample signals, depending upon which integrator was selected by the E1/E2 Integrator Selector. Figure 5-10 shows integrations performed on servo pulses of 50% and 75% duty cycles, respectively.

Figure 5-11 shows an entire operation cycle of the E1 and E2 Servo Sample Generator and Integration logic.

Guard Band Detector Flip-Flop - If the Guard Band flip-flop detects that only one integration has been performed because only one set of servo samples was detected this flip-flop is set. The special servo format for the Guard band zones on the disk surface comprises contiguous S_1 bursts and an absence of S_2 bursts for the outer Guardband or contiguous S_2 bursts and an absence of S_1 bursts for the Inner Guardband.

If only one integration is performed during Sector Time (i.e., only one of the S_1 or S_2 sample bursts is detected) the Guardband Detector flip-flop is set. If two integrations are performed, the flip-flop is reset, indicating Guardband.

5.1.7.2   Positioner Signal and Ready to R/W Signal Logic -

Sample One Shot and Driver - The Sample One-Shot is set during E1 time by the E1/E2 Integrator Selector. The Sample Driver provided sample timing pulses to the Position Signal Sample and Hold circuit.

INT (H) —— INTEGRATE (H)
E46-5

SERVO —— SERVO DATA LATCH
DATA   E46-6
LATCH.

—— SERVO DATA
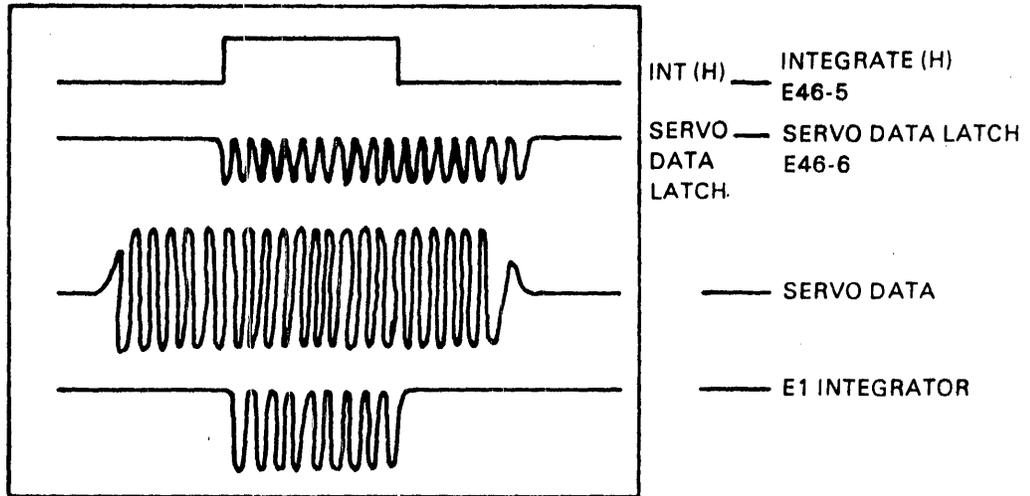
—— E1 INTEGRATOR

CZ-1052

Figure 5-9   Servo Data and Integrate Enable Waveforms

I/5-27

Labels (left to right panels share labels):
INTEGRATE (H)
SERVO DATA LATCH
READ
INTEGRATOR OUTPUT
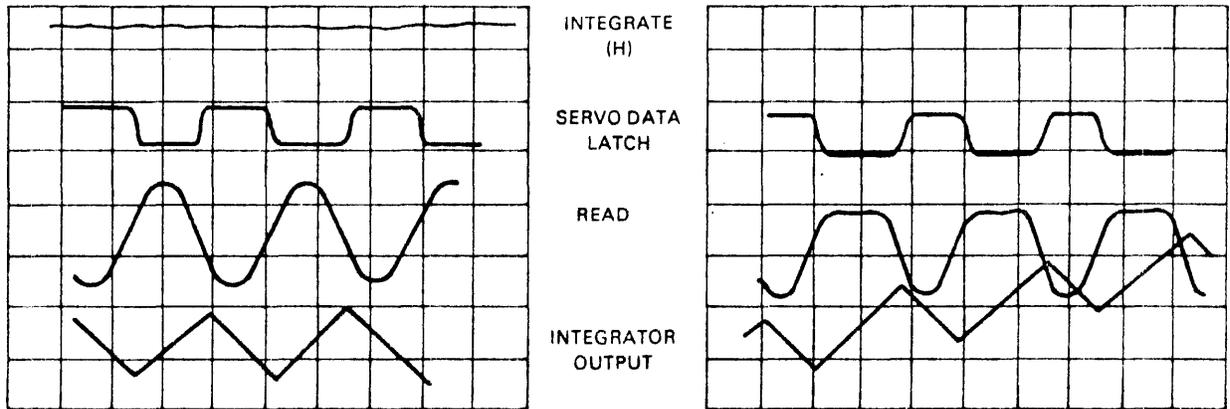
CZ-1053

Figure 5-10 50% and 75% Duty Cycle Integration

SECTOR TIME (L)

SECTOR PULSE (L)

E1, E2, HEADER DATA

AMPLITUDE SENSOR (H)

INTEGRATE ENABLE (H)

E1 TIME (L)

E2 INTEGRATOR

E1 INTEGRATOR

10 μs/DIV
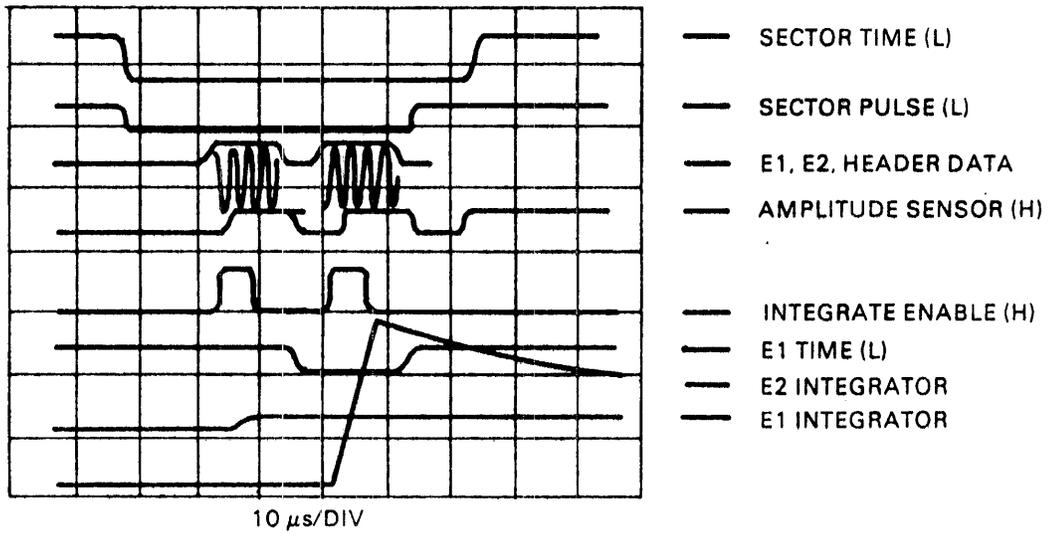
CZ-1054

Figure 5-11   Integrator Logic Waveforms

Position Signal Sample and Hold Circuit - The Position Signal is produced by combining the sample signal timing pulses from the sample one-shot driver and the amplitude of the Integrated El Servo Signal.

Position Null Detector - The Positioner Null Detector senses the amplitude of the Position Signal. When it reaches a level ranging from +0.6 to -0.6 volts, an enable signal is sent to the Retrigger Disable Latch.

Ready to Read/Write Timer - When the Retrigger Disable Latch is set, a 6.5 millisecond timeout occurs. The latch is set by the enable signal from the Position Null Detector and the Signal Enable Timeout (L) from the Velocity Control Logic (DL2). Figure 5-12 is a set of scope waveforms showing the generation of the Ready to Read/Write signal.

5.2   DC SERVO AND POWER MODULE

The DC Servo and Power Module provides regulated dc voltages for the drive and servo amplifier control for the positioner.

The power portion of the module contains the following elements:

- +8 volt, -8 volt, and +5 volt DC Regulators

- +5 volt Reference Source

- Undervoltage Detector

- +5 volt disable and Emergency Retract Control

- Overvoltage Crowbar

- Invert/Non-Invert Sensors

The Servo Amplifier portion of the Module contains the following elements:

- Velocity/Positioner Mode Selection Switches

- Invert/Non-Invert Selection Control

- Summing Amplifier

- Power Amplifier

- Tachometer Amplifier

- Motor Current Sensing Resistor

E25-10

READY TO R/W
E25-5

POSITIONER SIGNAL
(1 TRACK SEEK)
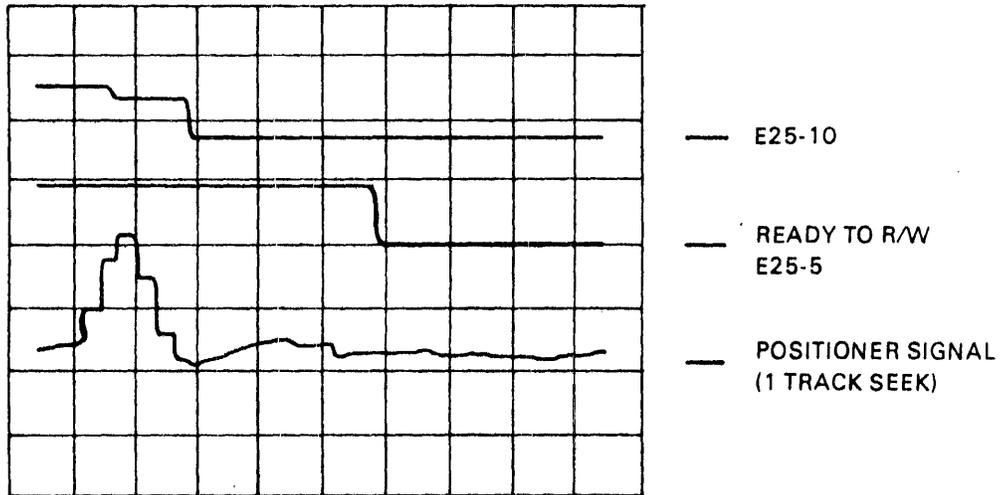
CZ-1055

Figure 5-12   Ready to Read/Write Generation

5.2.1 Voltage Regulators

Inputs to the +8, -8, and +5 volt regulators is provided by the ±11.5 volt power supply which is located on the drive power panel.

The 5 amp pico fuse protects the drive logic in the event of a short within the +5 volt regulator.

5.2.2 Overvoltage Crowbar

If the 5 volt regulator fails (5 volt level increases to 6.5 volts), the Overvoltage Crowbar provides current limiting protection.

5.2.3 +5 Volt Disable and Emergency Retract

If the read/write heads are loaded and a 5 volt undervoltage condition is detected, the signal Home Drive is enabled. This signal is fed directly to the DC Servo Summing Amplifier and results in an emergency retraction of the positioner at a velocity of 15 ips.

5.2.4 Undervoltage Detector

If this circuit detects a +5 volt undervoltage condition, the signals Power On Reset (L) and DC Low (H) are generated. Power On Reset (L) is used to clear all device registers and logic in the event of a momentary power failure or during device startup.

5.2.5 Invert/Non-invert Selection Control

The Direction signal from the State Control Logic (DL1) is sensed by the Invert/Non-invert detectors (Sheet 1). The signal Non Invert (L) allows the positioner to be driven forward (toward the spindle). The signal Invert (L) allows the positioner to be drive backward (away from the spindle).

5.2.6 Velocity/Positioner Mode Selection Switches

The positioner is in Velocity Mode except when it is locked on a data track (Positioner Mode). The signal Velocity Mode (L) from the State Control ROM (DL1) enables the Velocity Command from the Velocity ROM 6(DL2) to drive the positioner during seeks, load head state, etc. The signal Positioner Mode (L) enables the Positioner Signal to drive the positioner in one-half track increments when it is locked on a predetermined data track.

5.2.7 Tachometer Amplifier

The Tachometer Amplifier produces the Velocity Signal from the positioner velocity feedback signal. The Tachometer Velocity signal is sent to the Count Logic (DL3) where it is decoded into three velocity levels for address inputs to the Count ROM.

5.3   READ/WRITE MODULE
The Read/Write Module contains the logic elements listed below.

- Head Selection and Steering Logic

- Write Enable flip-flop

- Write Data flip-flop

- Write Current Source and Switch

- Write Current Drivers

- Write Data Error Detector

- Current in Heads Detector

- Read Amplifier

- Zero Crossing Detectors

- Servo and Read Data Pulse Detectors

- Amplitude Sensor Level Detectors

- Fall-Time Detector

- Pick-Time Detector

5.3.1   Head Selection and Steering Circuit
The signal Head Select Zero (L) enables the Head Select $\emptyset$ Gate and
disables Head 1 by pulling its center tap to ground. This allows
Read Data sensed by Head $\emptyset$ to be sent to the Read Preamplifier
(sheet 2) via steering diodes D_{11} and D_{13}.

If Head Select Zero is high, the center tap of Head $\emptyset$ is grounded
and Read Data from head 1 is sent to the Read Preamplifier via
steering diodes D_{12} and D_{14}.

During a write operation, the combination of Write Gate (L) and
Head Select Zero is used to enable the Write Head Zero Gate or the
Write Head 1 Gate. If head $\emptyset$ is selected, transistors Q_4 and Q_6
are turned on. If head 1 is selected, transistors Q_5 and Q_7 are
turned on.

The steering network for head $\emptyset$ comprises diodes D_7, D_8, D_{11}, and
D_{13}.   During a write operation, write current is fed to head $\emptyset$
from the Current Drivers (Q_2 and Q_3) via steering diodes D_7 and
D_8.

The steering network for head 1 comprises diodes D_9, D_{10}, D_{12}, and D_{14}. During a write operation, write current is fed to head 1 from the Current Drivers (Q_2 and Q_3) via steering diodes D_9 and D_{10}.

5.3.2   Write Current Source and Drivers
The write current source generates 90 milliamperes of current for the Write Current Drivers. The signal Write Gate (H) enables the Write Current Switch. Write data from the Write Data flip-flop switches the Write Current Drivers Q_2 and Q_3.

5.3.3   Write Data Flip-Flop
The Write Data flip-flop is held reset by the Write Enable flip-flop until the first write data pulse from the controller is sensed in conjunction with Write Gate.

5.3.4   Write Error Detector
The signal Write Data Error Pulse (L) is generated when Write Gate (L) is enabled and no Write Data is detected.

5.3.5   Current in Heads Detector
The signal Current in Heads (L) is sent back to the Error Logic (DL5) where it is compared with the signal Write Gate. If there is write current flowing in the heads and no Write Gate is detected, a Current In Heads Error is generated.

5.3.6   Read Amplifier Circuits
The Read Amplifier portion of the Read/Write Module comprises the elements listed below.

- A Read Preamplifier which amplifies the raw output from the selected head

- A differentiator (L_1 and C_8) which converts the raw analog read signals to pulsed waveforms

- A filter network (L_2, L_3, L_4, C_{15}, and C_{16}) which removes noise from the read pulses.

5.3.7   Zero Crossing Detectors
The Zero Crossing Detectors separate the filtered read pulses into separate pulse trains which are then shaped by R/C networks C_{17}, R_{50} and C_{39}, R51.

5.3.8   Amplitude Sensor
The Amplitude Sensor Level Detectors, the Pick-time Detector, and Fall-time Detector generate the data pulse envelope signal Amplitude Sensor (H). This signal identifies the S_1 and S_2 Servo Data Pulses and the Header Data.

5.4 AC SERVO MODULE
The AC Servo Module provides the functions listed below.

- Control of the cartridge Access Door Solenoid which prevents opening the door until the disk has stopped rotating

- Brush drive motor control

- Spindle drive motor control

5.4.1 Cartridge Access Door Solenoid
When the State Control Logic (DL1) is in the Load Cartridge Sate, the signal Load Cartridge Enable (H) is generated. This signal turns off transistor Q_5 which, in turn, produces the signal Solenoid Drive (H). The access door may be opened at this time. When the RUN pushbutton is depressed, Load Cartridge Enable goes low, energizing the solenoid and locking the access door.

5.4.2 Brush Drive Motor Control
When the State Control Logic (DL1) is in the Brush Cycle State, the signal Brush Cycle (L) is generated. This signal energizes the Brush Motor Relay K1 which applies ac hot to the Brush Motor. When the Brush Motor has made one complete revolution, sweeping the cam-driven brushes across the disk surface, the Brush Home Switch is again closed. The State Control Logic disaables Brush Cycle (L) which deenergizes the Brush Motor Relay.

5.4.3 Spindle Drive Motor Control
The Spindle Drive Motor is controlled by the AC Servo Module during the three states of the State Control ROM listed below.

- Spinup

- Controlled Speed (RUN mode)

- Spin down.

5.4.3.1 Spinup State - After the cartridge has been loaded, the cartridge access door has been closed, and the RUN switch has been depressed, the State Control ROM goes into the Spinup State. As the disk turns, the sector slots located on the cartridge armature are sensed by the sector transducer. The disk speed is checked by counting the number of Clock Pulses between sector pulses. If the disk speed control logic determines that the spindle speed is too low (more than 640 microseconds between sector pulses), the signal Control Speed Up (L) enables the photo coupler E2 which switches an R/L network into the SCR drive circuit. This provides 60% of the available ac power to the spindle motor. As soon as the spindle speed reaches the point where the time between sector pulses is 639 microseconds, the Disk Speed Control Logic (DL4) generates the signal Disk On Speed (L).

5.4.3.2   Controlled Speed State - The AC Servo Module is in the controlled speed state when the time between sector pulses ranges from 640 to 593 microseconds.

When the time between sector pulses reaches 625 microseconds, Control Speed Up is disabled. This allows another R/L network to be switched into the SCR drive circuit and provides 20% of the available ac power to the drive motor.

5.4.3.3.   Spin Down State - If the State Control ROM goes into the Spin Down State, it generates the signal Brake (L). Brake (L) energizes Relay K_2 and enables photocoupler E1 to provide a half-wave dynamic brake signal to the motor.

SECTION II   SERVICING PROCEDURES

This chapter defines the maintenance philosophy and acquaints the reader with the structure of this portion of the manual. It defines the required resources available to correctly maintain the RLØ1/RLØ2 Disk Subsystem. The maintenance controls and indicators are also discussed here.

1.1 MAINTAINABILITY FEATURES
The following paragraphs summarize the RLØ1/RLØ2 Hardware Maintenance Plan. The manual organization is outlined and an overview of the various troubleshooting techniques is discussed. A listing of Field Replaceable Units (FRUs) is also given.

1.1.1 Hardware Maintenance Plan
Serviceability has been a major consideration in the design of the RLØ1/RLØ2 Disk Subsystem. A large portion of the drive electronics has been incorporated on one logic module, the drive logic board. The remaining electronics exist on the read/write module, dc servo module, ac servo module and the front panel.

All electromechanical subassemblies and logic modules can be replaced in an average time of twenty minutes. This replacement capability is accomplished without the aid of special alignment fixtures or tools. These designed-in features readily permit a maintenance philosophy of module or subassembly swap-out. Therefore, the troubleshooting strategy is to isolate the failing module or subassembly and replace it.

1.1.2 Additional Documentation
Table 1-1 lists the hardware documentation that will be available to support the RLØ1/Ø2 Disk Subsystem.

Table 1-1   RL∅1/∅2 Documentation

Name	Microfiche Number	Hard Copy Number
RL11 Controller Technical Description Manual	EP-∅RL11-TD	EK-∅RL11-TD
RLV11 Controller Technical Manual	EP-RLV11-TD	EK-RLV11-TD
RL8A Omnibus Controller Technical Manual	EP-∅RL8A-TM	EK-∅RL8A-TM
RL∅1 Disk Drive Illustrated Parts Breakdown	EP-∅∅∅16-IP	EK-∅RL∅1-IP
RL∅2 Disk Drive Illustrated Parts Breakdown	EP-∅∅∅16-IP	EK-∅RL∅2-IP
RL∅1/RL∅2 Preventive Maintenance Procedures	EP-∅∅∅∅8-PM	EK-RL∅12-PM
RL∅1/RL∅2 Pocket Service Guide	N/A	EK-RL∅12-PG
RL∅1/RL∅2 Disk Subsystem User's Guide	N/A	EK-RL∅12-UG

1.1.3 Field Replaceable Units

Table 1-2 is a list of RL01/RL02 Field Replaceable Units (FRU's).
Some of the FRU's contain components that are easily checked and
replaced. In these cases, an FRU may be repaired instead of
replaced. For example, a lamp may be replaced on the front panel
or a pico fuse replaced on the DC Servo module. The decision to
replace or repair an FRU should be based on such local
considerations as part availability, etc.

Some of the FRUs are interchangeable between the R1Ø1 and RLØ2 and
some are not. The interchangeability is indicated in Table 1-2.

Table 1-2   FRU Part Numbers and Interchangeability

The following FRUs are downward-compatible only. The RLØ2 modules
can be used on either drive with just a jumper change. The RLØ2
spindle can be used on either drive.

FRU	RLØ1 Part Number	RLØ2 Part Number
Read/Write Module	54-11844	54-13536
DC Servo Module	54-11850	54-13534
Template for DC Servo	74-18588	74-20826
Drive Logic Module (DLM)	54-12175	54-13531 (early)
		54-14025 (later)
Spindle	70-12120	70-15116

The following FRUs are the same for both drives.

FRU	RLØ1/Ø2 Part Number
5 amp fuse (DC Servo)	12-05747-00
AC Servo Module	54-11848
Front Panel	54-11846
Front Panel Lamp (GE 73)	12-12716-01
Sector Transducer	70-12137
Positioner	70-12117
Brush Drive Assembly	70-12112
Brush Assembly	70-16726
Spindle/Blower Motor	70-12114
Spindle Drive Belt	12-13369
Spindle Ground Brush	74-15294
Coarse Filter	74-15297
Absolute Filter	12-13097-03
I/O Terminator	70-12293-00

Table 1-2   FRU Part Numbers and Interchangeability

FRU   RL01/02 Part Number

Power Panel   70-12130
● Terminator Block
  (voltage selection)   74-16852-01A
● Circuit Breaker   12-14360-02
● Line Filter   12-12877-00
● Rectifier   11-10051-00
● transformer   16-13897-00
● Cap, 66,000 uF for + Vunreg   10-1353-00
● Cap, 20,000 uF for - Vunreg   10-13531-00
● Cap, for spindle motor   10-13102-00
● Muffin fan   12-09403-01

The following FRUs are not interchangeable between an RL01 and an
RL02.

FRU	RL01 Part Number	RL02 Part Number
Upper Head	74-17178-01	70-15637-01
Lower Head	74-17178-00	70-15637-00

1.1.4   Recommended Spare Parts List
Table 1-3 shows the Recommended Spare Parts List.

Table 1-3   Recommended Spare Parts List

Part Number	Description	Branch Stocked	Spares Kit
70-12130	Power Panel	Y	N
54-11844	Read/Write Module (RL01 only)	Y	Y
54-12526	Read/Write Module (RL01, RL02)	Y	Y
54-11846	Front Panel Board	Y	Y
54-11848	AC Servo Module	Y	Y
54-11850	DC Servo Module (RL01 only)	Y	Y
54-13534	DC Servo Module (RL01, RL02)	Y	Y
54-12175	Drive Logic Module (RL01 only)	Y	Y
54-14025	Drive Logic Module (RL01, RL02)	Y	Y
70-12107	Front Panel Cable	N	N
70-12108	Harness Power Panel	N	N
70-12109	Line Cable	Y	N
70-12110	Muffin Fan Cable	N	N
70-12112	Brush Drive Assembly	Y	Y
70-12114	Disk Motor Assembly	Y	N
70-12117	Positioner Assembly	Y	N
70-12119	Rear Cover	N	N
70-12120	Spindle Assembly (RL01 only)	Y	N
70-15116	Spindle Assembly (RL01, RL02)	Y	N

Table 1-2   Recommended Spare Parts List (Cont.)

Part Number	Description	Branch Stocked	Spares Kit
70-12123	Cable Logic	N	N
70-12126	Brush/Door Harness	N	N
70-16852-01A	Terminal Block Assembly	Y	N
70-12136	Positioner Harness	N	N
70-12137	Transducer Assembly	Y	Y
70-12139-01	Read/Write Cable	N	N
70-12139-02	AC Servo Cable	N	N
70-12140	DC Power Harness	N	N
70-12142	Power Harness	N	N
12-13369	Drive Belt	Y	Y
74-15297	Prefilter	Y	N
12-13097-03	Absolute Filter	Y	N
74-17178-00	Head "A" Up (RL01)	Y	Y
74-17178-01	Head "A" Down (RL01)	Y	Y
70-15637	Head "A" Up (RL02)	Y	Y
70-15638	Head "A" Down (RL02)	Y	Y
RL01K-DC	Cartridge (RL01)	Y	N
RL02K-DC	Cartridge (RL02)	Y	N
70-12293	Terminator	Y	N
70-12139-0D	DC Servo Cable	N	N
74-15231	Gasket, Blower	Y	N
12-09403-01	Fan	Y	N
12-14360-02	Circuit Breaker	N	N

1.2   SOFTWARE RESOURCES

1.2.1   Diagnostics
The various diagnostics available for RL8-A, RL11 and RLV11-based subsystems are described in Appendix B, Paragraph B.8, "Confidence Testing".

1.2.2   Diagnostic Supervisor
All of the diagnostics run under the Diagnostic Supervisor. When one of the diagnostics is called up, the Supervisor asks a series of questions that enable the operator to set various parameters governing the specific diagnostic.   The various commands the Supervisor will accept are summarized in the following paragraphs. (Questions whose answers are self-evident are not explained here.)

1.2.2.1   Hardcore Questions - Several of the questions that the Supervisor will ask do not have simple yes or no answers. These include the questions explained below.

The Supervisor will display the statement "TYPE TWO CHARACTER FOUR SECONDS APART" when no clock is on the system. The system will then subdivide the spacing for use as a clock. The four second interval should be as accurate as possible.

The prompt "DS-C>" is requesting one of eleven supervisor "commands", which are listed in Table 1-4.

Table 1-4 Diagnostic Supervisor Commands

COMMAND	DESCRIPTION
STA	STArt diagnostic and then produce questions for generation of the diagnostic parameter tables ("P" tables).
RES	REStart diagnostic at the point following the hardware questions. The "P" tables set up by the STA command will be used.
CON	CONtinue the diagnostic at the beginning of the subroutine that was being executed when the diagnostic was halted by an error or control "C".
PRO	PROceed testing with the diagnostic at the starting address of the subroutine following the one that caused the error report.
DIS	DISplay the hardware "P" tables for all the drives under test.
DRO	DROp the desired units from being tested. "UNITS", in this case, refers to the "P" table units, not necessarily the device unit numbers. The DIS command will give the operator the drive unit number.
ADD	ADD units back into the testing sequence after they had been dropped by the DRO command.
PRI	PRInt any performance or statistical tables accumulated by the diagnostic.

Table 1-4   Diagnostic Supervisor Commands (Cont)

COMMAND   DESCRIPTION

FLA   FLAgs command – The current setting
                             of all the flags set up under the
                             STA command are printed out for
                             inspection.

ZFL   Zero FLags command – All current
                             flags set by the STA command are
                             cleared by this command.

CCI   Create Core Image command – This
                             command enables a BIC file to be
                             created on these diagnostics to be
                             run under the XXDP media.   (See
                             listing for directions.)

Program Parameter Changes – Type in any combination of the
parameters listed in Table 1-5 to affect the indicated commands.

Table 1-5   Command Parameters

COMMAND   PARAMETER

STA   DS-C>STA/TESTS: (insert test numbers
                             desired from the test lists in the
                             individual diagnostic listings; e.g.
                             1:2 means tests 1 and 2, or 1-5:8-10
                             means tests 1 through 5 and 8
                             through 10.)

                             DS-C>STA/TESTS:6/PASS: (insert the
                             number of passes the diagnostic
                             should take before halting)

                             DS-C>STA/TESTS:6/PASS:2/FLAGS:
                             (insert any of these mnemonic(s)
                             representing a program flag(s)):

                             HOE – Halt On Error
                             LOE – Loop On Error
                             IER – Inhibit Error Report
                             IBE – Inhibit Basic Error
                                   reporting
                             IXE – Inhibit eXtended Error
                                   reporting
                             PRI – PRInt messages on line
                                   printer
                             PNT – PriNt Test numbers as
                                   they are being executed

Table 1-5   Command Parameters (Cont)

COMMAND	PARAMETER

	BOE - Bell On Error
	UAM - Bypass manual
	      intervention tests
	ISR - Inhibit Statistical
	      Reports
	IDR - Inhibit DRopping of
	      units

STA (cont)	DS-C>STA/TESTS:6/PASS:2/FLAGS:IER: PNT:BOE:IDR/EOP: (insert a number equalling the pass intervals at which the End Of Pass message will be printed; e.g. every other pass, every third pass, etc.) For example, utilizing all the possible parameter changes, the STA command would look like this: DS-C>STA/TESTS:6/PASS:2/FLAGS:IER: PNT:BOE:IDR/EOP:3
RES	Use TESTS, PASS, FLAGS and/or UNITS to be tested; e.g. DS-C>RES/TESTS:6 /UNITS:1 (this will run only test 6 on the device specified in "P" table 1)
CON	Use PASS or FLAGS only
PRO	Use FLAGS only
DRO	Use UNITS only
DIS	Use UNITS only
ADD	Use UNITS only
PRI	No variations
FLA	No variations
ZFL	No variations
CCI	Use TESTS, PASS or FLAGS

1.2.2.2 Console Controls – There are three console controls that can be used to affect a running diagnostic. They are all typed by holding down the "CONTROL" key while typing the specific letter.

Control "C" causes testing to cease and a return to the start (DS-C>).

Control "Z" causes default values to be taken in any of the three operator dialogues.

Control "O" causes a supression of typeouts for the remainder of the diagnostic or until another control "O" is typed.

1.2.2.3 Hardware Questions – It is during the hardware question portion of the Supervisor that the "P" (parameter) tables are built. There is one "P" table for every unit to be tested. Also, "UNITS" pertains to the "P" table number, not the device unit number. If there is doubt as to which unit number has been assigned to which drive, the DIS command (see Table 1-12) will supply the necessary information.

1.2.2.4 Software Question – The question "CHANGE SW(L)?" asks if any of the software parameters are to be changed. A "Y" will cause the program to ask various questions. For more detail refer to the individual program document.

1.3 MAINTENANCE CONTROLS AND INDICATORS
Figures 1-1 and 1-2 show all RL01/RL02 Disk Drive controls and indicators.

1.3.1 Power ON/OFF Circuit Breaker
When the ac power plug is inserted into a 115/230 Vac, 50/60 Hz outlet, ac power is applied to the rear panel circuit breaker on the drive. When the circuit breaker is turned on, ac power is applied to the drive and the blower motor is energized.

1.3.2 Power Terminal Block Assembly
The RL01/RL02 Disk Drive operates within two ac line voltage ranges at either 50 or 60 Hz:

    ^   90 – 132 Vac
    ^   180 – 264 Vac

These voltage ranges may be manually selected by changing the position of the terminal block assembly covers located at the rear of the drive. Refer to Figure 1-2.

LOAD SWITCH
AND INDICATOR

UNIT SELECT PLUG
AND READY INDICATOR

FAULT
INDICATOR

WRITE PROTECT SWITCH
AND INDICATOR
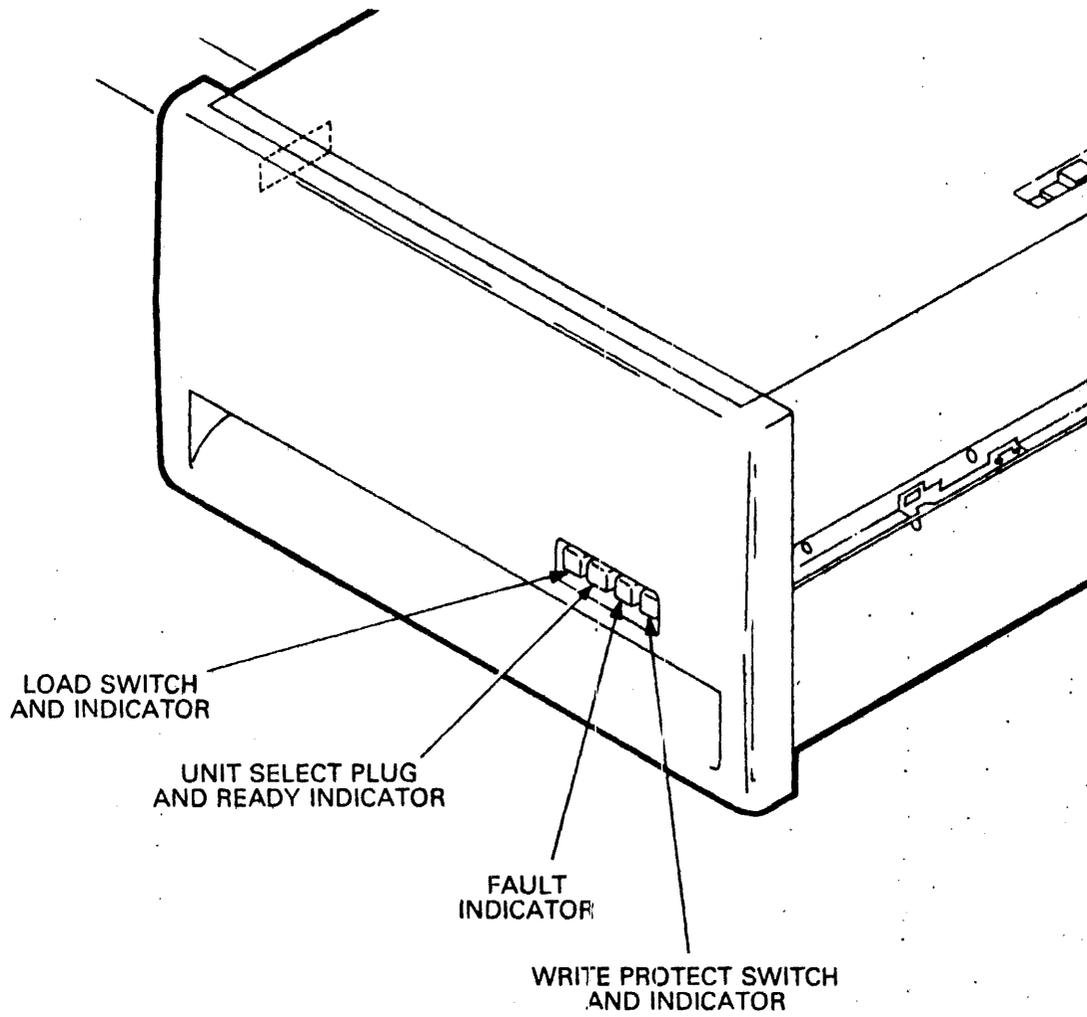
CZ-1005

Figure 1-1   RL01/RL02 Disk Drive Controls and Indicators
(Front Panel)

I/O CABLE ("CABLE IN")

TERMINATOR

NORMAL/LOW LINE VOLTAGE TERMINAL BLOCK COVER

110/220 VOLTS TERMINAL BLOCK COVER

CIRCUIT BREAKER

AC LINECORD

CABLE "OUT"
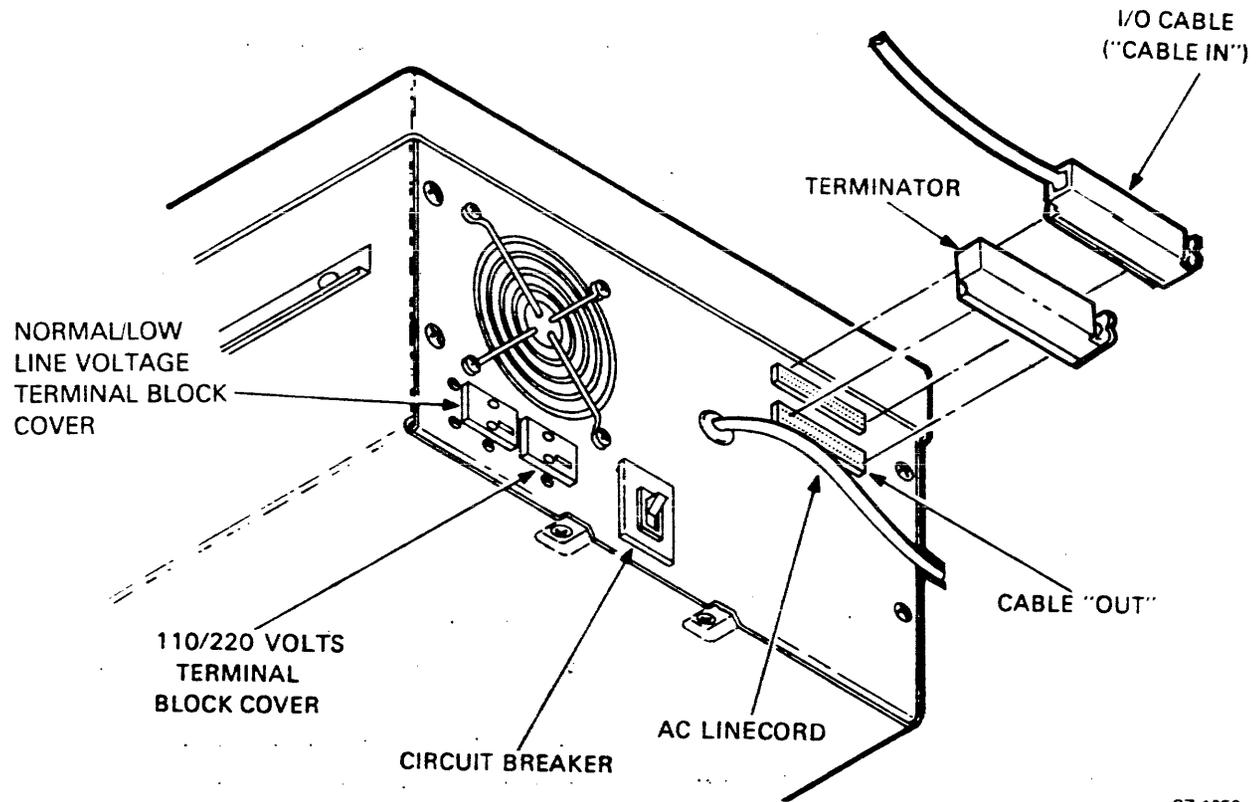
CZ-1056

Figure 1-2   RL01/RL02 Disk Drive Controls and Indicators (Rear Panel)

1.3.3 Run/Stop Switch with LOAD Indicator

This push on/push off switch, when depressed, energizes the spindle motor providing all of the following conditions have been met:

- The disk cartridge has been installed

- The cartridge protective cover is in place and the cartridge access door is closed

- All ac and dc voltages are within specifications

- The read/write heads are in the home position (retracted)

- The brushes are in the brush home position

When the run/stop switch is released, the spindle drive motor is deenergized if the read/write heads are not loaded. If the heads are loaded, they are immediately retracted and the spindle drive motor is then deenergized. In the event of a main power interrupt and subsequent power restoration, the drive will recycle up if the switch is in the depressed state since it contains mechanical memory.

The LOAD enable indicator is illuminated whenever all of these conditions have been met:

- The spindle is stopped
- The read/write heads are home
- The brushes are home
- The spindle drive motor is not energized

1.3.4 Unit Select (0, 1, 2, 3) Switch with READY Indicator

The unit select switch is a cam operated switch which is actuated by inserting a numbered, cammed button. The switch contacts are binary encoded so the drive interface logic recognizes the matching controller generated drive address code and the corresponding unit select number (0, 1, 2, or 3).

The numbered indicator, when lit, indicates a drive READY condition. This condition exists when all of these conditions have been met:

- The read/write heads are loaded
- The heads are detented on a specific track

1.3.5 FAULT Indicator

The FAULT indicator is lit whenever any of the following fault or error conditions develop in the disk drive:

- Drive Select Error
- Seek Time Out Error
- Write Current in Heads during Sector Time Error
- Loss of System Clock
- Write Protect Error
- Write Data Error
- Spin Error

1.3.6 WRITE PROTect Switch and Indicator

When this switch is pushed in, it will lock in the depressed position and the drive will be write protected. If the drive is writing as the switch is pushed in, FAULT will light. When the switch is pushed again, releasing it from the depressed state, the drive will no longer be write protected.

2.1 INTRODUCTION

This chapter describes the removal and replacement procedures for the various Field Replaceable Units (FRUs) in the RLØ1 and RLØ2 Disk Drives. The flow chart in Figure 2-1 illustrates the sequence of FRU removal. For example, to remove the spindle, the Cartridge Access Cover must be removed. This is followed by the Field Service Access Cover, the Spindle Access Cover and the belt from the spindle pulley. The FRUs are generally replaced in reverse order of removal.

The number in each oval of Figure 2-1 is the paragraph that describes the removal and replacement for that particular FRU.

Most of the removal and replacement procedures in this chapter contain references to earlier paragraphs. This drive is simple enough that the FE should not have to refer back to these other paragraphs once he has had some experience on the drive. The flow chart can serve as a quick reminder, if necessary.

2.2 FRONT BEZEL AREA

2.2.1 Front Bezel

To remove the front bezel:

1. Turn CB1 (rear panel) off and extend drive from cabinet.

2. Locate and remove the Phillips head screws as shown in Figure 2-2.

CAUTION
When removing the last screw, hold the front bezel so that the bezel will not strain the front panel switch cable.

3. Disconnect the front panel board cable. Note the orientation of the colored stripe on the cable.

To replace the front bezel:

1. Connect the front panel board cable.

2. Locate the top mounting holes in the front bezel and align them with the top mounting holes in the drive frame (Figure 2-2).

3. Secure the front bezel with the Phillips head screws, finger-tight only.

4. Slide the drive into the cabinet and align the front bezel for correct side-to-side clearance.

Figure 2-1   Removal and Replacement Sequence Flow Chart

FRONT BEZEL

PREFILTER

FRONT
PANEL
CABLE

MOUNTING
SCREWS (4)
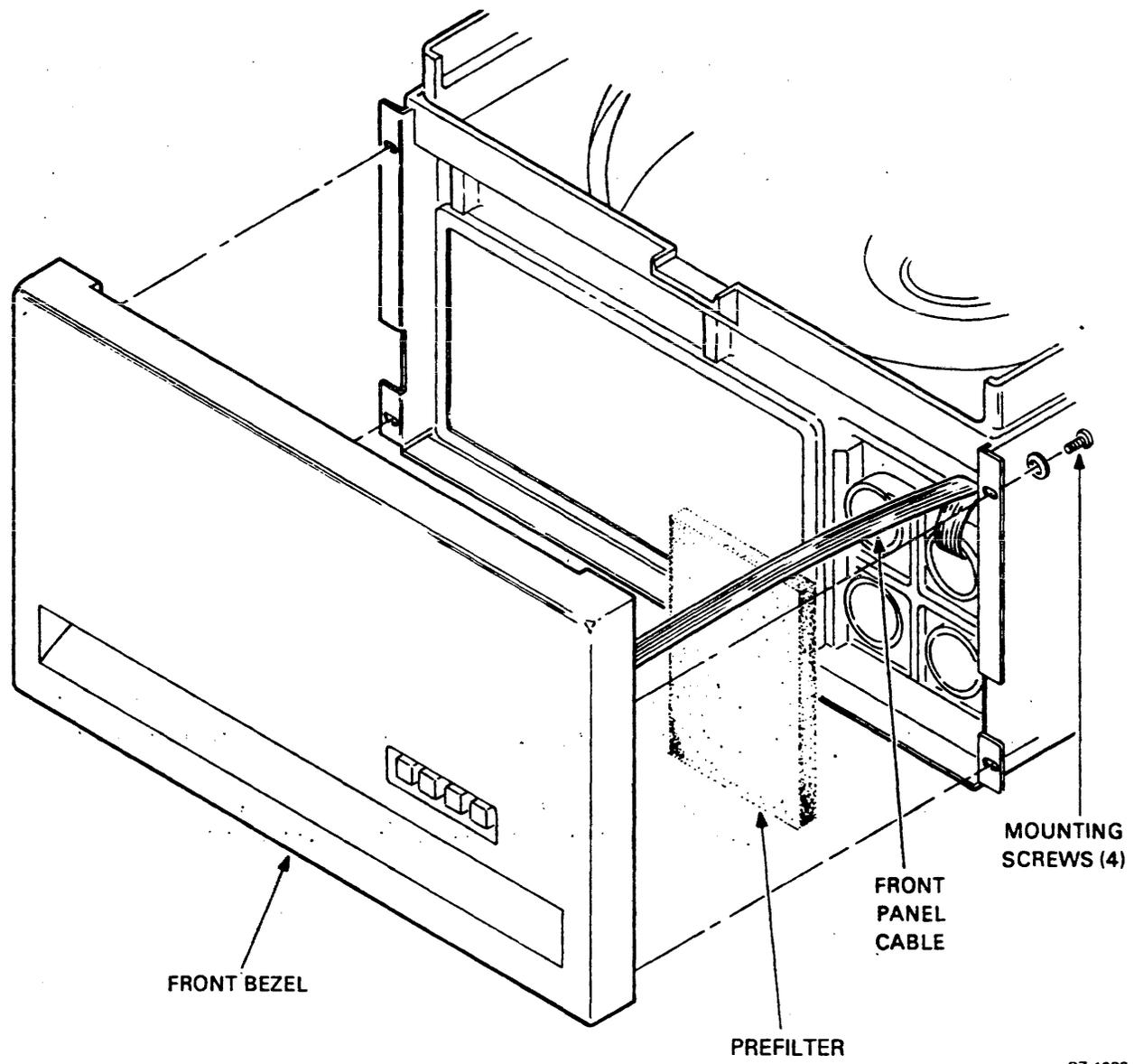
CZ-1080

Figure 2-2   Front Bezel

5.   Extend the drive from the cabinet and tighten the Phillips head screws securely.

6.   Slide the drive back into the cabinet.

2.2.2 Prefilter

To remove the prefilter: .

1.   Remove the front bezel (Paragraph 2.2.1).

2.   Remove the prefilter located on the right front side of the drive (Figure 2-2).

To replace the prefilter:

1.   Install the prefilter in the recess located on the right front side of the drive, directly over the four air chamber tubes (Figure 2-2).

2.   Replace the front bezel (Paragraph 2.2.1).

2.2.3 Absolute Filter

To remove the absolute filter:

1.   Remove the front bezel (Paragraph 2.2.1).

2.   Locate the two plenum springs and two plenum cover latches as shown in Figure 2-3.

3.   Lift one of the plenum latches. While holding plenum spring, squeeze the latch and remove latch from bracket.

4.   Remove plenum spring.

5.   Repeat for the other plenum latch and spring.

6.   The plenum cover may now be removed by pulling the cover forward. This allows access to the filter (Figure 2-4).

7.   Use a screwdriver (or one of the plenum springs) to pry the left side of the filter out slightly **before** moving the right side. The filter can then be removed by rocking it from side to side until it slides free.

NOTE
Never reinstall a used absolute filter.

PLENUM
LATCH
(2 PLACES)

PLENUM
SPRING
(2 PLACES)

NOTE: SPRING MUST BE HELD DOWN
IN POSITION BEFORE INSTALLING LATCH LEVER
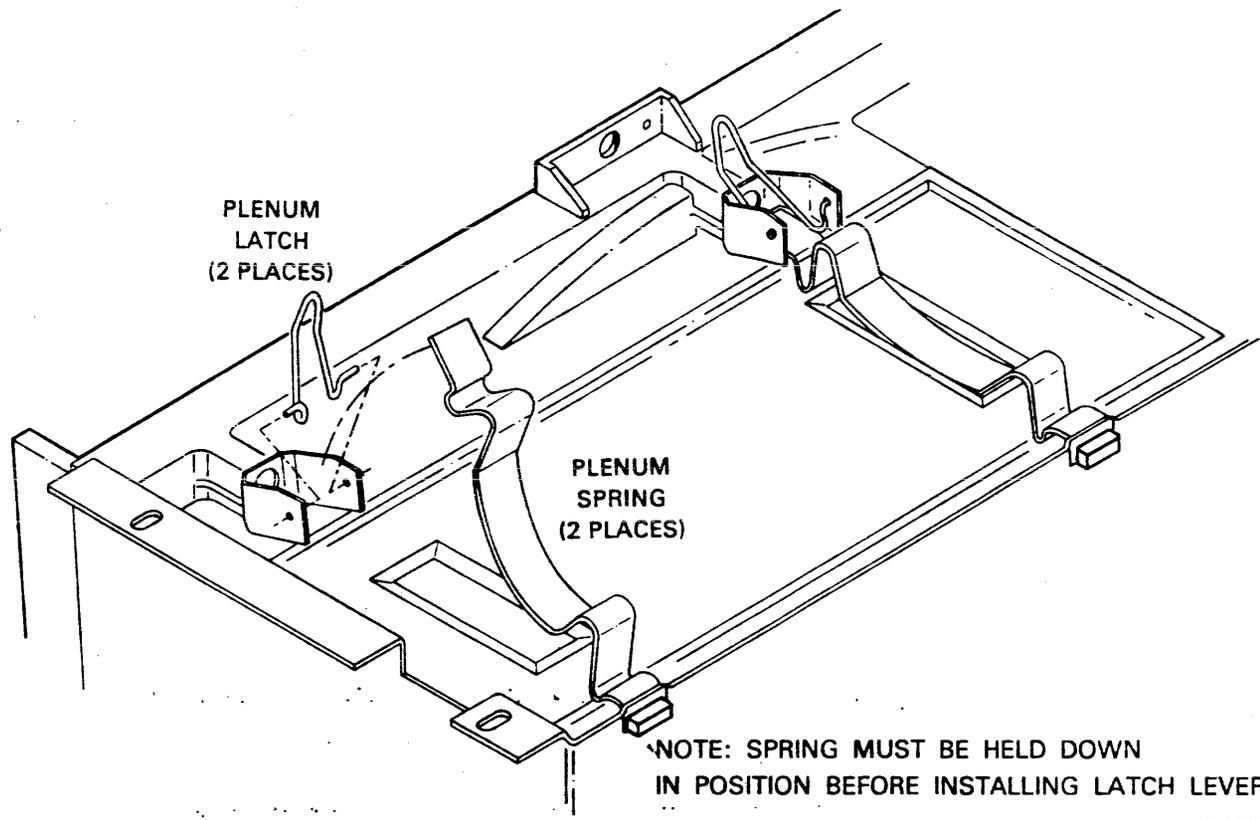
CZ-1058

Figure 2-3   Absolute Filter Access

ABSOLUTE
FILTER

AIR
FLOW

PLENUM
COVER
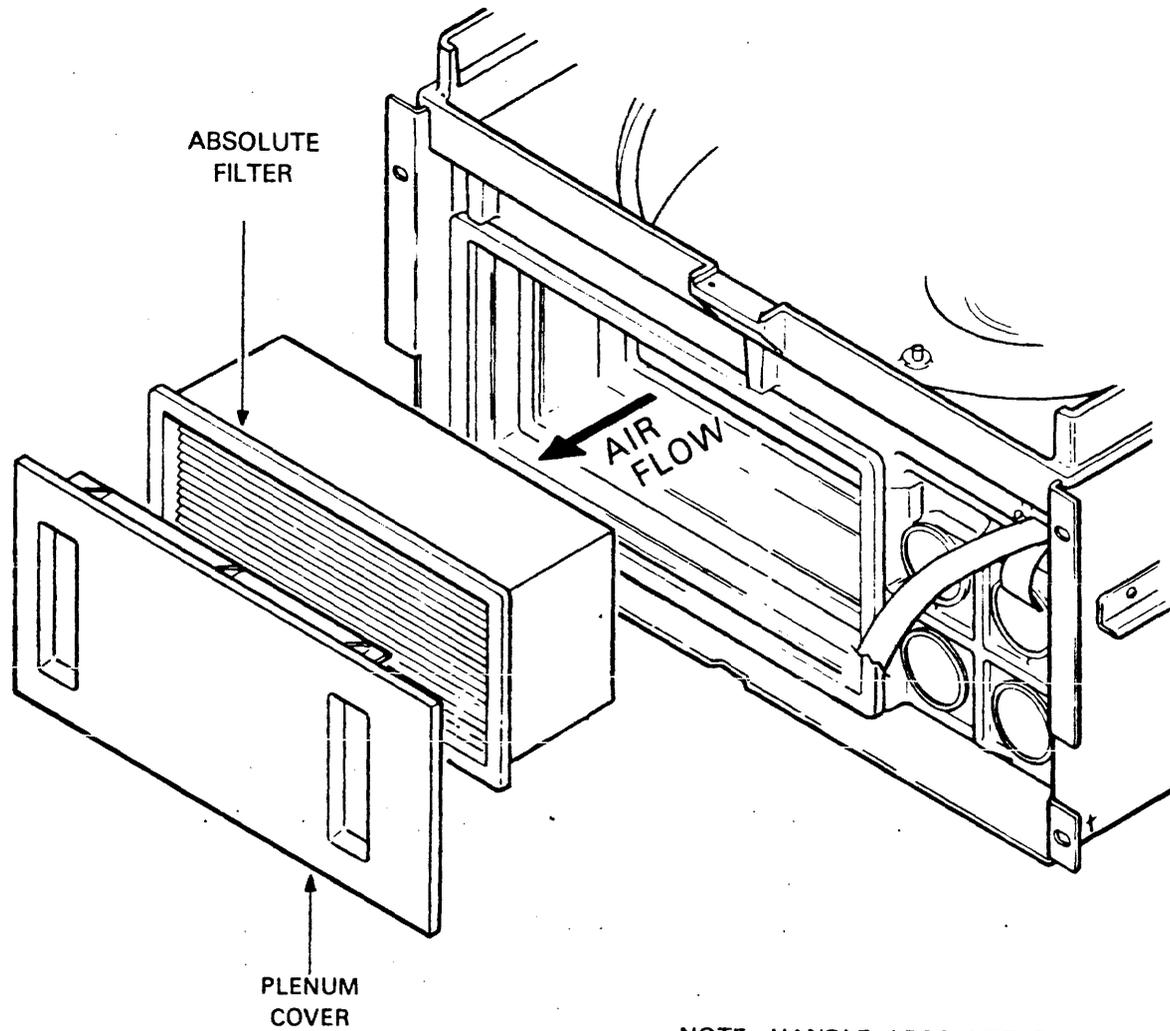
NOTE: HANDLE ABSOLUTE FILTER
BY ITS OUTSIDE HOUSING ONLY

CZ-1059

Figure 2-4   Absolute Filter

To replace the absolute filter:

1. Insert a new absolute filter into the air duct cavity located on the left front side of the drive. Be sure the filter is firmly seated against its gasket. It may be necessary to use a plenum spring to pry the filter into place.

2. Place clear plastic plenum cover over the absolute filter such that the cover seats on the gasket.

3. Install a plenum spring by inserting its bottom tang into the slot provided and rotating the spring such that it fits inside the plenum spring latch bracket (Figure 2-3).

4. While pressing the plenum spring firmly against the plenum cover, insert the plenum latch by squeezing the latch and placing the latch into the holes of the plenum latch bracket. See Figure 2-3.

5. Push the plenum latch into the "locked" position.

6. Repeat the process for the other plenum spring and latch.

7. Replace the front bezel (Paragraph 2.2.1).

2.2.4 Front Panel Board

To remove the front panel board:

1. Remove the front bezel (Paragraph 2.2.1).

2. Locate the screws holding the front panel board to the front bezel (Figure 2-5) and remove them.

To replace the front panel board:

1. Secure the front panel board to the front bezel (Figure 2-5).

2. Replace the front bezel (Paragraph 2.2.1).

2.2.5 Slide Rails

To remove the slide rails:

1. Turn CB1 off (rear panel) and extend the drive to its second set of stops by releasing the slide extension release catches on both slides. See Figure 2-6. Remove the I/O cables and unplug the ac line cord.

2. Locate and remove the two screws securing the drive to each slide as shown in Figure 2-6 (detail).
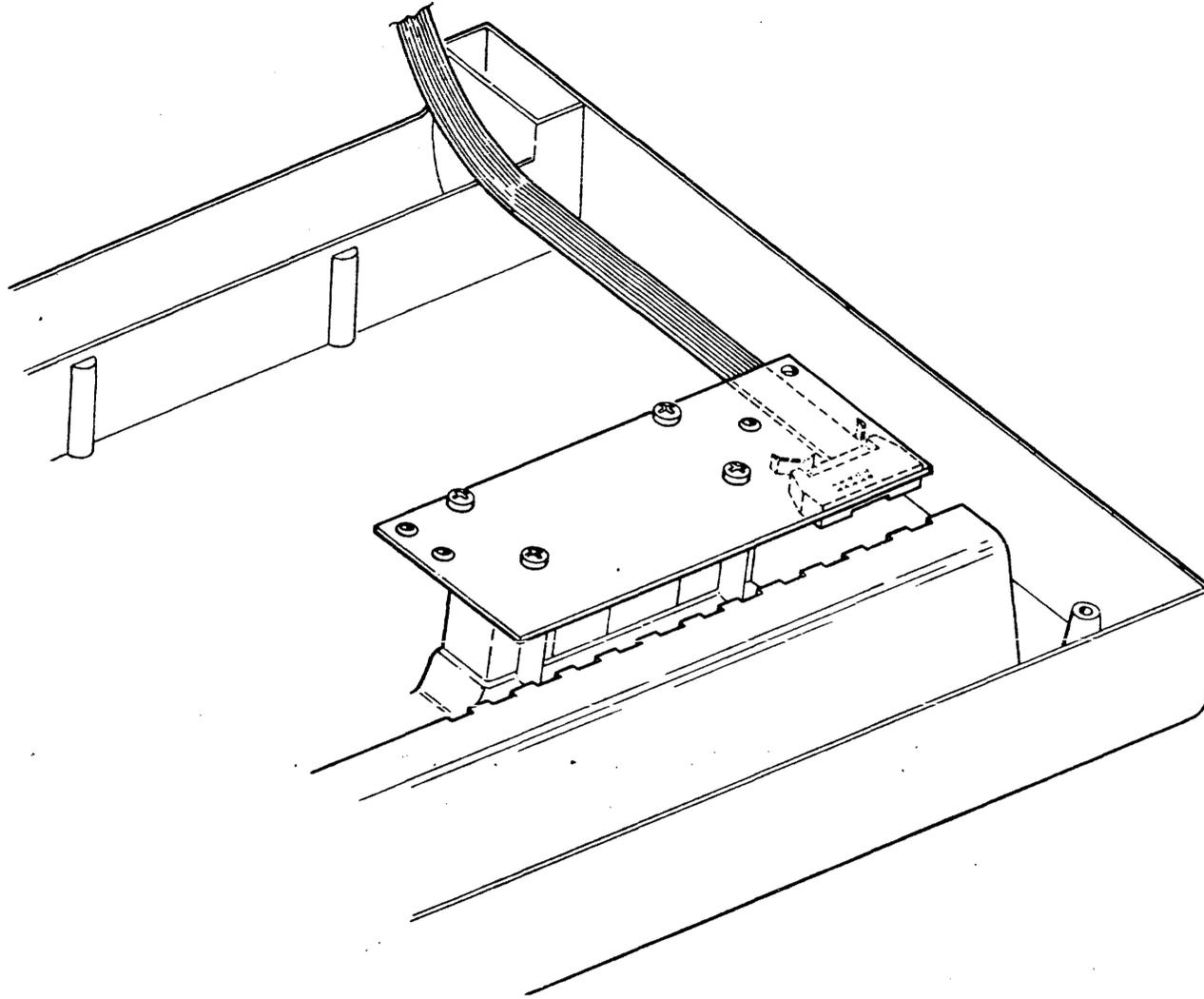
CZ-0008

Figure 2-5   Front Panel Printed Circuit Board

LOCKING LATCH

ACCESS SLOT

SLIDE EXTENSION
RELEASE CATCH

SLIDE
RAILS

SLIDES

SEE
DETAIL
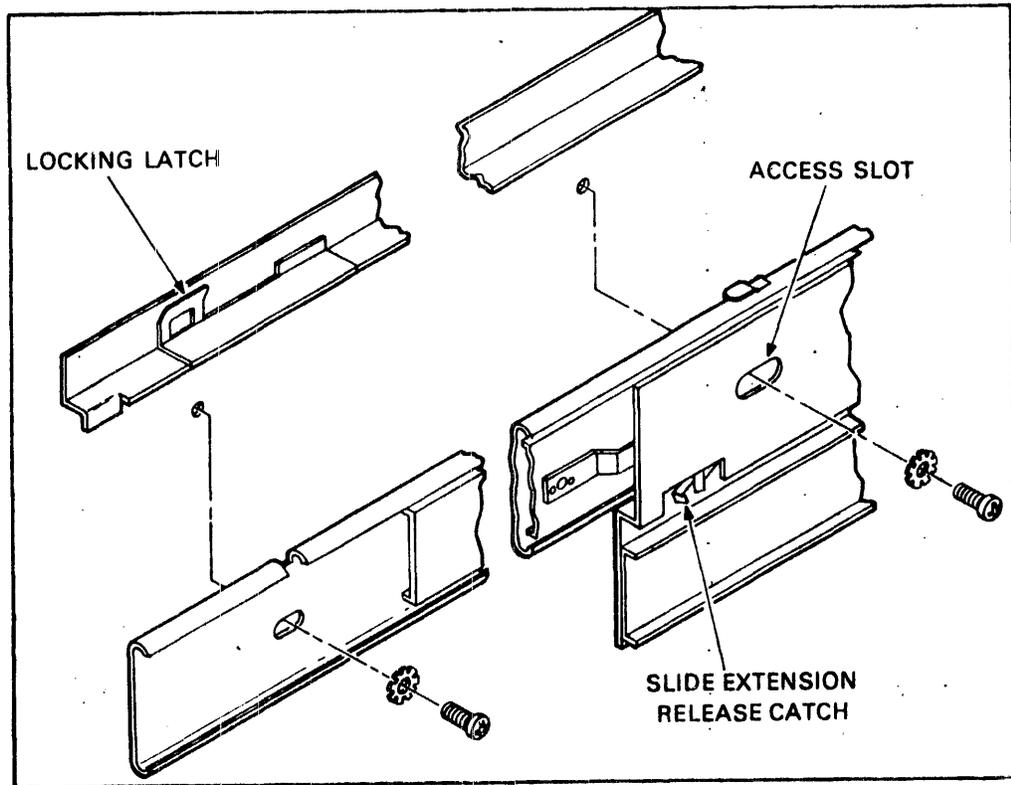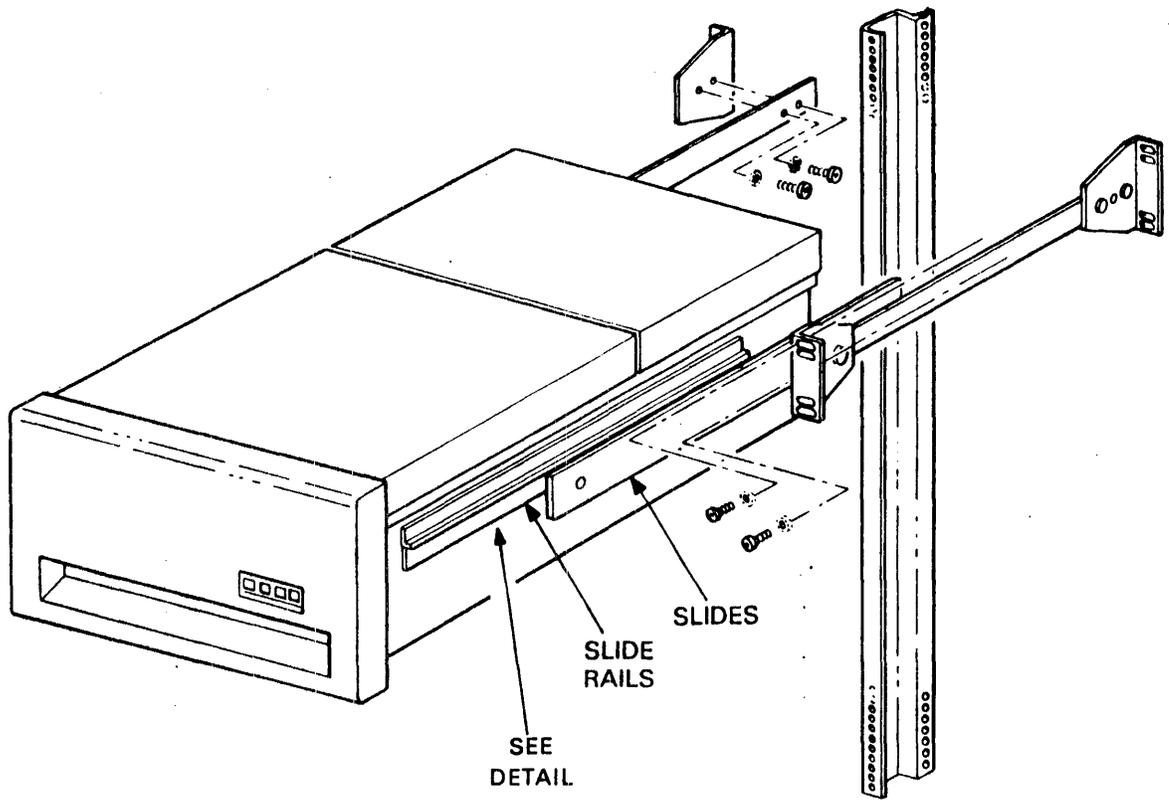
CZ-0009

Figure 2-6   Slide Rails

3. Locate the locking latch on each drive rail. (See Figure 2-6.) Actuate them by pulling each latch away from the drive and lifting at the same time to remove the drive from the slides.

WARNING
The drive weighs 34 kg (75 lb). Use care when lifting the drive.

4. The slide rails may now be removed easily by removing the four screws on either side that hold the rails in place.

To replace the slide rails:

1. Secure the slide rails to the side of the drive, using four screws on each rail.

2. Extend both slides fully and place the drive onto the slides. Ensure the locking latch engages on each side (Figure 2-6).

3. Secure the front slide screws first, then adjust the slide position to gain access to the rear screws. See Figure 2-6.

4. Push the drive into the cabinet and reconnect the ac line cord and I/O cables. Turn CB1 back on.

2.3 ACCESS COVERS

2.3.1 Field Service Access Cover

To open the Field Service Access Cover:

1. Turn CB1 off (rear panel) and extend the drive from the cabinet.

2. Locate and remove the captive screws in the cover as shown in Figure 2-7.

3. Lift the cover up slightly and rotate backward. Rest the cover on the rear flange of the baseplate, using the holding bracket (Figure 2-7).

To remove the Field Service Access Cover:

1. Remove all cables connected to the Drive Logic Module (Figure 2-8) noting the orientation of the colored stripe on each cable.

2. Lift cover off the holding bracket and set aside.

CARTRIDGE ACCESS COVER
FIELD SERVICE ACCESS COVER

F. S. COVER

HOLDING
BRACKET

CAPTIVE
SCREWS

CARTRIDGE
COVER

COVER
LATCH

LATCH
MECHANISM

LATCH
SOLENOID
COVER
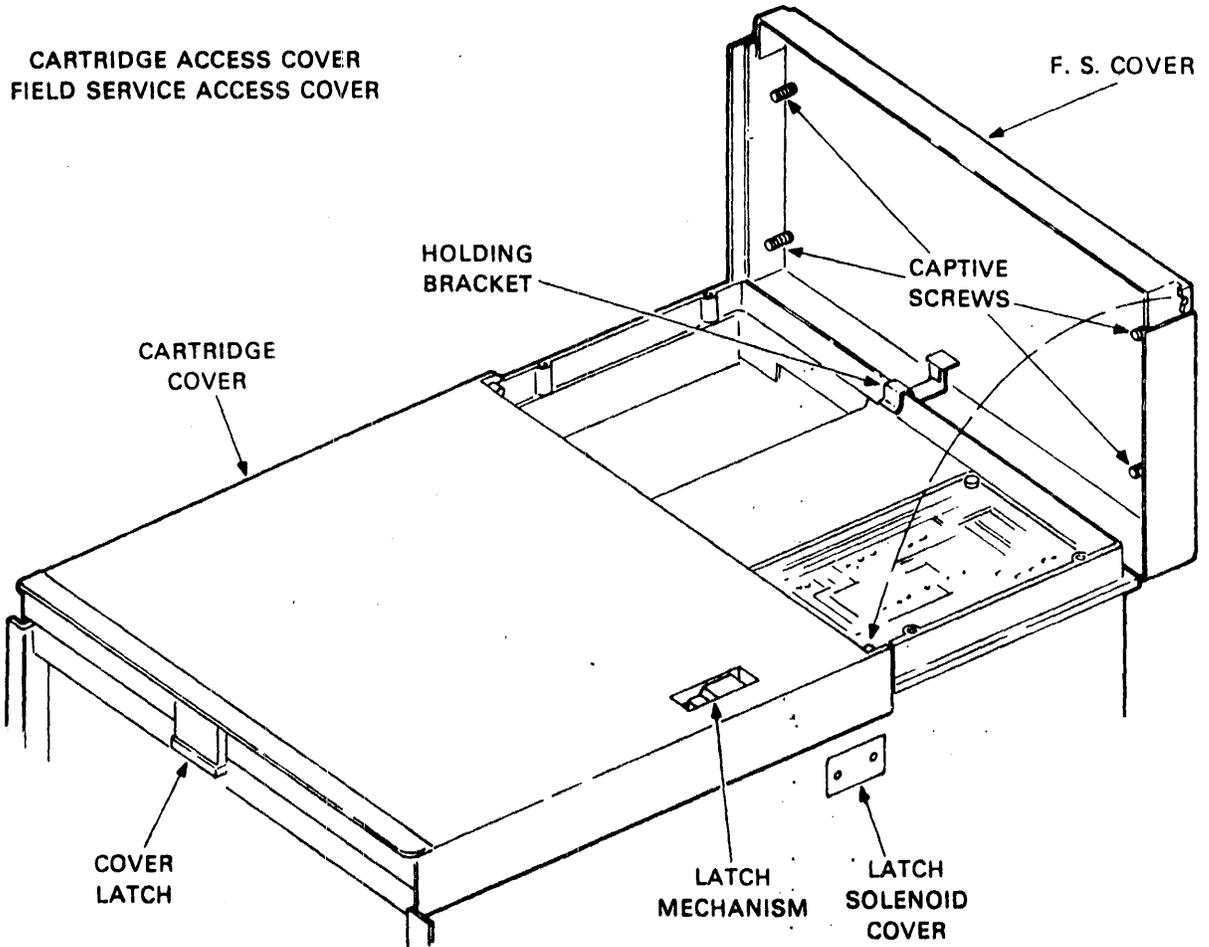
CZ-0010

Figure 2-7   Field Service Access Cover

DRIVE LOGIC
MODULE

A.C.
SERVO MODULE

R/W
MODULE

D.C. SERVO MODULE
AND TEMPLATE
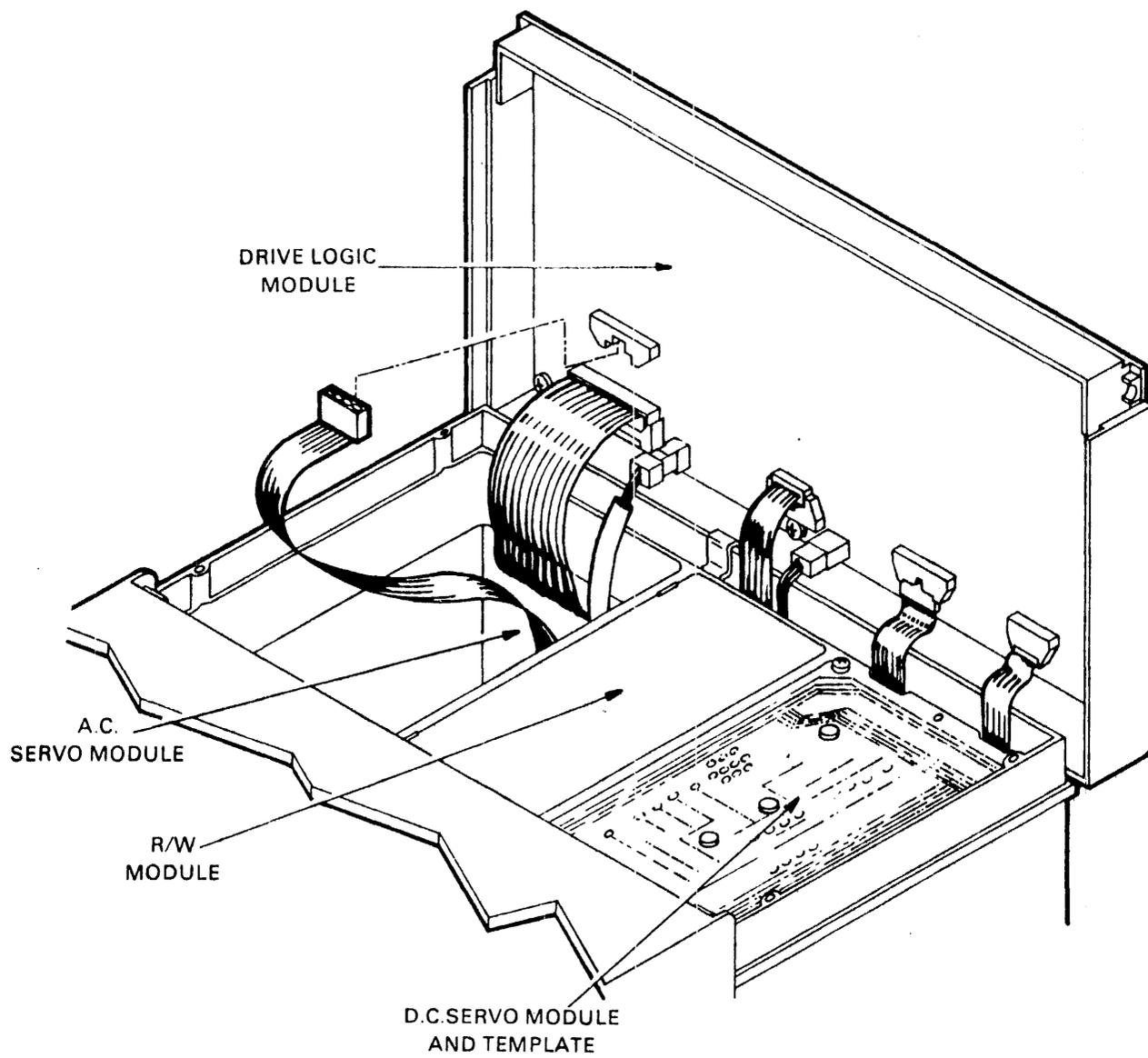
CZ-0011

Figure 2-8   Module Location

To replace the Field Service Access Cover:

1. Place the cover on the rear flange of the baseplate (Figure 2-7).

2. Reconnect all cables to the Drive Logic Module.

3. Lift the cover slightly, rotate it forward and place it into position. The Cartridge Access Cover is held in place by the front edge of the Field Service Access Cover.

4. Tighten the captive screws.

5. Turn CB1 on and slide the drive back into the cabinet.

2.3.2 Cartridge Access Cover

To remove the Cartridge Access Cover:

1. Open the Field Service Access Cover (Paragraph 2.3.1).

2. Lift the rear part of the Cartridge Access Cover approximately two inches.

3. Push backwards on the cover latch mechanism. The cover will pop up in front.

4. Lift cover straight up off the baseplate. The spring-loaded cover arms will snap to the rearward position.

To replace the Cartridge Access Cover:

1. Pull the spring-loaded cover arms forward so that they are parallel to the cover.

2. Guide the cover arms in the rollers provided on the casting.

3. Position the cover over the drive baseplate and lower the front edge until it engages the latch at the top front lip of the drive baseplate.

4. Lower rear edge to the baseplate.

5. Close the Field Service Access Cover (Paragraph 2.3.1).

2.4 BRUSH AREA

2.4.1 Brush Drive

To remove the brush drive:

1. Remove the Field Service Access Cover (Paragraph 2.3.1).

2. Remove the Cartridge Access Cover (Paragraph 2.3.2).

3. Locate the DC Servo Module (see Figure 2-8 for location).

4. Remove the four screws securing the plastic template and module to the baseplate.

5. Lift the module straight up and place it in the baseplate slots (Figure 2-9).

6. Locate the brush motor assembly (see Figure 2-10) and remove the Phillips head screws located at the three corners of the assembly.

7. Detach the keyed cable connector (Figure 2-9).

8. Lift the brush motor assembly straight up.

To replace the brush drive:

1. Place the brush motor assembly over its mounting surface and plug in the keyed cable connector.

2. Insert the brush motor assembly into cavity and secure with three Phillips head screws.

3. Replace the DC Servo Module.

4. Replace the Cartridge Access Cover (Paragraph 2.3.2).

5. Replace the Field Service Access Cover (Paragraph 2.3.1).

2.4.2 Brush Tips

The brush tips and brush holder arms are replaced as one unit. To remove the arms (and tips):

1. Remove the brush drive assembly (Paragraph 2.4.2).

2. Invert brush motor assembly and place on work surface. Remove retaining ring and flatwasher (Figure 2-11).

3. Carefully lift on brush drive link assembly at end connecting brush holder assembly, then pivot link assembly out of the way.

CAUTION
Too much force may break the plastic locating dowels.

4. Slide brush holder off mounting shaft.

BRUSH MOTOR DRIVE
CABLE CONNECTOR

*NOTE:
LOCATION OF CONNECTOR
IS IN THE CAVITY UNDER
THE D.C. SERVO MODULE.

DC SERVO MODULE

DC SERVO
HOLDING
SLOT

DC SERVO
HOLDING
SLOT

CZ-1063

Figure 2-9   DC Servo Module

BRUSH MOTOR
ASSEMBLY

SPINDLE ASSEMBLY

SECTOR TRANSDUCER ASSEMBLY
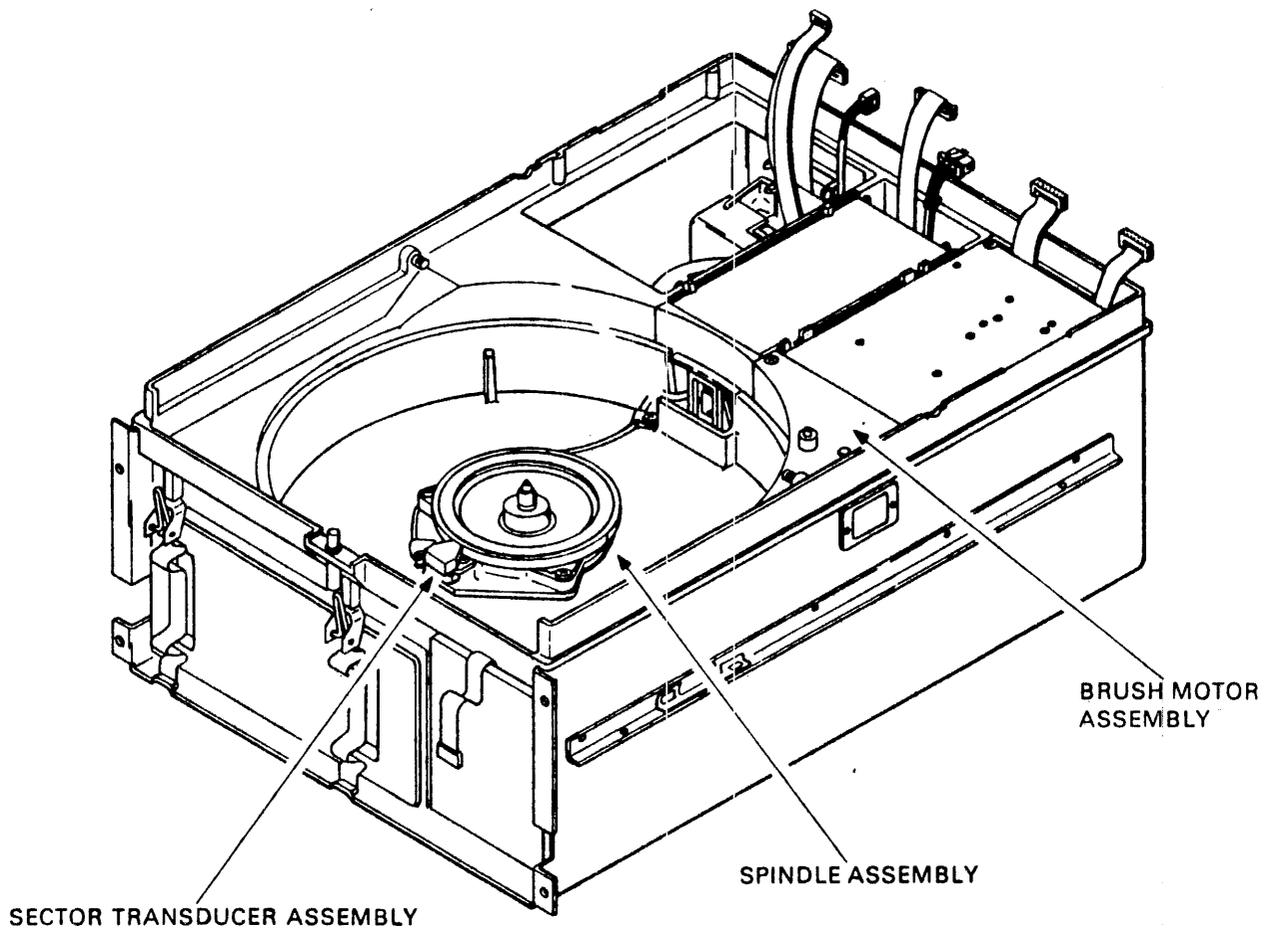
CZ-0012

Figure 2-10   Exposed Drive Baseplate

BRUSH HOLDER ASSY

BRUSH TIPS

FLATWASHER 2 PLACES

RETAINING RING

FLAT WASHER

RETAINING RING

BRUSH ARM ASSY

FLAT WASHER

BRUSH DRIVE LINK ASSEMBLY
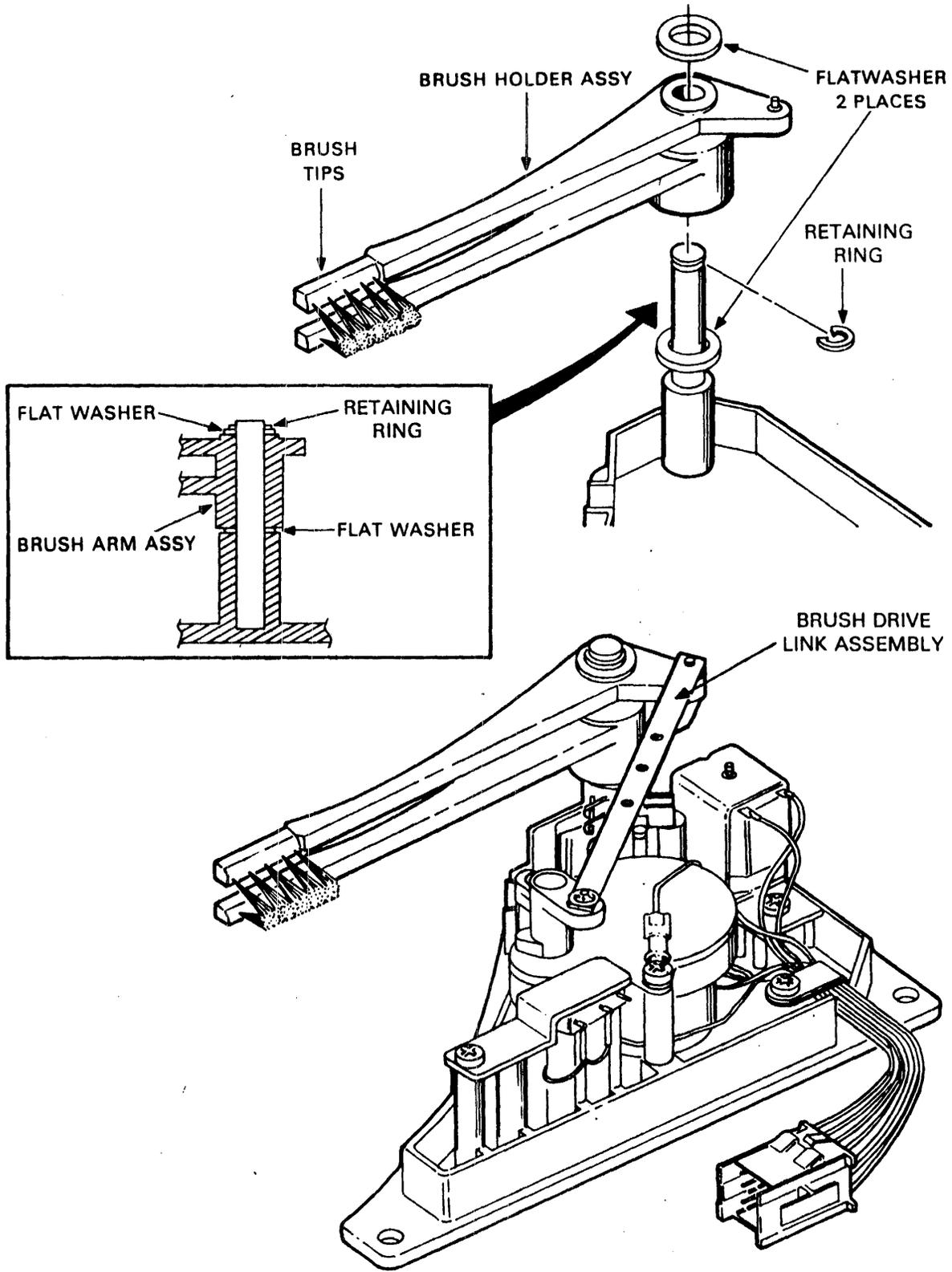
CZ-0013

Figure 2-11 Exposed Brush Drive Assembly

To replace the brush arms (and tips):

1. Slide new brush holder arms onto mounting shaft (Figure 2-11).

2. Install flatwasher and retaining ring as shown in Figure 2-11.

3. Replace brush drive link assembly onto brush holder dowel as shown in Figure 2-11.

4. Replace the brush drive (Paragraph 2.4.1).

2.5 MODULES

2.5.1 AC Servo Module

To remove the AC Servo Module:

1. Unplug the ac power cord.

2. Open the Field Service Access Cover (Paragraph 2.3.1).

3. Locate the AC Servo Module (Figure 2-8). Remove the cover (Figure 2-12) and disconnect all the cables.

NOTE
The cover holddown tabs may have to be bent out of the way in order to lift the module cover.

4. Unplug all the cables and lift the module out of the drive.

To replace the AC Servo Module:

1. Slide the module into place.

2. Connect all the cables and replace the cover.

3. Replace the Field Service Access Cover (Paragraph 2.3.1).

4. Replace the ac power cord.

2.5.2 DC Servo Module

To remove the DC Servo Module:

1. Unplug the ac power cord.

2. Open the Field Service Access Cover (Paragraph 2.3.1).

3. Locate the DC Servo Module (Figure 2-8).

AC SERVO
MODULE
COVER

AC SERVO
MODULE

COVER
HOLDDOWN TABS
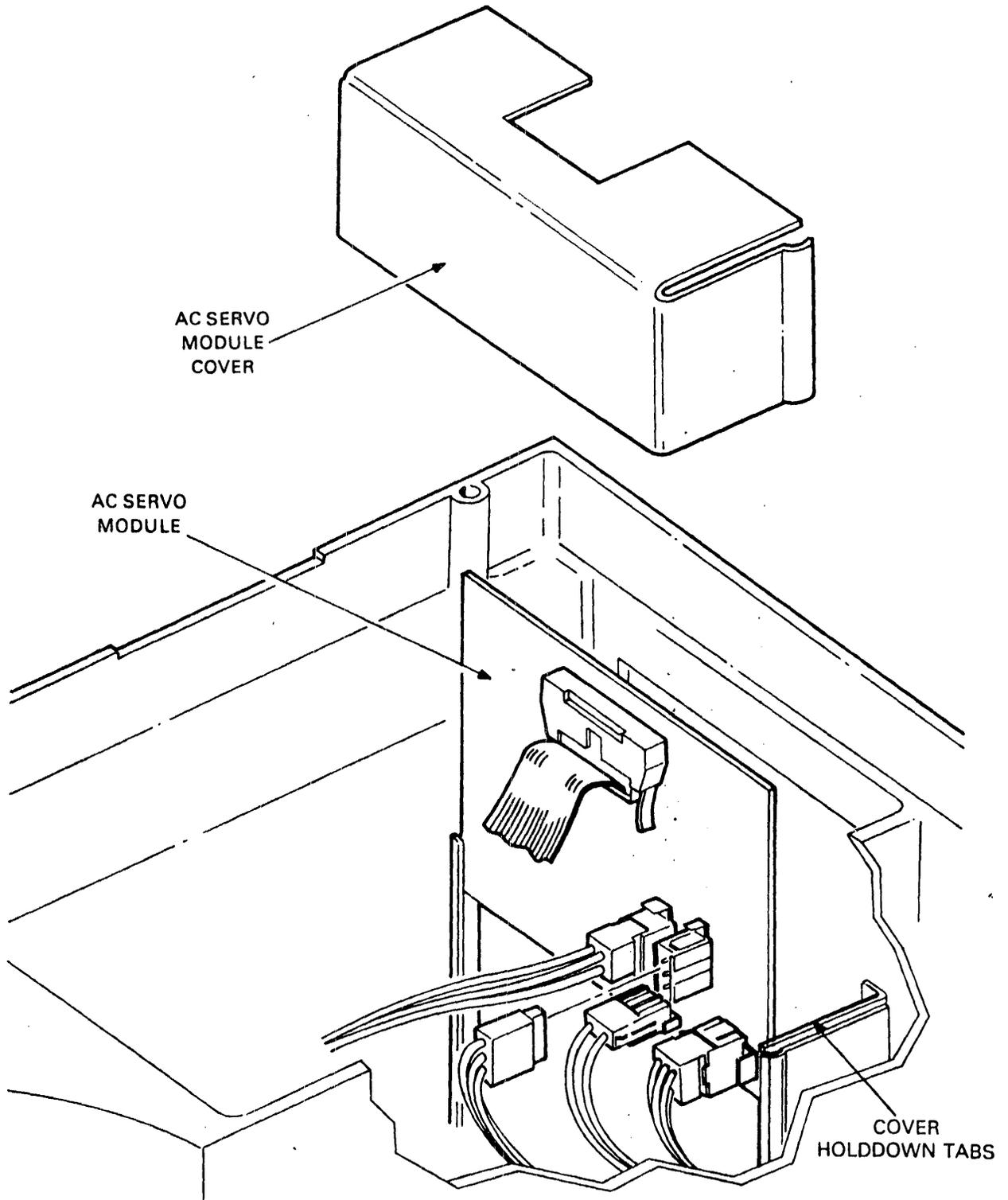
CZ-0014

Figure 2-12   AC Servo Module

4. Remove the four screws securing the plastic template and module to the baseplate.

5. Lift the module and disconnect all the cables.

To replace the DC Servo Module:

1. Connect all cables to the module.

2. Place the module back into the baseplate.

3. Lay the plastic template into positon on top of the module and secure it with the four screws.

NOTE
If the DC Servo Module being replaced is the "old" module (Part No. 54-11850), use the "old" template (Part No. 74-18588). If the module being replaced is a "new" module (Part No. 54-13536), it must be covered with a different template (Part No. 70-29826).

4. Replace the Field Service Access Cover (Paragraph 2.3.1).

5. Replace the ac power cord.

2.5.3 Drive Logic Module

To remove the Drive Logic Module:

1. Open the Field Service Access Cover (Paragraph 2.3.1).

2. Remove all cables connected to the Drive Logic Module (Figure 2-8). Be sure to note the orientation of the stripe on each cable.

3. Remove the Phillips head screws holding the module to the cover, and lift out the module.

To replace the Drive Logic Module:

1. Replace the module inside the Field Service Access Cover and secure the module with the Phillips head screws.

2. Reconnect the cables to the module.

3. Close the Field Service Access Cover (Paragraph 2.3.1).

2.5.4 Read/Write Module

To remove the Read/Write Module:

1. Remove the disk cartridge (if one is in place).

NOTE

The Read/Write "Assembly" consists of
the Read/Write Module and several parts
surrounding the module. Only the module
itself should be replaced. If the
module is ordered by Part No. 54-11844
(RLØ1) or Part No. 54-13536 (RLØ1 or
RLØ2), the assembly will <u>not</u> come with
it.

2.   Remove the Field Service Access Cover (Paragraph 2.3.1)

3.   Remove the Cartridge Access Cover (Paragraph 2.3.2).

4.   Locate the Read/Write Module assembly (Figure 2-8).

5.   Lift the assembly up, rotate it toward the DC Servo
     Module and rest it on the baseplate locating pins (Figure
     2-13).

6.   Disconnect the R/W head cables from the assembly.

7.   Remove the top cover of the assembly (Figure 2-14) by
     carefully prying back the four plastic locking tabs and
     lifting the cover. This is easily accomplished by prying
     one tab at a time and lifting the cover slightly at each
     corner.

8.   Remove the front piece of the assembly (Figure 2-14).

9.   Remove the module cable.

1Ø. Slide the module out of the pan (Figure 2-14).

To replace the Read/Write Module:

1.   Slide the module into the pan (Figure 2-14).

2.   Reconnect the cable to the Read/Write Module.

3.   Replace the front piece of the assembly.

4.   Replace the top cover of the assembly by pushing down on
     the cover until the four plastic tabs secure the cover.

5.   Reconnect the cables to the assembly (Figure 2-13).

6.   Place the assembly back into the baseplate.

7.   Replace the Cartridge Access Cover (Paragraph 2.3.2).

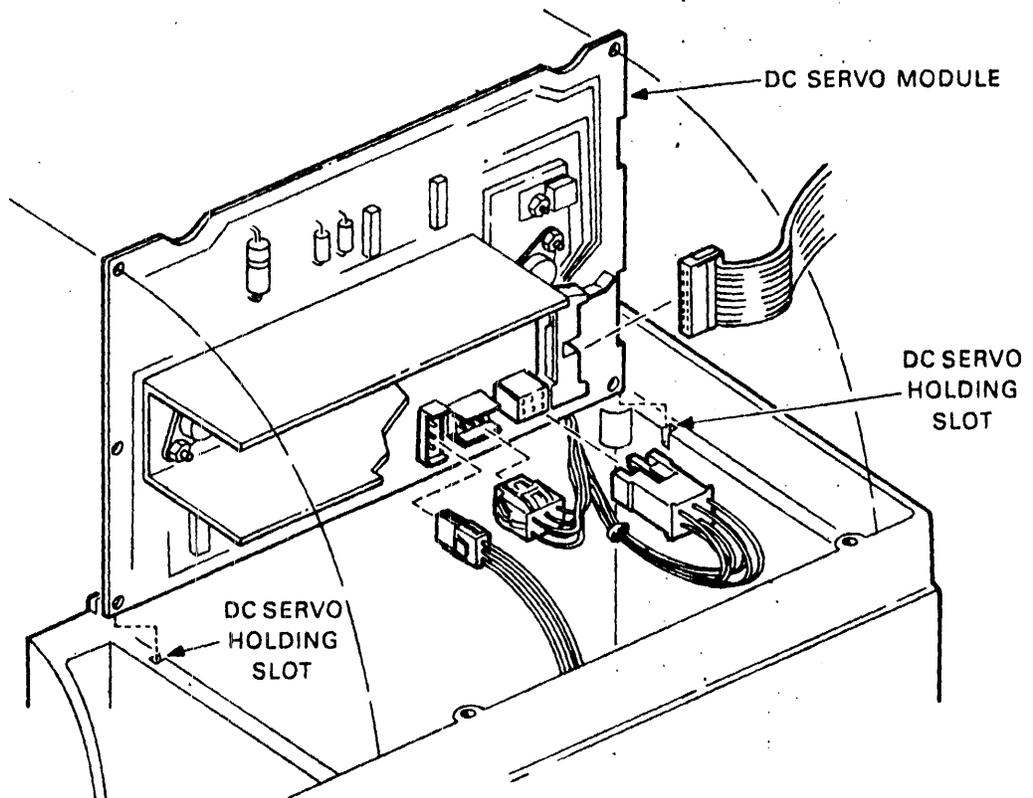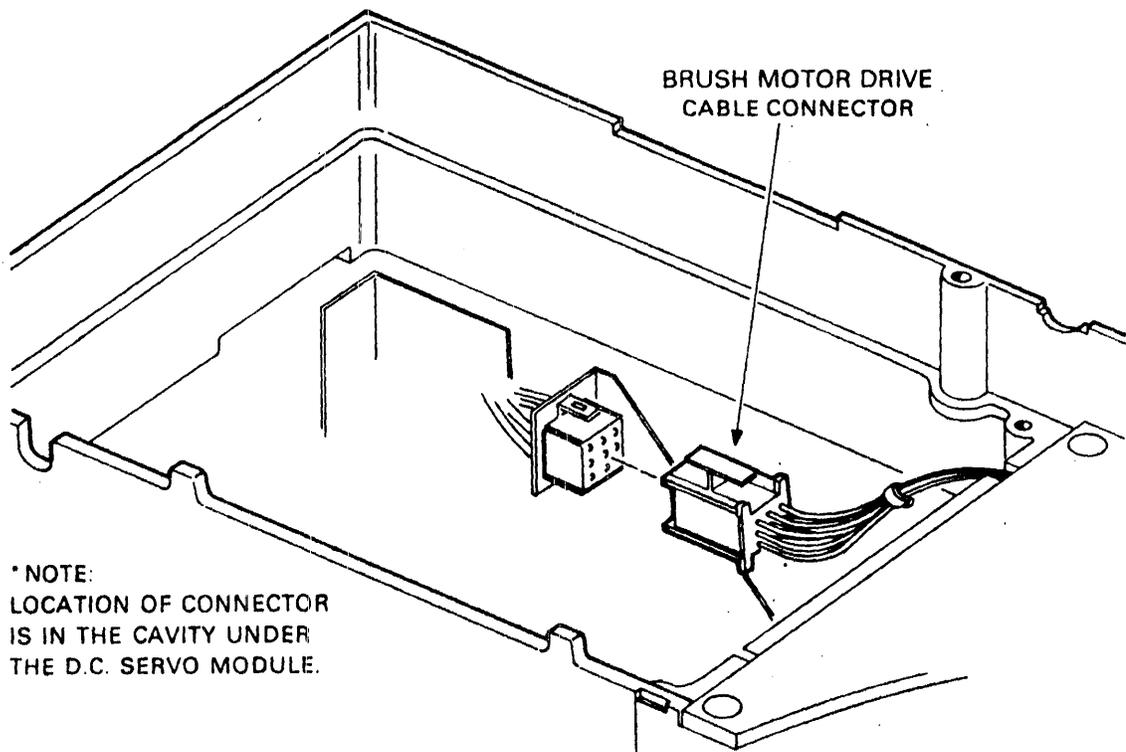8.   Replace the Field Service Access Cover (Paragraph 2.3.1).

PLUG FOR
LOWER HEAD

J3

J2

PLUG FOR
UPPER HEAD

R/W
MODULE

HOLDING
FLANGES

UPPER
HEAD
CABLE

LOWER
HEAD
CABLE

IN-LINE
SERVO
CONNECTOR

POSITIONER
ASSEMBLY
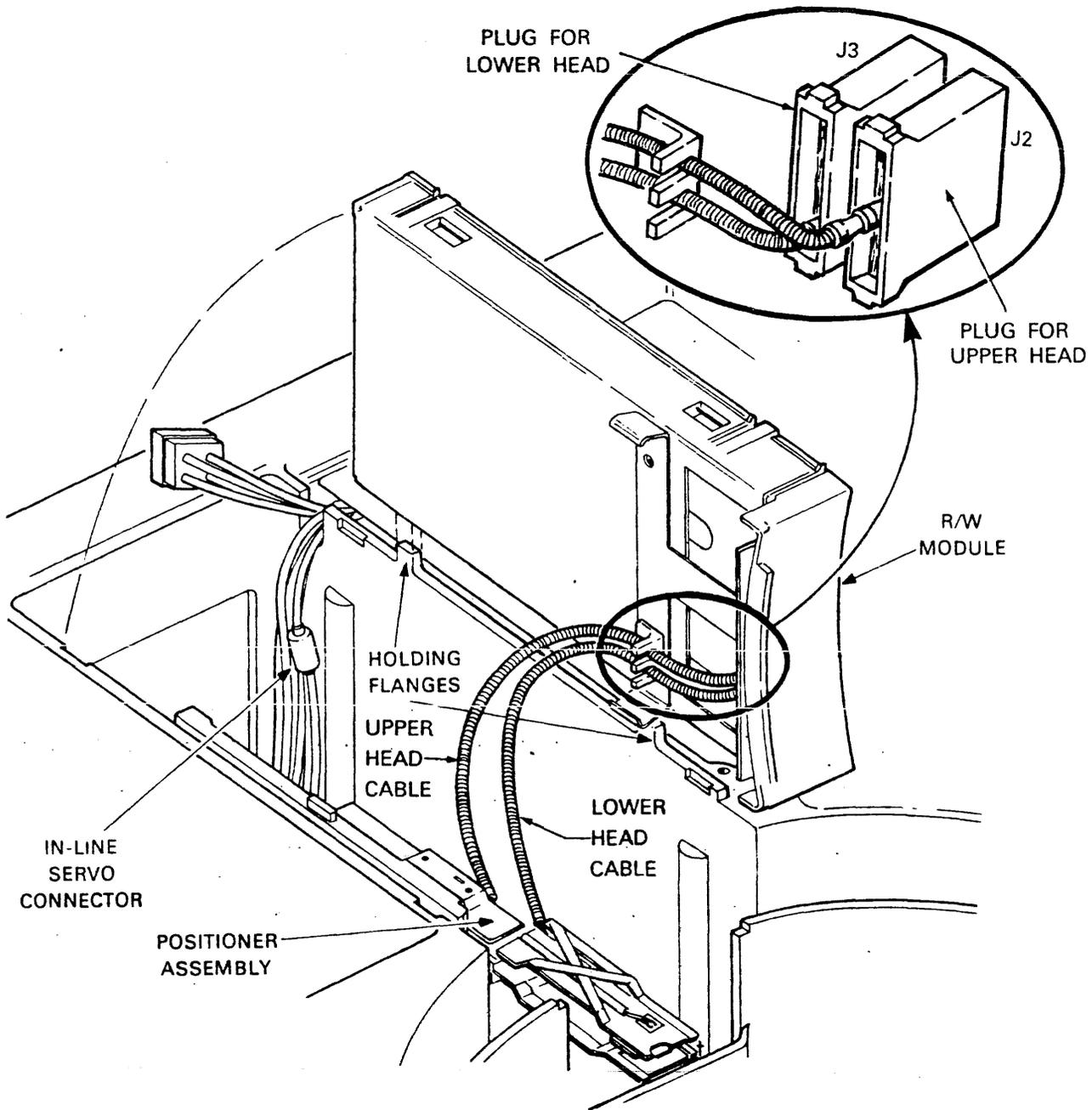
CZ-2054

Figure 2-13   Read/Write Module (Upright)
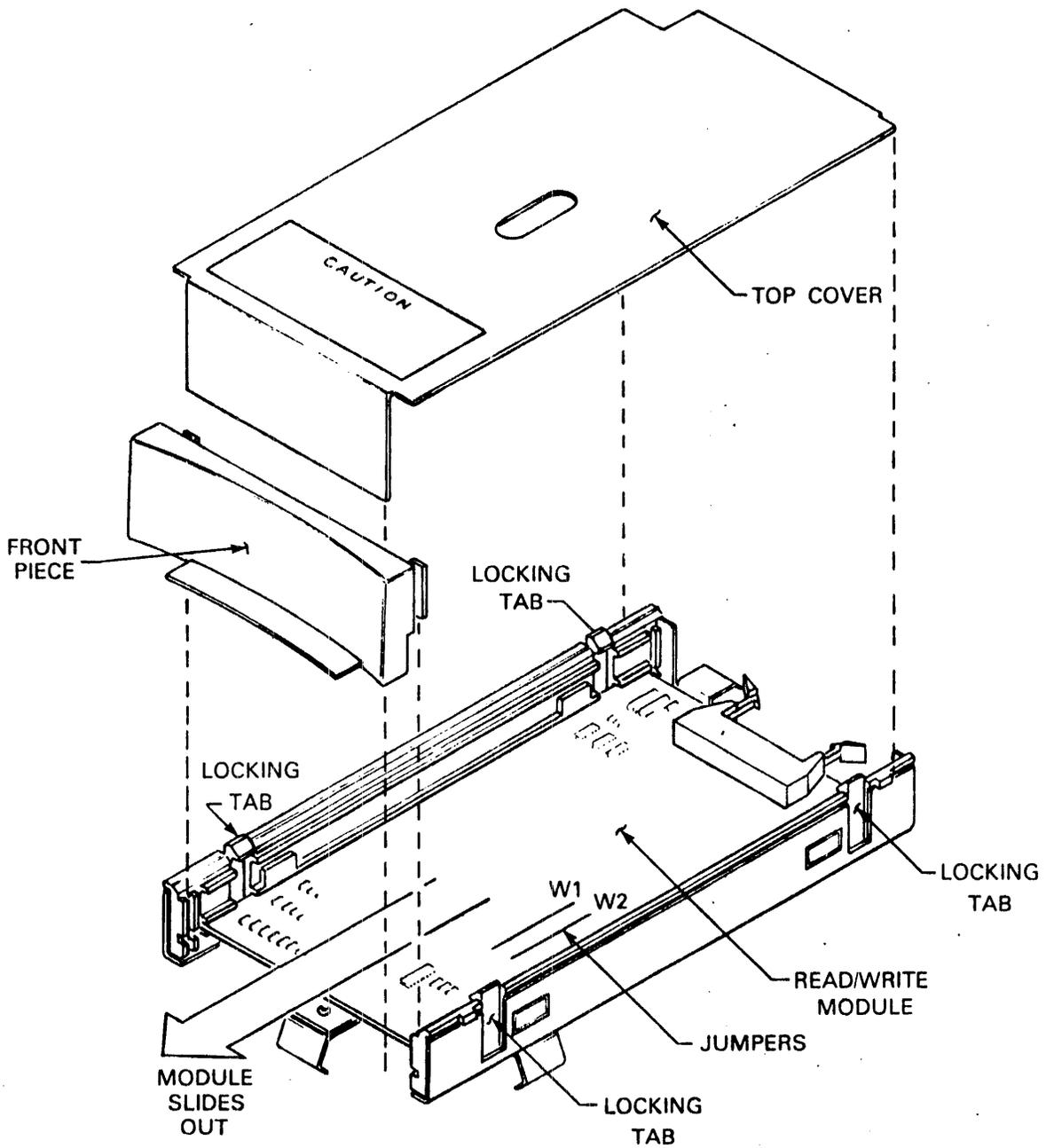
Figure 2-14   Read/Write Module Box Disassembly

2.6 SPINDLE AREA

2.6.1 Belt From Spindle Pulley

To remove the belt from the spindle pulley:

    1.   Remove the Spindle Access Cover (see Figure 2-15).

    2.   Slip belt off the spindle pulley.

To replace the belt on the spindle pulley:

    1.   Slide the drive belt on the pulley and rotate the spindle so that the pulley will drag the belt onto itself.

    2.   Replace the Spindle Access Cover.

2.6.2 Spindle Ground Button

To remove the spindle ground button:

    1.   Remove the Spindle Access Cover (see Figure 2-15).

    2.   Using Figure 2-16 as a guide, pull down on the ground brush strap enough to allow the ground brush to drop.

To replace the spindle ground button:

    1.   Pull down on the ground brush spring just enough to insert the ground brush (Figure 2-16).

    2.   Rotate the spindle several times to ensure firm seating and to check that the spindle does not bind.

    3.   Replace the Spindle Access Cover (see Figure 2-15).

2.6.3 Spindle

To remove the spindle:

    1.   Remove the Field Service Access Cover (Paragraph 2.3.1).

    2.   Remove the Cartridge Access Cover (Paragraph 2.3.2).

    3.   Remove the belt from the spindle pulley (Paragraph 2.6.1).

    4.   Remove the two screws holding the sector transducer to the spindle (Figure 2-17).

    5.   Remove the cable clamp (one screw) holding the sector transducer cable to the spindle (Figure 2-17).

    6.   Lift the spindle straight up out of the baseplate.

BOTTOM OF DRIVE

SPINDLE ACCESS COVER
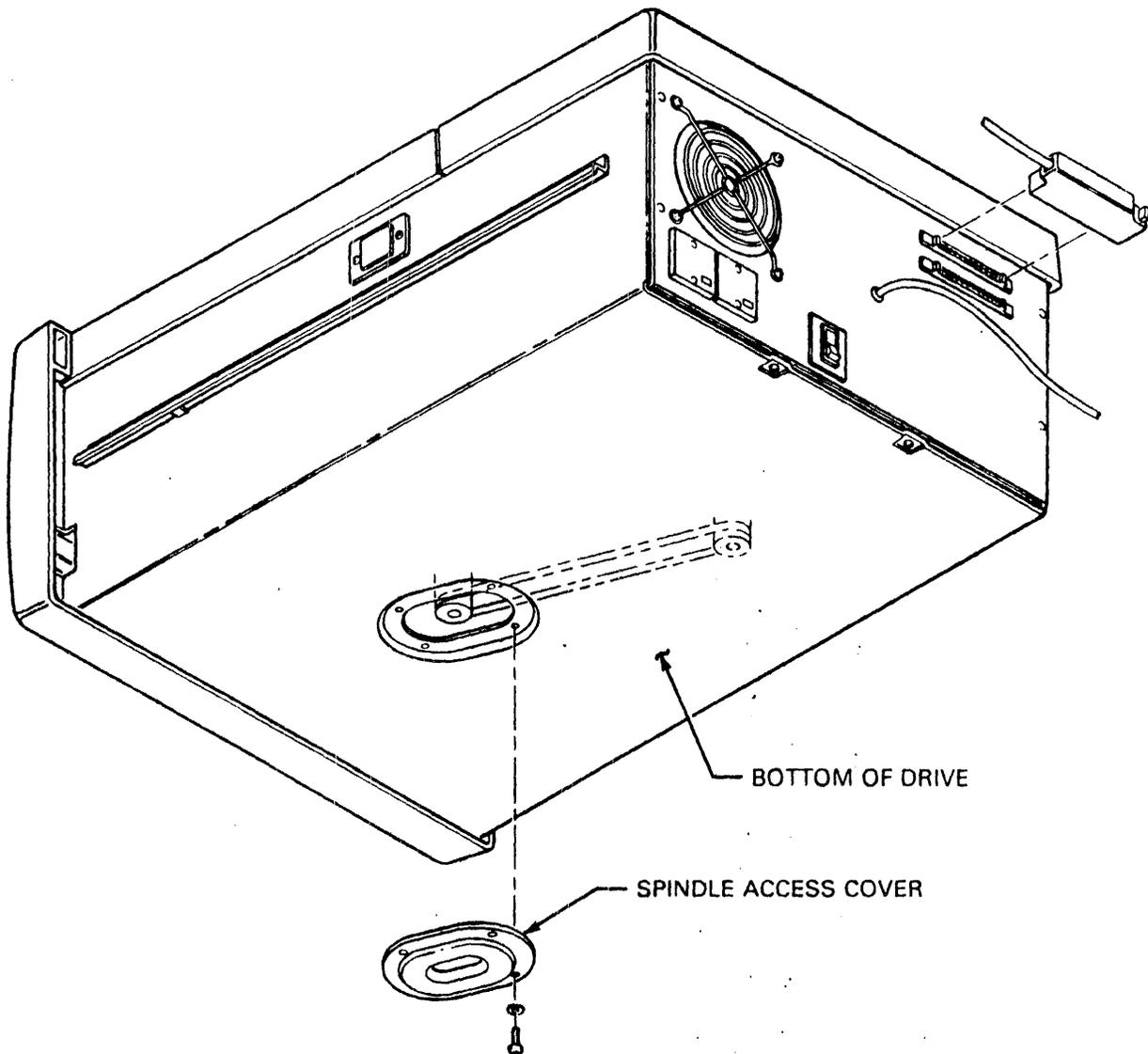
CZ-1060

Figure 2-15   Spindle Access Cover

Figure 2-16   Spindle Ground Button

SCREW

LOCKWASHER

TRANSDUCER

A

B

SCREW

LOCKWASHER

FLATWASHER

CABLE
CLAMP

A

SCREW

LOCKWASHER

GND LUG

LOCKWASHER

B
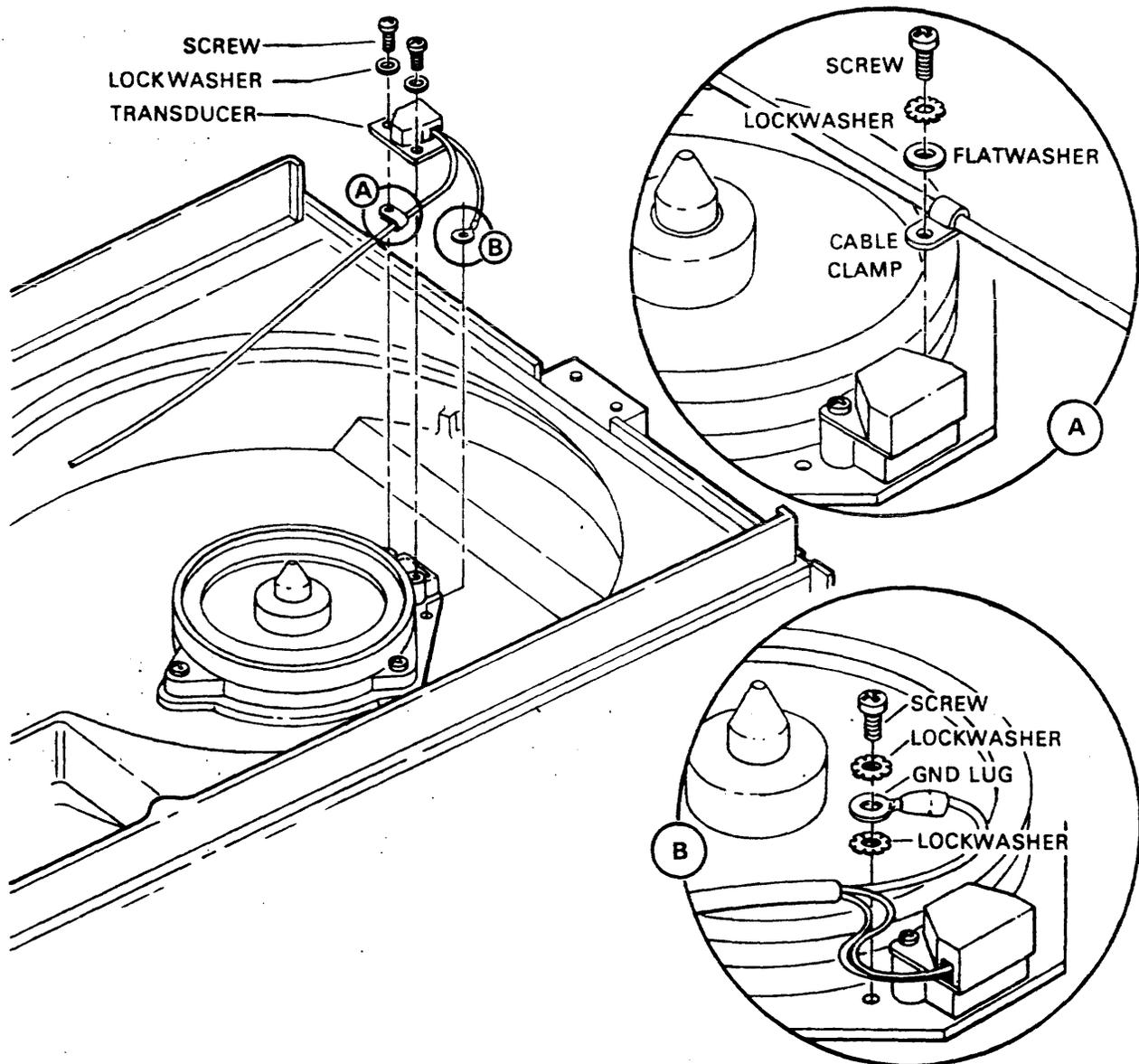
CZ-1061

Figure 2-17   Sector Transducer Mounting

To replace the spindle:

1. Insert the spindle into the baseplate. Position the spindle so that the locating pin fits into the recess in the spindle assembly.

2. Secure the spindle to the baseplate with three Phillips head screws.

3. Replace the belt on the pulley (Paragraph 2.6.1).

4. Replace the Cartridge Access Cover (Paragraph 2.3.2).

5. Replace the Field Service Access Cover (Paragraph 2.3.1).

2.6.4 Sector Transducer

To remove the sector transducer:

1. Remove the Field Service Access Cover (Paragraph 2.2.1).

2. Remove the Cartridge Access Cover (Paragraph 2.3.2).

3. Remove the two screws holding the transducer to the spindle (Figure 2-17).

4. Remove the screw holding the transducer cable clamp to the spindle (Figure 2-17).

5. Remove the screw holding the transducer ground lug to the baseplate.

6. Remove the three other cable clamp screws.

7. Unplug the cable from the Drive Logic Module, noting the orientation of the stripe on the cable.

8. Remove the transducer cable, noting the path of cable routing.

To replace the sector transducer:

1. Route the transducer cable in the drive following the path of removal.

2. Replace the three screws in the cable clamps and reinstall into the baseplate.

3. Replace the screw holding the transducer ground lug to the baseplate (Figure 2-17).

4. Replace the screw holding the transducer cable clamp to the spindle (Figure 2-17).

5.   Replace the two screws holding the transducer to the spindle (Figure 2-17).

6.   Replace the Cartridge Access Cover (Paragraph 2.3.2).

7.   Replace the Field Service Access Cover (Paragraph 2.3.1).

2.7   POSITIONER AREA

2.7.1   Postioner

To remove the positioner:

1.   Remove the Field Service Access Cover (Paragraph 2.3.1).

2.   Remove the Cartridge Access Cover (Paragraph 2.3.2).

3.   Remove the DC Servo Module (Paragraph 2.5.2).

4.   Remove the Read/Write Module assembly (Paragraph 2.5.4, Steps 1 through 5).

5.   Remove the head cables from the module assembly (Figure 2-13).

6.   Remove the six screws holding the positioner to the baseplate (Figure 2-18).

7.   Lift the positioner up and out of the drive area.

NOTE
The Read/Write heads are not part of the postioner assembly. Thus, they will have to be removed from the old positioner and attached to the new one. The head removal and replacement procedure is described in Paragraph 2.7.2.

To replace the positioner:

1.   Place the positioner back into the baseplate of the drive.

NOTE
The postioner is fragile. Do not drop it into place. Lower it gently.

2.   Secure the positioner to the baseplate with the six Phillips-head screws (Figure 2-18).

3.   Replace the head cables into the module assembly (Figure 2-13).

4.   Replace the DC Servo Module (Paragraph 2.5.2).

THESE 2 SCREWS ARE
NEAREST THE MOTOR
SHAFT AND ARE THE LONGEST
OF THE SIX MOUNTING
SCREWS.

HEADS HOME SWITCH
ADJUSTING SCREW

POSITIONER
ADJUSTING
SLOT

POSITIONER
ADJUSTING SLOT

CZ-1079
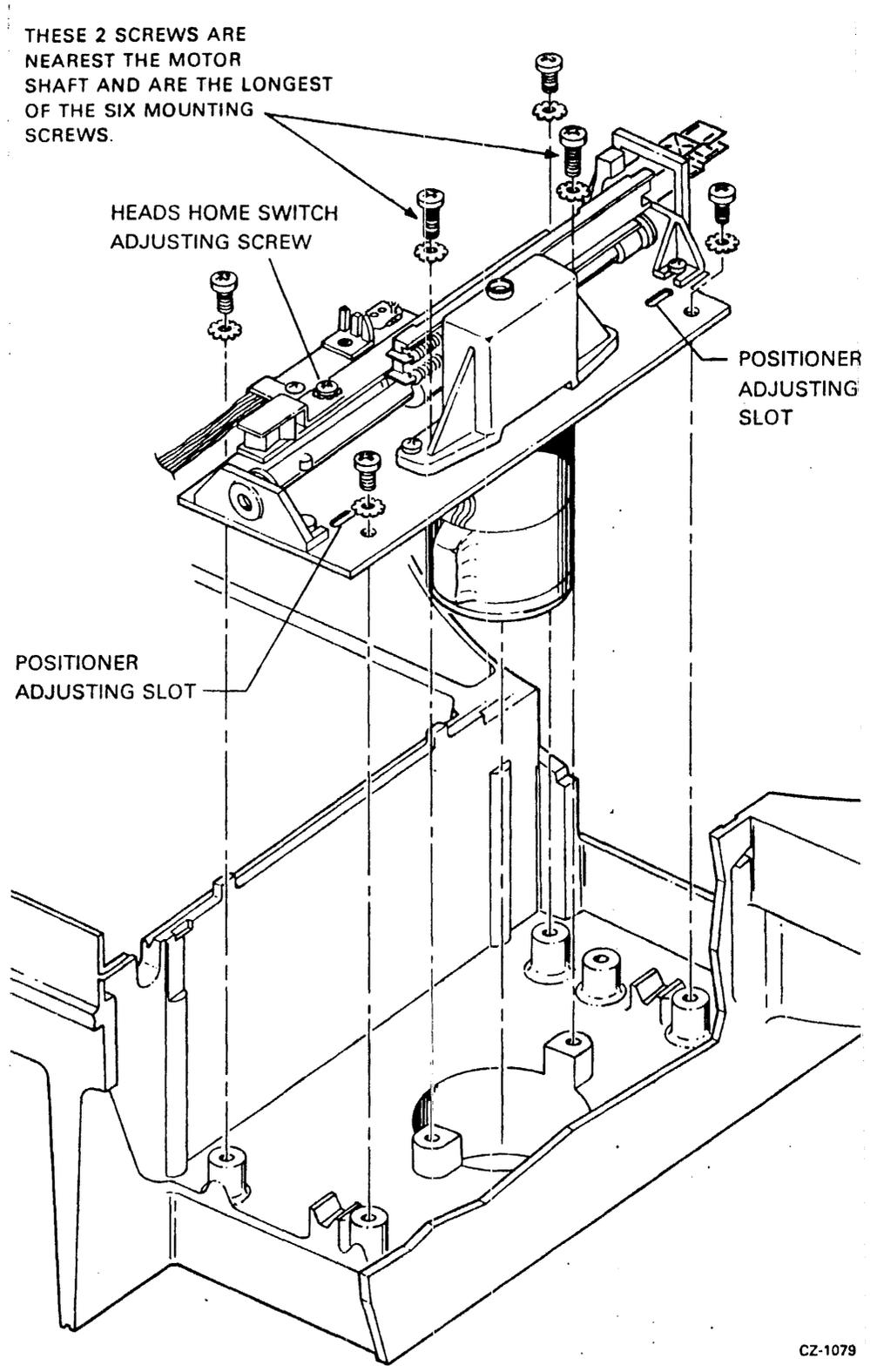
Figure 2-18   Positioner Assembly

5. Replace the Read/Write Module assembly (Paragraph 2.5.4).

6. Replace the Cartridge Access Cover (Paragraph 2.3.2).

7. Replace the Field Service Access Cover (Paragraph 2.3.1).

8. Perform the Positioner Radial Alignment (Chapter 3, Paragraph 3.5).

2.7.2 Read/Write Heads

To remove the Read/Write heads:

1. Remove the Field Service Access Cover (Paragraph 2.3.1).

2. Remove the Cartridge Access Cover (Paragraph 2.3.2).

3. Remove the Read/Write Module assembly (Paragraph 2.5.4).

4. Disconnect the head cables from the module assembly (Figure 2-13).

5. Use a 3/32" Allen wrench to loosen the captive head retaining screw and carefully slide the head forward, out of the positioner assembly (Figure 2-19).
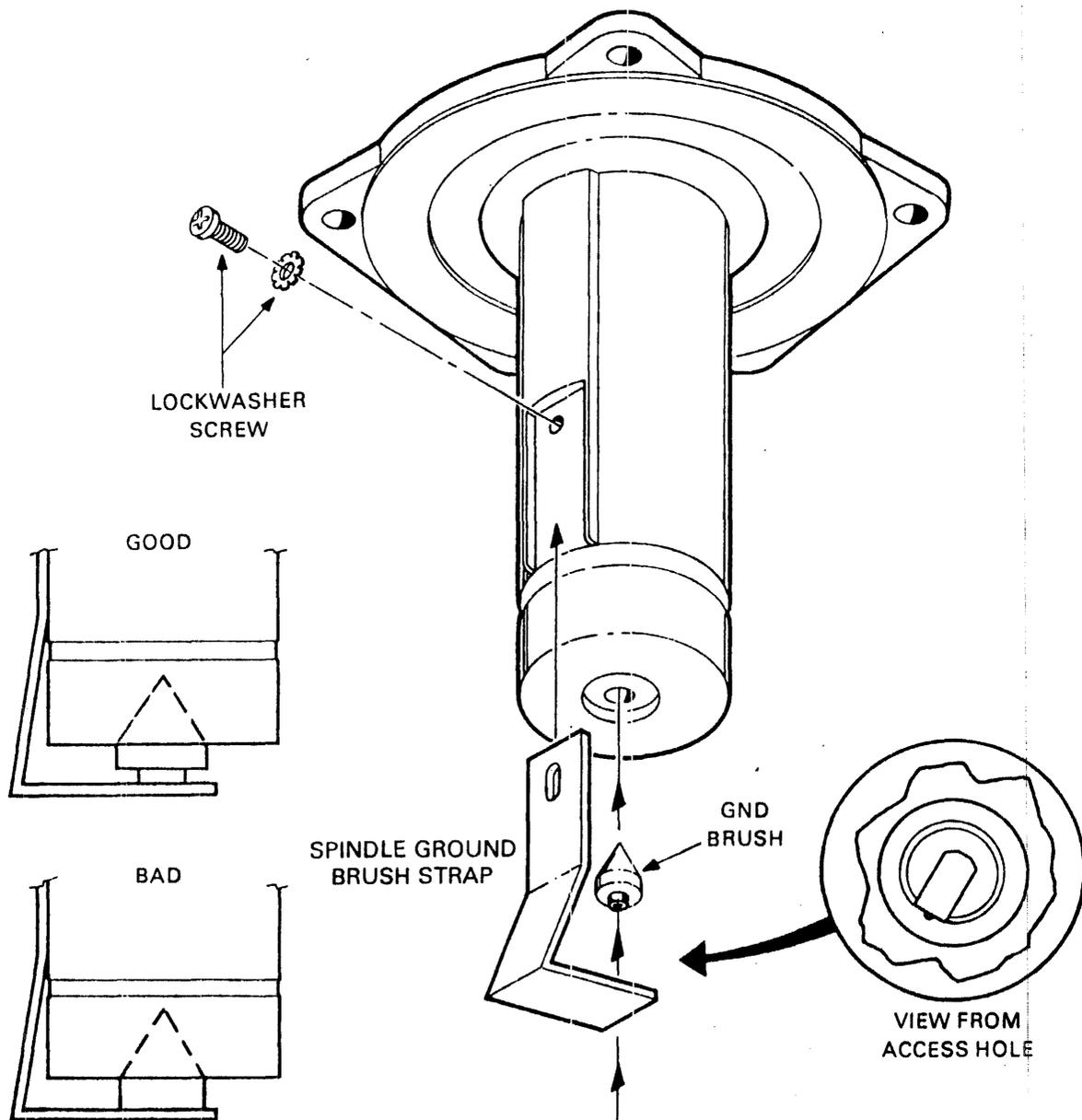
CAUTION
Do not allow the head being removed to bump or drag on the other head during the procedure.

6. Repeat for the other head.

To replace the Read/Write heads:

1. Insert the lower head into the positioner frame such that:

   o The locating pin (Figure 2-19) is in the recess of the tailstack of the head

   o The tailstack fits into the carriage assembly

   o The corner of the head fits into the plastic extension

2. Slide the head to the rear of the drive so that the head is up against the locating pin.

LOWER
HEAD

UPPER
HEAD

PLASTIC
EXTENSION

LOWER HEAD LOCATING PIN

CARRIAGE
ASSEMBLY
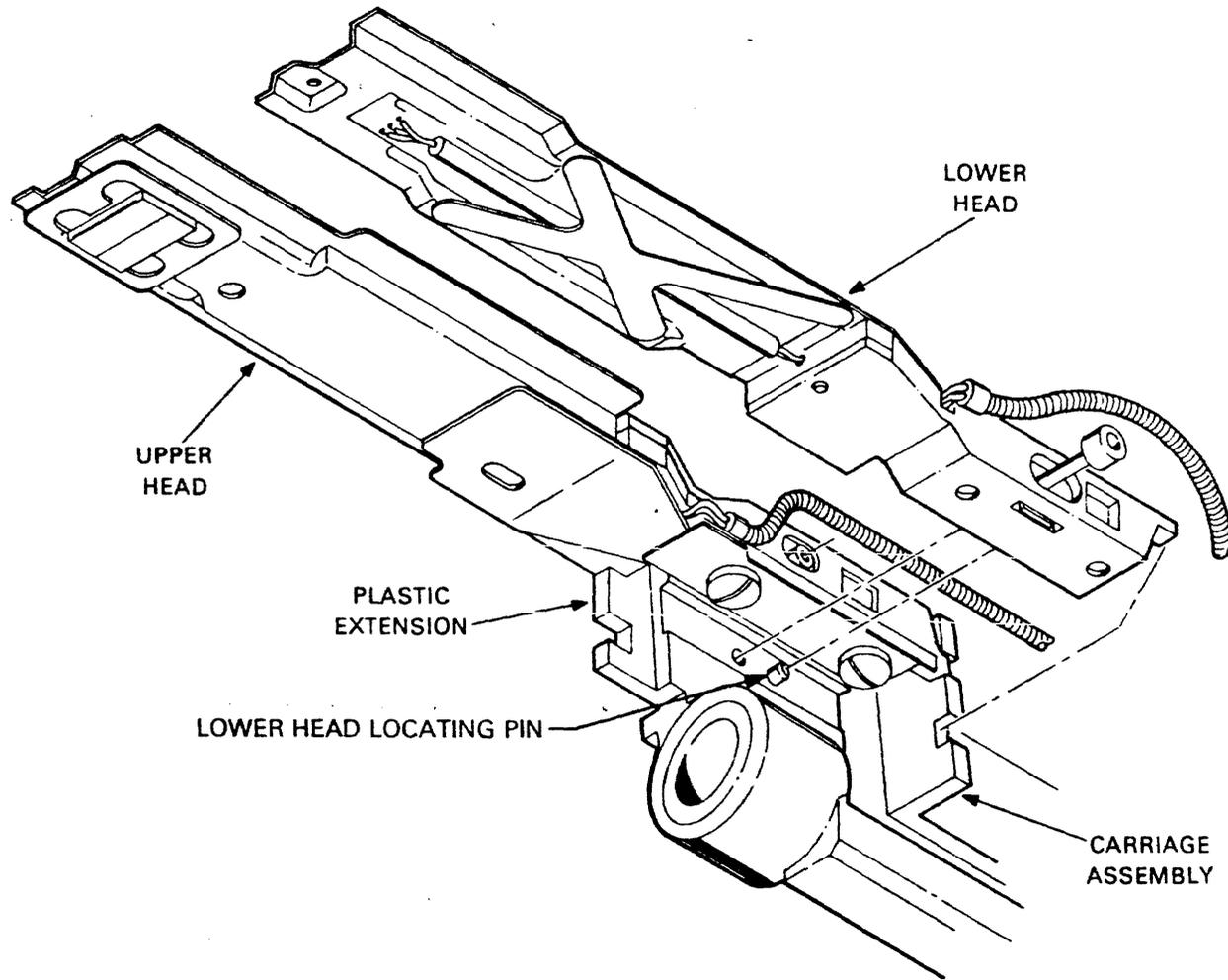
CZ-1003

Figure 2-19. Read/Write Heads

3.	Using the 3/32" Allen wrench, snug the holddown screw to secure the head in place.

CAUTION
The screw is being tightened into an aluminum casting. Do not overtighten this screw and no damage will occur to the threads in the casting.

4.	Insert the upper head into the positioner frame, being careful not to strike the lower head.

5.	Secure with the holddown screw.

6.	Reconnect the head cables into the Read/Write Module connectors (Figure 2-13). The lower head cable (J3) is inserted into the connector to the left of the upper head cable connector. The J3 connector is the one closer to the rear of the drive.

7.	Replace the Read/Write module assembly (Paragraph 2.5.4).

8.	Replace the Cartridge Access Cover (Paragraph 2.3.2).

9.	Replace the Field Service Access Cover (Paragraph 2.3.1).

10.	Perform the Read/Write head alignment (Paragraph 3.6).

2.8   REAR PANEL AREA

2.8.1 Power Supply

To remove the power supply:

1.	Remove the drive from the slide rails (Paragraph 2.2.5, Steps 1 through 3).

2.	Remove the Field Service Access Cover (Paragraph 2.3.1).

3.	Remove the Cartridge Access Cover (Paragraph 2.3.2).

4.	Remove the AC Servo Module (Paragraph 2.5.1).

5.	Remove the DC Servo Module (Paragraph 2.5.2, Steps 1 through 4).

6.	Place the DC Servo Module on its edge in the mounting slots provided (Figure 2-9) and disconnect cable J1.

7.	Disconnect brush motor drive cable from its connector (Figure 2-11).

8. At the rear of the drive, remove the six mounting screws (Figure 2-20).

                              CAUTION
            The power panel assembly will swing out
            away from the drive after the last screw
            is removed. Therefore, the power supply
            panel should be held firmly in place
            until the last screw is removed.

To replace the power panel assembly:

1. Slide the rear panel assembly into the rear of the drive, ensuring that:

    • The top edge of the panel fits under the rear casting flange (see Figure 2-21, callout #1)

    • The bottom edge of the panel fits over the bottom pan of the drive (see Figure 2-21, callout #2)

2. While holding the panel firmly, start the two bottom screws so that the panel will be held in place for the remaining four screws.

3. Reconnect J1 of the DC Servo Module.

4. Reconnect the brush motor drive cable (Figure 2-9).

5. Replace the DC Servo Module (Paragraph 2.5.2).

6. Replace the AC Servo Module (Paragraph 2.5.1).

7. Replace the Cartridge Access Cover (Paragraph 2.3.2).

8. Replace the Field Service Access Cover (Paragraph 2.3.1).

9. Replace the drive into the cabinet (Paragraph 2.2.5).

2.8.2 Spindle Drive Belt

To remove the spindle drive belt:

1. Remove the power supply (Paragraph 2.8.1).

2. Remove the belt from the spindle pulley (Figure 2-15).

3. Remove the drive motor tension spring from the motor housing (Figure 2-22).

4. Pull belt out through the back of the drive.

I/O CABLE
("CABLE IN")

TERMINATOR

NORMAL/LOW
LINE VOLTAGE
TERMINAL BLOCK
COVER

110/220 VOLTS
TERMINAL
BLOCK COVER

CIRCUIT BREAKER

AC LINECORD

CABLE "OUT"
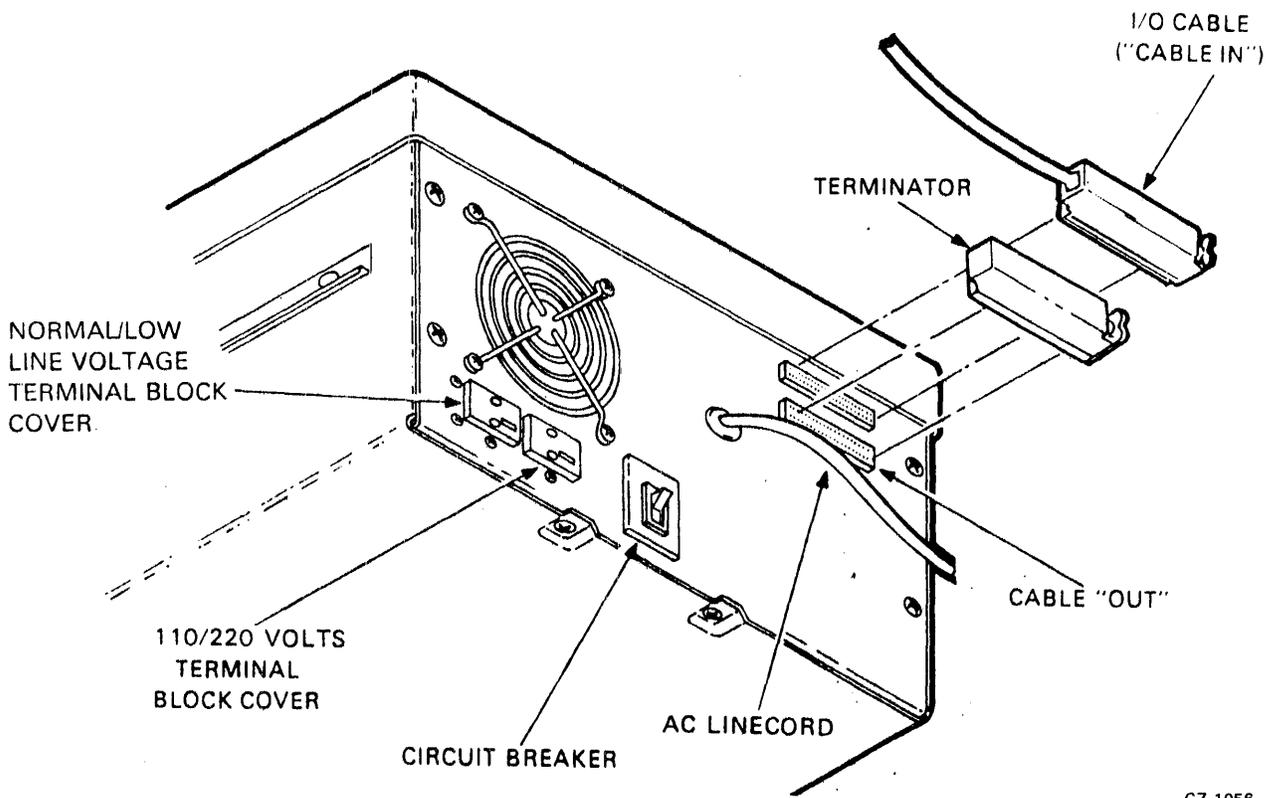
CZ-1056

Figure 2-20   Rear View of Drive

1

2

MOUNTING
SCREWS (6)

REAR POWER PANEL ASSEMBLY
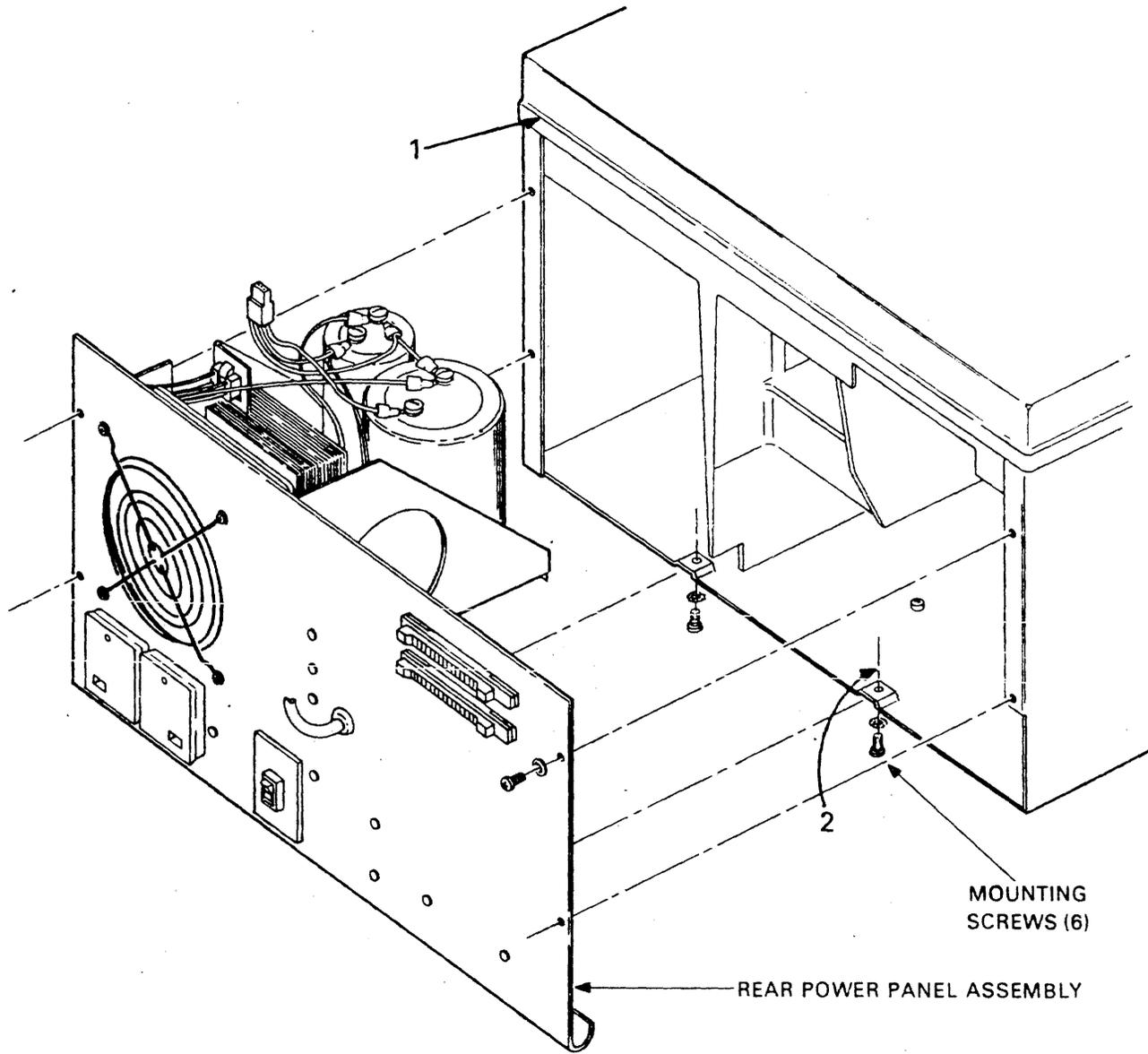
CZ-0015

Figure 2-21   Rear Panel Assembly

SCREW
LOCKWASHER
STEEL WASHER
SPRING WASHER
STEEL WASHER
DELRIN WASHER

DELRIN WASHER

SPRING (EXTENSION)
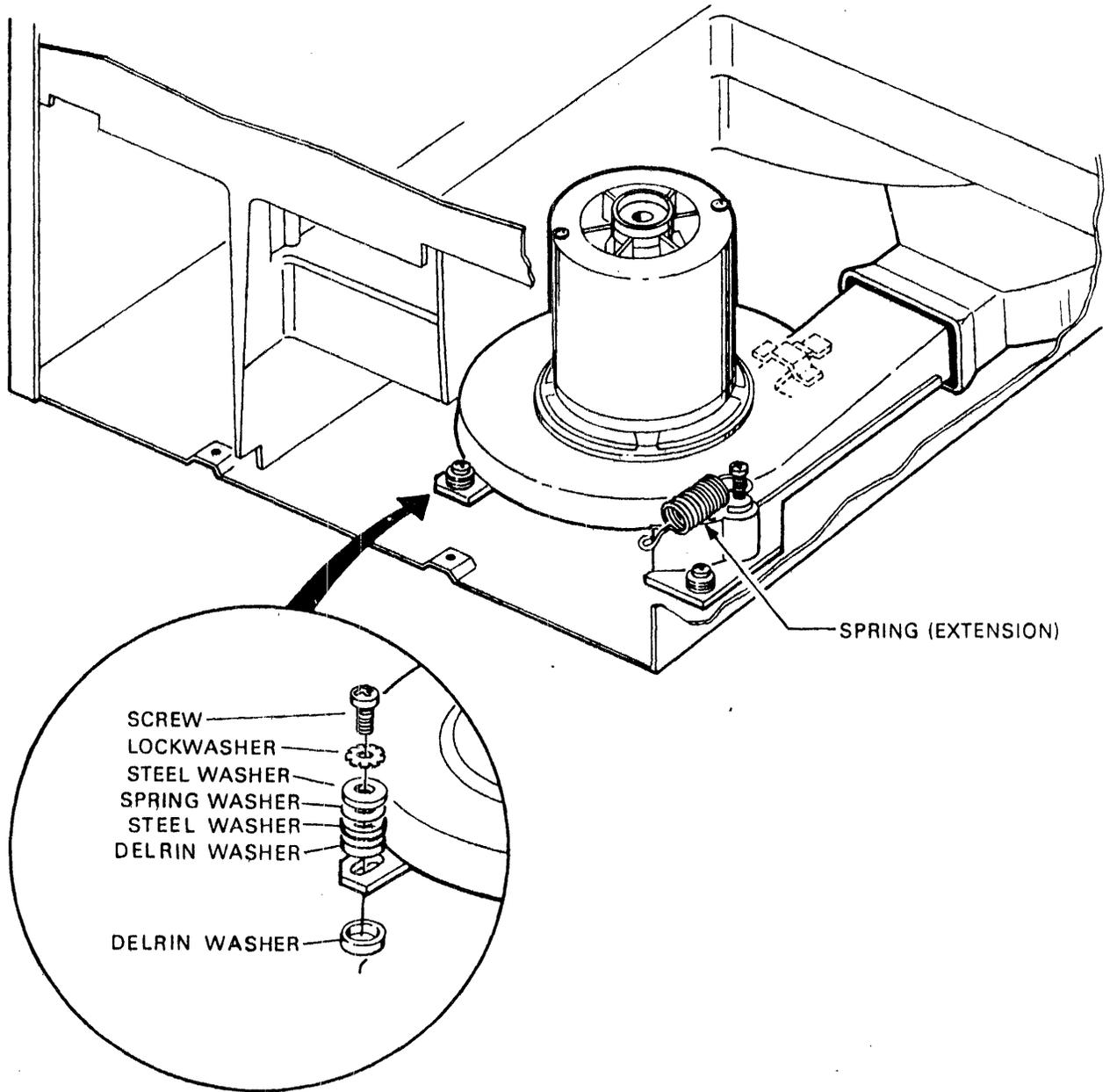
CZ-1062

Figure 2-22 Drive Motor Mounting

To replace the spindle drive belt:

1. Ensure the drive motor housing is as far forward in the
    drive as it will go.

2. Slip belt under housing (around the drive motor pulley)
    and slide the belt in the direction of the spindle
    pulley.

.3 From the access in the bottom of the drive, slip the belt
    onto the spindle pulley.

4. Ensure the belt is still on the motor housing pulley.

5. Slide drive motor housing as far to the rear of the drive
    as it will go, and reinstall the tension spring.

6. Rotate the spindle several times to position the belt on
    the self-centering pulleys and check for binding and/or
    twists in the belt.

7. The belt should have proper tension as applied by the
    tension spring. Figure 2-23 illustrates the proper belt
    tension.

8. Reinstall the power supply panel (Paragraph 2.8.1).

2.8.3 Power Supply Fan

To remove the power supply fan:

1. Remove the power supply (Paragraph 2.8.1).

2. Disconnect the ac plug to the fan.

3. Remove the four screws and nuts holding the fan in place.
    The bottom two nuts can be accessed with an open-end
    wrench or a pair of long-nosed pliers.

To replace the power supply fan:

1. Place the fan in place with the ac socket located on the
    top and the airflow direction arrow pointing to the rear
    of the assembly.

2. Reinstall the four screws securing the fan and finger
    guard.

3. Reinstall the power supply (Paragraph 2.8.1).
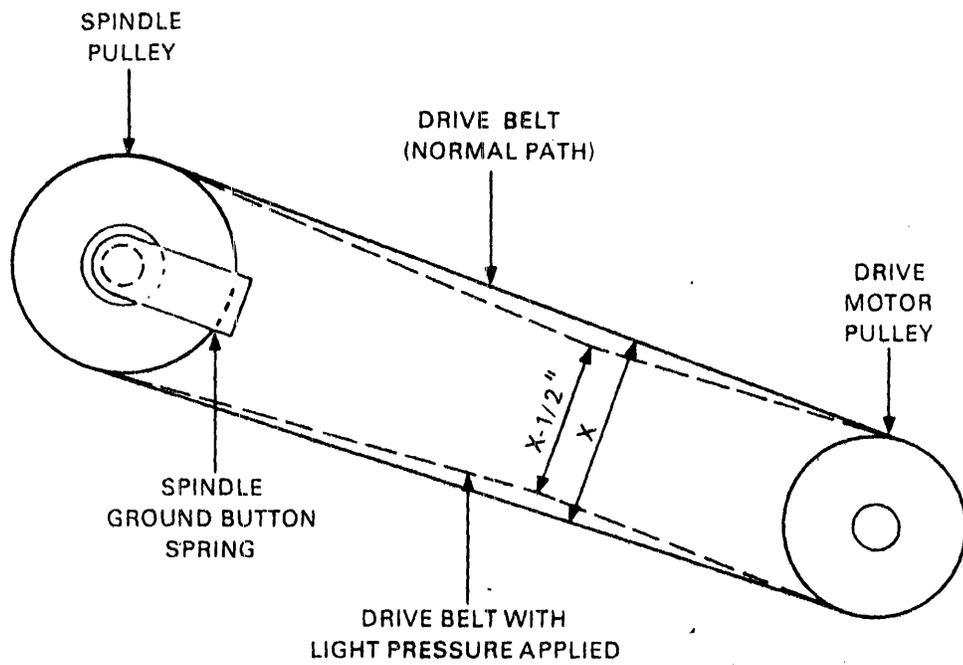
Figure 2-23 Drive Belt Tension

2.8.4 Circuit Breaker

To remove the circuit breaker:

1.   Remove the power supply (Paragraph 2.8.1).

2.   Locate the circuit breaker (Figure 2-24) and mark the wires going to the four breaker terminals.

3.   Remove the four wires on the breaker assembly.

4.   Squeeze on the four plastic holding tabs (two on the top of the breaker and two on the bottom) to release the breaker from the panel (Figure 2-24).

5.   Slide the breaker out the panel, toward the rear.

To replace the circuit breaker:

1.   Slide the breaker into the power supply panel, ensuring that the "OFF" position is down.

2.   Reconnect the wires going to the breaker, as marked when removed.

3.   Reinstall the power supply panel (Paragraph 2.8.1).

2.8.5 Spindle Drive Motor

To remove the spindle drive motor:

1.   Remove the power supply (Paragraph 2.8.1).

2.   Remove the drive motor tension spring from the motor housing (Figure 2-22).

3.   Remove the two drive motor mounting screws from the standoffs (Figure 2-25).

4.   Slide the drive motor housing forward slightly and lift the assembly up approximately one-half inch.

5.   Drive belt should have fallen off; if not, remove it.

6.   Slide drive motor out of the drive.

To replace the spindle drive motor:

1.   Check to see if the drive belt is still on the spindle pulley. If not, replace it.

2.   From the back of the drive, pull on the belt to take away the slack.

REAR PANEL
ASSEMBLY
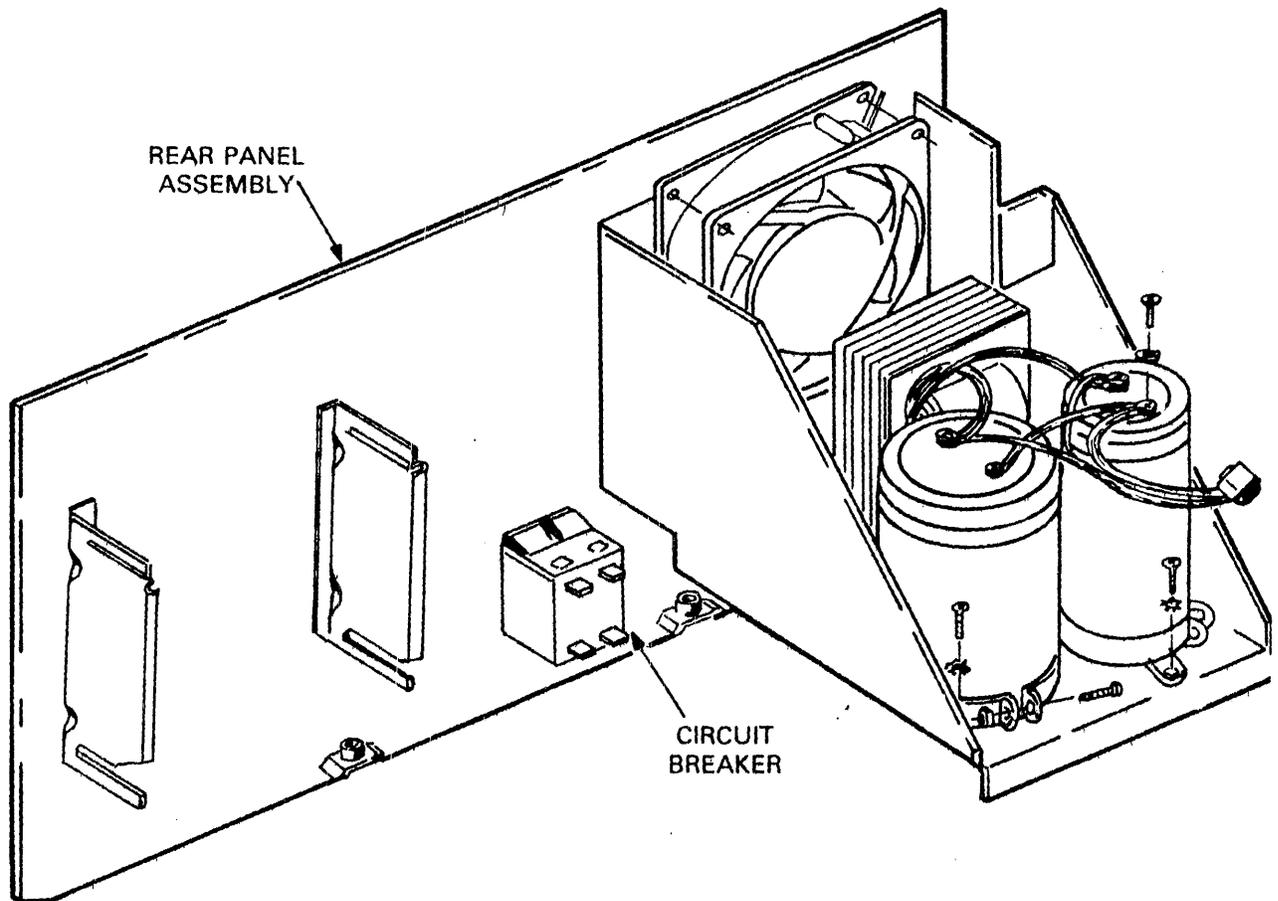
CIRCUIT
BREAKER

CZ-0017

Figure 2-24 Circuit Breaker

FILTER
DUCT

BRACKET
(C)

STANDOFFS
2 PLACES

TAB (B)

DISK MOTOR ASSY

TENSION
SPRING
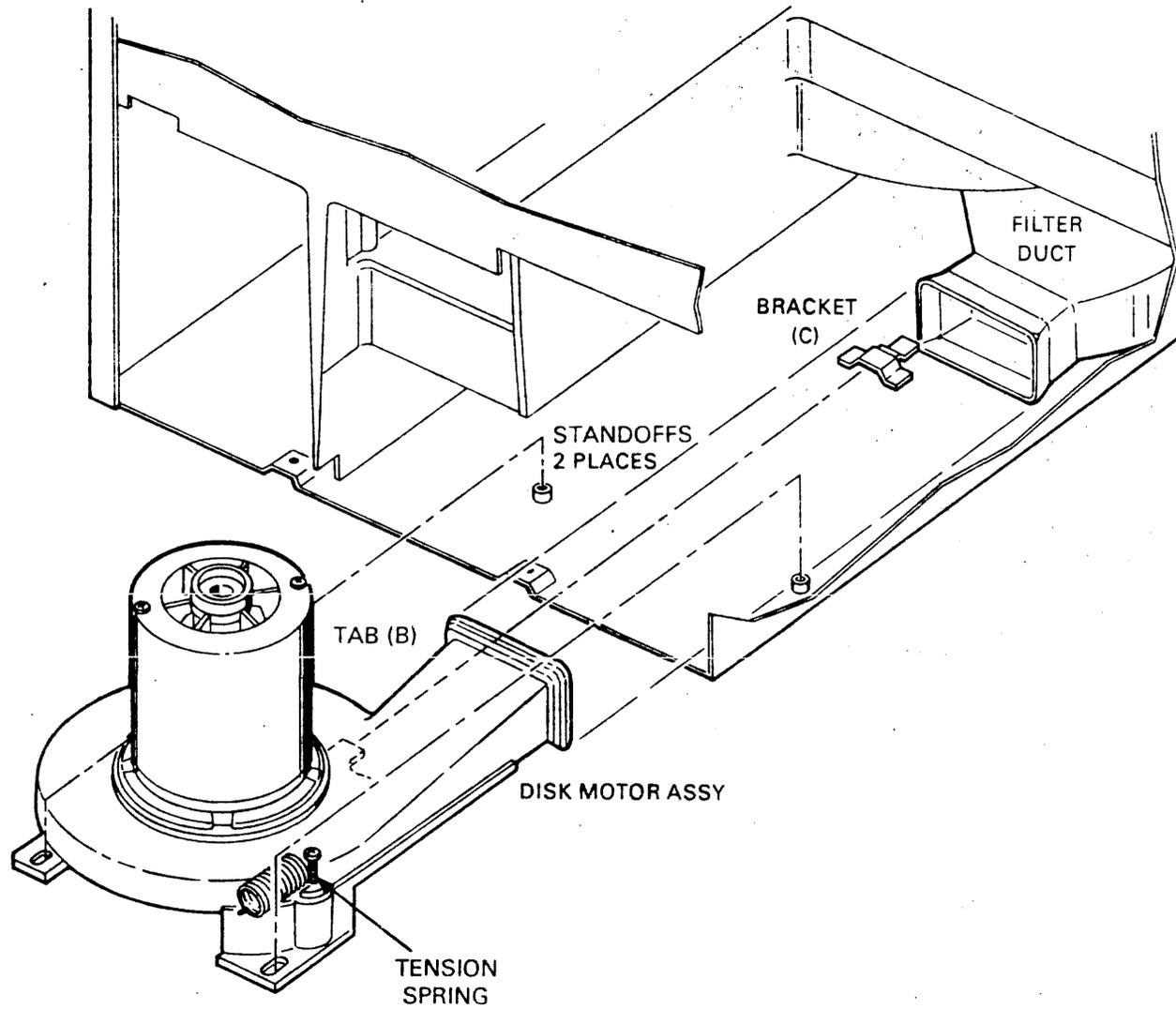
CZ-1064

Figure 2-25   Drive Motor Assembly Technique

3. Slip the belt onto the drive motor pulley.

4. Using Figure 2-25, reinstall drive motor into the rear of the drive, noting that:

    ● Tab (B) fits under bracket (C)

    ● Blower housing mounting pads fit over the standoffs

    ● Delrin spacers are still on the standoffs

5. Check that belt did not come off the motor pulley.

6. If the belt is still on, check to see if it came off the spindle pulley. If belt is off, replace on the pulley.

7. Attach the drive motor tension spring to the motor housing (Figure 2-22).

8. Install mounting hardware on drive motor housing, using Figure 2-25 as a guide.

9. Pull backward on the drive motor housing to apply tension to the belt. Tension spring should hold motor in place.

10. Rotate spindle several times to position belt on the crowned self-centering pulleys.

11. The belt should have proper tension as applied by the tension spring. Figure 2-23 illustrates proper belt tension.

12. Reinstall the power supply panel (Paragraph 2.8.1).

3.1   INTRODUCTION

Many of the checks, adjustments and alignments described in this chapter deal with the Drive Logic Module (DLM). Because there are three different versions of the DLM, it is necessary to first identify the particular type of module on the drive being serviced. The three versions are shown in Figure 3-1.

- Version 1 (Part No. 54-12175) can be identified by the fact that the two Berg connectors in the lower right hand of the module point down, which the other two along the bottom row point up. This board will only operate in an RL01.

- Version 2 (Part No. 54-13531) has all four connectors in the bottom row pointing up, as in Figure 3-1. This module will function in an Rl01 or an RL02.

- Version 3 (Part No. 54-14025) has the same arrangement of Berg connectors as Version 2, but it also has test lugs (shown in Figure 3-1) that are not on either of the other two modules.

The service jumpers used in these checks and adjustments are listed in Table 3-1.

Table 3-1   Service Jumpers for Drive Logic Module

VERSION	DEFEAT COVER SWITCH	DEFEAT POS SIG	DEFEAT SK TO	SELECT HEAD 1
1	E33-3 to E33-7	TP8 to TP1-6	E17-6 to E17-7	--
2	E54-12 to E54-7	TP6 to TP1-4	E10-8 to E10-7	--
3	TP19 to TP20	TP25 to TP26	TP23 to TP24	TP21 to TP22

In the course of performing some of the alignments, it is necessary to select Head 1 and then later reselect Head 0. The mehtods for accomplishing this are shown in Table 3-2.

VERSION 1

T2 T3

TP6

TP5

TP1

TP2

TP8   TP7   TP12   T1
       •TP11   •TP9

J5 R

TP13
J14   R   J6   J2   J4   R   J11 R

J12   R   TP10 •TP4   •TP3
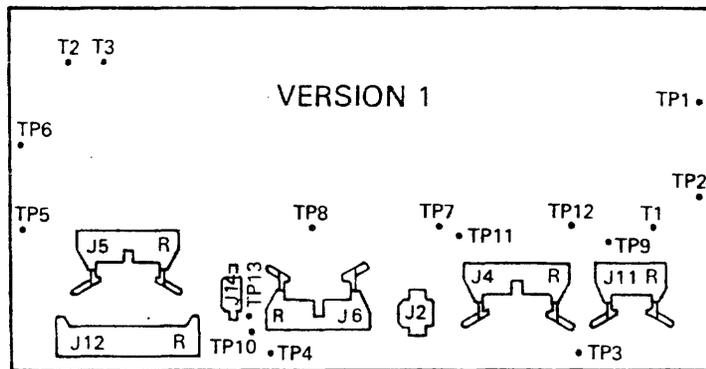
54-12175
RL01 ONLY

NOTE:
J11 AND J4
POINT DOWN

J14   J2

```
1      6 4 2
2
3      5 3 1
```

VERSION 2   W1

TP4   TP13   TP12   TP2•
                                TP16
                                    TP11

T1   T3
T2•

J5   R   TP6

J14
R   J6   J2   J4   R   J11 R

TP3 J12   R   TP14
              •TP5   TP15-7- 8-10-9   TP1•   TP18 → TP17
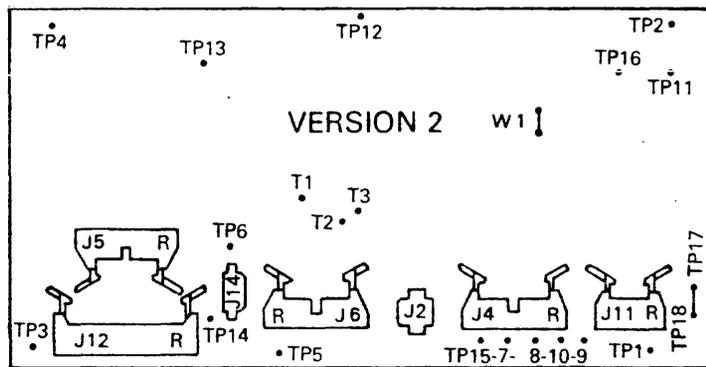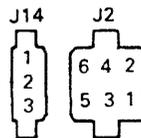
54-13531
RL02 OR RL01
W1 IN FOR RL01
W1 OUT FOR RL02

NOTE:
J4 AND J11 POINT UP
NO TP19 THRU 26

VERSION 3

TP4   TP12 TP21 ⊙ ⊙ TP22   TP2
        •TP13
    ⊙ TP19   TP16
    ⊙ TP20   TP11
                                         W1
                    T1   T3   TP23
    TP25 ⊙   ⊙
        ⊙ TP26   ⊙
        •TP6   T2   TP24
J5   R
                                    R   R   TP17
J14
    R   J6   J2   J4   R   J11 R
TP3 J12   R   TP14   TP18
            •TP5   TP15-7- 8-10-9   TP1
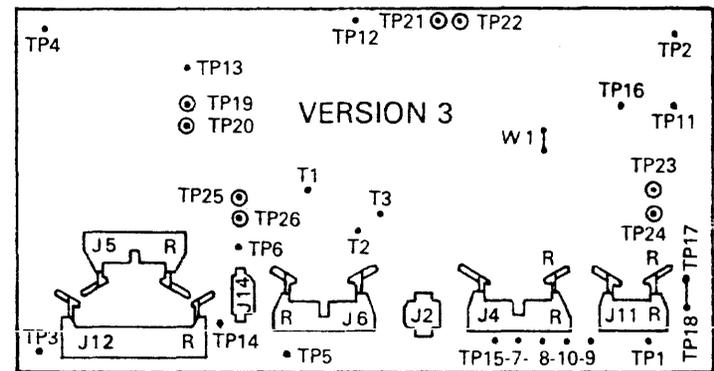
NOTE: R DENOTES RED STRIPE

54-14025
RL02 OR RL01
W1 IN FOR RL01
W1 OUT FOR RL02

NOTE:
J4 AND J11 POINT UP
HAS TP19 THRU 26

JUMPER
TEST LUGS   EFFECT
19-20   DEFEAT COVER CLOSED
21-22   SELECT HEAD 1
23-24   DISABLE SKTO
25-26   DEFEAT POS SIG
(THESE TEST LUGS ARE CIRCLED)

CZ-0018

Figure 3-1   Drive Logic Module Layout

Table 3-2 Methods for Selecting Heads

	DLM VERSION 1 OR 2	DLM VERSION 3
PDP-11	Load DZRLCXX or CZRLIXX and run head alignment routine. WRITE PROTect switch in = Head 1, out = Head 0	Jumper TP21 to 22 = Head 1 No jumper = Head 0
PDP-8	Load AJRLBXX or AJRLHXX and run head alignment routine. WRITE PROTect switch in = Head 1, out = Head 0	Same as above

NOTE
If diagnostics are not available, toggle in the appropriate program shown in Appendix C.

3.2 VOLTAGE CHECKS

The DC Servo module template indicates voltage test points. Check the following voltages.

Voltage	Limits
$+V_{un}$	+14V to +18V
$-V_{un}$	-14V to -18V
$+5V$	+4.85V to +5.35V
+8V	+7.7V to +8.3V
-8V	-7.7V to -8.3V

The regulators on the DC Servo module are not adjustable. If a voltage is out of tolerance, the faulty FRU should be replaced.

The +5V can be killed by a blown pico fuse, a thermal switch on the DC Servo heat sink, an overvoltage crowbar, or a home switch on the positioner not closed during power up.

3.3 SECTOR TRANSDUCER OUTPUT CHECK

This check verifies a correct output of the sector transducer.

A. Required Tools:

1. Oscilloscope with probe
2. DIP clip.

B. Check:

   1. Remove both top cover assemblies.

   2. Install cartridge.

   3. Defeat the cover interlock (Table 3-1).

   4. Depress LOAD switch.

   5. While waiting for the heads to load onto the pack, set up the oscilloscope (sync internal negative-going).

   6a. Version 1 of DLM: Place oscilloscope probe on E8, pin 8.

   6b. Version 2 of DLM: Place oscilloscope probe on TP14.

   6c. Version 3 of DLM: Place oscilloscope probe on TP14.

   7. The signal displayed on the oscilloscope should be similar to that shown in Figure 3-2. The peak output of the negative portion of the waveform should be between $0.35Vp$ and $1.5Vp$.

                         NOTE
   The wave form must be negative-going first.

3.4 SECTOR PULSE TIMING CHECK
This is a check of the sector pulse width and repetition rate. The repetition rate is a function of spindle speed.

A. Required Tools:

   Oscilloscope with probe.

B. Check:

   1. Remove both top cover assemblies.

   2. Defeat cover interlock (Table 3-1).

   3. Install cartridge.

   4. Depress LOAD switch.

   5a. Version 1 of DLM: Place the probe on TP9.

   5b. Version 2 of DLM: Place the probe on TP11.

   5c. Version 3 of DLM: Place the probe on TP11.

+V.

OV.

-V.

.35V.
to
1.5 V.

TIME = 100 μSEC/DIV.
VOLTS = 200 MV/DIV.

MA·1602
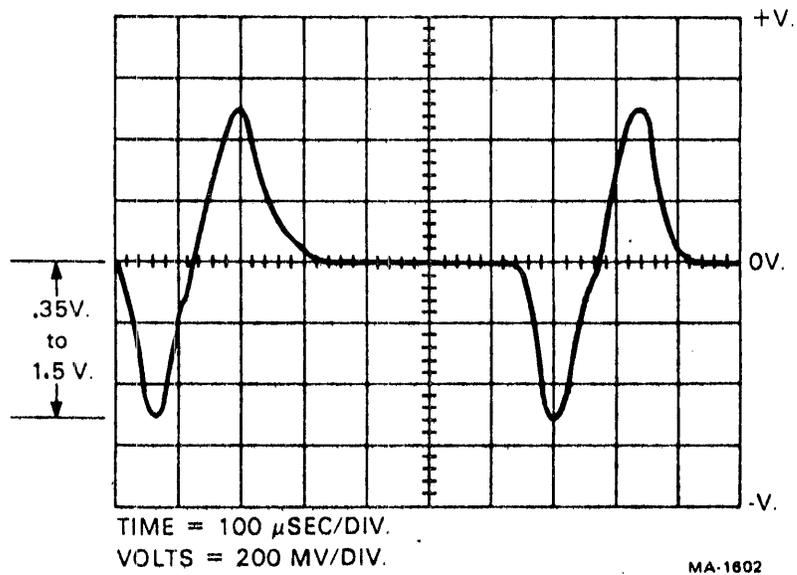
Figure 3-2   Sector Transducer Output

6. Set the oscilloscope to sync internal, negative-going. The signal displayed on the oscilloscope should be the same as in Figure 3-3. Sector pulse width should be 62.5 microseconds. Correct disk speed ranges from 594 microseconds to 639 microseconds, with 624 being the desired norm. The sector pulses should be stable at some time period within that range.

3.5   POSITIONER RADIAL ALIGNMENT
This adjustment assures that the servo burst (as read by the read/write heads) occur in the proper time relation to the sector pulses from the cartridge hub. It also enables the technician to observe how straight the carriage motion is over the length of travel, and also acts as a check for head skew.

A.   Tools Required:

1. Oscilloscope with two probes

2. Two flat-blade screwdrivers

3. One Phillips head screwdriver

4a. One DIP clip, one pin-to-pin jumper and one test lead, or

4b. Two pin-to-pin jumpers and two DIP clips

5. Diagnostic listed in Table 3-2.

B.   Positioner Alignment Check:

1. Remove both top cover assemblies.

2. Defeat POS SIG, SKTO and cover interlock (Table 3-1).

3. Place the Read/Write module box assembly up and out of the way of the carriage assembly.

4. Install cartridge.

5. Depress LOAD switch.

6. Wait for heads to load onto the pack.

7. Disable servo drive to the carriage by disconnecting the in-line connector (Figure 3-4).

8. Select Head 1 (Table 3-2).

9. Place the Channel B oscilloscope probe on TP2 (data) of the Read/Write module and Channel A ground on TP3.
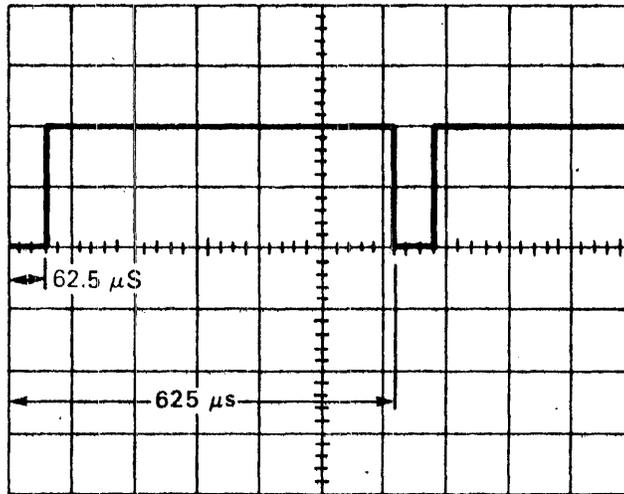
TIME = 100 μs/DIV.
VOLTS = 2V/DIV.

CZ-1078

Figure 3-3   Sector Pulse Timing

PLUG FOR
LOWER HEAD

J3

J2

PLUG FOR
UPPER HEAD

R/W
MODULE

HOLDING
FLANGES

UPPER
HEAD
CABLE

LOWER
HEAD
CABLE

IN-LINE
SERVO
CONNECTOR

POSITIONER
ASSEMBLY

CZ-2054

Figure 3-4   Positioner and Read/Write Module Box Assembly

10a. Version 1 of DLM: Place Channel A probe on TP9 (SEC TIME) and Channel B ground on any signal ground (TP1-TP4).

10b. Version 2 of DLM: Place Channel A probe on TP11 (SEC TIME) and Channel B ground on any signal ground (TP1-TP4).

10c. Version 3 of DLM: Place Channel A probe on TP11 (SEC TIME) and Channel B ground on any signal ground (TP1-TP4).

11. Set the oscilloscope to sync internal, negative-going on Channel A and observe the waveform shown in Figure 3-5.

NOTE
S1 and S2 servo bursts may not appear in the positive/negative proportions shown in Figure 3-5, depending upon which track the head is centered on.

12. Measure the time between the negative-going edge of the sector pulse and the beginning of the S1 servo burst when the positioner is at Cylinder 0. Record this value.

13. Select Head 0 (Table 3-2).

14. Repeat Step 12 for Head 0. Record this value.

15. If the difference between these two values is greater than six microseconds, replace Head 0 (see Chapter 2) and go back to Step 14. If either of the two values falls outside of the 15 + 3 microsecond specification, perform the alignment procedure (Part C below. Otherwise, continue.

16. Manuallly move the carriage to the last data track (track 255 on an RL01 or track 511 on an RL02). As Head 0 enters the inner guard band, S1 disappears. Move the positioner back until S1 appears.

17. Measure the time between the negative-going edge of the sector pulse and the beginning of the S1 servo burst when the positioner is at the last cylinder. It should be 15 + 3 microseconds. If so, the check is complete. Otherwise perform the adjustment (Part C) below.
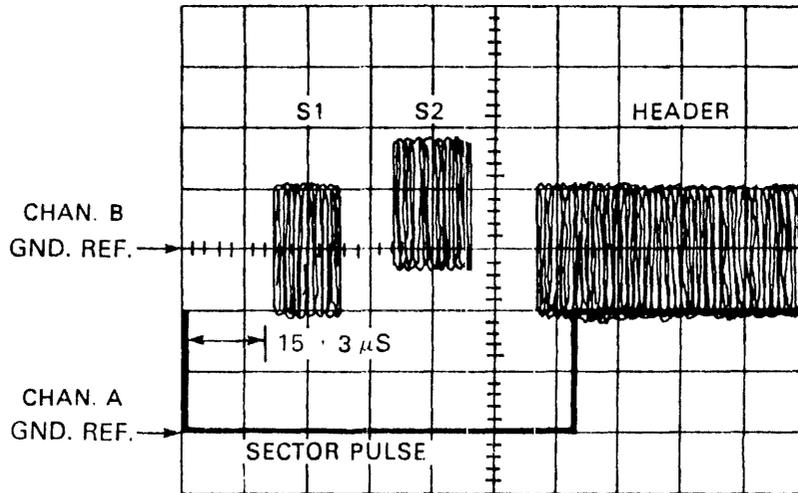
TIME: 10 MICROSEC/DIV.
CHAN: "A" 500 MILLI VOLTS/DIV.
CHAN: "B" 2 VOLTS/DIV.   CZ-1077

Figure 3-5   Servo Bursts and Sector Pulse

C. Positioner Alignment

1. Using Figure 3-6 as a guide, locate the six largest Phillips screws on the positioner baseplate.

2. Loosen (but do not remove) the six screws holding down the positioner.

3. Take the two flat-blade screwdrivers and insert them into the adjusting slots on the positioner.

4. Move the positioner assembly against the right hand side of the drive (toward the Read/Write module).

5. Manually move the carriage to its approximate center of travel.

6. Using the two flat-blade screwdrivers in the adjusting slots, slide the positioner baseplate until the 15 + 3 microsecond specification between the fall of the sector pulse and the rise of the S1 servo burst can be met. (See Figure 3-5).

NOTE
Equal pressure must be exerted on the screwdrivers when sliding the positioner to ensure that the baseplate is kept straight.

7. Tighten the six retaining screws in small increments.

8. Check the 15 + 3 microseconds specification for Head 0 at track 0 and the last track. If the head is within the specification, the check is complete. Otherwise, repeat the adjustment (Part C) above.

3.6   HEAD ALIGNMENT
This procedure will ensure that the two heads are in line with each other to cut down on the servo tracking time when switching heads.

NOTE
The Positioner Radial Alignment (Paragraph 3.5) should be done before attempting the head alignment, so that any head skew that may be present will be detected BEFORE the head alignment.

THESE 2 SCREWS ARE
NEAREST THE MOTOR
SHAFT AND ARE THE LONGEST
OF THE SIX MOUNTING
SCREWS.

HEADS HOME SWITCH
ADJUSTING SCREW

POSITIONER
ADJUSTING
SLOT

POSITIONER
ADJUSTING SLOT
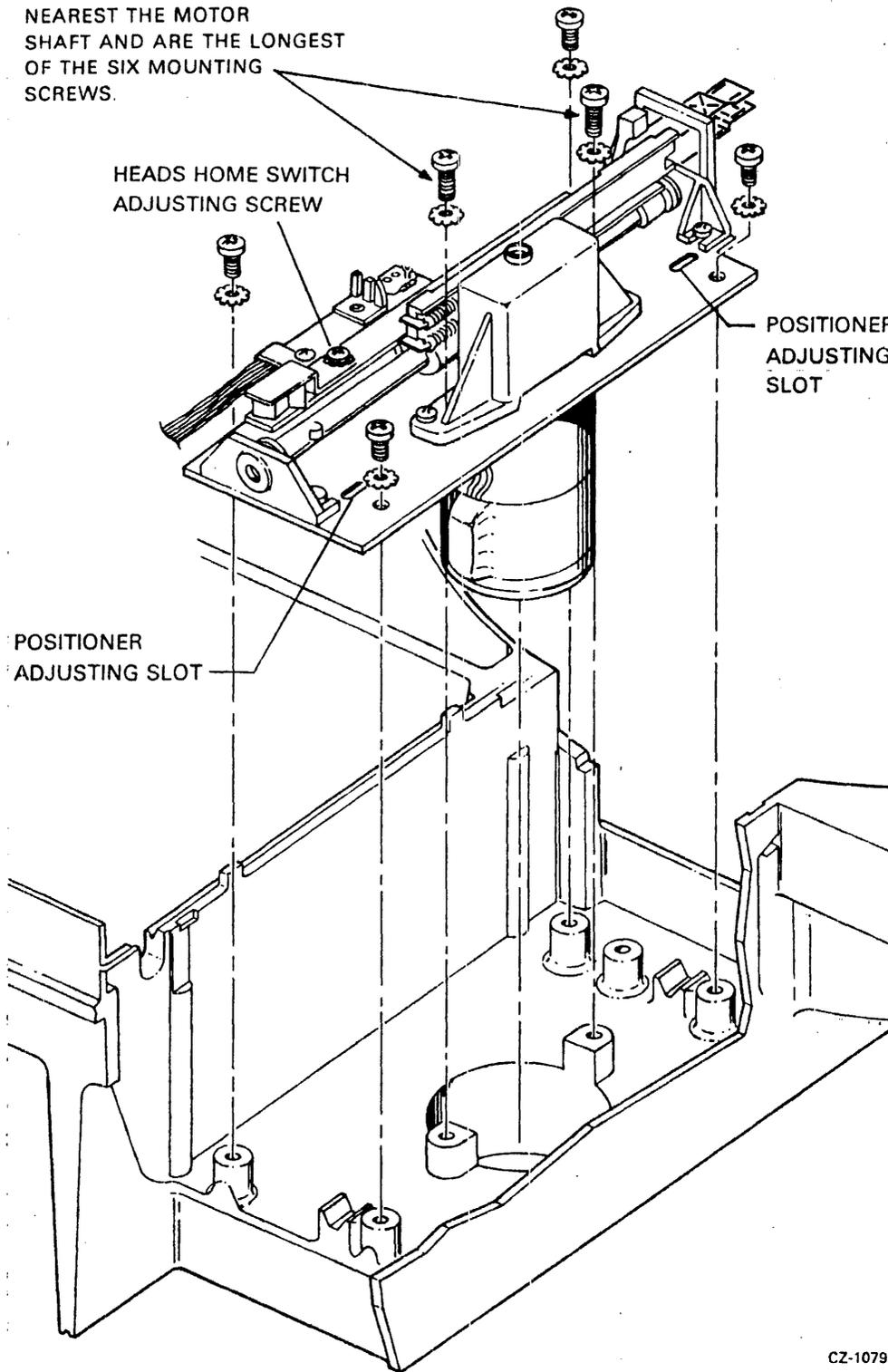
CZ-1079

Figure 3-6   Positioner Assembly

II/3-12

A. Required Tools:

1. Oscilloscope with three probes

2. 3/32" Allen wrench

3. Flat-blade screwdriver

4a. One DIP clip, one pin-to-pin jumper and one test lead
    (alligator clip), or

4b. Two pin-to-pin jumpers and two DIP clips
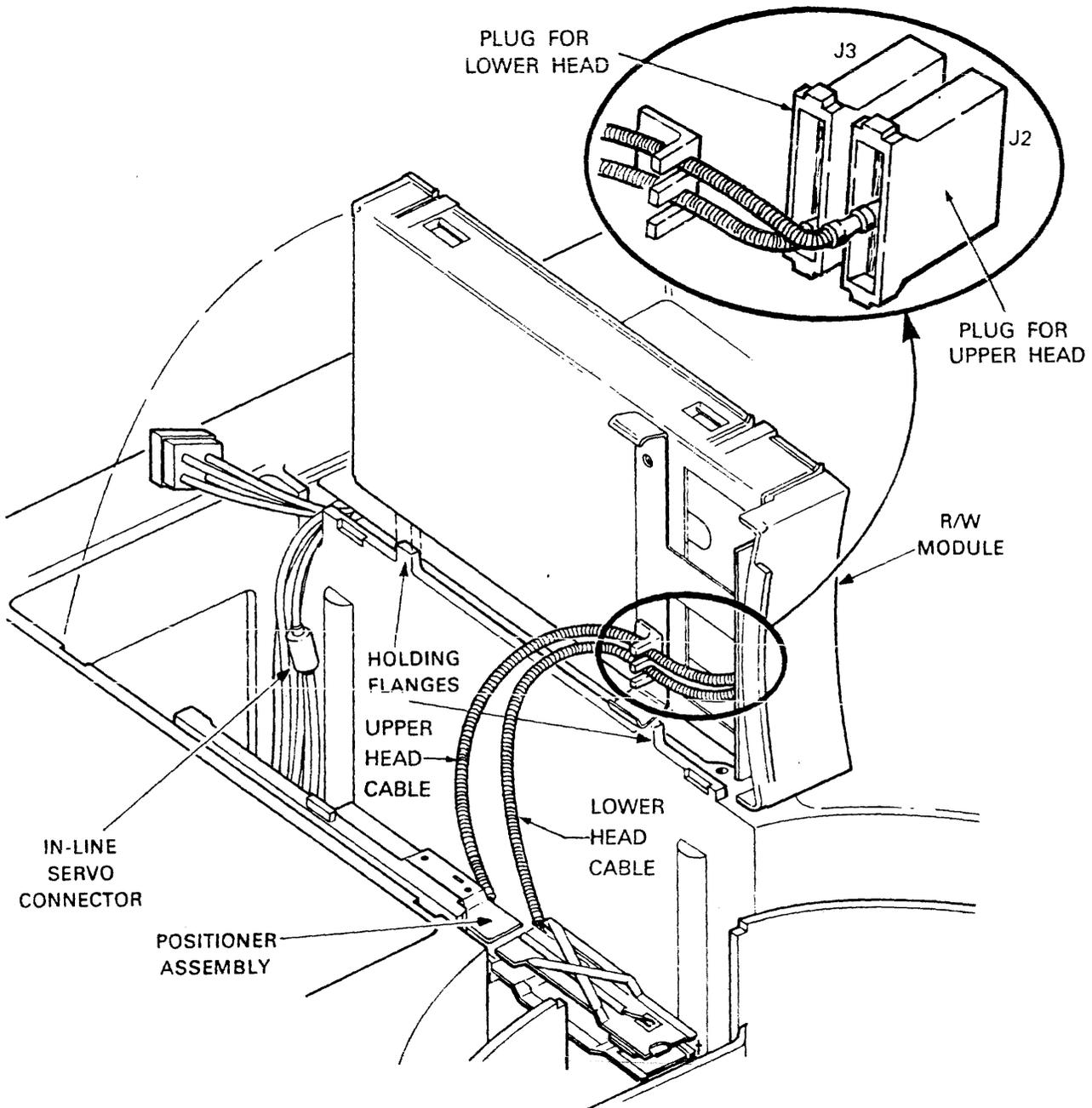
5. Diagnostic listed in Table 3-2.

NOTE
No alignment cartidge is required.

B. Alignment Check:

1. Remove both top cover assemblies.

2. Defeat SKTO and POS SIG (Table 3-1).

NOTE
These jumpers enable the diagnostic
routine to work by disabling the Seek
Timeout Error.

3. Defeat cover interlock (Table 3-1).

4. Place the Read/Write module box assembly up and out
    of the way of the carriage assembly.

5. Install cartridge.

6. Depress the LOAD switch.

7. Wait for the heads to load onto the pack.

8. Disable servo drive to the carriage by disconnecting
    the servo in-line connector (Figure 3-4).

9. Select Head 1 (Table 3-2).

10. Place the Channel A oscilloscope probe on TP2 of the
    Read/Write module (Servo Data) and Channel A ground
    on the test point ground (TP3) of this module.

11a. Version 1 of DLM: Place the Channel B probe on E11
     pin 7 (Position Signal) and external sync probe on
     TP9 (SEC TIME).

11b. Version 2 of DLM: Place the Channel B probe on TP15 (Position Signal) and external sync porbe on TP11 (SEC TIME).

11c. Version 3 of DLM: Place the Channel B probe on TP15 (Position Signal) and external sync probe on TP11 (SEC TIME).

12. Set the oscilloscope to sync internal, negative-going and observe the waveform shwon in Figure 3-7.

NOTE

S1 and S2 servo bursts may not appear in the same positive/negative proportions shown in Figure 3-7 depepnding upon which track the head is centered on.

13. Manually position the carriage to track 0 by observing the S1/S2 servo burst waveforms. Move the positioner in reverse (away from spindle) until S2 disappears (as in Figure 3-8), the carriage is in the outer guard band area. Move the positioner slowly forward (toward the spindle) until S2 reappears.

14. Move the positioner until the Position Signal (Channel B) goes to ground potential. The head is now on the centerline of data track 0.

15. Select Head 0 (Table 3-2).

16. The Position Signal (Channel B) should be within 0.5 volts of the Position Signal presented by head 1. If it is not, perform the head alignment described below.

17. Slowly move the carriage in reverse (away from the spindle). The S2 data burst should decrease in amplitude and finally disappear. See Figure 3-8. The Position Signal (Channel B) should also have moved in the negative direction and stopped. If the signal did not stop, but instead reversed direction and continued (as the carriage continued moving) then more data tracks were crossed. Therefore, Head 0 was not on track 0, necessitating a head alignment (described below).

C. Head Alignment

1. Using the 3/32" Allen wrench, loosen the Head 0 retaining screw and slide the head to the rear against its stop.

2. Select Head 1 (Table 3-2).

TIME = 10μS/DIV.
CHAN A = 500 MV/DIV.
CHAN B = 500 MV/DIV.
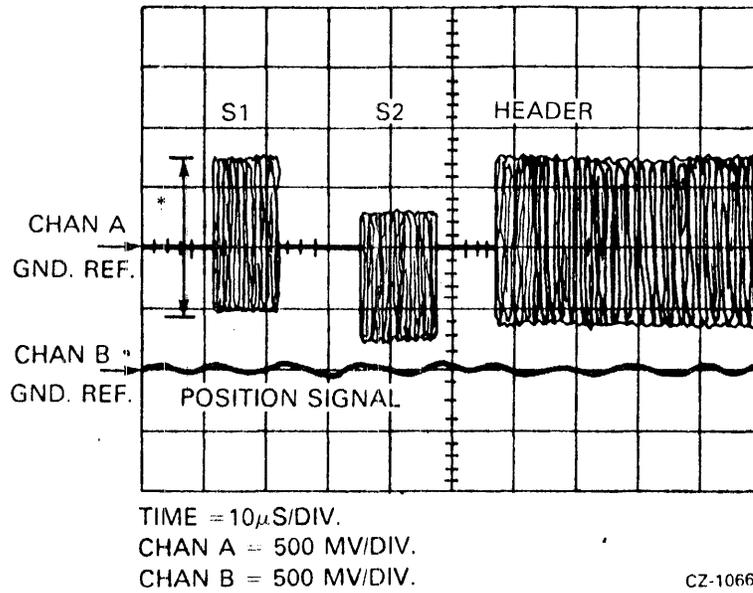
CZ-1066

Figure 3-7   Servo Bursts and Position Signal

TIME = 10µS/DIV.
CHAN A = 500 MV/DIV.
CHAN B = 500 MV/DIV.
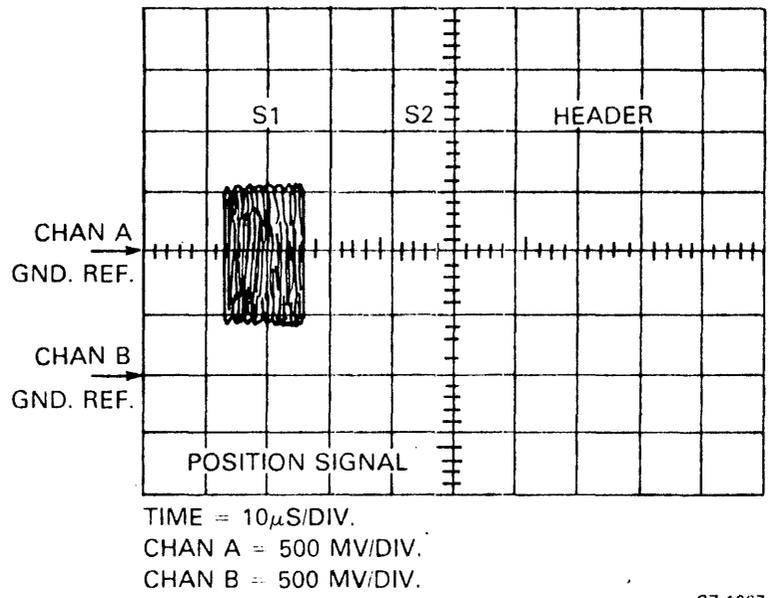
CZ-1067

Figure 3-8   Outer Guard Band Servo Data

3. Manually position thee carriage to track 0 by observing the S1/S2 burst waveforms. When S2 disappears (as in Figure 3-8), the carriage is in the outer guard band area. Move the positioner slowly forward until S2 reappears and the Position Signal reaches ground.

4. Select Head 0.

NOTE
While performing steps 5 and 6 (which follow), be sure that the carriage does not move.

5. Insert a flat-blade screwdriver between the tailstock of Head 0 and the rear stop.

6. While holding the carriage, use the screwdriver to move Head 0 forward until the S2 servo burst reappears and the Position Signal reaches ground.

7. Tighten the head retaining screw with the 3/32" Allen wrench. Do not over tighten the screw.

CAUTION
If the retaining screw is overtighened, the threads on the aluminum frame may be damaged.

8. Select Head 1 (Table 3-2).

9. The next few steps check to see that the heads have been properly aligned. Begin this check by manually positioning the carriage to track 0. As before, this is doen by observing the S1/S2 servo burst waveforms. When S2 disappears, as shown in Figure 3-8, the carriage is once again in the outer guard band area. Move the positioner slowly forward until S2 reappears.

10. Move the positioner until the Position Signal (Channel B) goes to ground potential. The head is now on the centerline of data track 0.

11. Select Head 0.

12. The Position Signal (Channel B) should be within 0.5 volts of the Position Signal presented by Head 1. If it is not, this head alignment procedure must be repeated.

13. After observing that the position signals from each head are within 0.5 volts of each other, check to see that both heads were aligned over track 0. First, mvoe the carriage slowly in reverse. If Head 0 was over track 0, then the S2 data will decrease in amplitude and finally disappear. See Figure 3-8. Also, the Position Signal (Channel B) should have moved in the negative direction and stopped. If the signal did not stop, but instead reversed direction and continued (as the carriage continued moving) then more data tracks were crossed. Therefore, Head 0 was not on track 0, necessitating a head alignment (repeat this procedure).

3.7 READ SIGNAL AMPLITUDE CHECK

This check compares the amplitudes of the read signal from each Read/Write head against the data in the engineering specification.

A. Required Tools:

1. Oscilloscope with three probes

2a. One DIP clip, one pin-to-pin jumper and one test lead (alligator clip), or

2b. Two pin-to-pin jumpers and two DIP clips

3. Diagnostic listed in Table 3-2.'

B. Check:

1. Remove both top cover assemblies.

2. Defeat SKTO, POS SIG and cover interlock (Table 3-1).

3. Place the Read/Write module box assembly up and out of the way on the carriage assembly.

4. Install cartridge.

5. Depress the LOAD switch.

6. Wait for the heads to load.

7. Disable the servo drive to the carriage by disconnecting the in-line connector.

8. Place the Channel A oscilloscope probe on TP2 of the Read/Write module (Servo Data).

9a. Version 1 of DLM: Place Channel B probe on E11 pin 7 (Position Signal) and place the external sync probe on TP9 (Sector Time).

9b. Version 2 of DLM: Place Channel B probe on TP15 (Position Signal) and place the external sync probe on TP11 (Sector Time).

9c. Version 3 of DLM: Place Channel B probe on TP15 (Position Signal) and place the external sync probe on TP11 (Sector Time).

10. Set the oscilloscope to sync internal, negative-going and observe the waveform shown in Figure 3-7.

11. Move the positioner forward until the S1 servo burst loses amplitude and finally disappears.

12. Pull the positioner back slowly until the S1 servo burst returns. This will be the last data track on the disk (track 255 on an RL01, track 511 on an RL02).

13. Carefully move the positioner until it is on the track centerline. This is done by observing the Channel B signal which is the Integrated Position signal. It will be at a ground reference when on track (see Figure 3-7).

14. Measure and record the amplitude of the S1 burst for both heads (see Table 3-2 to select heads) while on this track centerline (as indicated by the asterisk in Figure 3-7. Ensure that the positioner does not move from the track centerline.

15. The lower of the two amplitudes should be no less than 432 mv.

16. Reposition the carriage to track 0 by reversing the carriage until S2 disappears (outer guard band) and the forward until S2 reappears.

17. Measure and record the amplitude of both heads. Table 3-2 explains how to select heads.

18. The amplitude of the S1 burst on track 0 should be less than 2.38 volts.

19. Replace either or both heads that do not meet the specifications.

NOTE
If both heads fail to meet the specifi-
cation, it is possible that the Read/
Write module is bad. Replace the module
(see Chapter 2) and repeat the proce-
dure. If a head is replaced, it must be
aligned (see Paragraph 3.6). The radial
alignment must also be checked
(Paragraph 3.5).

3.8   SPINDLE RUNOUT CHECK
Excessive runout in the spindle assembly or cartridge can cause
severe tracking problems for the positioning system. This check
will determine whether:

1.   Runout exists or does not exist
2.   Runout is in the cartridge
3.   Runout is in the spindle.

A.   Required Tools:

1.   Oscilloscope with probe and ground leads
2.   DIP clip
3.   Jumper
4.   Several test cartridges

B.   Runout Check:

1.   Remove both top cover assemblies.

2.   Place the Read/Write module box assembly up and out
      of the way of the carriage assembly.

3.   Defeat cover interlock (Table 3-1).

4.   Install cartridge.

5.   Depress LOAD switch.

6.   Wait for heads to load onto the pack.

7.   Disable servo drive to the carriage by disconnecting
      the in-line connector (Figure 3-4).

8a.   Version 1 of DLM: Place Channel A oscilloscope probe
      on E11 pin 7 (Position Signal) and place Channel A
      ground on TP7 (Integrator Ground).

8b.   Vrsion 2 of DLM: Place Channel A oscilloscope probe
      on TP15 (Position Signal) and place Channel A ground
      on TP5 (Integrator Ground).

TIME = 5MS/CM
VOLTS = 200MV/DIV.

CZ-1068
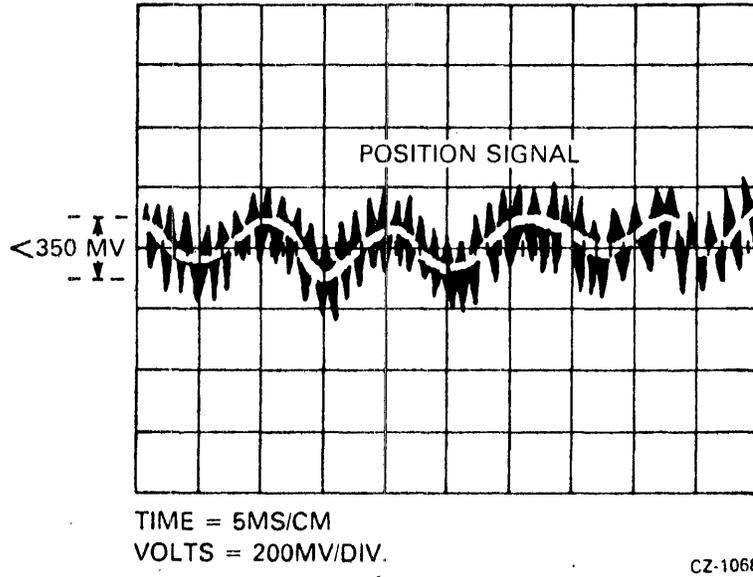
Figure 3-9   Position Signal

8c. Version 3 of DLM: Place Channel A oscilloscope probe
on TP15 (Position Signal) and place Channel A ground
on TP5 (Integrator Ground).

9. Set the oscilloscope to sync internal, negative-going
and observe the waveform in Figure 3-9.

10. The waveform representing runout should be measured
symmetrically about the ground reference.

11. The amplitude of the runout should be no greater than
350 mv.

12. If the specification cannot be met, runout exists and
another cartridge is needed to determine if the
runout exists in the cartridge or the spindle.

NOTE
Ideally, the oscilloscope will display a
nearly straight line of dots.

13. To confirm a seating problem, re-seat the cartridge
and repeat the runout check. If the runout is within
specification, the problem has been solved. If the
runout is still out of specification, continue with
Step 14.

14. Spindle and cartridge are still suspect, so install a
second cartridge and repeat check. If runout is now
within the specification, the first cartridge is bad.
If the runout check fails once more, assume that the
spindle bearings are bad and replace the spindle
assembly.

3.9 POSITION SIGNAL GAIN CHECK
Insufficient amplitude of the Position Signal cound result in the
carriage not being able to hold itself on track, resulting in read
errors and possible seek errors. Too high an amplitude could
result in a jitter which, in turn, emits a vibrating-type noise
from the carriage that may generate seek timeout errors.

A. Required Tools:

1. Oscilloscope with probe and ground leads
2. One DIP clip, one pin-to-pin jumper.

B. Gain Check:

1. Remove both top cover assemblies.

2. Place the Read/Write module box assembly up and out
of the way of the carriage assembly.

3. Defeat cover interlock (Table 3-1).

4. Install cartridge.

5. Depress LOAD switch.

6. Wait for heads to load onto the pack.

7. Disable servo drive to the carriage by disconnecting the in-line connector (Figure 3-4).

8a. Version 1 of DLM: Place Channel A oscilloscope probe on E11 pin 7 (Position Signal) and place Channel A ground on TP7 (Integrator Ground).

8b. Version 2 of DLM: Place Channel A oscilloscope probe on TP15 (Position Signal) and place Channel A ground on TP5 (Integrator Ground).

8c. Version 3 of DLM: Place Channel A oscilloscope probe on TP15 (Position Signal) and place Channel A ground on TP5 (Integrator Ground).

9. Observe the waveform in Figure 3-10(a) while manually moving the carriage back and forth.

10. Measure the peak-to-peak deviation of the Position Signal amplitude about the ground reference. It should be 3.7 ± 0.7 volts.

NOTE
1. If these amplitudes are not within tolerance, the head load operation would most likely fault.

2. Look at the servo data waveforms at TP2 of the Read/Write module for a smooth sinusoidal waveform, as in Figure 3-10(b). If something like Figure 3-10(c) is seen, the head azimuth angle is wrong. In this case, replace the Read/Write head.

3. If the head azimuth is good, then check to see if the +8Vdc voltages are out of tolerance (Paragraph 3.2).

POSITION SIGNAL

GND. REF.

(A)

TIME = 5 MS/DIV.
VOLTS = 1 VOLT/DIV.

(B)

(SMOOTH SINUSOID)

(C)

(REPLACE HEAD)
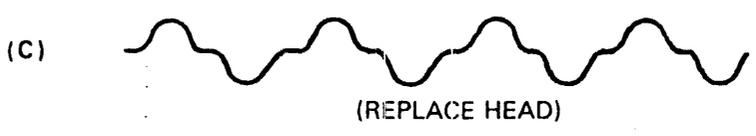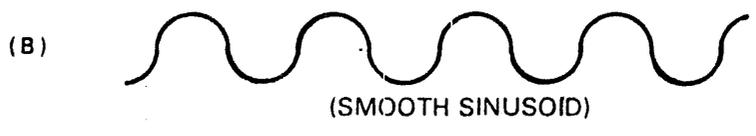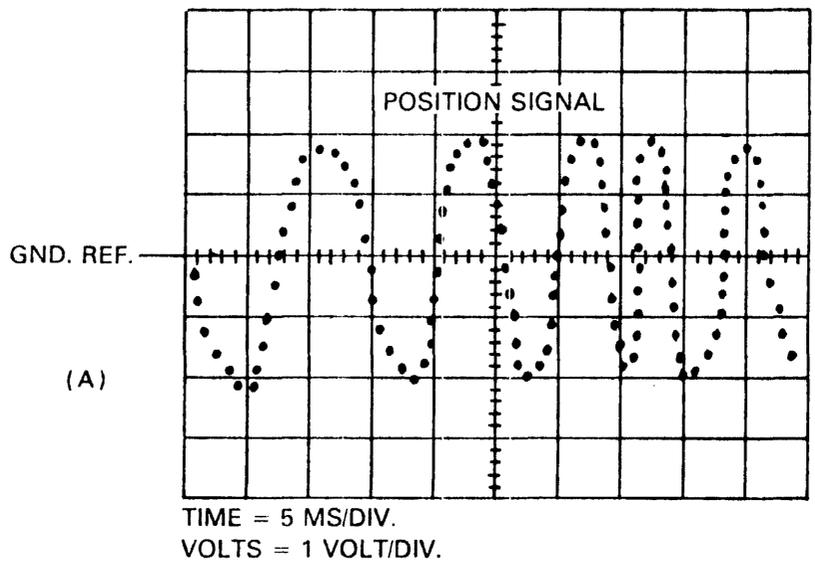
CZ-1069

Figure 3-10   Position Signal Gain Check Waveforms

3.10 TACHOMETER AC NOISE PICK-UP CHECK
This procedure checks the amount of noise being picked up by the tachometer. If the noise is excessive, the positioner will have a hard time holding onto a track signal. In this case, the READY light may flicker.

A. Required Tools:

1. Oscilloscope with probe and ground leads
2. DIP clip
3. Jumper.

B. Check:

1. Remove both top cover assemblies.

2. Place the Read/Write module up and out of the way of the carriage assembly.

3. Defeat cover interlock (Table 3-1).

4. Install cartridge.

5. Depress LOAD switch.

6. Wait for heads to load onto the pack.

7. Disable servo drive to the carriage by disconnecting the in-line connector (Figure 3-4).

8. Set the oscilloscope (sync internally) as follows:

    a. Channel A probe should be on TP1 of the DC Servo Module (Summing Amp).

    b. Channel A ground should be on TP11 of the DC Servo Module (Signal Ground).

9. Each drive's summing amplifier output at this point will look slightly different, but it should be similalr to the waveform shown in Figure 3-11.

10. The signal seen should have a peak-to-peak value of no more than 600 mv.

11. If the signal is out of tolerance, the DC Servo module could be bad or the drive motor may be too noisy. Replace the module, and if that does not solve the problem, replace the drive motor (see Chapter 2).
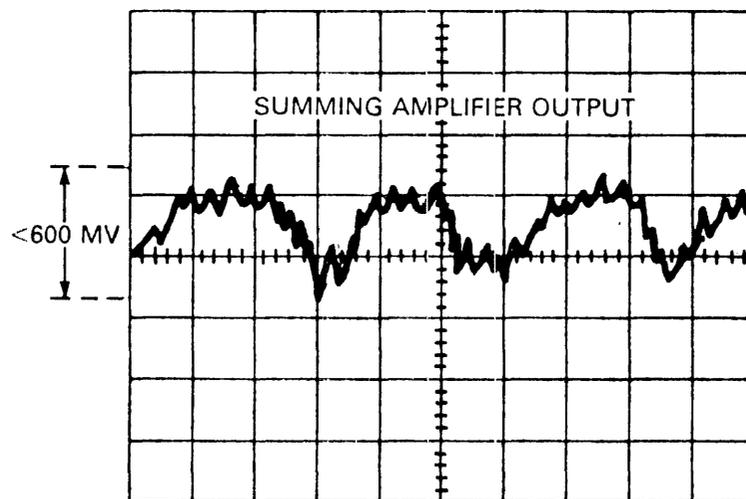
Figure 3-11 Summing Amplifier Output

3.11 VELOCITY PROFILE CHECK

By causing the positioner to perform an oscillating seek, the velocity profile can be checked for duration, amplitude and waveshape.

    A.   Required Tools:

        1.   Oscilloscipe with probe and ground leads
        2.   Toggle-in oscillating seek program (Appendix C)
        3.   DIP clip
        4.   Jumper.

    B.   Check:

        1.   Remove both top cover assemblies.

        2.   Install cartridge.

        3.   Defeat top cover interlock (Table 3-1).

        4.   Depress LOAD switch.

        5.   Wait for heads to load onto the pack.

        6.   Using the oscillating program shown in Appendix C, cause an oscillating seek from track 0 to track 255 (RL01) or track 511 (RL02).

       7a. Version 1 of DLM: Place the Channel A oscilloscope probe on TP12, place the Channel A ground on any of the DLM ground points (TP1 through TP6 are ground) and place the external trigger on E38 pin 12 (SIGN FWD).

       7b. Version 2 of DLM: Place the Channel A oscilloscope probe on TP8, place Channel A ground on any of the DLM ground test points (TP1 through TP4 are ground) and place the external trigger on E25 pin 12 (SIGN FWD).

       7c. Version 3 of DLM: Place the Channel A oscilloscope probe on TP8, place the Channel A ground on any of the DLM ground points (TP1 through TP4 are ground) and place the external trigger on E25 pin 12 (SIGN FWD).

        8.   Set the oscilloscope to sync internal, positive-going and observe the waveform shwon in Figure 3-12.

        9.   The peak amplitude of the waveform should be between 4.6 and 5.0 volts.

TACHOMETER OUTPUT VELOCITY SIGNAL

4.6 TO
5.0 V

4.6 TO
5.0 V

← 80 TO 86 MS →
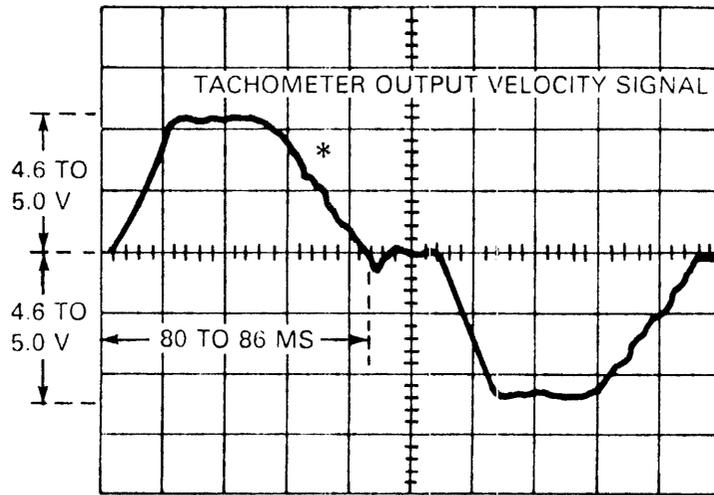
TIME = 20 MS/DIV.
VOLTS = 2V/DIV.

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Figure 3-12   Tachometer Output Velocity Signal

10. The maximum seek time should be between 80 and 86 milliseconds.

11. Observe the trailing edge of the waveform (as indicated by an asterisk In Figure 3-12). There should be a slight "stepping" slope. If the observed slope has spikes in it, the positioner needs replacing as it is not rolling smoothly.

12. If the other specifications (in Steps 9 and 10) cannot be met, the DC Servo module is probably at fault.

3.12 SERVO DRIVE MOTOR CURRENT CHECK
One possible cause of seek errors is excessive drive motor current. This check will determine if there is too much current.

A. Required Tools:

1. Oscilloscope with probes and ground leads
2. Toggle in oscillating seek program (Appendix C)
3. DIP clip
4. Jumper.

B. Check:

1. Remove both top cover assemblies.

2. Defeat top cover interlock (Table 3-1).

3. Install cartridge.

4. Depress LOAD switch.

5. Wait for heads to load onto the pack.

6. Using the oscillating seek program listed in Appendix C, cause an oscillating seek from track 0 to track 255 (RL01) or track 511 (RL02).

7. Place Channel A oscilloscope probe on TP3 of the DC Servo module.

8a. Version 1 of DLM: Place the external trigger on E38 pin 12 (SIGN FWD).

8b. Version 2 of DLM: Place the external trigger on E25 pin 12 (SIGN FWD).

8c. Version 3 of DLM: Place the external trigger on E25 pin 12 9SIGN FWD).

9. Observe the waveform shown in Figure 3-13.

POSITIONER MOTOR CURRENT

GND. REF.

TIME = 20MS/DIV.
VOLTS = 500MV/DIV.

CZ-1072
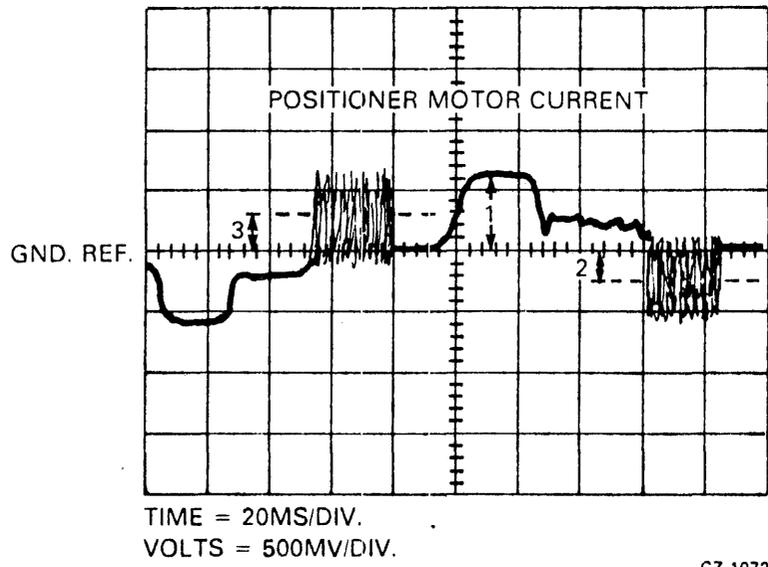
Figure 3-13   Positioner Motor Current Check

10. Measure the points called out in the figure and compare them to the following:

#1 should be between 750 and 780 mv.
#2 and #3 should be less than or equal to 500 mv.

11. Failure to meet specifications requires replacement of the positioner/drive motor assembly (described in Chapter 2).

3.13 ACCESS TIME CHECK

The access time is checked by performing oscillating seeks and observing the Position Signal and "Ready to Read/Write".

A. Required Tools:

1. Oscilloscope with probes and ground leads
2. Toggle-in oscillating seek program (Appendix C)
3. DIP clip
4. Jumper.

B. Check:

1. Remove both top cover assemblies.

2. Defeat the top cover interlock (Table 3-1).

3. Install cartridge.

4. Depress LOAD switch.

5. Wait for heads to load onto the pack.

6. Using the oscillating seek program shown in Appendix C, issue a one track seek.

7a. Version 1 of DLM: Place Channel A oscilloscope prove on E25 pin 12 (Ready to Read/Write).

7b. Version 2 of DLM: Place Channel A oscilloscope probe on TP16 (Ready to Read/Write).

7c. Version 3 of DLM: Place Channel A oscilloscope probe on TP16 (Ready to Read/Write).

8. Observe the waveform depicted in Figure 3-14.

9. Measure the time the "Ready to Read/Write" signal is low. It should be less than or equal to 15 milliseconds.
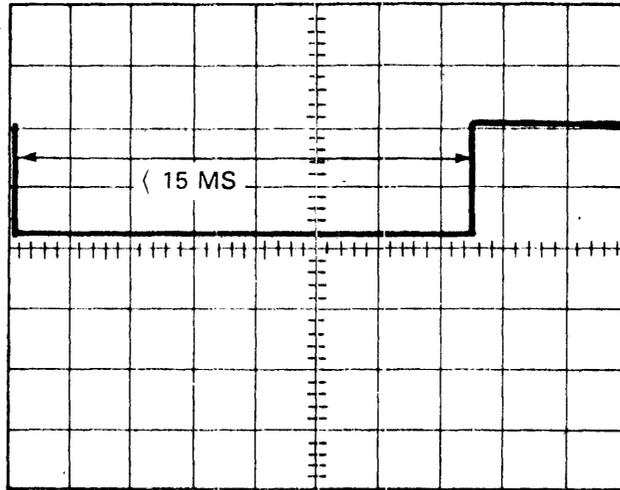
TIME = 2 MS/DIV
VOLTS = 2 V/DIV

CZ-2063

Figure 3-14   Access Time Check (One Track Seek)

10.   Issue a seek from track 0 to track 85 (RL01) or track
      170 (RL02) and check to see that "Ready to Read/
      Write" is low for slightly less than 55 milliseconds.
      See Figure 3-15.

11.   Issue a seek from track 0 to track 255 (RL01) or
      track 511 (RL02) and check to see that "Ready to
      Read/ Write" is low for slightly less than 100
      milliseconds. See Figure 3-16.

12.   If the specifications are not met, the DLM could be
      at fault, or the positioner itself may be binding due
      to excessive friction. (See Paragraph 3-12.)
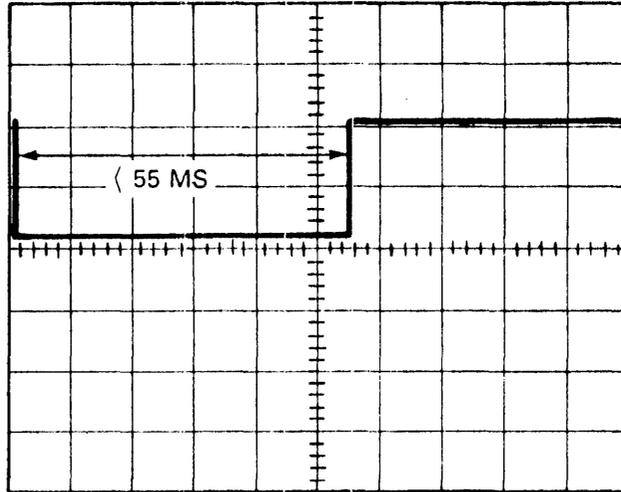
TIME = 10MS/DIV

VOLTS = 2V/DIV

CZ-2064

Figure 3-15   Access Time Check (85 Track Seek)
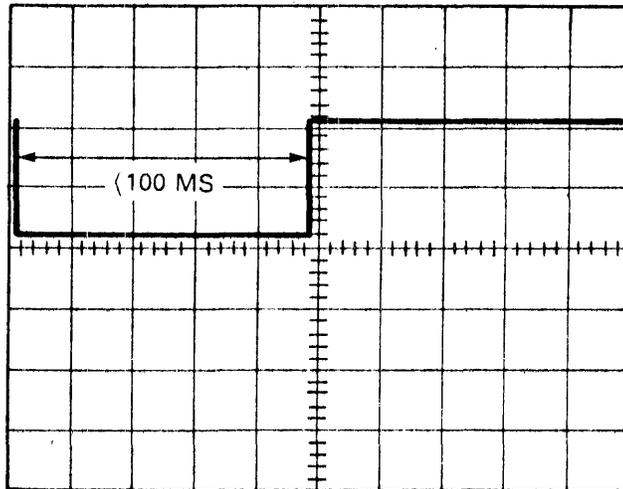
TIME = 20 MS/DIV
VOLTS = 2 V/DIV

CZ-2065

Figure 3-16   Access Time Check (255 Track Seek)

APPENDICES

APPENDIX A - REGISTER SUMMARY

APPENDIX B - INSTALLATION

APPENDIX C - TOGGLE-IN PROGRAMS

APPENDIX D - RL11 CONFIGURATION AND INSTALLATION
           CONSIDERATIONS

A.1   RL11/RLV11 ADDRESSABLE REGISTERS

Table A-1   Controller Addressable Registers

Address (octal)	Type (read/write)	Register Name/Mnemonic	Basic Function
774400	R/W	Control Status (CS)	Indicates drive ready condition; decodes drive commands and provides overall control functions and error indications.
774402	R/W	Bus Address (BA)	Indicates memory location involved in data transfer during a normal read or write operation.
774404	R/W	Disk Address (DA)	(1) Holds disk address during a data transfer such as Read or Write; or (2) holds the drive command word for a Seek command; or (3) holds the drive command word for a Get Status command
774406	R/W	Multipurpose (MP)	(1) Functions as word counter when transferring read/write data between Unibus and drives; or (2) acts as storage buffer when reading drive status; or (3) stores header information from controller silo when executing a read header command.

A.1.1 Control Status Register

CONTROL STATUS REGISTER (CSR)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ERR	DE	NXM	E2	E1	E0	DS1	DS0	CRDY	IE	BA17	BA16	F2	F1	F0	DRD

READ ONLY   READ/WRITE   REA ONL

CZ-20

Bit(s)	Name	Function
0	Drive Ready (DRDY)	When set, this bit indicates that the selected drive is ready to receive a command. The bit is cleared when a Seek operation is initiated and set when the Seek operation is completed.
1-3	Function Code	These bits are set by software to indicate the command to be executed.

F2	F1	F0	Command	Octal Code
0	0	0	No Op (RL11) or Maint. (RLV11)	0
0	0	1	Write Check	1
0	1	0	Get Status	2
0	1	1	Seek	3
1	0	0	Read Header	4
1	0	1	Write Data	5
1	1	0	Read Data	6
1	1	1	Read Data Without Header Check	7

Command execution requires that bit 7 (Controller Ready) be cleared by software. A zero transferred into bit 7 of the CSR can be considered as a Go bit.

4-5	Bus Address Extension Bits (BA16, BA17)	The two most significant bus address bits. Read and written as data bits 4 and 5 of the CS register but considered as address bits 16 and 17 of the bus address register.

Bit(s)	Name	Function
6	Interrupt Enable (IE)	When this bit is set by software, controller is allowed to interrupt the processor at the normal command or error termination.
7	Controller Ready (CRDY)	When cleared by software, this bit indicates that the command in bits 1-3 is to be executed. When set, this bit indicates the controller is ready to accept another command.
8-9	Drive Select (DS0, DS1)	These bits determine which drive will communicate with the controller via the drive bus.
10	Operation Incomplete (OPI)	When set, this bit indicates that the current command was not completed within 200 ms.
11	Data CRC (DCRC) or Header CRC (HCRC) or Write Check (WCE)	If OPI (bit 10) is cleared and this bit is set, a CRC error has occurred when reading the data (DCRC).

If OPI (bit 10) is set and bit 11 is also set, the CRC error has occurred on the header (HCRC).

If OPI (bit 10) is cleared and bit 11 is set and the function command was a Write Check, a Write Check error (WCE) has occurred. |

Bit(s)	Name	Function
12	Data Late (DLT) or Header Not Found (HNF)	This bit is set during a Write when the silo is empty but the word count has not yet reached zero (meaning that the bus request was ignored for too long). The OPI bit will not be set. This bit will be set during a read when the silo is full (meaning that the word being read could not enter the silo and the bus request has been ignored for too long). The OPI bit will not be set. When this bit and OPI are both set, a 200 ms timeout occurred while the controller was searching for the correct sector to read or write (no header compare - HNF).

Error Summary

Error	Bits 12	Bits 11	Bits 10
OPI	0	0	1
Read Data CRC	0	1	0
Write Check	0	1	0
Header CRC	0	1	1
Data Late	1	0	0
Header Not Found	1	0	1

Bit(s)	Name	Function
13	Non-Existent Memory (NXM)	This bit is set when the addressed memory does not respond within the proper time frame during a direct memory access (DMA) data transfer.
14	Drive Error (DE)	This bit is tied directly to the DE interface line. When set, it indicates that the selected drive has flagged an error. (The source of the error can be determined by executing a Get Status command.) DE can be cleared by executing a Get Status command with bit 3 of the DA register set.

Bit(s)	Name	Function
15	Composite Error	When set, this bit indicates that one or more of the error bits (bits 10-14) is set. If the IE bit (bit 6 of CS) is set and an error occurs (which sets bit 7), an interrupt will be initiated.

A.1.2 Bus Address Register

BUS ADDRESS REGISTER (BAR)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8	BA7	BA6	BA5	BA4	BA3	BA2	BA1	0

READ/WRITE

CZ-2035

Bit(s)	Name	Function
0-15	BA0 thru BA15	These bits point to the Unibus address that data is to be transferred to/from. Normally a memory address, BA16 and BA17 are in the CSR bits 4 and 5.

A.1.3 Disk Address Register

A.1.3.1 Disk Address Register During a Seek Command

DAR DURING SEEK COMMAND

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DF8	DF7	DF6	DF5	DF4	DF3	DF2	DF1	DF0	0	0	HS	0	DIR	0	1

CZ-2010

Bit(s)	Name	Function
0	—	Must be a 1.
1	—	Must be a 0.

Bit(s)	Name	Function
2	Direction (DIR)	This bit indicates the direction in which a Seek is to take place. When the bit is set, the heads move toward the spindle (to a higher cylinder address). When the bit is cleared, the heads move away from the spindle (to a lower cylinder address). The actual distance moved depends on the cylinder address difference (bits 7-15).
3	-	Must be a 0.
4	Head Select (HS)	Indicates which head (disk surface) is selected. A one indicates the lower head; a zero, the upper head.
5-6	-	Reserved.
7-15	Cylinder Address Difference DF 08:00	Indicates the number of cylinders the heads are to move on a seek.

A.1.3.2 Disk Address Register During Read or Write Data Command

DAR DURING READING OR WRITING DATA COMMANDS

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	HS	SA5	SA4	SA3	SA2	SA1	SA0

CZ-2011

Bit(s)	Name	Function
0-5	Sector Address SA 05:00	Address of one of the 40 sectors on a track.
6	Head Select (HS)	Indicates which head (disk surface) is to be selected. A one indicates the lower head; a zero, the upper head. The correct track (head and cylinder) must be previously selected by a Seek.
7-15	Cylinder Address CA 08:00	Address of the cylinders being accessed.

A.1.3.3 Disk Address Register During a Get Status Command

DAR DURING GET STATUS COMMAND

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X	0	0	0	0	RST	0	1	1

CZ-2037

Bit(s)	Name	Function
0	–	Must be a 1.
1	Get Status (GS)	Must be a 1, indicating to the drive that the status word is being requested. At the completion of the Get Status command, the drive status word is read into the controller Multipurpose (MP) register.
2	–	Must be a 0.
3	Reset (RST)	When this bit is set, the drive clears its error register before sending a status word to the controller.
4-7	–	Must be a 0.
8-15	–	Not used during a Get Status.

A.1.4 Multipurpose Register

A.1.4.1 Multipurpose Register During a Get Status Command

MPR AFTER GET STATUS COMMAND

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WDE	CHE	WL	SKTO	SPE	WGE	VC	DSE	DT	HS	CO	HO	BH	STC	STB	STA

CZ-2012

A-7

Bit(s)	Name	Function
0-2	State C:A ST C:A	These bits define the state of the drive.

	C	B	A	
	0	0	0	Load Cartridge
	0	0	1	Spin Up
	0	1	0	Brush Cycle
	0	1	1	Load Heads
	1	0	0	Seek (Track Counting)
	1	0	1	Lock On (Keeping on track)
	1	1	0	Unload Heads
	1	1	1	Spin Down

Bit(s)	Name	Function
3	Brush Home (BH)	Set when the brushes are home.
4	Heads Out (HO)	Set when the heads are over the disk.
5	Cover Open (CO)	Set when the cartridge access cover is open or the dust cover is not in place.
6	Head Select (HS)	Indicates the currently selected head. A zero indicates the upper head; a one, the lower head.
7	Drive Type (DT)	A zero indicates an RL01; a one, an RL02.
8	Drive Select Error (DSE)	Set when a multiple drive selection is detected.
9	Volume Check (VC)	Set when a cartridge is spun-up. Cleared by execution of a Get Status command with Bit 3 asserted.
10	Write Gate Error (WGE)	Set during Write Gate if one or more of the following conditions occur.

o Drive is not "Ready to Read/Write"
o Drive is Write Protected
o Sector pulse is occurring
o Drive has another error

Bit(s)	Name	Function
11	Spin Error (SPE)	Set when spindle has not reached speed in the required time during spin-up or when spindle speed is too high.

Bit(s)	Name	Function
12	Seek Time Out (SKTO)	Set when the heads do not come on track in the required time during a Seek command or when "Ready to Read/Write" is lost while the drive is in position (lock-on) mode.
13	Write Lock (WL)	Set when the drive is Write Protected.
14	Current Head Error (CHE)	Set if write current is detected in the heads when Write Gate is not asserted.
15	Write Data Error (WDE)	Set if Write Gate is asserted but no transitions are being detected on the Write Data line.

A.1.4.2 Multipurpose Register During a Read Header Command

MPR AFTER READ HEADER COMMAND

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	HS	SA5	SA4	SA3	SA2	SA1	SA0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ZEROES															

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CRC															
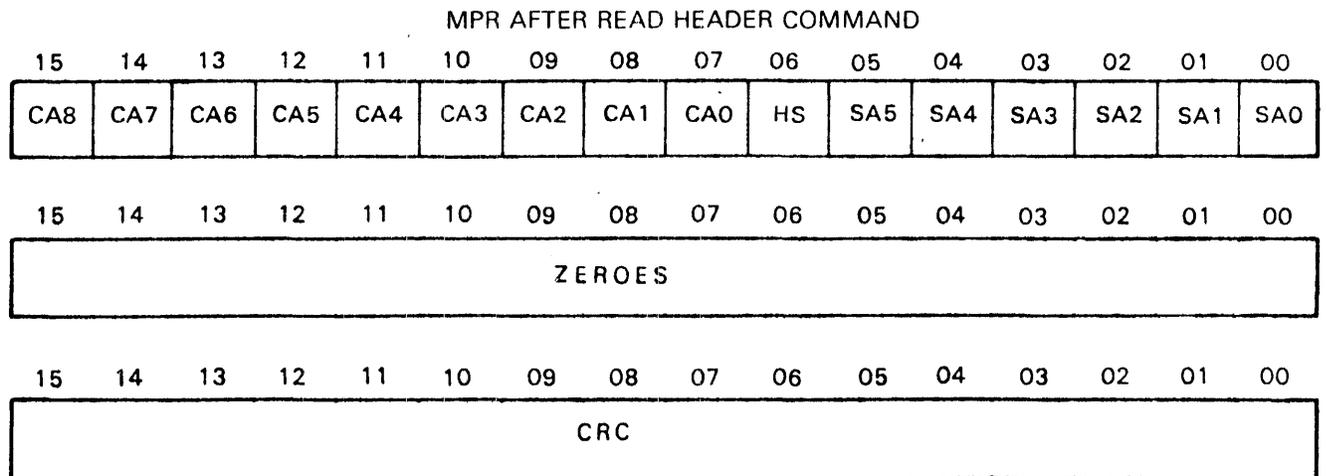
CZ-2013

Bit(s)	Name	Function
0-5	SA0:SA5	Sector Address
6	HS	Head Select - Upper head = 0, lower head = 1
7-15	CA0:CA8	Cylinder Address

A.1.4.3 Multipurpose Register During Read/Write Data Commands

MPR DURING READ/WRITE COMMANDS FOR WORD COUNT

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	1	1	WC12	WC11	WC10	WC9	WC8	WC7	WC6	WC5	WC4	WC3	WC2	WC1	WC0

CZ-2036

Bit(s)	Name	Function
0-12	Word Count WC 12:00	Contains the two's complement of total number of words to be transferred.
13-15		Must be ones.

MP Register Programming Note — The RL01/RL02 Disk Drive will not do spiral read/writes. If data is to be transferred past the end of the last sector of a track, it is necessary to break up the operation into the following steps.

1. Program the data transfer to terminate at the end of the last sector of the track.

2. Program a seek to the next track. This can be either a head switch to the other surface but same cylinder or a head switch and move to the next cylinder.

3. Program the data transfer to continue at the start of the first sector at the next track.

A.2   RL8-A ADDRESSABLE REGISTERS

Table A-2   RL8-A Instruction Set

OCTAL CODE *	MNEMONIC	FUNCTION
6600	RLDC	Clear controller, all registers, AC and flags. (Do not use to terminate a disk function.)
6601	RLSD	Skip on function done, then clear if set to a one
6602	RLMA	Load Break MA Register from AC 0:11
6603	RLCA	Load Command Register A from AC 0:11
6604	RLCB	Load Command Register B from AC 0:11, execute command
6605	RLSA	Load Sector Address Register from AC 0:5
6607	RLWC	Load Word Count Register from AC 0:11
6610	RRER	Read Error Register into AC 0, 1, 2, 10, 11
6611	RRWC	Read Word Count Register into AC 0:11
6612	RRCA	Read Command Register A into AC 0:11
6613	RRCB	Read Command Register B into AC 0:11
6614	RRSA	Read Sector Address Register into AC 0:5
6615	RRSI	Read silo word into AC 0:11
6617	RLSE	Skip on composite error, then clear if set to a one

*Alternate device code, 62 and 63

A.2.1   Command Register A

A.2.1.1   Command Register A During a Seek Command

COMMAND REGISTER A DURING A SEEK COMMAND

00	01	02	03	04	05	06	07	08	09	10	11
DIR	HS	X	MSB								LSB

CYLINDER DIFFERENCE

CZ-2016

Bit(s)	Name	Function
AC0	Direction (DIR)	This bit indicates the direction in which a Seek is to take place. When the bit is set, the heads move toward the spindle (to a higher cylinder address). When the bit is cleared, the heads move away from the spindle (to a lower cylinder address). The actual distance moved depends on the cylinder address difference (bits 3-11).
AC1	Head Select (HS)	Indicates which head (disk surface) is to be selected. A one indicates the lower head; a zero, the upper head.
AC2	–	Spare
AC3:11	Cylinder Address Difference	Indicates the number of cylinders the heads are to move on a seek.

A.2.1.2   Command Register A During Read or Write Data Command

COMMAND REGISTER A DURING A READ/WRITE DATA COMMAND

00	01	02	03	04	05	06	07	08	09	10	11
0	HS	0	MSB								LSB

CYLINDER ADDRESS
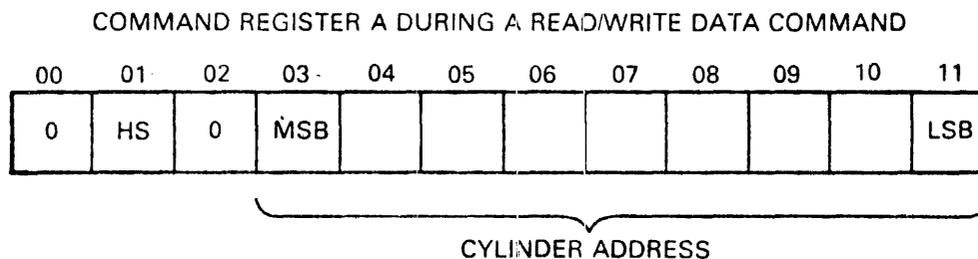
CZ-2017

Bit(s)	Name	Function
AC0	–	Must be zero
AC1	Head Select (HS)	Indicates which head (disk surface) is to be selected. A one indicates the lower head; a zero, the upper head. The correct track (head and sector) must be previously selected by a Seek.
AC2	–	Must be zero
AC3:11	Cylinder Address	Cylinder address

A.2.2 Command Register B

COMMAND REGISTER B

00	01	02	03	04	05	06	07	08	09	10	11
RES	MAIN	MODE	IE	MSB	LSB	EMA0	EMA1	EMA2	FC	FB	FA

DRIVE SELECT
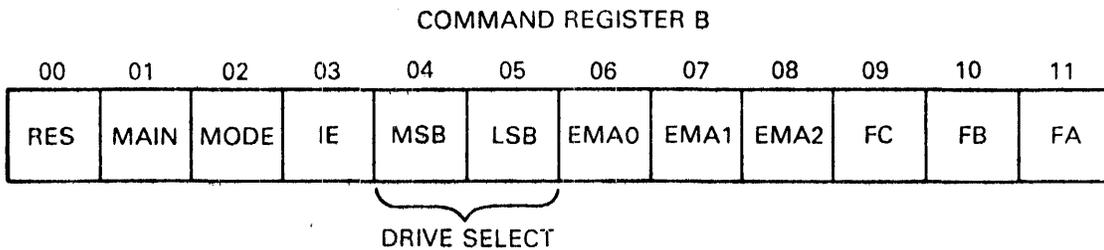
CZ-2018

Bit(s)	Name	Function
AC0	–	Reserved
AC1	Maintenance	The contents of the Disk Address (DA) Register are looped back to the silo for maintenance purposes. Bit 2 of Command Register B must also be set for this function to work correctly.
AC2	Mode	When set, this bit indicates that the data field will be 256 8-bit words per sector. When zero, the data field will be truncated to 170 12-bit words per sector. This bit must be set when a Maintenance, a Get Status or a Read Header command is to be executed.
AC3	Interrupt Enable (IE)	When this bit is set, the controller is allowed to interrupt the processor at the conculsion of a normal command or error termination.

A-13

Bit(s)	Name	Function
AC4:5	Drive Select (DS0, DS1)	These bits determine which drive will communicate with the controller via the drive bus.
AC6:8	Extended Memory Addressed (EMA)	These three bits define the memory field location. This allows up to 32K memory locations to be addressed on processors having more than 4K of memory.
AC9:11	Function Code	These bits indicate the command to be executed by the controller/disk subsystem.

Bit 9	Bit 10	Bit 11	Command
0	0	0	Maintenance
0	0	1	Reset
0	1	0	Get Status
0	1	1	Seek
1	0	0	Read Header
1	0	1	Write Data
1	1	0	Read Data
1	1	1	Read Data Without Header Check

A.2.3 Break Memory Address Register

BREAK MEMORY ADDRESS REGISTER

00	01	02	03	04	05	06	07	08	09	10	11
BM 00	BM 01	BM 02	BM 03	BM 04	BM 05	BM 06	BM 07	BM 08	BM 09	BM 10	BM 11
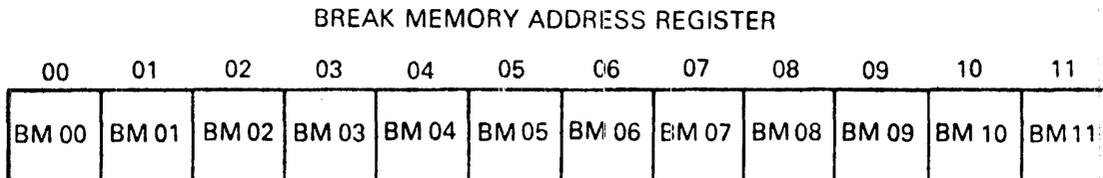
CZ-2019

Bit(s)	Name	Function
AC0:11	BM0:11	Memory Address

A.2.4 Word Count Register

WORD COUNT REGISTER

00	01	02	03	04	05	06	07	08	09	10	11
WC 00	WC 01	WC 02	WC 03	WC 04	WC 05	WC 06	WC 07	WC 08	WC 09	WC 10	WC 11

CZ-2020

Bit(s)	Name	Function
AC0:11	WCO:11	Word Count

A.2.5 Sector Address Register

SECTOR ADDRESS REGISTER

00	01	02	03	04	05
SA 00	SA 01	SA 0 2	SA 03	SA 0 4	SA 05

CZ-2021

Bit(s)	Name	Function
AC0:5	SA0:5	Sector Address

A.2.6 Error Register

ERROR REGISTER

00	01	02	03	04	05	06	07	08	09	10	11
DCRC	OPI	DLT				NOT DEFINED				DE	DRDY
HCRC		HNF									

CZ-2022

Bit(s)	Name	Function
AC0	Data CRC (DRCR) or Header CRC (HCRC)	If OPI is cleared and this bit is set, the CRC error occurred in the data (DCRC). If OPI is set and this bit is also set, the CRC error occured on the header (HCRC).
AC1	Operation Incomplete (OPI)	When set, this bit indicates that the current command was not completed withing 200 ms. It is also used in conjunction with bits 0 and 2 of this register.

A-15

Bit(s)	Name	Function
AC2	Data Late (DLT) or Header Not Found (HNF)	This bit is set during a Write if the silo is empty and the word count is not yet zero (meaning that no word was available for writing). OPI will not be set. This bit is set during a Read if the silo is full and the word count is not yet zero (meaning that the word being read could not enter the silo). OPI will not be set. When this bit and OPI are both set, then a 200 ms timeout occurred while the controller was searching for the correct sector to read or write (no header compare - HNF).
AC0:2	Error Code	Summary

Error	Bits		
	00	01	02
DLT	0	0	1
OPI	0	1	0
HNF	0	1	1
DCRC	1	0	0
HCRC	1	1	0

Bit(s)	Name	Function
AC10	Drive Error (DE)	This bit is tied directly to the Drive Error interface line. When set, it indicates that the selected drive has flagged an error. The source of the error can be determined by a Get Status. The DE bit is cleared with a Reset command to the drive.
AC11	Drive Ready (DRDY)	When set, this bit indicates that the selected drive is ready to receive a command. The bit is cleared when a Seek operation is initiated and set again when the Seek operation is completed.

A.2.7 Silo Buffer

A.2.7.1 Silo Buffer After a Get Status Command

SILO BUFFER — STATUS WORD 1

00	01	02	03	04	05	06	07	08	09	10	11
NOT DEFINED				DT	HS	CO	HO	BH	STC	STB	STA

WORD 1
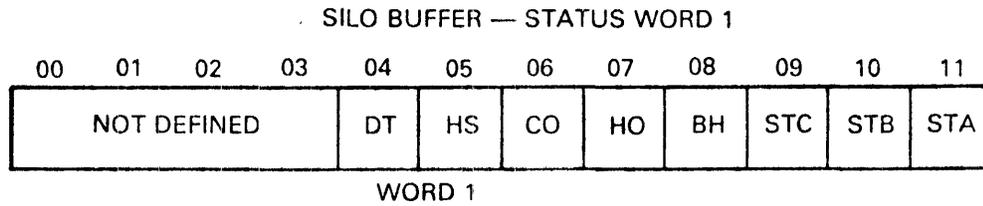
CZ-2023

Bit(s)	Name	Function
AC0:3	–	Undefined
AC4	Drive Type	A zero indicates an RL01; a one, an RL02.
AC5	Head Select (HS)	Indicates currently selected head. A zero indicates the upper head; a one, the lower head.
AC6	Cover Open (CO)	Set when the cartridge access cover is open or the dust cover is not in place.
AC7	Heads Out (HO)	A one indicates that the heads are over the disk; a zero indicates that the heads are home.
AC8	Brush Home (BH)	Set when the brushes are home.
AC9:11	State Bits	These bits define the state of the disk drive.

State Bit Definitions

Bit A	Bit B	Bit C	Definition
0	0	0	Load Cartridge
0	0	1	Spin-up
0	1	0	Brush Cycle
0	1	1	Load Heads
1	0	0	Seek (track counting)
1	0	1	Lock-on (keeping on track)
1	1	0	Unload Heads
1	1	1	Spin-down

A-17

SILO BUFFER — STATUS WORD 2

00	01	02	03	04	05	06	07	08	09	10	11
NOT DEFINED				WDE	CHE	WL	STO	SPE	WGE	VC	DSE

WORD 2
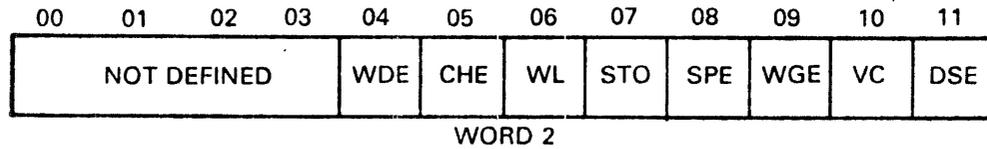
CZ-2024

Bit(s)	Name	Function
AC0:3	–	Undefined
AC4	Write Data Error (WDE)	This bit is set when Write Gate is on but no transitions were detected on the Write Data line.
AC5	Current Head Error (CHE)	This bit is set when Write Current is detected in the heads but Write Gate was not asserted.
AC6	Write Lock (WL)	Set when the drive is Write Protected.
AC7	Seek Time Out Error (SKTO)	Set when the heads do not come on track in the required time during a Seek command or when "Ready to Read/Write" is lost while the drive is in Position (lock-on) mode.
AC8	Spin Error (SPE)	Set when the spindle does not come up to speed within 40 seconds or when the spindle speed is too high.
AC9	Write Gate Error (WGE)	Set if Write Gate is asserted and one or more of the following conditions is true.

1. Drive is not "Ready to Read/Write"
2. Drive is Write Protected
3. Drive is in the midst of sector time
4. Drive has another error asserted

| AC10 | Volume Check (VC) | Set when a cartridge has been spun-up. This bit is reset by a Get Status command. |
| AC11 | Drive Select Error (DSE) | Set when one or more drives have the same number (unit select plug) or have responded to the same number. |

A.2.7.2 Silo Data Buffer During a Read Header Command

SILO BUFFER — HEADER WORDS

00	01	02	03	04	05	06	07	08	09	10	11
NOT DEFINED				LSB	HS	MSB					LSB

WORD 1

CYLINDER ADDRESS   SECTOR ADDRESS

00	01	02	03	04	05	06	07	08	09	10	11
NOT DEFINED				MSB							

WORD 2

CYLINDER ADDRESS

NOT DEFINED	0	0	0	0	0	0	0	0

WORD 3

NOT DEFINED	0	0	0	0	0	0	0	0

WORD 4

NOT DEFINED								LSB

WORD 5

HEADER CRC

NOT DEFINED	MSB							

WORD 6

HEADER CRC

CZ-2025

A-19
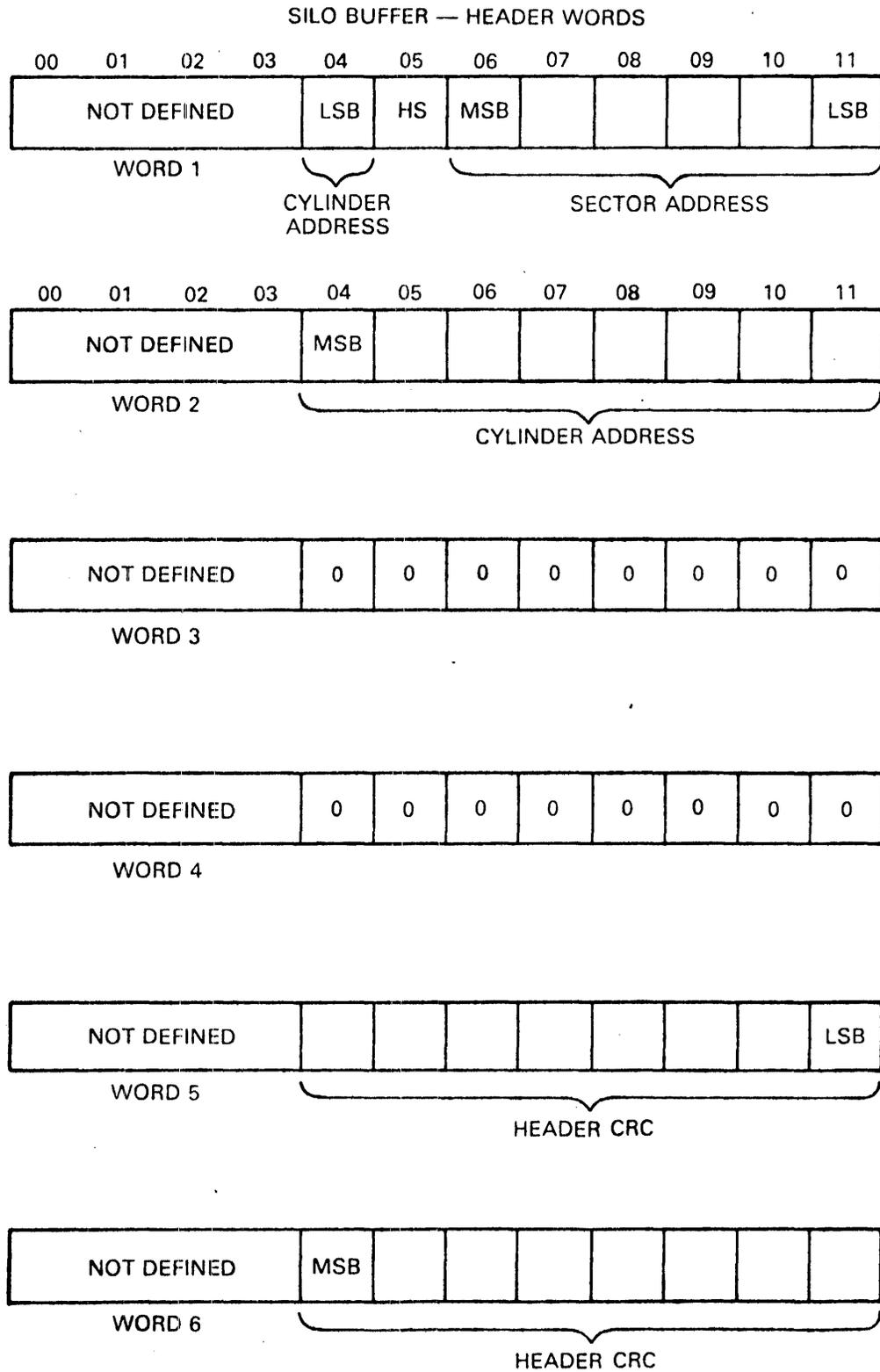
WORD 1 - HEADER

Bit(s)	Name	Function
AC0:3	-	Undefined
AC5	Cyl Add	LSB of Cylinder Address
AC5	HS	Head Select - lower head = 1, upper head = 0
AC6:11	Sec Add	Sector Address

WORD 2 - HEADER

Bit(s)	Name	Function
AC0:3	-	Undefined
AC4:11	Cyl Add	Cylinder Address - eight high order bits

WORD 3 - HEADER

Bit(s)	Name	Function
AC0:3	-	Undefined
AC4:11	-	Zeros

WORD 4 - HEADER

Bit(s)	Name	Function
AC0:3	-	Undefined
AC4:11	-	Zeros

WORD 5 - HEADER

Bit(s)	Name	Function
AC0:3	-	Undefined
AC4:11	CRC	Eight LSB of CRC word

WORD 6 - HEADER

Bit(s)	Name	Function
AC0:3	-	Undefined
AC4:11	CRC	Eight MSB of CRC word

B.1 SITE PREPARATION AND PLANNING

This appendix describes power, space, environmental, cabling and safety requirements that must be considered before installation of the RL01/RL02 Disk Subsystem.

B.1.1 Environmental Considerations

The RL01/RL02 Disk Subsystem is designed to operate in a business or light industry environment. Although cleanliness is an important consideration in the installation of any computer system, it is particularly crucial for proper operation of a disk drive. The RL01K/RL02K Disk Cartridge is not sealed while being loaded and is therefore vulnerable to dust or smoke particles suspended in the air, as well as fingerprints, hair, lint, etc. These minute obstructions can cause head crashes, resulting in severe damage to the read/write heads and disk surfaces.

B.1.1.1 Cleanliness – The RL01/RL02 Disk Drives can operate in an ambient with less than one million particles per cubic foot of air which are 0.5 micron or larger in diameter. The drive contains a filter system which, under these conditions, maintains the particle count within the cartridge below 100 particles per cubic foot.

B.1.1.2 Space Requirements – Provision should be made for service clearances of 1 m (36 in) at the front and rear of the rack or cabinet in which the drive is mounted and 1 m (36 in) at either side.

Storage space for the RL01K/RL02K cartridges should also be made available. Each cartridge has a diameter of approximately 38 cm (15 in) and a height of approximately 6 cm (2.5 in).

> **CAUTION**
> RL01K/RL02K disk cartridges must never be stacked on top of each other. A designated shelf area or specially designed disk cartridge storage unit is recommended (see the DIGITAL Supplies and Accessories Catalog).

B.1.1.3 Floor Loading – The weight of the RL01/RL02 Disk Drive alone is 34 kg (75 lb), which will not place undue stress on most floors. However, the added weight of the rack or cabinet as well as the number of drives to be installed should be considered in relation to the weight of existing computer systems. Possible future expansion should also be a consideration.

B.1.1.4   **Heat Dissipation** - The heat dissipation of each RL01/RL02 Disk Drive is 546 Btu/hour maximum. The approximate cooling requirements for the entire system can be calculated by multiplying this figure by the number of drives, adding the result to the total heat dissipation of the other system components, and then adjusting the total figure to compensate for personnel, cooling system efficiency, etc. It is advisable to allow a safety margin of at least 25 percent above the maximum estimated requirements.

B.1.1.5   **Acoustics** - Most computer sites require at least some degree of acoustical treatment. However, the RL01/RL02 Disk Subsystem should not contribute unduly to the overall system noise level. Ensure that acoustical materials used do not produce or harbor dust.

B.1.1.6   **Temperature** - The RL01/RL02 Disk Subsystem will operate over a temperature range of 10° C (50° F) to 40° C (104° F). The maximum temperature gradient is 16.6° C (30° F) per hour. The nonoperating temperature range is from -40° C (-40° F) to 66° C (151° F).

B.1.1.7   **Relative Humidity** - Humidity control is important for proper operation of any computer system since static electricity may cause memory errors or even permanent damage to logic components. The RL01/RL02 Disk Subsystem is designed to operate within a relative humidity range of 10 to 90 percent, with a maximum wet bulb temperature of 28° C (82° F) and a minimum dew point of 2° C (36° F). The nonoperating relative humidity range is from 10 to 95 percent, with a maximum wet bulb temperature of 46° C (115° F).

B.1.1.8   **Altitude** - Computer systems operating at high altitudes may have heat dissipation problems. Altitude also affects the flying height of read/write heads in disk drives. The maximum altitude specified for operating the RL01/RL02 Disk Subsystem is 2440 m (8000 ft). Also, the maximum allowable operating temperature is reduced by a factor of 1.8° C per 1000m (1° F per 1000 ft) above sea level. Thus, the maximum allowable operating temperature at 2440 m (8000 ft) would be reduced to 36°C (96° F).

B.1.1.9   **Power and Safety Precautions** - The RL01/RL02 disk subsystem presents no unusual fire or safety hazards to an existing computer system. AC power wiring should be checked carefully, however, to ensure that its capacity is adequate for the added load as well as for any possible expansion. The RL01/RL02 Disk Drive is UL listed and CSA certified.

B.1.1.10   Radiated Emissions – Any source of electromagnetic interference (EMI) that is near the computer system may affect the operation of the processor and its related peripheral equipment. Common EMI sources that are known causes of failures include:

- Thunderstorms
- Broadcast stations
- Radar
- Mobile communications
- High-voltage power lines
- Power tools
- Arc welders
- Vehicle ignition systems
- Static electricity

The effect of radiated EMI emissions on a computer system is unpredictable. Thus, grounding plays an important role in protecting the circuits used in disk drive subsystems.

To help reduce the effects of known high-intensity EMI emissions perform the following actions:

- Ground window screens and other large metal surfaces.

- Ensure that the overall computer system is grounded properly (refer to Paragraph B.14, Grounding Requirements).

- Provide proper storage (metal cabinets with doors) for disk cartridges.

B.1.1.11   Attitude/Mechanical Shock – Performance of the RL01/RL02 Disk Subsystem will not be affected by an attitude where maximum pitch and roll do not exceed 15 degrees.

The subsystem is designed to operate while a half-sine shock pulse of 10 gravity peak and 10 ± 3 ms duration is applied once in either direction of three orthagonal axes (three pulses total).

B.1.2   Options
The RL01/RL02 Disk Drive can be shipped with various controllers (for Unibus, Ommibus and LSI-11 Bus computer systems), and can be configured for 115 Vac 230 Vac operation.

Table B-1 shows saleable RL01/RL02 subsystem options. Table B-2 shows RL01/RL02 option components.

Table B-1   Saleable RLØ1/RLØ2 Subsystem Options

Option Number	Description
RLØ1A	RLØ1 Unit, BC2ØJ I/O Cable, Chassis Slide and Mounting Hardware
RLØ2A	RLØ2 Unit, BC2ØJ I/O Cable, Chassis Slide and Mounting Hardware
RLØ1-AK	RLØ1-A (Drive), RLØ1K-DC (Cartridge)
RLØ2-AK	RLØ2-A (drive), RLØ2K-DC (cartridge)
RLØ1K-DC	RLØ1 Data Cartridge
RLØ2K-DC	RLØ2 Data Cartridge
RL11-AK	RLØ1-AK, RL11 Controller, BCØ6R, Terminator
RL211-AK	RLØ2-AK, RL11 Controller, BCØ6R, Terminator
RLV11-AK	RLØ1-AK, RLV11 Controller, BCØ6R, Terminator
RLV21-AK	RLØ2-AK, RLV11 Controller, BCØ6R, Terminator
RL8A-AK	RLØ1-AK, RL8-A Controller, BCØ6R, Terminator
RL28A-AK	RLØ2-AK, RL8-A Controller, BCØ6R, Terminator

Table B-2 Saleable Cabinet Options
(Includes skins, doors, covers, trim, and power controllers)

Type	Volts	Dwg	Remarks
J950	110	H960-BC	Includes five 26.67 cm (10.5 in) high panels
	220	H960-BD	
J967	110	H967-BA	26.67 cm (10.5 in) cover panels (H950-QA) must be ordered if required.
	220	H967-BB	
H9500	110	H9603-ED	SWLB with H9514-B top covers
	220	H9603-EE	DWLB with H9514-A top covers
	110	H9601-ED	
	220	H9601-EE	SWHB complete hiboy cabinet
	110	H9602-EA	
	220	H9602-EB	DWHB complete hiboy cabinet
	110	H9600-EA	
H9500	220	H9600-EB	SWHB option arrangement dwg. Order as required.
		H9602-B-O	
		H9600-A-O	DWHB option arrangement dwg. Order as required.
		H9603-B-O	SWLB option arrangement dwg. Order as required.
H9500		H9601-A-O	DWHB option arrangement dwg. Order as required.

Saleable Cable Options: Where an I/O cable length of more than 10 feet is required, order one of the following:

Order No.	Part No.	Length
BC20J-20	7012122-20	6 m (20 ft)
BC20J-40	7012122-40	12 m (40 ft)
BC20J-60	7012122-60	18 m (60 ft)

Total length of cable(s) from the controller to the last drive must not exceed 30 m (100 ft).

B.1.3 AC Power Requirements

The RL01 or RL02 drive can operate within one of two voltage ranges that are manually selected by means of two terminal blocks located at the rear of the device (Figure B-1). These voltage ranges are:

	110 Vac	220 Vac
NOM	110-120	220-256
LO	90-105	180-210

The drive will operate when the line frequency is between 47.5 and 63 Hz.

B.1.3.1   Standard Applications — The drive can be shipped from the factory as a free-standing unit or mounted in various racks and cabinets (refer to Paragraph B.1.2, Options).

If the drive is shipped as a free-standing unit, the 2.74 m (9 ft) ac power cord is terminated with a NEMA type 5-15P plug (DIGITAL Part No. 90-08938). This plug requires a NEMA type 5-15R receptacle (Figure B-2).

B.1.3.2   Optional Applications — Operation in the high voltage range (180-256 Vac) will require reconfiguring the terminal block at the rear of the drive and changing the line cord plug (Figure B-1).

In 50 Hz applications, the line cord plug must be changed (Figure B-2).

B.1.4   Grounding Requirements

Each cabinet of a DIGITAL computer system is equipped with ground lug terminals that should be connected to a low-impedance earth ground by No. 4 AWG (5 mm/0.20 in) copper wire or stranded No. 4 AWG welding cable. A Burndy QA4C-B solderless lug (or equivalent) is recommended for terminating the cable. DIGITAL supplies a standard grounding conductor with each I/O and memory cabinet.

A steel building beam is an adequate ground in many instances. However, some disk-oriented systems may require additional connections to earth ground, in addition to the ground leads carried through various signal buses and ground connectors contained within the power cables. The green grounding wire in the power cable must also be returned to ground, usually through the conduit of the electrical distribution system. Note that the green wire is a not a current-carrying conductor, nor a neutral conductor.

Whenever possible, the system power panel must be either mounted in contact with bare building steel by bonded joints (Figure 2-3) or connected to the steel by a short length of cable.

I/O CABLE
("CABLE IN")

TERMINATOR

NORMAL/LOW
LINE VOLTAGE
TERMINAL BLOCK
COVER

CABLE "OUT"

110/220 VOLTS
TERMINAL
BLOCK COVER

AC LINECORD

CIRCUIT BREAKER
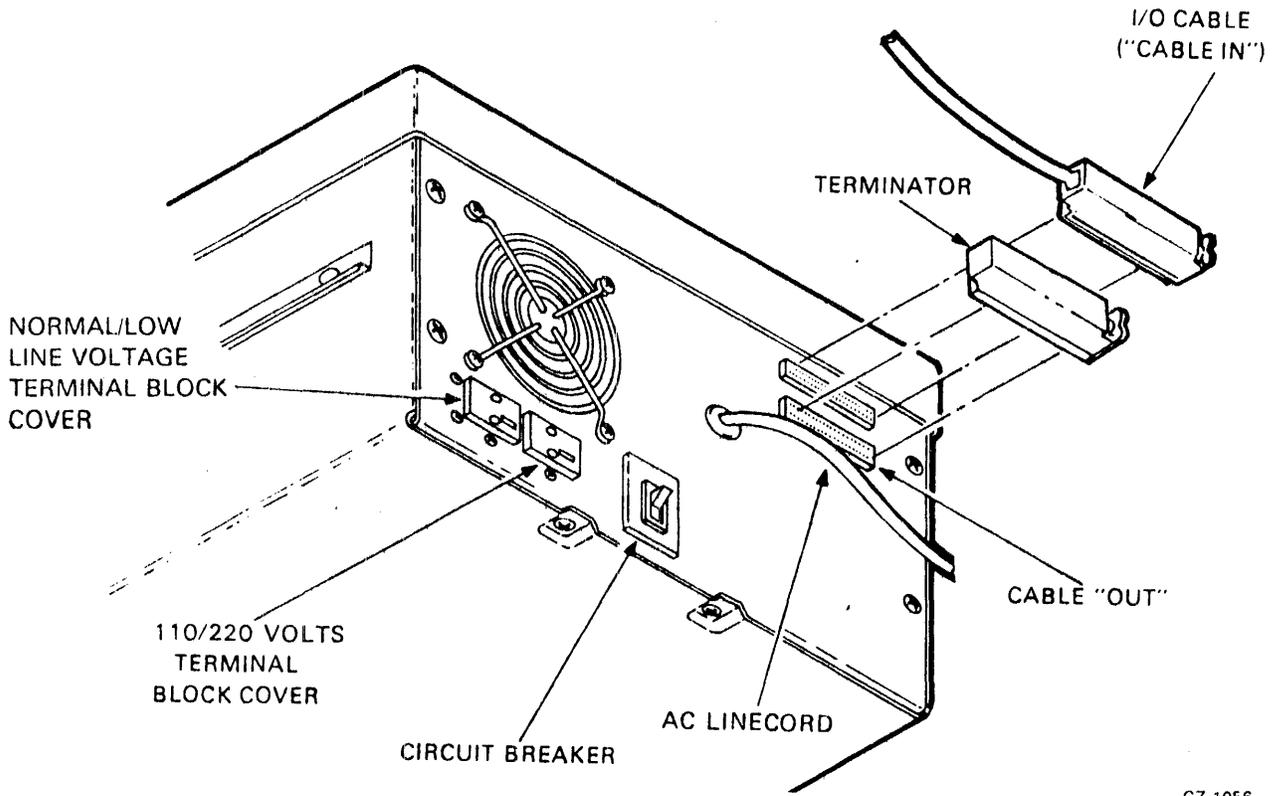
CZ-1056

Figure B-1   RL01/RL02 Disk Drive - Rear View

SOURCE	PLUG	RECEPTACLE	USED ON	
120V 15A 1-PHASE	HUBBEL #5266-C NEMA # 5-15P DEC # 90-08938	#6262 5-15R 12-05351	ALL 120 V TABLE-TOP COMPUTERS. STANDARD 120V LOW-CURRENT DISTRIBUTION. 120V TU10 UNITS. MOST 120V TERMINAL DEVICES.	POWER CONTROLLER 861-F
120/208V 30A 3-PHASE Y	HUBBEL #2611 NEMA # L5-30P DEC # 12-11193	#2610 L5-30R 12-11194	ALL 120V STANDARD CABINET MOUNTED EQPT.	POWER CONTROLLER 861-C
120/208-240V 20A 2-PHASE or 120/208V 20A 3-PHASE Y	HUBBEL #2411 NEMA # L14-20P DEC # 12-11045	#2410 L14-20R 12-11046	120V PDP-11/45 PRO-CESSOR CABINET ONLY.	POWER CONTROLLER 861-A
120/208V 20A 3-PHASE Y	HUBBEL #2511 NEMA # L21-20P DEC # 12-11209	#2510 L21-20R 12-11210	60 Hz RM 10 DRUM 60 Hz RP02/RP03/ RP04, RP05, RP06	
240V 15A 1-PHASE	NEMA # 6-15P DEC # 90-08853	6-15R 12-11204	ALL 240V TABLE-TOP COMPUTERS. STANDARD LOW-CURRENT 240V DISTRIBUTION. MOST 240V TERMINAL DEVICES. 240V TU10.	
240V 20A 1-PHASE	HUBBEL #2321 NEMA # L6-20P DEC # 12-11192	#2320 L6-20R 12-11191	ALL 240V STANDARD CABINET MOUNTED EQUIPMENT.	POWER CONTROLLER 861-B
240/416V 20A 3-PHASE Y	NEMA # -- NOT NEMA DEC # 12-09010	NOT NEMA 12-11259	60 Hz RM10 DRUM 60 Hz RP02/RP03/ RP04	
120V 30A 1-PHASE	HUBBEL #2811 NEMA L21-30P DEC 12-12314	#2810 L21-30R 12-12315	PDP11/70 PROCESSOR PDP 11/70 MEM. VAX-11/780 PROCESSOR	POWER CONTROLLER 861-D
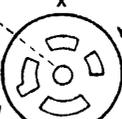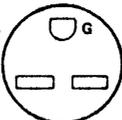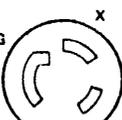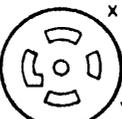
CP-1968

Figure B-2   approved Electrical Plugs and Receptacles

BUILDING STEEL
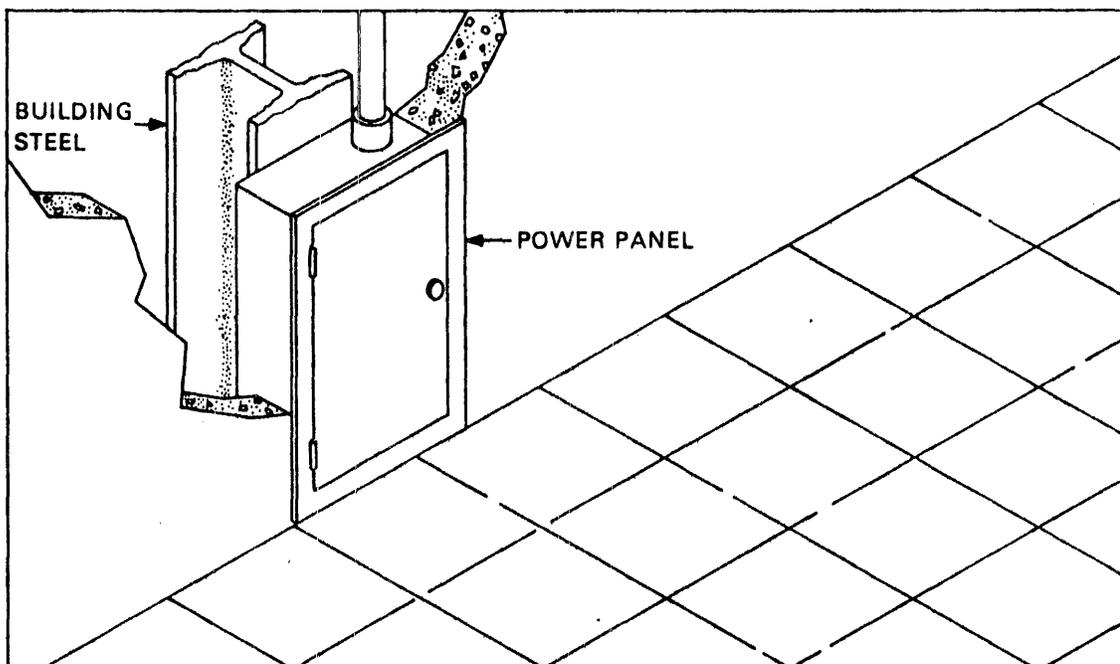
POWER PANEL

08-0717

Figure B-3   Power Panel Grounded to Building Frame

B-9

Where neither scheme is possible, a metal area (comprising the power panel, the conduit, and a metal plate) of at least 1 m^2 (10 ft^2) that is in contact with masonry must be connected to the green ground wire (Figure B-4). The connecting wire must not exceed 1.5 m (5 ft) in length and should be at least a No. 12 AWG (2mm).

When two cabinets are bolted together, DIGITAL bonds them electrically with a No. 4 AWG conductor (5 mm/0.20 in) or by several copper mesh straps connected between the cabinet frames.

After the grounding system is installed, it is advisable to take a voltage reading between the cabinet frame and the nearest grounded object. NBFU No. 70 (published by the National Bureau of Underwriters) provides further details regarding preferred grounding procedures.

B.1.5   Installation Constraints
The route from the receiving area to the installation site that the equipment will travel should be studied in advance to ensure problem-free delivery. Among the considerations are:

- Height and location of loading doors
- Size, capacity, and availability of elevators
- Number and size of aisles and doors en route
- Bends or obstructions in hallways.

B.2   AC CABLING
Computer equipment requires a power source with a minimum number of voltage and frequency disturbances. Line voltage disturbances greater than 1/4 cycle (measured at the receptacle during system operation) are undesirable.

DIGITAL power wiring conforms to Underwriters Laboratories, Inc., Handbook UL No. 478, National Electrical Code standards, and the type II requirements of the National Fire Protection Association (NFPA 70). This means that in the United States the wire used as equipment ground is green, or green with a yellow stripe; it carries no load current (except in emergency), but does carry leakage current. No equipment is permitted to leave DIGITAL that does not have a grounding connection to its frame.

The grounded conductor is light grey or white. It must not be used to ground equipment. Its purpose is to conduct current.

Lines 1, 2, and 3 in a typical 60 Hz power system (Figure B-5) are represented by black, red, and blue wires, respectively, and phase rotation is in that order.

POWER PANEL

CONCRETE
FLOOR
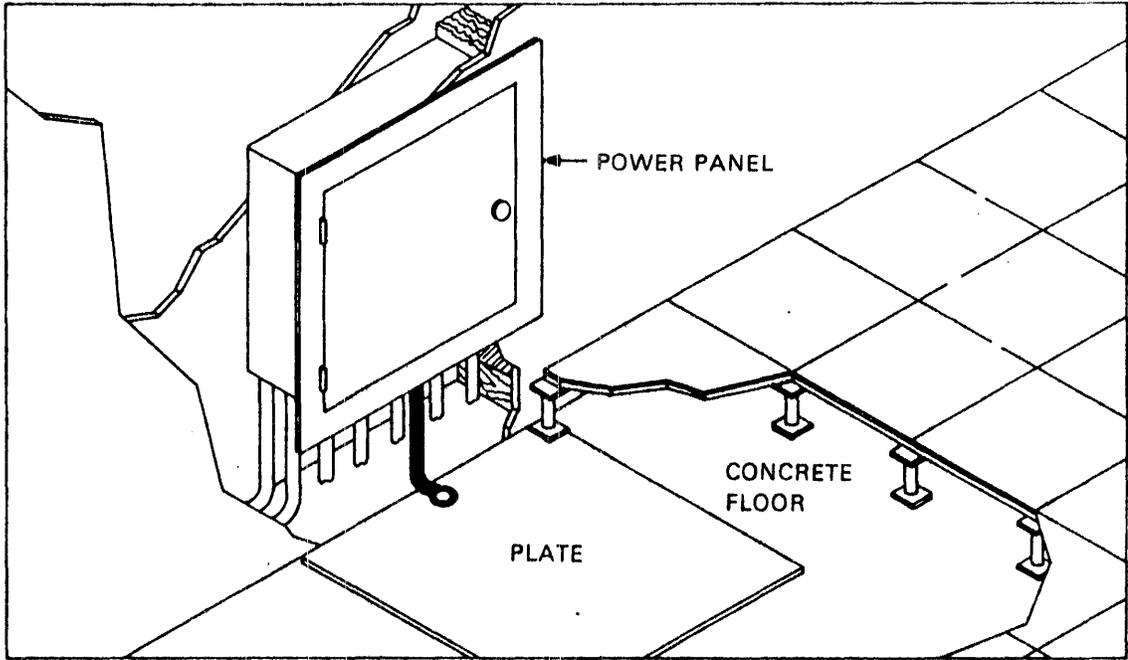
PLATE

08 - 0718

Figure B-4   Power Panel Grounded to Metal Plate

MAIN CIRCUIT
BREAKER OR
CUT-OFF CONTACTOR

PHASE A

208V   120V

PHASE B

MAIN SUPPLY
TRANSFORMER
(ONLY SECONDARY SHOWN)

208V   208V   120V

PHASE C

120V   NEUTRAL

FRAME GROUND

TO SINGLE PHASE LOADS
(TYPICAL)

TO THREE
PHASE LOADS
(TYPICAL)
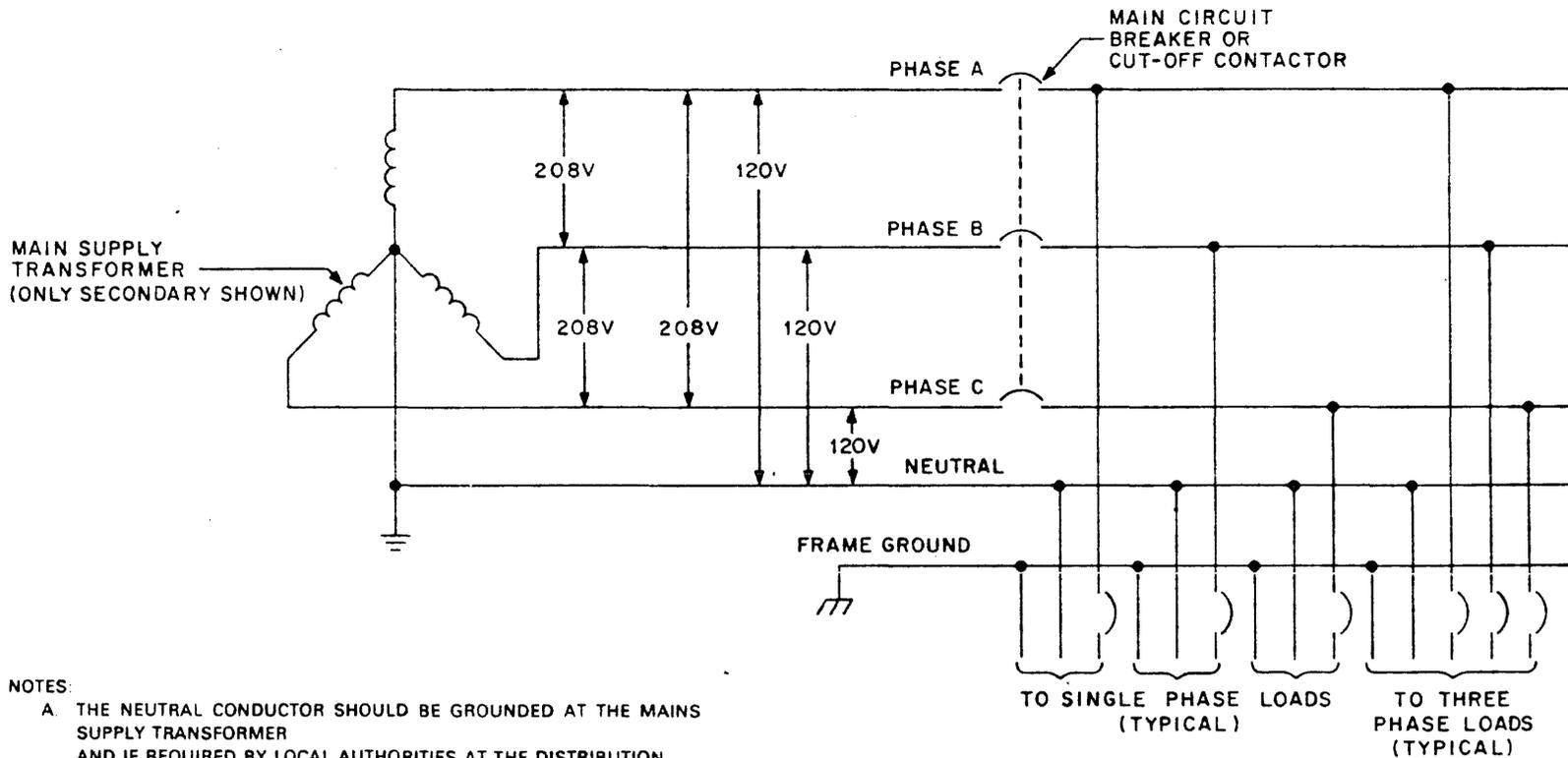
NOTES:
A. THE NEUTRAL CONDUCTOR SHOULD BE GROUNDED AT THE MAINS
   SUPPLY TRANSFORMER
   AND IF REQUIRED BY LOCAL AUTHORITIES AT THE DISTRIBUTION
   PANEL AND ELSEWHERE.

B. THE FRAME GROUND CONDUCTOR MAY CONSIST OF ELECTRICAL
   METALLIC CONDUIT OR
   RACEWAY IF APPROVED BY LOCAL AUTHORITIES.

MA-1185

Figure B-5   Typical 60Hz Power System

CAUTION
Where no grounded wire can be
guaranteed, it must not be assumed.
There are some 115 V/60 Hz systems
within the United States where neither
side of the line is grounded (115 V
3-phase delta).

Figure B-6 shows a typical 50Hz power system.

Two types of power systems can be used to provide power to the
NEMA type L14-20R receptacle. The type shown in Figure B-7 is
referred to as split-phase (or 2-phase 180 displaced) 120/240 Vac.
It comprises a center-tapped transformer with 120 Vac between the
center tap and either of the two legs. 240 Vac exists between the
two outside legs.

The second type (Figure B-8) is referred to as 3-phase Y (120
displaced) 120/280 Vac. The 120 Vac exists between neutral and any
of the three other legs (X, Y, or Z), and 208 Vac exists between
any two of the outer legs (i.e., between X and Y, X and Z, or Y
and Z). Although Figure B-8 shows the X and Y connections as the
two phases used for the receptacle, any two of the three phases
shown can be used.

The ground terminal on the L14-ZOR receptacle will normally have a
green screw, the neutral terminal will be white or silver, and the
"hot" terminal will be brass covered.

B.3   INSTALLATION - GENERAL
The controller should be installed first, followed by the
drive(s). Next, the diagnostics should be run to demonstrate that
the subsystem is functioning properly or to diagnose any problems.
Paragraph B.4 explains the installation of the RL11 Controller,
Paragraph B.5 deals with the RLV11 and Paragraph B.6 describes
RL8-A installation.

Paragraph B.7 contains instructions to install the unit and
Paragraph B.8 explains acceptance testing and contains separate
paragraphs for each of the three controllers. Paragraph B.9
describes the use of the M9312 bootstrap module that may be used
on RL11-based systems.

B.4   RL11 CONTROLLER INSTALLATION
The RL11 Controller (M7762) is a single hex-height module that can
be installed in any hex-height SPC slot. Connector J1 connects
the controller to the drive bus (Figure B-9).

Of the 21 jumpers on the RL11 Controller, five are used for
factory test purposes. The remaining 16 are for address
selection:

        W1-W6   VECTOR ADDRESS (160)
        W7-W16   BASE ADDRESS (774400)

MAIN CIRCUIT
BREAKER OR
CUT-OFF CONTACTOR

PHASE A

380/416V   220/240V

MAIN SUPPLY
TRANSFORMER
(ONLY SECONDARY SHOWN)

PHASE B

380/   380/   220/240V
416V   416V

PHASE C

220/240V

NEUTRAL

SAFETY EARTH GROUND

TO SINGLE PHASE LOADS   TO THREE
(TYPICAL)   PHASE LOADS
                               (TYPICAL)
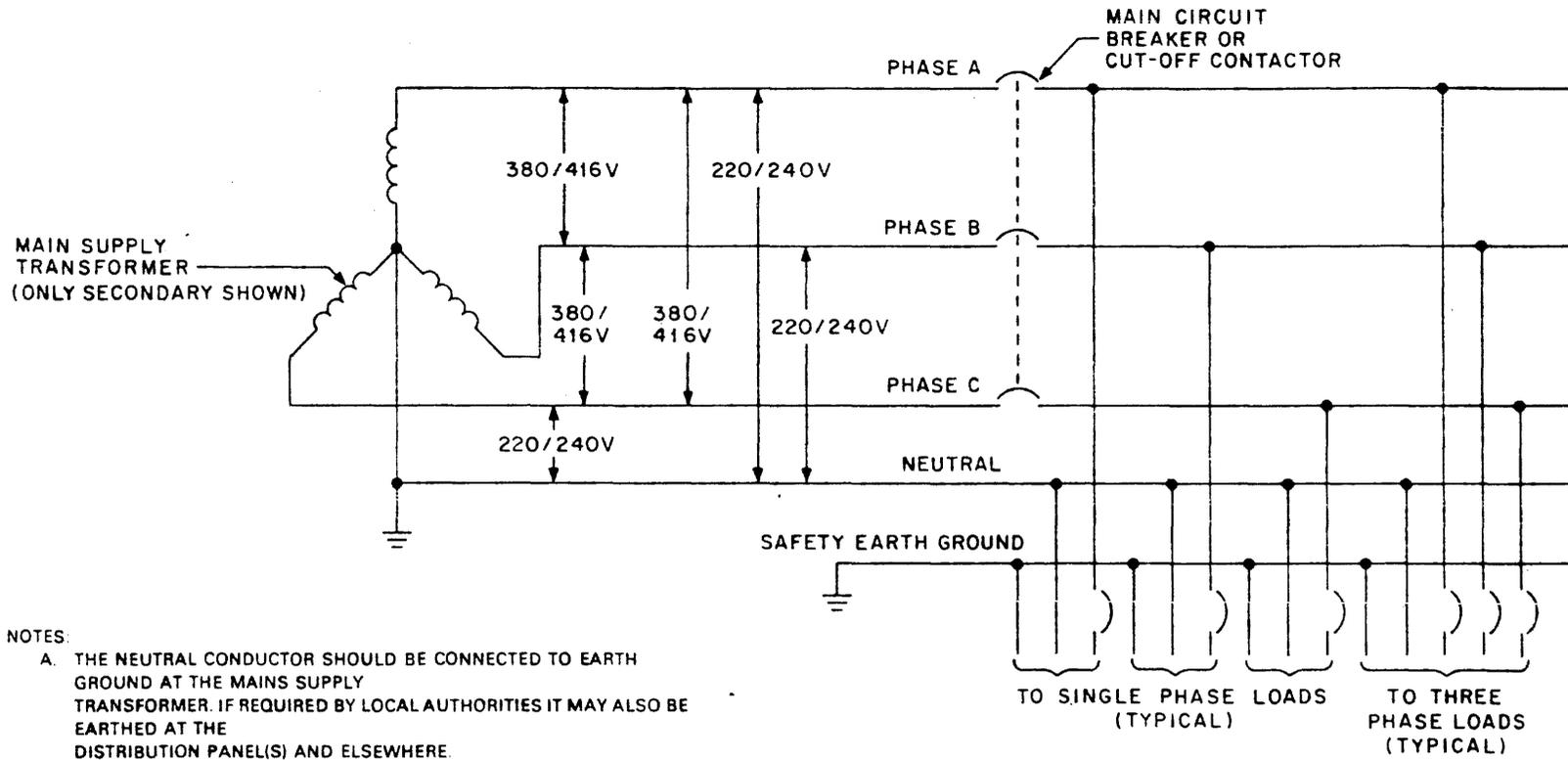
NOTES:
A. THE NEUTRAL CONDUCTOR SHOULD BE CONNECTED TO EARTH
   GROUND AT THE MAINS SUPPLY
   TRANSFORMER. IF REQUIRED BY LOCAL AUTHORITIES IT MAY ALSO BE
   EARTHED AT THE
   DISTRIBUTION PANEL(S) AND ELSEWHERE.

B. THE SAFETY EARTH GROUND CONDUCTOR MAY CONSIST OF
   ELECTRICAL METALLIC CONDUIT OR
   RACEWAY IF APPROVED BY LOCAL AUTHORITIES.

MA-1460

Figure B-6   Typical 50Hz Power System
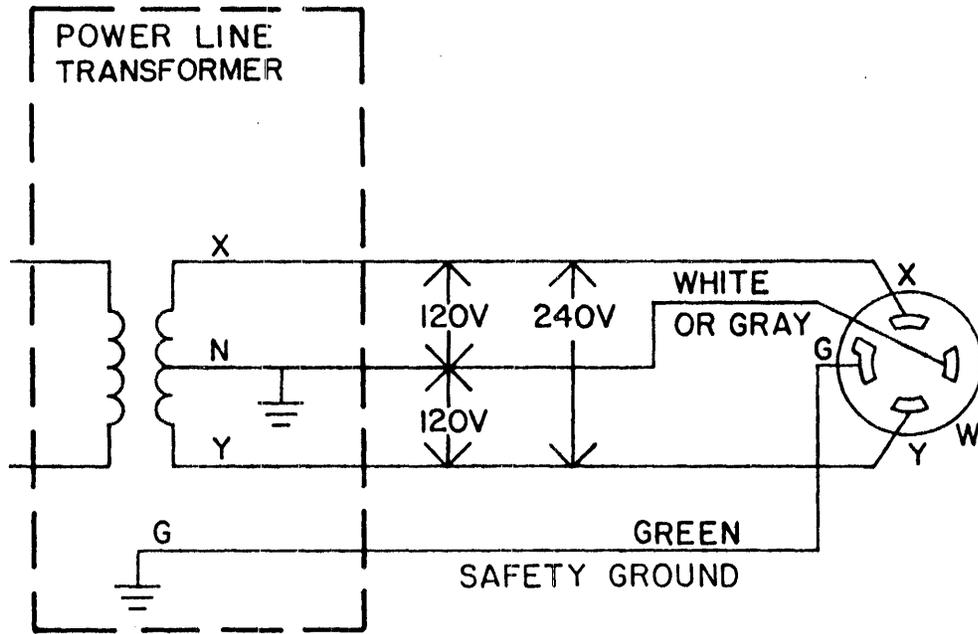
(A) 120/240V SPLIT-PHASE (TWO PHASE)

Figure B-7   Split Phase (2-Phases) Power System

POWER LINE
TRANSFORMER

Z

X

120V   208V

N

120V

Y

G

WHITE
OR
GREY

X

G

Y   W

GREEN

SAFETY GROUND
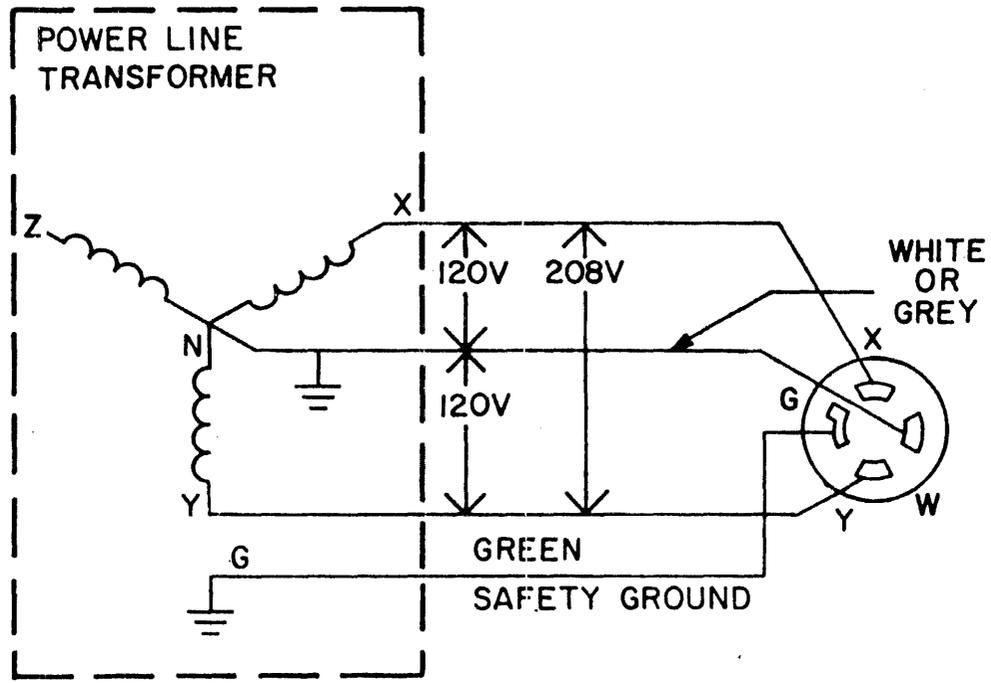
(B) 120/208V THREE PHASE

11-2294

Figure B-8   Three Phase Y Power System
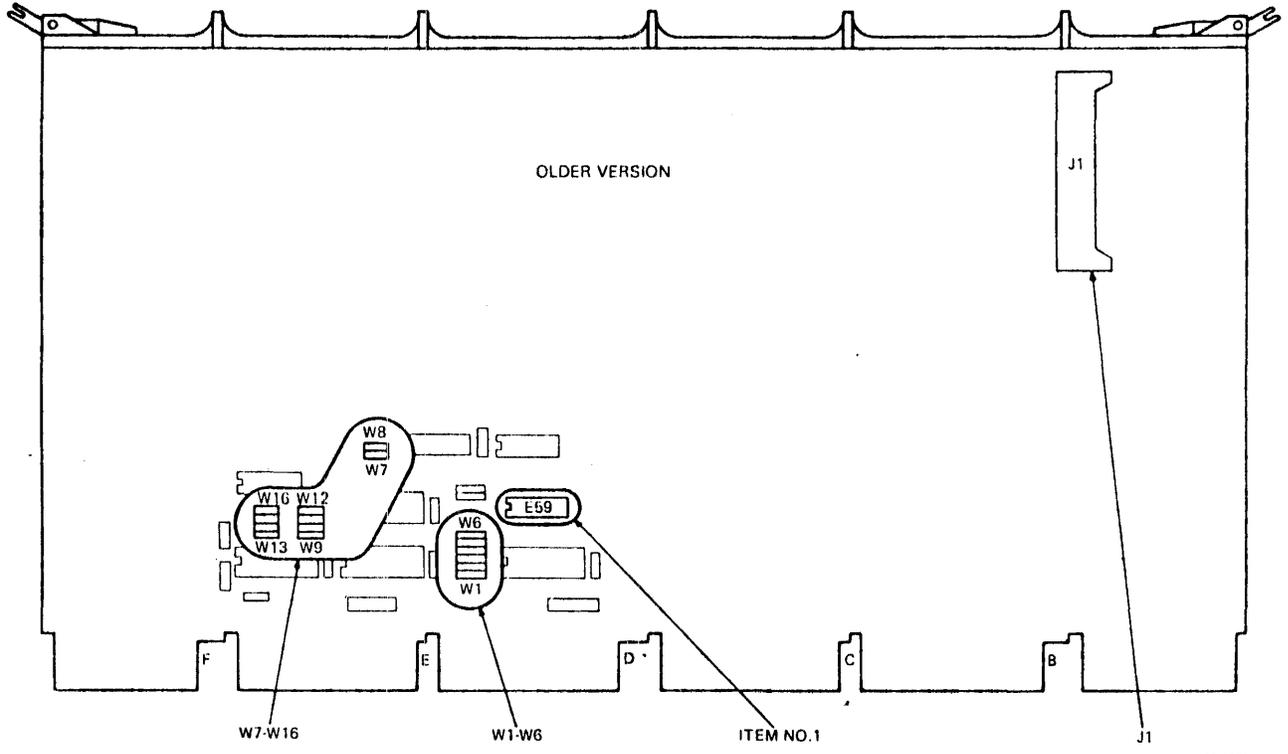
Figure B-9 RL11 Component Layout (Sheet 1 of 2)
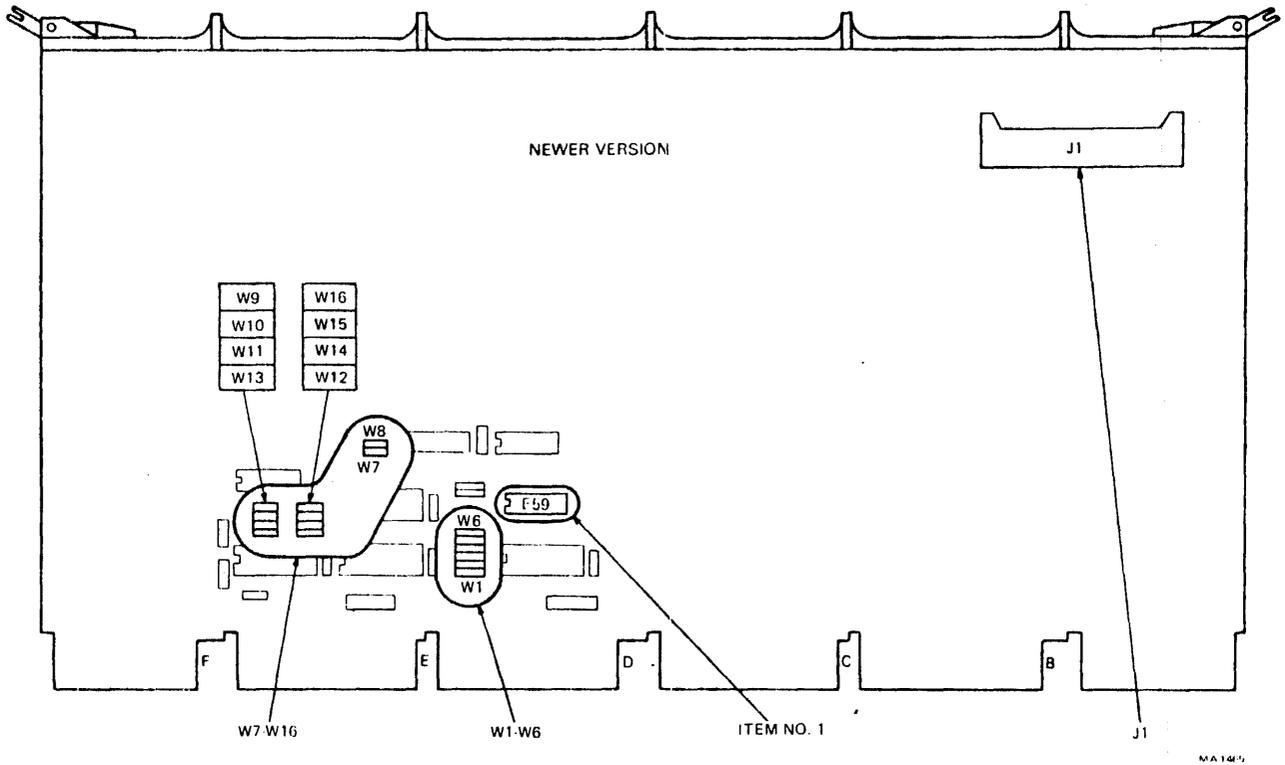
Figure B-9   RL11 Component Layout (Sheet 2 of 2)

The Unibus priority plug sets the priority for bus requests. For the RL11 subsystem, bus requests are at priority level 5 (BR5/BG5). (See Figures B-10 and B-11.)

To install the controller:

1. Remove the M7762 module from its shipping container and examine it for any physical damage.

2. If a priority level other than 5 is required, obtain an appropriate priority jumper assembly or set up the priority jumper assembly (item 1, Figure B-9) using Figure B-18 as a guide. The vector and base address jumpers W1-W16 are for 160 and 774400, respectively. If the subsystem configuration requires other than standard addresses, set the jumpers up as shown in Figure B-10. Physical location of these jumpers is shown on Figure B-9.

3. Install the ribbon cable (BC06R-XX) with the red indicator stripe to the right and the smooth side facing the viewer when viewing the component side of the controller as shown in Figure B-12. Dress the cable as necessary.

4. Insert the controller into its appropriate slot in the SPC backplane as shown in Figure B-12 after ensuring that the slot does not contain a grant continuity module in row D. Do not chafe the ribbon cable. Route the cable up and out to the rear of the cabinet, allowing for cable strain relief.

5. Remove the jumper between CA1 and CB1, (NPR Grant) on the backplane, if the jumper exists.

VECTOR ADDRESS SCHEME

	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	0			0			0				1		6				0	
	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0
	X	X	X	X	X	X	X	X	X	X	W_1	W_3	W_4	W_5	W_6	W_2	X	X

FOR VECTOR ADDRESS   160 - W_3, W_4, W_5 JUMPERS IN

W_1, W_2, W_6 JUMPERS OUT

BASE ADDRESS SCHEME

2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	7			7			4			4			0			0		
1	1	1	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0
X	X	X	X	X	X	W_{12}	W_{16}	W_{15}	W_{14}	W_7	W_8	W_9	W_{11}	W_{10}	W_{13}	X	X	X

FOR BASE ADDRESS 774400 – W_{12}, W_{16}, W_7 JUMPERS IN

W_1, W_9, W_{10}, W_{11}, W_{13}, W_{14}, W_{15}, JUMPERS OUT
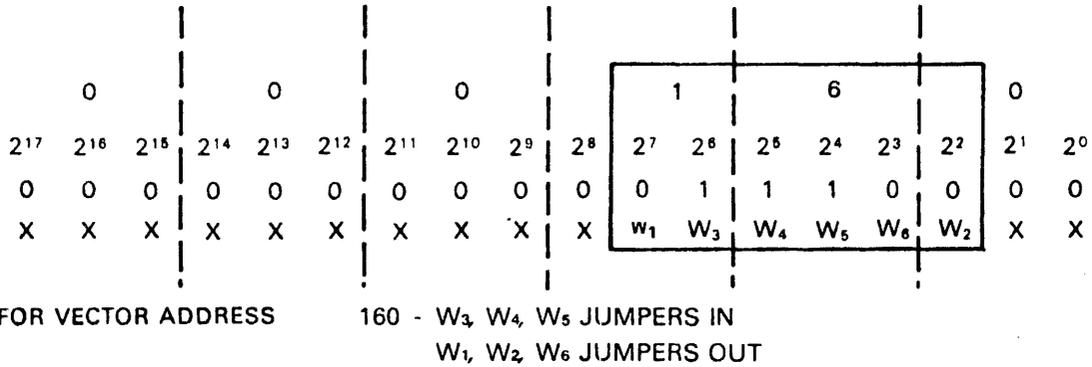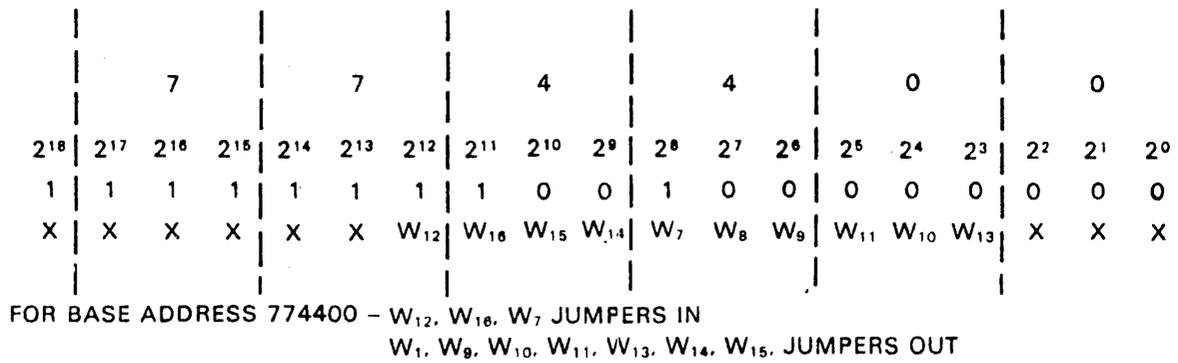
NOTE:
X'S DENOTE DON'T CARE (NOT SELECTABLE)
1'S DENOTE JUMPER IN
0'S DENOTE JUMPER OUT

CZ-2004

Figure B-10   RL11 Base and Vector Address Jumper Configurations

POSITIONER
FRONT VIEW:

POSITIONER
RESTRAINING
BRACKET

LATCH
SOLENOID
ACCESS COVER
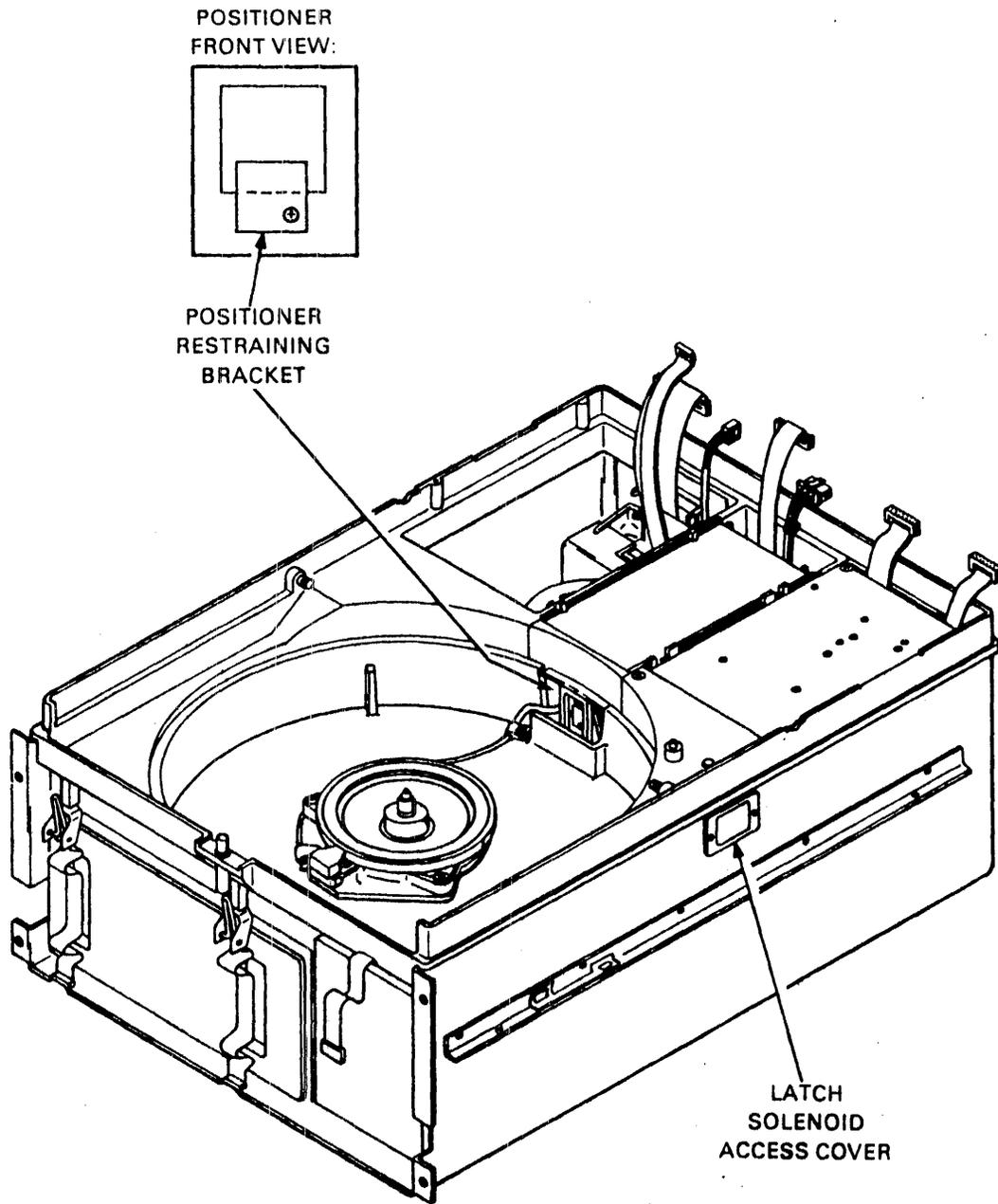
CZ-2003

Figure B-11   RL11 Priority Jumper Assembly Connections
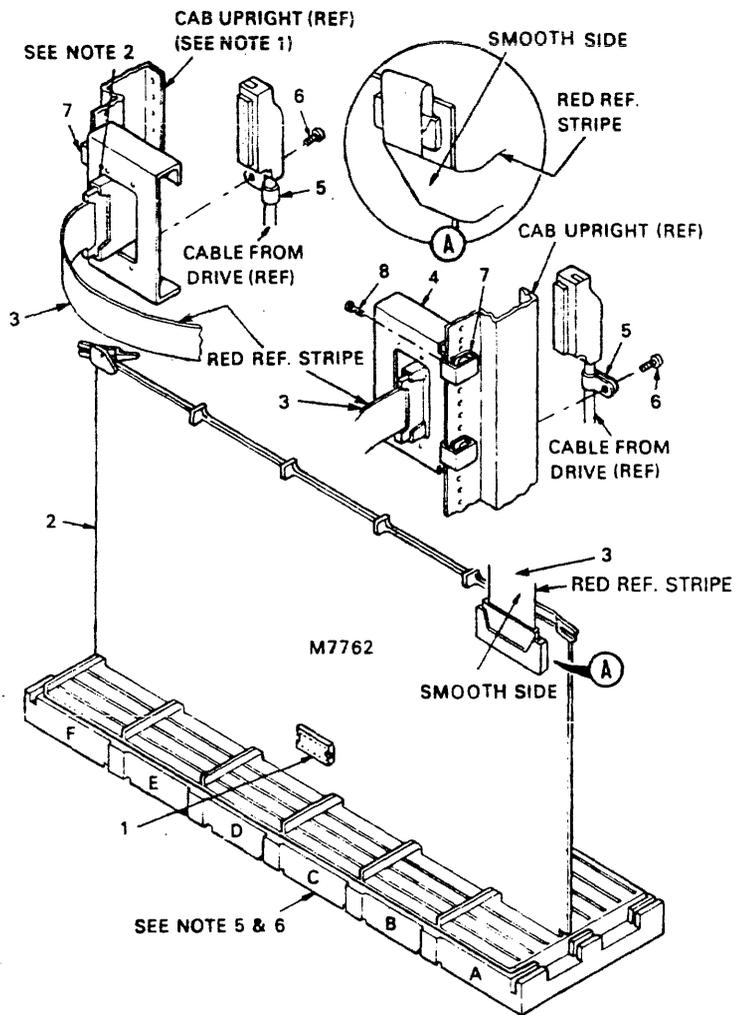
NOTES:

1. WHEN INSTALLED IN BA11K OR BA11L EXPANSION BOX, BC06R CABLE (ITEM #3) SHOULD BE FOLDED 90° AND ROUTED UP OUT OF THE BOX AS SHOWN.

2. WHEN ALTERNATE MOUNTING POSITION IS USED CONNECTOR IN TRANSITION BRACKET MUST BE INVERTED SO THAT I/O CABLE FROM DRIVE WILL HANG IN A DOWNWARD POSITION AS SHOWN.

3. ITEM #3 THRU ITEM #8 ARE NOT ASSEMBLED AT THIS POINT BUT ARE SHIPPED WITH UNIT FOR ASSEMBLY AT INSTALLATION TIME.

4. PRIORITY JUMPER ASSY (ITEM #1) TO BE PLUGGED INTO M7762 AT FINAL ASSY.

5. THE RL11 MODULE (M7762) WILL OCCUPY ONE HEX SPC SLOT.

6. JUMPER WIRE FROM CA1 TO CB1 ON THE SPC BACKPLANE MUST BE REMOVED AT INSTALLATION.

DESCRIPTION	DWG PART NO.	ITEM NO.
2 SCREW, PHL TRS HD. #10-32 X .50 LG	9006073-03	8
2 NUT, SPRING #10-32	9007786-00	7
1 SCREW, TAP-TLTE. #8 X .38 LG	9006418-01	6
1 CLAMP, CABLE	9007083-00	5
1 TRANSITION BRACKET ASSY	C-AD-7012415-0-0	4
1 CABLE ASSY	D-UA-BC06R-06	3
1 RL11 CONTROLLER	D-UA-M7762-0-0	2
1 PRIORITY JUMPER ASSY	5408778	1

CZ-2005

Figure B-12   RL11 Controller Installation

6.   Install the transition bracket at the rear of the cabinet shown in Figure B-12. Assemble and install transition connector.

7.   Connect the other end of the ribbon cable (BC06R-XX) with the red indicator stripe on the top. Use Figure B-12 as a guide.

8.   Apply system power and, using a suitable measuring device (i.e., digital voltmeter or equivalent), verify the voltages are within the ranges specified below.

VOLTAGE	RANGE	TEST POINT	
GROUND		AC2	
+5 VDC	+4.75 TO +5.25 VDC	AA2	BACKPLANE
+15 VDC	+14.25 TO +15.75 VDC	CV1	LOCATION
-15 VDC	-15.75 TO -14.25 VDC	CB2	

Measure all voltages between the ground test point and the appropriate voltage test point. If any adjustments to the power supply are necessary, refer to the appropriate manual.

B.5   RLV11 CONTROLLER INSTALLATION

An RLV11 Controller is comprised of a bus interface module (M8014) and the drive bus module (M8013). Each module has switches, jumpers, trimpots, and connectors that are explained in the following paragraphs.

B.5.1   Bus Interface Module

The bus interface module (M8014) contains the logic circuits that perform the following major functions:

- LSI-11 bus interface functions
- Programmable registers
- Silo data storage and control circuits

An illustration of the component side of M8014 is shown in Figure B-13. The location of the bus address switches, the vector address switches, and the connector finger assignments are shown in this figure.

The bus address switch is used to set up the device base address. It is normally factory preset to 7440. This means the device CS register has an address of 174400 and the MP register has an address of 174406. The switches have the ON and OFF positions labeled. The ON position is the logical 1 or true state (Figure B-14).

The vector address switch is used to select the address of the vector for this device when it interrupts. It is factory preset for an address of 160 (Figure B-15).

RLV11 BUS INTERFACE MODULE (M8014)
COMPONENT SIDE 1

MSB
BUS ADDRESS SWITCH
LSB
MSB
VECTOR SWITCH
LSB

D   C   B   A

V   A   V   A   V   A   V   A

CZ-2006
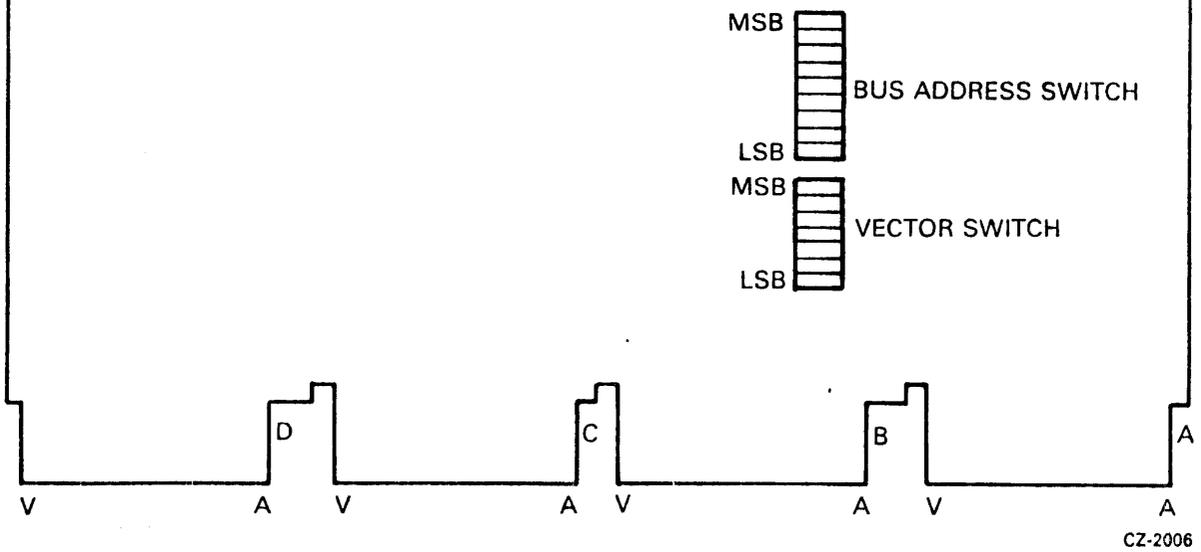
Figure B-13   RLV11 Bus Interface Module
(M8014) (Component Side)
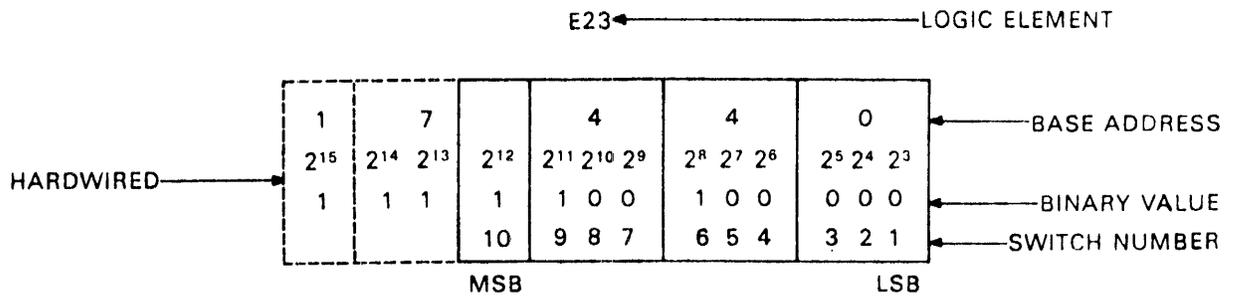
B-24

E23 ◄──────────── LOGIC ELEMENT

1	7		4	4	0	◄── BASE ADDRESS

HARDWIRED ──────►

2^{15} | 2^{14} 2^{13} | 2^{12} | 2^{11} 2^{10} 2^9 | 2^8 2^7 2^6 | 2^5 2^4 2^3

1 | 1 1 | 1 | 1 0 0 | 1 0 0 | 0 0 0 ◄── BINARY VALUE

| 10 | 9 8 7 | 6 5 4 | 3 2 1 ◄── SWITCH NUMBER

MSB   LSB

FOR EACH "0" SET THE CORRESPONDING SWITCH "OFF"

FOR EACH "1" SET THE CORRESPONDING SWITCH "ON"

USE THIS SCHEME TO SELECT THE APPROPRIATE BASE
ADDRESS IF A DIFFERENT BASE ADDRESS IS REQUIRED

CZ-2034

Figure B-14   RLV11 Base Address Switch Settings
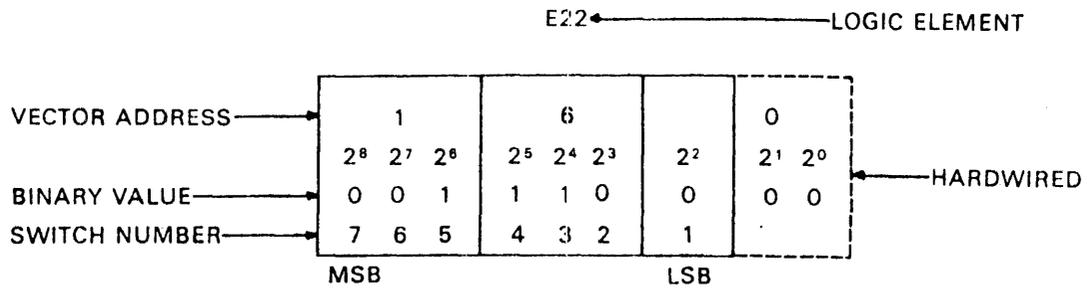
E22 ← ─────────── LOGIC ELEMENT

VECTOR ADDRESS ──────►

1			6				0	
2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
0	0	1	1	1	0	0	0	0
7	6	5	4	3	2	1		

BINARY VALUE ──────►

SWITCH NUMBER ──────►

────── HARDWIRED

MSB   LSB

FOR EACH "0" SET THE CORRESPONDING SWITCH "OFF"

FOR EACH "1" SET THE CORRESPONDING SWITCH "ON"

USE THIS SCHEME TO SELECT THE APPROPRIATE
VECTOR ADDRESS IF A DIFFERENT VECTOR
ADDRESS IS REQUIRED

CZ-2007

Figure B-15   RLV11 Vector Address Switch Settings

B.5.2   Drive Module

The drive module (M8013) contains the circuitry that performs the following major functions:

- Data formatting and error detecting circuits
- Control microsequencer and timing circuits
- Drive bus interface

An illustration of the component side of M8013 is shown in Figure B-16.

NOTE
Adjustments to the RLV11 are preset at
the factory and are not to be adjusted
in the field.

B.5.3   Module Slot Location

Modules M8013 and M8014 must be inserted into the H9273 backplane (Figure B-17) such that the M8013 module is in the slot closest to the processor. Outside of this one restriction, the two modules can be inserted in any two unused slots. The controller priority level is based solely on its electrical distance from the microprocessor module in slot 1.

B.5.4   Module Installation

1. Using the normal configuration rules, select two adjacent slots in the backplane for the two controller modules.

2. Insert the ribbon cable (BC06R-XX) into J1 on the M8013 with the red stripe edge toward the top (Row A) of the module.

3. Insert the M8013 module into the selected slot that is closest to the processor.

4. Examine the M8014 to insure that the base address switches and the vector address switches are set correctly. See Figures B-14 and B-15.

5. Insert the M8014 module next to the M8013.

6. Install the transition bracket at the rear of the cabinet as shown in Figure B-12. Assemble and install the transition connector.

7. Connect the other end of the ribbon cable with the red stripe up.

CABLE CONNECTOR TO DRIVE

W2   R 4 1   VCO POT

RLV11 DRIVE MODULE (M8013)
COMPONENT SIDE 1
JUMPERS W2 AND W4 IN PLACE FOR EPROM USE
JUMPERS W1 AND W3 IN PLACE FOR MASKED ROM USE

W1

E49
ROM
OR
EPROM
W4 W3

D   C   B   A

V   A V   A V   A V   A

NOTE:
JUMPERS ARE ZERO OHM COMPOSITION RESISTORS

CZ-2008
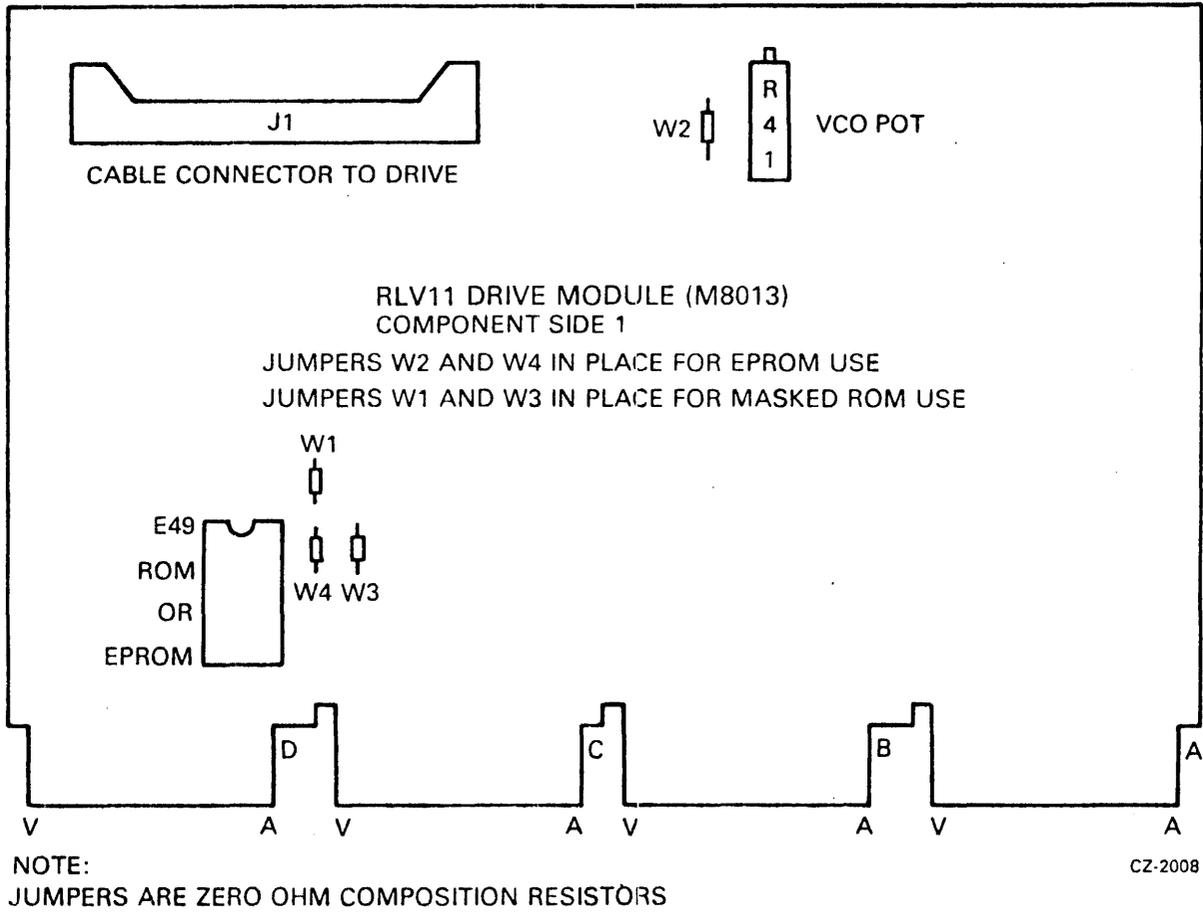
Figure B-16   RLV11 Drive Module (M8013)

(MODULE SIDE VIEW OF 9 SLOT BACKPLANE)

MA-0566
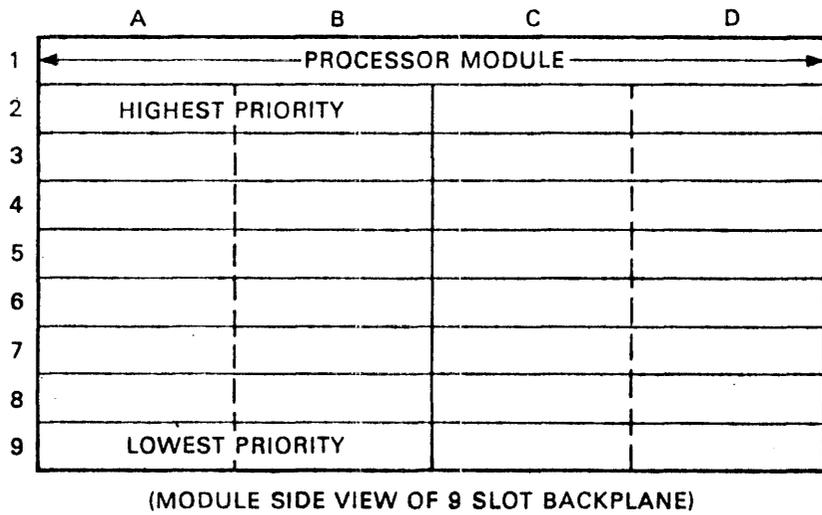
Figure B-17   H9723 Backplane Grant Priority Structure

B-28

8. Apply system power and, using a suitable measuring device (i.e., digital voltmeter or equivalent), verify that the voltages are within the ranges specified below.

Voltage	Range	Test Point
Ground		AC2
+5 Vdc	+4.75 Vdc to +5.25 Vdc	AA2
+12 Vdc	+11.5 Vdc to +12.5 Vdc	AD2
-5 Vdc	-5.25 Vdc to -4.75 Vdc	AL1 (M8013 only)

NOTE
The -5 Vdc is generated on the M8013 module. It is not adjustable but must be within specifications for proper operation. Module replacement is the only corrective procedure.

Measure all voltages between the ground test point and the appropriate voltage test point. If any adjustments to the power supply are necessary, refer to the appropriate processor's service manual.

B.6   RL8-A CONTROLLER INSTALLATION

B.6.1   Introduction
The RL8-A Omnibus controller module (M8433) contains the following logic functions:

- Interface logic
- Programmable registers
- Silo data storage and control
- Data formatting and error detection
- Control microsequencer and timing logic
- Drive bus interface logic

NOTE
Adjustments on the RL8-A are preset at the factory and are not to be changed in the field.

B.6.2   Module Slot Location
The module can be inserted into any unused Omnibus hex-height slot between the CPU and the first memory element. The controller is connected to the first drive via a BC80J-20 interface cable. Connections between drives are made using a BC20J-XX (70-12122-10) cable.

B.6.3   Module Installation

1. Remove the M8433 module (see Figure B-18) and interface cable (BC08J-20) from the shipping container and inspect them for physical damage.
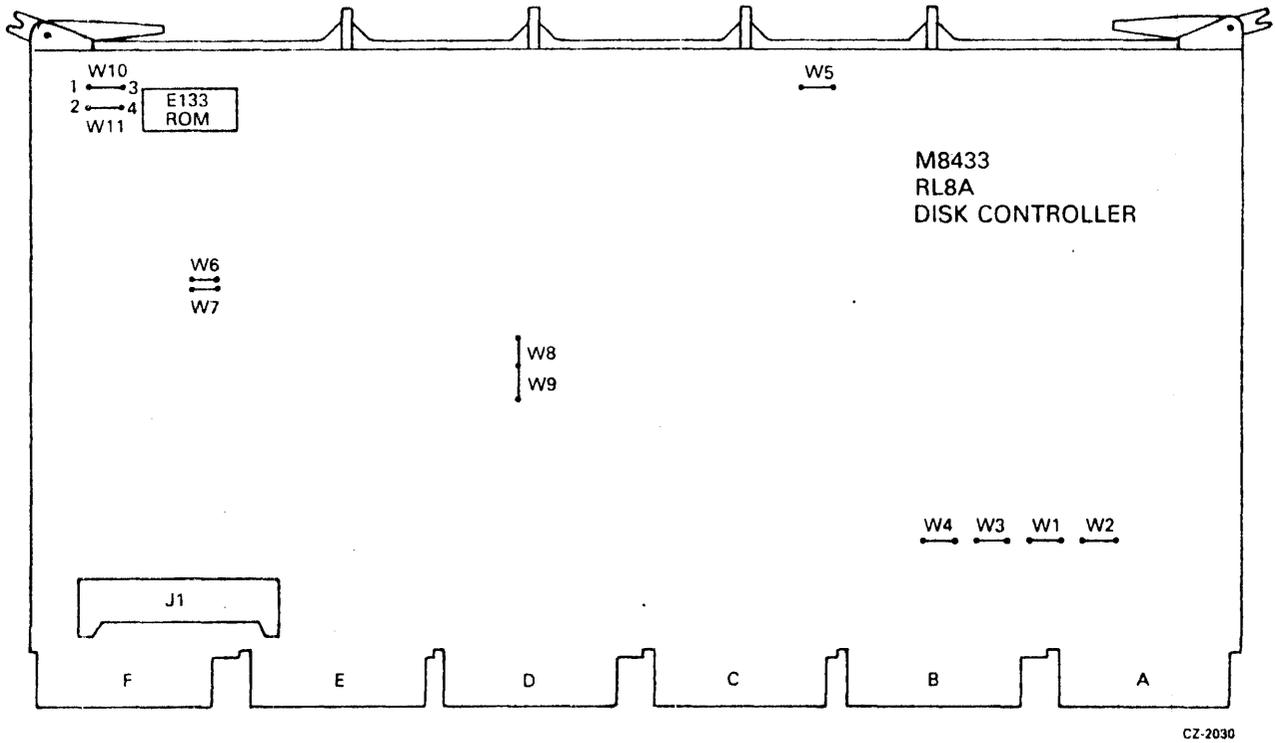
Figure B-18   RL8-A Jumpers

2. Verify the proper jumper configuration for device codes
    and priority (Figure B-18).

Device Code	W1	W2
60,61	IN	OUT
62,63	IN	IN

Break Priority	W3	W4	W5
0	IN	OUT	IN
1	OUT	IN	OUT

    NOTE
    RL8-A is shipped from the factory with a
    priority of 0.

Device Type	W8	W9		
RL01	OUT	IN		
RL02	IN	OUT		

ROM Type (E133)	W10	W11	W6	W7
012E2	OUT	IN	IN	OUT
8708 or 2708	IN	OUT	OUT	IN

3. Position the BC80J-20 interface-to-drive cable in the
    PDP-8 chassis and connect the Berg connector to the M8344
    module.

4. Install the M8344 module into selected slot in the
    Omnibus backplane.

5. Route the cable out to where the first drive will be
    installed.

B.7   RL01/RL02 DISK DRIVE INSTALLATION

B.7.1   Unpacking and Inspection

1. When delivered, each drive and its associated cabinetry
    are enclosed by a heavy cardboard carton and attached to
    a shipping skid (Figure B-19). Remove the plastic straps
    that secure the shipping carton to the skid.

2. Remove the lid from the top of the carton.

3. Remove the staples that fasten the wooden crating slats
    and carton flanges to the skid.

FULL TELESCOPE CAP
(9905446)

5-PANEL FOLDER
(9905975)

CRATING SLAT
(7606858)

CUSHIONED
SHIPPING SKID

STAPLES
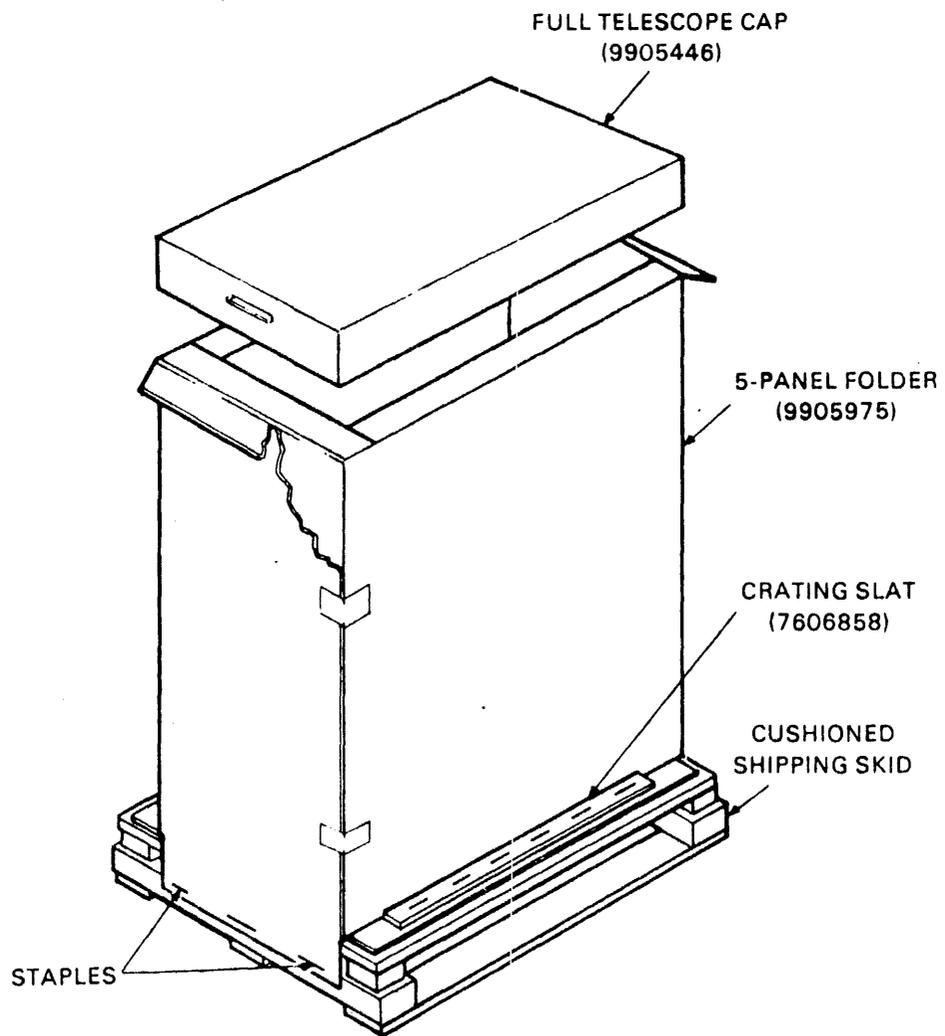
11-4979

Figure B-19   H950 Shipping Package

4.   Remove the shipping carton.

5.   Inspect the cabinet and drive for signs of damage. Retain all packing material and receipts in the event that any claims for shipping damage must be filed. All claims should be filed promptly with the transportation company.

B.7.2   RL01/RL02 Disk Drive Unit Mounting

NOTE
If the RL01/RL02 is to be mounted in an H950 cabinet, the shipping brackets must be retained and refitted after installation. This is the only way to prevent the drive from sliding while repositioning or moving the H950 cabinet.

The drive may be shipped in a rack or cabinet as an integral part of a system or may be shipped in a separate container for addition to an existing system.

If the drive is to be installed in an existing rack or cabinet, install the chassis slides first as described in Steps 1 through 6 below (Figure B-20). The procedure for installing the drive itself begins with Step 7.

1.   Install cabinet stabilizers before mounting the drive.

2.   Remove the slides from the disk drive.   (Retain the hardware for reassembly.)

3.   Install slides into the rack or cabinet using enclosed hardware. Be sure the slides are at the correct height to permit installation of pop panels (dress panels) upon completion of installation. Also verify that the slides do not bind on any hardware used to mount the slide.

4.   Extend slides to lock position.

5.   Slide drive onto chassis slides and reinstall security mounting hardware.

6.   Ensure that the disk drive moves easily on the slides, that there is no binding in the cabinet, and that the proper height has been maintained for dress panels.

7.   Open the drive access cover.

SLIDES

SLIDE
RAILS

SEE
DETAIL

LOCKING LATCH

ACCESS SLOT

SLIDE EXTENSION
RELEASE CATCH
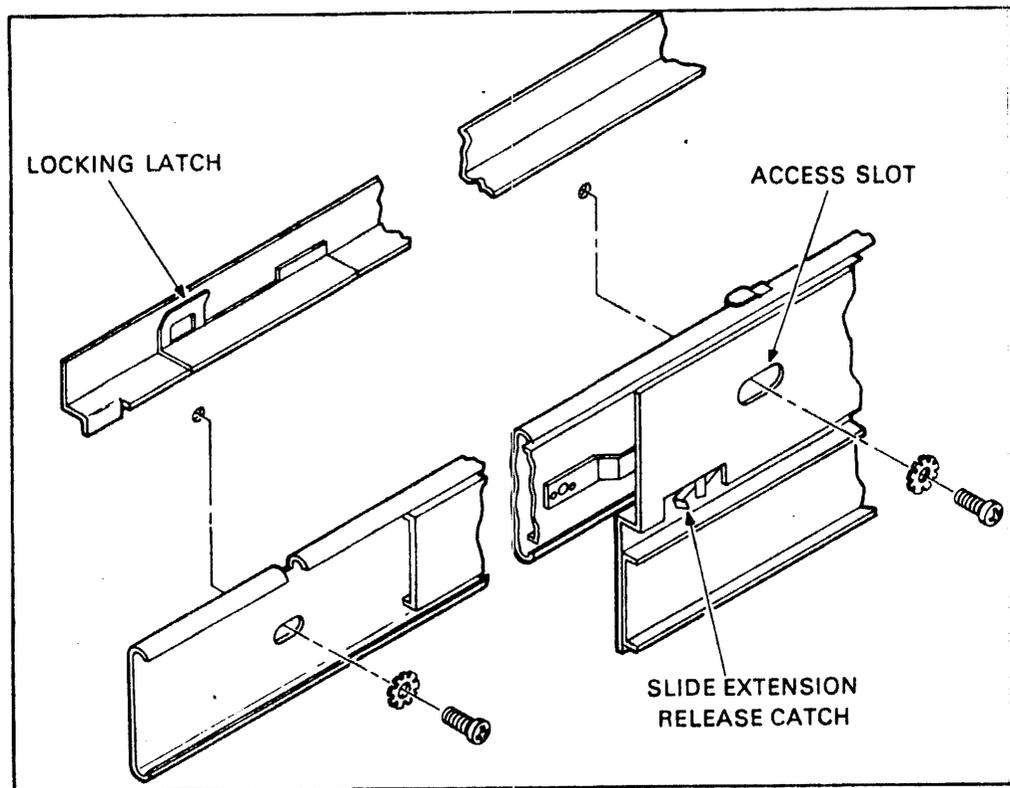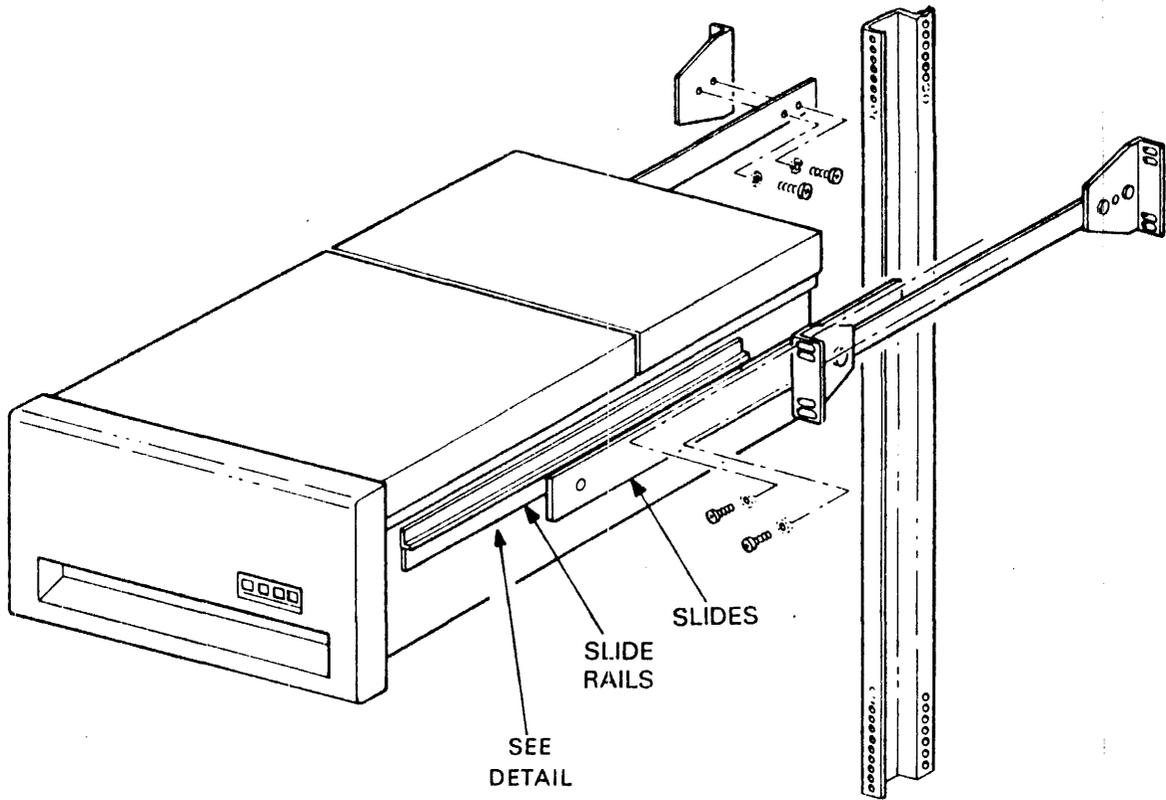
CZ-0009

Figure B-20   RL01/RL02 Cabinet Installation

B-34

NOTE

There is a safety interlock in the RL01
and RL02 Disk Drives that locks the drive
access cover when the drive has no power.
The manual release to bypass this
interlock is located on the right side of
the drive under a small access cover
(Figure B-21). Remove the cover to reach
the solenoid. Pull down on the solenoid
and operate the top release mechanism at
the same time to open the drive access
cover. After the drive access cover is
open, replace the solenoid cover.

8. Loosen the head restraining bracket screw located on the
    positioner. Turn the bracket 90 degrees and retighten
    the screw (Figure B-22).

9. On newer drives, these are two shipping screws on the
    bottom of the unit that secures the spindle/blower motor.
    Remove the screws.

10. If the drive is being install in a dual-drive cabinet
    that has an interlock system to prevent more than one
    drive being extended at a time, ensure that is is
    connected.

11. Inspect the terminal block covers at the rear of the
    drive. Ensure that they are configured properly for the
    input power available (Figure B-22).

CAUTION

Connection to the wrong power source
will result in serious damage to the
disk drive.

12. If there is only one disk drive in the system, or if this
    is the last drive of the daisy chain, install a
    terminator assembly (DIGITAL part no. 70-12293) in the
    "cable out" location at the rear of the drive (Figure
    B-22).

13. If this is an RL11- or an RLV11-based system, route the
    I/O cable BC20J-XX (DIGITAL part no. 70-12122-10) between
    the first drive and the transition connector. If this is
    an RL8-A-based system, route the BC80J-20 cable from the
    RL8-A to the first drive.

POSITIONER
FRONT VIEW:

POSITIONER
RESTRAINING
BRACKET

LATCH
SOLENOID
ACCESS COVER
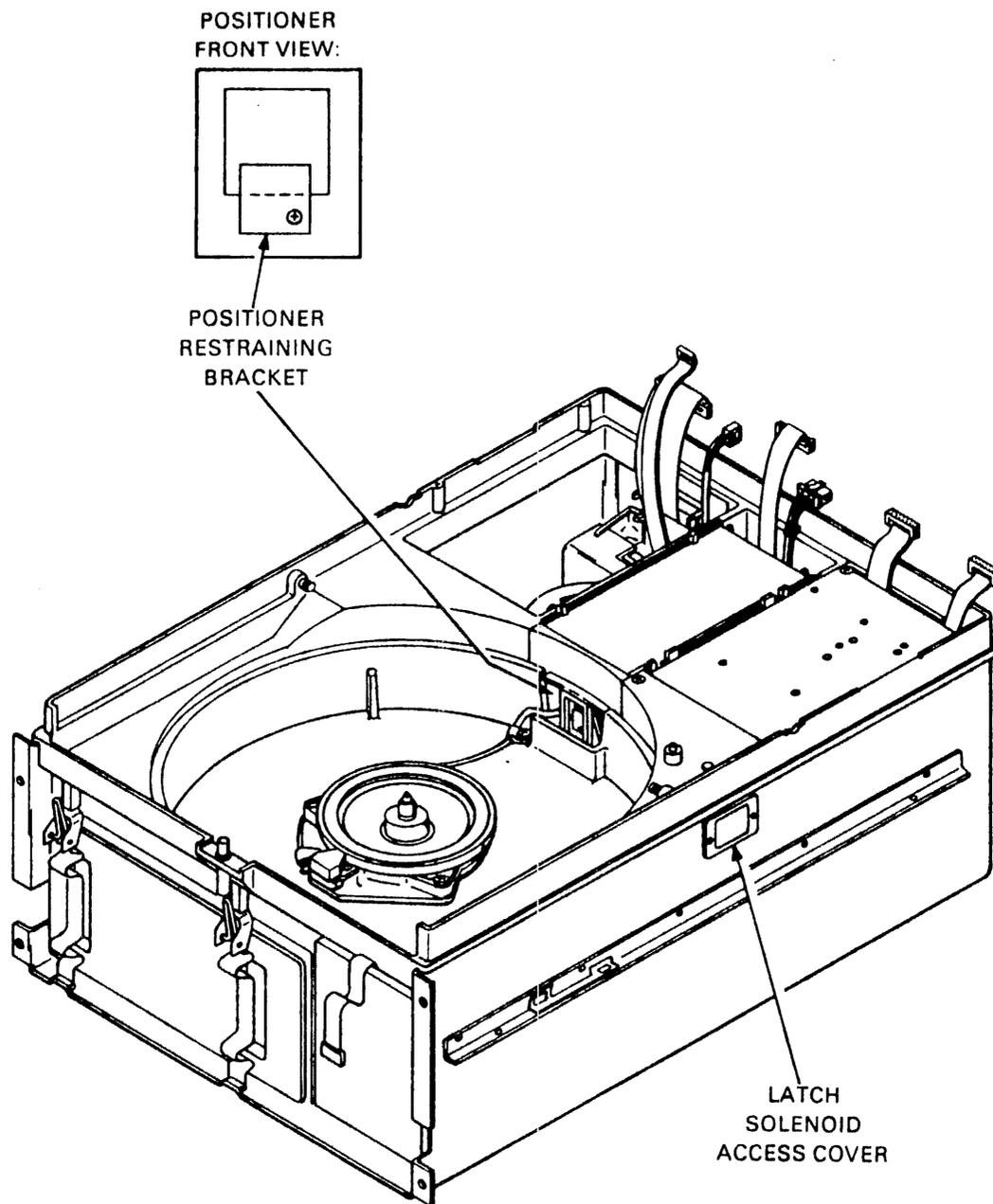
CZ-2003

Figure B-21   RL01/RL02 - Covers Removed

I/O CABLE
("CABLE IN")

TERMINATOR

NORMAL/LOW
LINE VOLTAGE
TERMINAL BLOCK
COVER

110/220 VOLTS
TERMINAL
BLOCK COVER

CIRCUIT BREAKER

AC LINECORD
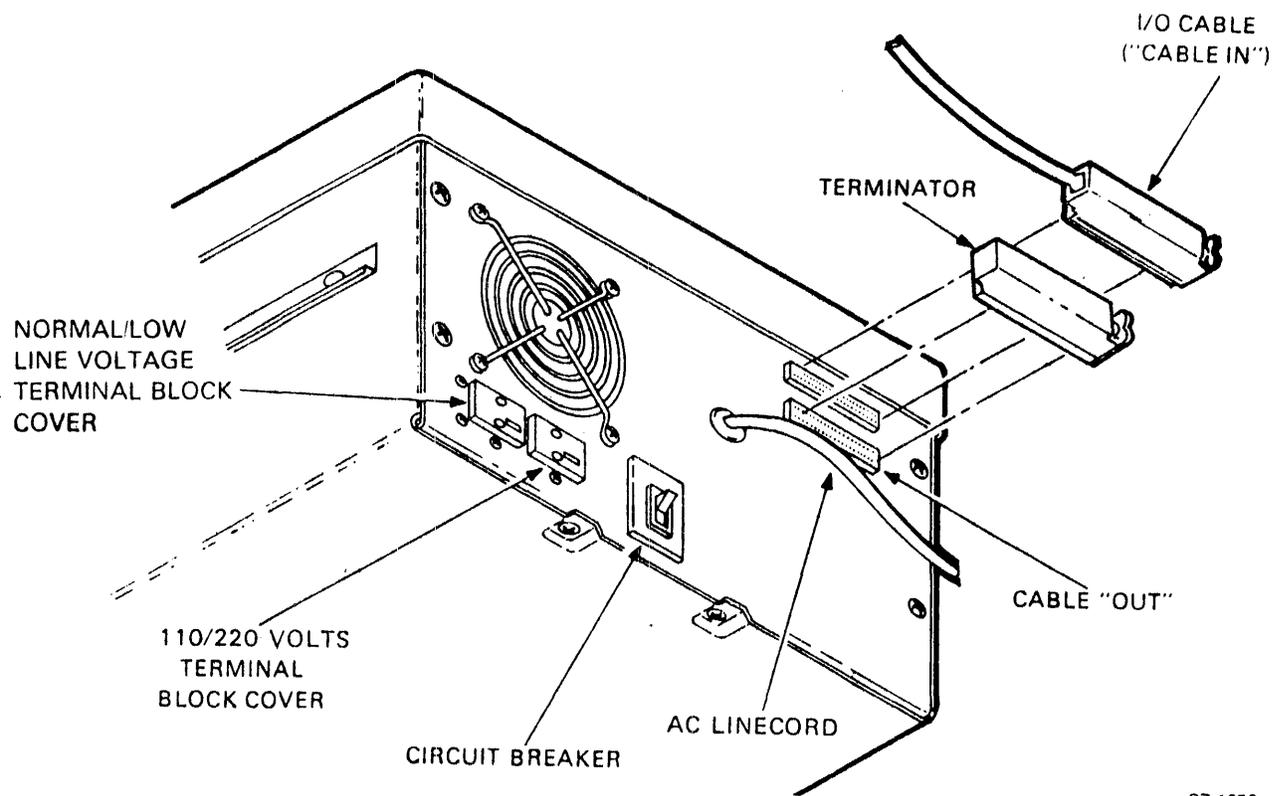
CABLE "OUT"

CZ-1056

Figure B-22 RL01/RL02 Disk Drive - Rear View

14. If this is a multidrive installation, connect an I/O cable from "cable in" of this drive to the "cable out" connector of the previous drive. Repeat for each drive.

NOTE
The total length of cable from controller to the last drive must not exceed 30 m (100 ft).

15. Install the proper unit select plug at the front of the drive (Figure B-23).

B.7.3 Drive Prestart-up Inspection

To begin the inspection procedure, remove the top cover by loosening the captive screws and lifting the cover straight up. Rest the cover on the rear of the drive (Figure B-24). With the drive power off, follow these steps.

1. Ensure that the positioner restraining bracket is secured out of position to prevent interference with it (Figure B-22).

2. Ensure that the positioner is home.

3. Ensure that the read/write head gimbels are not bent or dirty. (If they are dirty, clean with a solution of 91 percent alcohol and 9 percent water and a lint-free wiper.

4. Ensure that the spindle rotates freely and its top surfaces are not dirty. (Clean as described above.)

5. Ensure that the brush assembly is home (not exposed).

6. Ensure that the logic modules and connectors are seated firmly.

7. Turn CB1 ON.

8. Ensure that the spindle rotates slowly counterclock wise for approximately 15 seconds and stops. At this time, the LOAD light will come on.

9. Ensure that the FAULT light is not on.

10. Ensure that the muffin fan at the rear of the drive is operating.

LOAD SWITCH
AND INDICATOR

UNIT SELECT PLUG
AND READY INDICATOR

FAULT
INDICATOR

WRITE PROTECT SWITCH
AND INDICATOR
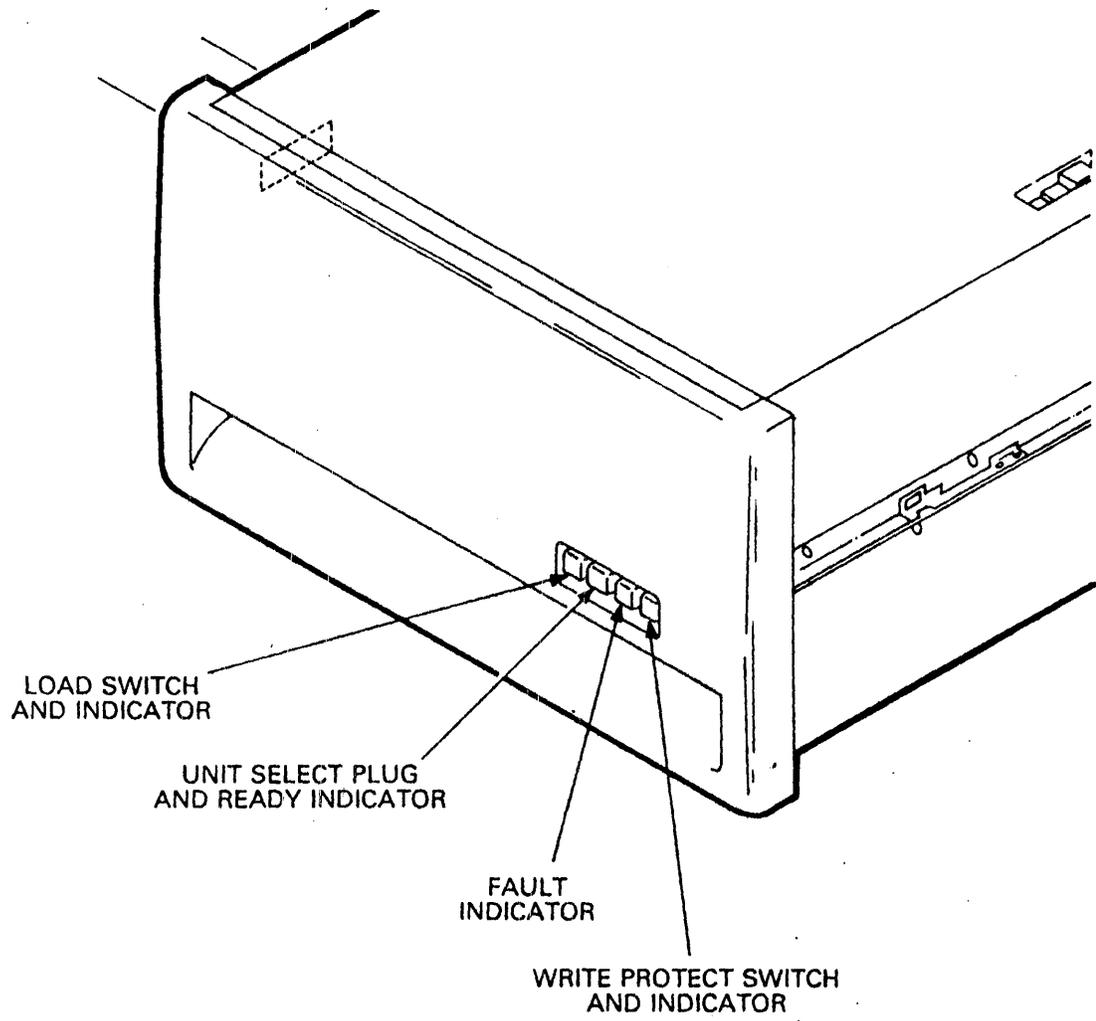
CZ-1005

Figure B-23   RL∅1/RL∅2 Disk Drive - Front View

11. Using a suitable measuring device (i.e., digital voltmeter or equivalent), ensure the following drive voltages are within the specified tolerances.

Voltage	Range	Test Point
+15UNREG	(+15.0 to +18.0 Vdc)	+VUNREG
-15UNREG	(-15.0 to -18.0 Vdc)	-VUNREG
+5REG	(+4.85 to +5.35 Vdc)	TP8
+8REG	(+7.7 to +8.3 Vdc)	TP4
-8REG	(-7.7 to -8.3 Vdc)	TP5

See Figure B-24 for dc servo module location. Test points are located on the mask covering the dc servo module (Figure B-25).

12. Verify that the WRITE PROTect switch cycles in and out and the indicator lights up when the switch is pressed.

13. Verify that the LOAD switch cycles in and out and the indicator light goes out when the switch is pressed. Return switch to the "out" position.

14. Turn off CB1.

15. Reinstall the top cover and secure with the captive screws.

16. Ensure that the drive access cover cannot be opened.

17. Turn CB1 on and ensure the drive access cover will open.

B.7.4   Drive Star-tup Operation Check

1. With the drive power ON, install a scratch cartridge.

2. Close the cover, press the LOAD switch and note that:

   o   the LOAD light goes out

   o   When the cartridge reaches nominal speed (after approximately 30 seconds), a brush cycle commences. When the brushes have returned home, the read/write heads will load and approach cylinder 0. When the heads have locked onto cylinder 0, the READY light will illuminate. The total time for this process is approximately 45 seconds.

DRIVE LOGIC
MODULE

A.C.
SERVO MODULE

R/W
MODULE

D.C.SERVO MODULE
AND TEMPLATE
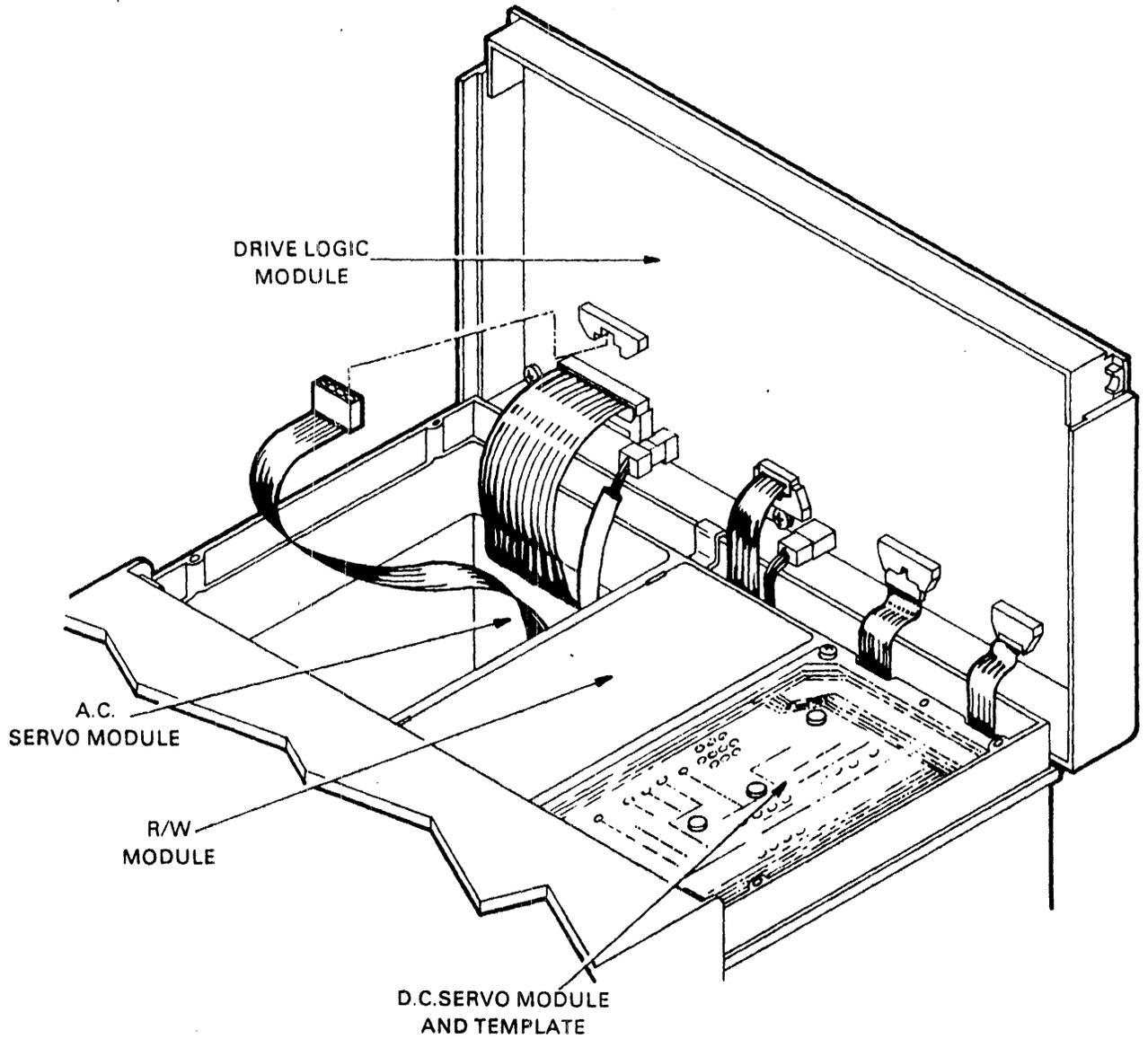
CZ-0011

Figure B-24 RL01/RL02 Disk Drive - Exposed Drive Logic Module

B-41

3. Press the LOAD switch again. The READY light should go off and the read/write heads should retract to their home position. The spindle should slow down and then come to a complete stop after about 30 seconds. The LOAD light should illuminate when the spindle has stopped.

4. If the drive startup operation check detailed above is successfully completed (i.e., the READY indicator illuminates), run the subsystem confidence tests described in Paragraph B.8.

B.8   CONFIDENCE TESTING

Confidence testing consists of running the diagnostic programs. Each diagnostic has a listing that contains operating instructions. Each listing explains system hardware requirements, software environment, which features are tested and how they are tested, program options and how to select them, how to interprete printouts, error handling, device information tables, dialogue with the Diagnostic Supervisor, and complete operating instructions. The listings are available as hard copy printouts or on microfiche.

The binary form of the diagnostic programs are available on various media. It is always advisable to keep a copy of the RL01/RL02 diagnostics on a media other than the RL01K or RL02K cartridge so that the diagnostics can be loaded through another device if the RL subsystem is down.

The old MAINDEC naming system is being replaced with a new naming system. Manual and microfiche designations are also being converted. In addition, part numbers are being assigned that conform to DIGITAL's standard twelve character part number system.

When ordering diagnostic media, listings, manuals, or microfiche, check the current catalog or index for the latest designation and revision level. The applicable catalogs and indexes are listed in Table B-3. Unless otherwise specified when ordering, the latest revision will be shipped.

Table B-3   Diagnostic Catalogs and Indexes

NAME		PART NUMBER
PDP-11	Diagnostic Software Components Catalog*	AV-B021E-TC
PDP-8	Software Components Catalog*	AV-0872B-TA
PDP-11	MAINDEC Index	AH-9026P-MC
PDP-8	MAINDEC Index	AH-6572G-MA

* NOTE: Both of these catalogs are available on microfiche (EP-08/11DC-02)

B.8.1   RL11-Based Diagnostics

The diagnostic package used for an RL11/RL01 subsystem before the release of the RL02 consisted of the six free-standing programs listed in Table B-4.   There were two revisions, Revision A and Revision B.   These programs handled only RL01 drives (not RL02 units).

Table B-4   RL11-Based Diagnostics

CZRLAA0	Controller Test Part 1
CZRLBA0	Controller Test Part 2
CZRLCA0	Drive Test Part 1
CZRLDA0	Drive Test Part 2
CZRLEA0	Performance Exerciser
CZRLFA0	Drive Compatibility Test

These diagnostics can be run free-standing, under the Diagnostic Supervisor, manually under XXDP, chainable under XXDP (except CZRLFA0 which requires manual intervention), or under manufacturing checkout environments such as SLIDE or ACT-11.

A new diagnostic package is available to test either an RL01 or an RL02 unit.   The kit numbers are listed in Table B-5 and the contents of the tests are shown in Table B-6.

There is a new program added to the package named CZRLMA0.   It is used to read the Bad Sector File and can be used to write entries into the field writable portion of the Bad Sector File.   This program is not a diagnostic and should not be used as one.   It assumes that the system is functioning properly.

Table B-5   RL11 Diagnostic Kit Numbers

PART NUMBER	DESCRIPTION
ZJ283-RB	Documentation and Paper Tape
ZJ283-RZ	Documentation Only
ZJ283-PB	Paper Tape Only
ZJ283-FR	Microfiche Only

Table B-6   RL11 Diagnostic Components

PART NUMBER	NAME	ITEM	
AC-F111A-MC	CZRLGA0 CONTROLLER TEST #1	DOCUMENTATION	
AH-F110A-MC		FICHE	
AK-F108A-MC		PAPER TAPE	#1
AK-F109A-MC		PAPER TAPE	#2
AF-F111A-M0		DECO	
AC-F115A-MC	CZRLHA0 CONTROLLER TEST #2	DOCUMENTATION	
AH-F114A-MC		FICHE	
AK-F112A-MC		PAPER TAPE	#1
AK-F113A-MC		PAPER TAPE	#2
AF-F115A-M0		DECO	
AC-F119A-MC	CZRLIA0 DRIVE TEST #1	DOCUMENTATION	
AH-F118A-MC		FICHE	
AK-F116A-MC		PAPER TAPE	#1
AK-F117A-MC		PAPER TAPE	#2
AF-F119A-M0		DECO	
AC-F123A-MC	CZRLJA0 DRIVE TEST #2	DOCUMENTATION	
AH-F122A-MC		FICHE	
AK-F120A-MC		PAPER TAPE	#1
AK-F121A-MC		PAPER TAPE	#2
AF-F123A-M0		DECO	
AC-F127A-MC	CZRLKA0 PERFORMANCE EXERCISER	DOCUMENTATION	
AH-F126A-MC		FICHE	
AK-F124A-MC		PAPER TAPE	#1
AK-F125A-MC		PAPER TAPE	#2
AF-F127A-M0		DECO	
AC-F131A-MC	CZRLLA0 DRIVE COMPATIBILITY TEST	DOCUMENTATION	
AH-F130A-MC		FICHE	
AK-F128A-MC		PAPER TAPE	#1
AK-F129A-MC		PAPER TAPE	#2
AF-F131A-M0		DECO	
AC-F135A-MC	CZRLMA0 BAD SECTOR FILE UTILITY	DOCUMENTATION	
AH-F134A-MC		FICHE	
AK-F132A-MC		PAPER TAPE	#1
AK-F133A-MC		PAPER TAPE	#2
AF-F135A-M0		DECO	

In addition to the free-standing diagnostics, there is a DECX11 module for use with the DECX11 System Exerciser. The current revision is designated RLAA and is in DECX11 Option Library #5 DXQLQ. Revision A (RLAA) will operate an RL01 drive only. Revision B (RLAB) will operate either an RL01 or an RL02.

There is also an RL subsystem driver for the Maintenance Program Generator (MPG).

The binary form of the diagnostics are included as part of XXDP. This makes them available on media for the RK05, RK06, RK07, RL01, RX01, DECtape, magnetic tape, and DECassette.

The use of XXDP, DECX11, and MPG is explained in the manuals listed in Table B-7.

Table B-7   User Documents

PART NUMBER HARD COPY	PART NUMBER MICROFICHE	NAME
AC-9093I-MC	EP-DZQXA-J-D	CZQXAI0 XXDP USER GUIDE
AC-8240Z-MC	AH-8242Z-MC	CXQBAZ0 DECX11 USER DOCUMENT
AC-816JC-MC	EP-DTUMA-C-D	CTUMAC0 MPG USER MANUAL

B.8.2   RLV11-Based Diagnostics

The RLV11 Controller-based subsystem is tested with the same set of diagnostics as the RL11 Controller subsystem with the following exception. The RLV11 has an internal maintenance feature that is not tested by the RL11 diagnostics so there is one additional diagnostic program called the CVRLAA0 Diskless Test. It should be run first.

The diagnostic kit includes the same items as the RL11 diagnostic kit plus the CVRLAA0 test. The RLV11 kit designations are shown in Table B-8.

Table B-8   RLV11 Diagnostic Kit Designations

DESIGNATION	CONTENTS
ZJ285-RB	Documentation and Paper Tape
ZJ285-RZ	Documentation Only
ZJ285-PB	Paper Tape Only
ZJ285-FR	Microfiche Only

The DECX11 module is the same one used for the RL11.

B.8.3   RL8A-Based Diagnostics

There are six free-standing diagnostic programs for the RL8-A Controller-based system. There is also a DECX8 module for use with the DECX8 system exerciser. These diagnostics are available as individual components (see Table B-9) or in a kit (see Table B-10).

Table B-9   RL8-A/RLØ1 Diagnostic Components

PART NUMBER	DESIGNATION
AC-C656A-MA	AJRLAAØ, RL8A DISKLESS CONTROL TEST (DOC)
AH-C657A-MA	AJRLAAØ, RL8A DISKLESS CONTROL TEST (FICHE)
AK-C658A-MA	AJRLAAØ, RL8A DISKLESS CONTROL TEST (P. TAPE)
AL-C659A-NA	AJRLAAØ, RL8A DISKLESS CONTROL TEST (DECTAPE)
AC-C66ØA-MA	AJRLBAØ, RL8A/RL01 DRIVE TEST 1 (DOCUMENT)
AH-C661A-MA	AJRLBAØ, RL8A/RL01 DRIVE TEST 1 (FICHE)
AK-C662A-MA	AJRLBAØ, RL8A/RL01 DRIVE TEST 1 (P. TAPE)
AL-C663A-NA	AJRLBAØ, RL8A/RL01 DRIVE TEST 1 (DECTAPE)
AC-C664A-MA	AJRLCAØ, RL8A/RL01 DRIVE TEST 2 (DOCUMENT)
AH-C665A-MA	AJRLCAØ, RL8A/RL01 DRIVE TEST 2 (FICHE)
AK-C666A-MA	AJRLCAØ, RL8A/RL01 DRIVE TEST 2 (P. TAPE)
AL-C667A-NA	AJRLCAØ, RL8A/RL01 DRIVE TEST 2 (DECTAPE)
AC-C668A-MA	AJRLDAØ, RL8A/RL01 COMPAT. VERIFY (DOCUMENT)
AH-C669A-MA	AJRLDAØ, RL8A/RL01 COMPAT. VERIFY (FICHE)
AK-C67ØA-MA	AJRLDAØ, RL8A/RL01 COMPAT. VERIFY (P. TAPE)
AL-C671A-NA	AJRLDAØ, RL8A/RL01 COMPAT. VERIFY (DECTAPE)
AC-C672A-MA	AJRLEAØ, RL8A/RL01 PERF. EXER. (DOCUMENT)
AH-C673A-MA	AJRLEAØ, RL8A/RL01 PERF. EXER. (FICHE)
AK-C674A-MA	AJRLEAØ, RL8A/RL01 PERF. EXER. (P. TAPE)
AL-C675A-NA	AJRLEAØ, RL8A/RL01 PERF. EXER. (DECTAPE)
AC-C676A-MA	AXRLAAØ, RL8A DECX8 MODULE (DOCUMENT)
AH-C677A-MA	AXRLAAØ, RL8A DECX8 MODULE (FICHE)
AK-C678A-MA	AXRLAAØ, RL8A DECX8 MODULE (P. TAPE)
AC-C682A-MA	AJRLGAØ, RL8A/RL01 PACK VERIFY (DOCUMENT)
AH-C683A-MA	AJRLGAØ, RL8A/RL01 PACK VERIFY (FICHE)
AK-C684A-MA	AJRLGAØ, RL8A/RL01 PACK VERIFY (P. TAPE)
AL-C685A-NA	AJRLGAØ, RL8A/RL01 PACK VERIFY (DECTAPE)

Table B-1Ø   RL8-A/RLØ1 Diagnostic Kits

PART NUMBER	CONTENTS
ZB233-RB	DOCUMENTATION AND PAPER TAPE
ZB233-RZ	DOCUMENTATION ONLY
ZB233-PB	PAPER TAPE ONLY
ZB233-FR	MICROFICHE

Table B-11   RL8/RLØ2 Diagnostic Kits

PART NUMBER	CONTENTS
ZF241-RZ	DOCUMENTATION
ZF241-RB	DOCUMENTATION AND PAPER TAPE
ZF241-PB	PAPER TAPE
ZF241-FR	FICHE
ZF241-PH	RLØ2
ZF241-RH	RLØ2 AND DOCUMENTATION

Table B-12   RL8/RLØ2 Diagnostic Components

PART NUMBER	NAME	ITEM
AC-C656C-MA	AJRLACØ RL8A DISKLESS CONTROL TEST	DOCUMENTATION
AH-C657C-MA		FICHE
AK-C658C-MA		PAPER TAPE
AL-C659C-NA		DEC TAPE
AC-F362A-MA	AJRLHAØ RL8/RLØ2 SEEK/FUNCTION	DOCUMENTATION
AK-F363A-MA		PAPER TAPE
AH-F364A-MA		FICHE
AL-F365A-MA		DEC TAPE
AF-F362A-MØ		DECO/DEPO
AC-F366A-MA	AJRLIAØ RL8/RLØ2 READ/WRITE	DOCUMENTATION
AK-F367A-MA		PAPER TAPE
AH-F368A-MA		FICHE
AL-F369A-MA		DEC TAPE
AF-F366A-MØ		DECO/DEPO
AC-F370A-MA	AJRLJAØ RL8/RLØ2 DRIVE COMPAT	DOCUMENTATION
AK-F371A-MA		PAPER TAPE
AH-F372A-MA		FICHE
AL-F373A-MA		DEC TAPE
AF-F370A-MØ		DECO/DEPO
AC-F374A-MA	AJRLKAØ RL8/RLØ2 PERF. EXER.	DOCUMENTATION
AK-F375A-MA		PAPER TAPE
AH-F376A-MA		FICHE
AL-F377A-MA		DEC TAPE
AF-F374A-MØ		DEPO/DECO
AC-F378A-MA	AJRLLAØ RL8/RLØ2 PACK VERIFY	DOCUMENTATION
AK-F379A-MA		PAPER TAPE
AH-F380A-MA		FICHE
AL-F381A-MA		DEC TAPE
AF-F378A-MØ		DECO/DEPO
AC-F382A-MA	AXRLBAØ DEC/X8 MOD RL8/RLØ2	DOCUMENTATION
AK-F383A-MA		PAPER TAPE
AH-F384A-MA		FICHE
AF-F382A-MØ		DECO/DEPO

B.9 USE OF THE M9312 BOOTSTRAP WITH AN RL11 SUBSYSTEM

The M9312 module is used on many PDP-11 Unibus systems to provide bootstrap capability as well as other functions. The module has five IC sockets for ROM chips, four of which are reserved for peripheral bootstrap programs. There are several ROM chips available for the different peripheral devices, and an M9312 is configured by selecting the appropriate chips for the particular system on which it is used.

The RL subsystem bootstrap program is contained in ROM chip number 23-751A9. This chip can be ordered individually and is also available in kit MR11-EA, which consists of an M9312 module plus all the available ROM chips.

An RL system disk can be booted by a command to the console emulator (a program that is a feature of the M9312). The device mnemonic for the RL11 is DL or DLn, where n is the unit number (0 through 3).

More information on the M9312 is available in the M9312 Technical Manual. It is available in printed form (EK-M9312-TM) or on microfiche (EP-M9312-TM).

C.1   HEAD SELECTION PROGRAM FOR RL11/RLV11

The following program causes Head 1 (lower head) to be selected (on unit 0) if the WRITE PROTect switch is in and Head 0 (upper head) to be selected if the switch is out.

```
1000        012700          Housekeeping
1002        174400
1004        012701
1006        174404
1010        105710          Wait
1012        100376
1014        012711          Get Status Command
1016        000013
1020        012710
1022        000004
1024        105710          Wait
1026        100376
1030        013702          Status Word
1032        174406
1034        006302
1036        010203
1040        006303
1042        105702          Check HS Bit
1044        100405
1046        005703          Check WL Bit
1050        100357          Equal, Loop
1052        012711          Set HS Bit
1054        000021
1056        000404          Go to Seek Command
1060        005703          Check WL Bit
1062        100752          Equal, Loop
1064        012711          Reset HS Bit
1066        000001
1070        012710          Seek Command
1072        000006
1074        000745          Loop
```

C.2   HEAD SELECTION PROGRAM FOR RL8-A

The following program causes Head 1 (lower head) to be selected (on unit 0) if the WRITE PROTect switch is in and Head 0 (upper head) to be selected if the switch is out.

```
200     6600            Clear Controller
201     1234
202     6604            Get Status Command
203     6601            Wait
204     5203
205     6615            First Word of Status
206     0232
207     7640            Check HS Bit
210     5217            HS=1, Go to 217
211     6615            Second Word of Status
212     0233
213     7650            Check WL Bit
214     5201            HS=WL, Go to 201
215     7332
216     5224
217     6615            Second Word of Status
220     0233
221     7640            Check WL
222     5201            HS=WL, Go to 201
223     7300
224     6603            HS to Command REG A
225     7325
226     6604            Seek Command to Command REG B
227     6601            Wait
230     5227
231     5201            Loop to 201
232     0100            Constant
233     0040            Constant
234     1002
```

C.3 GET STATUS (WITH OR WITHOUT RESET) ON AN RL11/RLV11 SUBSYSTEM
To accomplish this, it is necessary to:

1.   Deposit a 3 into DAR at 774404 (or 13 to Reset)

2.   Deposit a 4 into CSR at 774400 (or 404, 1004, 1404 for units 1, 2, 3)

3.   Wait for operation to be complete

4.   Examine contents of MPR at 774406.

On some PDP-11 systems this can be accomplished manually using the console. On other PDP-11 systems it is necessary to run a program such as given below. Start at 1000 and when it halts, examine memory location 1032.

To get status on unit 1, 2, or 3 modify location 1010 to 404, 1004, or 1404.

To reset drive modify location 1002 to 13.

1000	012737	Get Status Command
1002	000003	Use 13 to Reset
1004	174404	.
1006	012737	
1010	000004	Use 404, 1004, 1404 for Units 1 ,2 , 3
1012	174400	
1014	105737	Wait
1016	174400	
1020	100375	
1022	013737	Move Result to Memory
1024	174406	
1026	001032	
1030	000000	Halt
1032	000000	Result

C.4   GET STATUS ON AN RL8-A SUBSYSTEM

The following program will GET STATUS from unit 0. To access unit
1, 2, 3 change location 212 to 1102, 1202, 1302.

Start the program at 200 - at the first halt, the first byte of
the status word is displayed in the accumulator - at the second
halt, the second byte is displayed.

```
200        7300
201        1212              Get Status
202        6604
203        6601              Wait
204        5203
205        6615              Get First Byte
206        7402              Halt and Display Frist Byte
207        6615              Get Second Byte
210        7402              Halt and Display Second Byte
211        5200              Jump to Start
212        1002              Constant
```

C.5   OSCILLATING SEEK FOR RL11/RLV11

The following program will cause unit zero to perform an oscillating seek. To drive units other than unit 0, swap the unit number plugs or modify locations 1044 and 1054 to reflect the unit number in bits 8 and 9.

The number of cylinders involved is inserted into bits 15 through 7 and bit 0 is set in the switch register before starting the programs at 1000. If no switch register is available, modify location 1012 from 177570 to 001060 and put the number of cylinders in bits 17 through 7 and set bit 0 in location 1060.

The common values for the switch register are:

Number of cylinders (in decimal)	Value of Switch Register (in octal)
1	000205
85	025205
170	052405
255	077605
511	177605

1000	012706	Set Stack Pointer
1002	001000	
1004	012700	Set Device Address into R0
1006	174400	
1010	013701	Set Difference into R1
1012	177570	
1014	004537	Go Seek
1016	001032	
1020	042701	Change direction bit in R1
1022	000004	
1024	004537	Go Seek
1026	001032	
1030	000767	Loop Back
1032	105710	Wait
1034	100376	
1036	010137	Seek
1040	174404	
1042	012710	
1044	000006	
1046	105710	Wait
1050	100376	
1052	012710	Read header to kill time for SKTO
1054	000010	
1056	000205	Return

C.6   OSCILLATING SEEK FOR RL8-A

The following program will cause unit 0 to perform an oscillating
seek.   To drive units other than 0, swap unit number plugs.
Insert the number of cylinders into the switches before starting
at location 200.   The usual values for the switch register are: 1
cylinder=1, 85 cyl=125, 170 cyl=252, 255 cyl=377 and 511 cyl=777.

```
200          7201          Reset
201          6604
202          7604          Get Number
203          4221          Go Wait for Ready
204          3225          Store number
205          1225
206          6603          Seek
207          7325
210          6604
211          4221          Go Wait for Ready
212          7307          Read Header to Delay for SKTO
213          6604
214          1225
215          1226          Change Direction Bit
216          7500          Check for Time to Restore
217          5202          Loop to Start
220          5203          Loop
221          0000          Wait for Ready
222          6601
223          5222
224          5621
225          0000          Temp
226          4000          Constant
```

D.1   SPC CONSIDERATIONS

The RL11 is a Small Peripheral Controller (SPC) but does not unconditionally fit into any SPC slot. Early SPCs were always quad height modules or combinations of smaller (single or dual) modules that involved only four rows. Thus, the standard pin assignments applied only to rows C, D, E and F on a hex-height backplane. Many new options, such as the RL11, are hex-height modules and therefore require that rows A and B be vacant since some SPC slots use rows A and B for Unibus cables or power connectors. Som hex-height options require standard Unibus pinning on rows A and B and some require Modified Unibus Device (MUD) pinning. In the case of the RL11, the only connections used on rows A and B are the +5v and ground. Thus, these rows can be either standard Unibus or MUD pinning.

The early SPCs did not utilize Direct Memory Access (DMA) data transfers to/from memory and therefore those signals were not part of the original SPC pin assignments. Some of the newer options, such as the RL11, do utilize DMA transfers. There is a new pin assignment called SPC PRIME that includes these signals. If the R111 is to be used in an older (non-SPC PRIME) slot then it is necessary to ensure that the following signals are wired on the backplane.

- Pin CA1 – NPG In
- Pin CB1 – NPG Out
- Pin FJ1 – NPR
- Pin CV1 – AC LO
- Pin CU1 – +15v

If the slot has SPC PRIME pinning then another precaution must be taken. NPG continuity is maintained across an empty SPC PRIME slot by a backplane jumper from pin CA1 to pin CB1. This jumper must be removed whenever a DMA-type option is installed, such as an RL11, and the jumper must be added if the module is removed. This consideration is in addition to the normal Bus Grant Continuity card used in row D of all empty SPC slots.

D.2   CONFIGURATION CONSIDERATIONS

When configuring a Unibus system for the best priority assignments, two characteristics of a peripheral option must be taken into consideration. These are the peak word transfer rate and the Tl time (Tl time is a function of the peak transfer rate and the silo size). The RL11 has a peak transfer rate of 256kHz (3.9 microseconds/word) and a Tl time of 62.4 microseconds. This dictates its position in the priority scheme. The recommended priority scheme is listed below.

```
CPU
        Memory
        RK11/RK05
        TM11/TU10
        TC11/TU56
        RL11/RL01-RL02
        RJS04
        RM02
        RJP04
        RK611/RK06-RK07
        RP11C/RP03
        RJS03
        TJU16
        RF11/RS11
DB11
```

Other general configuration rules are:

- On a PDP-11 Unibus, a combination of two disk subsystems and a tape or floppy disk subsystem is considered maximum.

- On a PDP-11/70 system, one Unibus disk subsystem is considered maximum if there are Massbus disks.

- A disk subsystem should not be installed beyond a bus expander.