DEC-00-HTHAA-A-D

digital equipment international

TECHNICIAN'S HANDBOOK 1974

compiled by

Training Department

Digital Equipment International Ballybrit Galway Ireland

First Edition February 1974

Second Printing May 1974

Third Printing August 1974

Fourth Printing April 1975

Fifth Printing March 1977

Copyright © 1974, 1975, 1977

Digital Equipment International

3/77-15

CONTENTS

FOREWORD

The content of this book is draft information which has been compiled at short notice. Please inform your Training Department of any errors, ambiguities or omissions you find.

Any comments or suggestions concerning the format, content or scope of the book would be welcomed by the Training Department.

CALENDAR 1974/1975

NAME: _____

AREA: _____

1974 FISCAL CALENDAR

FIRST QUARTER

MONTH	S	M	T	W	T	F	S
JUL	1	2	3	4	5	6	7
	8	9	10	11	12	13	14
	15	16	17	18	19	20	21
	22	23	24	25	26	27	28
AUG	29	30	31	1	2	3	4
	5	6	7	8	9	10	11
	12	13	14	15	16	17	18
	19	20	21	22	23	24	25
SEP	26	27	28	29	30	31	1
	2	3	4	5	6	7	8
	9	10	11	12	13	14	15
	16	17	18	19	20	21	22
	23	24	25	26	27	28	29

SECOND QUARTER

MONTH	S	M	T	W	T	F	S
OCT	30	1	2	3	4	5	6
	7	8	9	10	11	12	13
	14	15	16	17	18	19	20
	21	22	23	24	25	26	27
NOV	28	29	30	31	1	2	3
	4	5	6	7	8	9	10
	11	12	13	14	15	16	17
	18	19	20	21	22	23	24
DEC	25	26	27	28	29	30	1
	2	3	4	5	6	7	8
	9	10	11	12	13	14	15
	16	17	18	19	20	21	22
	23	24	25	26	27	28	29

THIRD QUARTER

MONTH	S	M	T	W	T	F	S
JAN	30	31	1	2	3	4	5
	6	7	8	9	10	11	12
	13	14	15	16	17	18	19
	20	21	22	23	24	25	26
FEB	27	28	29	30	31	1	2
	3	4	5	6	7	8	9
	10	11	12	13	14	15	16
	17	18	19	20	21	22	23
MAR	24	25	26	27	28	1	2
	3	4	5	6	7	8	9
	10	11	12	13	14	15	16
	17	18	19	20	21	22	23
	24	25	26	27	28	29	30

FOURTH QUARTER

MONTH	S	M	T	W	T	F	S
APR	31	1	2	3	4	5	6
	7	8	9	10	11	12	13
	14	15	16	17	18	19	20
	21	22	23	24	25	26	27
MAY	28	29	30	1	2	3	4
	5	6	7	8	9	10	11
	12	13	14	15	16	17	18
	19	20	21	22	23	24	25
JUN	26	27	28	29	30	31	1
	2	3	4	5	6	7	8
	9	10	11	12	13	14	15
	16	17	18	19	20	21	22
	23	24	25	26	27	28	29

1975 FISCAL CALENDAR

FIRST QUARTER

MONTH	S	M	T	W	T	F	S
JUL	30	1	2	3	4	5	6
	7	8	9	10	11	12	13
	14	15	16	17	18	19	20
	21	22	23	24	25	26	27
AUG	28	29	30	31	1	2	3
	4	5	6	7	8	9	10
	11	12	13	14	15	16	17
	18	19	20	21	22	23	24
SEP	25	26	27	28	29	30	31
	1	2	3	4	5	6	7
	8	9	10	11	12	13	14
	15	16	17	18	19	20	21
	22	23	24	25	26	27	28

THIRD QUARTER

MONTH	S	M	T	W	T	F	S
JAN	29	30	31	1	2	3	4
	5	6	7	8	9	10	11
	12	13	14	15	16	17	18
	19	20	21	22	23	24	25
FEB	26	27	28	29	30	31	1
	2	3	4	5	6	7	8
	9	10	11	12	13	14	15
	16	17	18	19	20	21	22
MAR	23	24	25	26	27	28	1
	2	3	4	5	6	7	8
	9	10	11	12	13	14	15
	16	17	18	19	20	21	22
	23	24	25	26	27	28	29

SECOND QUARTER

MONTH	S	M	T	W	T	F	S
OCT	29	30	1	2	3	4	5
	6	7	8	9	10	11	12
	13	14	15	16	17	18	19
	20	21	22	23	24	25	26
NOV	27	28	29	30	31	1	2
	3	4	5	6	7	8	9
	10	11	12	13	14	15	16
	17	18	19	20	21	22	23
DEC	24	25	26	27	28	29	30
	1	2	3	4	5	6	7
	8	9	10	11	12	13	14
	15	16	17	18	19	20	21
	22	23	24	25	26	27	28

FOURTH QUARTER

MONTH	S	M	T	W	T	F	S
APR	30	31	1	2	3	4	5
	6	7	8	9	10	11	12
	13	14	15	16	17	18	19
	20	21	22	23	24	25	26
MAY	27	28	29	30	1	2	3
	4	5	6	7	8	9	10
	11	12	13	14	15	16	17
	18	19	20	21	22	23	24
JUN	25	26	27	28	29	30	31
	1	2	3	4	5	6	7
	8	9	10	11	12	13	14
	15	16	17	18	19	20	21
	22	23	24	25	26	27	28

2

TROUBLE SHOOTING

MAINTENANCE

The work of the computer technician in the manufacturing environment is part of a much wider subject - maintenance. Maintenance divides into two parts and our work contributes to each:

(a) Preventive Maintenance:

aimed at preventing unserviceability. The production of a reliable and high quality product is the foundation of the preventive maintenance programme at the customers site. The initial adjustments made during manufacture are to secure reliable as well as optimum performance.

(b) Corrective Maintenance:

fixing a piece of equipment which is not working properly or not working at all. In our environment there is a peculiarity - the equipment with which we deal will probably never have worked before.

Maintenance is closely related to another subject - RELIABILITY - which has a close bearing on both aspects of our work.

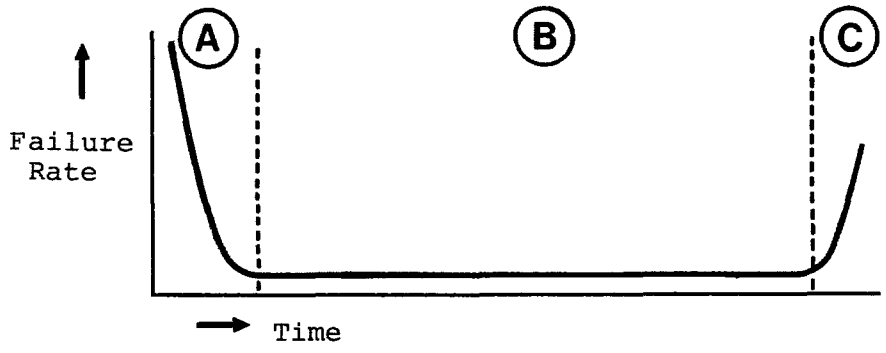
RELIABILITY

It is easy to understand that a piece of machinery must have a degree of reliability. No machine is perfectly reliable - the wear between moving parts takes care of that - but, on the other hand, few machines are totally unreliable, if we exclude those that are nearly worn out.

The reliability of a mechanism is related to its complexity and its quality and is measured as a Failure Rate (failures per "n" hours or "n" operations) or as a MEAN TIME BETWEEN FAILURES (MTBF).

Now consider a piece of electronic equipment. One might expect to encounter 100% reliability because of the lack of moving parts. Unfortunately the cycling of the components between their ON and OFF temperatures produces expansions and contractions that fatigue metal and plastics and give rise to electrical failures. Nevertheless the reliability of electronic devices is far greater than that of mechanical or electro-mechanical devices.

If we draw a graph of reliability against time for the working life of a batch of devices or components, the curve always comes out like this:



and three zones are easily discernible.

(A) Burn-In:

where initial failures occur: when the first contact with work weeds out delicate parts and exposes weaknesses.

(B) Useful Life:

with a relatively low rate of random failures.

(C) Wear Out:

when old age and wear and tear combine to produce a rising failure rate.

Of these three aspects of reliability our work is governed by the first - Burn-In, because our trouble shooting and testing procedures eliminate the weak and delicate components and represent a significant fraction of the Burn-In period of the systems we ship.

In trouble shooting newly manufactured modules, assemblies and sub-assemblies, the technician has to deal with faults stemming from two main sources:

(a) Component Failures

(b) Production Errors

COMPONENT FAILURES

Table 1 summarises the commonest faults associated with components. The components are given in order of failure rates. Although the typical rates quoted are for the Useful Life part of their reliability curves, the relative order of failure rates is approximately the same during Burn-in.

TABLE 1

COMPONENT	COMMON FAULT	TYPICAL CAUSES	% FAILURES PER 1000 HOURS
Lamps	Open Circuit	Fatigue from thermal and magnetic motion at ON/OFF	1.2
Capacitors (electrolytic)	Open Circuit Short Circuit	Stressed and broken connections Dielectric breakdown or leakage	0.2
Transistors (Si-power)	Performance Change Open Circuit Short Circuit	Seal or chip defect Broken bond or connection Crystalline breakdown - connection clearance	0.08
Capacitors (paper)	Open Circuit Short Circuit	Stressed and broken connections Dielectric failure	0.05
Transistors (Ge - power)		See Si Power Transistors	0.05
Capacitors Glass/Mica		See Paper Capacitors	0.03
Relays	Contact Failure Action Failure	Arcing - corrosion - fatigue Mechanical stress	0.03
Resistors (variable)	Change in value Open Circuit	Track wear - substrate cracks - turn shorts Wiper or connection failure	0.03
I.C's. (linear)	Performance Change Short Circuits Open Circuits	Chip and package defects - stresses Fouled connections Broken bonds and connections	0.03

COMPONENT	COMMON FAULT	TYPICAL CAUSES	% FAILURES PER 1000 HOURS
Zener Diodes	Performance Change	Chip and package defects	
	Short Circuits	Crystal failures	0.01
	Open circuits & intermittent connections	Bond and connection failure	
Switches		See Relays	0.01
Transformers	Short Circuits	Insulation failure or connector clearance	
	Open Circuits	Connector or winding failure	0.01
Transistors (Ge -low pwr.)		See Si-power Transistors	0.01
I.C's. Digital		See I.C's linear	0.01
Resistors (WW)	Value change	shorted turns	0.01
	Open Circuit	Fatigued winding or connector	
Transistors (Si Low Pwr.)		See Transistors (Si-power)	0.008
Multiway Connectors	High R	Galvanic corrosion	
	Open Circuit	Broken Pin	0.005
	Short Circuit	Bent Pin	
Diodes	Performance Change	Crystal defects	
	Short circuit	Crystal failure	0.005
	Open Circuit	Bond failure	
Resistors (film & comp)	Value Change	Substrate cracks - composition aging	
	Open Circuit	Cracking, connector failure	0.005

COMPONENT	COMMON FAULT	TYPICAL CAUSES	% FAILURES PER 1000 HOURS
Connection (solder)	Open	Fatigue	0.001
Connection (wrapped)	Open	Fatigue	0.0001

PRODUCTION ERRORS

No matter how rigorous the inspection procedure of the production areas a percentage of errors escape detection. Some of the more common errors are listed below.

COMPONENT	ERRORS
I.C's.	1. Reversed 2. Wrong type 3. Legs not inserted (bent under by insertion machine)
Resistors	1. Wrong Value 2. Wrong Place 3. One connector in wrong hole 4. Missing 5. Additional - inserted in space intended to be vacant 6. Diode or capacitor instead
Diodes	1. Wrong type 2. Wrong place 3. One connector in wrong hole 4. Missing 5. Additional - inserted in space intended to be vacant 6. Resistor or capacitor instead 7. Reversed
Capacitors	1. Wrong type 2. Wrong value 3. Wrong place 4. Connector in wrong hole 5. Wrong polarity 6. Diode or resistor instead 7. Additional - inserted in space intended to be vacant

COMPONENT	ERRORS
Etch	1. Cracked tracks (sometimes two or more at same site. 2. Break in track(s) 3. Lifted track 4. Missing etch - lifted or guillotined off on one or more edges 5. Solder shorts 6. Open circuit plated through holes Note - all defects may be concealed by components or handles.
Joints	1. Dry 2. Unsoldered 3. Excess solder shorting components or tracks. 4. Open circuit - apparently soldered.

TROUBLE SHOOTING

The process of trouble shooting divides into three stages:

1. Detection of the fault
2. Location of the fault
3. Repair of the fault

FAULT DETECTION

This merely implies "becoming aware" of the existence of a fault. Because, in our case, the technician is the first user of the equipment this stage holds few complications. This is not true in other environments where the technician has to unravel the ideas and actions of the user - where "faulty readers" need switching on and "dead videos" need the brightness turned up.

FAULT LOCATION

The technician can use a number of different methods to locate a fault. He can:

(a) Start at the output end of a system and search back towards the input until he finds the point at which the "signal" stops.

(b) Start at the input end of the system and search forward to locate the point at which the "signal" is lost.

(c) Start half-way between input and output and move forward to a new half-way point if the "signal" is present, or backward if not.

(d) Cast about at random until he discovers the fault.

(e) Gather all available information and use his power of reasoning and his theoretical knowledge to deduce which components have failed.

These methods have names. They are known respectively as:

(a) Output - to - input.

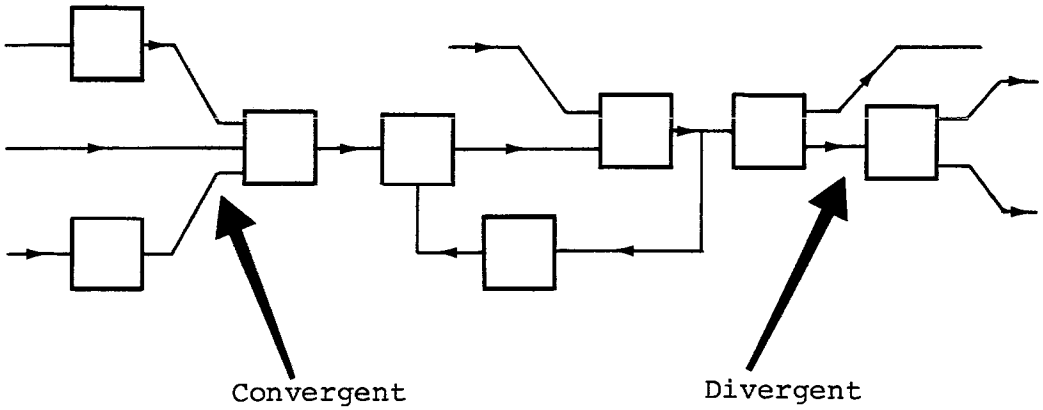
(b) Input - to - output

(c) Half split

(d) Random or non-systematic

(e) Theoretical analysis or non-sequential.

If we consider these methods applied to this functional diagram.



(a) Output-to-input is of most use in the convergent area (a lot of combinational logic falls into this category).

(b) Input-to-output is of most use in the divergent area.

(c) Half split is the fastest way to identify the faulty area of the system but is applicable to a system with a long serial aspect and which, like the diagram, can be considered in "functional" blocks.

(d) Random is difficult to justify.

(e) Theoretical analysis, for ordinary mortals, is likely to be a technique to support either a, b, or c.

Generally speaking, a reasonable plan would be to use the half split method to localise the area of the fault and then to use output-to-input or input-to-output according to the nature of the circuitry in that area.

To support the methods of fault location there are certain 'tools' at the disposal of the technician. Some of these, alone or in combination, are powerful enough to obviate the need for a formal method of fault location but this is only true when the system or fault is relatively uncomplicated. Usually these "tools" are included as techniques or aids in the location sequence. They are listed below in the order in which they should be of use when tracing an obscure fault in a large system to component level:

a) Logical Approach Work deliberately, eliminating the irrelevant as you go so that each decision has only to be made once. Untidy thinking often sends us round the same loop of deduction several times - with varying results for each cycle.

b) Pencil and Paper An invaluable aid to the previous item allowing us to work out and record the most logical approach to the fault. When having second thoughts later on we have a record of the sequence of reasoning - complete with its errors.

c) Knowledge If you don't know how the thing works then you are reduced to the RANDOM method of fault location with the added disadvantage of not knowing what you are looking for. If you have only a partial knowledge then every deduction you make will be suspect and surrounded with alternatives.

d) Experience As time passes the technician accumulates a mental file of faults which eventually separates into groups of related faults. The diary section of this book is intended to help this process.

e) Symptoms Make sure that you use all of the data that the hardware offers: all lamp and register indications and switch settings. Note the effect of, and response to, manual operation. If the correct output is not obtained from a system then the incorrect output, if any, may be significant.

f) Diagnostics. This is an extension of the previous item, but the power of repetitive self-testing is realised against intermittent and partial failures. Too often the reserve of diagnostic programmes is inadequately used. Make sure that the programmes and listings are up to date.

g) Programming. Vital to the selection, understanding and interpretation of diagnostics and vital for the generation of your own test programmes - another neglected technique.

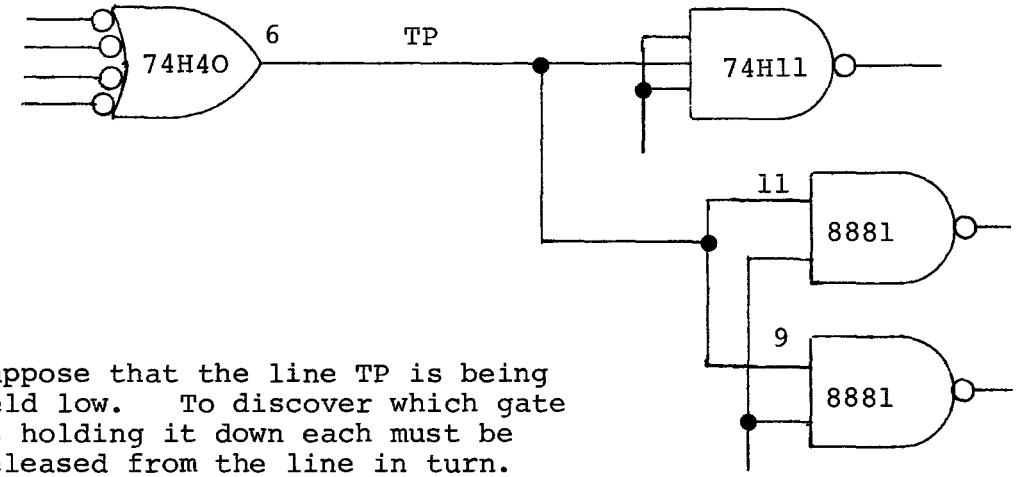
h) Documentation. Manuals, Handbooks, Prints, Timing diagrams and Flow-charts - OF THE CORRECT REVISION. The flow-charts and timing diagrams are generally underestimated. They are the only source of dynamic information - the data is presented with the provisos of relative timing included.

j) Substitutions. The location of a fault within a particular module or assembly can be confirmed by substituting an identical item that is known to be serviceable. The occasional substitution of a good module also checks the continued serviceability of the other parts of the system which may have suffered during the trouble-shooting process.

k) Inspection. A close examination for production errors at the suspected site can often reveal the cause of the fault.

l) Test Equipment. The intelligent use of test-equipment which is well kept and properly calibrated includes the frequent checking of its performance - 'scope probes need frequent checking.

m) Hand Tools. Generally associated with the repair of faults but often useful in the final stages of fault location. In this situation, for instance:



Suppose that the line TP is being held low. To discover which gate is holding it down each must be released from the line in turn.

By sucking away the solder from, say - pin 6 of the 74H40 and checking that it is isolated from the etch with a multi-meter the line is disconnected from the gate (without damaging the IC) and its state can be checked.

At this final stage it is sometimes possible to combine the rectification of the fault with the last stage of fault location. If, in the example above, the two 8881's were in the same IC and one of them were known to be at fault the obvious course of action would be to change the IC.

The way in which a technician works varies from fault to fault but in each case the sequence of events will include some of the methods and techniques mentioned here. The order in which they are used is again a function of circumstances and can differ widely from the order suggested here. For instance - the half-split method may be found to be useless for identifying the faulty function at system level but ideal for pin-pointing the faulty component in a sub-assembly.

FAULT RECTIFICATION

The action taken to remove a fault from a system will usually involve making an adjustment or replacing a component. In both cases you will need hand tools.

TOOLS

Keep your tools safe and in good condition. They will stay in good condition longer if you don't lend them. Several Tools need special attention:

a) Soldering Iron Keep at least two bits - one fine point and one long chisel. The fine point serves (for technicians dealing with modules) as a general purpose bit but having such a small surface area for its volume it gets very hot and is hard to keep in good condition. It also tends to develop a pronounced hook at the tip when used for heavier work and this can lead to damage in delicate work. For heavier jobs change to a chisel bit. The occasional bit change removes the oxide dust from the element body and helps to keep the iron efficient. Bit changing can be carried out when the iron is hot by manipulating the retaining collar and hot parts with pliers. Bits should be cleaned frequently and for this reason the sponge must be moistened often. If ever the flex of the iron gets damaged or burnt have it replaced.

b) Cutters Keep a fine pair for working on IC's. A narrow point is needed to clip the pins cleanly. When trimming pins or leads make sure the clippings are aimed in a safe direction.

c) Solder Sucker Do not modify the action of a solder sucker by tampering with the spring. The intensity of its action can be adjusted at the point of work by tilting the nozzle to allow extra air to enter. Do not use

oily or greasy lubricants in the bore of the sucker - they will destroy the internal washers. To maintain an efficient action the cylinder should be cleared of debris frequently.

SOLDERING

The object of a soldered joint is to join two pieces of metal for electrical continuity with a degree of mechanical strength. In the electronics industry the two pieces of metal will almost always be copper because:

a) It is a good conductor of electricity

b) It is relatively cheap in comparison to silver

c) It is flexible and withstands wear

d) It is a good conductor of heat

If an attempt is made to solder together two pieces of bare copper wire with the aid of a dry iron and some bar solder it will be impossible to produce a soldered joint. To produce a successful joint the solder must be able to flow freely into the pores of the metal: this freedom to flow is prevented by the presence of copper oxide on the surface of the metal and also by sundry other contaminants.

To remove the oxide and contamination a fairly savage flux would be needed - a substance like 'killed spirit' which would be too corrosive for our use. So, in practice we dont attack copper oxide with severe fluxes: we prevent the copper from oxidising by plating it with a thin layer of another metal which does not oxidise so readily and which solders easily (tin and tin-lead coatings are common). The plating oxidises, of course but this oxide is easy to deal with and a mild flux is adequate. For our purposes the solder is made as a fine tube and the flux is put in the tube.

Solder manufactured in the form of wire with the flux inside is known as cored solder. The flux is usually resin which is comparatively mild but strong enough to deal with ordinary surface contamination.

There are two jargon words associated with soldering:

Wetting. When a surface of metal has a coating of bright molten solder adhering to it the surface is said to be wetted. The flowing on of the molten solder is called wetting.

Tinned. When the wetted surface has cooled it is known as a tinned surface. A soldering iron is tinned by cleaning the bit and applying a coating of bright molten solder - in other words, by wetting the bit with solder.

To make a soldered joint:

a) Tin the bit of the iron and wipe or shake off surplus solder.

b) Heat the joint by applying the tip of the bit so that the joint is between you and the bit -

c) At the same time apply the tip of the solder to the joint from the front.

d) At the moment the joint 'wets' remove the solder and then the iron.

e) Keep the joint perfectly still until the solder is seen to set.

The amount of solder applied to the joint is a matter of timing at the instant of wetting. The aim is to produce a joint with a concave fillet of solder -the upper photographs on page 4-62 of the Workmanship Standards Manual illustrate the required effect.

Surplus solder at the joint can run through a plated-through hole and cause solder shorts beneath components on the other side of a board. On the other hand, an attempt to make the joint with insufficient solder causes overheating and the formation of dusty oxides which the flux cannot remove.

Above all - any movement of a joint before it has set must be avoided. Movement of a setting joint produces a dry joint with a typical dull grainy appearance. Dry joints have little or no mechanical strength and electrical properties which can vary from open circuit to semi-conductor rectification.

I C REMOVAL

The following sequence assumes that the IC is not to be saved for re-use:

a) Cut the legs of the IC at the top where they enter the body of the device using a pair of miniature side-cutters. Remove the body of the IC.

b) Remove each leg by applying heat and gently withdrawing it from side 1 using a pair of fine-nosed pliers. If a leg is reluctant to move, leave it.

c) Turn the board over and heat each hole individually, removing solder with a de-soldering tool. If any remaining leg is retained by a bend at the tip it can be straightened and the removal completed from side 1. Where no obstruction is apparent the addition of a little extra solder may facilitate removal.

d) Clean both sides of the area with solvent and inspect for damage.

NOTES

3

GENERAL NOTES

OPERATIONAL AMPLIFIERS

The idea of the amplifier as a 'component' to be inserted into a piece of equipment and adjusted for the required performance seems to have originated in the late 1940's. This idea became a reality in the 1960's with the arrival of the integrated circuit.

The underlying principle of such a versatile amplifier is that the parameters of an amplifier can be set by adjusting the amount of FEEDBACK between its input and output terminals.

For an 'op-amp' to be truly versatile it would need to have:

(a) Infinite gain
(b) Infinitely High input impedance
(c) Zero output impedance
(d) Infinite bandwidth

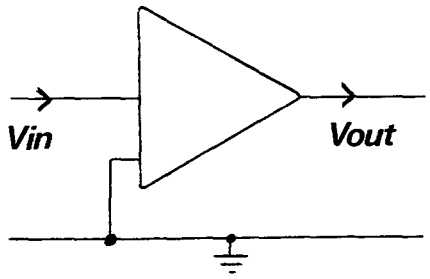
We could, of course, add small physical size and minute power consumption.

In practice the op-amp is a very high gain, wide band, direct-coupled amplifier with a performance that can be pre-set over a wide range by selecting a suitable feedback arrangement.

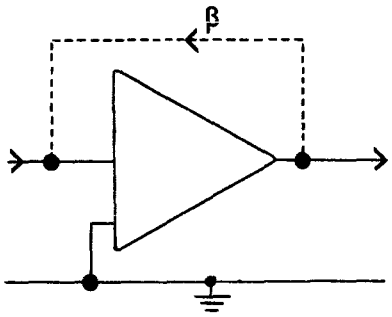
FEEDBACK

In a simple amplifier, having a gain of A

Vout = A x Vin



If we feed back a portion of Vout the performance of the amplifier is modified. The fraction of Vout fed back is designated β so



V fed back = β.Vout

So, with Feedback, Vin becomes Vin + β.Vout and since Vout = A.Vin

$$Vin' = Vin + \beta.A.Vin$$

Now Gain = $\frac{Vout}{Vin}$

So gain with feedback, A' = $\frac{A.Vin}{Vin + \beta.A.Vin}$

$$A' = \frac{A}{1 + A\beta}$$

Let's try an example:

Suppose we have an amplifier with a gain of 50

If Vin = 1V

$\therefore$ Vout = 50V

Now suppose we feedback 1% of this, i.e. β = 0.01

Now Vin = 1 Volt + (0.01 x 50)

= 1V + 0.5V

= ?

Remember, Vin and Vout are a.c. signals so 1V + 0.5V is a matter of relative phase. Let us exclude all but IN-PHASE and ANTI-PHASE.

If β is in-phase 1V + 0.5V = 1.5V so now Vin is bigger, Vout gets bigger. βVout gets bigger so Vin gets bigger again ..... This is a POSITIVE FEEDBACK and gives us impressive gain figures, instability and oscillators.

Let us concentrate on the ANTI-PHASE condition:

$$\begin{aligned} & 1V + 0.5V \text{ anti-phase} \\ = \; & 1V - 0.5V \\ = \; & 0.5V \end{aligned}$$

So Vout drops to 25V and β drops to 0.25V.....

It is quicker to use the "gain with feedback" formulae.

$$A' = \frac{A}{1 + A\beta} = \frac{50}{1 + (50 \times 0.01)}$$

$$= \frac{50}{1.5} = 33.3\dot{}$$

So Vout settles at $33\frac{1}{3}$ V.

In practical op-amps, gain is very high. If we feedback a large portion of Vout

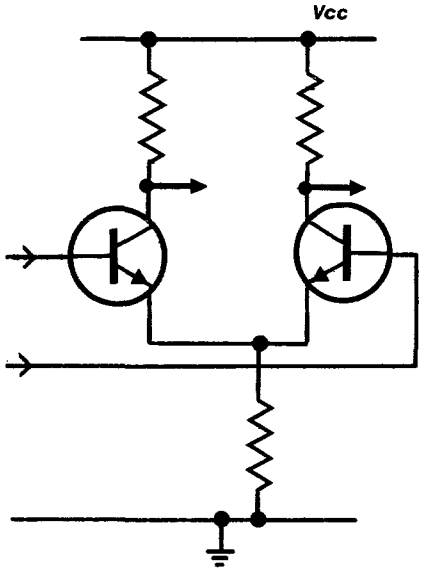
$$1 + A\beta \simeq A\beta$$

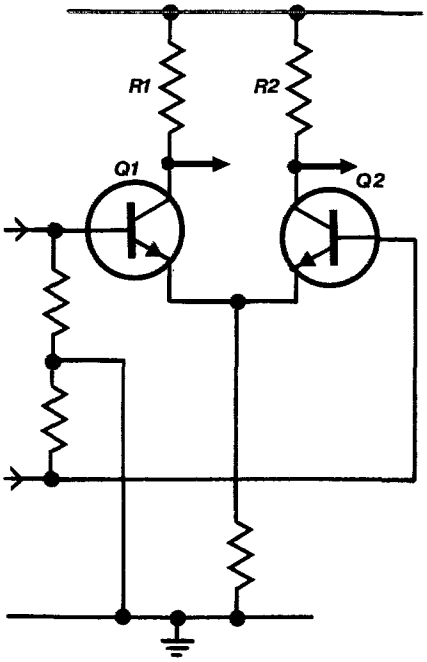
$$\text{so Gain} = \frac{A}{1 + A\beta} = \frac{A}{\beta A} = \frac{1}{\beta}$$

So the feedback fraction sets the gain and since β is determined by the feedback components, the gain of an op-amp is selectable for any particular application (within reason).

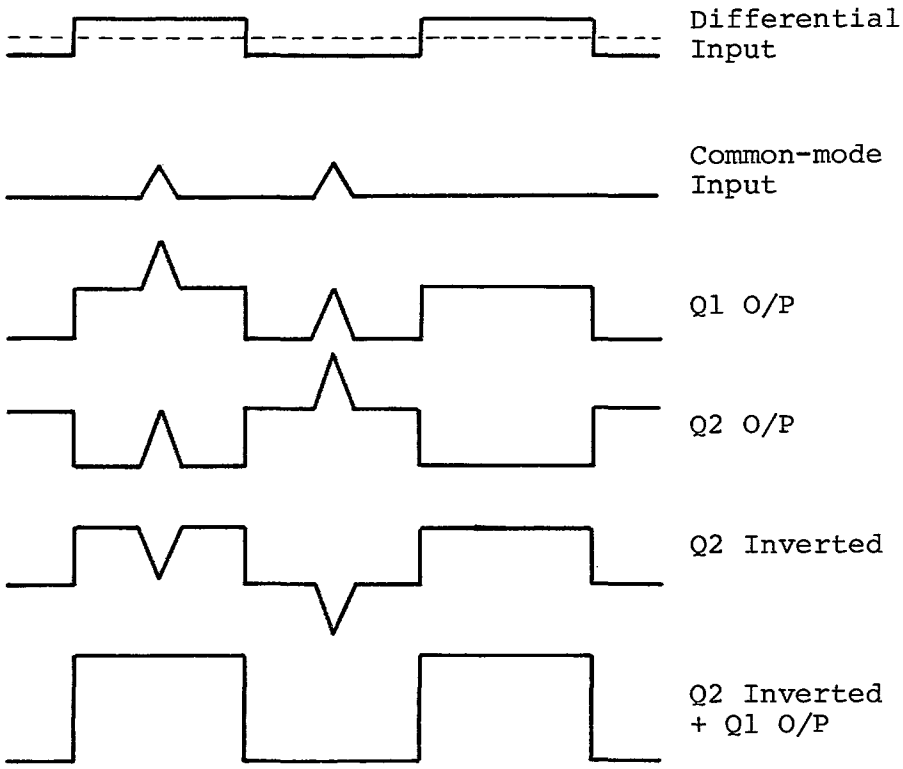
THE DIFFERENTIAL AMPLIFIER

Several circuits are suitable for use as direct-coupled amplifiers but, of these, the differential amplifier has superior stability and interference rejection qualities. The dual input arrangement of this circuit gives the op-amp much of its versatility.

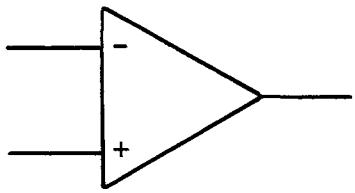




If Q1 and Q2 are matched and if R1 = R2 then in the quiescent state the two collectors will be at the same potential. If we apply a differential signal to the input terminals, (inputs are driven with opposite polarities) one collector potential will rise and the other will fall - in other words antiphase outputs will result. But - if a signal affects both inputs equally, in the same sense (noise, for example) then both collectors will respond in phase. This in-phase response to common-mode inputs can be used to cancel interference.



Because the differential amplifier forms the first stage of an op-amp the symbol is:



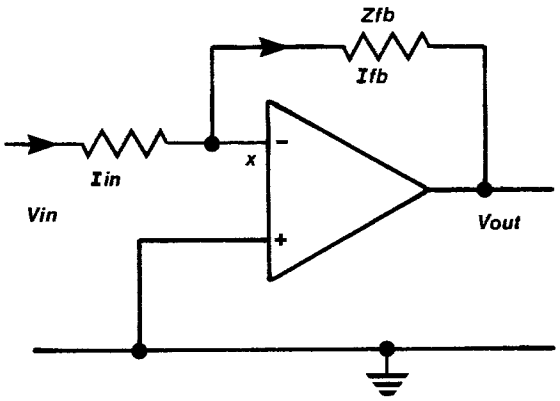
where

+ is the non-inverting input
- is the inverting input.

This allows the selection of either positive or negative feedback.

VIRTUAL EARTH

If we consider the op-amp in the inverting mode:



Because the gain is extremely high then the current into the amplifier at point X must be virtually zero; and if this is so then the voltage at point X must also be virtually zero. In fact, point X is a virtual Earth - approximately at ground without actually being grounded - under all operating conditions.

We must now account for Vin and Iin. Vin must be dropped across Zin and Iin can only flow through Zfb, as Ifb. So if Iin = Ifb and point X is at ground (virtual) then

$$\frac{Vin}{Zin} = -\frac{Vout}{Zfb}$$

$$\therefore \frac{Vout}{Vin} = -\frac{Zfb}{Zin} = \text{Gain}$$

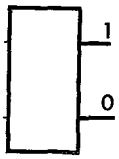
This is a re-statement of the earlier argument but in a more practical context. It is also an elaboration of Fig. 2, Page 272 of the 1973-74 LOGIC HANDBOOK - part of an article on op-amps to which the reader is referred for terminology and configuration details.

FLIP FLOPS

If we think of flip-flops as logic elements, and not as sophisticated bistable circuits, it is surprising how little there is to know about them. Since we spend so much of our time dealing with flip-flops we must be clear about their operation.

There are certain factors common to all types of flip-flop:

a) Complementary Outputs:

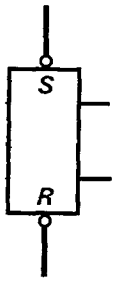


Every flip-flop has two outputs which we know as the 1 and Ø outputs. They are also called Q and $\bar{Q}$, true and false, ON and OFF, and SET and RESET. These two outputs are usually opposite in state - if one is Hi then the other is Lo and vice-versa.

When 1 is Hi and Ø is Lo the flip-flop is said to be SET.

When 1 is Lo and Ø is Hi the flip-flop is said to be RESET.

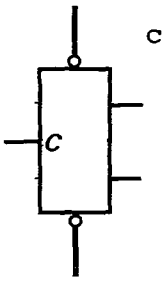
b) SET and/or RESET Inputs:



Most flip-flops have inputs which can force the outputs to a particular state. These inputs are enabled Lo. If held high they have no effect on the operation of the device. The input which forces the set condition is called SET (sometimes PRE for PRESET) and the other, which forces Reset is known as RESET.

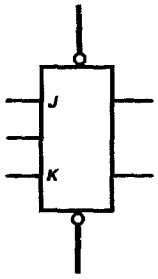
Note: If both inputs are made Lo at the same time both outputs go Hi - normally an undesirable state.

c) Clock Input:



Most flip-flops have a clock input that controls the insertion of binary data. The clock pulse usually causes the flip-flop to record the input state prevailing before the pulse.

J-K FLIP FLOP



The J-K has two data inputs, designated J and K. Data applied to these inputs will not affect the outputs

UNTIL THE CLOCK PULSE ENDS.

The effect the inputs have on the outputs is quite definite. On the trailing edge of the clock pulse the outputs:

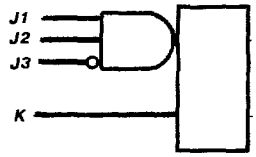
Do not change if J and K are both Lo.

Complement if both J and K are Hi.

Otherwise they copy the inputs.

Inputs		Outputs when Clock Pulse Ends	
J	K	1	0
Lo	Lo	No Change	
Lo	Hi	Lo	Hi
Hi	Lo	Hi	Lo
Hi	Hi	Changes	

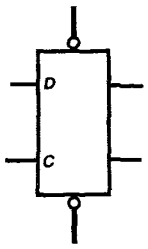
Sometimes the J or K or both inputs have combinational gating included within the device. For example:



Here the J input is determined by J1, J2, and J3 where

$J = J1 . J2 . \overline{J3}$

D-TYPE FLIP FLOP



The D-type has a single information input, D. The output responds to the state of the D input

AT THE START OF THE CLOCK PULSE.

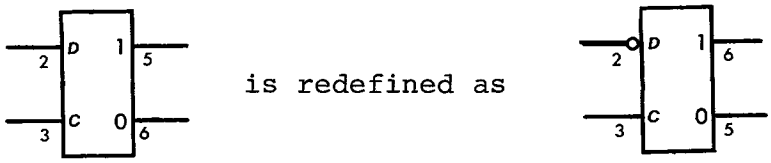
It will not respond to a change of input taking place during or after the pulse. The behaviour of the D-type at the leading edge of the clock pulse is simply:

a) If D is Lo it RESETS (or stays Reset).

b) If D is Hi it SETS (or stays Set).

REDEFINED D-TYPE FLIP FLOP

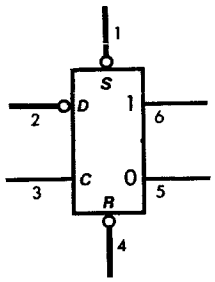
In modern logic circuitry many signals are true (asserted) when Lo. This means that the D-type often has its "active" condition as RESET - a state associated with "inactive". This situation is remedied by re-drawing the device with the Ø output in the 1 position and vice-versa. In other words, the pin numbers for the outputs are reversed; so for the 7474:



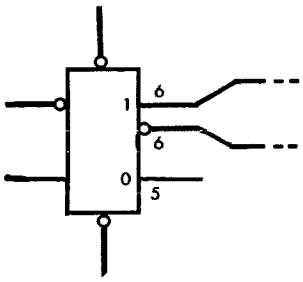
Notice that the sense of the D input is inverted to signify the change.

We now have a flip-flop that looks SET when responding to a Lo assertion. All that is needed now is to change the Set and Reset input titles so that their effects match the new arrangement:

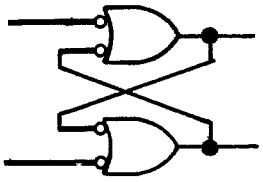
This gives the final redefinition as:



One final complication. Sometimes outputs are shown twice on the same flip-flop - one for each sense of the output. In other words an output is drawn for the circuits it affects when Hi and again for those it affects when Lo.



SET/RESET FLIP FLOP



This flip-flop has no clock input.

If a Lo is applied:

(a) to the Set input the flip-flop SETS (or stays set)

(b) to the Reset input the flip-flop RESETS (or stays Reset)

(c) to both inputs both outputs go Hi, but on removal of the inputs the output state is unpredictable.

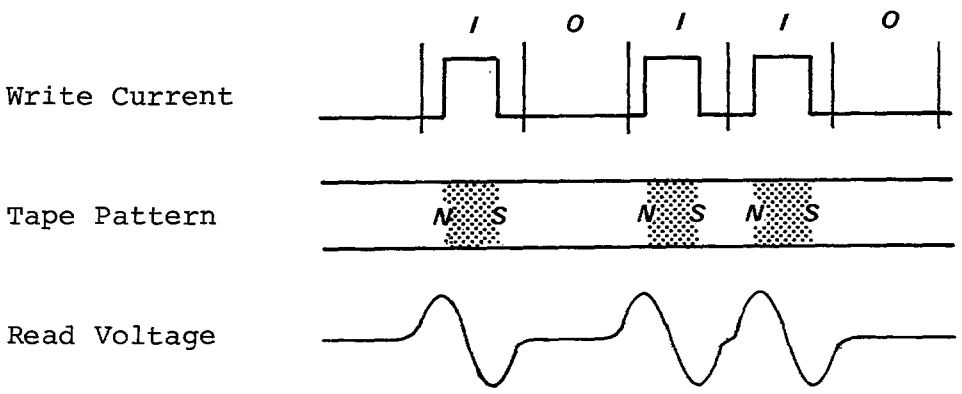
MAGNETIC DATA RECORDING

These elementary notes summarise the methods of magnetic recording available to the engineer. Some methods not in current use are included to indicate the advantages of those that are.

The bit cell boundaries, pulse directions and field polarities have been chosen arbitrarily as innumerable variations will be encountered in practice. Alternative titles are given where a recording technique is known by more than one name.

METHOD

Pulse Recording
or Return to Zero (single polarity)

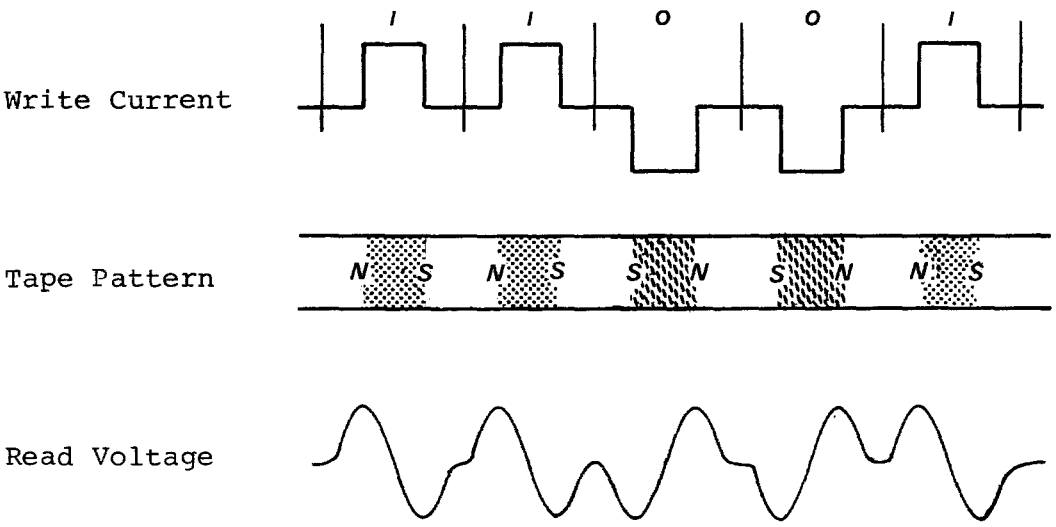


Pulses of Write Current are applied for 'ones'. Zeros are signified by absence of pulse.

Disadvantage: Since zero bit cells contain no event the data is not self-clocking.

When the tape or surface has been pre-magnetised (saturated by a D.C. erase) this method is known as Return to Saturation or Return to Bias.

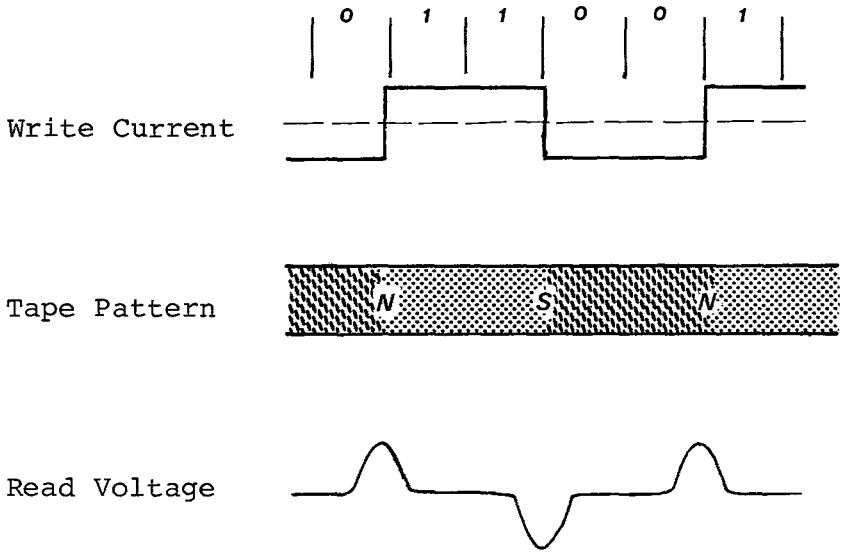
METHOD: Return to Zero
or Return to Zero (2 polarity)



A development of the previous method with zeros written by current pulses in the opposite direction. As there is an event in each bit cell the data can be self-clocking. The greater signal range gives an improved signal to noise ratio.

METHOD

Non-return to Zero
or NRZ - Change on Change

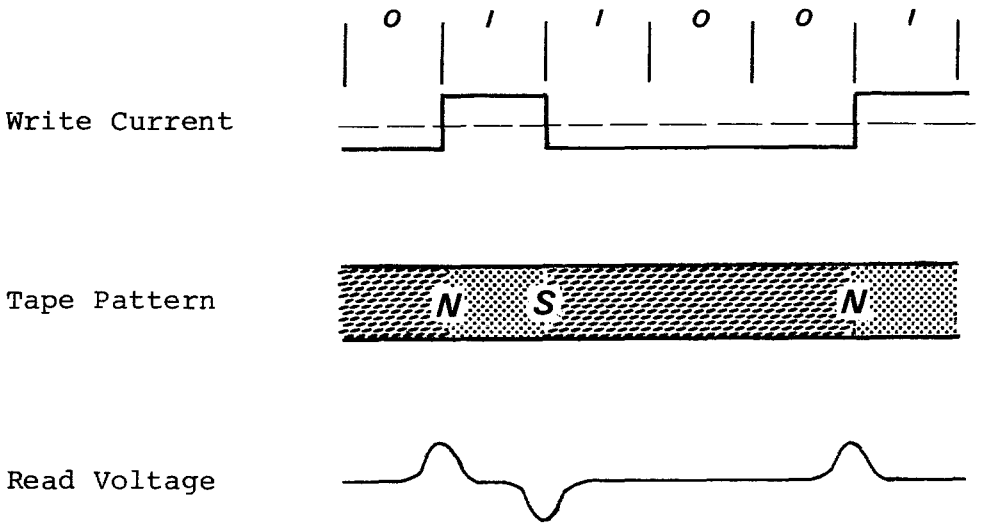


The write current reverses only on bit changes, i.e. Ø to 1 or 1 to Ø.

Note that write current always flows and that data is not self-clocking as some bits are not marked by an event.

METHOD NRZI known variously as:

i) Non-return to Zero Inverted
ii) Non-return to Zero Inhibited
iii) Non-return to Zero Incremented
iv) NRZ change on ones.



Write current reverses to indicate a 1. No reversal for a Ø.

Not self clocking. Preferred to NRZ as any error affects only one bit whereas an error in NRZ propagates i.e. affects all subsequent bits in the read cycle.

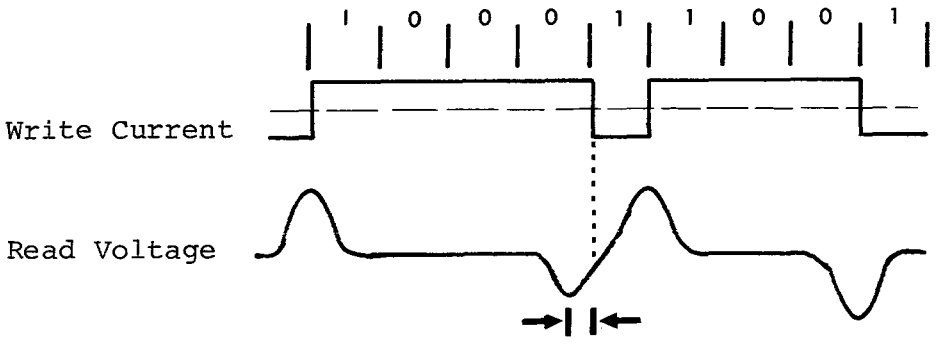
Used in several D.E.C. products including TU1Ø, TU2O, DF32, and RSØ8.

SYSTEM LIMITATIONS

The recovery of data which has been recorded using the techniques described above simply involves an amplitude detection system (and suitable clocking arrangements to mark the data times for the NRZ systems).

Noise pulses caused by tape imperfections do not usually have sufficient magnitude to be interpreted as data but any large pulse would also have to coincide with data-time in the NRZ systems.

So - error rates can be insignificant when signals have to meet both amplitude and timing standards. Unfortunately, these standards limit the amount of data we can record on a given length of surface since compression of the data produces wide variations in amplitude and timing. For example, if we raise the data rate in NRZI



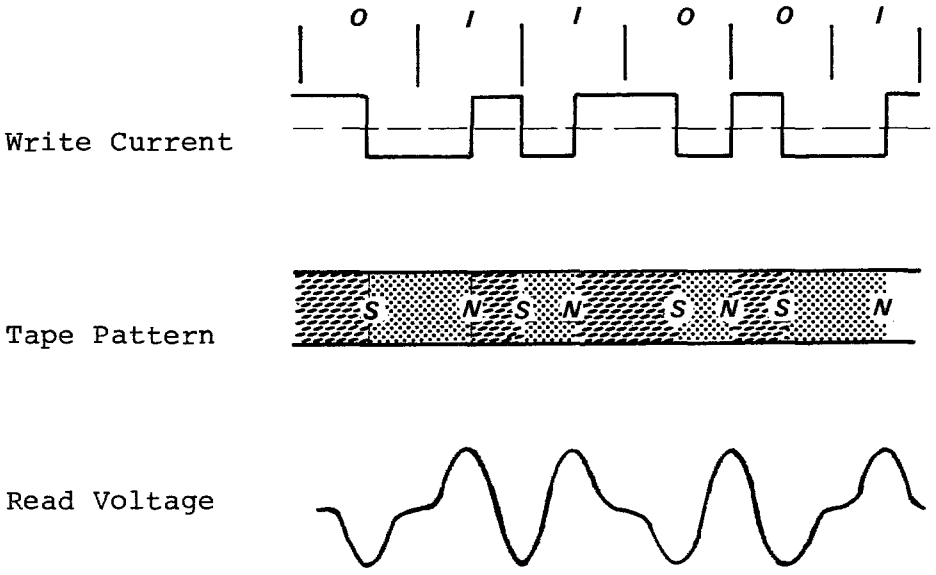
certain pulses degrade both in amplitude and timing: for two reversals close together the detected voltage for the first is just getting established when the field of the next reversal influences it causing an early peak of reduced amplitude.

It is possible to overcome this deficiency of NRZI by detecting the zero-crossings instead of the peaks of the read waveform. This modified form of NRZI is used in the RK05.

NRZI used with zero-crossing (more accurately, zero-approaching) detection gives low error rates and high data density. There remains the one major disadvantage - the data is not self-clocking - which means that in multi-track systems head skew, both static and dynamic, can interfere with the relationship between the clock and data tracks. Also, in single track systems clock information must be combined with data.

For these reasons use is often made of phase and frequency modulation techniques, the commonest of which is described overleaf.

METHOD Phase Modulation
or Manchester
or Phase Encoded

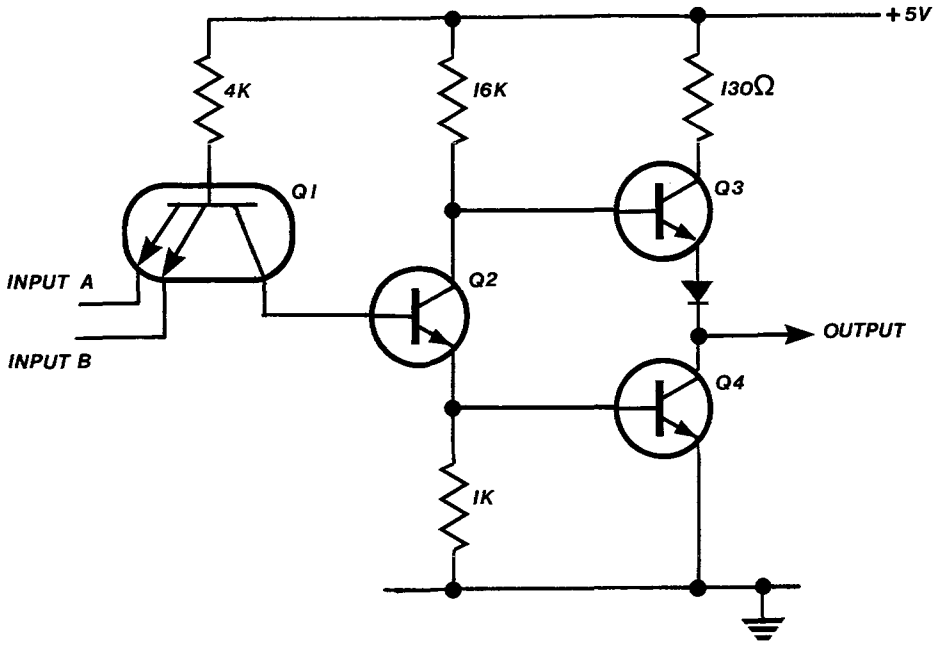


A 1 is indicated by a flux reversal in one direction and a Ø by a reversal in the other direction. Information is retrieved by merely detecting the polarity of the output pulses.

However, some intermediate flux reversals are necessary to enable transitions of the correct polarity to be made and thus frequencies of up to twice the bit rate are encountered.

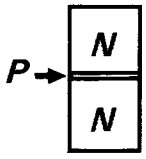
This form of recording is used in the TU60 and Dectape.

THE TTL NAND GATE

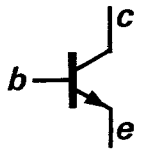


This circuit is fundamental to the system of TTL logic and yet the conventional analytical approach to its operation is not easy to grasp, especially for the technician encountering logic for the first time.

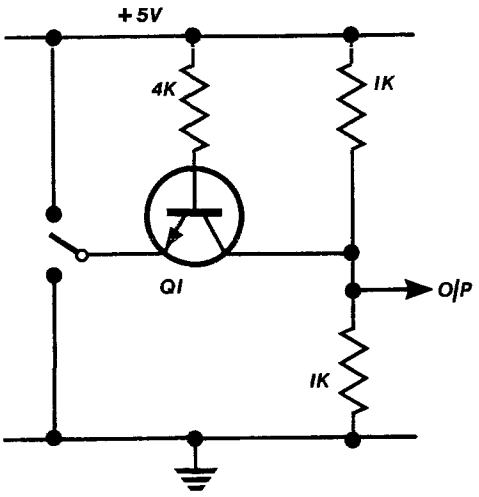
An N-P-N transistor consists essentially of two blocks of N type semi-conductor separated by a thin layer of P-type.



We usually think of the transistor as its symbol is drawn, with the base controlling the flow of electron current from emitter to collector. But, when a transistor is used as a switch it will still work if the collector and emitter are interchanged: both are N-type and even in discrete transistors where emitter and collector dopings are markedly different, the device will still function upside-down.

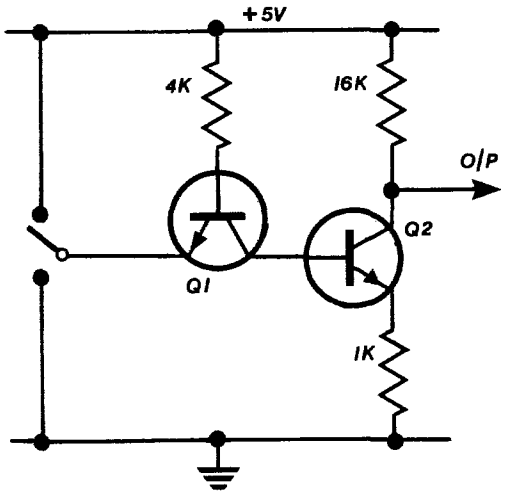


Consider this circuit:-



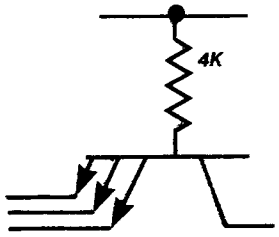
The emitter of the transistor can be switched to either Ø V or +5V. If it is taken to Ø V then, because the base is high it will switch the transistor on and connect the output point to Ø V. (O/P goes to "about" Ø V - in fact 0.4V = Vce (sat) for any transistor).

When the switch is taken to +5V the transistor works upside-down; the emitter behaves as a collector and the collector as an emitter. Now the transistor is on (still with its base high) but this time the output point is connected to +5V via an "ON" transistor so output goes to about +5V.

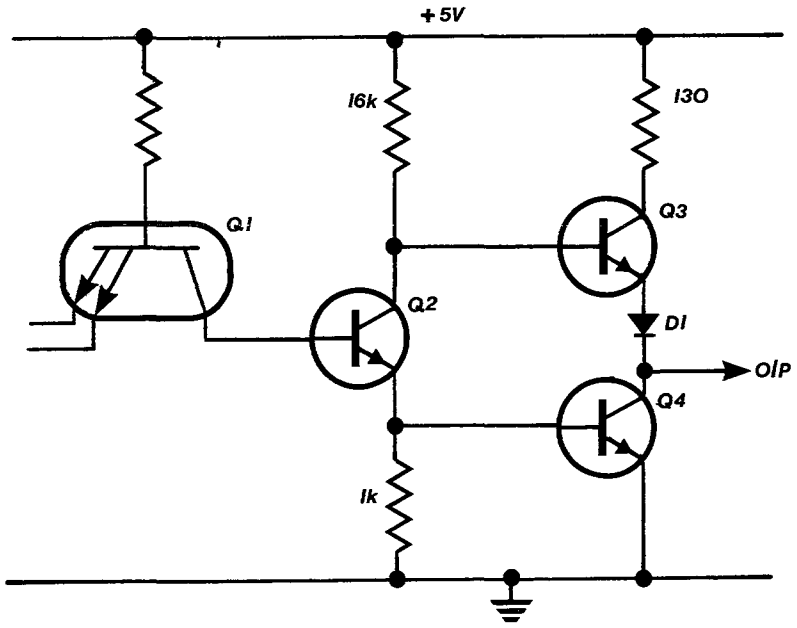


If the collector of Q1 is taken to the base of a second transistor Q2, then Q2 will be cut off when the switch is to ground (because Q2 base is taken to about Ø V via Q1) and the output will rise to +5V. When the switch is at +5V, the base of Q2 is high: Q2 conducts heavily and the divider effect of the 16k and 1k resistors combined with Vce (Sat) gives an output of about 0.7V.

To provide multiple inputs Q1 is given a number of emitters. If one or more of these is taken LOW the transistor works as a normal N-P-N and Q2 is off. However, if all the emitters are HIGH then Q1 operates in its inverted mode and turns on Q2. This gives a NAND function.

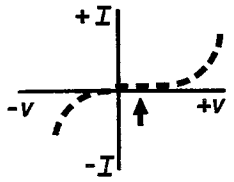


TOTEM POLE OUTPUT



Q2 is used as a phase splitter and drives a cascade pair Q3 and Q4. When Q2 is cut off its emitter is at ground and Q4 must also be off. Q2 collector is at +5V - so is Q3 base. Q3 is therefore on and the output is High.

When Q2 is conducting its emitter is a fraction of a volt above ground - enough to turn on Q4 and switch the output to ground. Q3 base is slightly higher in potential than Q4 base and Q3 would like to conduct - but diode D1 has to operate in the flat part of its characteristic, just above ØV, and limits the current to a negligible value.



FORMULAE

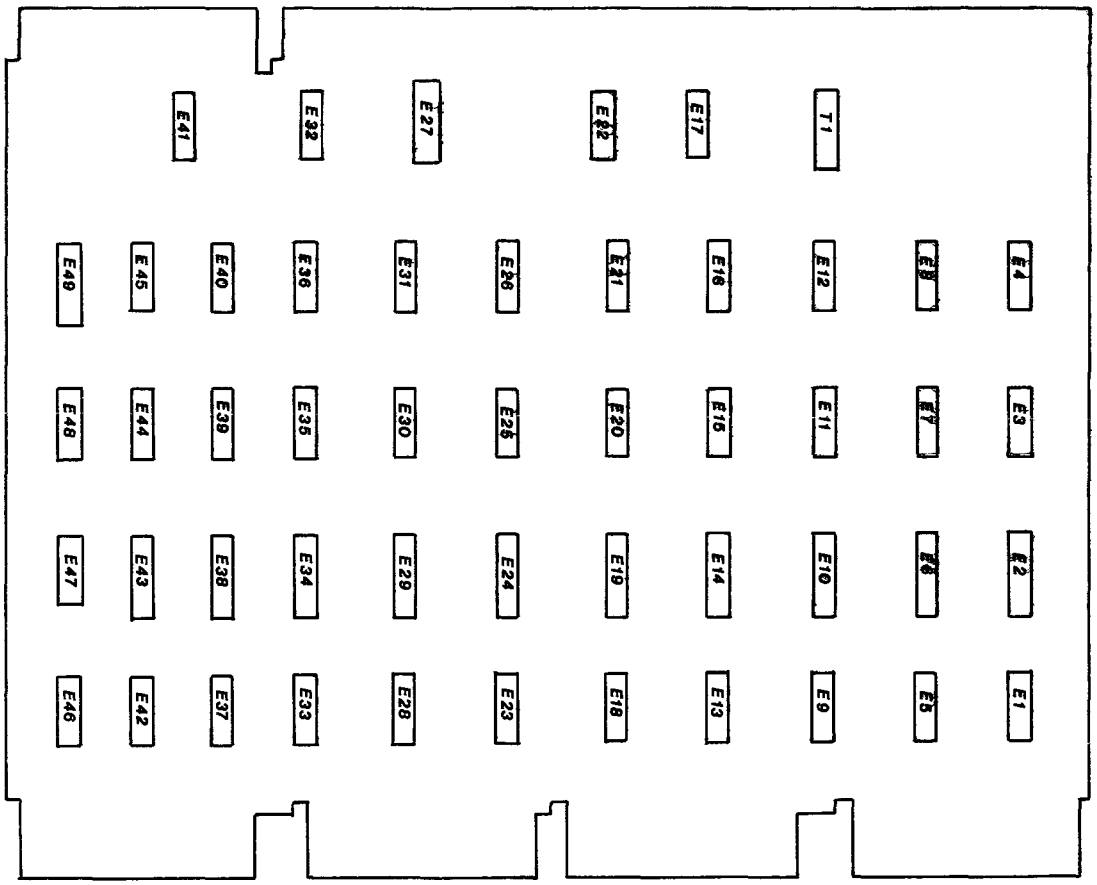
Resistors	$R = R_1 + R_2$ $1/R = 1/R_1 + 1/R_2$ $R = \frac{R_1 \ R_2}{R_1 + R_2}$	in series in parallel 2 in parallel
Ohms Law	$I = E/R \quad R = E/I \quad E = IR$	
Power	$P = VI \quad P = I^2R \quad P = \frac{E^2}{R}$	
Charge in Capacitor	$Q = VC$	Q in Couls C in Farads V in Volts
Capacitors	$1/C = 1/C_1 + 1/C_2$ $C = \frac{C_1 \ C_2}{C_1 + C_2}$ $C = C_1 + C_2$	in series 2 in series in parallel
Capacitive Reactance	$X_c = \frac{1}{2\pi fc}$	f in Hz
Charge/ Discharge of CR	$T = 5CR$	T = time to 99.7% change
CR Time - constant	$T = CR$	T in Secs
Capacitor Charge State	$V = V_s e^{-(\frac{t}{cr})}$	V = aiming voltage e = 2.7182

Inductors	$L = L_1 + L_2$	in series
	$1/L = 1/L_1 + 1/L_2$	in parallel
	$L = \frac{L_1 \quad L_2}{L_1 + L_2}$	2 in parallel
	$L = L_1 + L_2 + 2M$	series with mutual inductance
	$L = \frac{L_1 \quad L_2 - M^2}{L_1 + L_2 + 2M}$	parallel with mutual inductance
LR Time constant	$T = L/R$	T in secs. L in Henries.
Charge / Discharge of LR	$T = 5\ L/R$	T = time for 99.7% change
Inductor Charge State	$I = I_s e^{-(\frac{tL}{R})}$	I in Amps e = 2.7182 I_s = aiming current
Inductive Reactance	$X_L = 2\pi fL$	f in Hz
Q of Coil	$Q = \frac{X_L}{R}$	
Resonant Frequency	$f = \frac{1}{2\pi\sqrt{LC}}$	
Impedance	$Z = R$	series resonance
	$Z = \frac{L}{CR}$	Parallel resonance
	$Z = \sqrt{X^2 + R^2}$	X and R in series
	$Z = \frac{R \quad X}{\sqrt{R^2 + X^2}}$	X and R in parallel
	$Z = R \pm jX$	combined impedances

Conductance	$G = {}^{1}/_{R}$	G in mhos
Susceptance	$B = {}^{1}/_{X}$	B in mhos
Admittance	$Y = {}^{1}/_{Z}$	Y in mhos
Transistor	$Hfb = \frac{\Delta I_c}{\Delta I_e}$ $Hfe = \frac{Hfb}{1 - Hfb} = \frac{\Delta I_c}{\Delta I_b}$	
Gain	$A = \frac{Vout}{V\ in}$ $A' = \frac{\beta}{1 - \beta}$	 with feedback β = Fb fraction

LOCATION OF I.C's.

With the module component side up the I.C's are numbered starting beside the A1 contact set. This plan of the M8330 shows the system:



It also shows two of the pitfalls:

(a) Note that after E12 comes T1 which looks like an I.C. and could easily be included in the count. (In fact, transformers are given E numbers in some modules - G227 for example.)

(b) I.C's. falling out of line are counted as single I.C. rows. Here E32 could be taken as part of row E33-36 and again cause mis-identification.

IF IN DOUBT CONSULT THE PRINT.

INFORMATION DIRECTORY

In this list the abbreviations used indicate the book in which the information will be found.

LSDH - Logic System Design Handbook

WSM - Workmanship Standards Manual

LH - Logic Handbook

CLW - Computer Lab Workbook

ITDDL - Introduction to DEC Drawing & Logic

SCH - Small Computer Handbook

ITP - Introduction to Programming

ITEM	REF.	CHAPTER/PAGE
Cable		
characteristics	LSDH	Ch. 4
connections	WSM	Ch. 1 Ch. 6
types	LH	393
Component Identifier	WSM	Ch. 8
Decimal to Binary Conversion	CLW ITP	App.F Ch. 1
Flip Flops	LH	11
timing	LH	18
signal names	ITDDL	2.20
Flow Charting	SCH	3.3
Flow Chart Symbols	ITP	App.C
Gates		
timing considerations	LH	16
unused inputs	LH	16
truth tables	ITDDL	

Information Directory (cont'd)

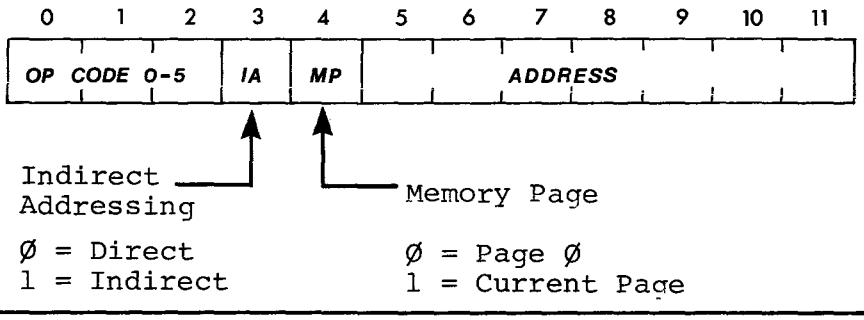
8 FAMILY NOTES

Mnemonic	Code	Operation	Time (μsec.)
		BASIC INSTRUCTIONS	
AND	0000	logical AND	2.6
TAD	1000	2's complement add	2.6
ISZ	2000	increment, and skip if zero	2.6
DCA	3000	deposit and clear AC	2.6
JMS	4000	jump to subroutine	2.6
JMP	5000	jump	1.2
IOT	6000	in/out transfer	-
OPR	7000	operate	1.2

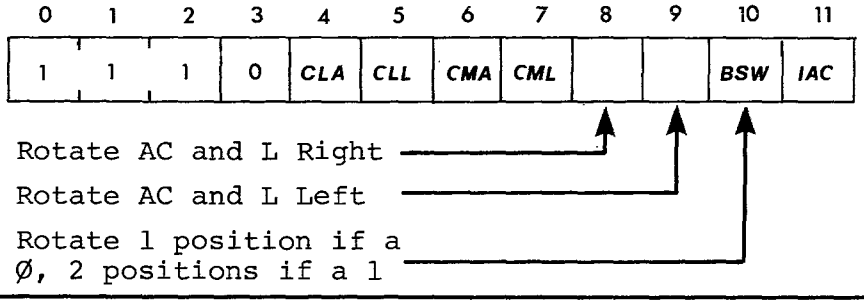
		GROUP 1 OPERATE MICROINSTRUCTIONS (1.2)	
			Sequence
NOP	7000	no operation	-
CLA	7200	clear AC	1
CLL	7100	clear link	1
CMA	7040	complement AC	2
CML	7020	complement link	2
RAR	7010	rotate AC and link right one	4
RAL	7004	rotate AC and link left one	4
RTR	7012	rotate AC and link right two	4
RTL	7006	rotate AC and link left two	4
IAC	7001	increment AC	3
BSW	7002	Swap Bytes in AC	4

		GROUP 2 OPERATE MICROINSTRUCTIONS (1.2)	
			Sequence
SMA	7500	skip on minus AC	1
SZA	7440	skip on zero AC	1
SPA	7510	skip on plus AC	1
SNA	7450	skip on non zero AC	1
SNL	7420	skip on non-zero link	1
SZL	7430	skip on zero-link	1
SKP	7410	skip unconditionally	1
OSR	7404	inclusive OR, switch register with AC	3
HLT	7402	halts the program	3
CLA	7600	clear AC	2

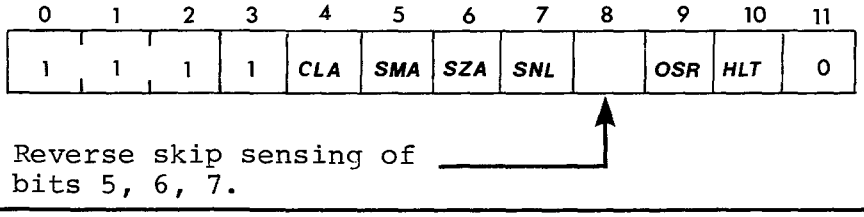
MEMORY REFERENCE INSTRUCTION BIT ASSIGNMENTS



GROUP 1 OPERATE INSTRUCTION BIT ASSIGNMENTS



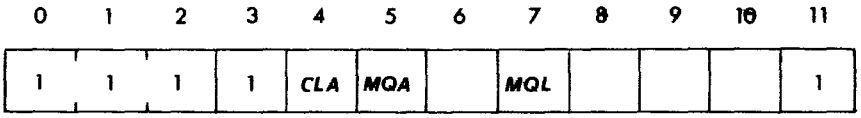
GROUP 2 OPERATE INSTRUCTION BIT ASSIGNMENTS



RIM LOADERS

(Low Speed)		(High Speed)	
7756/	6032	7756/	6014
7757/	6031	7757/	6011
7760/	5357	7760/	5357
7761/	6036	7761/	6016
7762/	7106	7762/	7106
7763/	7006	7763/	7006
7764/	7510	7764/	7510
7765/	5357	7765/	5374
7766/	7006	7766/	7006
7767/	6031	7767/	6011
7770/	5367	7770/	5367
7771/	6034	7771/	6016
7772/	7420	7772/	7420
7773/	3776	7773/	3776
7774/	3376	7774/	3376
7775/	5356	7775/	5357

MQ MICROINSTRUCTION BIT ASSIGNMENTS



MEMORY EXTENSION & TIME SHARING TYPE MC8-E

CDF	62n1	Change to Data Field n	1.2
CIF	62n2	Change to Instruction Field n	1.2
CDI	62n3	Change to Data Field and Instruction Field n	1.2
CINT	6204	Clear User Interrupt	1.2
RDF	6214	Read Data Field	1.2
RIF	6224	Read Instruction Field	1.2
RIB	6234	Read Interrupt Buffer	1.2
RMF	6244	Restore Memory Field	1.2
SINT	6254	Skip on User Interrupt	1.2
CUF	6264	Clear User Flag	1.2
SUF	6274	Set User Flag	1.2

COMBINED OPERATE MICROINSTRUCTIONS

			Sequence
CIA	7041	complement and increment AC	2, 3
LAS	7604	load AC with switch register	2, 3
STL	7120	set link (to 1)	1, 2
GLK	7204	get link (put link in AC bit 11)	1, 4
CLA CLL	7300	clear AC and link	1
CLA IAC	7201	set AC = 1	1, 3
CLA CMA	7240	set AC = - 1	1, 2
CLL RAR	7110	shift positive number one right	1, 4
CLL RAL	7104	shift positive number one left	1, 4
CLL RTL	7106	clear link, rotate 2 left	1, 4
CLL RTR	7112	clear link, rotate 2 right	1, 4
SZA CLA	7640	skip if AC = 0, then clear AC	1, 2
SZA SNL	7460	skip if AC = 0 or link is 1, or both	1
SNA CLA	7650	skip if AC $\neq$ 0, then clear AC	1, 2
SMA CLA	7700	skip if AC $<$ 0, then clear AC	1, 2
SMA SZA	7540	skip if AC $\leq$ 0	1,
SMA SNL	7520	skip if AC $<$ 0 or link is 1, or both	1
SPA SNA	7550	skip if AC $>$ 0	1
SPA SZL	7530	skip if AC $\geq$ 0, and if the link is 0	1
SPA CLA	7710	skip if AC $\geq$ 0, then clear AC	1, 2
SNA SZL	7470	skip if AC $\neq$ 0 and link = 0	1

MQ MICROINSTRUCTION

			Time (μsec.)
NOP	7401	No operation	1.2
CLA	7601	Clear AC	1.2
MQL	7421	Load MQ from AC then Clear AC	1.2
MQA	7501	Inclusive OR the MQ with the AC	1.2
CAM	7621	Clear AC and MQ	1.2
SWP	7521	Swap AC and MQ	1.2
ACL	7701	Load MQ into AC	1.2
CLA,SWP	7721	Load AC from MQ then Clear MQ	1.2

INTERNAL IOT MICROINSTRUCTIONS

PROGRAM INTERRUPT AND FLAG

			Time (μsec.)
SKON	6000	Skip if Interrupt ON, and turn OFF	1.2
ION	6001	Turn Interrupt ON	1.2
IOF	6002	Turn Interrupt OFF	1.2
SRQ	6003	Skip on Interrupt Request	1.2
GTF	6004	Get Interrupt Flags	1.2
RTF	6005	Restore Interrupt Flags	1.2
SGT	6006	Skip on Greater Than Flag	1.2
CAF	6007	Clear All Flags	1.2

LOADING CONSTANTS INTO THE AC (1.2 μSEC.)

OCTAL Constant	Decimal Constant	OCTAL Instruction	Instructions Combined
5777	-1025	7352	CLA CLL CMA RTR
6000	-1024	7333	CLA CLL CML IAC RTL
7775	-3	7346	CLA CLL CMA RTL
7776	-2	7344	CLA CLL CMA RAL
7777	-1	7340	CLA CLL CMA
4000	-0	7330	CLA CLL CML RAR
0000	0	7300	CLA CLL
0001	1	7301	CLA CLL IAC
0002	2	7305	CLA CLL IAC RAL
0002	2	7326	CLA CLL CML RTL
0003	3	7325	CLA CLL CML IAC RAL
0004	4	7307	CLA CLL IAC RTL
0006	6	7327	CLA CLL CML IAC RTL
0100	64	7302	CLA IAC BSW
2000	1024	7332	CLA CLL CML RTR
3777	2047	7350	CLA CLL CMA RAR

EXTENDED ARITHMETIC ELEMENT KE8-E (optional)			
Mode Instructions			
SWAB	7431		switch Mode from A to B
SWBA	7447		switch Mode from B to A
Shift Instructions			
SCA	7441		logical OR step counter with AC
SCA CLA	7641		step counter to AC
SCL	7403	(Mode A)	step counter load (from memory)
NMI	7411		normalize
SHL	7413		shift left
ASR	7415		arithmetic shift right
LSR	7417		logical shift right
ASC	7403	(Mode B)	AC to step counter
Arithmetic Instructions			
MVY	7405		multiply
DVI	7407		divide
SAM	7457	(Mode B)	subtract AC from MQ
Double Precision Instructions (Mode B)			
DLD	7763		double precision load
DST	7445		double precision store
DAD	7443		double precision add
DPIC	7573		double precision increment
DCM	7575		double precision complement
DPSZ	7451		double precision skip if zero

TELETYPE KEYBOARD READER		
Mnemonic Symbol	Octal Code	Operation
KCF	6030	Clear Keyboard Flag
KSF	6031	Skip on Keyboard Flag
KCC	6032	Clear Keyboard Flag, and AC, Advance Reader
KRS	6034	Read Keyboard Buffer Static
KIE	6035	Set/Clear Interrupt Enable
KRB	6036	Read Keyboard Buffer, Clear Flag

TELETYPE TELEPRINTER PUNCH		
Mnemonic Symbol	Octal Code	Operation
TFL	6040	Set Teleprinter Flag
TSF	6041	Skip on Teleprinter Flag
TCF	6042	Clear Teleprinter Flag
TPC	6044	Load Teleprinter and Print
TSK	6045	Skip on Printer or Keyboard Interrupt
TLS	6046	Clear Flag Load Teleprinter and Print

PC8-E READER PUNCH		
Mnemonic Symbol	Octal Code	Operation
RPE	6010	Set Reader/Punch Interrupt Enable
RSF	6011	Skip on Reader Flag
RRB	6012	Read Reader Buffer
RFC	6014	Reader Fetch Character
RFC RRB	6016	Read Buffer and Fetch New Character
PCE	6020	Clear Reader/Punch Interrupt Enable
PSF	6021	Skip on Punch Flag
PCF	6022	Clear Punch Flag
PPC	6024	Load Punch Buffer and Punch Character
PLS	6026	Clear Flag Load Punch Buffer and Punch

LE-8 LINE PRINTER		
Mnemonic Symbol	Octal Code	Operation
PSKF	6661	Skip on Character Flag
PCLF	6662	Clear the Character Flag
PSKE	6663	Skip on Error
PSTB	6664	Load Printer Buffer, Print on Full Buffer or Control Character
PSIE	6665	Set Program Interrupt Flag
PCLF PSTB	6666	Clear Line Printer Flag, Load Character, and Print
PCIE	6667	Clear Program Interrupt Flag

TC08-P DECTAPE CONTROL

Mnemonic Symbol	Octal Code	Operation	Time (μs)
DTRA	6761	Read Status Register A	2.6
DTCA	6762	Clear Status Register A	2.6
DTXA	6764	Load Status Register A	2.6
DTLA	6766	Clear and Load Status Register A	3.6
DTSF	6771	Skip on Flag	2.6
DTRB	6772	Read Status Register B	2.6
DTXB	6774	Load Status Register B	2.6

TD8-E DECTAPE CONTROL

Mnemonic Symbol	Octal Code	Operation
SDSS	67X1	Skip if single line flag is set.
SDST	67X2	Skip if time error flag is set.
SDSQ	67X3	Skip if Quad Line flag is set.
SDLC	67X4	Load Command Register from the AC, clear Time Error, and start UTS delay if UNIT, DIRECTION, or STOP/GO flip-flops are changed.
SDLD	67X5	Load Data Register from the AC, do not clear the AC, and clear Single Line and Quad Line flags.
SDRC	67X6	Load contents of Command Register, Mark Track Register, and Status bits into the AC. Clear Single Line and Quad Line flags.
SDRD	67X7	Load contents of Data Register into the AC, and clear Single Line and Quad Line flags.

TA8-E DEC CASSETTE IOT INSTRUCTIONS

Mnemonic Symbol	Octal Code	Operation
KCLR	67X0	Clear all. Clears Status A and B Registers.
KSDR	67X1	Skip on Data flag, for either a read or a write.
KSEN	67X2	Skip on, EOT/BOT or EOF or Drive Empty or Timing Error, Block Error or Write Lock and "Write" True.
KSBF	67X3	Skip on Ready Flag.
KLSA	67X4	Load Status A from AC 4-11, clear AC, load complement Status A back into AC.
KSAF	67X5	Skip on any flag or error condition.
KGOA	67X6	Assert the contents of Status A, transfer data into the AC for a read, out of the AC into the Read/ Write buffer for a write.
KRSB	67X7	Read Status B into AC 4-11.

RK08-P CONTROL & RK01 DISK DRIVE & CONTROL

Mnemonic Symbol	Octal Code	Operation	Time (μs)
DLDA	6731	Load Disk Address (Maintenance Only)	2.6
DLDC	6732	Load Command Register	2.6
DLDR	6733	Load Disk Address and Read	2.6
DRDA	6734	Read Disk Address	2.6
DLDW	6735	Load Disk Address and Write	2.6
DRDC	6736	Read Disk Command Register	3.6
DCHP	6737	Load Disk Address and Check Parity	4.6
DRDS	6741	Read Disk Status Register	2.6
DCLS	6742	Clear Status Register	2.6
DMNT	6743	Load Maintenance Register	3.6
DSKD	6745	Skip on Disk Done	3.6
DSKE	6747	Skip on Disk Error	4.6
DCLA	6751	Clear All	2.6
DRWC	6752	Read Word Count Register	3.6
DLWC	6753	Load Word Count Register	3.6
DLCA	6755	Load Current Address Register	3.6
DRCA	6757	Read Current Address Register	4.6

VT8-E INSTRUCTIONS

Mnemonic Symbol	Octal Code	Operation
DPLA	6050	Load starting address of data buffer
DPGO	6051	Load starting extended address of data buffer and go - start display after next vertical retrace in one of the two modes. Enable or disable interrupts from keyboard and printer.
DPSM	6052	Stop the display. Inhibit video and further device-initiated breaks.
DPMB	6053	Maintenance instruction - perform a single one-cycle data break.
DPMD	6054	Maintenance instruction - read extended break, address or status registers.
DPCL	6056	Skip on real-time clock flag; clear the flag if it is set.
DPBELL	6057	Generate a half-second audible tone.
Keyboard Instructions		
DKCF	6030	Clear keyboard flag.
DKSK	6031	Skip on keyboard flag.
DKCC	6032	Clear keyboard flag, clear AC.
DKOB	6034	OR contents of keyboard buffer with AC, and deposit in AC.
SKIN	6035	Enable interrupt if AC 11 = 1. Disable interrupt if AC 11 = 0.
DKRB	6036	Read keyboard buffer - transfer contents of keyboard buffer to AC - clear keyboard flag.
Printer Instructions		
PNSF	6040	Set printer flag.
PNSK	6041	Skip on printer flag.
PNCF	6042	Clear printer flag.
	6043	Not used.
PNLP	6044	Load printer buffer from AC5-11 - print.
PNSI	6045	Skip if about to interrupt.
PNPC	6046	Load printer buff - print - clear printer flag.

RF08 DISK FILE

Mnemonic Symbol	Octal Code	Operation
DCIM	6611	Clear Disk Interrupt Enable and Core Memory Address Extension Register
DIML	6615	Load Interrupt Enable and Memory Address Extension Register.
DIMA	6616	Load Interrupt and Extended Memory Address
DFSE	6621	Skip on Disc Error
DISK	6623	Skip Error or Completion Flag
DCXA	6641	Clear High Order Address Register
DXAL	6643	Clear and Load High Order Address Register
DXAC	6645	Clear AC & Load DAR into AC
DMMT	6646	Initiate Maintenance Register.

DF32-D DISK FILE AND CONTROL

Mnemonic Symbol	Octal Code	Operation	Time (μs)
DCMA	6601	Clear Disk Address Register	2.6
DMAR	6603	Load Disk Address Register and Read	3.6
DMAW	6605	Load Disk Address Register and Write	3.6
DCEA	6611	Clear Disk Extended Address	2.6
DSAC	6612	Skip on Address Confirmed Flag	2.6
DEAL	6615	Load Disk Extended Address	3.6
DEAC	6616	Read Disk Extended Address	3.6
DFSE	6621	Skip on Zero Error Flag	2.6
DFSC	6622	Skip on Data Completion Flag	2.6
DMAC	6626	Read Disk Memory Address Register	3.6

VC8-E CRT DISPLAY CONTROL

Mnemonic Symbol	Octal Code	Operation
DILC	6050	Clears Enables, Flags and Delays
DICD	6051	Clears Done Flag
DISD	6052	Skip on Done Flag
DILX	6053	Load X Register
DILY	6054	Load Y Register
DIXY	6055	Clear Done Flag; Intensify- Set Done Flag
DILE	6056	Transfers AC to Enable Register
DIRE	6057	Transfers Display Enable/Status Register to AC

CR8-E CARD READER & CONTROL or CM8-E OPTICAL MARK CARD READER & CONTROL		
Mnemonic Symbol	Octal Code	Operation
RCSF	6631	Skip on Data Ready
RCRA	6632	Read Alphanumeric
RCRB	6634	Read Binary
RCNO	6635	Read Conditions Out to Card Reader
RCRC	6636	Read Compressed
RCNI	6637	Read Condition in From Card Reader
RCSD	6671	Skip on Card Done Flag
RCSE	6672	Select Card Reader and Skip if Ready
RCRD	6674	Clear Card Done Flag
RCSI	6675	Skip if Interrupt Being Generated
RCTF	6677	Clear Transition Flags

XY8-E INCREMENTAL PLOTTER CONTROL		
Mnemonic Symbol	Octal Code	Operation
PLCE	6500	Clear Interrupt Enable
PLSF	6501	Skip on Plotter Flag
PLCF	6502	Clear Plotter Flag
PLPU	6503	Pen Up
PLLR	6504	Load Direction Register, Set Flag
PLPD	6505	Pen Down
PLCF PLLR	6506	Clear Flag, Load Direction Register, Set Flag
PLSE	6507	Set Interrupt Enable

TM8-E/F MAGTAPE CONTROL

Mnemonic Symbol	Octal Code	Operation
LWCR	6701	Load Word Count Register
CWCR	6702	Clear Word Count Register
LCAR	6703	Load Current Address Register
CCAR	6704	Clear Current Address Register
LCMR	6705	Load Command Register
LFGR	6706	Load Function Register
LDBR	6707	Load Data Buffer Register
RWCR	6711	Read Word Count Register
CLT	6712	Clear Transport
RCAR	6713	Read Current Address Register
RMSR	6714	Read Main Status Register
RCMR	6715	Read Command Register
RFSR	6716	Read Function Register & Status
RDBR	6717	Read Data Buffer
SKEF	6721	Skip if Error Flag
SKCB	6722	Skip if Not Busing
SKJD	6723	Skip if Job Done
SKTR	6724	Skip if Tape Ready
CLF	6725	Clear Controller and Master

DATA TRANSFER SIGNALS

Control Signals CO, Cl, C2 control the data path and loading within the processor. They come into play during I/O transfers and are controlled from outside by the peripheral interface. When it is time for a device to make either an input or output transfer, the device will ground the appropriate combination of C control lines.

	CO L	Cl L	C2 L
Output, AC Unchanged	Hi	Hi	Hi
Output, AC Cleared	Lo	Hi	Hi
Input, AC Or'd with Input Data	Hi	Lo	Hi
Jam Input	Lo	Lo	Hi
Input, Data Added to PC	Lo	Hi	Lo
Input Data to PC	Lo	Lo	Lo

ASCII CODE

Character	Code	Character	Code
A	301	!	241
B	302	"	242
C	303	#	243
D	304	$	244
E	305	%	245
F	306	&	246
G	307	'	247
H	310	(	250
I	311	)	251
J	312	*	252
K	313	+	253
L	314	,	254
M	315	-	255
N	316	.	256
O	317	/	257
P	320	:	272
Q	321	;	273
R	322	<	274
S	323	=	275
T	324	>	276
U	325	?	277
V	326	@	300
W	327	[	333
X	330	/	334
Y	331	]	335
Z	332	↑	336
0	260	←	337
1	261	EOT	204
2	262	W RU	205
3	263	RU	206
4	264	BELL	207
5	265	Line Feed	212
6	266	Return	215
7	267	Space	240
8	270	ALT MODE	375
9	271	Rub Out	377
		Escape	233

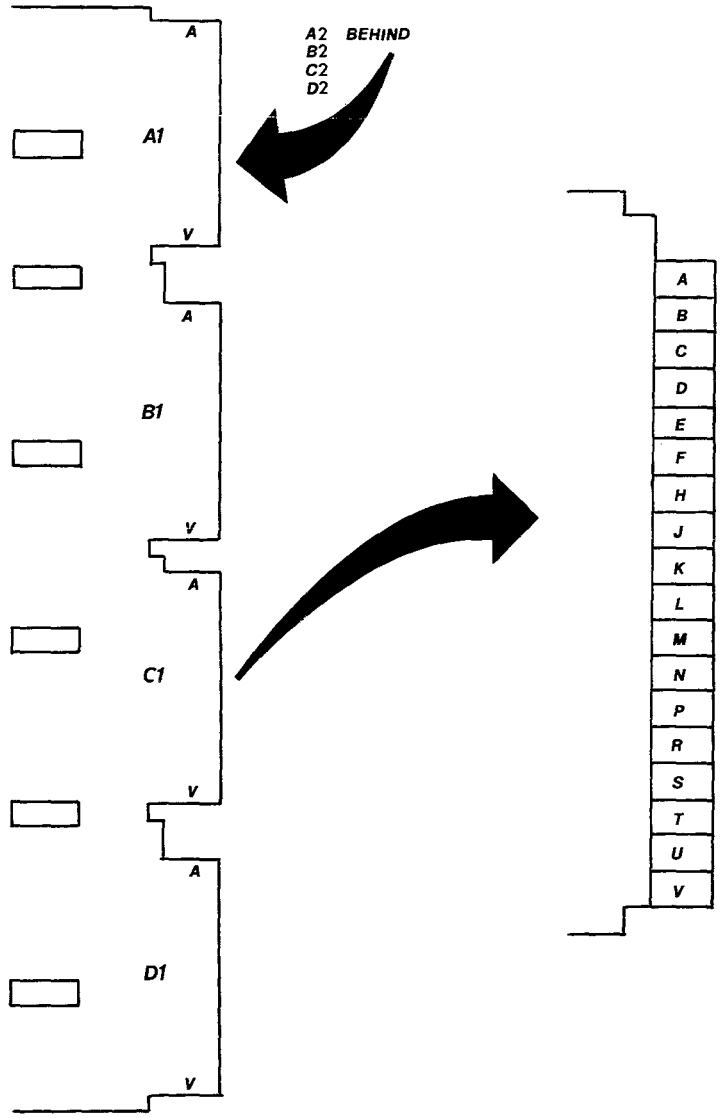
PIN	D1	D2	C1	C2	B1	B2	A1	A2
A		+15V		+5V		+5V		+5V
B		-15V		-15V		-15V		-15V
C	GND	GND	GND	GND	GND	GND	SP*GND	GND
D	MA8 L	IRØ L	IO PAUSE L	TP1 H	MA4 L	INT STB H	MAØ L	EMAØ L
E	MA9 L	IR1 L	CØ L	TP2 H	MA5 L	BRK PROG L	MA1 L	EMA1 L
F	GND	GND	GND	GND	GND	GND	GND	GND
H	MA1Ø L	IR2 L	C1 L	TP3 H	MA6 L	MA,MS LD L	MA2 L	EMA2 L
J	MA11 L	F L	C2 L	TP4 H	MA7 L	OVERFLOW L	MA3 L	MEM START L
K	MD8 L	D L	BUS STB L	TS1 L	MD4 L	BRK DA CT L	MDØ L	MD DIR L
L	MD9 L	E L	INT I/O L	TS2 L	MD5 L	BRK CYC L	MD1 L	SOURCE H
M	MD1Ø L	USR MD H	N L XFR L	TS3 L	MD6 L	LA EN. L	MD2 L	STROBE H
N	GND	GND	GND	GND	GND	GND	GND	GND
P	MD11 L	F SET L	INT RQST L	TS4 L	MD7 L	INT PROG H	MD3 L	INHIBIT H
R	DATA 8 L	PULSE LA H	INIT. H	LNK DATA L	DATA 4 L	RES 1 H	DATA Ø L	RETURN H
S	DATA 9 L	STOP L	SKIP L	LNK LOAD L	DATA 5 L	RES 2 H	DATA 1 L	WRITE H
T	GND	GND	GND	GND	GND	GND	GND	GND
U	DATA 1Ø L	KEY CTRL L	CPMA DIS L	IND 1 L	DATA 6 L	RUN L	DATA 2 L	ROM ADDR L
V	DATA 11 L	SW L	MS,IR DIS L	IND 2 L	DATA 7 L	POWER OK H	DATA 3 L	LINK L

Blank pins are not interconnected on the bus but may be test points on individual modules.

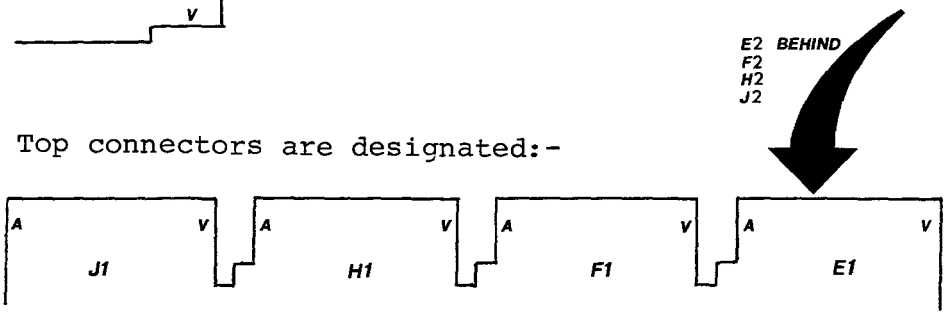
* This pin is connected to GND on the bus but serves as a logic signal within modules to facilitate testing.

OMNIBUS PIN ASSIGNMENTS

MODULE CONTACT DESIGNATORS



Top connectors are designated:-



Information Directory

In this list the abbreviations used indicate the book in which the information will be found.

ITP	-	Introduction to Programming
SCH	-	Small Computer Handbook
LH	-	Logic Handbook
Vol I Vol II Vol III	- - -	PDP8e/f/m Maintenance Manual

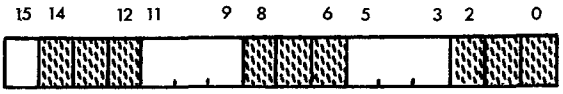
P continued		
Part Numbers (DEC)	Appendix Spare Parts List	SCH
	Appendix of Each Chapter	Vol II & III
Program (Echo Test, Print all characters, clean core, etc.)	4-1	Vol I
R		
Ringing	10-30	SCH
Receivers	10-36	SCH
Rim	App.E	ITP
S		
Subroutines	3-16	ITP
Software (general)	2-20	SCH
T		
Terminations	10-30	SCH
Tape (Paper) Formats	4-16	ITP
	A-21	SCH
Thresholds (TTL)	9	LH

NOTES

5

11 FAMILY NOTES

WORD FORMAT



Binary-Octal Representation

GENERAL REGISTER ADDRESSING

Mode	R

Mode	Name	Symbolic	Description
0	register	R	(R) is operand [ex.R2=%2]
1	register deferred	(R)	(R) is address
2	auto increment	(R)+	(R) is adrs; (R)+(1 or 2)
3	auto-incr deferred	@(R)+	(R) is adrs of adrs; (R)+2
4	auto-decrement	-(R)	(R) -(1 or 2): (R) is adrs
5	auto-decr deferred	@-(R)	(R) -2; (R) is adrs of adrs
6	index	X(R)	(R) +X is adrs
7	index deferred	@X(R)	(R) +X is adrs of adrs

PROGRAM COUNTER ADDRESSING Reg = 7

Mode	7

2	immediate	#n	operand n follows instr
3	absolute	@#A	address A follows instr
6	relative	A	instr adrs + 4 + X is adrs
7	relative deferred	@A	instr adrs + 4 + X is adrs of adrs

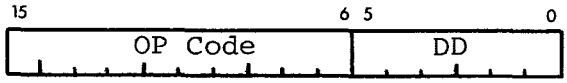
LEGEND

Op Codes	Operations
■ = 0 for word/1 for byte	()= contents of
SS = source field (6 bits)	s = contents of source
DD = destination field (6 bits)	d = contents of destin.
R = gen reg. (3 bits), 0 to 7	r = contents of register
XXX = offset (8 bits) +127 to -128	← = becomes
N = number (3 bits)	X = relative address
NN = number (6 bits)	% = register definition

continued overleaf

LEGEND (continued)	
Boolean	Condition Codes
∧ = AND V = inclusive OR ⊻ = exclusive OR ~ = NOT	* = conditionally set/cleared - = not affected 0 = cleared 1 = set

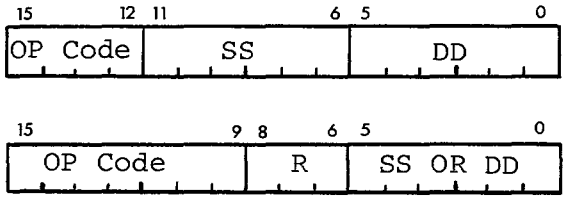
SINGLE OPERAND OPR dst



Mnemonic	Op Code	Instruction	dst Result	N	Z	V	C
General							
CLR(B)	■050DD	clear	0	0	1	0	0
COM(B)	■051DD	complement (1's)	~ d	*	*	0	1
INC(B)	■052DD	increment	d + 1	*	*	*	-
DEC(B)	■053DD	decrement	d - 1	*	*	*	-
NEG(B)	■054DD	negate (2's com)	-d	*	*	*	*
TST(B)	■057DD	test	d	*	*	0	0
Rotate & Shift							
ROR(B)	■060DD	rotate right	→C, d	*	*	*	*
ROL(B)	■061DD	rotate left	C, d←	*	*	*	*
ASR(B)	■062DD	arith shift right	d/2	*	*	*	*
ASL(B)	■063DD	arith shift left	2d	*	*	*	*
SWAB	0003DD	swap bytes		*	*	*	0
Multiple Precision							
ADC(B)	■055DD	add carry	d + C	*	*	*	*
SBC(B)	■056DD	subtract carry	d - C	*	*	*	*
▲SXT	0067DD	sign extend	0 or -1	-	*	*	-

▲ Applies to the 11/40 & 11/45 computers
● Applies to the 11/45 computer

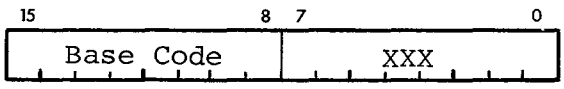
DOUBLE OPERAND OPR src, dst OPR src, R or OPR R, dst



Mnemonic	Op Code	Instruction	Operation	N	Z	V	C
General							
MOV(B)	■1SSDD	move	d←s	*	*	0	-
CMP(B)	■2SSDD	compare	s-d	*	*	*	*
ADD	06SSDD	add	d←s + d	*	*	*	*
SUB	16SSDD	subtract	d←d - s	*	*	*	*
Logical							
BIT(B)	■3SSDD	bit test (AND)	s∧d	*	*	0	-
BIC(B)	■4SSDD	bit clear	d← (~s)∧d	*	*	0	-
BIS(B)	■5SSDD	bit set (OR)	d←s v d	*	*	0	-
Register▲							
MUL	070RSS	multiply	r←r x s	*	*	0	*
DIV	071RSS	divide	r←r/s	*	*	*	*
ASH	072RSS	shift arithmetically		*	*	*	*
ASHC	073RSS	arith shift combined		*	*	*	*
XOR	074RDD	exclusive OR	d←r ⊻ d	*	*	0	-

BRANCH B - - location

If condition is satisfied Branch to location, New PC← Updated PC + (2 x offset)



Op code = Base Code + XXX

adrs of br instr + 2

Mnemonic	Base Code	Instruction	Branch Condition
Branches			
BR	000400	branch (unconditional)	(always)
BNE	001000	br if not equal (to 0)	≠0 Z = 0
BEQ	001400	br if equal (to 0)	=0 Z = 1
BPL	100000	branch if plus	+ N = 0
BMI	100400	branch if minus	- N = 1
BVC	102000	br if overflow is clear	V = 0
BVS	102400	br if overflow is set	V = 1
BCC	103000	br if carry is clear	C = 0
BCS	103400	br if carry is set	C = 1

BRANCH (cont'd)

Mnemonic	Base Code	Instruction	Branch Condition
Signed Conditional Branches			
BGE	002000	br if greater or eq (to 0)	≥0 N⊻V=0
BLT	002400	br if less than (0)	<0 N⊻V=1
BGT	003000	br if greater than (0)	>0 Zv(N⊻V)=0
BLE	003400	br if less or equal (to 0)	≤0 Zv(N⊻V)=1
Unsigned Conditional Branches			
BHI	101000	branch if higher	> CvZ=0
BLOS	101400	branch if lower or same	≤ CvZ=1
BHIS	103000	branch if higher or same	≥ C = 0
BLO	103400	branch if lower	< C = 1

JUMP & SUBROUTINE

Mnemonic	Op Code	Instruction	Notes
JMP	0001DD	jump	PC←dst
JSR	004RDD	jump to subroutine	use same R
RTS	00020R	return from subroutine	use same R
MARK▲	0064NN	mark	aid in subr rtn.
SOB▲	077RNN	subtract 1 & br (if ≠ 0)	(R)-1, then if (R) ≠ 0: PC← Updated PC - (2 x NN)

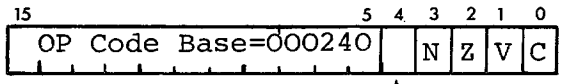
TRAP & INTERRUPT

Mnemonic	Op Code	Instruction	Notes
EMT	104000-104377	emulator trap (not for general use)	PC at 30, PS at 32
TRAP	104400-104777	trap	PC at 34, PS at 36
BPT	000003	breakpoint trap	PC at 14, PS at 16
IOT	000004	input/output trap	PC at 20, PS at 22
RTI	000002	return from interrupt	
RTT▲	000006	return from interrupt	inhibit T bit trap

MISCELLANEOUS

Mnemonic	Op Code	Instruction
HALT	000000	halt
WAIT	000001	wait for interrupt
RESET	000005	reset external bus
NOP	000240	(no operation)
●SPL	00023N	set priority level (to N)
▲MFPI	0065SS	move from previous instr space
▲MTPI	0066DD	move to previous instr space
●MFPD	1065SS	move from previous data space
●MTPD	1066DD	move to previous data space

CONDITION CODE OPERATORS



0 = Clear selected cond code bits
1 = Set selected cond code bits

Mnemonic	Op Code	Instruction	N	Z	V	C
CLC	000241	clear C	-	-	-	0
CLV	000242	clear V	-	-	0	-
CLZ	000244	clear Z	-	0	-	-
CLN	000250	clear N	0	-	-	-
CCC	000257	clear all cc bits	0	0	0	0
SEC	000261	set C	-	-	-	1
SEV	000262	set V	-	-	1	-
SEZ	000264	set Z	-	1	-	-
SEN	000270	set N	1	-	-	-
SCC	000277	set all cc bits	1	1	1	1

PDP11-40 FLOATING POINT UNIT

Mnemonic	Op Code	Instruction	N	Z	V	C
FADD	07500R	floating add	*	*	0	0
FSUB	07501R	floating subtract	*	*	0	0
FMUL	07502R	floating multiply	*	*	0	0
FDIV	07503R	floating divide	*	*	0	0

FLOATING POINT; PDP11-45

Mnemonic	Op Code	Instruction	Operation
CFCC	170000	copy fl cond codes	
SETF	170001	set floating mode	FD←0
SETI	170002	set integer mode	FL←0
SETD	170011	set fl dbl mode	FD←1
SETL	170012	set long integer mode	FL←1
LDFPS	1701 src	load FPP prog status	
STFPS	1702 dst	store FPP prog status	
STST	1703 dst	store (exc codes & adr)	
CLRF,CLRD	1704 fdst	clear floating/double	fdst←0
TSTF, TSTD	1705 fdst	test fl/dbl	
ABSF,ABSD	1706 fdst	make absolute fl/dbl	fdst←|fdst|
NEGF,NEGD	1707 fdst	negate fl/dbl	fdst←-fdst
MULF,MULD	171(AC)fsrc	multiply fl/dbl	AC←AC x fsrc
MODF,MODD	171(AC+4)fsrc	multiply & integerize	
ADDF,ADDD	172(AC)fsrc	add fl/dbl	AC←AC + fsrc
LDF,LDD	172(AC+4)fsrc	load fl/dbl	AC←fsrc
SUBF,SUBD	173(AC)fsrc	subtract fl/dbl	AC←AC−fsrc
CMPF,CMPD	173(AC+4)fsrc	compare fl/dbl (to AC)	
STF,STD	174(AC)fdst	store fl/dbl	fdst←AC
DIVF,DIVD	174(AC+4)fsrc	divide fl/dbl	AC←AC/fsrc
STEXP	175(AC)dst	store exponent	
STCFI,STCFL STCDI,STCDL	175(AC+4)dst	store & convert fl or dbl to int or long int	
STCFD,STCDF	176(AC)fdst	store & convert (dbl-fl)	
LDEXP	176(AC+4)src	load exponent	
LDCIF,LDCID LDCLF,LDCLD	177 (AC)src	load & convert int or long int to fl or dbl	
LDCDF,LDCFD	177(AC+4)fsrc	load & convert (dbl-fl)	

HARDWARE MULTIPLY-DIVIDE (KE11-A)

OP/REG	ADDRESS	READ	WRITE
DIV Divide	777300	Read Zero's	Load Divisor, Start divide.
AC	777302	Read AC	Load AC
MQ	777304	Read MQ	Load MQ, sign extends into AC
MUL Multiply	777306	Read Zero's	Load multiplicand. Start multiply
SC SR	777310 777311	Read SC and SR	Load SC and load SR bits 0, 6, 7
NOR Normalize	777312	Read SC	Start Normalize
LSH Logical Shift	777314	Read Zero's	Load SC, Start logical shift
ASH Arithmet. Shift	777316	Read Zero's	Load SC, start arithmetic shift

NUMERICAL OP CODE LIST

Op Code	Mnemonic
00 00 00	HALT
00 00 01	WAIT
00 00 02	RTI
00 00 03	BPT
00 00 04	IOT
00 00 05	RESET
00 00 06	RTT
00 00 07	(unused)
00 01 DD	JMP
00 02 0R	RTS
00 02 10	(unused)
00 02 27	
00 02 3N	SPL
00 02 40	NOP
00 02 41	cond codes
00 02 77	
00 03 DD	SWAB
00 04 XXX	BR
00 10 XXX	BNE
00 14 XXX	BEQ
00 20 XXX	BGE
00 24 XXX	BLT
00 30 XXX	BGT
00 34 XXX	BLE
00 4R DD	JSR
00 50 DD	CLR
00 51 DD	COM
00 52 DD	INC
00 53 DD	DEC
00 54 DD	NEG
00 55 DD	ADC
00 56 DD	SBC
00 57 DD	TST

Op Code	Mnemonic
00 60 DD	ROR
00 61 DD	ROL
00 62 DD	ASR
00 63 DD	ASL
00 64 NN	MARK
00 65 SS	MFPI
00 66 DD	MTPI
00 67 DD	SXT
00 70 00	(unused)
00 77 77	
01 SS DD	MOV
02 SS DD	CMP
03 SS DD	BIT
04 SS DD	BIC
05 SS DD	BIS
06 SS DD	ADD
07 0R SS	MUL
07 1R SS	DIV
07 2R SS	ASH
07 3R SS	ASHC
07 4R DD	XOR
07 50 0R	FADD
07 50 1R	FSUB
07 50 2R	FMUL
07 50 3R	FDIV
07 50 40	(unused)
07 67 77	
07 7R NN	SOB
10 00 XXX	BPL
10 04 XXX	BMI
10 10 XXX	BHI
10 14 XXX	BLOS
10 20 XXX	BVC
10 24 XXX	BVS
10 30 XXX	BCC,BHIS
10 34 XXX	BCS,BLO

Op Code	Mnemonic
10 40 00	EMT
10 43 77	
10 44 00	TRAP
10 47 77	
10 50 DD	CLRB
10 51 DD	COMB
10 52 DD	INCB
10 53 DD	DECB
10 54 DD	NEGB
10 55 DD	ADCB
10 56 DD	SBCB
10 57 DD	TSTB
10 60 DD	RORB
10 61 DD	ROLB
10 62 DD	ASRB
10 63 DD	ASLB
10 64 00	(unused)
10 64 77	
10 65 SS	MFPD
10 66 DD	MTPD
10 67 00	(unused)
10 77 77	
11 SS DD	MOVB
12 SS DD	CMPB
13 SS DD	BITB
14 SS DD	BICB
15 SS DD	BISB
16 SS DD	SUB
17 00 00	floating point
17 77 77	

PROCESSOR REGISTER ADDRESSES

Processor Status Word PS - 777 776

Current Mode ▲
Previous Mode▲
Gen Reg Set●
Trace Trap
Negative
Zero
Overflow
Carry

00 = Kernel▲ 01 = Supervisor● 11 = User▲

▲Stack Limit Register - 777 774

●Program Interrupt Request - 777 772

General Registers	R0 - 777 700	R4 - 777 704
(console use only)	R1 - 777 701	R5 - 777 705
	R2 - 777 702	R6 - 777 706
(not for 11/45)	R3 - 777 703	R7 - 777 707

Console Switches & Display Register - 777 570

INTERRUPT VECTORS

000	(reserved)
004	Time Out & other errors
010	illegal & reserved instr
014	BPT
020	IOT
024	Power Fail
030	EMT
034	TRAP
240	PIRQ
244	Floating Point trap
250	Segmentation trap

DEVICE REGISTER ADDRESSES

Device		Control & Status	Data Buffer	Vector	Priority Level
CR11	Card Reader	777 160		230	BR6
	data buffer 1		777 162		
	data buffer 2		777 164		
KW11-L	Line Clock	777 546	-	100	BR6
KW-11-P	Real Time Clock		772 542	104	BR6
	control & status	772 540			
	counter	772 544			
LA30	DECwriter				
	keyboard	777 560	777 562	60	BR4
	printer	777 564	777 566	64	BR4
LP11	Line Printer	777 514	777 516	200	BR4
LT33	Teletype				
	keyboard	777 560	777 562	60	BR4
	printer	777 564	777 566	64	BR4
PC11	Paper Tape				
	reader	777 550	777 552	70	BR4
	punch	777 554	777 556	74	BR4
RC11/	Disk (64K words)		777 456	210	BR5
RS64	look ahead	777 440			
	disk address	777 442			
	error status	777 444			
	command & status	777 446			
	word count	777 450			
	current address	777 452			
	maintenance	777 454			
RF11/	Disk (256K words)		777 472	204	BR5
RS11	control status	777 460			
	word count	777 462			
	current mem adrs	777 464			
	disk address	777 466			
	adrs ext error	777 470			
	maintenance	777 474			
	look ahead	777 476			
RK11/	Disk Cartridge		777 416	220	BR5
RK05	drive status	777 400			
	error	777 402			
	control status	777 404			
	word count	777 406			
	current address	777 410			
	disk address	777 412			
	maintenance	777 414			

Device Register Addresses (cont'd)

Device	Control & Status	Data Buffer	Vector	Priority Level
TC11/ DECtape		777 350	214	BR6
TU56 control	777 340			
command	777 342			
word count	777 344			
current address	777 346			
TM11/ Magtape		772 530	224	BR5
TU10 status	772 520			
command	772 522			
byte counter	772 524			
current address	772 526			
read lines	772 532			

ABSOLUTE LOADER

Starting Address:- 500

Memory Size:

4K	017
8K	037
12K	057
16K	077
20K	117
24K	137
28K	157

(or larger)

BOOTSTRAP LOADER

Address	Contents	Address	Contents
-744	016 701	-764	000 002
-746	000 026	-766	- 400
-750	012 702	-770	005 267
-752	000 352	-772	177 756
-754	005 211	-774	000 765
-756	105 711	-776	177 560 (KB)
-760	100 376	or	177 550 (PR)
-762	116 162		

773 000	Paper Tape Bootstrap
773 100	Disk/DECtape Bootstrap
773 200	Card Reader Bootstrap

MR11-DB BOOTSTRAP LOADER

Device	Starting Address
RF11	773 100
RK11	773 110
TC11	773 120
TM11	773 136
RP11	773 154
RC11	773 220

7-BIT ASCII CODE

Octal Code	Char.	Octal Code	Char.	Octal Code	Char.
000	NUL	053	+	126	V
001	SOH	054	,	127	W
002	STX	055	-	130	X
003	ETX	056	.	131	Y
004	EOT	057	/	132	Z
005	ENQ	060	0	133	[
006	ACK	061	1	134	\
007	BEL	062	2	135	]
010	BS	063	3	136	^
011	HT	064	4	137	-
012	LF	065	5	140	`
013	VT	066	6	141	a
014	FF	067	7	142	b
015	CR	070	8	143	c
016	SO	071	9	144	d
017	SI	072	:	145	e
020	DLE	073	;	146	f
021	DC1	074	<	147	g
022	DC2	075	=	150	h
023	DC3	076	>	151	i
024	DC4	077	?	152	j
025	NAK	100	@	153	k
026	SYN	101	A	154	l
027	ETB	102	B	155	m
030	CAN	103	C	156	n
031	EM	104	D	157	o
032	SUB	105	E	160	p
033	ESC	106	F	161	q
034	FS	107	G	162	r
035	GS	110	H	163	s
036	RS	111	I	164	t
037	US	112	J	165	u
040	SP	113	K	166	v
041	!	114	L	167	w
042	"	115	M	170	x
043	#	116	N	171	y
044	$	117	O	172	z
045	%	120	P	173	{
046	&	121	Q	174	|
047	'	122	R	175	}
050	(	123	S	176	~
051	)	124	T	177	DEL
052	*	125	U		

UNIBUS PIN ASSIGNMENTS

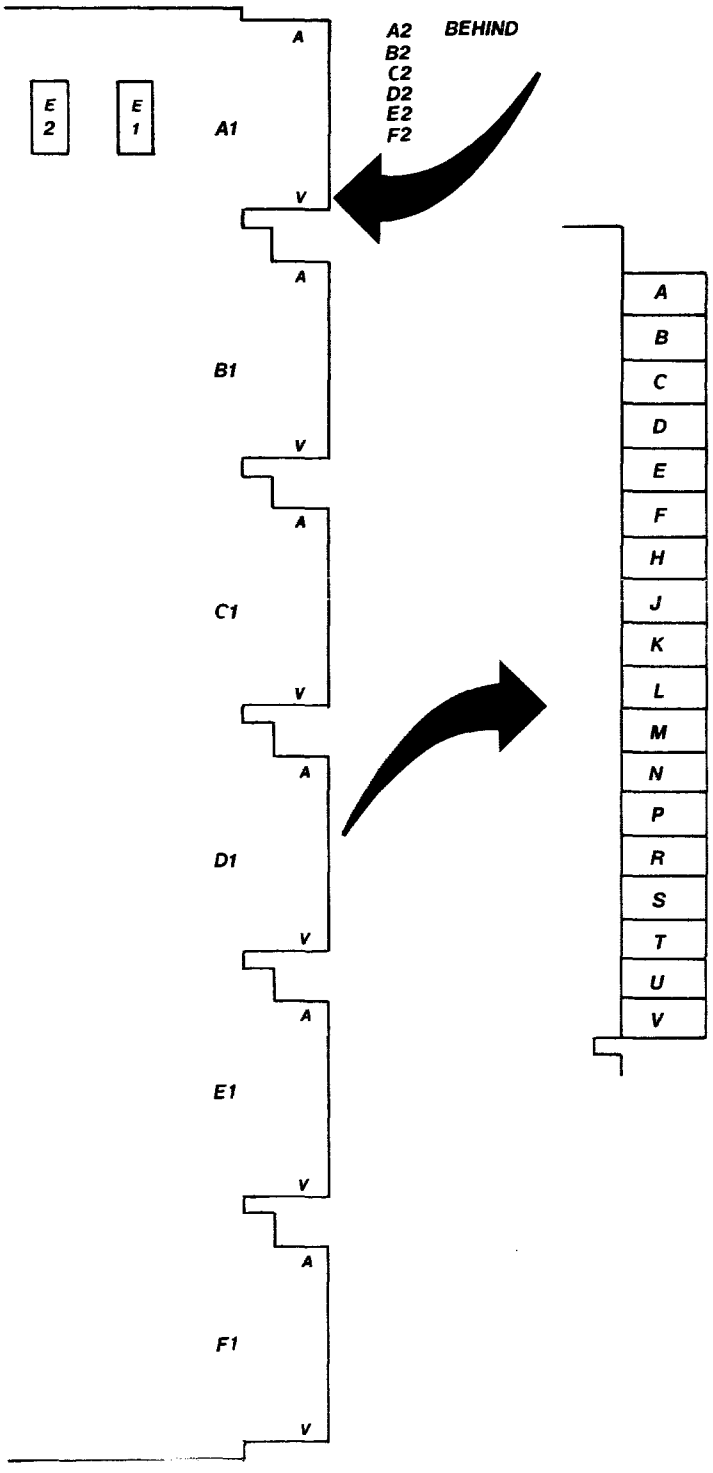
Pin	Signal		Pin	Signal	
AA1	INIT	L	BA1	BG6	H
AA2	Power (+5V)		BA2	Power (+5V)	
AB1	INTR	L	BB1	BG5	H
AB2	Ground		BB2	Ground	
AC1	DO0	L	BC1	BR5	L
AC2	Ground		BC2	Ground	
AD1	DO2	L	BD1	Ground	
AD2	DO1	L	BD2	BR4	L
AE1	DO4	L	BE1	Ground	
AE2	DO3	L	BE2	BG4	H
AF1	DO6	L	BF1	ACLO	L
AF2	DO5	L	BF2	DCLO	L
AH1	DO8	L	BH1	AO1	L
AH2	DO7	L	BH2	AO0	L
AJ1	D10	L	BJ1	AO3	L
AJ2	DO9	L	BJ2	AO2	L
AK1	D12	L	BK1	AO5	L
AK2	D11	L	BK2	AO4	L
AL1	D14	L	BL1	AO7	L
AL2	D13	L	BL2	AO6	L
AM1	PA	L	BM1	AO9	L
AM2	D15	L	BM2	AO8	L
AN1	Ground		BN1	A11	L
AN2	PB	L	BN2	A10	L
AP1	Ground		BP1	A13	L
AP2	BBSY	L	BP2	A12	L
AR1	Ground		BR1	A15	L
AR2	SACK	L	BR2	A14	L
AS1	Ground		BS1	A17	L
AS2	NPR	L	BS2	A16	L
AT1	Ground		BT1	Ground	
AT2	BR7	L	BT2	C1	L
AU1	NPG	H	BU1	SSYN	L
AU2	BR6	L	BU2	CO	L
AV1	BG7	H	BV1	MSYN	L
AV2	Ground		BV2	Ground	

UNIBUS PIN ASSIGNMENTS

Signal		Pin	Signal		Pin
AOO	L	BH2	DO6	L	AF1
AO1	L	BH1	DO7	L	AH2
AO2	L	BJ2	DO8	L	AH1
AO3	L	BJ1	DO9	L	AJ2
AO4	L	BK2	D1O	L	AJ1
AO5	L	BK1	D11	L	AK2
AO6	L	BL2	D12	L	AK1
AO7	L	BL1	D13	L	AL2
AO8	L	BM2	D14	L	AL1
AO9	L	BM1	D15	L	AM2
A1O	L	BN2	Ground		AB2
A11	L	BN1	Ground		AC2
A12	L	BP2	Ground		AN1
A13	L	BP1	Ground		AP1
A14	L	BR2	Ground		AR1
A15	L	BR1	Ground		AS1
A16	L	BS2	Ground		AT1
A17	L	BS1	Ground		AV2
ACLO	L	BF1	Ground		BB2
BBSY	L	AP2	Ground		BC2
BG4	H	BE2	Ground		BD1
BG5	H	BB1	Ground		BE1
BG6	H	BA1	Ground		BT1
BG7	H	AV1	Ground		BV2
BR4	L	BD2	INIT	L	AA1
BR5	L	BC1	INTR	L	AB1
BR6	L	AU2	MSYN	L	BV1
BR7	L	AT2	NPG	H	AU1
CO	L	BU2	NPR	L	AS2
C1	L	BT2	PA	L	AM1
DOO	L	AC1	PB	L	AN2
DO1	L	AD2	+5V*		AA2
DO2	L	AD1	+5V*		BA2
DO3	L	AE2	SACK	L	AR2
DO4	L	AE1	DCLO	L	BF2
DO5	L	AF2	SSYN	L	BU1

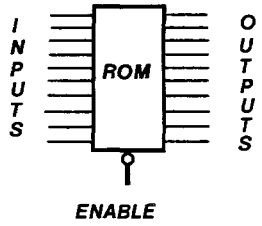
* +5V is wired to these pins to supply power to the bus terminator only. +5V should never be connected via the Unibus between system units.

MODULE CONTACT DESIGNATIONS



ROM MAPS

The inputs to a ROM are matrixed in a system of AND gates so that each combination of Hi and Lo input signals enables a particular internal bus-bar. If there are n inputs then there will be 2^n internal bus-bars.



Initially, the ROM chip is manufactured with every bus-bar connected via diodes to each of the outputs. In the 'blasting' process any undesired connection between a bus-bar and an output is rendered open-circuit. Thus each combination of inputs selects a particular combination of outputs. The particular way in which a ROM has been blasted is expressed in a ROM map. ROM maps are constructed to show the output combination which each unique input combination produces. They are laid out as follows:

OUTPUTS

```
                                    /( =Y4 (Pin   9) Conf MPC Ø3L
                                    ▲/( =Y3 (Pin  10) Conf MPC Ø2L
                                    ▲▲/( =Y2 (Pin  11) Conf MPC Ø1L
                                    ▲▲▲/( =Y1 (Pin  12) Conf MPC Ø4L
                                    ▲▲▲▲
Octal    Decimal                    ▲▲▲▲   Octal
Address  Address   HGFEDCBA         ▲▲▲▲   Data
  1ØØ      64     Ø1ØØØØØØ         ØØ11   ØØ3
  1Ø1      65     Ø1ØØØØØ1         ØØ11   ØØ3
  1Ø2      66     Ø1ØØØØ1Ø         ØØ11   ØØ3
   ¦        ¦        ¦              ¦      ¦
   ¦        ¦        ¦              ¦      ¦
  175      125     Ø11111Ø1         ØØ11   ØØ3
  176      126     Ø111111Ø         Ø1Ø1   ØØ5
  177      127     Ø1111111         ØØ11   ØØ3
                   ▲▲▲▲▲▲▲▲
INPUTS             ▲▲▲▲▲▲▲/( A(Pin #Ø5) is DPE CC Zero (1) H
                   ▲▲▲▲▲▲/( B(Pin #Ø6) is DPE CC Cout (1) H
                   ▲▲▲▲▲/( C(Pin #Ø7) is DPE CC Neg (1) H
                   ▲▲▲▲/( D(Pin #Ø4) is DPE CC Vbit (1) H
                   ▲▲▲/( E(Pin #Ø3) is DPF IR 1Ø (1) H
                   ▲▲/( F(Pin #Ø2) is DPF IR Ø9 (1) H
                   ▲/( G(Pin #Ø1) is DPF IR Ø8 (1) H
                   /( H(Pin #15) is DPF IR 15 (1) H
```

Note:

Pin designations differ from map to map.

When trouble shooting a processor, it is best to ignore the columns headed Octal Address, Decimal Address, and Octal Data. The column headed by a string of letters in reverse alphabetical order represents the possible input combinations. The pin numbers are given at the bottom of the column. The next column gives the output combination relevant to each particular input combination. The pin numbers are given at the top of the column.

PDP11 UNIBUS SIGNALS

Signal	Asserted	No of Lines	Function
Bus Address AO to A17	L	18	Specify an address in core, in the processor or in a peripheral device.
Bus Data DO to D15	L	16	Supply a 16-bit data word.
Bus Ctrl Line CO Bus Ctrl Line C1	L L	1 1	Define one of four Unibus operations.
N.P.R. (Non Processor Request)	L	1	Asserted by a device wishing to gain control of the bus without interrupting the current programme.
N.P.G. (Non-Processor Grant)	H	1	Asserted by the processor to grant bus control in response to a N.P.R.
B.R. (Bus Request)	L	4	Asserted by a device requesting bus control in order to interrupt the current program (four priority levels - BR7, BR6, BR5, BR4)
B.G. (Bus Grant)	H	4	Asserted by the processor to grant bus control in response to a B.R. (Four priority levels, BG7, BG6, BG5, BG4.)
Bus Sack	L	1	Asserted by a device to acknowledge an N.P.G. or a B.G.
Bus Bsy	L	1	Asserted by a device to take over bus control.
Bus Int. (Interrupt)	L	1	Asserted by a device after it has received bus control (B.Bsy asserted) to indicate to the processor that it wishes to interrupt the current programme. Simultaneously the device puts its vector address on the bus data lines. This vector address is the core address of the appropriate device-handling sub-routine.

Continued Overleaf

PDP11 Unibus Signals (Cont'd)

Signal	Asserted	No of Lines	Function
Bus M. Sync. (Master Sync.)	L	1	Asserted by bus master to inform slave that address, data and control signals are valid on the bus.
Bus Slave Sync.	L	1	Asserted by slave to inform the bus master that he (slave) has completed the instruction issued by the master.
Bus A.C. LO	L	1	Monitors A.C. power supply and initiates power fail routine in the event of a failure.
Bus D.C. LO	L	1	Held high for 70 milli-seconds during power fail routine.
Bus Parity	L	2	Used by parity memory option.
Bus Initialise	L	1	20 millisecond pulse used to clear all device registers on the bus. Generated at 1. Power Up 2. Start Switch 3. Reset Instruction

INFORMATION DIRECTORY

In this list the abbreviations used indicate the book in which the information will be found.

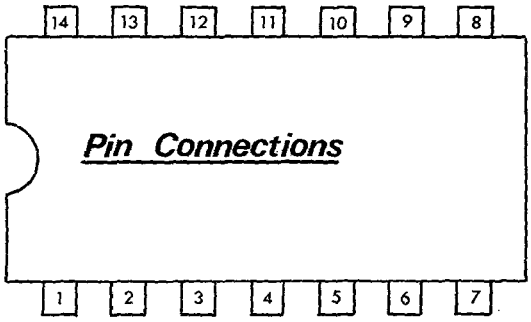
11/05CM	PDP11/05 Computer Manual
11/40SMM	PDP11/40 System Maintenance Manual
KD11/A.PM	KD11/A Processor Manual
PH	Peripherals Handbook, 1973-74
11Pr.HB	PDP11 05/10/35/40 Processor Handbook
RMM	Relevant Maintenance Manual
11/45Pr.HB	PDP11/45 Processor Handbook

IC INDEX

This section contains basic information on the more common devices in use within the company. The information is laid out in the following form:

Device Designator

Dec Part No.

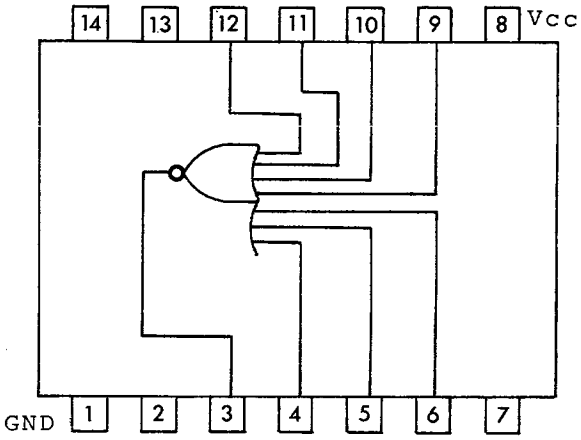


Title

Amplifying or detailed information follows the diagram. Further details can be found in the published data of the major manufacturers or in the purchase specification (held in the reproduction centre).

WHERE THIS INDEX DISCLOSES A SIMILARITY BETWEEN DEVICES, UNDER NO CIRCUMSTANCES IS IT TO BE TAKEN AS AN AUTHORITY TO EFFECT A SUBSTITUTION.

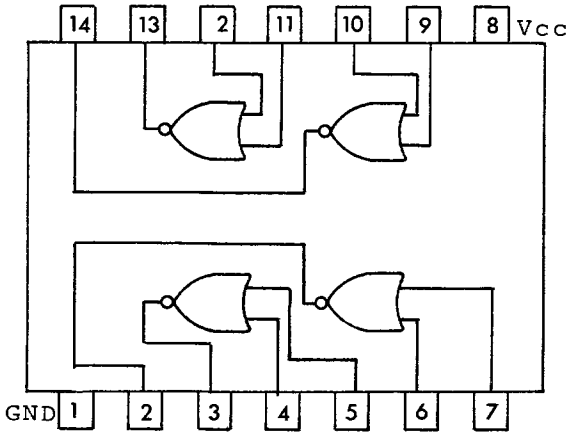
314



19-09704

Single
7-Input
NOR Gate

380



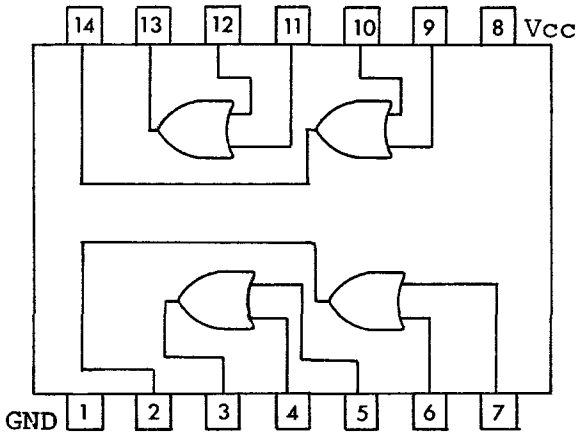
19-09485

Quad
2-Input
NOR Gate

384

19-09486

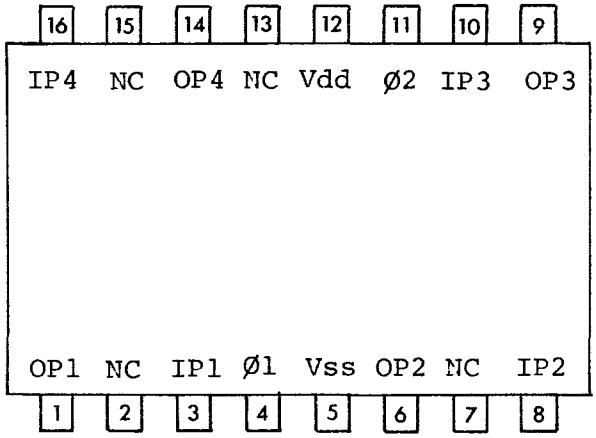
Quad
2-Input
OR Gate



1402

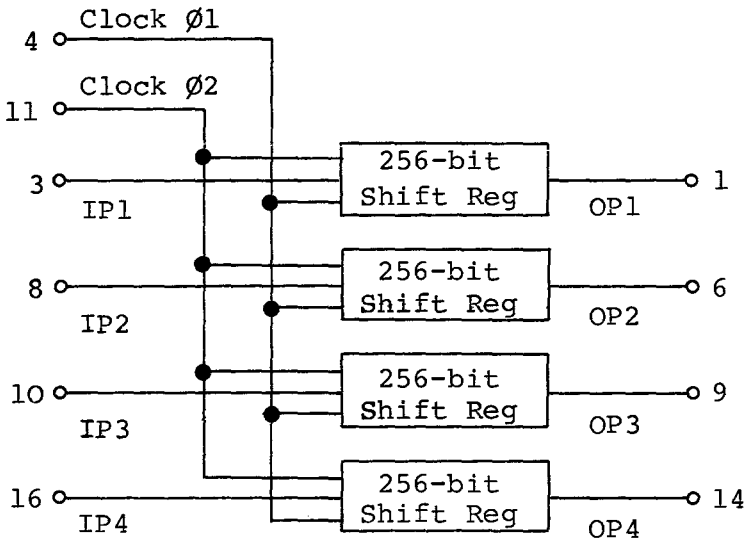
19-10206

Quad
256-bit
Shift Reg.



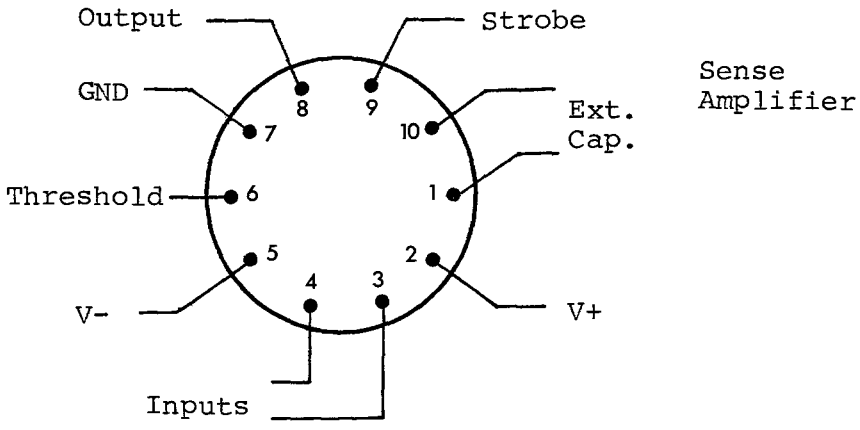
This device can be used as a quad 256-bit shift register, or a dual 512-bit shift register, or a 1024-bit shift register, by suitably interconnecting the inputs and outputs of the individual registers.

This is a MOS device and uses a Vss of +5V and a Vdd of -5V. Clock Ø2 is the antiphase version of clock Ø1. Both clock inputs are required for the shifting action to take place.



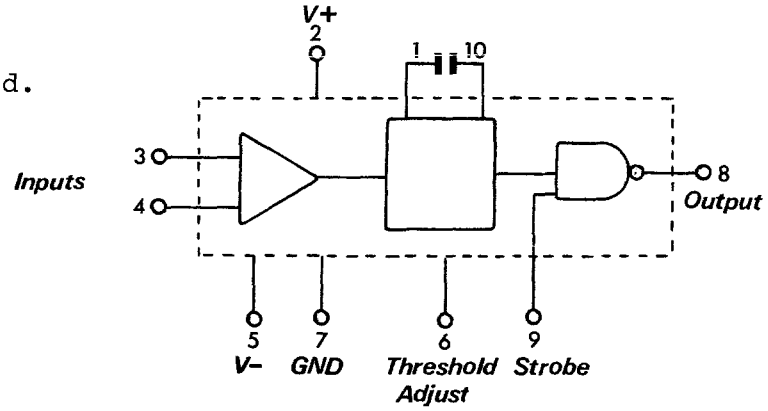
1540G

19-05521



Continued Overleaf

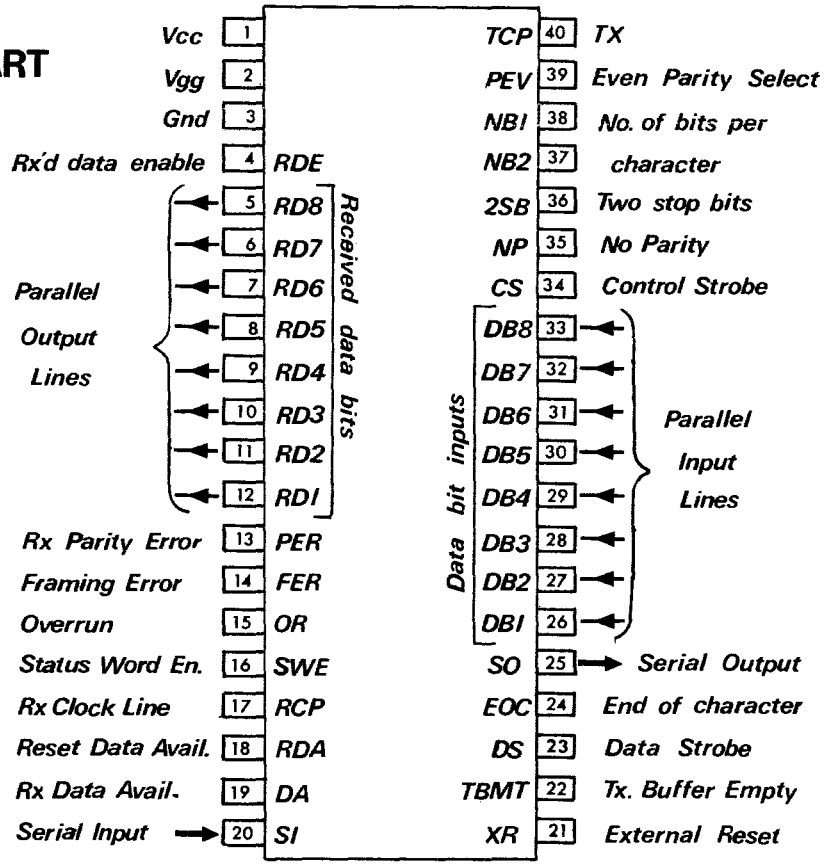
1540G cont'd.



1808

19-10459

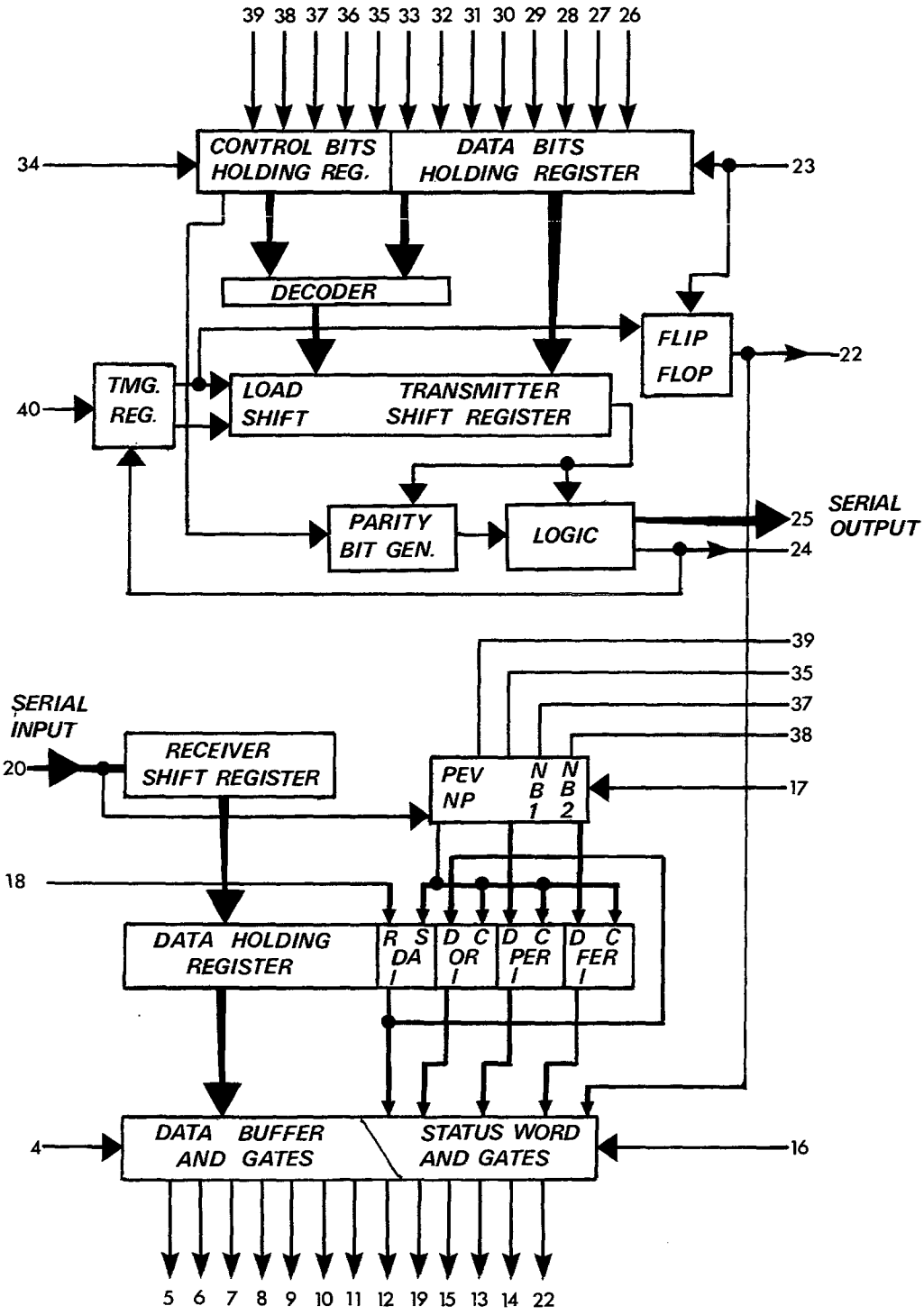
UART



PIN NO.	SYMBOL	NAME	FUNCTION
1	Vcc	Vcc Power Supply	+5v. supply
2	Vgg	Vgg Power Supply	-12v. supply
3	Gnd	Ground	Ground
4	RDE	Received Data Enable	A low on the receiver enable line places the received data onto the output lines.
5-12	RD8-RD1	Received Data Bits	These are the 9 data output lines. These lines may be "Wire-Ored". When 5, 6, or 7 level code is selected the most significant unused bits are Low. Character will be right justified into the least significant bits. RD1 (Pin 12) is the least significant bit, RD8 (Pin 5) is the most significant bit. A High indicates a Mark.
13	PER	Receive Parity Error	This line goes to a High if the received character parity does not agree with the selection (Pin 39).
14	FER	Framing Error	This line goes to a High if the received character has no valid Stop bit. i.e. the bit following the Parity bit is not marking.
15	OR	Overrun	This line goes to a High if the previously received character is not read (DA line not Reset) before the present character is transferred to the receiver holding register.
16	SWE	Status Word Enable	A Low on this line places the Status Word bits (PE, DA, TBMT, FE, OR) onto the output lines.
17	RCP	Receiver Clock Line	Requires a clock 16 times required Rx baud rate.
18	RDA	Reset Data Available	A Low on this line will reset the DA line.

Continued Overleaf

PIN NO.	SYMBOL	NAME	FUNCTION
19	DA	Received Data	This line goes to a High when an entire character has been received and transferred to the receiver Holding register.
20	SI	Serial Input	This line accepts the Serial bits input stream. A High must be present when Data is not being received. High is a Mark. Low is a Space.
21	XR	External Reset	Should be pulsed after Power turn on to a High. Reset all registers. Sets Serial Output line to a High. Sets TBMT to a High. Sets EOC to a High.
22	TBMT	Transmitter Buffer Empty	The Transmitter Buffer Empty flag goes to a High when the data bits Holding Register may be loaded with another character.
23	DS	Data Strobe	A Low to High transition on this line will enter the data bits into the Data Bits Holding Register. Data loading is controlled by the rising edge of DS.
24	EOC	End of Character	This line goes to High each time a full character including Stop bits is transmitted. It remains at this level until the start of transmission which is the mark to space transition of the Start bit. It will remain at a High when data is not being transmitted.
25	SO	Serial Output	This line will serially, by bit, provide the entire transmitted character. It will remain at a High when no data is being transmitted. High is a Mark, Low is a Space.
26-33	DB1-DB8	Data Bit Inputs	These are the 8 parallel data input lines. If 5, 6 or 7 bits are transmitted the least most significant bits are used. DB1 is the least significant bit (Pin 26). DB8 is the most significant bit, (Pin 33). A High input will cause a mark (High) to be transmitted.



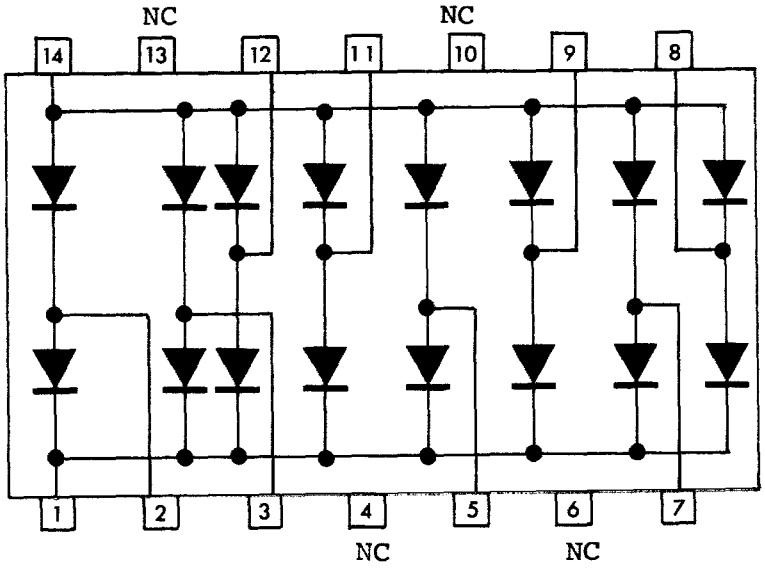
Continued Overleaf

PIN NO.	SYMBOL	NAME	FUNCTION
34	CS	Control Strobe	A high on this lead will enter the control bits (POE, NB1, NB2, SB, NP) into the control bits Holding register. This line can be strobed or hard wired to a High level.
35	NP	No Parity	A High on this lead will eliminate the parity bit from the transmitted and received character. The stop bits will immediately follow the last data bit on transmission. The receiver will not check parity or reception. It will, when asserted, also clamp the PE to a Low.
36	2SB	Two Stop Bits	This lead will select the number of stop bits. 1 or 2 to be appended immediately after the parity bit. A low will insert 1 stop bit and a High will insert 2 stop bits.
37-38	NB2, NB1	Number of Bits/ Charact.	37 38 Bits/Character L L 5 L H 6 H L 7 H H 8
39	PEV	Even Parity Select	L Inserts/checks odd H Inserts/checks even
40	TCP	Trans-mitter	Requires clock freq. 16 times required Tx baud rate.

2501

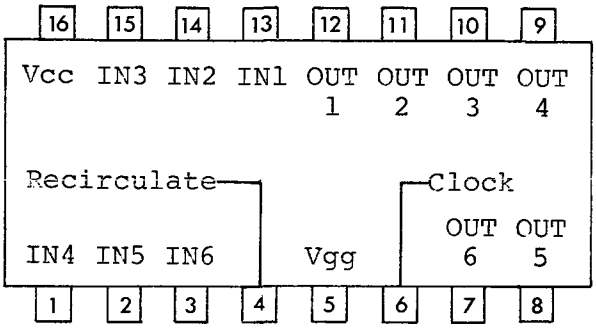
19-10010

Diode Array 16 Core Driver

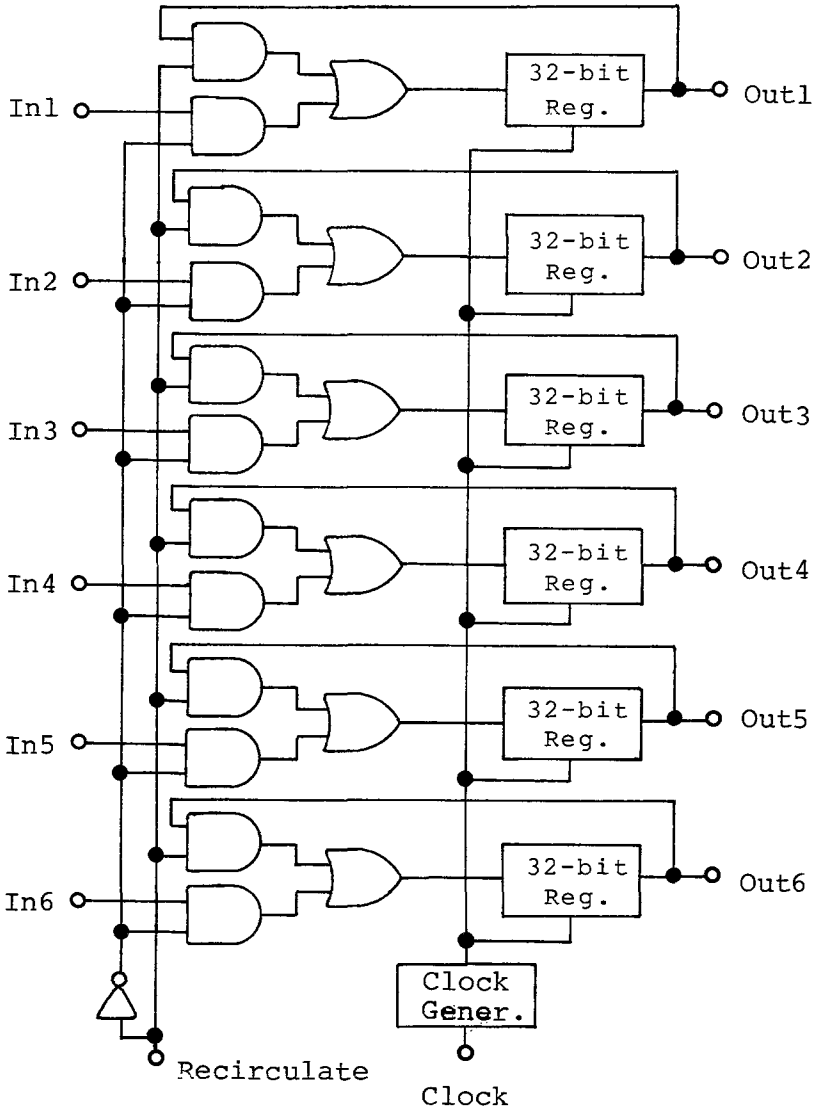


2518

21-11049



Hex 32-bit
Shift
Register



Continued Overleaf..

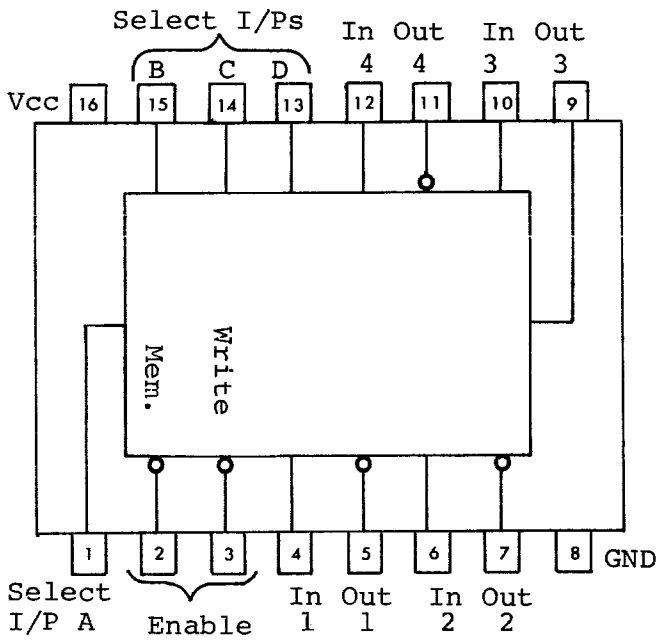
RECIRCULATE	FUNCTION
1	Registers recirculate
0	Data entered from inputs

NOTE: Recirculate is also labelled "load".

3101

19-10653

64-bit
Read
Write
Memory



A matrix of 64 flip flops arranged to give 16 words of 4 bits each. The required word is addressed via the 4 select inputs.

WRITE Data at the inputs is entered at the selected address.

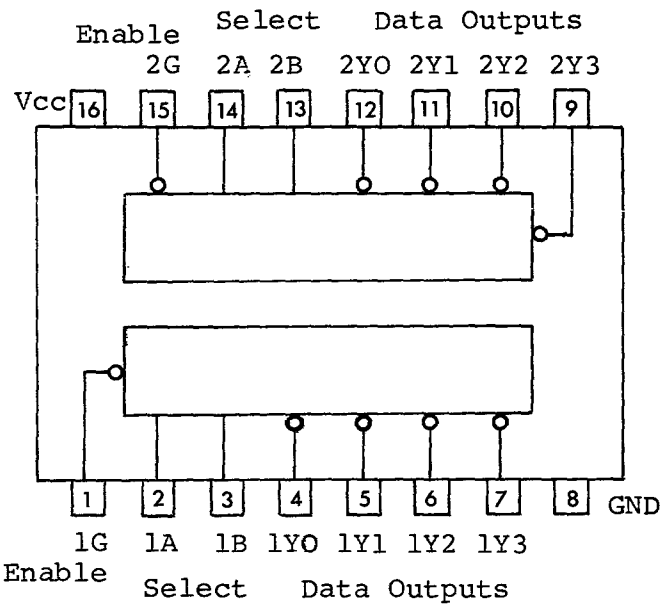
READ The complement of the data stored at the selected address is non-destructively read at the sense outputs.

ME	WR	OPERATION
L	L	Write
L	H	Read
H	L	Inhibit
H	H	-

Open collector outputs are provided to allow expansion of the word length. Thus, several devices can be used together to form a fast-access (approx. 33 ns) scratch-pad memory.

4007

19-09867



Dual
2-line to
4-line
Decoder

INPUTS			OUTPUTS			
ENABLE	SELECT					
G	B	A	YO	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

Assigns the input (L at ENABLE) to one of 4 outputs, determined by the 'SELECT' settings.

5314

19-10391

See 314.

A version of 314 selected for speed of operation and noise immunity.

5380

19-10392

See 380.

A version of 380 selected for speed of operation and noise immunity.

5384

19-10394

See 384.

A version of 384 selected for speed of operation and noise immunity.

5603

23-000A2-03

See 74187 for pin connections.

A version of the same device but data is not entered by the manufacturer.

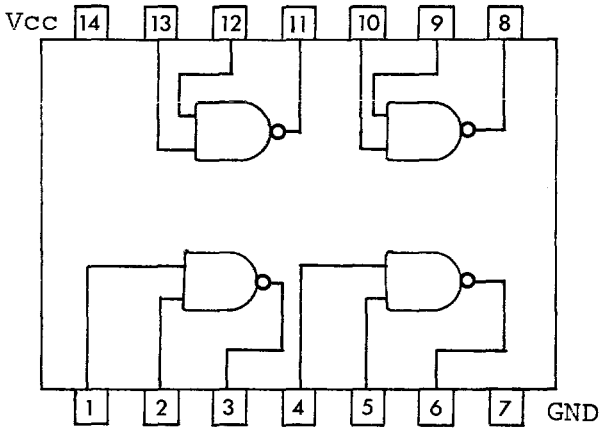
6380

19-09971

See 380.

A version of 380 selected for speed of operation and noise immunity.

7400



19-05575

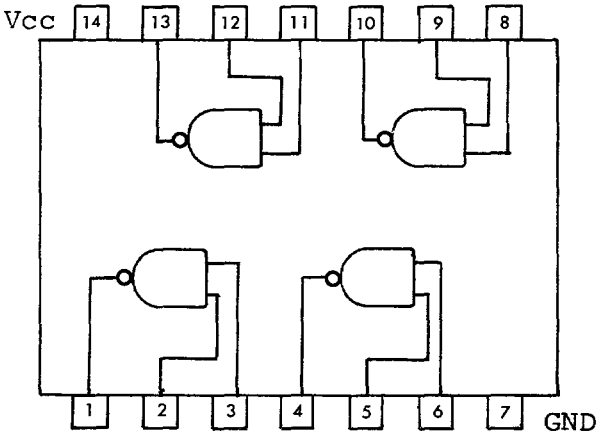
Quad
2-Input
NAND Gate

74H00

See 7400.

19-09056

7401



19-05590

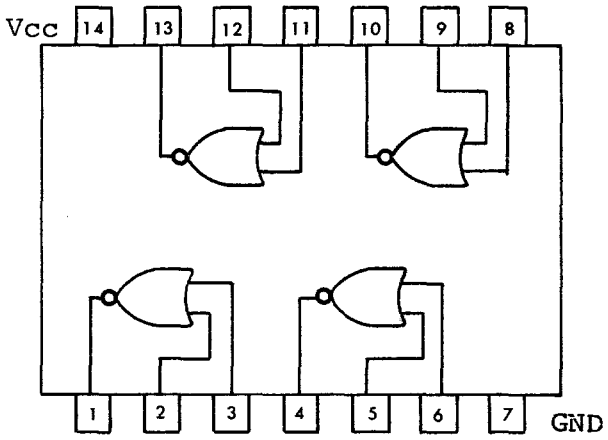
Quad
2-Input
NAND Gate

Open collector outputs.

7402

19-09004

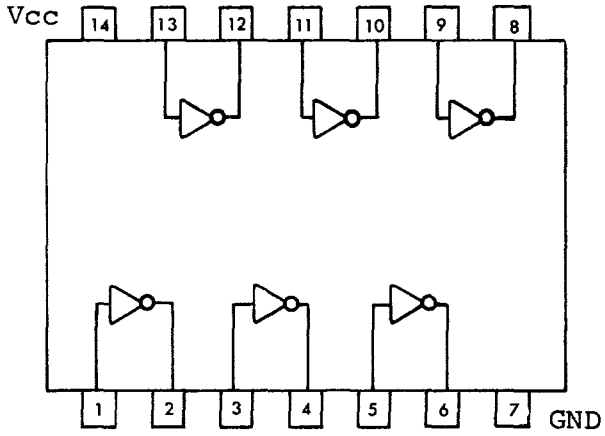
Quad
2-Input
NOR Gate



7404

19-09686

Hex
Inverter



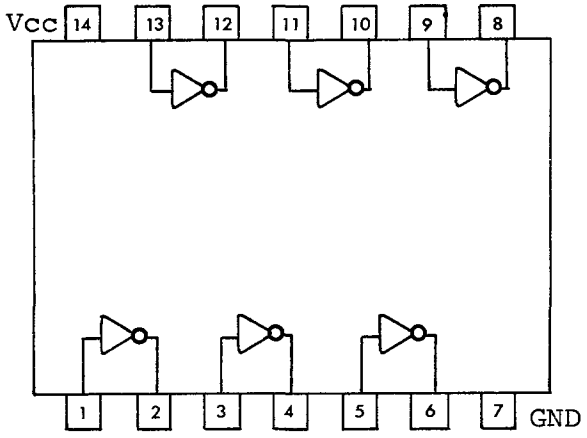
74H04

See 7404.

19-09931

7405

19-09930

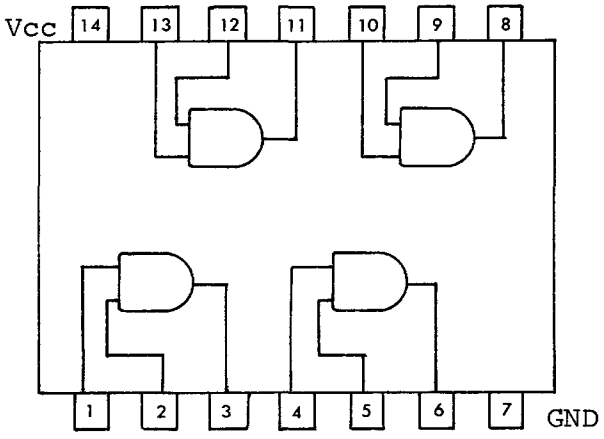


Hex
Inverter

Open collector outputs.

7408

19-10155

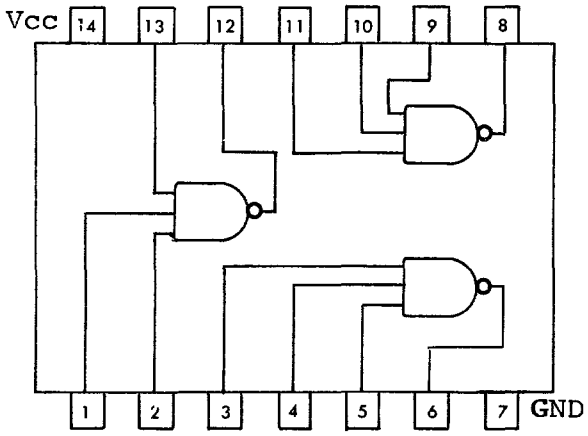


Quad
2-Input
AND Gate

7410

19-05576

Triple
3-Input
NAND Gate



74H10

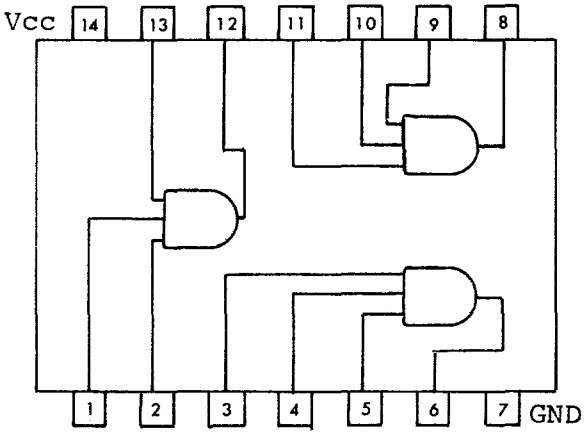
See 7410.

19-09057

74H11

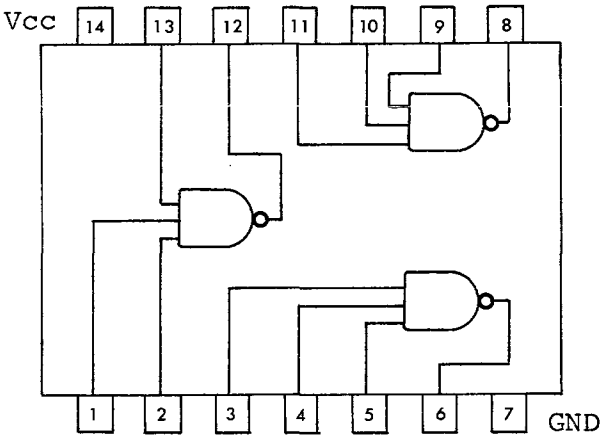
19-09267

Triple
3-Input
AND Gate



7412

19-09955

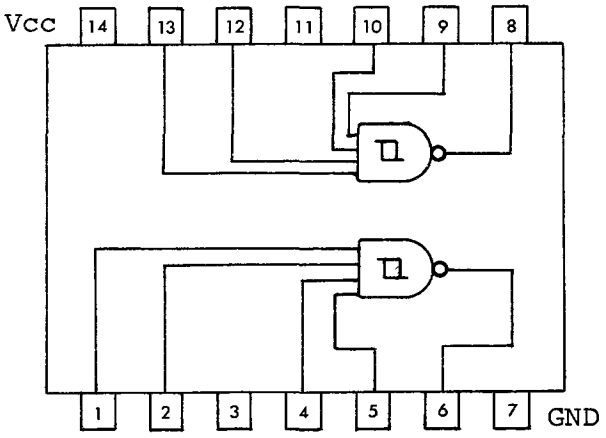


Triple
3-Input
NAND Gate

Open collector outputs

7413

19-09989

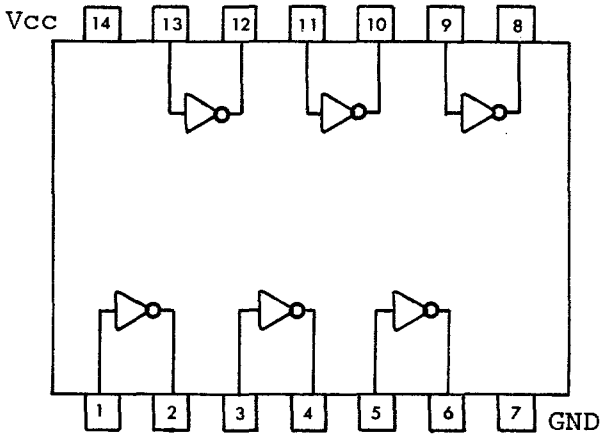


Dual
4-input
NAND
Schmitt
Triggers

7416

19-09928

Hex
Inverter
Buffer/
Driver

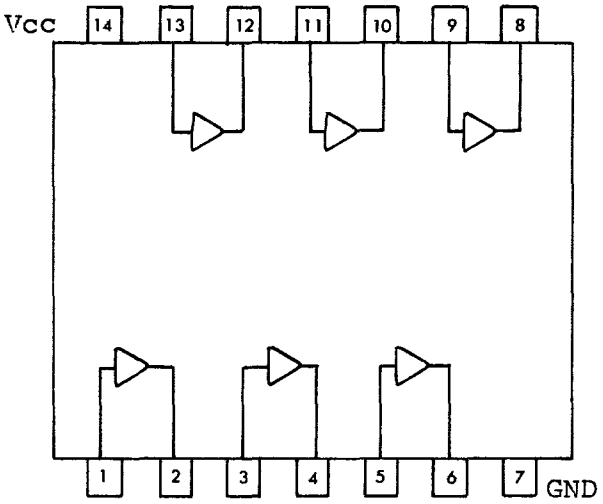


Open collector high voltage outputs.

7417

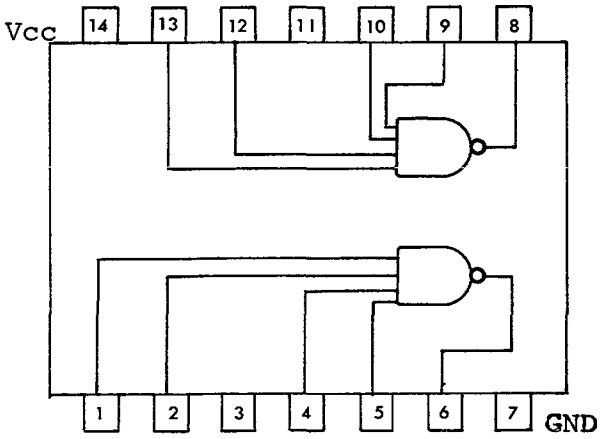
19-09929

Hex
Buffer/
Driver



Open collector high voltage outputs.

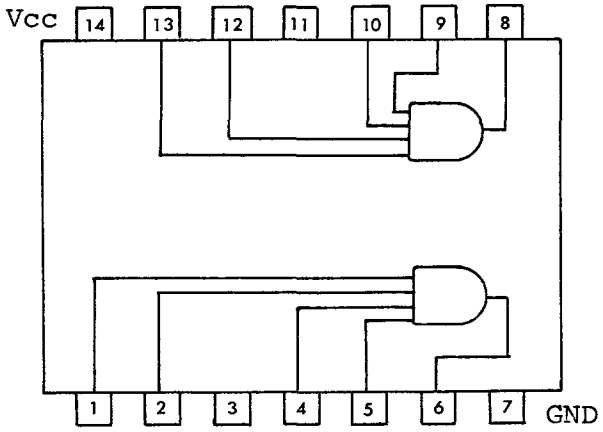
7420



19-05577

Dual
4-Input
NAND Gate

74H21



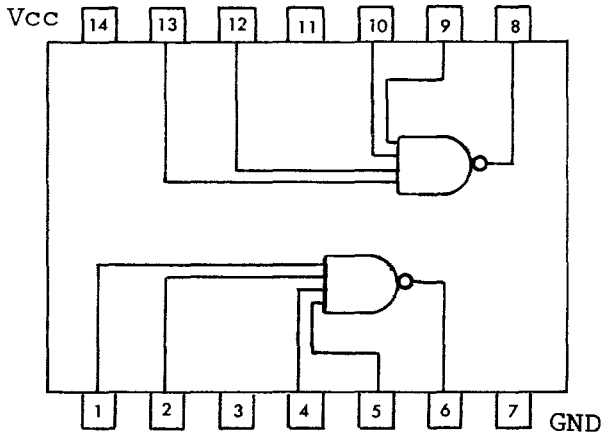
19-09058

Dual
4-Input
AND Gate

74S22

19-10540

Dual
4-Input
NAND Gate

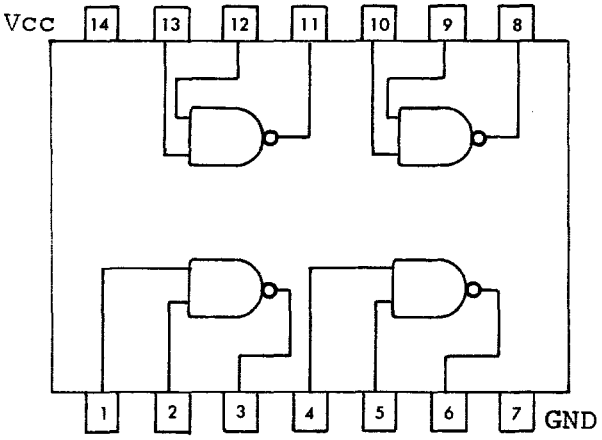


Open collector outputs

7426

19-10236

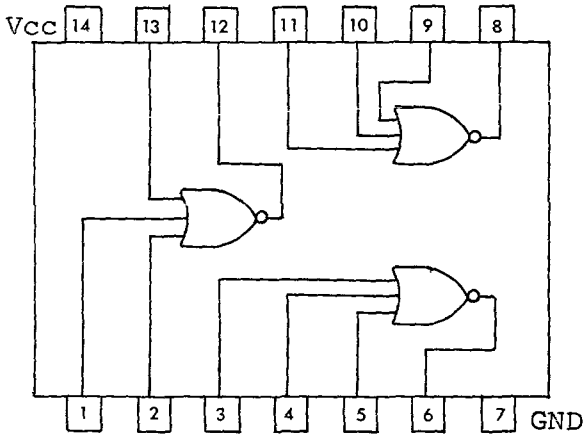
Quad
2-Input
NAND Gate



High voltage interface.

7427

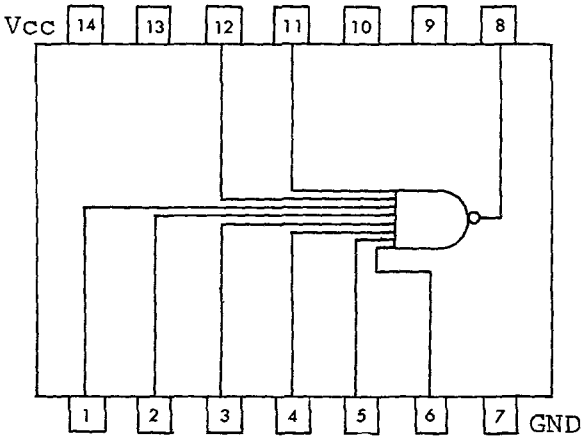
19-10878



Triple
3-Input
NOR Gate

7430

19-05578

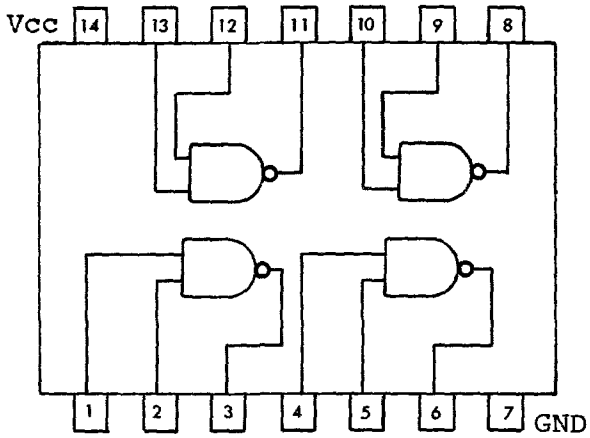


8-Input
NAND
Gate

7437

19-10091

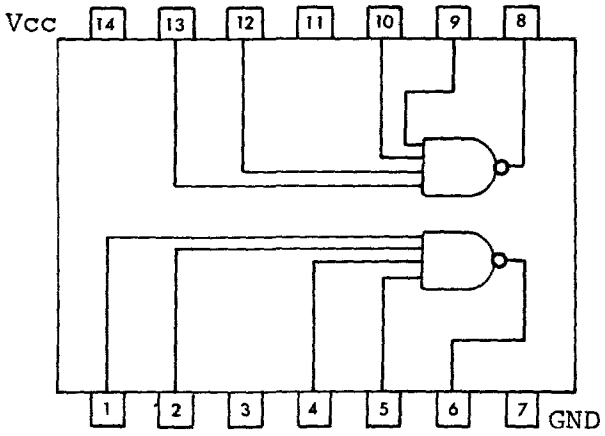
Quad
2-Input
NAND
Buffer



7440

19-05579

Dual
4-Input
NAND
Buffer

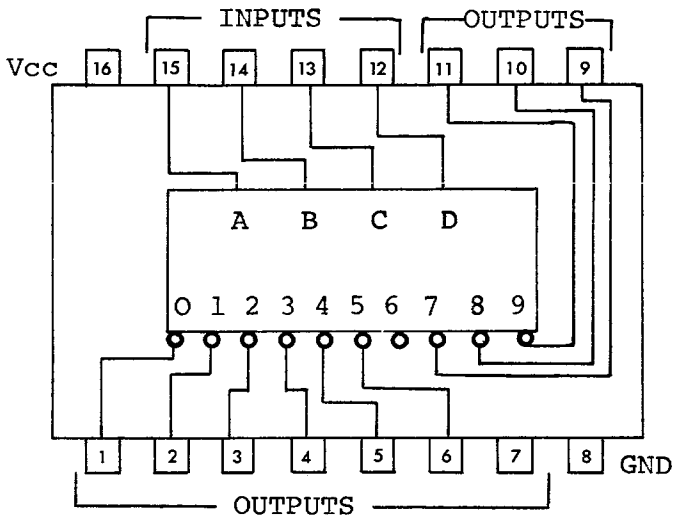


74H40

See 7440.

19-05586

7442



19-10046

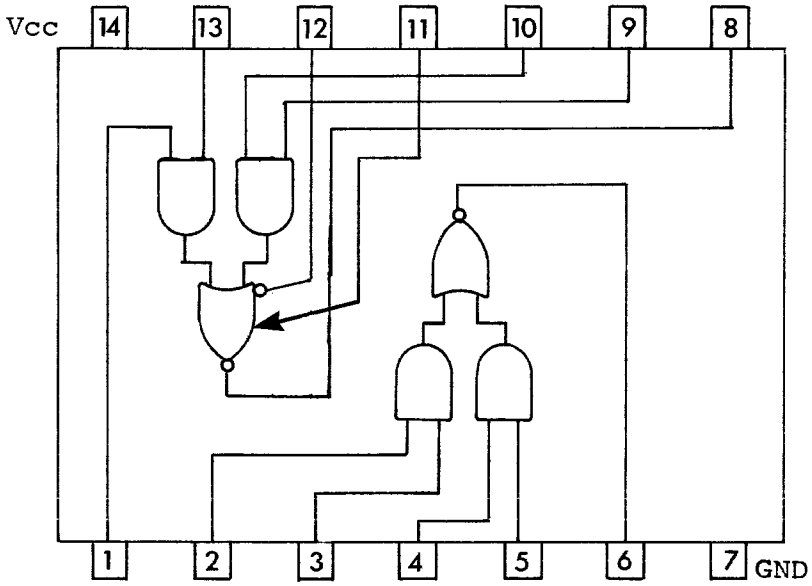
BCD to Decimal Decoder

INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

7450

19-05580

Dual
2-Wide
2-Input
AND-OR
Invert
Gate



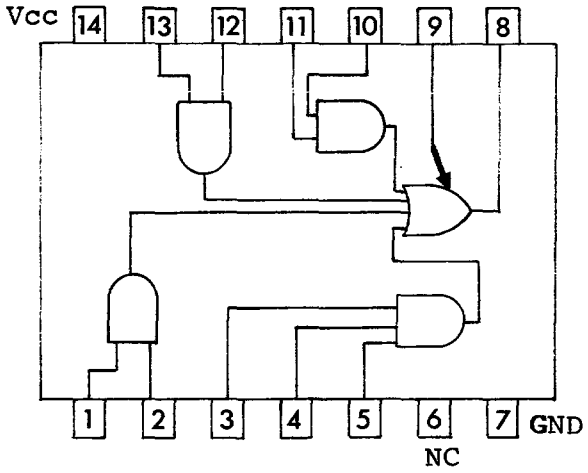
Used in X-OR, comparator and select functions.

74H50

See 7450.

19-09060

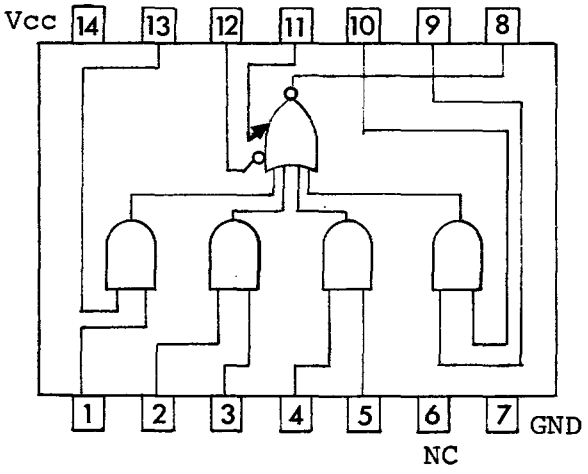
74H52



19-09061

Expandable
4-Wide
AND-OR
Gate

7453



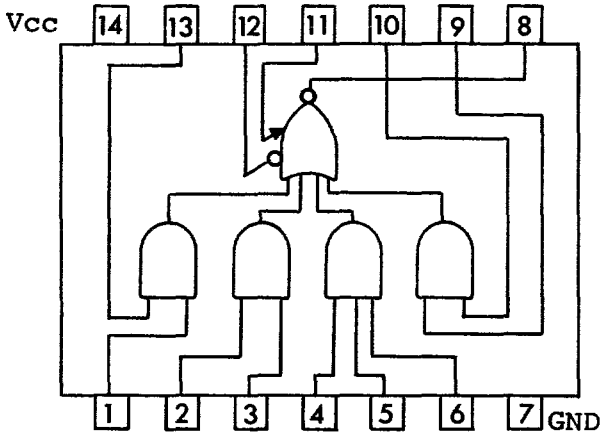
19-05582

Expandable
4-Wide
AND-OR
Invert Gate

74H53

19-09062

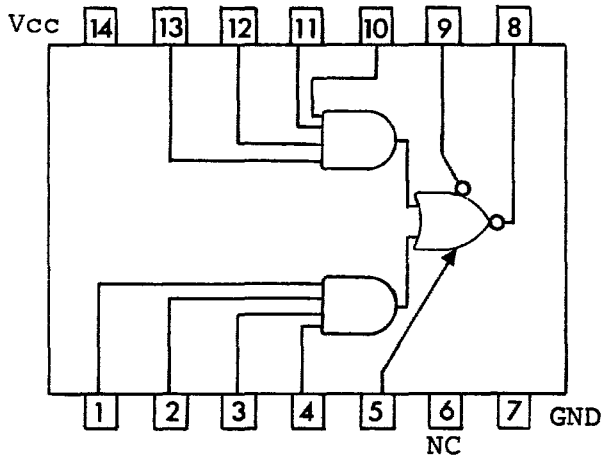
Expandable
4-Wide
AND-OR
Invert
Gate



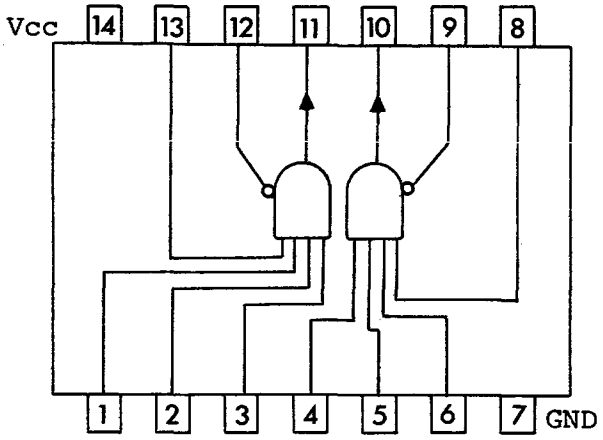
74H55

19-09063

Expandable
2-Wide
4-Input
AND-OR
Invert
Gate



7460



19-05581

Dual
4-Input
Expander

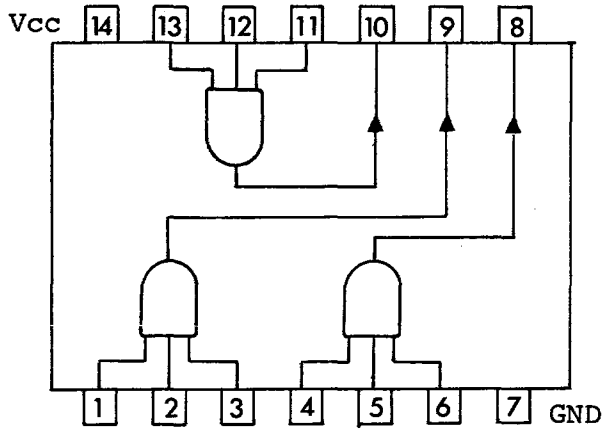
Used in conjunction with
expandable gates.

74H60

See 7460.

19-09064

74H61



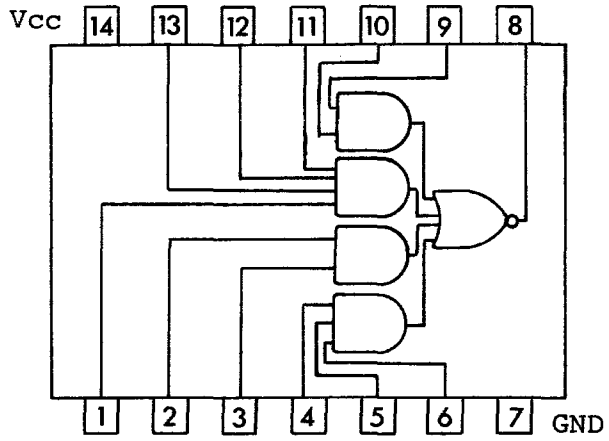
19-09065

Triple
3-Input
Expander

74S64

19-10542

4-2-3-2
Input
AND-OR
Invert
Gate



74S65

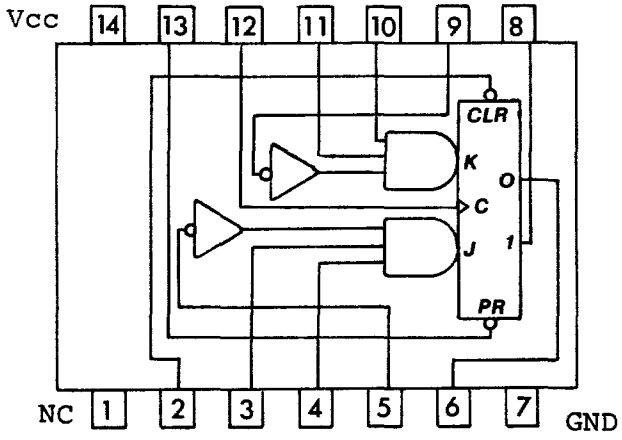
As 74S64, with open collector outputs.

19-10543

7470

19-05589

Gated
J - K
Flip-Flop



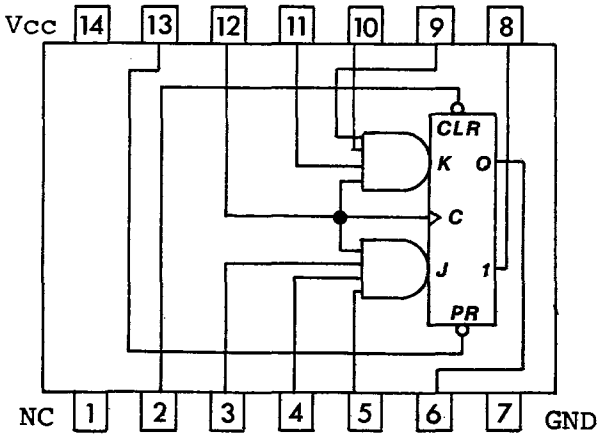
INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	1	ø
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	↑	H	L	H	L
H	H	↑	L	H	L	H
H	H	↑	L	L	No Change	
H	H	↑	H	H	Changes	
H	H	L	X	X	No Change	

$J = J1.\ J2.\ \overline{J3}$

$K = K1.\ K2.\ \overline{K3}$

Input information is transferred to the outputs on the positive-going edge of the clock pulse.

74H72



19-09068

J-K
Flip-Flop

Continued Overleaf..

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	1	Ø
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	⎍	L	L	No Change	
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	Changes	

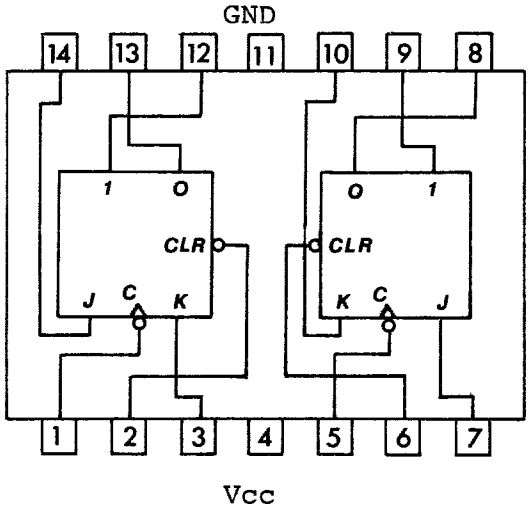
J = J1. J2. J3

K = K1. K2. K3

7473

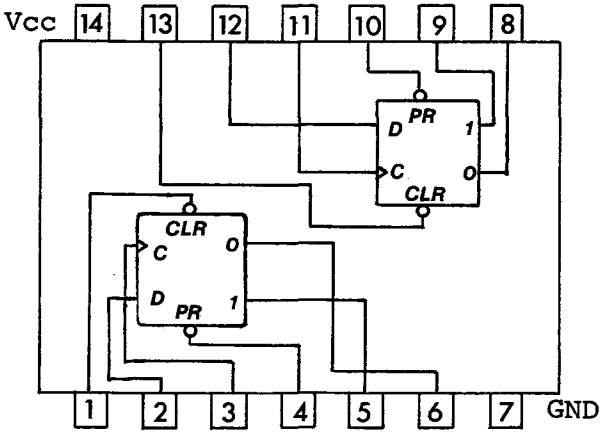
19-05587

Dual
J-K
Flip Flop



INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	1	0
L	X	X	X	L	H
H	⎍	L	L	No Change	
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	Changes	

7474



19-05547

Dual
D-Type
Flip Flop

Continued Overleaf..

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	1	Ø
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	No Change	

74H74

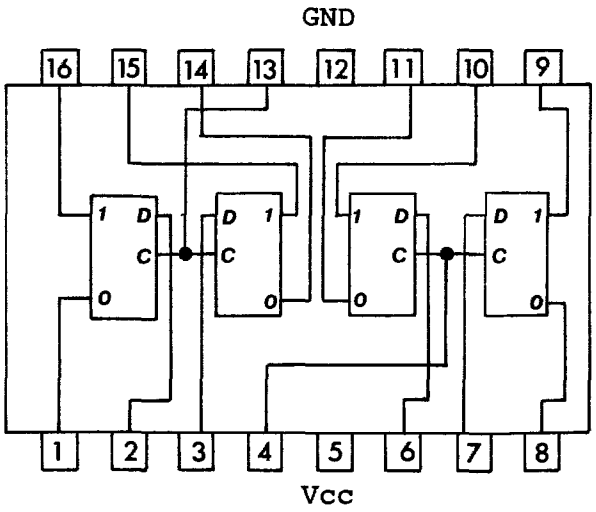
See 7474.

19-09667

7475

19-09050

Quad
Bistable
Latch

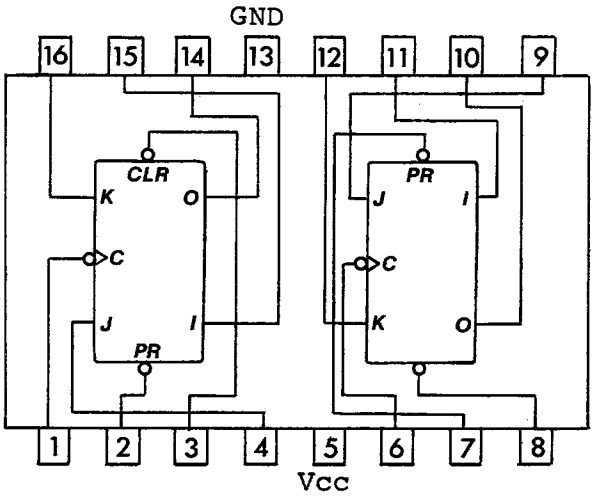


Function Table
for each latch

INPUTS		OUTPUTS	
D	C	1	Ø
L	H	L	H
H	H	H	L
	L	No Change	

When the Enable (C) is H each latch responds to the information at its D input, i.e.: latch RESETS when D goes low - SETS when D goes H. The transition of Enable to L causes the latches concerned to lock in their pre-transition state.

7476



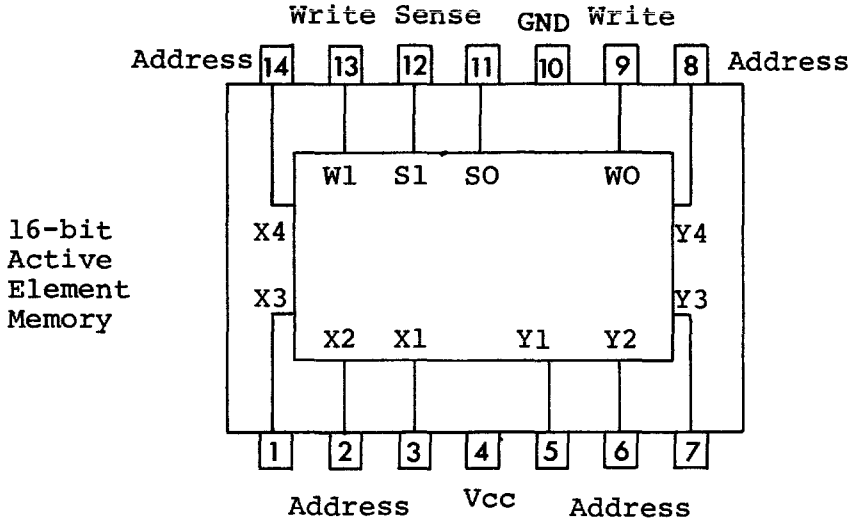
19-05585

Dual
J - K
Flip-Flop

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	1	Ø
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	⎍	L	L	No Change	
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	Changes	

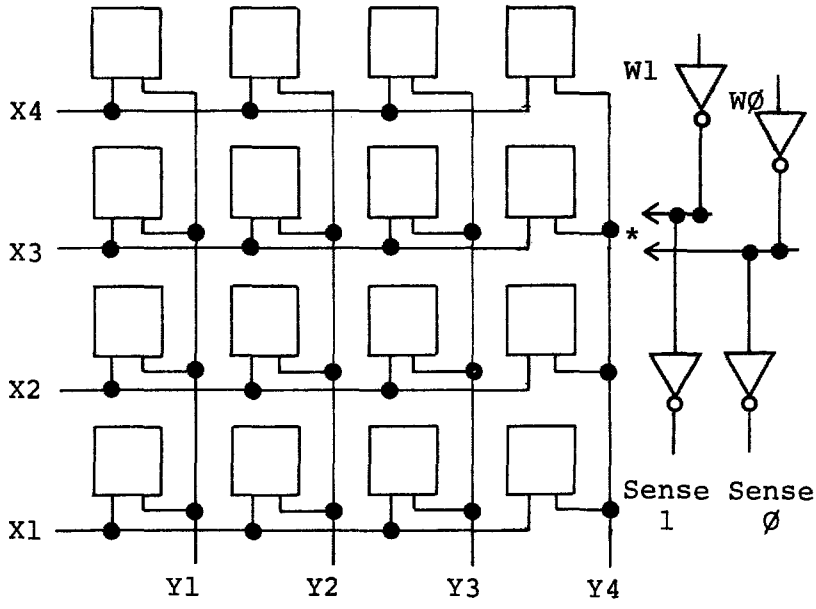
7481

19-09714



16-bit Active Element Memory

16 Flip-flops arranged in a 4 x 4 matrix. Each flip-flop is 1 bit of 16 words : the word length is determined by the number of memories connected in parallel.



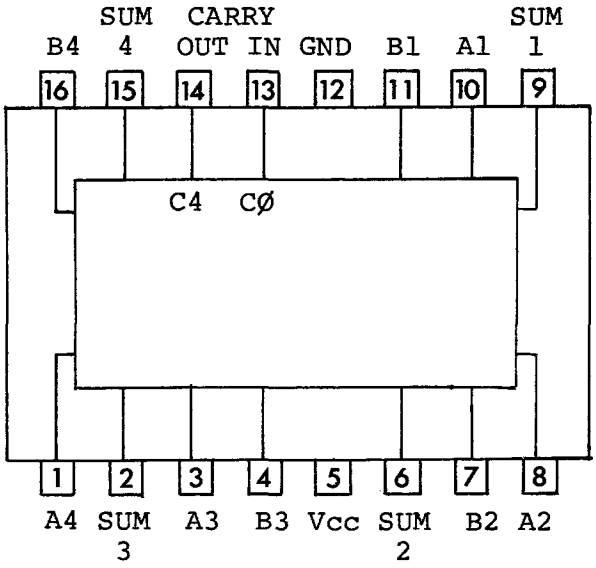
* To all 16 flip-flops.

To address a flip-flop (word) the X and Y lines associated with that flip-flop are taken H.

To store information, the required flip-flop is addressed and a High applied to W1 (to write a 1) or WØ (to write a Ø).

To read information, the state of the addressed flip-flop is found at the sense outputs. Reading is non-destructive. The memory is volatile - data is lost if Vcc is removed.

7483



19-09932

4-bit Binary Full Adder

A1-4 = Number

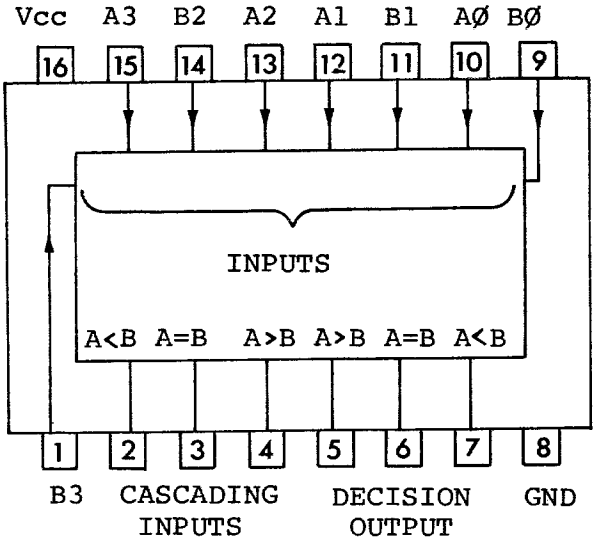
B1-4 = Addend

S1-4 = Sum

7485

19-10224

4-Bit
Magnitude
Comparator



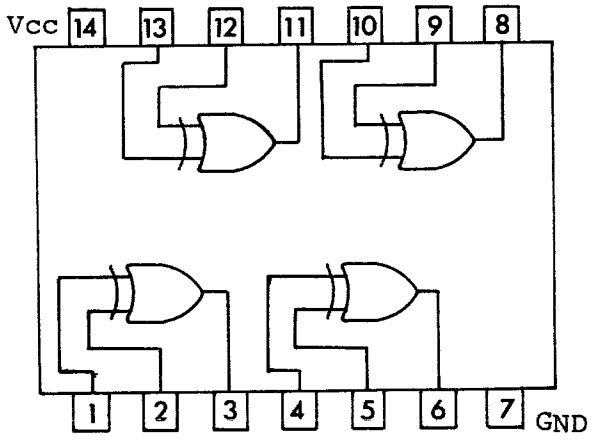
Compares two 4-bit numbers for magnitude and indicates the decision with a H on the appropriate output line.

When devices are cascaded to allow comparison of numbers larger than 4 bits, the decision outputs are connected to the related cascading inputs of the device handling the next most significant bits. The stage handling the least significant bits must have a H applied to the A=B input.

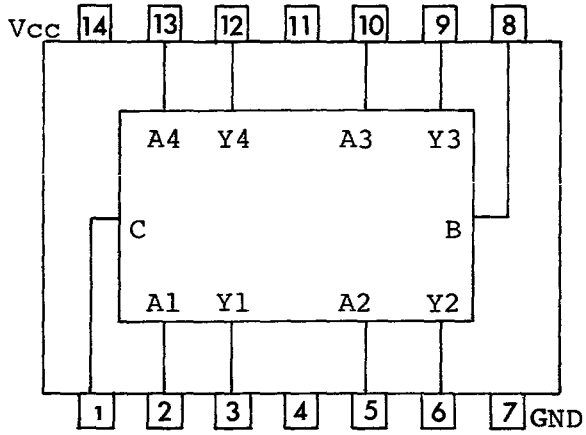
7486

19-10011

Quad
2-Input
Exclusive-OR
Gate



74H87



19-09927

4-bit
True/
Complement
Zero/one
Element

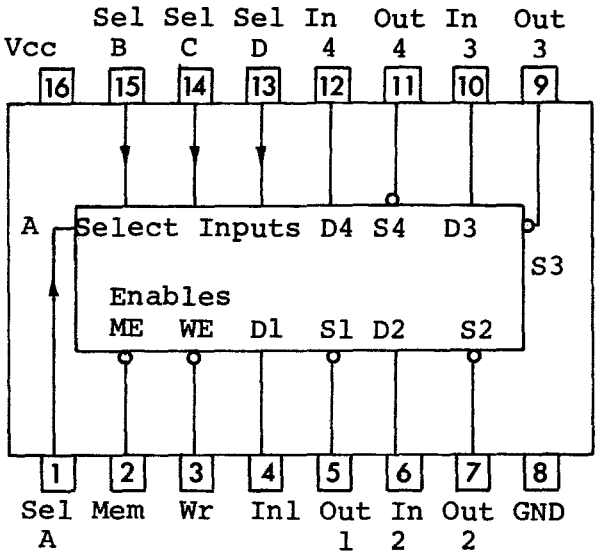
Operation is controlled by the B and C inputs to transmit the data at the inputs (A1 - 4) to the outputs (Y1 - 4) either true or complemented; or to set the outputs to the complement of the C input. Thus:-

CONTROL INPUTS		OUTPUTS			
B	C	Y1	Y2	Y3	Y4
L	L	$\overline{A1}$	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$
L	H	A1	A2	A3	A4
H	L	H	H	H	H
H	H	L	L	L	L

7489

19-10396

64-bit
Read/
Write
Memory

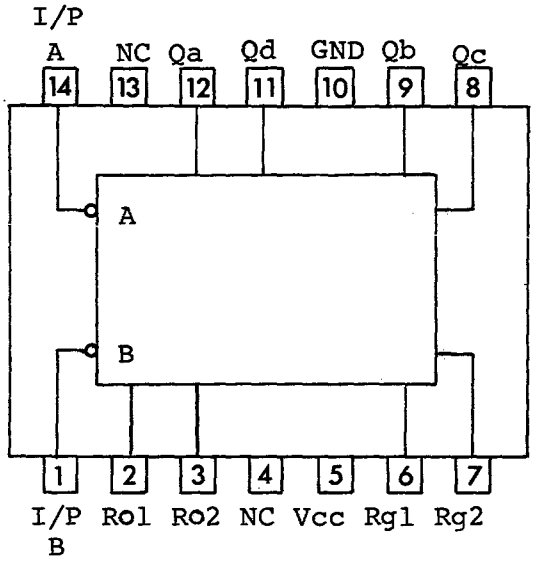


64 flip-flops arranged to give 16 4-bit words. Open collector outputs allow expansion of word length and the number of words.

The required word is addressed in binary on the select inputs: data can then be written or read:-

OPERATION	ME	WE	OUTPUT STATE
Write	L	L	Complement of data in
Read	L	H	Complement of Sel word
Inhibit Storage	H	L	Complement of data in
-	H	H	High

7490



19-09051

Decade Counter

Counts the H to L transitions at the A input. The maximum count before reset is determined by the connections to I/P A and I/P B. e.g. with Qa connected to B:

COUNT	OUTPUT			
	Qd	Qc	Qb	Qa
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

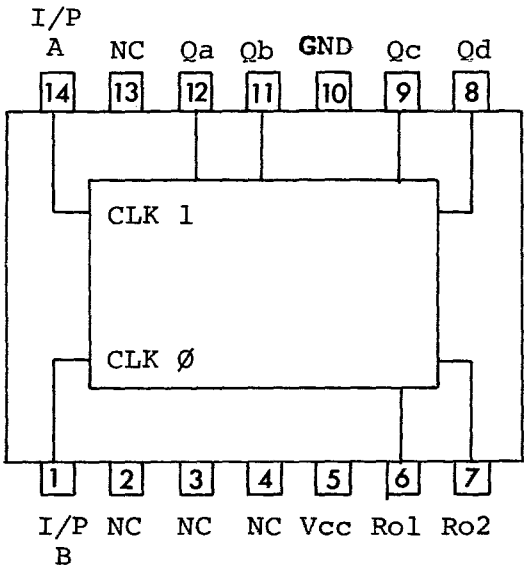
RESET INPUTS				OUTPUT			
Ro1	Ro2	Rg1	Rg2	Qd	Qc	Qb	Qa
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X				
L	X	X	L				
X	L	L	X				

FUNCTION TABLE

7492

19-09053

Divide
By
Twelve
Counter



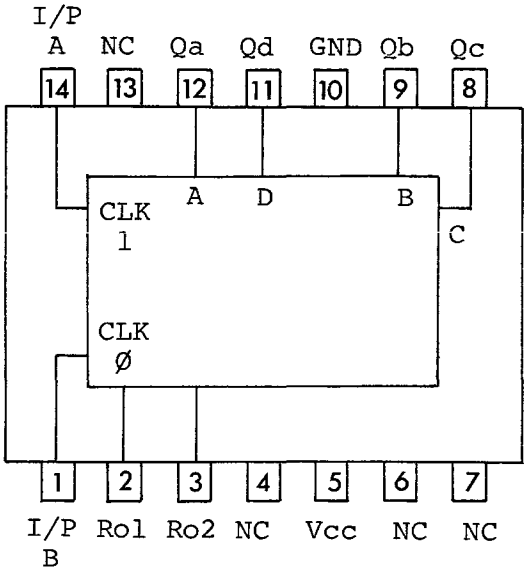
Counts the H to L transitions at I/P A. With the B I/P connected to Qa the count is:

FUNCTION TABLE

RESET INPUTS		OUTPUTS			
Ro1	Ro2	Qd	Qc	Qb	Qa
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

	OUTPUTS			
COUNT	Qd	Qc	Qb	Qa
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

7493



19-09054

4-Bit
Binary
Counter

Counts H to L transitions at I/P A. With B I/P connected to Qa the count is:

COUNT	OUTPUT			
	Qd	Qc	Qb	Qa
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

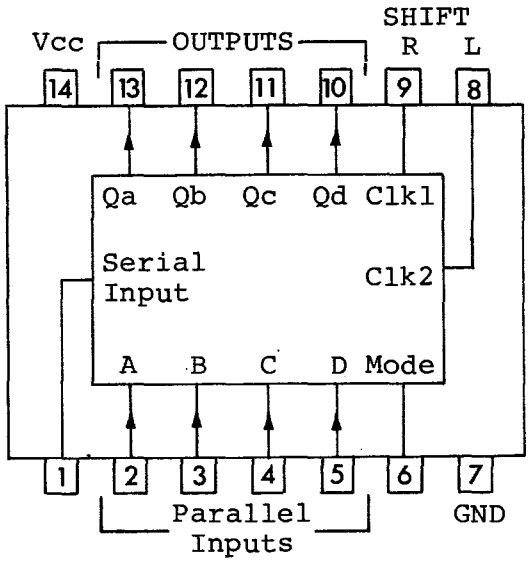
FUNCTION TABLE

RESET INPUTS		OUTPUT			
Rol	Ro2	Qd	Qc	Qb	Qa
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

7495

19-09055

4-bit
Parallel
Access
Shift
Register



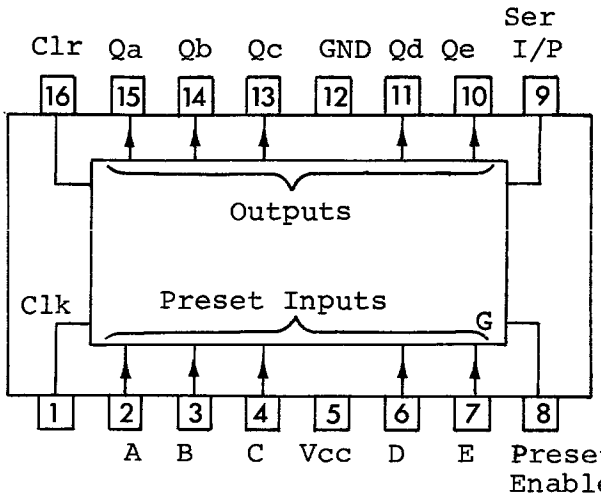
Parallel Load: Data at the parallel inputs is loaded, with mode H, and appears at the outputs after ↓ of clock 2.

Shift Right: Occurs on ↓ of clock 1 with mode L. Moves data one bit along register and loads the serial input level to stage A for every clock pulse.

Shift Left: Occurs on ↓ of clock 2 with Mode H but requires outputs to be connected to inputs of previous stages.

7496

19-10363

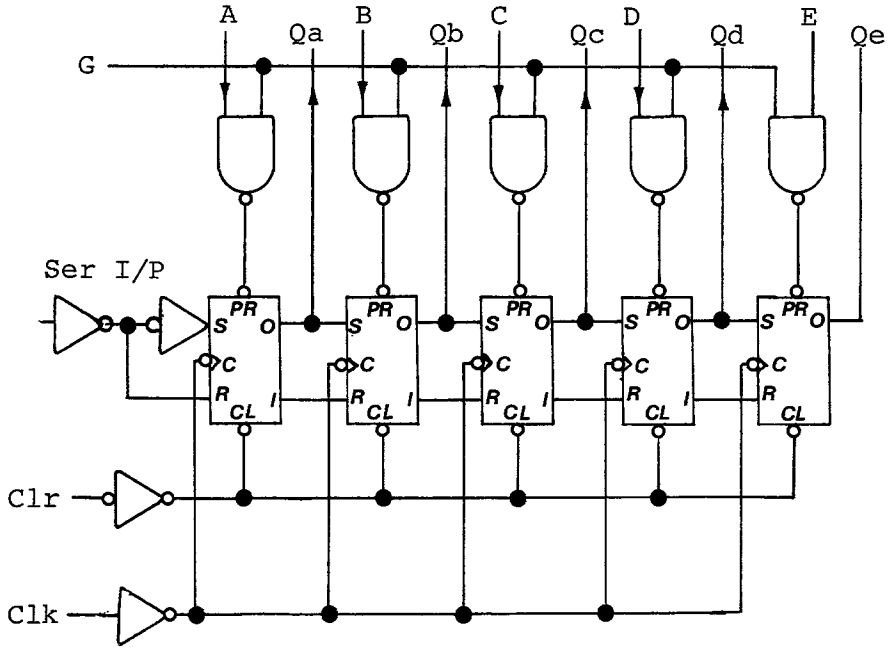


5-bit Shift Register

All five flip-flops in the register can be cleared by applying L to clear with preset enable or preset inputs L.

Paralled loading is accomplished by applying data to the preset inputs and pulsing PRESET ENABLE H.

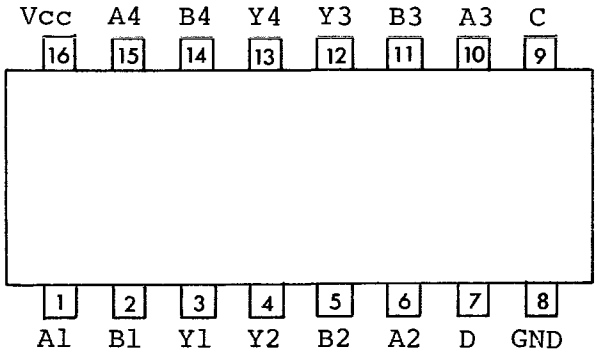
With CLEAR H and PRESET ENABLE L the data is right shifted 1 bit per clock ↑ and data at serial input is entered at stage A.

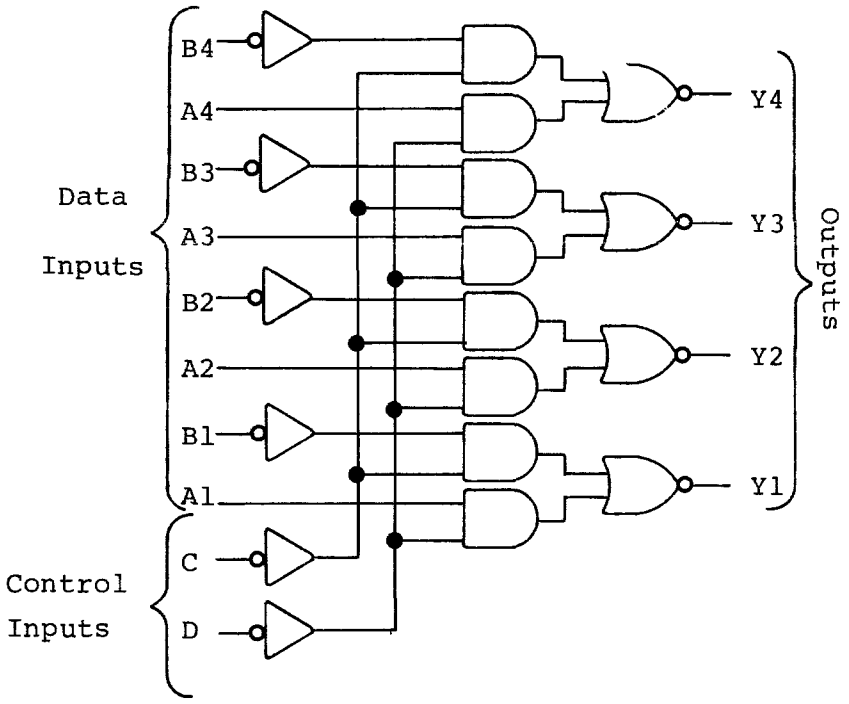


8235

19-09935

4-bit
2 Input
Multiplexer

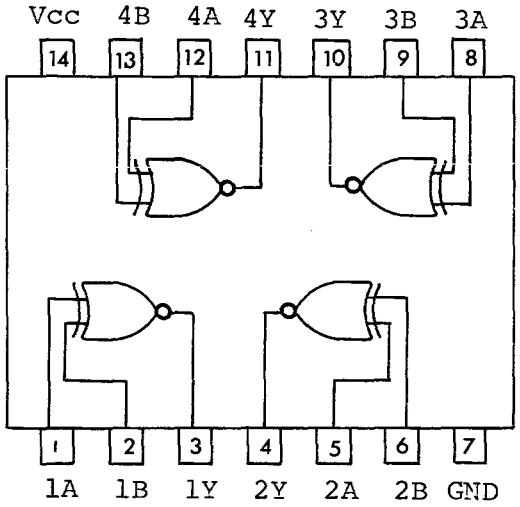




Open
Collector
Outputs.

CONTROL INPUT		DATA INPUT		OUTPUT
C	D	An	Bn	Yn
L	L	L	L	L
		L	H	H
		H	L	L
		H	H	L
L	H	-	-	Bn
H	L	-	-	$\overline{An}$
H	H	-	-	H

8242

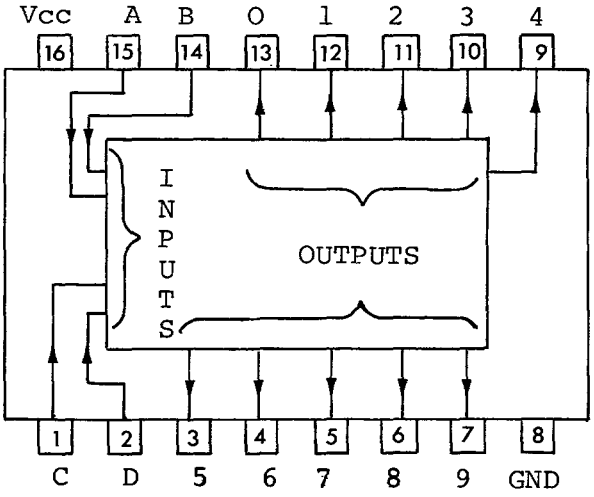


19-09712

Quad
2 Input
EX-NOR

Open collector outputs are provided to permit tying for multi-bit comparisons.

8251



19-09594

BCD
to Decimal
Decoder

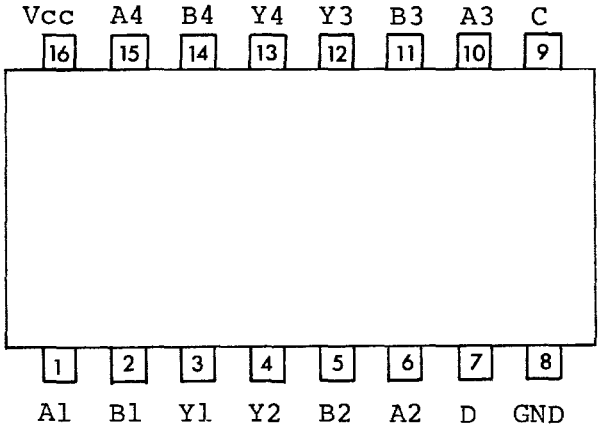
Continued Overleaf

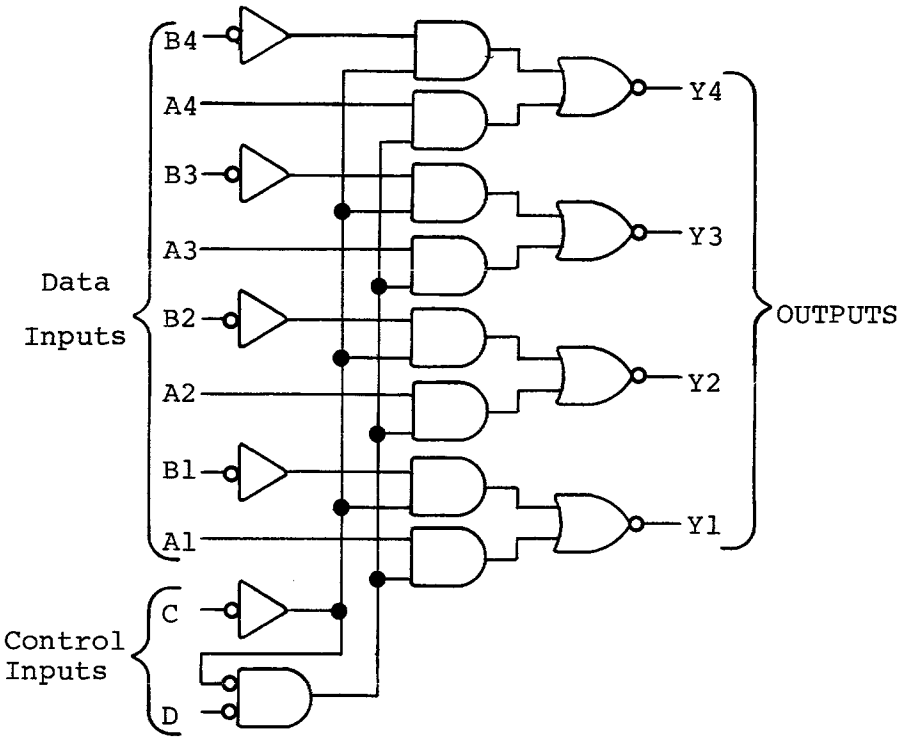
INPUTS				OUTPUTS									
D	C	B	A	O	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	X	X
H	L	H	H	H	H	H	H	H	H	H	H	X	X
H	H	L	L	H	H	H	H	H	H	H	H	X	X
H	H	L	H	H	H	H	H	H	H	H	H	X	X
H	H	H	L	H	H	H	H	H	H	H	H	X	X
H	H	H	H	H	H	H	H	H	H	H	H	X	X

8266

19-09934

Quad
2-line
to 1-line
Selector



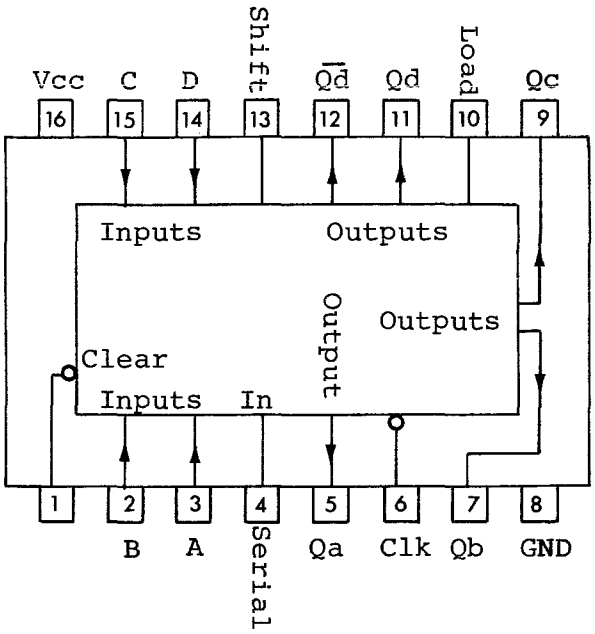


CONTROL INPUT		OUTPUT
C	D	Yn
L	L	Bn
L	H	Bn
H	L	$\overline{An}$
H	H	H

8271

19-09615

4-bit
Parallel
Access
Shift
Register



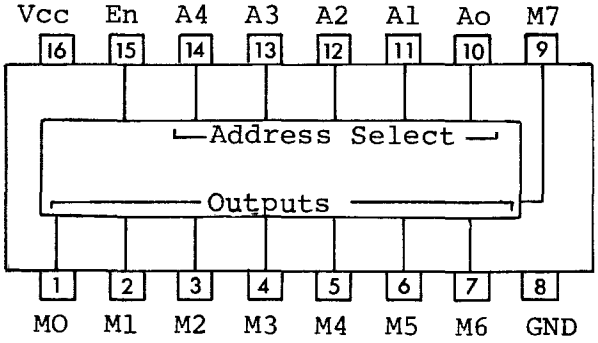
CONTROL SIGNAL		REGISTER FUNCTION
LOAD	SHIFT	
L	L	Hold
H	L	Parallel Load
L	H	Shift * Right
H	H	

* + Serial Input into Stage A.

8598

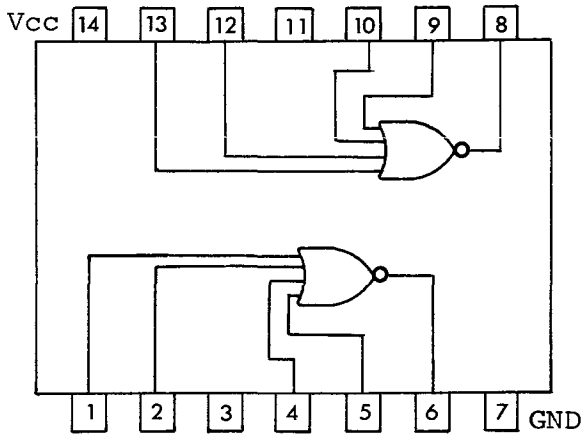
23-000A1-02

32 x 8-Bit
R.O.M.



Required address set on select lines.
Data at output when En. low.

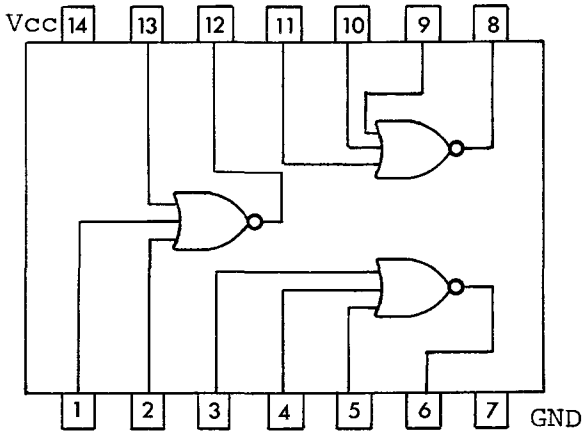
8815



19-09713

Dual
4-Input
NOR Gate

8875



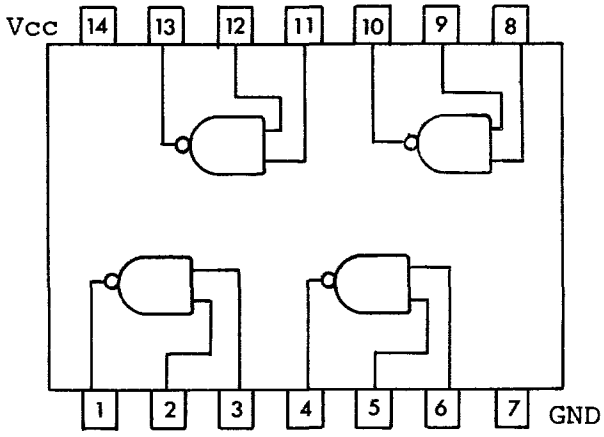
19-10647

Triple
3-Input
NOR Gate

Same function as 7427 but circuitry and characteristics different.

8881

19-09705



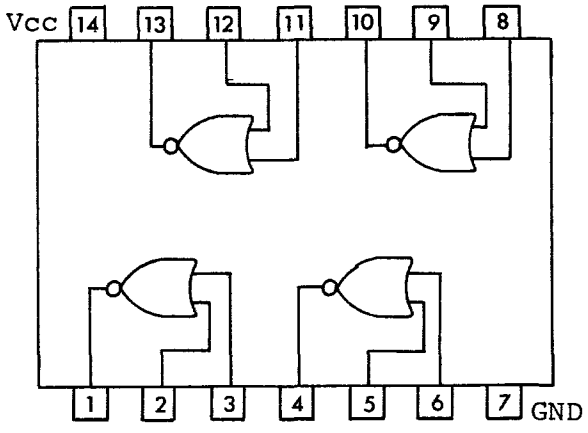
Quad
2-Input
NAND Gate

Open collector outputs.

Same function as 7401 but different circuitry and characteristics allow it to handle greater currents. This makes the device suitable for use as a Unibus Driver.

8885

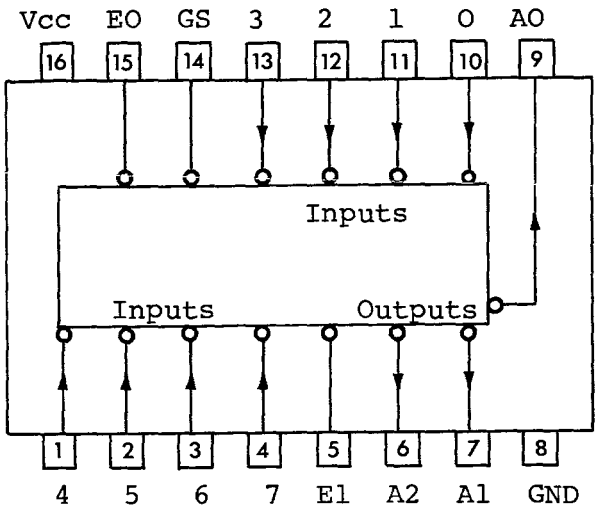
19-10649



Quad
2-Input
NOR Gate

Same function as 7402 but circuitry and characteristics different.

9318



19-10454

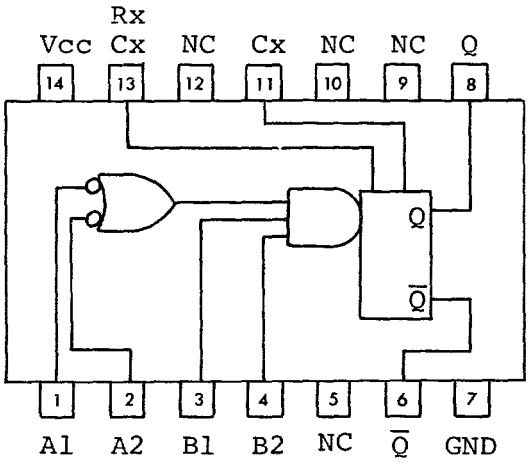
8-Input
Priority
Encoder

E1	0	1	2	3	4	5	6	7	GS	Ao	A1	A2	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

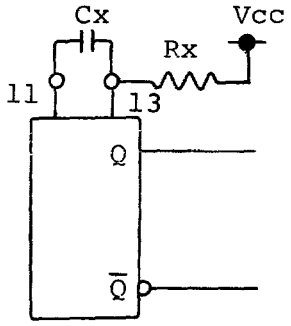
The 9318 accepts data from 8 active low inputs and provides a binary representation on the 3 active low outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line 7 having the highest priority. A high on the input enable (E1) will force all outputs to the inactive state and allow new data to settle without producing erroneous information at the outputs. A group signal output (GS) and an enable output (EO) are provided with the three data outputs. The GS is active level low when all inputs are high. Using the output enable along with the input enable allows priority encoding of N input signals. Both EO and GS are inactive high when the input enable is high.

9601

19-09373



Monostable Multi-vibrator



Duration of the output pulse is a function of the external timing components which must be connected thus:-

The input gating allows leading or trailing edge triggering:-

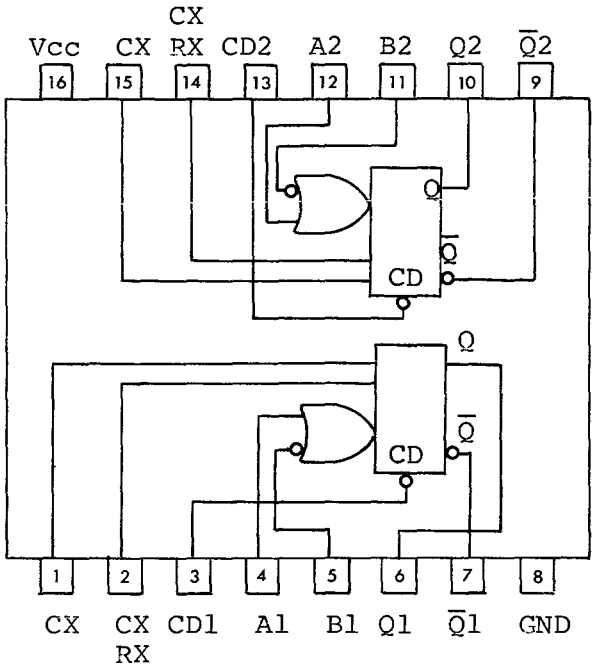
The device is retriggerable: the application of a further trigger pulse before the delay times-out will cause the output pulse to extend its duration.

Retriggering can be prevented by tying the $\overline{Q}$ output to an active Low.

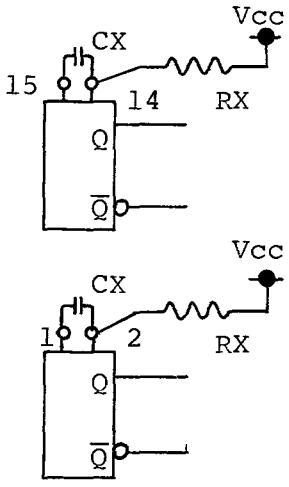
INPUTS				OUTPUTS	
A1	A2	B1	B2	Q	$\overline{Q}$
H	H	X	X	L	H
↓	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	↑	H	⎍	⎎
L	X	H	↑	⎍	⎎
X	L	H	H	L	H
X	L	↑	H	⎍	⎎
X	L	H	↑	⎍	⎎
H	↓	H	H	⎍	⎎
↓	↓	H	H	⎍	⎎
↓	H	H	H	⎍	⎎

9602

19-10951



Dual Monostable Multi-vibrator



The duration of the output pulse for each monostable is set by the associated timing components:

The output pulse can be terminated before its normal width by taking the CD input (Reset) Low.

INPUTS			OUTPUTS	
A	B	CD	Q	Q̄
L	↑	H	⎍	⎎
↑	H	H	⎍	⎎
X	X	L	RESETS	

The input gating allows leading or trailing edge triggering:-

The device like the 9601 is retriggerable. This facility can be overidden by taking Q̄ to an active L (or Q to a high).

11380

See 380.

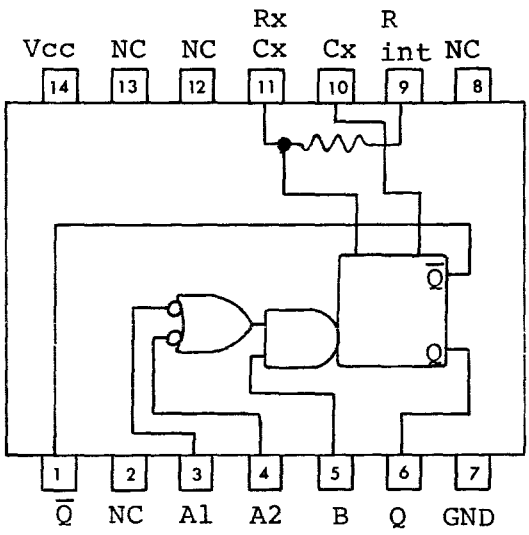
19-11113

A version of the 380 but with different circuitry and characteristics.

74121

19-10230

Monostable Multi-vibrator



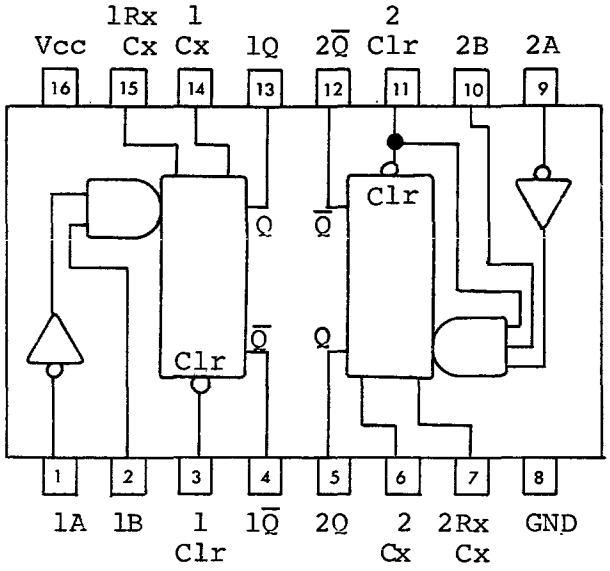
An internal timing resistor is provided. The timing capacitor is connected between pins 11 and 10.

The input coding allows leading or trailing edge triggering:-

INPUTS			OUTPUTS	
A1	A2	B	Q	$\bar{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎎
↓	H	H	⎍	⎎
↓	↓	H	⎍	⎎
L	X	↑	⎍	⎎
X	L	↑	⎍	⎎

74123

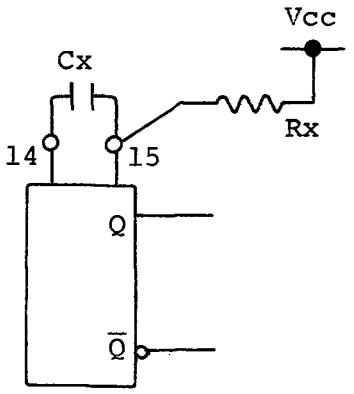
19-10436

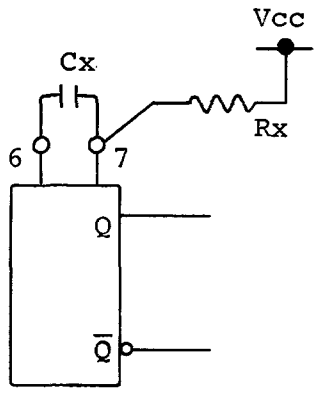


Dual
Retriggerable
Monostable
Multivibrator

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

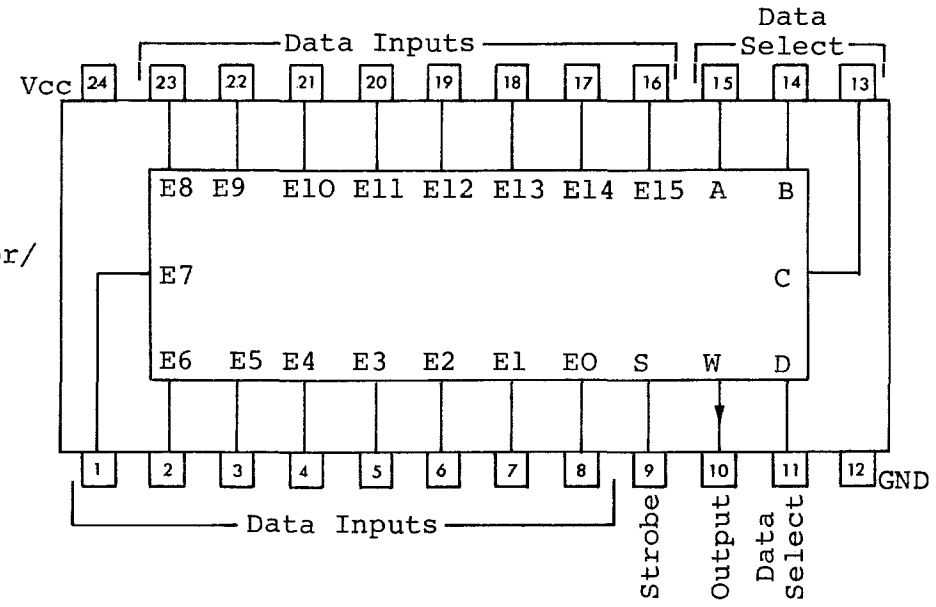
The input gating allows leading or trailing edge triggering. The device is retriggerable: by applying a further trigger pulse during the output pulse its duration can be extended. The clear input allows any output pulse to be terminated independently of the timing components, Rx and Cx, which are connected thus:-





74150

19-10153



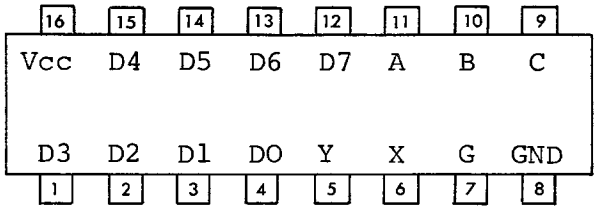
16 - 1 Data Selector/ Mux.

Selects one of 16 data sources.

The internal logic is similar in form to that shown for the 74151.

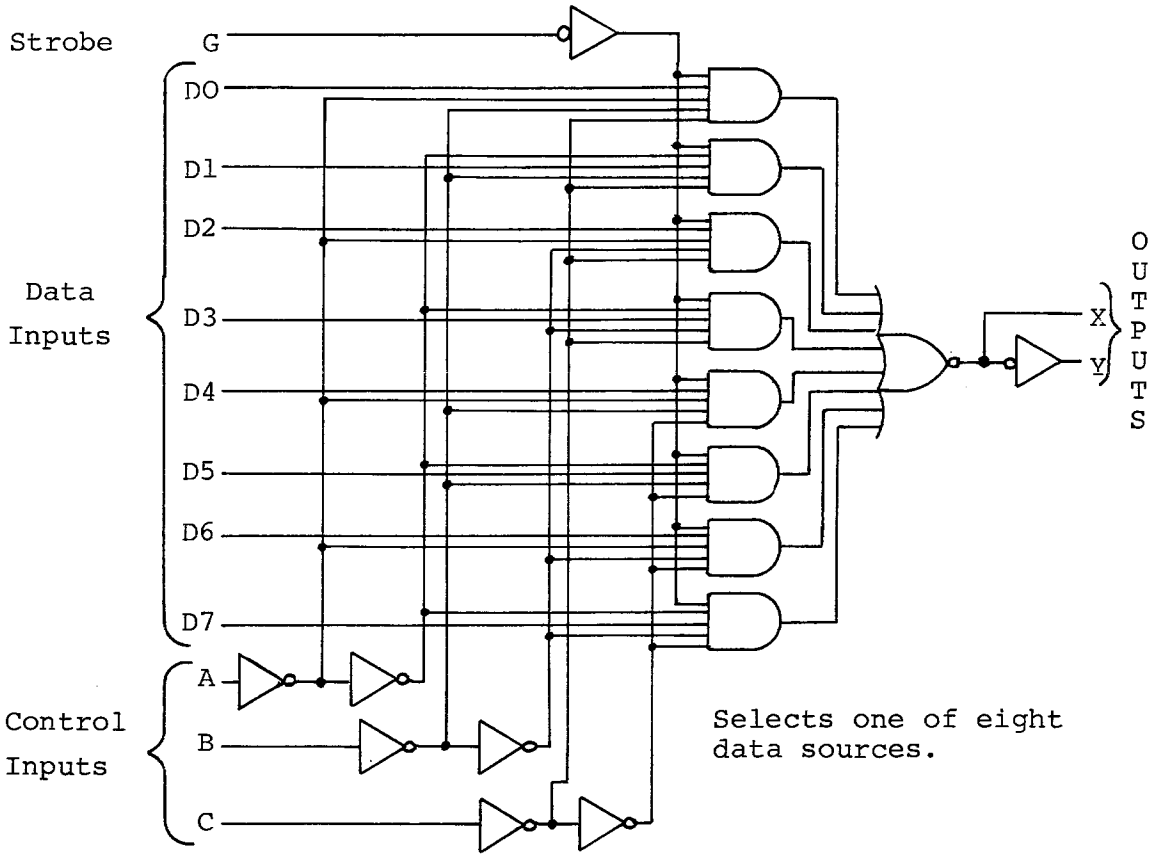
INPUTS					OUTPUT
SELECT				STROBE	
D	C	B	A	S	W
X	X	X	X	H	H
L	L	L	L	L	$\overline{E0}$
L	L	L	H	L	$\overline{E1}$
L	L	H	L	L	$\overline{E2}$
L	L	H	H	L	$\overline{E3}$
L	H	L	L	L	$\overline{E4}$
L	H	L	H	L	$\overline{E5}$
L	H	H	L	L	$\overline{E6}$
L	H	H	H	L	$\overline{E7}$
H	L	L	L	L	$\overline{E8}$
H	L	L	H	L	$\overline{E9}$
H	L	H	L	L	$\overline{E10}$
H	L	H	H	L	$\overline{E11}$
H	H	L	L	L	$\overline{E12}$
H	H	L	H	L	$\overline{E13}$
H	H	H	L	L	$\overline{E14}$
H	H	H	H	L	$\overline{E15}$

74151



8 - 1
Data
Selector
Mux.

19-09936



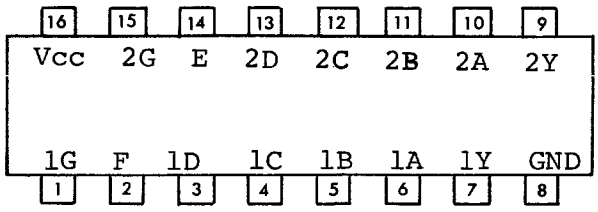
Selects one of eight data sources.

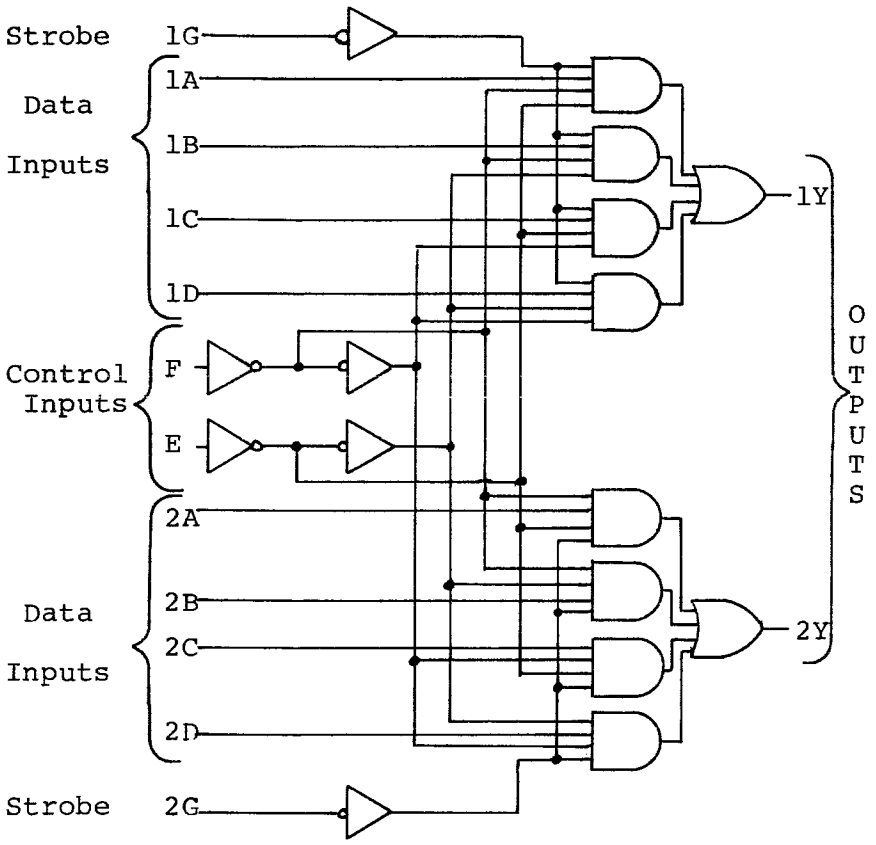
CONTROL INPUTS			STROBE	OUTPUT
A	B	C	G	X
L	L	L	L	$\bar{D0}$
H	L	L	L	$\bar{D1}$
L	H	L	L	$\bar{D2}$
H	H	L	L	$\bar{D3}$
L	L	H	L	$\bar{D4}$
H	L	H	L	$\bar{D5}$
L	H	H	L	$\bar{D6}$
H	H	H	L	$\bar{D7}$
Don't Care			H	H

74153

19-09937

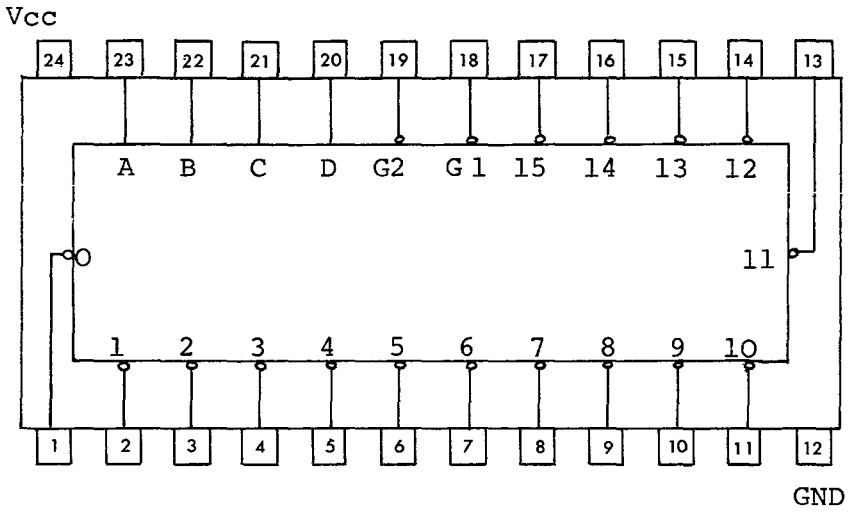
Dual
4 - 1
Data
Selector/
Mux.





CONTROL INPUT		STROBE	OUTPUT
E	F	G	Y
L	L	L	A
H	L	L	B
L	H	L	C
H	H	L	D
Don't Care		H	L

74154



19-09701

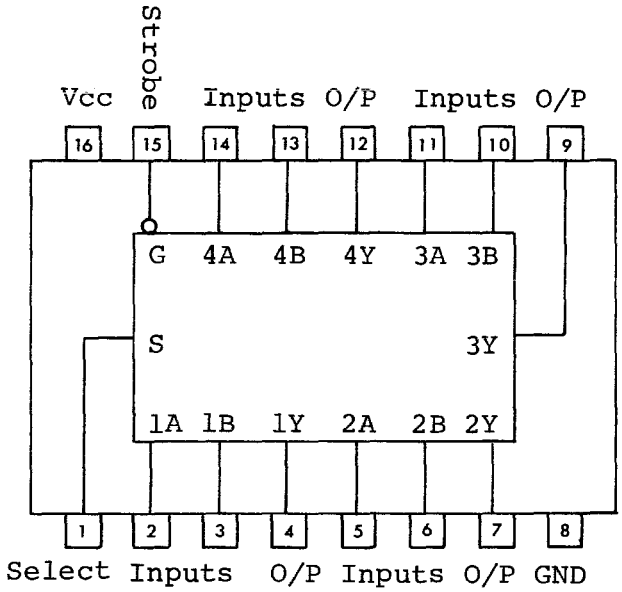
4-Line
to
16-Line
Decoder/
Mux.

INPUTS						OUTPUTS														
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

74157

19-10655

Quad
2 - 1
Data
Selector
Mux.



INPUTS				OUTPUT
STROBE	SELECT	A	B	Y
H	X	X	X	L
L	L	-	-	A
L	H	-	-	B

Strobe H sets all outputs Low. With Strobe Low, select input directs either A or B inputs to outputs.

74S158

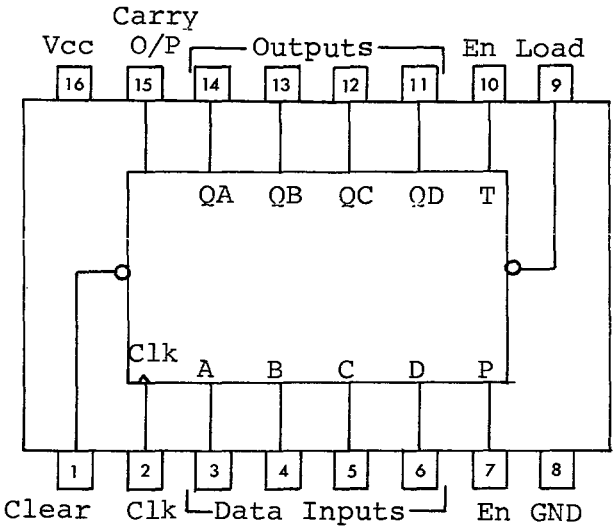
19-10549

Quad
2 - 1
Data
Selector/
Mux.

See 74157 for pin connections; but outputs inverted, thus:-

INPUTS				OUTPUT
STROBE	SELECT	A	B	Y
H	X	X	X	H
L	L	-	-	$\overline{A}$
L	H	-	-	$\overline{B}$

74161

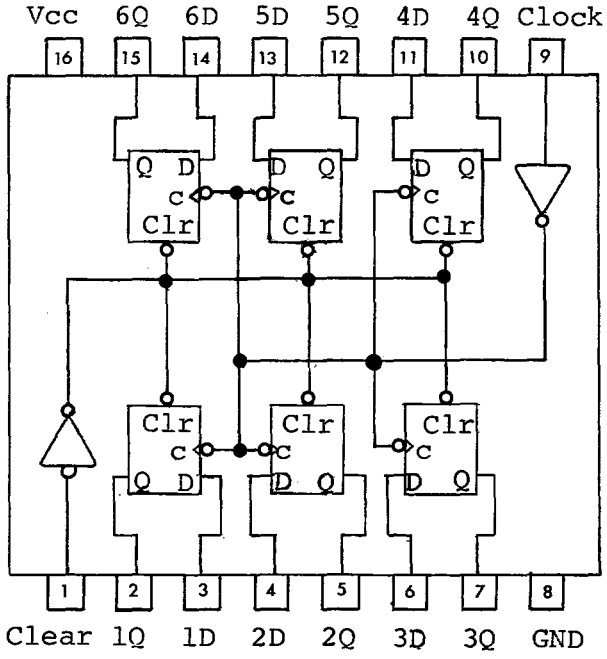


19-10650

Synchronous
4-bit
Binary
Counter

The counter is cleared by applying a Low to CLEAR. Presetting occurs when LOAD is taken Low: Information at the data input is then entered on the next clock ↑. Both count enable inputs (P and T) must be taken H to count. The carry output is used for cascading counters.

74174



19-10652

Hex
D-Type
Flip-Flop

Continued Overleaf..

74174 Continued

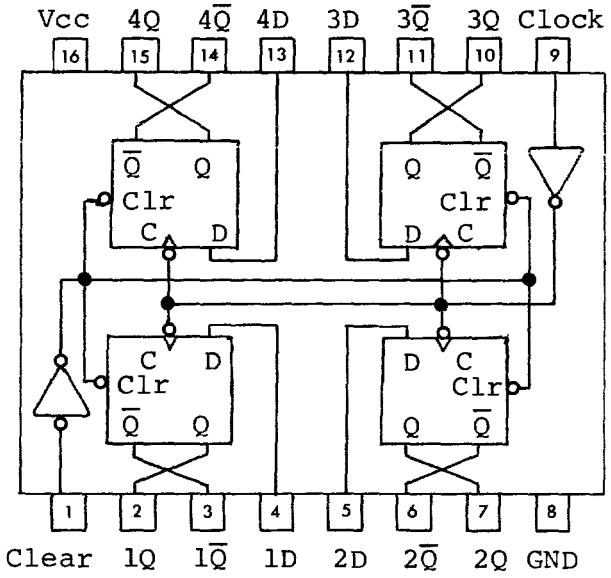
Information at the D inputs is transferred to the Q outputs on the positive-going edge of the clock pulse.

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	No Change

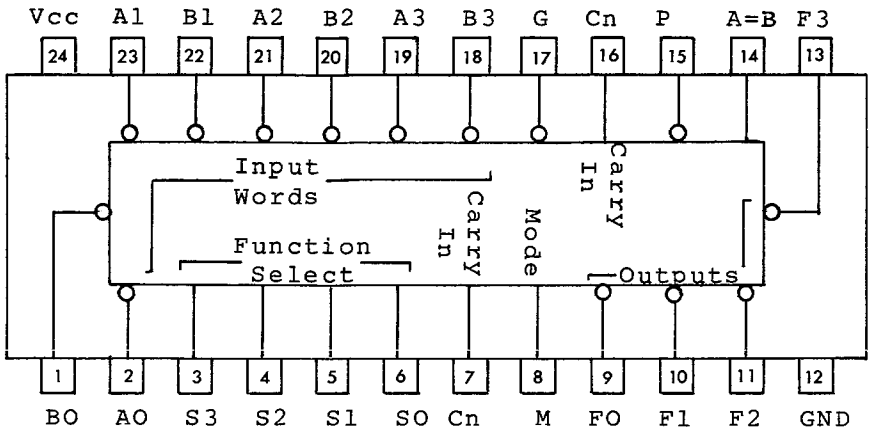
74175

19-10651

Quad
D-Type
Flip-Flop



INPUTS			OUTPUTS
CLEAR	CLOCK	D	Q Q̄
L	X	X	L H
H	↑	H	H L
H	↑	L	L H
H	L	X	No Change



74181

19-09982

Arithmetic Logic Unit

G and P = Look Ahead Carry.

The 74181 performs logic functions with Mode High, or Arithmetic functions with Mode Low. The required functions are selected at the SELECT inputs. The interpretation of the functions depends on the assertion level of the data - the alternatives are given in the following tables:-

SELECT. 3 2 1 0	DATA ASSERTED HIGH		
	M=H LOGIC FUNCTIONS	M = L; ARITHMETIC OPERATIONS	
		Cn = H	Cn = L
L L L L	$F = \overline{A}$	F = A	F = A ▶+ 1
L L L H	$F = \overline{A+B}$	F = A+B	F = (A+B) ▶+ 1
L L H L	$F = \overline{A}B$	$F = A+\overline{B}$	$F = (A+\overline{B})$ ▶+ 1
L L H H	F = 0	F = -1 (2COMP)	F = ZERO
L H L L	$F = \overline{AB}$	$F = A$ ▶+ $A\overline{B}$	$F = A$ ▶+ $A\overline{B}$ ▶+ 1
L H L H	$F = \overline{B}$	$F = (A+B)$ ▶+ $A\overline{B}$	$F = (A+B)$ ▶+ $A\overline{B}$ ▶+ 1
L H H L	$F = A \oplus B$	F = A - B - 1	F = A - B
L H H H	$F = A\overline{B}$	$F = A\overline{B}$ - 1	$F = A\overline{B}$
H L L L	$F = \overline{A} + B$	F = A ▶+ AB	F = A ▶+ AB ▶+ 1
H L L H	$F = \overline{A \oplus B}$	F = A ▶+ B	F = A ▶+ B ▶+ 1
H L H L	F = B	$F = (A+\overline{B})$ ▶+ AB	$F = (A+\overline{B})$ ▶+ AB ▶+ 1
H L H H	F = AB	F = AB - 1	F = AB
H H L L	F = 1	F = A ▶+ A*	F = A ▶+ A ▶+ 1
H H L H	$F = A + \overline{B}$	F = (A+B) ▶+ A	F = (A+B) ▶+ A ▶+ 1
H H H L	F = A + B	$F = (A+\overline{B})$ ▶+ A	$F = (A+\overline{B})$ ▶+ A ▶+ 1
H H H H	F = A	F = A - 1	F = A

* Each bit is shifted to the next more significant position.

+ = OR ⊕ = EX OR ▶+ = Arithmetic Plus (Add)

Continued Overleaf..

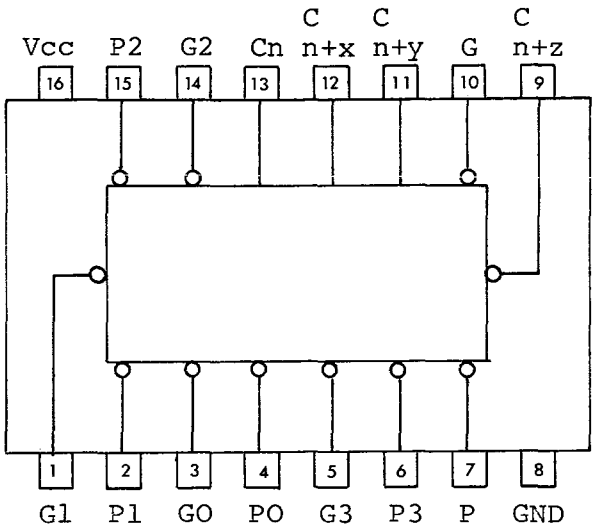
74181 continued.

SELECT. 3 2 1 0	DATA ASSERTED LOW: M=H LOGIC FUNCTIONS	M=L; ARITHMETIC OPERATIONS: Cn = L	Cn = H
L L L L	$F = \overline{A}$	F = A - 1	F = A
L L L H	$F = \overline{AB}$	F = AB - 1	F = AB
L L H L	$F = \overline{A} + B$	$F = A\overline{B} - 1$	$F = A\overline{B}$
L L H H	F = 1	F = -1 (2COMP)	F = ZERO
L H L L	$F = \overline{A + B}$	$F = A \blacktriangleright\!\!+ (A+\overline{B})$	$F = A \blacktriangleright\!\!+ (A+\overline{B}) \blacktriangleright\!\!+ 1$
L H L H	$F = \overline{B}$	$F = AB \blacktriangleright\!\!+ (A+\overline{B})$	$F = AB \blacktriangleright\!\!+ (A+\overline{B}) \blacktriangleright\!\!+ 1$
L H H L	$F = \overline{A \oplus B}$	F = A - B - 1	F = A - B
L H H H	$F = A + \overline{B}$	$F = A + \overline{B}$	$F = (A+\overline{B}) \blacktriangleright\!\!+ 1$
H L L L	$F = \overline{A}B$	$F = A \blacktriangleright\!\!+ (A + B)$	$F = A \blacktriangleright\!\!+ (A+B) \blacktriangleright\!\!+ 1$
H L L H	$F = A \oplus B$	$F = A \blacktriangleright\!\!+ B$	$F = A \blacktriangleright\!\!+ B \blacktriangleright\!\!+ 1$
H L H L	F = B	$F = A\overline{B} \blacktriangleright\!\!+ (A+B)$	$F = A\overline{B} \blacktriangleright\!\!+ (A+B) \blacktriangleright\!\!+ 1$
H L H H	F = A + B	F = A + B	$F = (A+B) \blacktriangleright\!\!+ 1$
H H L L	F = O	$F = A \blacktriangleright\!\!+ A^*$	$F = A \blacktriangleright\!\!+ A \blacktriangleright\!\!+ 1$
H H L H	$F = A\overline{B}$	$F = AB \blacktriangleright\!\!+ A$	$F = AB \blacktriangleright\!\!+ A \blacktriangleright\!\!+ 1$
H H H L	F = AB	$F = A\overline{B} \blacktriangleright\!\!+ A$	$F = A\overline{B} \blacktriangleright\!\!+ A \blacktriangleright\!\!+ 1$
H H H H	F = A	F = A	F = A + 1

* Each bit is shifted to the next more significant position.

The device functions as a comparator in the subtract mode (F = A minus B) with Cn High. When the input words are equal A = B is High.

74182



19-10019

Look-Ahead Carry Generator

Used in conjunction with adders or A.L.U's. in arithmetic operations to anticipate the carry inputs and thus increase the speed greatly.

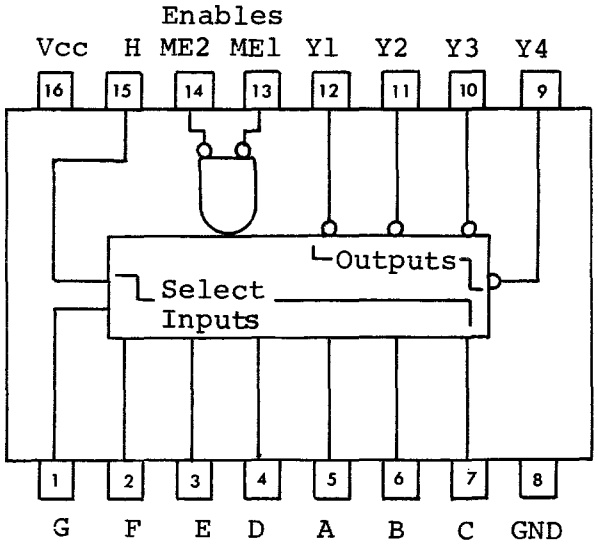
DESIGNATION	FUNCTION
GO, G1, G2, G3	Carry Generate Inputs Active-Low
PO, P1, P2, P3	Carry Generate Inputs Active-Low
Cn	Carry Input
Cn+x, Cn+y, Cn+z	Carry Outputs
G	Carry Generate Output Active-Low
P	Carry Propagate Output Active-Low

The SN74182 is a high-speed, look-ahead carry generator capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propogate-carry functions are provided.

74187

23-000A2-01

256 Word
4-bit
Read Only
Memory



Data is entered by the manufacturer and cannot be changed. Open collector outputs.

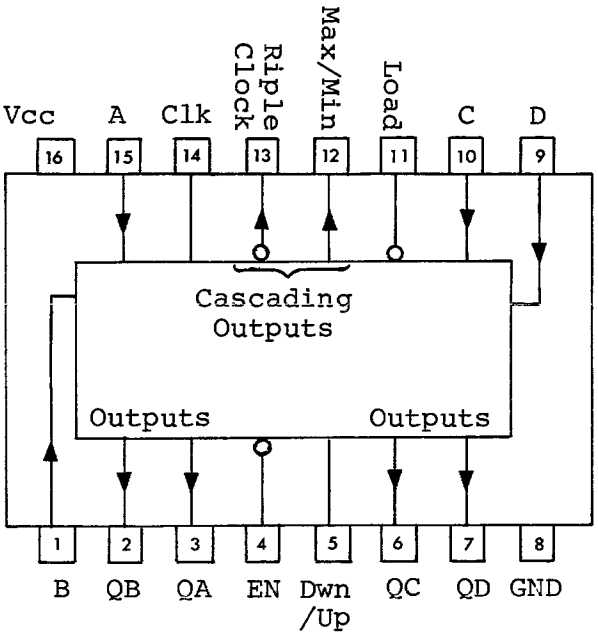
Word selection is in 8-bit binary:

WORD	H	G	F	E	D	C	B	A
0	L	L	L	L	L	L	L	L
1	L	L	L	L	L	L	L	H
2	L	L	L	L	L	L	H	L
-								
-								
-								
254	H	H	H	H	H	H	H	L
255	H	H	H	H	H	H	H	H

When either or both of the ENABLE inputs is taken High the memory is inhibited and all four outputs go High.

74191

19-10096



4-bit
Binary
Synchronous
Up-Down
Counter

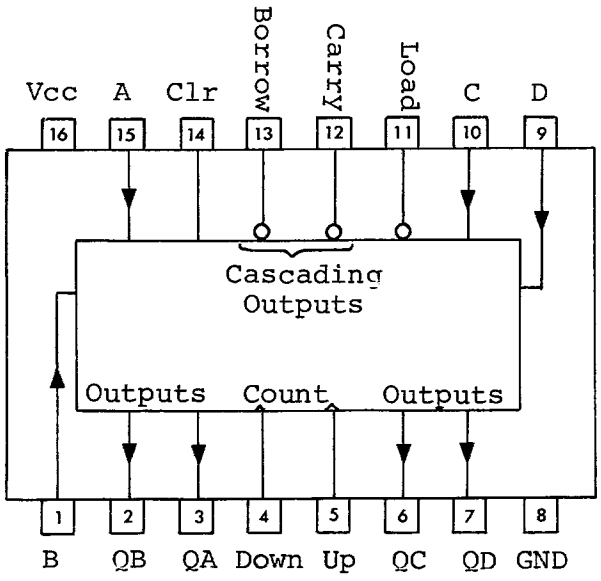
A, B, C, D = Parallel Inputs

The counter counts 1 for each clock ↑ when En is Low. If Down/Up is Low the counter counts up - if High it counts down.

The counter may be preset by setting the required data at the parallel inputs. The outputs will assume these levels when LOAD is taken Low.

74193

19-10018



4-Bit
Binary
Synchronous
Up-Down
Counter

A, B, C, D, = Inputs

Continued Overleaf..

The counter counts the L to H transitions of the Count (Clock) inputs. The direction of counting is determined by which COUNT input is pulsed while the other is held High.

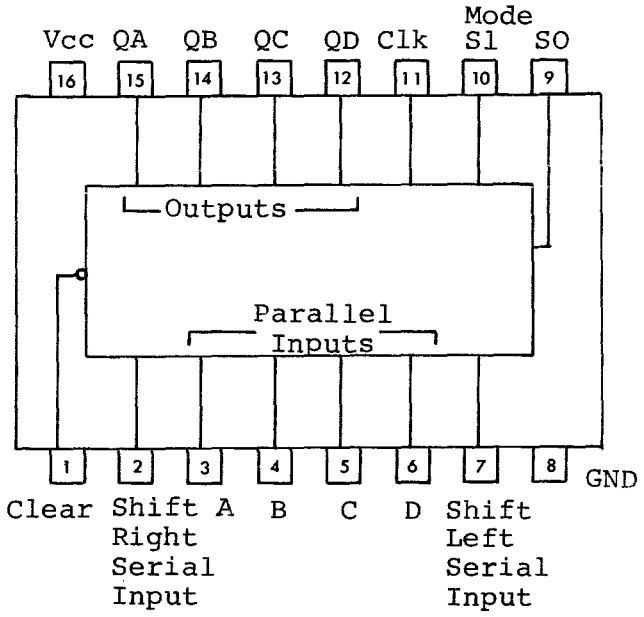
When a High is applied to CLEAR all four outputs are forced Low.

The counter may be preset by setting the required data at the parallel inputs. The outputs will assume these levels when LOAD is taken Low.

74194

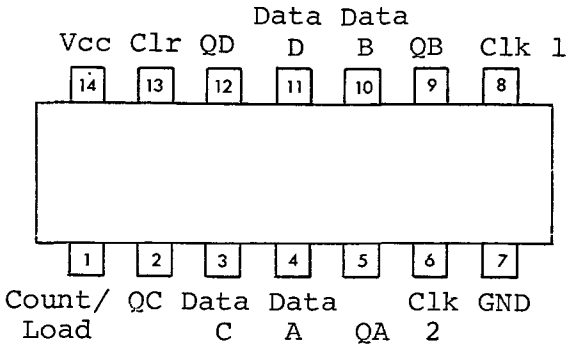
19-10623

4-Bit
Bidirectional
Shift
Register



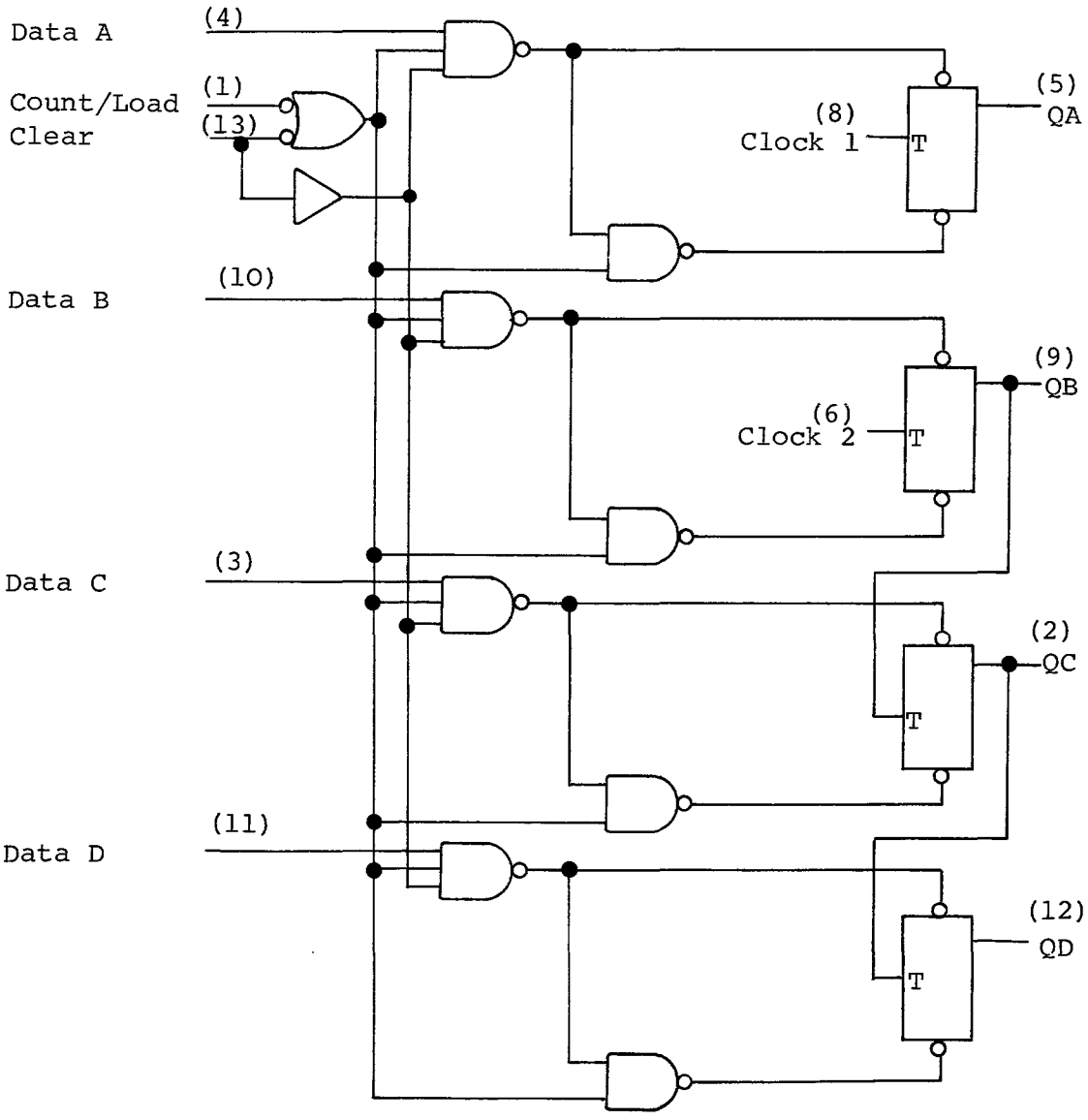
INPUTS				OUTPUTS
CLEAR	SØ	S1	CLOCK	Qa Qb Qc Qd
L	X	X	X	L L L L
H	X	X	L	No Change
H	H	H	↑	Parallel Load
H	L	H	↑	Shift Right + Right Serial Input to Qa
H	H	L	↑	Shift Left + Left Serial Input to Qd
H	L	L	X	No Change

74197



19-10035

Binary Counter/ Latch



Continued Overleaf..

Divide by 2 operation. Input at clock 1: Output at Qa.

Divide by 8. Input at clock 2: Output at Qd.

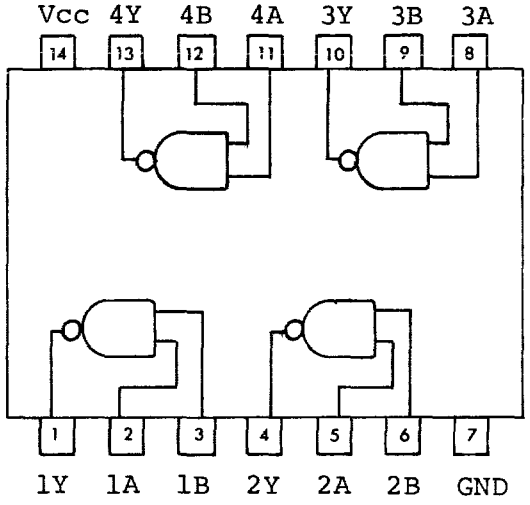
Binary Counter; Qa must be connected to CLOCK 2. The counter can be preset by setting the required starting value on the data inputs and a Low on COUNT/LOAD. (This is also known at latch operation).

The CLEAR input overrides the clock inputs and sets the outputs Low.

97401

19-09973

Quad
2-Input
NAND Gate



Low output leakage current. Open collectors.

NOTES

7

SAFETY

This chapter is intended as a supplement to existing safety information and instructions at the plant.

SAFETY

The computer technician is not exposed to many hazards. The commonest concern the ***EYES.***

(a) Solvent Splashes

When applying solvents with a brush, make sure the hairs "flick" away from you. Do not inhale solvent fumes.

(b) Wire Clippings

The wedge action of side cutters can send a clipping a long way with surprising accuracy. Make sure the firing line is downwards and below eye level.

(c) Solder

Once in a while a conductor under tension can flick a speck of molten solder.

The ***FORK LIFT TRUCK*** is one of the finest generators of accidents in industry. When it's around, be ***CAREFUL.***

This leaves the risk of ***ELECTRIC SHOCK*** - considered to be slight in our environment, and for that reason it gets forgotten entirely, with the result that every now and again somebody finds himself acting as a conductor.

The following paragraphs explain the exact nature of the hazard. The flow-chart shows how to help the victim of an electrical accident.

ELECTRIC SHOCK

Death by electric shock is a consequence of current passing through the body. The actual cause of death can be any of, or a combination of:

(a) Heart Damage

The normal action of the heart is that of a pump activated by electric pulses. A pulse from the brain contracts the muscle around the lower heart chambers moving blood into the upper chambers. While this is going on the pulse is moving up a delay line of nervous material called the BUNDLE OF HISS. When it emerges it contracts the muscle around the upper chambers and the blood, with valves behind it closed by pressure, exits via a large artery called the Aorta. The point here is not the technical economy of having one pulse do the work of two, but that the whole thing is electronic and cannot be expected to function again after receiving a sizeable fraction of mains power.

(b) Cessation of Breathing

The nervous system controlling our breathing does not take kindly to mains power. In fact, it stops working - but this stoppage is usually temporary.

(c) Burns

Large amounts of power passing through the body will produce charring at the high resistance points. Death from extensive burns usually results from the body retiring into secondary shock (a different sort of shock) but we rarely encounter power in such quantities in our environment.

The effect electricity has on the human body is governed by several factors:

(a) Frequency

DC and low frequency A.C. are the worst.

(b) Current

Table 1

1 - 10 mA	perceptible
10 - 20 mA	painful contractions
20 - 100 mA	via chest interrupts breathing
100 - 200 mA	via heart causes permanent damage
200 mA +	Burns

(c) Path Through Body

Hand to hand or hand to foot - both involve the chest; i.e. breathing and heart.

The magnitude of the current passing through the body is governed by a well known expression $I = {}^{E}/_{R}$

E is a function of whichever generator the victim is connected to.

R is a function of skin resistance at the entry and exit points. (What goes on in between these points is wet meat, pipes containing fluids, and nerves, all of which add up to about zero ohms.) Skin resistance varies from about 500Ω when wet to 100k when dry.

We are now in a position to calculate our way through a few possible accidents.

Suppose somebody gets one hand on Mains Live while the other is clutching a metal bay frame, on a dry, cool day when his skin, moistened slightly by work, has a resistance of about 6k.

In the USA or Puerto Rico he would experience, across the chest, a current of $^{120}/_{6}$ = 20 mA. He would experience a painful contraction, which would throw him forcibly against the nearest object.

In Ireland, however, he would pass $^{220}/_{6}$ = 36.6 mA. His breathing would stop at about the same moment he hits the floor - unconscious. If his breathing were to stay in spasm for longer than 2½ minutes, he would begin to suffer brain damage, caused by oxygen starvation - maybe enough damage for the respiratory nervous system to lose interest in recovering.

And yet, prompt ARTIFICIAL RESPIRATION could have ensured his recovery.

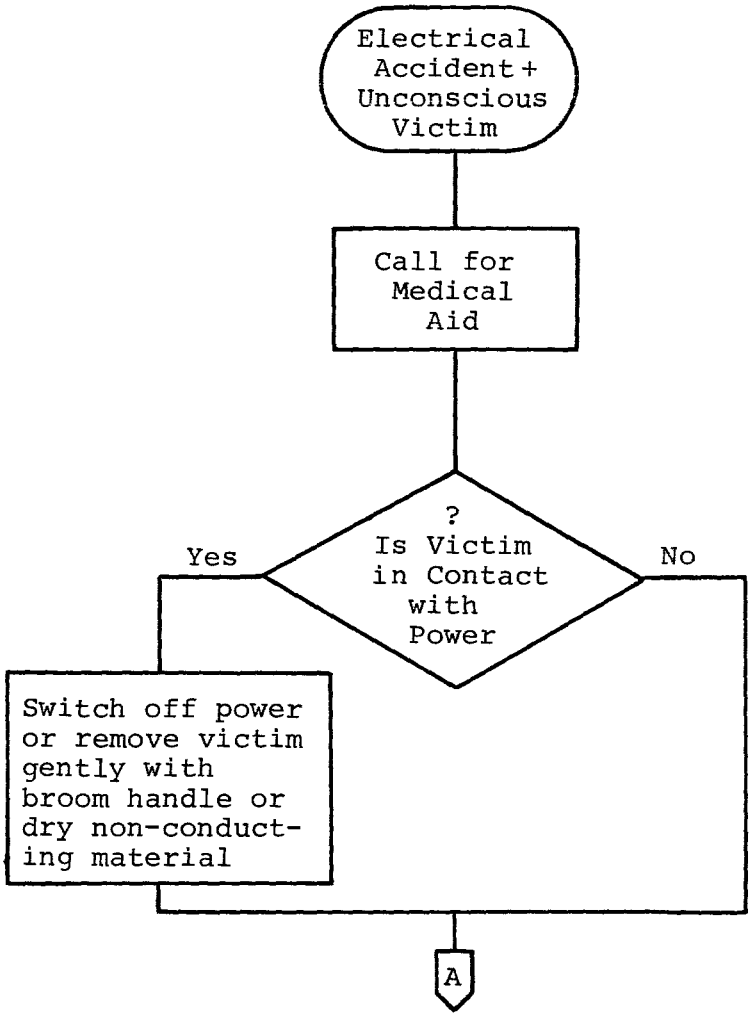
Now - imagine the same situation on a hot day after some physical exertion. The hands completing the circuit will be relatively wet - with sweat. Skin resistance of about 1.5k:

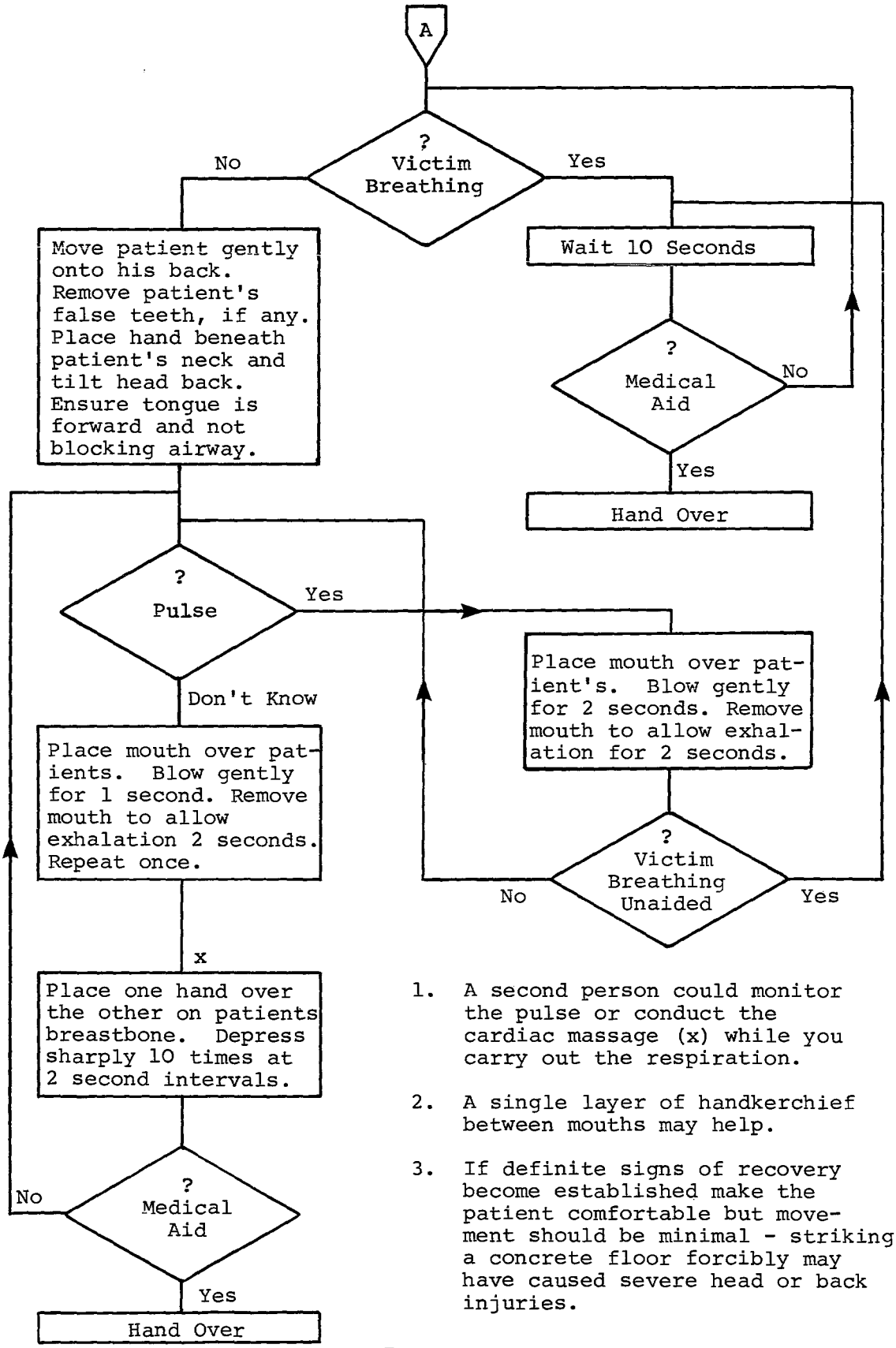
In the USA the victim will pass $^{120}/_{1.5}$ = 80 mA, and will certainly lose his respiratory action, and will get into the condition just described, only worse.

In Ireland the casualty will pass $^{220}/_{1.5}$ = 146 mA. He will probably die instantaneously from heart damage: but he may not, and who will be in a position to say that he is dead?

In both cases ARTIFICIAL RESPIRATION must be started immediately and continued until expert medical opinion says that it should stop. A casualty can have a serviceable heart and yet not regain the power of breathing for some hours. Artificial respiration can keep shock victims alive.

RESUSCITATION





1. A second person could monitor the pulse or conduct the cardiac massage (x) while you carry out the respiration.

2. A single layer of handkerchief between mouths may help.

3. If definite signs of recovery become established make the patient comfortable but movement should be minimal - striking a concrete floor forcibly may have caused severe head or back injuries.

NOTES

INFORMATION REQUEST

The Manufacturing training group plans an annual revision of the Technicians Handbook.

Your comments and suggestions will help us in our effort to improve its content and usefulness. Please take a few minutes and send us your thoughts.

1. What factual errors, if any, did you find? (Please be specific, give page numbers, etc.)
   Comments _____
   _____
   _____

2. In general, were the copy and illustrations easy to understand?
   Comments _____
   _____
   _____

3. Did you feel any important subject needed a more detailed explanation?
   Comments _____
   _____
   _____

4. Did you feel any superfluous or unnecessary information was given?
   Comments _____
   _____
   _____

5. What changes, if any, would you like to see made in the next edition?
   _____
   _____
   _____

Thank you for your help.

Your Name _____
Organization _____
Location _____
_____

Mail to:
Howard Brown
Manufacturing Training
Maynard, Mass.