

**GT40/GT42
user's guide**

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GT40/GT42 GRAPHIC DISPLAY TERMINAL

1.1 PURPOSE AND SCOPE

This guide describes the operation of the GT40 and GT42 Graphic Display Terminals. The following information is included: start-up procedures, equipment specifications, programming techniques, interfacing, and a description of the ROM Bootstrap.

1.2 GENERAL DESCRIPTION

The GT40/42 Graphic Display Terminal (Figures 1 through 5) is a high performance graphic display system that operates through a PDP-11/10 computer. The GT40/42 is designed for applications that require both a visual display and a computation capability. The system can display either alphanumeric information, graphic data such as drawings, diagrams, and patterns, or any combination of these. It is particularly valuable for displaying dynamic, fast-changing data such as waveforms. The GT40/42 can function as a general purpose computer when not performing as a display terminal. In this nondisplay mode of operation, it can operate as a stand-alone system or initiate communications with a host computer as part of a computer network.

1.3 SYSTEM ORGANIZATION

The GT40/42 consists of eight basic components organized to form the system described above. These components are:

- Central Processor Unit (CPU)
- Display Processor Unit (DPU) in which is included the Bootstrap Read Only Memory (ROM)
- Communications Interface Module
- Memory
- Keyboard
- Cathode Ray Tube (CRT) Monitor
- Light Pen
- Power Supply

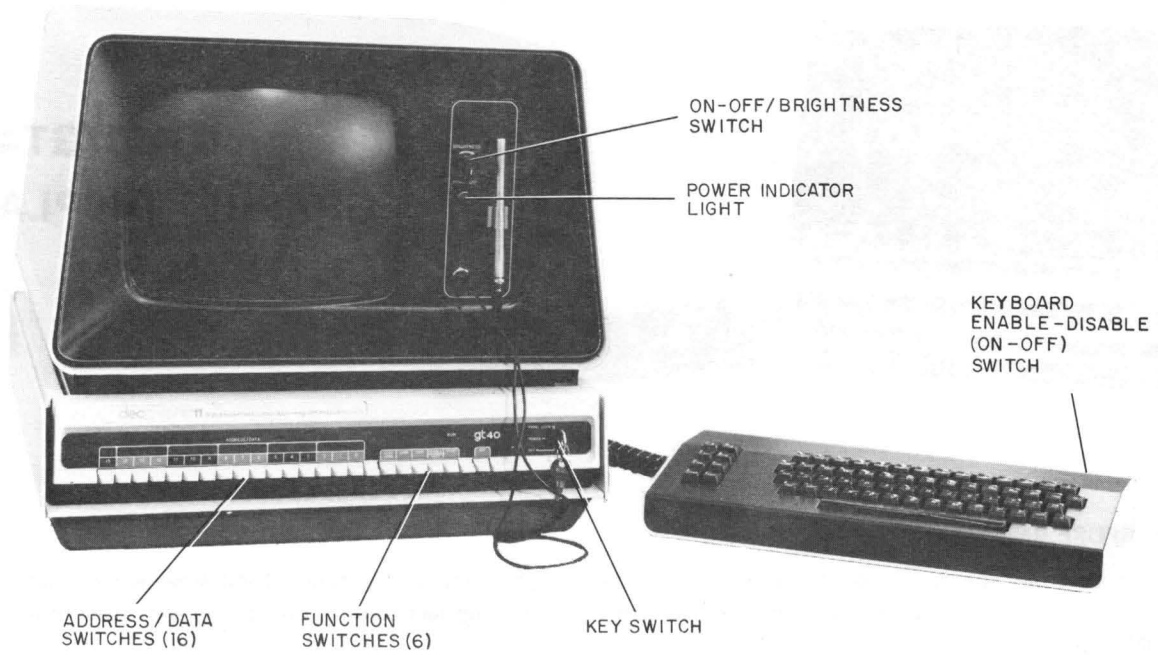


Figure 1 GT40 Graphic Display Terminal



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Figure 2 GT42 Graphic Display Terminal

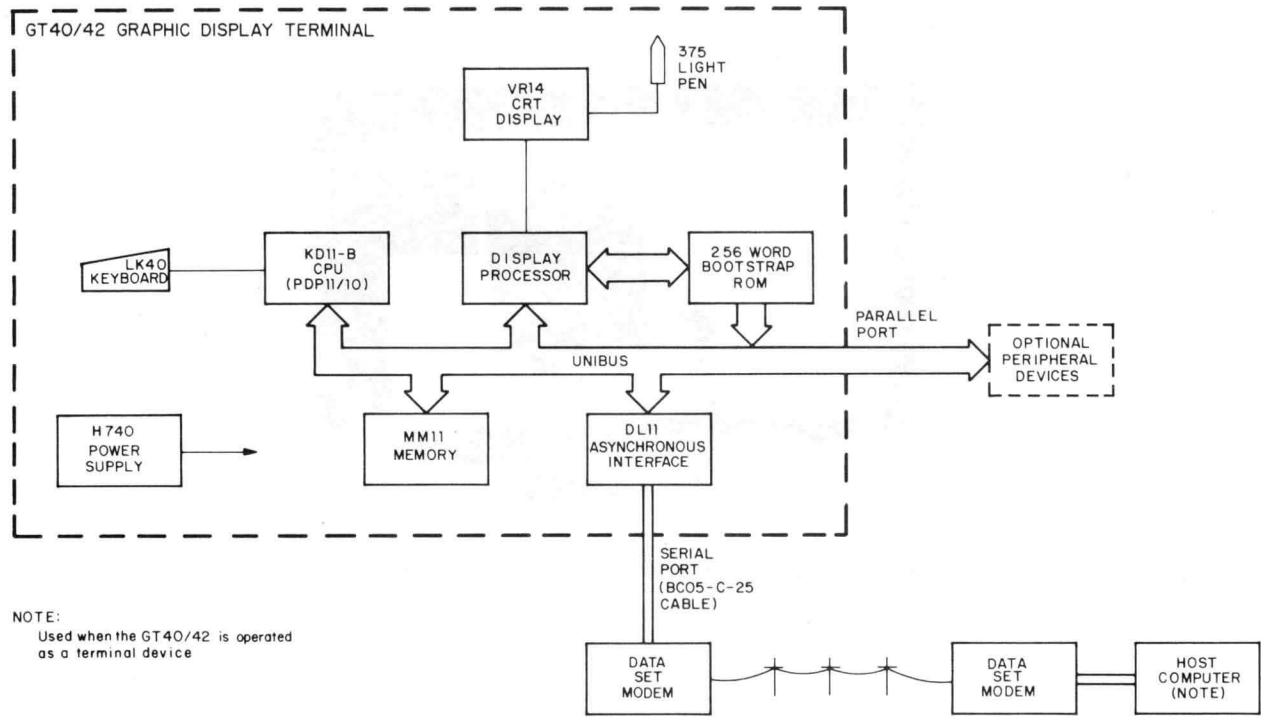


Figure 3 GT40/42 Graphic Display Terminal, Block Diagram

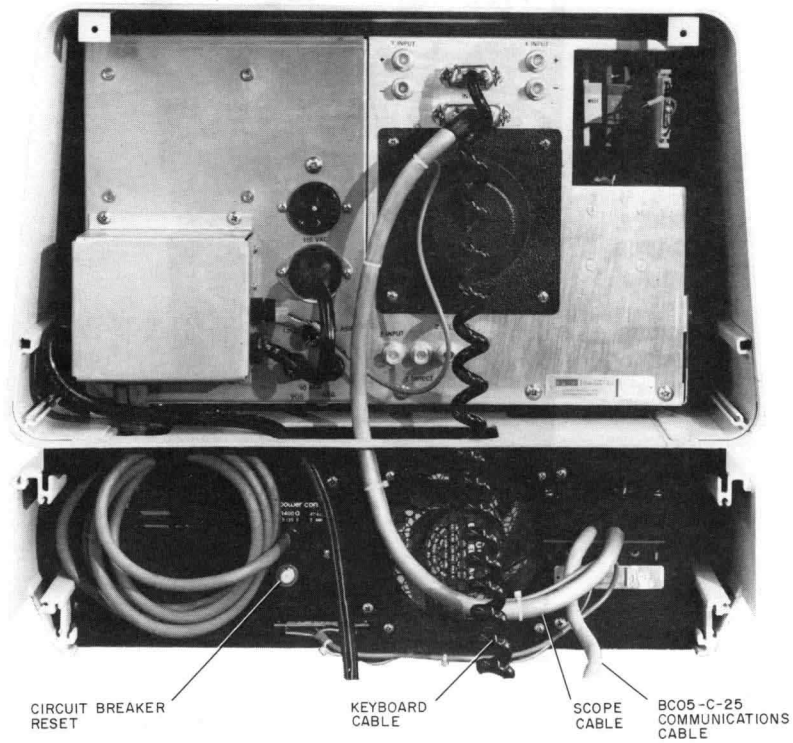
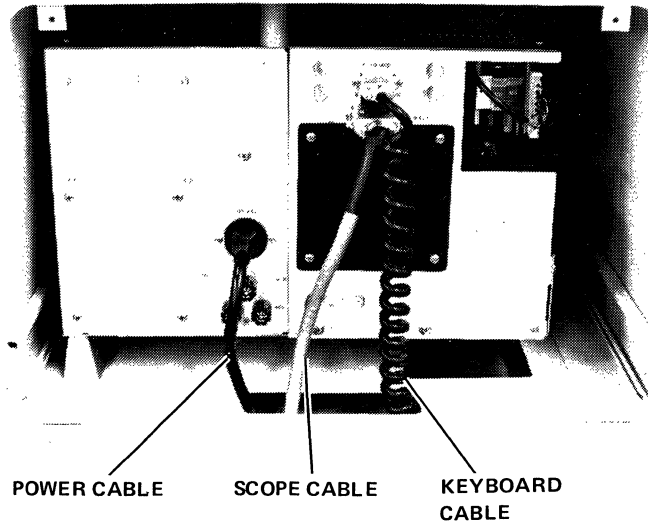
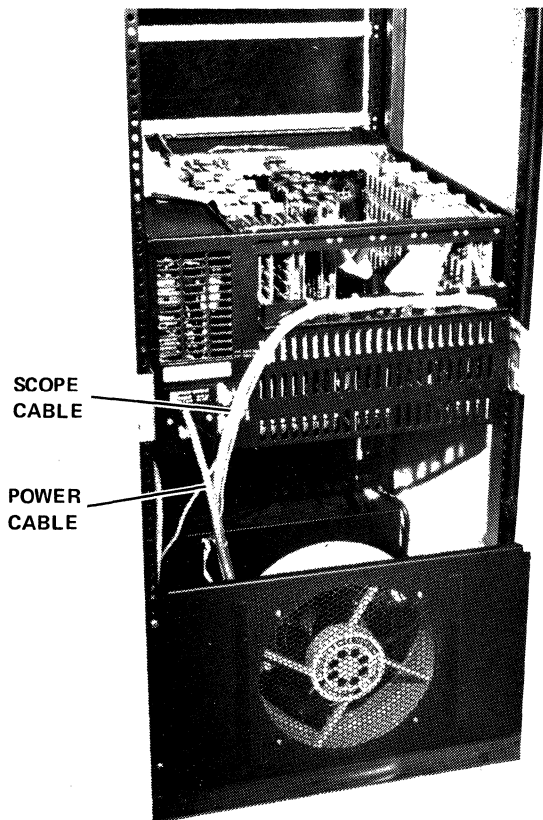


Figure 4 GT40, Rear View



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Figure 5 GT42, Rear View

1.4 SYSTEM OPERATION

The GT40/42 is a stable system that requires only minimum adjustments because it employs a combination of digital and analog techniques as opposed to analog circuits alone. The vector function operates efficiently, providing a good compromise of speed and accuracy and assuring a precise digital vector calculation. The presentation and accumulation of vectors means that every point of a vector is available in digital form.

During plotting, the end-point position is automatically retained, preventing accumulated errors or drift. Four different vector types — solid, long dash, short dash, and dot dash — are possible through standard hardware.

The GT40/42 character generator has both upper and lower case capability with a large repertoire of displayable characters. The display is the automatically refreshing type rather than the storage type so that a bright, continuous image, with excellent contrast ratio, is provided during motion or while changes are being made in the elements of the picture. A hardware blink feature is applicable to any characters or graphics drawn on the screen. A separate line clock in the display permits the GT40/42 to be synchronized to the line frequency. Scope resolution is precise enough to allow overprinting.

The terminal includes logic for descender characters such as “p” and “g,” positioning them correctly with respect to the text line. In addition to the 96 ASCII printing characters, 31 special characters are included which are addressed through the shift-in/shift-out control codes. These special characters include some Greek letters, architectural symbols, and math symbols. Characters can be drawn in italics simply by selecting the feature through the status instruction bit. Brightness and contrast are such that the scope can be viewed in a normally lighted room.

The instruction set consists of four control-state instructions and five data-state formats. The control instructions set the mode of data interpretation, set the parameters of the displayed image, and allow branching of the instruction flow. Data can be interpreted in any of five different formats, allowing tasks to be accomplished efficiently from both a core usage and time standpoint. The graph/plot feature of the GT40/42 automatically plots the x or y values according to preset distances as values for the opposite axis are recorded.

1.5 EQUIPMENT SPECIFICATIONS

The GT40/42 Graphic Display Terminal operating requirements and physical characteristics are listed by component in the following paragraphs. Refer to Volume 2 of the *GT40 Graphic Display Terminal Maintenance Manual* for the specifications pertaining to the KD11-B Processor (PDP-11/10).

Display Processor

Instruction Word Length	16 bits
Raster Definition	10 bits
Viewable Area	x = 1024 raster unit (1777 ₈) y = 768 raster units (1377 ₈)
Paper Size	12 bits
Hardware Blink	Programmable
Hardware Intensity Levels	8
Line Frequency Synchronization	Hardware programmable
Character Font	6 X 8 dot matrix
Characters/Line	73

Number of Lines	31
Character Set	96 ASCII – upper and lower case plus 31 specials (Greek letters, math symbols, etc.) (Refer to the appendix)
Control Characters	Carriage return Line feed Backspace
Bell Tone	Programmable
Italics	Hardware programmable
Line Type	Solid Long dash Short dash Dot dash
Data formats	Character (2 char/word) Short Vector (1 word) Long Vector (2 words) Point (2 words) Relative Point (1 word) Graphplot x/y (1 word/pt)
DPU Instructions	Set Graphic Modes Jump No operation (NOP) Load Status Register A Load Status Register B

DL11 Communications Interface Operating Specifications

Data Input and Output	Serial data, EIA and CCITT specifications compatible with Bell 103 and 202 Data Sets
Data Format	1 start bit 5, 6, 7, 8 data bits 1, 1.5, or 2 stop bits, odd, even or no parity.
Power Required	1.8A @ +5V 0.150A @ - 15V 0.050A @ +9 to +15V
Cable Length EIA	All baud rates: 50 ft (15.24m)
Noise Margin EIA	5V

MM11 Core Memory (refer also to Volume 2 of the *GT40 Graphic Display Terminal Maintenance Manual*).

Type	Magnetic core, read/write, coincident current, random access
Organization Capacity	Planar, 3D, 3-wire

Access Time

DATI	400 ns
DATIP	400 ns
DATO, DATOB	200 ns

Cycle Time

DATI	900 ns
DATIP	450 ns
DATO, DATOB (PAUSE L)	900 ns
DATO, DATOB (PAUSE H)	450 ns

LK40 Keyboard

Number of Keystations	58 (Major board) 8 (Minor board)
Encoding Format	1968 USASCII
Number of Codes	Either 96 or 128 codes (internal switch controllable,
Output Data Format	8-bit ASCII 1 start bit 7 data bits 2 stop bits
Baud Rate	Approximately 150 baud
Output Signal	20-mA current loop
Bell	Tone generator
Controls	Enable/Disable transmit

CRT Monitor

Viewable Area	
GT40	6.75 × 9 in. (17.145 × 22.86 cm)
GT42	8.5 × 11 in. (21.590 × 27.940 cm)
Brightness	> 30 fL (measured using a shrinking raster technique)
Contrast Ratio	> 10:1
Phosphor Type	P39 doped with IR
Pincushion	±1% of full scale to best fit line
Spot Size	< 20 mils inside the usable screen area at a brightness of 30 fL [Full Width at Half Maximum (FWHM)]

Jitter	< ±1/2 spot diameter
Repeatability	< ±1 spot diameter (repeatability is the deviation from the nominal location of any given spot)
Gain Change	From a fixed point on the screen, less than ±0.3% gain change for each ±1% line voltage variation
Temperature Range	0° to 50°C (operating)
Relative Humidity	10 to 90% (noncondensing)
Linearity	Maximum deviation of any straight line will be < 1% of the line length measured perpendicular to a best-fit straight line
Deflection Method	Magnetic (70° diagonal deflection angle)
Focus Method	Electrostatic
High Voltage	10.5 kV dc nominal (voltage proportional to input line voltage). Supply is self-contained and equipped with a bleeder resistor.
Shielding	CRT is fully enclosed in a magnetic shield.
Overload Protection	Unit is protected against fan failure or air blockage by thermal cutouts. Power supply and amplifiers are current limited. Phosphor protection is provided against fault conditions.

Light Pen

Length	5.0 in. (12.7 cm)
Diameter	0.45 in. (tapered to 0.35 in.) (1.143 cm) (0.889 cm)
Light Sensing	Phototransistor
Connector	Phono Plug
Signal Amplification	G840 Light Pen Amplifier module in VR14 CRT Display

Power Supply

Refer to Volume 2 of the *GT40 Graphic Display Terminal Maintenance Manual* for a detailed list of power supply specifications.

Environmental

Shock, Nonoperating	DEC STD 102, 205 at 30 ± 10 ms half-sine
Vibration, Nonoperating	DEC STD 102, Vertical 1.89 G rms 10 – 300 Hz
Operating Ambient Temperature	DEC STD 102, Class A, 60° – 95°F (16° – 35°C)
Relative Humidity (noncondensing)	DEC STD 102, Class 2, 20 – 80%

Physical

Weight

	GT40	GT42
CRT Monitor	80 lb (36.24 kg)	85 lb (38.55 kg)
Processor Cabinet	60 lb (27.18 kg)	275 lb (124.74 kg)
Keyboard	6.25 lb (2.83 kg)	6.25 lb (2.83 kg)

GT40 Size

	Height	Width	Depth
CRT Monitor	12.5 in. (31.75 cm)	19.75 in. (50.165 cm)	22.25 in. (56.515 cm)
Processor Cabinet	5.25 in. (13.335 cm)	19.75 in. (50.165 cm)	23.25 in. (59.055 cm)
Keyboard	3.0 in. (7.62 cm)	15.625 in. (42.227 cm)	6.625 in. (16.827 cm)

GT42 Size

	Height	Width	Depth
CRT Monitor	15 in. (38.10 cm)	21.5 in. (54.61 cm)	27 in. (68.58 cm)
Processor Cabinet	50 in. (127.00 cm)	21 in. (53.34 cm)	38 in. (96.52 cm)
Keyboard	3 in. (7.62 cm)	16.625 in. (42.227 cm)	6.625 in. (16.827 cm)

2.1 GT40/GT42 START-UP PROCEDURES

The procedure used to start the GT40/GT42 Graphic Display Terminal is determined by the system configuration. A GT40/GT42 that operates as a terminal in a larger system is started differently than a GT40/GT42 that functions as a stand-alone device. Four procedures are presented in the following paragraphs: GT40/GT42 Terminal Systems, GT42 Paper Tape Systems, GT40 Paper Tape Systems, and GT42 Bootstraps for Other Devices.

2.1.1 GT40/GT42 Terminal Systems

The following procedure is used to initiate the ROM Bootstrap from the PDP-11/10 console on the GT40/42.

1. Determine that the GT40/42 power cord is connected to an appropriate electrical outlet.
2. Turn the console key switch (Figure 1) to the POWER position.
3. Turn the front panel ON-OFF/BRIGHTNESS switch fully counterclockwise and then 3/4 of the way in the clockwise direction. The red power indicator light just below the switch should be on at this time.
4. Press the console ENABLE/HALT switch down to halt the computer.
5. Press the spring-loaded START switch twice; this resets the computer.
6. Place 166000₈ in the Switch register (SR). This is the starting address for the Bootstrap program in the Read-Only Memory (ROM) (Figure 20).
7. Press LOAD ADDRESS to load the address into the computer.
8. Return the ENABLE/HALT switch to the up-most position.
9. Press the START switch. The RUN indicator light should be on at this time.

10. Ensure that the LK40 keyboard ENABLE/DISABLE (On-Off) switch is in the ON position (Figure 6).
11. The GT40/42 is now ready to transmit data to and receive data from the host computer via the DL11 Asynchronous Interface module.

NOTE

A detailed description of the ROM Bootstrap and the loading procedure from a host computer are contained in Paragraph 5.1.

2.1.2 GT42 Paper Tape Systems

The following procedure is used to initiate the ROM Bootstrap from the PDP-11/10 console on the GT42.

1. Determine that the GT42 power cord is connected to an appropriate electrical outlet.
2. Turn the console key switch (Figure 2) to the POWER position.
3. Turn the front panel ON-OFF/BRIGHTNESS switch fully counterclockwise and then 3/4 of the way in the clockwise direction. The red power indicator light just below the switch should be on at this time.
4. Press the console ENABLE/HALT switch down to halt the computer.
5. Press the spring-loaded START switch twice; this resets the computer.
6. Place 167400₈ in the Switch register (SR). This is the starting address for the paper tape Bootstrap program in the Read Only Memory (ROM).
7. Press LOAD ADDRESS to load the address into the computer.
8. Return the ENABLE/HALT switch to the up-most position.
9. Place the Absolute Loader in the specified reader with the special bootstrap leader code over the reader sensors (under the reader station).
10. Press START. The Absolute Loader tape will pass through the reader as data is being loaded into core.
11. The tape stops after the last frame of data has been read into core. The Absolute Loader is now in core. If the Absolute Loader tape does not read in immediately after depressing the START switch, perform steps 26 and 27 of Paragraph 2.1.3.

2.1.3 GT40 Paper Tape Systems

1. Determine that the GT40 power cord is connected to an appropriate electrical outlet.
2. Turn the console key switch (Figure 1) to the POWER position.
3. Turn the front panel ON-OFF/BRIGHTNESS switch fully counterclockwise and then 3/4 of the way in the clockwise direction. The red power indicator light just below the switch should be on at this time.
4. Press the console ENABLE/HALT switch down to halt the computer.
5. Press the spring-loaded START switch twice; this resets the computer.
6. The Bootstrap Loader will now be loaded (toggled) into the highest core memory bank. The locations and corresponding instructions of the Bootstrap Loader are listed in Table 1.

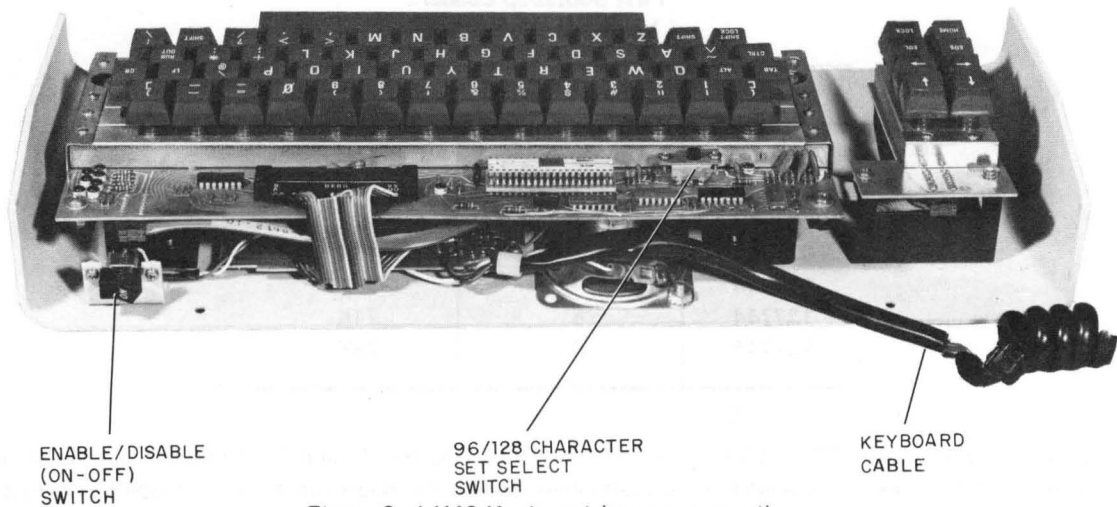


Figure 6 LK40 Keyboard (cover removed)

The Bootstrap Loader program instructs the computer to accept and store in core memory data that is punched on paper tape in bootstrap format. The Bootstrap Loader is used to load very short paper tape programs of 162_8 16-bit words or less (primarily the Absolute Loader and Memory Dump programs). Programs longer than this must be assembled into absolute binary format using the PAL-11A Assembler and loaded into memory using the Absolute Loader (step 19).

Table 1
Bootstrap Loader Instructions

Location	Instruction
xx7744	016701
xx7746	000026
xx7750	012702
xx7752	000352
xx7754	005211
xx7756	105711
xx7760	100376
xx7762	116162
xx7764	000002
xx7766	xx7400
xx7770	005267
xx7772	177756
xx7774	000765
xx7776	YYYYYY

In Table 1, xx represents the highest available memory bank. For example, the first location of the loader would be 037744_8 if the system contained an 8K memory. Table 2 lists the locations for the first Bootstrap Loader instruction as determined by the memory size. All other locations, for a given memory, are prefixed with the same two digits.

Table 2
First Bootstrap Loader
Instruction Locations

Location	Memory Bank	Memory Size
017744	0	4K
037744	1	8K
057744	2	12K
077744	3	16K
117744	4	20K
137744	5	24K
157744	6	28K

The contents of location xx7776 (YYYYYY in the Instruction column of Table 1) should contain the device status register address of the paper tape reader to be used when loading the bootstrap formatted tapes. Either paper tape reader may be used; their respective addresses are:

Teletype Paper Tape Reader – 177560
 High Speed Paper Tape Reader – 177550

7. Set xx7744 in the Switch register (SR) and press the LOAD ADDRESS switch (xx7744 will be displayed in the address register).
8. Set the first instruction, 016701, in the SR and lift the DEPOSIT switch (016701 will be displayed in the data register).

NOTE

When DEPOSITING data into consecutive words, the DEPOSIT automatically increments the address register to the next word.

9. Set the next instruction, 000026, in the SR and lift DEPOSIT (000026 will be displayed in the data register).
10. Set the next instruction in the SR and press the DEPOSIT switch. Continue depositing subsequent instructions until 000765 is stored in location xx7774.
11. Deposit the desired device status register address in location xx7776, the last location of the Bootstrap Loader.
12. Good programming procedure requires the verification of data that has been stored.
13. Set xx7744 in the SR and press the LOAD ADDRESS switch.
14. Press the EXAMINE switch. The octal instruction in location xx7744 will be displayed so that it can be compared with the correct instruction: 016701. If the instruction is correct, proceed to step 15, otherwise go to step 17.

15. Press the EXAMine switch. When the switch is held depressed, the ADDRESS/DATA indicators display the memory address. On releasing the switch, the instruction at that address is displayed. Compare the indicator display with the required instruction (Table 1). (The EXAMine switch automatically increments the address register.)
16. Repeat step 15 until all instructions have been verified or go to step 17 whenever the correct instruction is not displayed.

NOTE

Whenever an incorrect instruction is displayed, it can be corrected by performing steps 17 and 18.

17. When an incorrect instruction is displayed in the ADDRESS/DATA indicators, set the correct instruction in the SR and lift the DEposit switch.
18. Press and release the EXAMine switch to verify that the correct instruction has been deposited. Continue the checking (step 15) until all the instructions have been verified.
19. The Absolute Loader program will be loaded into core memory at this time. The Absolute Loader is a system program which, after being loaded into memory, allows the operator to load, into any core memory bank, data punched on paper tape in absolute binary format. It is used primarily to load the paper tape system software (excluding certain subprograms) and the user's object programs assembled with PAL-11A. The major features of the Absolute Loader include:
 - Testing of the checksum on the input tape to ensure complete, accurate loads.
 - Starting the loaded program upon completion of loading without additional user action, as specified by the .END in the program just loaded.
 - Specifying the load address of position independent programs at load time rather than at assembly time, by using the desired loader switch register option.

With the Bootstrap Loader in core memory, the Absolute Loader is loaded into memory starting anywhere between locations xx7500 and xx7742, i.e., 162₁₀ words. The paper tape input device used is specified in location xx7776 (step 11). The Absolute Loader tape begins with about two feet of special bootstrap leader code (ASCII code 351), not blank leader tape.

20. Set the ENABLE/HALT switch to HALT.
21. Place the Absolute Loader in the specified reader with the special bootstrap leader code over the reader sensors (under the reader station).
22. Set the SR to xx7744 (the starting address of the Bootstrap Loader) and press LOAD ADDRESS.
23. Set the ENABLE/HALT switch to ENABLE.
24. Press START. The Absolute Loader tape will pass through the reader as data is being loaded into core.
25. The tape stops after the last frame of data has been read into core. The Absolute Loader is now in core.

26. If the Absolute Loader tape does not read in immediately after depressing the START switch (step 24), it is due to one of the following causes:

- Bootstrap Loader not correctly loaded.
- The wrong input device was used.
- Code 351₈ was not directly over the reader sensors.
- The Absolute Loader tape was not properly positioned in the reader.

27. Any paper tape punched in absolute binary format is referred to as an absolute tape, and is loaded into memory using the Absolute Loader. When using the Absolute Loader, there are two methods of loading available: normal and relocated.

A normal load occurs when the data is loaded and placed in core according to the load addresses on the object tape. It is specified by setting bit 0 of the Switch register to zero immediately before starting the load.

There are two types of relocated loads.

- a. Loading to continue from where the loader left off after the previous load. This is used, for example, when the object program being loaded is contained on more than one tape. It is specified by setting the Switch register to 000001 immediately before starting the load.
- b. Loading into a specific area of core. This is normally used when loading position independent programs. A position independent program is one that can be loaded and run anywhere in available core. The program is written using the position independent instruction format. This type of load is specified by setting the Switch register to the load address and adding 1 to it, i.e., setting bit 0 to 1.

Optional Switch register settings for the three types of loads are listed in Table 3.

Table 3
Switch Register Configuration for Loading

Type of Load	Switch Register	
	Bits 1–14	Bit 0
Normal	(ignored)	0
Relocated – continue loading where left off	0	1
Relocated – load in specified area of core	nnnnn (specified address)	1

The absolute tape is now loaded using either of the paper tape readers. The desired reader is specified in the last word of available core memory (xx7776), the input device status word, as explained in step 6. The input device status word can be changed at any time prior to loading the absolute tape.

28. Set the ENABLE/HALT switch to HALT.

To use an input device different from that used when loading the Absolute Loader, change the address of the device status word (in location xx7776) to reflect the desired device, i.e., 177560 for the Teletype[®] reader or 177550 for the high speed reader.

29. Set the SR to xx7500 and press LOAD ADDR.
30. Set the SR to reflect the desired type of load.
31. Place the absolute tape in the proper reader with blank leader tape directly over the reader sensors.
32. Set ENABLE/HALT to ENABLE.
33. Press START. The absolute tape will begin passing through the reader station as data is being loaded into core.
34. The Absolute Loader was not correctly stored in memory if the absolute tape does not begin passing through the reader station. If this occurs, reload the loader (steps 20–25) and then the absolute tape (starting at step 28).

If the absolute tape halts in the middle of the tape, a checksum error occurred in the last block of data read. Normally, the absolute tape will stop passing through the reader station when it encounters the transfer address as generated by the .END statement, denoting the end of a program. If the system halts after loading, check that the low byte of the data register is zero. If so, the tape is correctly loaded. If not zero, a checksum error has occurred in the block of data just loaded, indicating that some data was not correctly loaded. Thus, the tape should be reloaded starting at step 1.

When loading a continuous relocated load, subsequent blocks of data are loaded by placing the next tape in the appropriate reader and pressing the CONTInue switch.

35. The Absolute Loader may be restarted at any time by starting at step 1.

2.1.4 GT42 Bootstraps For Other Devices

The GT42 contains bootstrap programs for the following devices:

Device	Starting Address (Octal)
TA11 Cassette	167500
RF11 Fixed Head Disk	167600
RC11 Fixed Head Disk	167720
RK11 Disk Cartridge	167610
RP11 Disk Pack	167654
TC11 DECtape	167620
TM11 Magnetic Tape	167636

The following procedure is used to initiate one of the above devices from the PDP-11/10 console of the GT42.

1. Determine that the GT42 power cord is connected to an appropriate electrical outlet.
2. Turn the console key switch to the POWER position.
3. Press the console ENABLE/HALT switch down to halt the computer.

[®] Teletype is a registered trademark of Teletype Corporation.

4. Press the spring-loaded START switch twice; this resets the computer.
5. Place the address of the device to be started into the Switch register. The device starting addresses are listed above.
6. Press the LOAD ADDRESS switch to load the address into the computer.
7. Return the ENABLE/HALT switch to the up-most position.
8. Press the START switch.

2.1.5 GT42 Graphics Test

The GT42 contains a short program which tests the fundamental graphic capabilities of the display processor. The program, which starts at octal address 167204, displays several lines and points on the CRT.

2.2 GT40/42 FAILURE PROCEDURES

The following procedures should be followed in the event the GT40/42 fails to operate properly. If, after performing these checks, equipment operation is still unsatisfactory, the user should notify the DEC Field Service Office of the problem.

If the GT40/42 is completely inoperative:

1. Check the circuit breaker on the rear panel of the GT40 (Figure 4) or in the cabinet of the GT42. Press the button to reset the circuit breaker.
2. Check the power cord to the wall receptacle. It should be properly seated.
3. Determine that the required power (115 or 230 Vac) is present at the wall receptacle.

If the display scope fails to turn on:

1. Check the keyboard cable connector on the GT40/42 rear panel for proper seating.
2. Check the power plugs on the rear panel and the power control box for proper seating.
3. Determine that the front panel ON-OFF/BRIGHTNESS switch is in the ON position (clockwise).
4. Check the following fuses on the rear panel and the power control box:
 - 5A SB (115 V system)
(or 3A SB for 230 V systems)
 - 10A (115 V systems)
(or 5A for 230 V systems)

If the keyboard is incapable of transmitting data:

1. Check the ON/OFF switch on the rear of the keyboard (Figure 6). Place it in the ON position.
2. Check the cable connectors on the GT40/42 rear panel (particularly the keyboard cable) for proper seating.

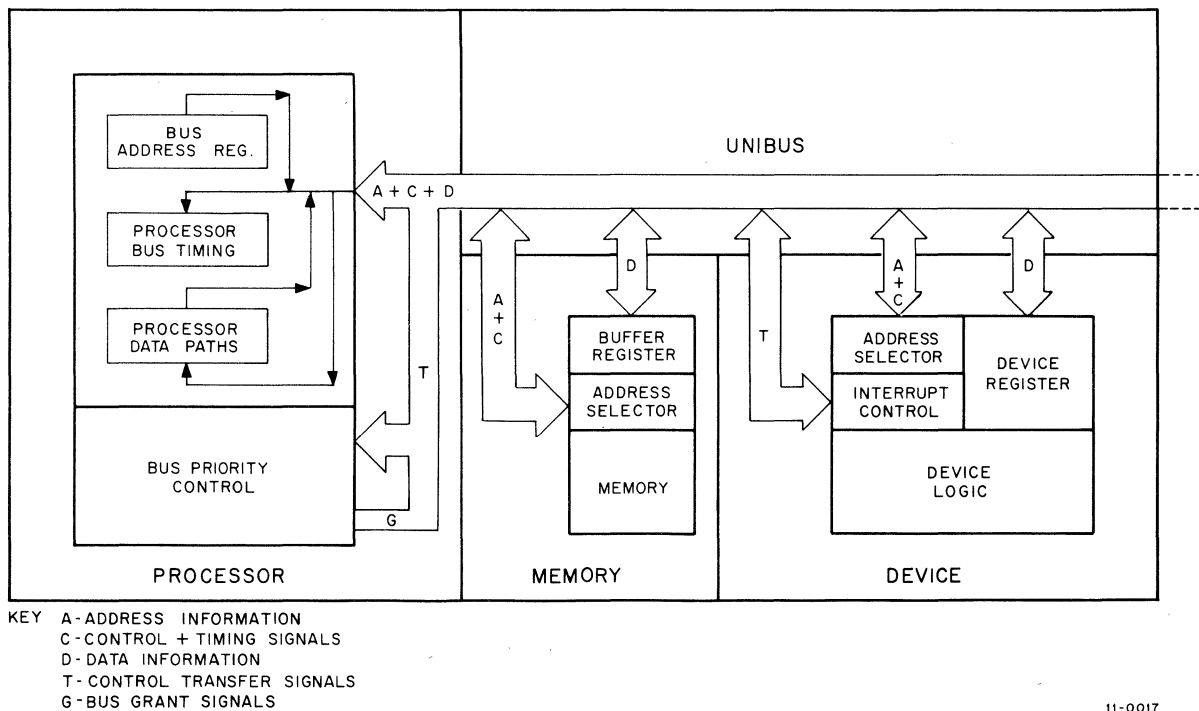
3.1 GT40/42 INTERFACES

Transferral of information between GT40/42 components and devices external to the basic system requires a means for connecting or interfacing an extended system. The interface can be considered to be the physical boundary between the GT40/42 and attached units; it provides the communication link between the display terminal and associated devices such as a host computer or additional memory units.

3.2 PARALLEL PORT

The GT40/42 possesses two interfaces. One, called the *parallel port*, uses conventional Unibus signals and connections to transfer data in parallel format. The other interface is employed in the transfer of asynchronous data, in a serial format, over a longer communications line. The two interfaces and their relation to the GT40/42 are shown in Figure 7.

The parallel port is used typically to interface local high speed peripheral devices such as additional core memory, disk storage units, etc. The parallel port is basically an extension of the PDP-11 family Unibus.



11-0017

Figure 7 Unibus Interface Block Diagram

3.2.1 Unibus Structure

The Unibus is a single common path that connects the processor, memory, and all peripherals. Addresses, data, and control information are transmitted along the 56 lines of the bus. All 56 signals and their functions are listed in Table 4.

Every device on the Unibus employs the same form of communication; thus, the processor uses the same set of signals to communicate with memory and with peripheral devices. Peripheral devices also communicate with the processor, memory, or other peripheral devices via the same set of signals.

All instructions applied to data in memory can be applied equally well to data in peripheral device registers, enabling peripheral device registers to be manipulated by the processor with the same flexibility as memory. This feature is especially powerful, considering the capability of PDP-11 instructions to process data in any memory location as though it were an accumulator.

Table 4
Unibus Signals

Name	Mnemonic	Source	Destination	Timing	Function
Data Transfer Signals (For transfer of data to or from master)					
Address	A(17:00)	Master	All	MSYN	Selects slave device
Data	D(15:00)	Master	Slave	MSYN (DATO, DATOB)	
		Slave	Master	SSYN (DATI, DATIP)	
Control	C(1:0)	Master	Slave	MSYN	Selects transfer operation
Master Sync	MSYN	Master	Slave	Beginning of transfer	Initiates operation and gates A, C, and D signals
Slave Sync	SSYN	Slave	Master	Data accepted (DATO, DATOB) Data Available (DATI, DATIP)	Response to MSYN
Parity Bit Low	PA	Master	Slave	Same as Data	Transmits parity bit, low byte
Parity Bit High	PB	Master	Slave	Same as Data	Transmits parity bit, high byte
Priority Transfer Signals (For transfer of bus control to a priority-selected master)					
Non-Processor Request	NPR	Any	Processor	Asynchronous	Highest priority bus request
Bus Request	BR(7:4)	Any	Processor	Asynchronous	Requests bus mastership
Non-Processor Grant	NPG	Processor	Next master	In parallel with data transfer	Transfers bus control
Bus Grant	BG(7:4)	Processor	Next master	After instruction	Transfers bus control
Selection Acknowledge	SACK	Next Master	Processor	Response to NPG or BG	Acknowledges grant & inhibits further grants
Bus Busy	BBSY	Master	All	except during transfer of control	Asserts bus mastership

Table 4 (Cont)
Unibus Signals

Name	Mnemonic	Source	Destination	Timing	Function
Interrupt	INTR	Master	Processor	After asserting BBSY (not after NPR), device may perform several transfers before asserting INTR.	Transfers bus control to handling routine in processor
Miscellaneous Signals					
Initialize	INIT	Processor	All	Asynchronous	Clear and reset signal
AC Low	AC LO	Power	All	Asynchronous	Indicates impending power failure
DC Low	DC LO				Indicates dc voltages out of tolerance, and system operation must be suspended.

NOTE

Signals on the Unibus are asserted when low (except for the unidirectional bus grant lines).

3.2.1.1 Bidirectional Lines – Most Unibus lines are bidirectional, allowing input lines to also be driven as output lines. This is significant in that a peripheral device register can be either read or used for transfer operations. Thus, the same register can be used for both input and output functions.

3.2.1.2 Master/Slave Relationship – Communication between two devices on the bus is based on a master/slave relationship. During any bus operation, one device, referred to as the bus master, has control of the bus when communicating with another device, the slave. A typical example of this relationship is the processor (master) transferring data to memory (slave). Master/slave relationships are dynamic. The processor, for example, passes bus control to a disk; the disk, as master, then communicates with a slave memory.

The Unibus is used by the processor and all I/O devices; thus, a priority structure determines which device gains control of the bus. Consequently, every device on the Unibus capable of becoming bus master has an assigned priority. When two devices capable of becoming bus master have identical priority values and simultaneously request use of the bus, the device that is electrically closest to the bus receives control.

3.2.1.3 Interlocked Communication – Communication on the Unibus is interlocked between devices. Each control signal issued by the master device must be acknowledged by a response from the slave to complete the transfer. Consequently, communication is independent of the physical bus length and the response time of the master and slave devices. The maximum transfer rate on the Unibus, with optimum device design, is one 16-bit word every 400 ns or 2.5 million 16-bit words per second.

3.2.2 Peripheral Device Organization and Control

Peripheral device registers are assigned addresses similar to memory; thus, all PDP-11 instructions that address memory locations can become I/O instructions, enabling data registers in peripheral devices to take advantage of all the arithmetic power of the processor.

The PDP-11 controls devices differently than most computer systems. Control functions are assigned to a register address, and then the individual bits within that register can cause control operations to occur. For example, the command to make the paper tape reader read a frame of tape is provided by setting a bit (the reader enable bit) in the control register of the device. Instructions such as MOV and BIS may be used for this purpose. Status conditions are also handled by the assignment of bits within this register, and the status is checked with TST, BIT, and CMP instructions.

3.2.3 Unibus Control Arbitration

The Unibus is capable of performing two basic and parallel tasks in order to allow transfers by multiple peripherals at maximum speed. The first is the actual transfer of data between the current bus master and its addressed slave. The second is the selection of the next bus master, the peripheral which will be allowed to assert control as soon as the bus becomes free. It is important to note that the granting of future mastership is in no way influenced by either the current master or its method of obtaining the bus. It is this fact which allows these functions to be performed in parallel and allows transfers on the bus at a maximum rate.

3.2.3.1 Priority Transfer Requests — To gain mastership of the Unibus, a peripheral must first make a request to the processor for the bus and then wait for its selection. The processor contains the logic necessary to arbitrate these requests because normally there are several requests pending at any given time.

There are two classes of requests: bus requests and non-processor requests. A bus request (BR) is simply a request by a peripheral to obtain control of the Unibus with the understanding by the processor that the peripheral may end its use of the bus with a processor interrupt. An interrupt is a command to the processor to begin executing a new routine pointed to by a location selected by a device. A non-processor request (NPR) is similarly a request for the bus, but with the exception that it may not interrupt the processor. Since the granting of an NPR cannot affect the execution of the processor, it can occur during or between instructions. BRs, however, by possibly causing execution to be diverted to a totally new routine, can only be granted between instructions. In this way, NPRs are assigned priority over any BR.

Between bus requests, there are four levels of priority created by four separate request lines. They are assigned priority levels 4 through 7; BR4 is the lowest and BR7 is the highest. These levels are associated with the program controlled priority level of the processor, controlled by bits 7, 6, and 5 of the processor status register. Only BRs on a priority level higher than the level of the processor are eligible for receiving a bus grant. Thus, during high priority program tasks, all or selected Unibus requests (hence interrupts) can be inhibited by raising the level of the processor priority.

Another form of priority arbitration occurs through the system configuration. When the processor grants a request, the grant travels along the bus until it reaches the first requesting device which terminates the grant. Therefore, along the same grant line, the device electrically nearest the processor has the highest priority. Also note that in the KD11-B, the internal line clock is logically the last device on BR6, and the keyboard or Teletype interface is logically the last device on BR4.

The GT40/42 relationship to this priority scheme is indicated in Table 5.

After a requesting device receives a bus grant it asserts its selection as next bus master until the bus is free, thus inhibiting other requests from being granted. When the bus becomes free, the selected device asserts control of the bus and relinquishes its selection as next bus master so that the priority arbitration among pending requests may continue.

**Table 5
GT40/42 Priority**

GT40/42 Component	Priority Level	Relative Physical Position from the CPU
DL11 Asynchronous Interface	BR5	2
Display Processor	BR4	1
Unibus Output Slot (Parallel Port)	—	3

NOTE: The MM11 memory is not shown as an active device because it always functions as a slave, never asserting a bus request itself.

3.2.3.2 Processor Interrupts — After gaining control of the bus through a BR, a device can perform one or more transfers on the bus and/or request a processor interrupt. This is typically requested after a device has completed a given task, e.g., typing a character or completing a block data transfer through NPRs. If a peripheral wishes to interrupt the processor, it must assert the interrupt after gaining control of the bus but before relinquishing its selection as next bus master. Thus the processor knows that it may not fetch the next instruction, but must wait for the interrupt to be completed. Along with asserting the interrupt, the device asserts the unique memory address, known as the interrupt vector address, containing the starting address of the device service routine. Address vector +2 contains the new processor status word (PSW) to be used by the processor when beginning the service routine. After recognizing the interrupt, the processor reads the vector address and saves it in an internal register. It then pushes the current PSW and program counter onto the stack and loads the new program counter (PC) and PSW from the vector address specified. The service routine is then executed.

NOTE

These operations are performed automatically and no device polling is required to determine which routine to execute.

The device service routine can cause the processor to resume the interrupted process by executing the return from interrupt (RTI) instruction which pops the top two words from the processor stack and transfers them back to the PC and PS registers.

3.2.3.3 Data Transfers — After asserting control of the Unibus, the device does not release control until it has completed either one or more data transfers or an interrupt. Typically, only one transfer is completed each time the device gains control of the bus because few single devices can give or receive information at the maximum Unibus rate. Holding the bus for multiple transfers inhibits other devices from using the bus.

A transfer is initiated by the master device asserting a slave address and control signals on the bus and a master or address validity signal. The appropriate slave recognizes the valid address, reads or writes the data, and responds with a transfer complete signal. The master recognizes the transfer complete, sends or accepts data, and drops the address validating signal. It can then assert a new address and repeat the process or release control of the bus completely.

The importance of this type of structure is that it enables direct device-to-device transfers without any interaction from the central processor. An NPR device, such as the high speed CRT display, can gain fast access to the bus and transfer data at high rates while refreshing itself from memory without slowing down the processor.

For a more detailed description of the Unibus and its function, refer to the *GT40 Graphic Display Terminal Maintenance Manual*, Volume 2 or to the *PDP-11 Peripherals Handbook*.

3.3 SERIAL PORT

The serial port is the primary means of interfacing the GT40/42 with a host or remote computer. Access to this port is through the DL11 Asynchronous Interface module and the 25-ft BC05-C-25 cable which terminates in a 25-pin, RS232-defined connector at a data set modem (Figure 3 and Table 6).

Table 6
BC05-C-25 Cable Output Connections

CINCH Connector Pin No. (to modem)	Signal
1	Ground
2	Transmitted Data
3	Received Data
4	Request to Send
5	Clear to Send
6	Data Set Ready
7	Ground
8	Carrier
9	+ Power
10	- Power
11	202 Secondary Transmit
12	202 Secondary Receive
13	Secondary Clear to Send
14	EIA Secondary Transmit
15	Serial Clock Transmit
16	EIA Secondary Receive
17	Serial Clock Receive
18	Unassigned
19	Secondary Request to Send
20	Data Terminal Ready
21	Signal Quality
22	Ring
23	Signal Rate
24	External Clock
25	Force Busy

3.4 DL11 PROGRAMMING

All software control of the DL11 Asynchronous Line Interface is performed by means of four device registers. These registers have been assigned bus addresses and can be read or loaded (with the exceptions noted) using any PDP-11 instruction referring to their addresses. Address assignments can be changed by altering jumpers on the address selection logic to correspond to any address within the range of 174000 to 177777. However, register addresses for the DL11 in the GT40/42 fall within the range of 175610 to 175616.

The four device registers and associated DL11 addresses are listed in Table 7.

Table 7
Standard DL11 Register Assignments for the GT40/42

Register	Mnemonic	Address
Receiver Status Register	RCSR	175610
Receiver Buffer Register	RBUF	175612
Transmitter Status Register	XCSR	175614
Transmitter Buffer Register	XBUF	175616

Figures 8 through 11 show the bit assignments for the four device registers. The unused and load-only bits are always read as 0s. Loading unused or read-only bits has no effect on the bit position. The mnemonic INIT refers to the initialization signal issued by the processor. Initialization is caused by one of the following: issuing a programmed RESET instruction; depressing the START switch on the processor console; or the occurrence of a power-up or power-down condition of the processor power supply.

In the following descriptions, *transmitter* refers to those registers and bits involved in accepting a parallel character from the Unibus for serial transmission to the external device; *receiver* refers to those registers and bits involved with receiving serial information from the external device for parallel transfer to the Unibus.

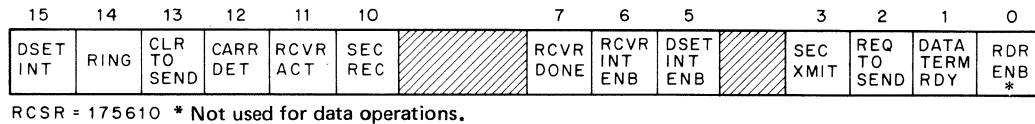


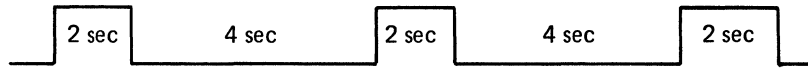
Figure 8 Receiver Status Register (RCSR) – Bit Assignments

3.4.1 Receiver Status Register

Bit	Name	Meaning and Operation
15	DATASET INT (Dataset Interrupt)	This bit initiates an interrupt sequence provided the DATASET INT ENB bit (05) is also set. This bit is set whenever CAR DET, RCVR ACT, or SEC REC changes state, i.e., on a 0 to 1 or 1 to 0 transition of any one of these bits. It is also set when RING changes from 0 to 1.

Cleared by INIT or by reading the RCSR. Because reading the register clears the bit, it is, in effect, a "read-once" bit.

- 14 RING When set, indicates that a RINGING signal is being received from the dataset. Note that the RINGING signal is not a level but an EIA control signal with the cycle time as shown below:



Read-only bit

- 13 CLR TO SEND (Clear to Send) The state of this bit is dependent on the state of the CLEAR TO SEND signal from the dataset. When set, this bit indicates an ON condition; when clear, it indicates an OFF condition.

Read-only bit.

- 12 CAR DET (Carrier Detect) This bit is set when the data carrier is received. When clear, it indicates either the end of the current transmission activity or an error condition.

Read-only bit.

- 11 RCVR ACT (Receiver Active) When set, this bit indicates that the DL11 interface receiver is active. The bit is set at the center of the START bit which is the beginning of the input serial data from the device and is cleared by the leading edge of RCVR DONE.

Read-only bit; cleared by INIT or by RCVR DONE (bit 07).

- 10 SEC REC (Secondary Receive or Supervisory Received Data) This bit provides a receive capability for the reverse channel of a remote station. A space (+6V) is read as a 1. (A transmit capability is provided by bit 03.)

Read-only bit; cleared by INIT.

- 9-8 Unused Not applicable.

- 07 RCVR DONE (Receiver Done) This bit is set when an entire character has been received and is ready for transfer to the Unibus. When set, initiates an interrupt sequence provided RCVR INT ENB (bit 06) is also set.

Cleared whenever the receiver buffer (RBUF) is addressed or whenever RDR ENB (bit 00) is set. Also cleared by INIT.

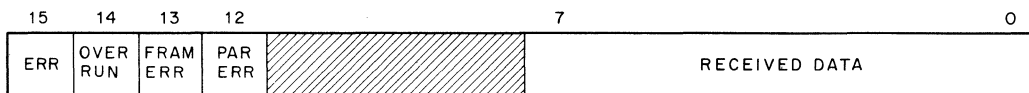
Read-only bit.

Bit	Name	Meaning and Operation
06	RCVR INT ENB (Receiver Interrupt Enable)	When set, allows an interrupt sequence to start when RCVR DONE (bit 07) sets. Read/write bit; cleared by INIT.
05	DATASET INT ENB (Dataset Interrupt Enable)	When set, allows an interrupt sequence to start when DATASET INT (bit 15) sets. Read/write bit; cleared by INIT.
04	Unused	Not applicable.
03	SEC XMIT (Secondary Transmit or Supervisory Transmitted Data)	This bit provides a transmit capability for a reverse channel of a remote station. When set, transmits a space (+6V). (A receive capability is provided by bit 10.) Read/write bit; cleared by INIT.
02	REQ TO SEND (Request to Send)	A control lead to the dataset which is required to transmission. A jumper ties this bit to REQ TO SEND or FORCE BUSY in the dataset. Read/write bit; cleared by INIT.
01	DTR (Data Terminal Ready)	A control lead for the dataset communication channel. When set, permits connection to the channel. When clear, disconnects the interface from the channel. Read/write bit; must be cleared by the program, is not cleared by INIT.

NOTE

The state of this bit is not defined after power-up.

00	RDR ENB (Reader Enable)	When set, this bit advances the paper-tape reader in ASR Teletype units and clears the RCVR DONE bit (bit 07). This bit is cleared at the middle of a START bit which is the beginning of the serial input from an external device. Also cleared by INIT. Write-only bit. Not used in dataset configurations.
----	----------------------------	--



RBUF = 175612

Figure 9 Receiver Buffer Register (RBUF) – Bit Assignments

3.4.2 Receiver Buffer Register

Bit	Name	Meaning and Operation
15	ERROR (Error)	Used to indicate that an error condition is present. This bit is the logical OR of OR ERR, FR ERR, and P ERR (bits 14, 13, and 12, respectively). Whenever one of these bits is set, it causes ERROR to set. This bit is not connected to the interrupt logic. Read-only bit; cleared by removing the error-producing condition.
NOTE		
Error indications remain present until the next character is received, at which time the error bits are updated. INIT does not necessarily clear the error bits.		
14	OR ERR (Overrun Error)	When set, indicates that reading of the previously received character was not completed (RCVR DONE not cleared) prior to receiving a new character. Read-only bit; cleared in the same manner as ERROR (bit 15).
13	FR ERR (Framing Error)	When set, indicates that the character that was read had no valid STOP bit. Read-only bit; cleared in the same manner as ERROR (bit 15).
12	P ERR (Parity Error)	When set, indicates that the parity received does not agree with the expected parity. This bit is always 0 if no parity is selected. Read-only bit; cleared in the same manner as ERROR (bit 15).
11–08	Unused	Not applicable.
07–00	RECEIVED DATA BITS	Holds the character just read. If less than eight bits are selected, then the buffer is right-justified into the least significant bit positions. In this case, the higher unused bit or bits read as 0s. Read-only bits; not cleared by INIT.



XCSR = 175614

Figure 10 Transmitter Status Register (XCSR) – Bit Assignments

3.4.3 Transmitter Status Register

Bit	Name	Meaning and Operation
15–08	Unused	Not applicable.
07	XMIT RDY (Transmitter Ready)	This bit is set when the transmitter buffer (XBUF) can accept another character. When set, it initiates an interrupt sequence provided XMIT INT ENB (bit 06) is also set. Read-only bit. Set by INIT. Cleared by loading the transmitter buffer.
06	XMIT INT ENB (Transmitter Interrupt Enable)	When set, allows an interrupt sequence to start when XMIT RDY (bit 07) sets.
05–03	Unused	Not applicable.
02	MAINT (Maintenance)	Used for maintenance function. When set, disables the serial line input to the receiver and connects the transmitter output to the receiver input which disconnects the external device input. It also forces the receiver to run at transmitter speed. Read/write bit; cleared by INIT.
01	Unused	Not applicable.
00	BREAK	When set, transmits a continuous space to the external device. Read/write bit; cleared by INIT.

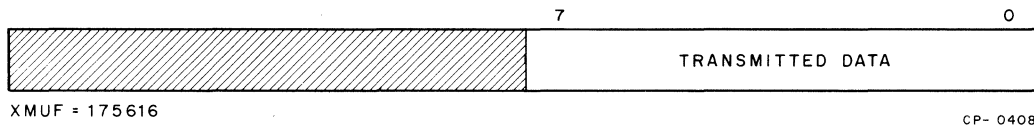


Figure 11 Transmitter Buffer Register (XBUF) – Bit Assignments

3.4.4 Transmitter Buffer Register

Bit	Name	Meaning and Operation
15–08	Unused	Not applicable.
07–00	TRANSMITTER DATA BUFFER	Holds the character to be transferred to the external device. If less than eight bits are used, the character must be loaded so that it is right-justified into the least significant bits. Write-only bits.

3.4.5 Interrupts

The DL11 interface uses BR interrupts to gain control of the bus to perform a vectored interrupt, thereby causing a branch to a handling routine. The DL11 has two interrupt channels: one for the receiver section and one for the transmitter section. These two channels operate independently; however, if simultaneous interrupt requests occur, the receiver has priority. The receiver section is capable of handling multiple source interrupts.

A transmitter interrupt can occur only if the interrupt enable bit (XMIT INT ENB) in the transmitter status register is set. With XMIT INT ENB set, setting the transmitter ready (XMIT RDY) bit initiates an interrupt request. When XMIT RDY is set, it indicates that the transmitter buffer is empty and ready to accept another character from the bus for transfer to the external device.

A receiver data interrupt can occur only if the interrupt enable (RCVR INT ENB) bit in the receiver status register is set. With RCVR INT ENB set, setting the receiver done (RCVR DONE) bit initiates an interrupt request. When RCVR DONE is set, it indicates that an entire character has been received and is ready for transfer to the bus. The additional interrupt request sources for the DL11 option are discussed in the following paragraphs.

The receiver portion of the DL11 in the GT40/42 dataset configuration can service multiple source interrupts. One of the receiver interrupt circuits is activated by RCVR INT ENB and RCVR DONE. The additional interrupt circuit can cause an interrupt only if the dataset interrupt enable bit (bit 05, DATASET INT ENB) in the receiver status register is set. With DATASET INT ENB set, setting the DATASET INT bit initiates an interrupt request. The DATASET INT bit can be set by one of four other bits: CAR DET, CLR TO SEND, SEC REC, or RING.

When servicing an interrupt for one condition, if a second interrupt condition develops, a unique second interrupt, as well as all subsequent interrupts, may not occur. To prevent this, either all possible interrupt conditions should be checked after servicing one condition or both interrupt enable bits (bits 05 and 06) should be cleared upon entry to the service routine for vector XX0 and then set again at the end of service.

The interrupt priority level is 5 with the receiver having a slightly higher priority than the transmitter in all cases. Note that the priority level can be changed with a priority plug.

Any DEC programs or other software referring to the standard BR level or vector addresses must also be changed if the priority plug or vector address is changed.

3.4.6 Timing Considerations

When programming the DL11 Asynchronous Line Interface, it is important to consider timing of certain functions in order to use the system in the most efficient manner. Timing considerations for the receiver transmitter, and break generation logic are discussed in the following paragraphs.

3.4.6.1 Receiver – The RCVR DONE flag (bit 07 in the RCSR) sets when the Universal Asynchronous Receiver/Transmitter (UART) has assembled a full character. This occurs at the middle of the first STOP bit. Because the UART is double buffered, data remains valid until the next character is received and assembled. This permits one full character time for servicing the RCVR DONE flag.

3.4.6.2 Transmitter – The transmitter section of the UART is also double buffered. The XMIT RDY flag (bit 07 in the XCSR) is set after initialization. When the buffer (XBUF) is loaded with the first character from the bus, the flag clears but then sets again within a fraction of a bit time. A second character can then be loaded, which clears the flag again. The flag then remains cleared for nearly one full character time.

3.4.6.3 Break Generation Logic – When the BREAK bit (bit 00 in the XCSR) is set, it causes transmission of a continuous space. Because the XMIT RDY flag continues to function normally, the duration of a break can be timed by the pseudo-transmission of a number of characters. However, because the transmitter section of the UART is double buffered, a null character (all 0s) should precede transmission of the break to ensure that the previous character clears the line. In a similar manner, the final pseudo-transmitted character in the break should be null.

3.4.7 Program Notes

The following notes pertain to programming the DL11 interface and contain information that may be useful to the programmer. More detailed programming information is given in the *Paper Tape Software Programming Handbook*, DEC-11-GGPC-D and in the individual program listings.

- a. Character Format – The character format for the DL11 consists of a START bit, five to eight DATA bits, 1, 1.5, or 2 STOP bits and the option of PARITY (odd or even) or no parity. This is illustrated in Figure 12. Note that when less than eight DATA bits are used, the character must be right-justified to the least significant bit. The character format pertains to both the receiver and the transmitter.
- b. Maintenance Mode – The maintenance mode is selected by setting the MAINT bit (bit 02) in the XCSR. In this mode, the interface disables the normal input to the receiver and replaces it with the output of the transmitter. The programmer can then load various bits into the transmitter and read them back from the receiver to verify proper operation of the DL11 logic circuits.

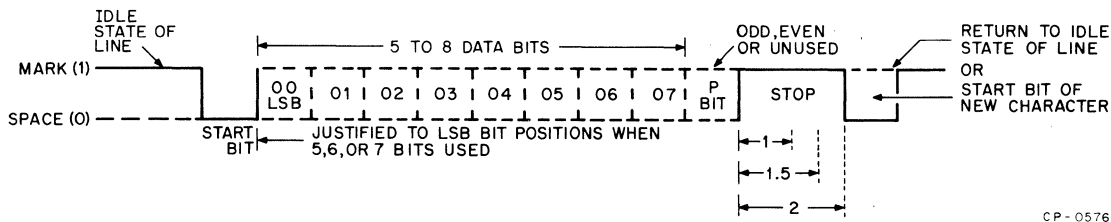


Figure 12 Serial Character Format

3.4.8 Program Example

Figure 13 is an example of a typical program that can be used as an echo program for a Type 103 dataset. When a remote terminal dials in, this program answers the call and provides a character-by-character echo. Characters are also copied onto the console device.

4.1 PROGRAMMING THE GT40/42

4.2 PROGRAMMING CONCEPT

The user should view the GT40/42 Graphic Display Terminal as two separate, programmed processors: a PDP-11/10 computer (CPU) and a special display processor (DPU). The PDP-11/10 is programmed to initiate the display, and is then free to execute its own program. All instructions available on the PDP-11/10 are executable in the GT40/42. Figure 14 shows the relationship of the GT40/42 components to the Unibus (the inset illustrates specific GT40/42 data flow via the Unibus).

The DPU communicates directly with the MM11 memory by way of non-processor requests (NPR), i.e., DMA requests. The PDP-11/10, connected in parallel, also uses the MM11 memory for executing its own PDP-11 code. The DPU executes display instructions stored in semi-contiguous memory locations called display lists. A memory layout example is shown in Figure 15. The Display Program Counter (DPC) in the DPU is addressed by the CPU, via the Unibus, and the data MOVED to the DPC becomes the starting address of the display list. All addresses placed on the Unibus are even numbers, i.e., word addresses.

```

000200 000200      ,#200
000200 000167 001616  START: JMP BEGIN ;JUMP TO BEGINNING OF PROGRAM

;SYMBOL DEFINITIONS

040000 RING# 040000 ;BIT 14 OF RCSR, RING
020000 CTS# 020000 ;BIT 13 OF RCSR, CLEAR TO SEND
000200 RDONE# 000200 ;BIT 07 OF RCSR, RECEIVER DONE
000002 DTR# 000002 ;BIT 01 OF RCSR, DATA TERMINAL READY
000200 XRDY# 000200 ;BIT 07 OF XCSR, TRANSMITTER READY

020000      ,#2000
020000 175610 RCSR# 175610 ;CSR OF RECEIVER
020002 175612 RBUF# 175612 ;BUF OF RECEIVER
002004 175614 XCSR# 175614 ;CSR OF TRANSMITTER
002006 175616 XBUF# 175616 ;BUF OF TRANSMITTER
002010 177564 CXCSR# 177564 ;CSR OF CONSOLE TRANSMITTER
002012 177566 CXBUF# 177566 ;BUF OF CONSOLE TRANSMITTER
002014 000000 BUFFER# 0 ;HOLDS CHARACTER RECEIVED
002016 000000 DELAY# 0 ;HOLDS DELAY COUNT, HIGH ORDER
002020 000000      ? ;HOLDS DELAY COUNT, LOW ORDER

;BEGINNING OF ECHO PROGRAM

002022 005077 177752 BEGIN: CLR @RCSR ;START BY INITIALIZING ALL BITS TO ZERO

002026 032777 040000 177744 LOOP1: BIT #RING,@RCSR ;CHECK FOR INCOMING CALL
002034 001774 BEQ #1,DELAY+2 ;BRANCH IF PHONE IS NOT RINGING
002036 052777 000002 177734 BIS #DTR,@RCSR ;PHONE IS RINGING, SO ANSWER WITH DTR
002044 012767 000005 177744 MOV #5,DELAY ;SET UP COUNT FOR DELAY

002052 032777 020000 177720 LOOP2: BIT #CTS,@RCSR ;CHECK FOR CLEAR TO SEND
002060 001007 BNE LOOP3 ;BRANCH IF ON
002062 162767 000001 177730 SUB #1,DELAY+2 ;CHECK DELAY
002070 005667 177722 SBC DELAY ;DECREMENT A TWO-WORD INTEGER
002074 001752 BEQ BEGIN ;BRANCH IF WE HAVE WAITED TOO LONG
002076 000765 BR LOOP2 ;BRANCH AND CONTINUE TO WAIT FOR CTS

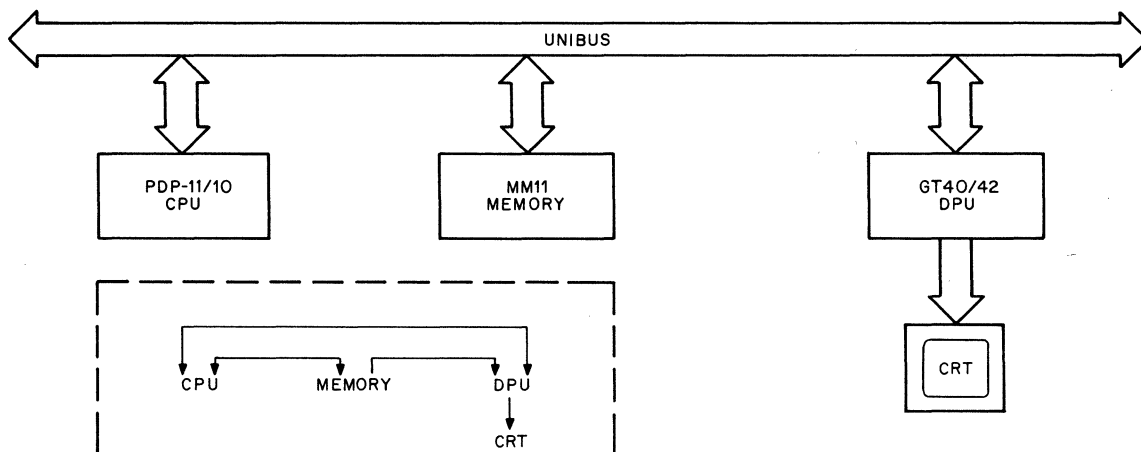
002100 032777 020000 177672 LOOP3: BIT #CTS,@RCSR ;IS CHANNEL STILL ESTABLISHED?
002106 001745 BEQ BEGIN ;BRANCH IF CTS NOT PRESENT
002110 032777 000200 177662 BIT #RDONE,@RCSR ;CHECK FOR RECEIVED CHARACTER
002116 001770 BEQ LOOP3 ;BRANCH IF NO CHARACTER RECEIVED
002120 017767 177656 177666 MOV @RBUF,BUFFER ;READ RECEIVED CHARACTER INTO BUFFER

002126 032777 000200 177650 LOOP4: BIT #XRDY,@XCSR ;CHECK FOR TRANSMITTER READY
002134 001774 BEQ LOOP4 ;BRANCH IF NOT READY
002136 016777 177652 177642 MOV BUFFER,@XBUF ;TRANSMIT CHARACTER TO REMOTE TERMINAL

002144 032777 000200 177636 LOOP5: BIT #XRDY,@CXCSR ;CHECK FOR CONSOLE TRANSMITTER READY
002152 001774 BEQ LOOP5 ;BRANCH IF NOT READY
002154 016777 177634 177630 MOV BUFFER,@CXBUF ;TRANSMIT CHARACTER TO CONSOLE
002162 000746 BR LOOP5 ;BRANCH AND WAIT FOR NEXT CHARACTER

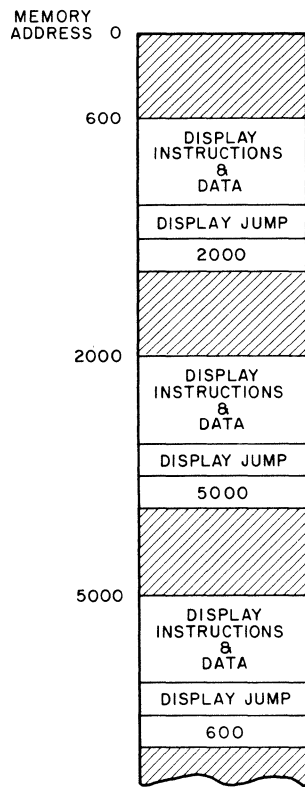
```

Figure 13 Program Example



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Figure 14 GT40/42 Data Paths



Shown are three "lists" of display instructions and data chained together by Display Jump instructions into one, closed display file. The shaded memory areas can be used by the CPU for PDP-11 code, data, buffer registers, etc.

CP-0653

Figure 15 Memory Layout Example

4.3 IMPORTANT REGISTERS (all addresses are in octal)

Display Addresses:

Display Program Counter (DPC) = 172000 (Read/Write)
 Resume Address (RA) = 172000 (Write)

(To resume a display, for example after a light pen hit, bit 0 (LSB) = 1 should be MOVed to the RA, i.e.,
 MOV #1, RA.)

Display Status Register = 172002 (Read/Write)

Contents (Read):

Stop Flag	Bit	(15) (MSB)
Mode		(14:11)
Intensity		(10:8)
Light Pen Flag		(7)
Shift Out		(6)
Edge Indicator		(5)
Italics		(4)
Blink		(3)
Spare (Not Used)		(2)
Line		(1:0)

(If an attempt is made to write to address 172002, the effect is to ring the BELL in the GT40/42, e.g.,
 MOV #2, 172002.)

X Status Register = 172004 (Read only)

Contents:
X Position Bits (9:0)
Graphplot Increment (15:10)

Y Status Register = 172006 (Read only)

Contents:
Y Position Bits (9:0)
Character Register (15:10)

(Note: When in the SHIFTED OUT character mode, and an illegal code (040 → 137₈) is fetched, the program is interrupted. The Character Register can then be read to find the dispatch to a user routine that is used to draw some special character.)

Display Interrupt Vector Addresses:

Stop Interrupt = 320/322
Light Pen Interrupt = 324/326
Time Out and Shift Out Interrupt = 330/332
(All display interrupts are requested at level BR4.)

DL11 Communications Interface Addresses:

Receive Status Register (RCSR) = 175610
Receive Buffer (RBUF) = 175612
Transmitter Status Register (XCSR) = 175614
Transmitter Buffer (XBUF) = 175616
(Additional DL11 programming information is included in Paragraph 3.1.)

DL11 Interrupt Vector Addresses:

Receiver Interrupt = 300/302
Transmitter Interrupt = 304/306
(DL11 interrupts are requested on level BR5.)

Miscellaneous Addresses:

CPU General Register R0 = 177700
(only console addressable) R7 = 177707

CPU Console Switches SWR = 177570
(console and CPU addressable)

CPU Status PS = 177776
(console and CPU addressable)

Keyboard Command and Status (KCSR) = 177560

Keyboard Data Buffer (KDBR) = 177562

Keyboard Interrupt Vector = 60/62

Line Frequency Clock (KW11-L) = 177546

ROM Bootstrap Memory = 166000
(Starting Address)

4.4 PDP-11 INSTRUCTION SET

A detailed description of the PDP-11 instruction set can be found in *GT40 Graphic Display Terminal, Volume 2* (DEC-11-HGTMA-A-D). This manual assumes the reader is familiar with the instruction set and general operation of the PDP-11/10.

4.5 GT40/42 DISPLAY PROCESSOR INSTRUCTION SET

The display processor instruction set consists of five basic instructions: Set Graphic Mode, Jump, No-op, Load Status Register A, and Load Status Register B. Figure 16 shows the breakdown, by bit position, of each instruction. Figure 17 provides similar information for the data words that accompany the instructions.

NOTE

The user should not insert 1-bits into those positions indicated as spare or unused.

4.6 PROGRAMMING EXAMPLES

The following programming examples are meant to provide the user with a basic introduction to GT40/42 programming technique. They have been kept brief in order that the points being illustrated not be lost as would be the case if larger, operational program examples were used.

Table 8 is a list of suggested mnemonics for GT40/42 operation.

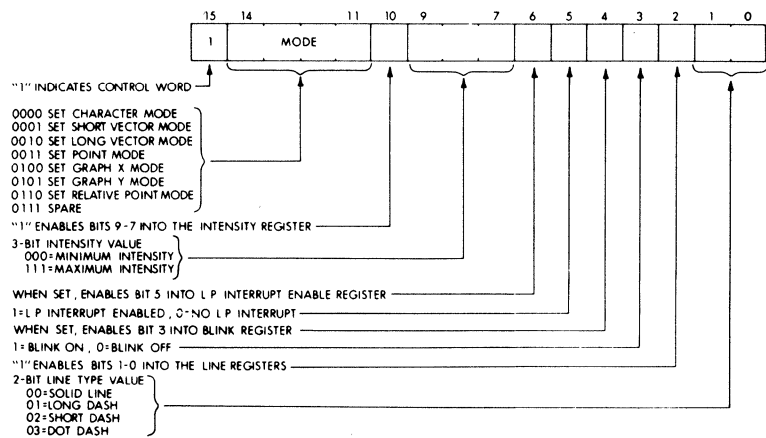
4.6.1 Initializing the Display Processor

To start the DPU, the CPU executes a short program that loads the Display (processor) Program Counter (DPC) with the starting address (SA) of the display file. The Stack Pointer must also be initialized to an address above 400₈ to prevent a stack overflow if an interrupt occurs.

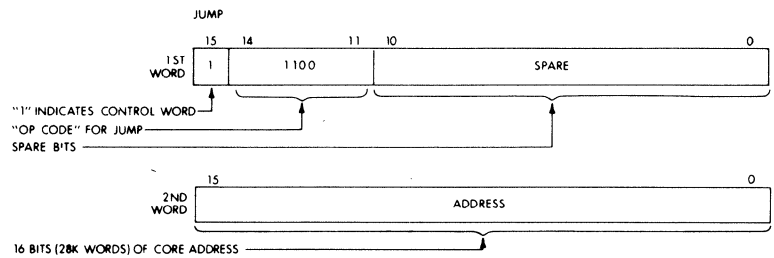
The following program performs these two operations.

Address	Instruction/Data	Mnemonic	Comment
1000	012706	MOV #500, R6	Initialize the
1002	500		stack pointer
1004	012737	MOV #SA, @ #DPC	Load the DPC
1006	2000		with SA = 2000
1010	172000		
1012	00001	WAIT	Wait (or other PDP-11 code)

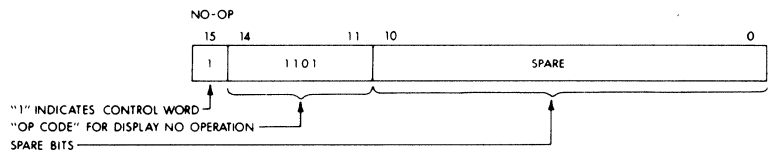
SET GRAPHIC MODE



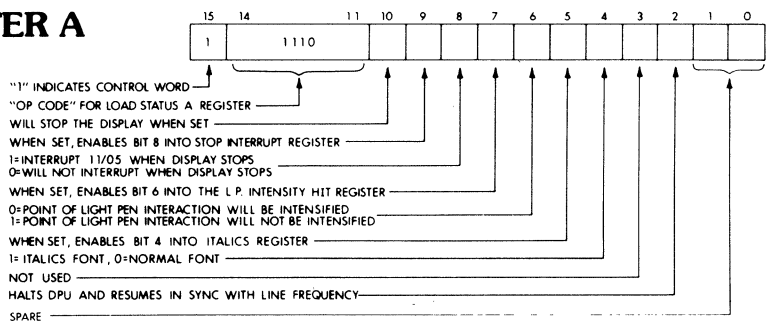
JUMP



NO-OP



LOAD STATUS REGISTER A



LOAD STATUS REGISTER B

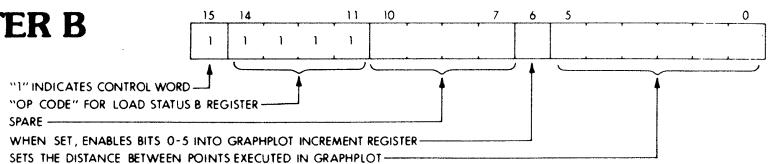
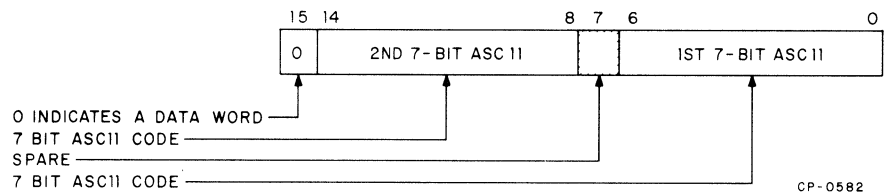
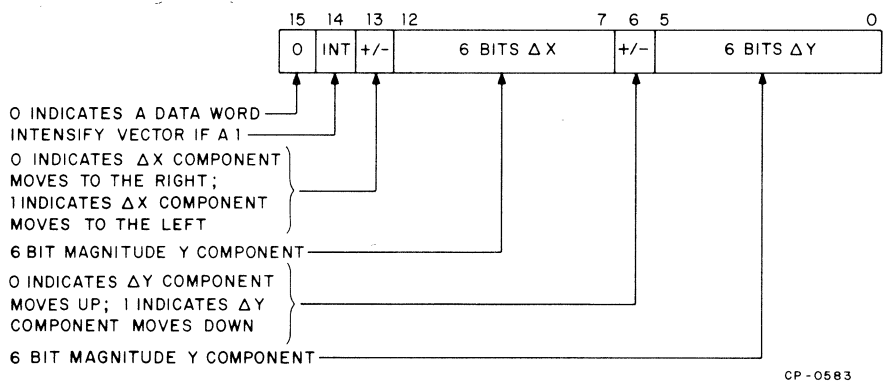


Figure 16 Instruction Word Functions

**CHARACTER
DATA FORMAT-
Mode 0000**



**SHORT
VECTOR MODE-
Mode 0001**



**LONG VECTOR
DATA FORMAT-
0010**

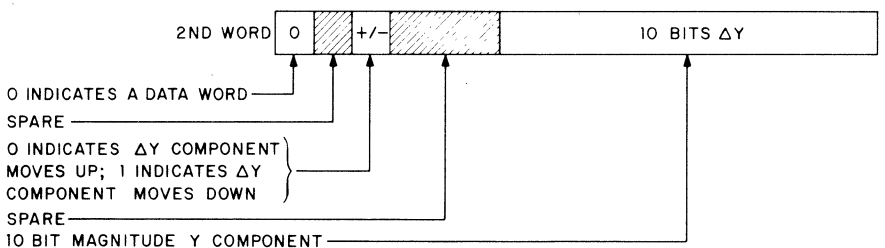
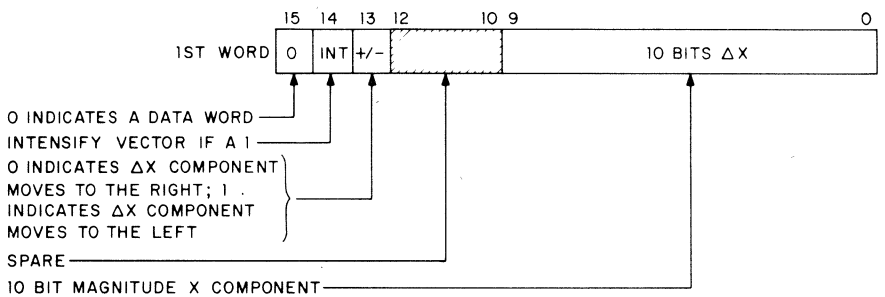
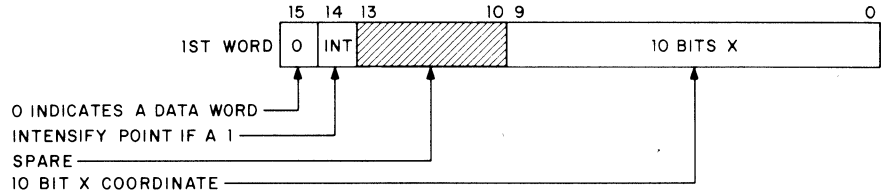
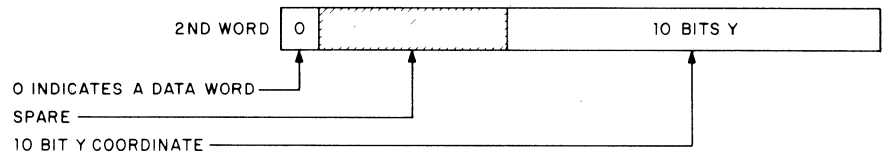


Figure 17 Data Word Formats (Sheet 1 of 2)

**POINT DATA
MODE-
Mode 0011**

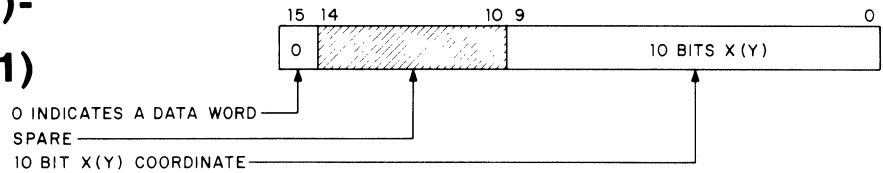


CP-0543



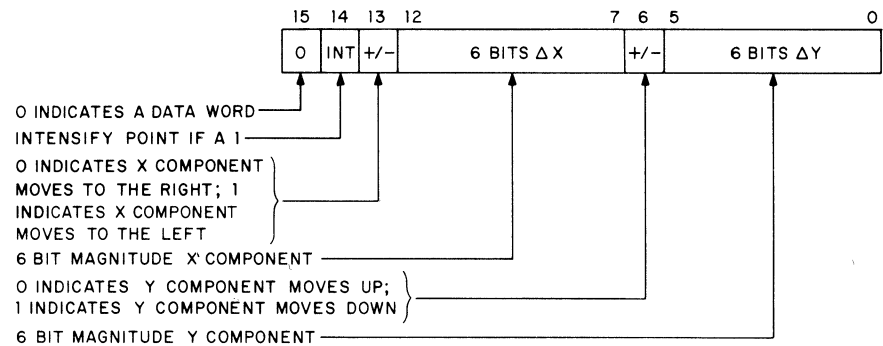
CP-0544

**GRAPHPLOT X(Y)-
Mode 0100 (0101)**



CP-0545

**RELATIVE
POINT MODE-
Mode 0110**



CP-0546

Figure 17 Data Word Formats (Sheet 2 of 2)

Table 8
Recommended GT40/42 Mnemonics

Mnemonic = Value				Function
Group 1				
	CHAR	=	100000	Character Mode
	SHORTV	=	104000	Short Vector Mode
	LONGV	=	110000	Long Vector Mode
	POINT	=	114000	Point Mode
	GRAPHX	=	120000	Graphplot X Mode
	GRAPHY	=	124000	Graphplot Y Mode
	RELATV	=	130000	Relative Point Mode
	INT0	=	2000	Intensity 0 (Dimmest)
	INT1	=	2200	Intensity 1
	INT2	=	2400	Intensity 2
	INT3	=	2600	Intensity 3
	INT4	=	3000	Intensity 4
	INT5	=	3200	Intensity 5
	INT6	=	3400	Intensity 6
	INT7	=	3600	Intensity 7 (Brightest)
	LPOFF	=	100	Light Pen Off
	LPON	=	140	Light Pen On
	BLKOFF	=	20	Blink Off
	BLKON	=	30	Blink On
	LINE0	=	4	Solid Line
	LINE1	=	5	Long Dash
	LINE2	=	6	Short Dash
	LINE3	=	7	Dot Dash
Group 2				
	DJMP	=	160000	Display Jump
Group 3				
	DNOP	=	164000	Display No Operation
Group 4				
	STATSA	=	170000	Load Status A Instruction
	DSTOP	=	173400	Display Stop and Interrupt
	SINON	=	1400	Stop Interrupt On
	SINOF	=	1000	Stop Interrupt Off

Table 8 (Cont)
Recommended GT40/42 Mnemonics

Mnemonic = Value			Function
	LPLITE	= 200	Light Pen Hit On
	LPDARK	= 300	Light Pen Hit Off
	ITAL0	= 40	Italics Off
	ITAL1	= 60	Italics On
	SYNC	= 4	Halt and Resume in Sync
Group 5			
	STATSB	= 174000	Load Status B Instruction
	INCR	= 100	Graphplot Increment
Group 6 (Vector/Point Mode)			
	INTX	= 40000	Intensify Vector or Point
	MAXX	= 1777	Maximum Δ X Component
	MAXY	= 1377	Maximum Δ Y Component
	MINUSX	= 20000	Negative Δ X Component
	MINUSY	= 20000	Negative Δ Y Component
Group 7 (Short Vector Mode)			
	MAXSX	= 17600	Maximum Δ X Component
	MAXSY	= 77	Maximum Δ Y Component
	MISVX	= 20000	Negative Δ X Component
	MISVY	= 100	Negative Δ Y Component

4.6.2 Display File

The following program causes a 200_8 unit box to be drawn with the lower left corner at screen location $500,500_8$. Initially, the DPC is loaded with the starting address. Then the display parameters, e.g., intensity, are established and the mode set to Point. The four vectors are drawn after the Point is executed and, to conclude the file, the last commands reload the DPC with the display file starting address. This results in the display file being re-executed; the CRT display is refreshed.

Address	Instruction/Data	Mnemonic	Comment
		. = 100	
100	012706	MOV #500, R6	Initialize the
102	500		stack pointer
104	012737	MOV #2000, @ #DPC	Load the DPC
106	2000		with SA = 2000
110	172000		
112	000001	WAIT	Wait
2000	117124	. = 2000	Point mode, intensity
		POINT+INT4+LPOFF	4, no light pen, no
		+BLKOFF+LINED	blink, solid lines.
2002	500	500	Unintensified point
2004	500	500	at X = 500, Y = 500
2006	110000	LONGV	Long vector mode
2010	40200	200+INTX	$\Delta X = 200, \Delta Y = 0,$
2012	0	0	intensified
2014	40000	0+INTX	$\Delta X = 0, \Delta Y = 200,$
2016	200	200	intensified
2020	60200	200+INTX+MINUS	$\Delta X = -200, \Delta Y = 0,$
2022	0	0	intensified
2024	40000	0+INTX	$\Delta X = 0, \Delta Y = -200,$
2026	20200	200+MINUS	intensified
2030	160000	DJMP	Jump to start of
2032	2000	2000	display file.

Note that since the parameters (intensity level, no blink, and line type) are specified in the point instruction, they need not be re-specified in the long vector instruction (2006) because they will not change unless the appropriate enable bits are set. The enable bits also allow the user to change, for example, the line type but not the intensity. In this case, only the line type enable bit is changed, not the intensity enable bit. This retention of current, not-to-be-changed, values saves both execution time and memory storage space.

4.6.3 Application of the Stop Interrupt

The Stop Interrupt provides close interaction between the CPU and the DPU. The following program restarts the display after the halt and interrupt sequence. This occurs at the end of each pass.

Address	Instruction/Data	Mnemonic	Comment
		. = 100	
100	012706	MOV #500, R6	Initialize the
102	500		stack pointer
104	012737	MOV #2000, @ #DPC	Load the DPC with
106	2000		SA = 2000
110	172000		
112	000001	WAIT	Wait for interrupt
114	776	BR.- 2	Jump back one
		. = 320	instruction
320	400	400	Address of next
			instruction to be
			executed after a
			Stop interrupt
322	200	200	Processor status
		. = 400	(BR level 4)
400	012737	MOV #1, @ #DPC	Resume the display

Address	Instruction/Data	Mnemonic	Comment
402	01		
404	172000		
406	02	RTI	Return from interrupt
2000	117124	.=2000 POINT+INT4+LPOFF +BLKOFF+LINED	Point mode, intensity 4, no light pen, no blink, solid lines.
2002	500	500	Unintensified point
2004	500	500	at X = 500, Y = 500
2006	110000	LONGV	Long vector mode
2010	40200	200+INTX	$\Delta X = 200, \Delta Y = 0,$
2012	0	0	intensified
2014	40000	0+INTX	$\Delta X = 0, \Delta Y = 200,$
2016	200	200	intensified
2020	60200	200+INTX+MINUS	$\Delta X = -200, \Delta Y = 0,$
2022	0	0	intensified
2024	40000	0+INTX	$\Delta X = 0, \Delta Y = -200$
2026	20200	200+MINUS	intensified
2030	173400	DSTOP	Enable Stop interrupt, Stop
2032	160000	DJMP	Jump to start of
2034	2000	2000	display file after a Resume

After initializing the DPU, the CPU WAITs for an interrupt. The DPU executes the display file, eventually performing the STOP with interrupt enabled. This causes a vectored interrupt to address 320₈.

Since the Stack Pointer was initialized to 500₈, the CPU stores its processor status and program counter in location 500₈ and 476₈ respectively; it pushes them on the "stack." Once stored, the CPU goes to location 320₈ and uses its contents as the address of the interrupt routine. The CPU takes the contents of location 322₈ as its new processor status. In this example, location 400₈ is the address of the interrupt handler and the CPU proceeds to that location.

The interrupt handler simply MOVes the number 1 to the DPC which is interpreted as a RESUME by the DPU. As the DPU resumes operation, it will fetch and interpret the next instruction after stopping, in this case a DJMP, back to the start of the display file. The final instruction of the interrupt handler is a Return from Interrupt (RTI), restoring the CPU to the status and location present before the interrupt, i.e., it pops two words off the stack. A computer branch back one instruction is executed, thus placing the CPU in a WAIT condition again.

4.7 PROGRAMMING RESTRICTIONS

As with any complex system, certain restrictions must be observed by the user if trouble-free operation is to be expected. In the case of the GT40/42, the programmer should be aware of certain programming limitations so that the hardware may be exercised more proficiently without violating hardware rules.

4.7.1 Stop and Sync, Microcoding

Stop and Sync appear in the Load Status A instruction. However, selection of both conditions in any given Load Status A instruction should be avoided. Priorities have been built into the GT40/42 hardware concerning the action on the microcoding of these bits. The rules are as follows:

1. Sync and Stop
Sync will override Stop. The display will stop but will resume in sync with the line frequency.

2. Stop and Sync with Stop Interrupt Enabled

Setting Stop with the Stop Interrupt enabled and Sync must be avoided. Under these conditions, the DPU will stop, post an interrupt, and restart automatically in sync with the line frequency. Since the Sync resume happens rather randomly with respect to the interrupt, the effect of this microcoding is undetermined.

4.7.2 Display File Changes

Restarting a Running Display – Restarting the DPU while the DPU is running should be avoided. It is possible to “catch” the DPU in the middle of a bus operation causing inconsistent or undetermined operation.

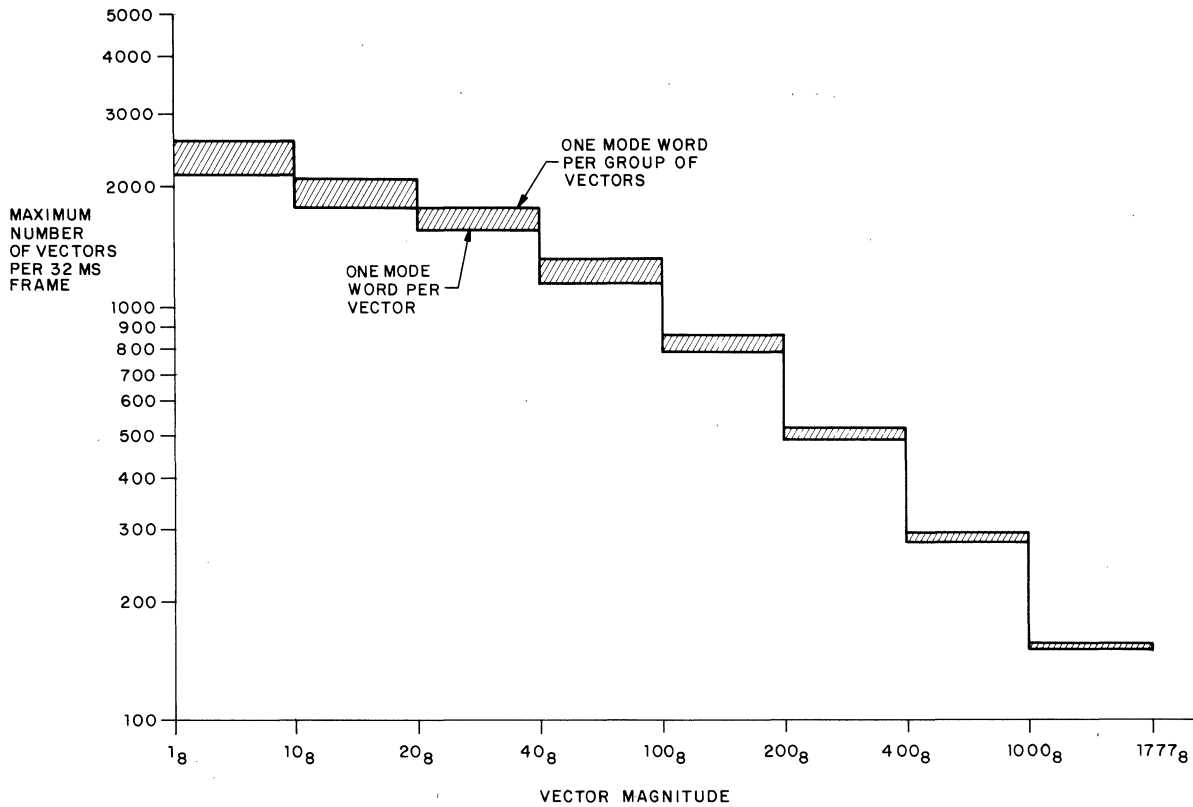
It is recommended that the DPU be halted with a Stop instruction before restarting it again.

Modification of the File – Dynamic modification of the display file should be avoided when possible. Normally the file can be modified dynamically without consequence. However, it is possible to cause problems when modifying two word instructions such as a Display Jump. For example, if the DPU fetched the first part of a DJMP while the CPU modified the second word, the DPU will process the DJMP order code and will take the modified second word as a correct address, causing the DPU to branch to a non-intended address. It is recommended that the DPU be halted before modifying the display file and that care be exercised in selecting the sequence of commands used to modify the file.

4.7.3 Non-Flicker Display

The quality of the image displayed on the screen is determined by many factors. Primarily, the display is controlled by internal adjustments (contrast, focus, etc.) and the external BRIGHTNESS control on the front panel. However, programming is also instrumental in producing better image quality. The selectable brightness feature, one of the display parameters controlled by the Set Graphic Mode instruction, is one example of the role that programming plays. Another is the control of image flicker, the repetitive dimming and brightening of all vectors and characters on the screen. Flicker, in this case, is caused by a relatively long program execution time, i.e., the time from the beginning of the display frame until the program recycles and the display is repeated. If this time is longer than about 1/30 of a second the screen fluorescence will decay (the image will become dimmer), and then brighten when the next frame begins, to the point where flicker is apparent. When the program time is less than 1/30 second, the display is reintensified before the image dims noticeably and there is no apparent flicker. Consequently, the objective, from a programming standpoint, is not to exceed this (1/30 second) execution period when designing a display program.

Program time, as defined above, and where vectors make up most of the display, is primarily determined by two factors: vector magnitude or length, and the number of vectors in the display frame. The longer the vectors and the greater the number of vectors the longer the display frame will be. Figure 18 shows the allowable limits, considering these two factors, for a flickerless display, defined here as display frames ≤ 32 ms (about 1/30 second). Note that a third factor is also present: the vector to mode word ratio. If this is a 1:1 ratio, then fewer vectors are allowed because the mode word itself requires time to be decoded – time that must be subtracted from the 32 ms period. However, this time is more efficiently used when the ratio increases, i.e., when a mode word is accompanied by a number of vectors; the total number of allowable vectors is increased. This is shown in Figure 18 as the shaded area for each vector length with the top line being the practical limit. If vector lengths vary, as is usually the case, the total number of each length must be taken into account; the aggregate must not cause the frame time to exceed 32 ms.



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Figure 18 Non-Flicker Display as Determined by Vector Quantity and Magnitude

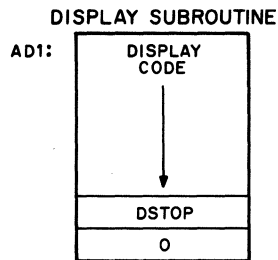
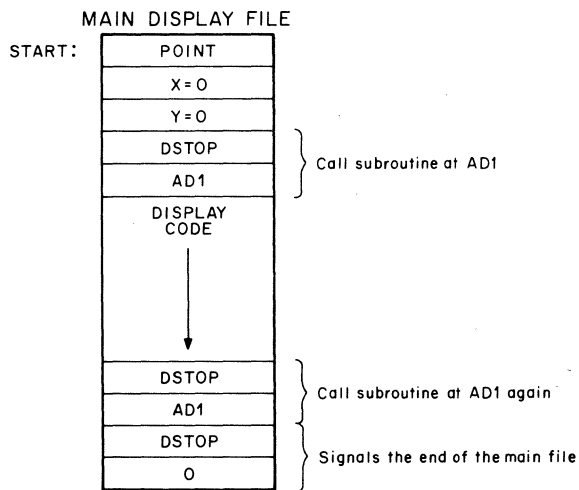
4.8 ADVANCED PROGRAMMING TECHNIQUES

4.8.1 Subroutines

This programming method is used when a section of display code is repeated a number of times during the execution of a display file. It precludes the need to store multiple copies of the routine in memory and therefore makes more efficient use of available storage space. Writing effective display subroutines is accomplished through use of the stop interrupt instruction (DSTOP) followed by an identifier that informs the interrupt service routine what to do or where to go. Figure 19 shows an example of how a display subroutine can be repeatedly called by the main display file. An example of an interrupt service routine is shown below. It is assumed that register R5 is used for the subroutine stack. STKST is the starting location for the subroutine stack.

Mnemonic	Comment
STPINT: TST @ DPC	Test the DPC
BEQ STOPO	If it contains a valid, non-zero address go to the next instruction; if not go to STOPO
MOV DPC, -(R5)	Push current DPC on stack
ADD #2, @R5	The stack now contains the return address from the subroutine.

	Mnemonic	Comment
	MOV @ DPC, DPC	Move address pointed to by DPC into the DPC, i.e., go to the subroutine.
	RTI	Exit
STOP0:	CMP R5, STKST	Is the subroutine stack empty?
	BEQ TOP	Yes, go to top of file
	MOV (R5)+, DPC	No, pop off a word and go there
	RTI	Exit
TOP:	MOV #START, DPC	Restart at TOP
	RTI	and exit



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Figure 19 Subroutining Example

4.8.2 Light Pen Interaction

The DPU is stopped when a light pen "hit" occurs during the display of a vector, character, or point, provided light pen interrupts are permitted (bits 5 and 6 of the Set Graphic Mode word must both be true to enable the LP interrupt function).

Priorities permitting, the LP hit interrupts the PDP-11. The interrupt service routine that is called in as a result of the LP interrupt has access to three data in the DPU (the data can be read by specifying the addresses indicated):

- Display Program Counter (DPC) Addr = 172000. Points to the instruction/data word following the data word on which the LP hit occurred.
- The X position of the display at the time the DPU stopped, Addr = 172004. A 10-bit absolute number.
- The Y position of the display at the time the DPU stopped, Addr = 172006. A 10-bit absolute number.

The service routine can respond to the LP interrupt by restarting the display in one of two ways:

- Resume the display – the operation in progress at the time of the interrupt is allowed to continue. Program example: MOV #1, DPC
- Restart the display – the operation in progress at the time of the interrupt is abandoned and a new display program routine is initiated. Program example: MOV #SA, DPC

4.8.3 Special Characters

The 31 special characters in the GT40/42 display character set are addressed through use of ASCII codes Shift Out (016_8) and Shift In (017_8).

When the DPU detects the character code 016_8 , the hardware enters the shift mode. In this mode codes 000 through 037_8 are decoded as special characters. (Appendix C contains a list of GT40/42 character codes.) Note that when the DPU is in the shift mode, the Shift Out code (016_8) itself is a legitimate printing character. The DPU is returned to the non-special character ASCII set (non-shift mode) when Shift In is decoded. Unlike the Shift Out code, the Shift In code (017_8) does not cause a special character to be displayed. If, when in the shift mode, the DPU detects a code $\geq 040_8$, the PDP-11 is interrupted by a Shift In/Time Out interrupt vector. This is because only the special characters (codes 000 through 037_8) are legal when in the shift mode. The PDP-11 now has access to the 6 low order bits of the 7-bit illegal code. These 6 bits could be used, for example, as an index to a table of software generated characters.

4.8.4 Edge Violations

An edge violation occurs if either the X or Y coordinate indicated for a relative display causes the display to go outside the physical limits of the CRT face. (Vectors, relative points, characters, and Graphplots are classified as relative type displays.) In the event of an edge violation, the edge flag in the status word is set and the display is clipped (terminated) at the edge of the screen; wrap-around does not take place. However, there is one exception in which wrap-around can occur. The GT40/42 hardware is capable of counting only up to 4095_{10} , i.e., 12 bits. Therefore, if the vector position exceeds this 12-bit limit, the count overflows to 0 and wrap-around occurs. For example, if four consecutive vectors with the same coordinates ($\Delta X = 1023$, $\Delta Y = 1$) are read, only the first vector is displayed; it is the only one that can be displayed within the physical address space. The other three vectors cause the count to legally exceed the 12-bit field. If a fifth vector, with the coordinates of $\Delta X = 10$ and $\Delta Y = 0$, is decoded, the vector will appear on the left of the display; the hardware has caused the display to wrap around. This relative X and Y counting is performed in a 12-bit circular fashion. Absolute points are limited to 10-bit addressing.

5.1 COMMUNICATIONS BOOTSTRAP READ-ONLY MEMORY (ROM)

The communications bootstrap ROM in the GT40 and the GT42 connects the Graphic Display Terminal to a host computer by way of the DL11 Asynchronous Line Interface. Two functions are performed:

1. The program allows ASCII dialogue with the host computer in order to perform such functions as logging in, etc., which presumably leads to
2. The ability to load the Graphic Display Terminal's core memory with an absolute PDP-11 program. This function is typically called a down-line load.

The ROM Bootstrap program is stored in a bipolar ROM contained in the display processor (M7014 module). The memory is assigned addresses starting at 166000_8 and is accessed via the Unibus and the display processor addressing hardware. Although physically located in the display processor, the communications ROM should be considered a separate, Unibus connected, memory device. In the GT40, the ROM contains 256 words; in the GT42, the ROM contains 512 words.

Appendix D contains a program listing of the ROM Bootstrap for the GT40 and Figure D-1 is a flow diagram for the program. Appendix E contains a program listing of the ROM Bootstrap for the GT42 and Figure E-1 is a flow diagram for the program.

5.1.1 Bootstrap Loader

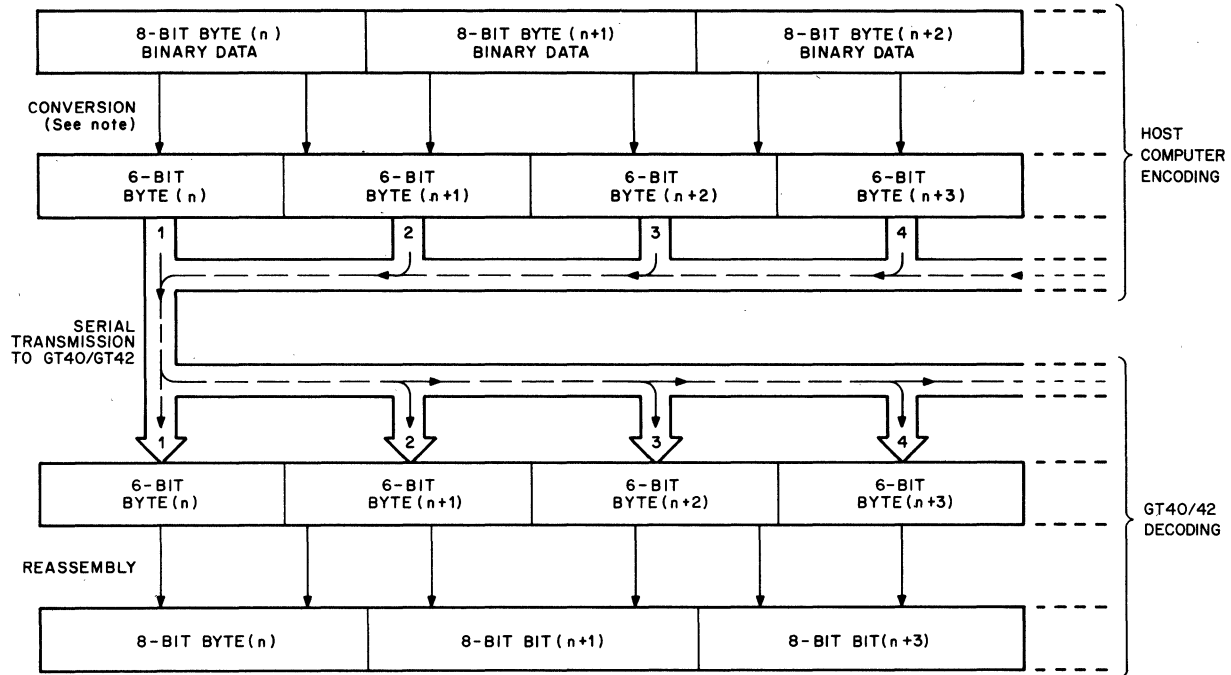
The communications down-line loader portion of the Bootstrap allows loading programs in all memory locations except for the absolute addresses 15700 through 15776_8 , which are used by the loader itself. If the user finds this restriction unacceptable, it is possible to reassemble a copy of the Bootstrap program with the tag COREND equal to the highest address in the user's memory, e.g., $\text{COREND} = 57776_8$ for a 12K memory. The procedure then is to load this modified Bootstrap first and then the user's program.

The loader will accept properly encoded ASCII strings and effect the loading of a PDP-11 absolute program. The encoding and decoding scheme is shown pictorially in Figure 20.

The loading procedure, from the host computer, is presented below in brief terms:

1. Initiate the Bootstrap by placing 166000 in the SR switches; press LOAD ADDRESS and START.
2. Transmit } (175_8) and then R (122_8) to reset the Bootstrap.
3. Transmit } (175_8) and then L (114_8) to start the Loader.
4. Transmit encoded characters representing the binary program to be loaded.
5. If a checksum error occurs during a load, B (102_8) and } (175_8) will be returned.
6. If the program loads but does not self-start, G (107_8) and } (175_8) are returned.
7. There is no return if the program is properly loaded and started.

To enable synchronization of the loader at high transfer rates, the host computer should transmit filler characters after step 3 above. These fillers should be nulls in multiples of three, as indicated in Figure 21. The @ symbol (100_8) is transmitted because 100_8 is added to all characters less than 040_8 ; therefore, null (000) + $100_8 = 100_8$. The filler requirement is satisfied by six nulls, i.e., eight @ symbols.



NOTE:
 If 6-Bit number $x < 40_8$ then $x = x + 100_8$; if 6-Bit number $x \geq 40_8$ then $x = x$. The resulting 6-Bit codes are 040_8 through 137_8 ; all are printable characters and symbols. They are serially transmitted in sequential order, until the end of the PDP-11 program, to the GT40 where they are reassembled into their 8-Bit binary format.

CP-0650

Figure 20 Encoding and Decoding of Serial Data

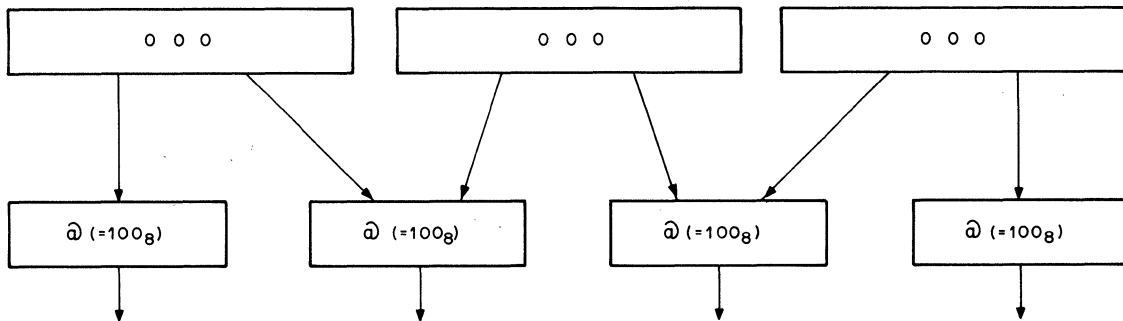
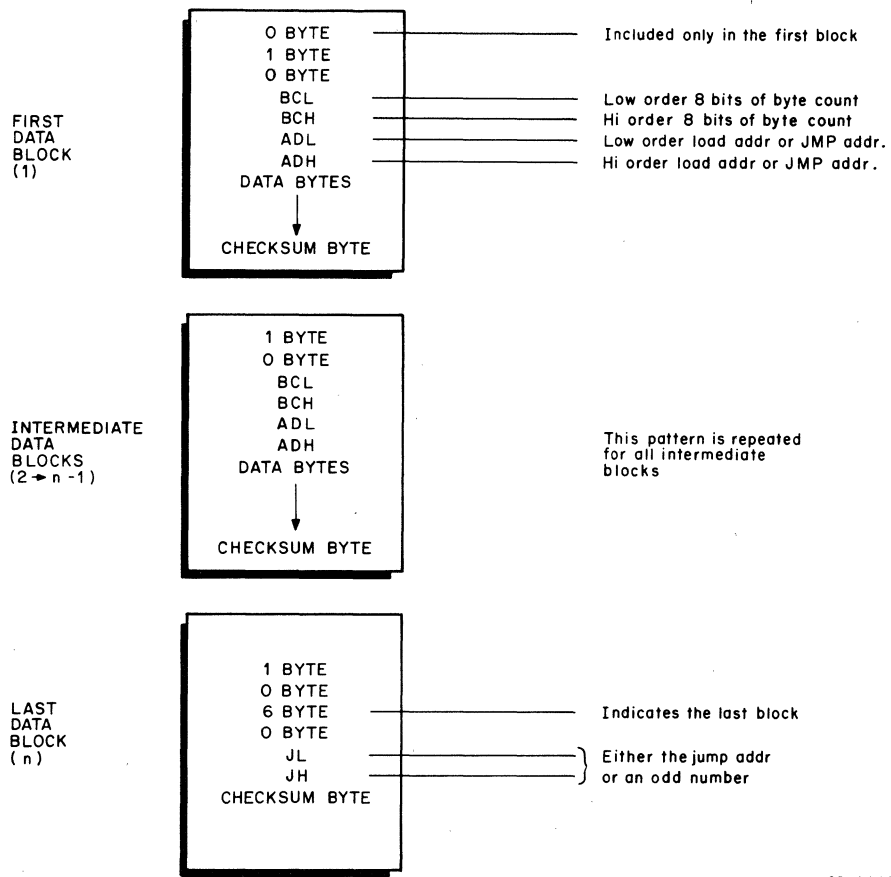


Figure 21 Filler Character Transmission to the GT40/42

It is necessary to preface the first "one" byte in the absolute program with a "zero" byte in order to save Bootstrap code. A normal absolute program, in octal, before encoding into the 6-bit tape format, is transmitted in the order shown in Figure 22. An example of a short program (in octal) and the resultant encoded characters transmitted are shown in Figure 23.



CP-0648

Figure 22 Absolute Program, Octal Format

5.1.2 Character Echoing

When not running in the LOADER mode, the Bootstrap allows the GT40/42 to communicate with the host computer in ASCII. Depressing a key on the LK40 keyboard at this time causes the ASCII character for that key to be sent to the host computer. If the host computer echoes the character, it will appear on the GT40/42 display (providing it is printable).

In reference to this type of display, several characteristics should be noted:

- The GT40 Bootstrap does not scroll. If the initial dialogue runs off the bottom of the screen, the operator must again depress START; the dialogue will then return to the top of the screen. In the GT42, the dialogue appears at the bottom of the screen and scrolls off the top when the screen is full.
- With the exception of 175₈ characters with codes of from 040₈ through 176₈ will be displayed on the screen. Code 175₈ is used to initiate restarting and loading of the GT40/42.
- In the GT40 the only control characters which affect the display are CARRIAGE RETURN, LINE FEED, and BACKSPACE. TAB, FORM FEED, etc. are not understood. In the GT42, TAB and FORM FEED characters are understood.
- The host computer should not send SHIFT OUT (016₈) because this character causes the GT40/42 hardware to generate a special character set. (This restriction applies only to the Bootstrap because of space limitations in this program. Normally the software would monitor all characters before inserting them into the display file.)

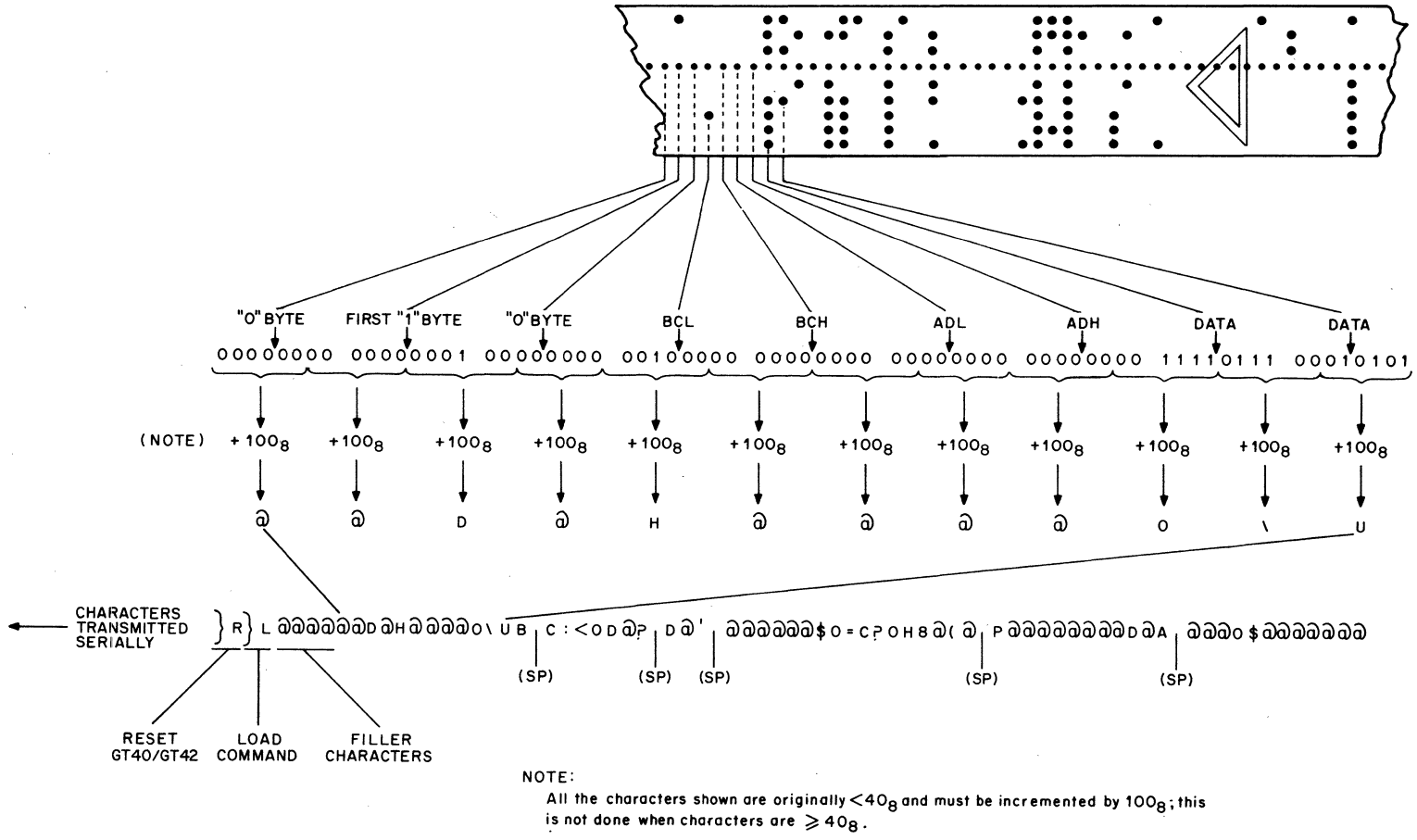
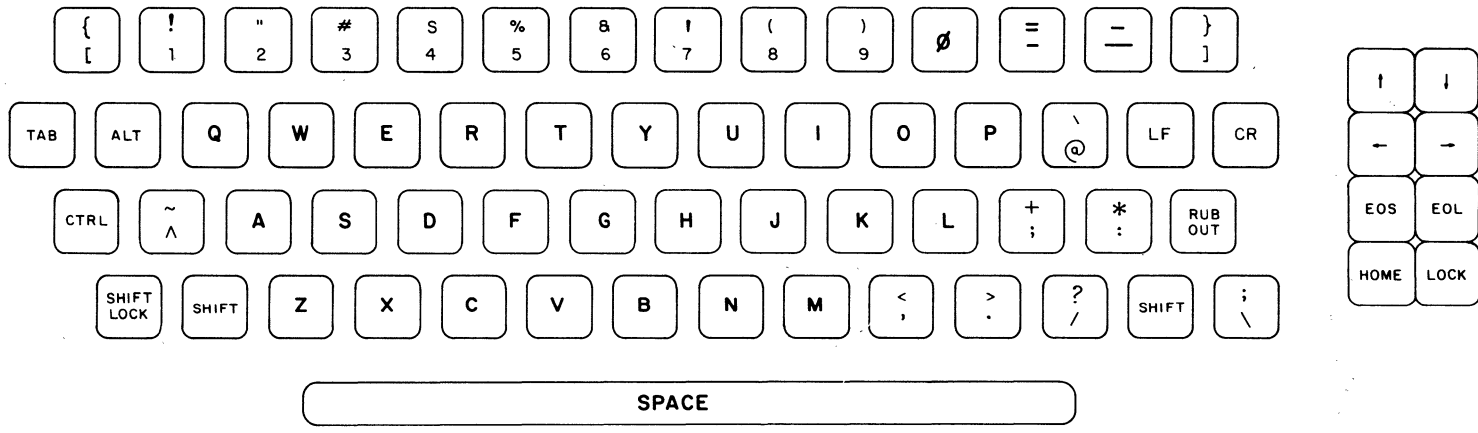


Figure 23 Absolute Program Conversion and Transmission

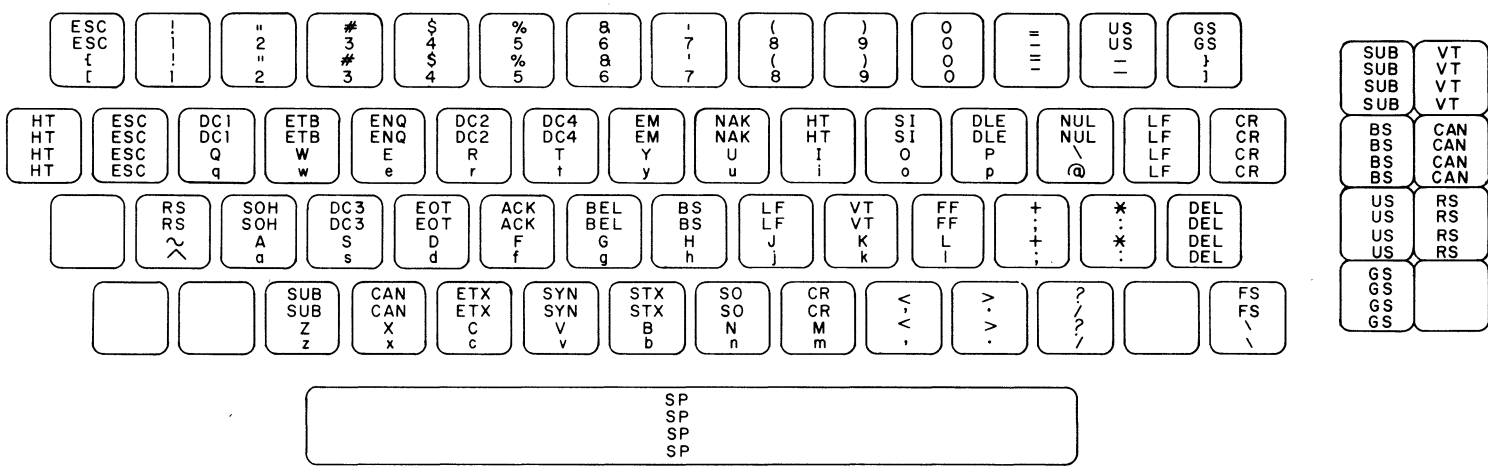
**APPENDIX A
KEY BOARD LAYOUT**



CP-0607

Figure A-1 Keyboard Key Configuration

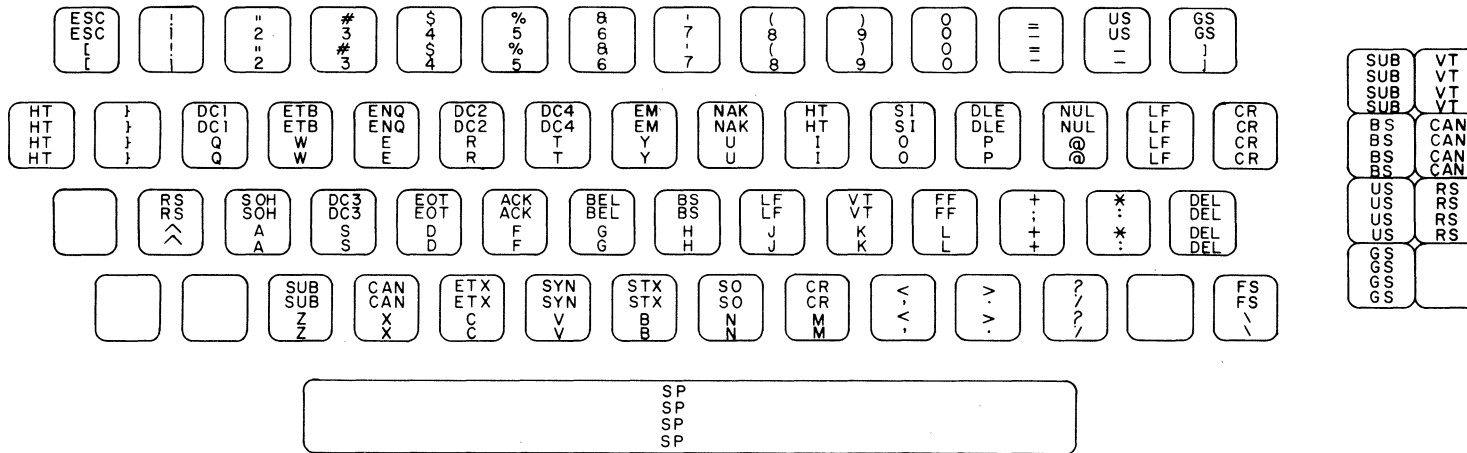
A-2



LEGEND:
 CONTROL & SHIFT
 CONTROL
 SHIFT
 UNSHIFT

CP-0609

Figure A-2 128-Character Keyboard (Position 1)



LEGEND
CONTROL & SHIFT
CONTROL
SHIFT
UNSHIFT

Figure A-3 64-Character Keyboard (Position 2)

APPENDIX B ADDRESS MAPPING

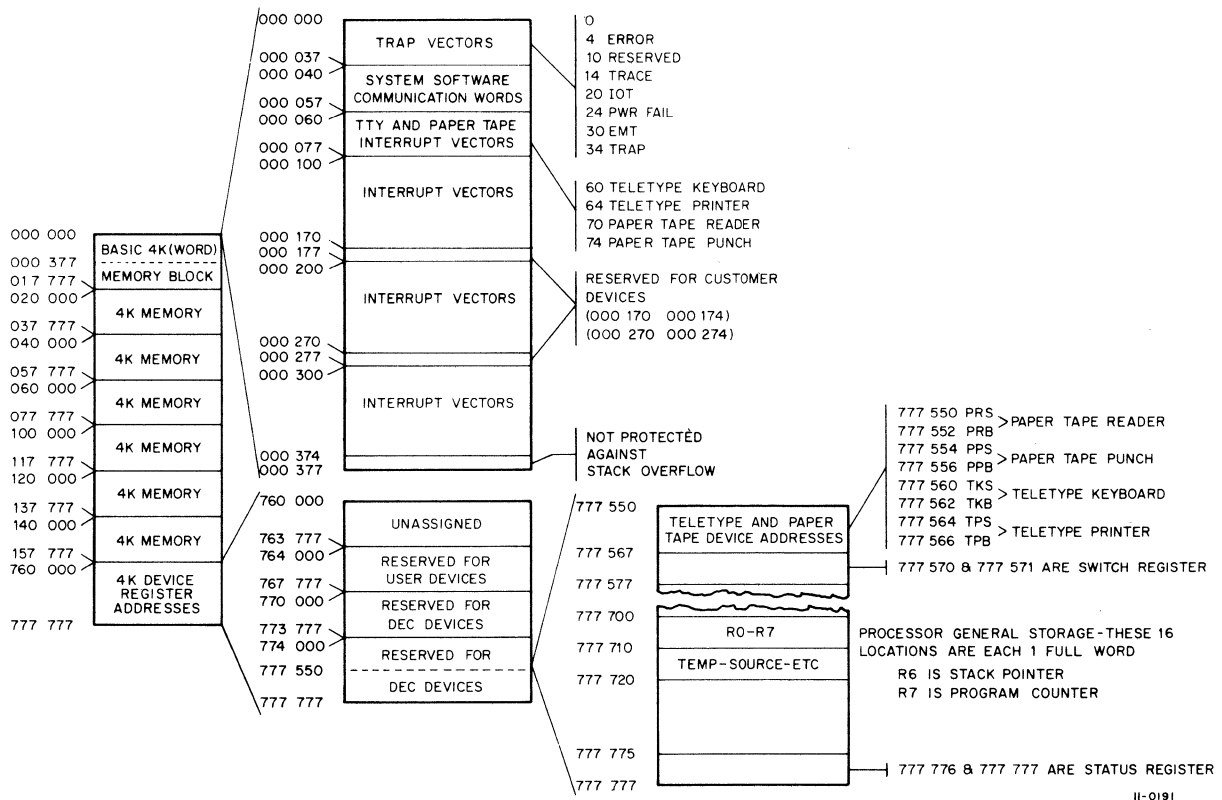


Figure B-1 Address Mapping

APPENDIX C CHARACTER CODES

7 Bit (octal)	ASCII Representation	Keyboard	GT40/42 Printing	GT40/42 Printing When Preceded By Shift-Out = 016
000	NUL	CTRL @		λ
001	SOH	CTRL A		α
002	STX	CTRL B		φ
003	ETX	CTRL C		Σ
004	EOT	CTRL D		δ
005	ENQ	CTRL E		Δ
006	ACK	CTRL F		~
007	BEL	CTRL G		∫
010	BS	CTRL H	Backspace	∩
011	HT	CTRL I (TAB)		ψ
012	LF	CTRL J (LF)	Line Feed	÷
013	VT	CTRL K		ο
014	FF	CTRL L		∴
015	CR	CTRL M (CR)	Carriage Return	μ
016	SO	CTRL N		£
017	SI	CTRL O		Shift In
020	DLE	CTRL P		π
021	DC1	CTRL Q		∥
022	DC2	CTRL R		Ω
023	DC3	CTRL S		σ
024	DC4	CTRL T		Υ
025	NAK	CTRL U		ε
026	SYN	CTRL V		←
027	ETB	CTRL W		→
030	CAN	CTRL X		↑
031	EM	CTRL Y		↓
032	SUM	CTRL Z		⌈
033	ESC	CTRL [(ALT)		⊥
034	FS	CTRL \		≠
035	GS	CTRL]		≈
036	RS	CTRL ~		∨
037	US	CTRL -		□
40	SP	SPACE BAR	Space 1 character	
41	!	SHIFT 1	!	
42	“	SHIFT 2	“	
43	#	SHIFT 3	#	

7 Bit (octal)	ASCII Representation	Keyboard	GT40/42 Printing	GT40/42 Printing When Preceded By Shift-Out = 016
44	\$	SHIFT 4	\$	
45	%	SHIFT 5	%	
46	&	SHIFT 6	&	
47	'	SHIFT 7	'	
50	(SHIFT 8	(
51)	SHIFT 9)	
52	*	SHIFT :	*	
53	+	SHIFT ;	+	
54	,	,	,	
55	- (minus)	-	-	
56	.	.	.	
57	/	/	/	
60	0	0	0	
61	1	1	1	
62	2	2	2	
63	3	3	3	
64	4	4	4	
65	5	5	5	
66	6	6	6	
67	7	7	7	
70	8	8	8	
71	9	9	9	
72	:	:	:	
73	;	;	;	
74	<	SHIFT ,	<	
75	=	SHIFT -	=	
76	>	SHIFT .	>	
77	?	SHIFT /	?	
100	@	@	@	
101	A	SHIFT A	A	
102	B	SHIFT B	B	
103	C	SHIFT C	C	
104	D	SHIFT D	D	
105	E	SHIFT E	E	
106	F	SHIFT F	F	
107	G	SHIFT G	G	
110	H	SHIFT H	H	
111	I	SHIFT I	I	
112	J	SHIFT J	J	
113	K	SHIFT K	K	
114	L	SHIFT L	L	
115	M	SHIFT M	M	
116	N	SHIFT N	N	
117	O	SHIFT O	O	
120	P	SHIFT P	P	
121	Q	SHIFT Q	Q	
122	R	SHIFT R	R	
123	S	SHIFT S	S	
124	T	SHIFT T	T	

7 Bit (octal)	ASCII Representation	Keyboard	GT40/42 Printing	GT40/42 Printing When Preceded By Shift-Out = 016
125	U	SHIFT U	U	
126	V	SHIFT V	V	
127	W	SHIFT W	W	
130	X	SHIFT X	X	
131	Y	SHIFT Y	Y	
132	Z	SHIFT Z	Z	
133	[[[
134	\	\	\	
135]]]	
136	^	^	^	
137	.	.	.	
140		SHIFT @		
141	a	A	a	
142	b	B	b	
143	c	C	c	
144	d	D	d	
145	e	E	e	
146	f	F	f	
147	g	G	g	
150	h	H	h	
151	i	I	i	
152	j	J	j	
153	k	K	k	
154	l	L	l	
155	m	M	m	
156	n	N	n	
157	o	O	o	
160	p	P	p	
161	q	Q	q	
162	r	R	r	
163	s	S	s	
164	t	T	t	
165	u	U	u	
166	v	V	v	
167	w	W	w	
170	x	X	x	
171	y	Y	y	
172	z	Z	z	
173		SHIFT [~	
174		SHIFT \	~	
175		SHIFT]	~	
176	~	SHIFT ^	~	
177	RUB OUT	R.O.	■	

Function Key Codes

← 10 ↑ 32 Home 35 EOS 37
→ 30 ↓ 33 EOL 36

;BOOTVT.S09 5/2/72

; VT-40 BOOTSTRAP LOADER, VERSION S09, RELEASE R01, 5/2/72

; COPYRIGHT 1972, DIGITAL EQUIPMENT CORPORATION.
; 146 MAIN STREET
; MAYNARD, MASSACHUSSETTS
; 01754

; WRITTEN BY JACK BURNES, SENIOR SYSTEMS ARCHITECT!

; THIS ROUTINE IS INTENDED TO BE LOADED IN THE ROM PORTION OF THE VT-40.

; REGISTER DEFINITIONS:

000000
000001
000002
000003
000004
000005
000006
000007

R0=%0
R1=%1
R2=%2
R3=%3
R4=%4
R5=%5
R6=%6
R7=%7

000006
000007

SP=R6
PC=R7

000000
000001
000002
000003
000004
000005

RET1=R0
INP1=R1
INP2=R2
WORK1=R3
WORK2=R4
SCR1=R5

;RETURN OF VALUE REGISTER.
;ARGUMENT FOR CALLED FUNCTION
;SECOND ARGUMENT.
;FIRST WORK REGISTER.
;SECOND WORKING REGISTER.
;SCRATCH REGISTER.

000003
000000
000005
000001

L,CKSM=WORK1
L,BYT=RET1
L,BC=SCR1
L,ADR=INP1

;OVERLAPPING DEFINITIONS FOR LOADER PORTION.

016000
166000

COREND=16000
ROMORG=166000

;FIRST LOCATION OF NON-CORE.
;WHERE THE ROM PROGRAM SHOULD GO.

000000
001360

STARTX=0
STARTY=1360

;WHERE TO START DISPLAYING THE X POSITIONS.
;WHERE TO START DISPLAYING THE Y.

172000			VT40PC=172000		;VT40 PROGRAM COUNTER.
177560			KBDIS=177560		;TTY INPUT STATUS.
175614			P100S=175614		;PDP-10 OUTPUT STATUS.
175610			P10IS=175610		;PDP-10 INPUT STATUS.
177562			KBDIB=KBDIS+2		;TTY INPUT BUFFER.
175612			P10IB=P10IS+2		;PDP-10 INPUT CHARACTER.
175616			P100B=P100S+2		;PDP-10 OUTPUT BUFFER.
015776			P100C=COREND-2		;CHARACTER TO BE SENT TO THE PDP-10
015772			P10IC=P100C-4		;INPUT CHARACTER FROM 10 PLUS ONE SAVE CHARACTER
015770			STKSRT=P10IC-2		;FIRST LOCATION OF STACK.
160000			JMPDIS=160000		;THE VT-40 DISPLAY JUMP INSTRUCTION.
000024			PWRFAL=24		;POWER FAIL RESTART LOCATION.
166000			,=ROMORG		;SET THE ORIGIN NOW!!!!
166000	012705	000026	START: MOV #PWRFAL+2,SCR1		;PICK UP POINTER TO P.F. STATUS.
166004	005015		CLR @SCR1		;CLEAR IT OUT TO BE SURE.
166006	010745		MOV PC,-(SCR1)		;SET UP THE RESTART LOCATION.
166010	000005		RESET		;RESET THE BUS.
166012	012767	000007	MOV #7,P10IS		;INITIALIZE PDP-10 INPUT
166020	012767	000001	MOV #1,KBDIS		;INITIALIZE TTY INPUT.
166026	012767	000201	MOV #201,P100S		;INITIALIZE PDP-10 OUTPUT.
166034	012706	015770	RESTR1: MOV #STKSRT,SP		;SET UP THE STACK NOW!
166040	005001		CLR L,ADR		;CLEAR ADDRESS POINTER.
166042	012702	160000	MOV #JMPDIS,INP2		;PLACE A DISPLAY JUMP INSTRUCTION IN A REGISTER.
166046	010221		MOV INP2,(L,ADR)+		;MOVE IT TO LOCATION 0.
166050	012711	166756	MOV #DISPRG,(L,ADR)		;MOVE ADDRESS POINTER INTO 2.
166054	012701	000030	MOV #PWRFAL+4,L,ADR		;SET UP WHERE WE WILL STORE CHARACTERS.
166060	005000		CLR RET1		;PREPARE TO INSERT A ZERO CHARACTER.
166062	004767	000022	JSR PC,DOCHAR		;INSERT IT NOW.
166066	005067	003706	CLR VT40PC		;CLEAR THE DISPLAY PROGRAM COUNTER AND START.
166072	004767	000210	MAJOR1: JSR PC,GETCHR		;GET A CHARACTER NOW.
166076	000240		NOP		
166100	000240		NOP		
166102	000240		NOP		
166104	012746	166072	MOV #MAJOR,-(SP)		;INSERT IN DISPLAY BUFFER NOW.

166110	010105		DOCHAR:	MOV	L,ADR,SCR1		;GET CURRENT BUUFER POSITION NOW.
166112	022525			CMP	(SCR1)+,(SCR1)+		;BYPASS CURRENT DISPLAY JUMP.
166114	005025			CLR	(SCR1)+		;CLEAR FUTURE ADDRESS FOR JUMP.
166116	010225			MOV	INP2,(SCR1)+		;STICK IN TEMPORARY JUMP WHILE WE REPLACE CURREN
166120	005015			CLR	(SCR1)		;A DISPLAY JUMP TO ZERO.
166122	005011			CLR	(L.ADR)		;NOW REPLACE CURRENT DISPLAY JUMP BY THE CHARACT
166124	050021			BIS	RET1,(L.ADR)+		;IT'S DONE THIS WAY TO WASTE 2 CYCLES.
166126	010211			MOV	INP2,(L.ADR)		;TO AVOID TIMING PROBLEMS WITH THE VT40.
166130	000207			RTS	PC		;AND FINALLY RETURN.
166132	004767	000124	GET8:	JSR	PC,GETSIX		;GET SIX BITS NOW.
166136	010046			MOV	RET1,-(SP)		;SAVE THE CHARACTER NOW.
166140	000401			BR	GETP84		;BYPASS THE 8'ER
166142	005002		GET84:	CLR	INP2		;RESET THE MAGIC REGISTER NOW.
166144	005722		GETP84:	TST	(INP2)+		;INCREMENT WHERE TO GO.
166146	066207	166250		ADD	GET8TB(INP2),PC		;UPDATE PC NOW.
	166152		GET8P=,				
166152	004767	000104	GET81:	JSR	PC,GETSIX		;GET A CHARACTER NOW.
166156	010004			MOV	RET1,WORK2		;SAVE FOR A SECOND.
166160	006300			ASL	RET1		
166162	006300			ASL	RET1		;SHIFT TO LEFT OF BYTE
166164	106300			ASLB	RET1		
166166	106116			ROLB	@SP		;PACK THEM IN.
166170	106300			ASLB	RET1		
166172	106116			ROLB	@SP		;A GOOD 8 BIT THING.
166174	012600			MOV	(SP)+,RET1		;POP AND RETURN NOW.
166176	000207			RTS	PC		
166200	006300		GET82:	ASL	RET1		;WORST CASE. SHIFT 4
166202	006300			ASL	RET1		
166204	106300			ASLB	RET1		
166206	106104			ROLB	WORK2		
166210	106300			ASLB	RET1		
166212	106104			ROLB	WORK2		
166214	106300			ASLB	RET1		
166216	106104			ROLB	WORK2		
166220	106300			ASLB	RET1		
166222	106104			ROLB	WORK2		
166224	010400			MOV	WORK2,RET1		
166226	012604			MOV	(SP)+,WORK2		
166230	000207			RTS	PC		
166232	006100		GET83:	ROL	RET1		
166234	006100			ROL	RET1		
166236	006004			ROR	WORK2		
166240	106000			RORB	RET1		
166242	006004			ROR	WORK2		
166244	106000			RORB	RET1		;FINAL CHARACTER ASSEMBLED.
166246	005726			TST	(SP)+		;FUDGE STACK.
166250	000207			RTS	PC		;AND RETURN NOW.

	166250		GET8TB =	,=2	;PUSH ZERO CONDITION BACK INTO NEVER-NEVER LAND.
166252	000000			,WORD GET81-GET8P	
166254	000026			,WORD GET82-GET8P	
166256	000060			,WORD GET83-GET8P	
166260	177770			,WORD GET84-GET8P	
166262	004767	000020	GETSIX:	JSR PC,GETCHR	
166266	020027	000040		CMP RET1,#40	
166272	002546			BLT L,BAD	
166274	020027	000137		CMP RET1,#137	
166300	003143			BGT L,BAD	
166302	000207			RTS PC	
166304	005726		GETCHP:	TST (SP)+	;UPDATE THE STACK,
166306	012700	015772	GETCHR:	MOV #P10IC,RET1	;SET UP POINTER TO THE INPUT CHARACTER.
166312	004767	000064	GETCHL:	JSR PC,CHECK	
166316	005710			TST @RET1	;ANY CHARACTERS THERE?
166320	001774			BEQ GETCHL	
166322	011046			MOV @RET1,-(SP)	;PUSH THE CHAR ON THE STACK.
166324	005020			CLR (RET1)+	;CLEAR THE CHAR GOT FLAG NOW.
166326	042716	177600		BIC #-200,(SP)	;CLEAR AWAY PARITY NOW.
166332	001764			BEQ GETCHP	;IF ZERO, GET ANOTHER
166334	022716	000177		CMP #177,(SP)	
166340	001761			BEQ GETCHP	;ALSO IGNORE RUBOUTS.
166342	022710	000175		CMP #175,@RET1	;WAS IT A "175"
166346	001007			BNE GETNP	;NOPE.
166350	011610			MOV (SP),@RET1	;YEP. RESET IN CASE OF ABORT.
166352	021027	000122		CMP @RET1,#122	;IS IT AN R
166356	001626			BEQ RESTR1	;YEP. RESTART
166360	021027	000114		CMP @RET1,#114	;IS IT AN L
166364	001455			BEQ LOAD	;YEP. LOAD.
166366	011610		GETNP:	MOV (SP),@RET1	;NOW DO THE FUDGING.
166370	012600			MOV (SP)+,RET1	
166372	020027	000175		CMP RET1,#175	
166376	001743			BEQ GETCHR	;IF ALTMODE, LOOP
166400	000207			RTS PC	
166402	005767	027370	CHECK:	TST P100C	;DO WE WANT TO OUTPUT?
166406	001410			BEQ CHECK1	;NO.
166410	105767	007200		TSTB P100S	;WE DO. IS THE 10 READY?
166414	100005			BPL CHECK1	;NOT QUITE.
166416	016767	027354	007172	MOV P100C,P100B	;IT'S READY. SEND THE CHARACTER.
166424	005067	027346		CLR P100C	;AND THE SAVED CHARACTER.
166430	105767	011124	CHECK1:	TSTB KBDIS	;HEY, IS THE KEYBOARD READY?
166434	100014			BPL CHECK3	;NOPE. NO LUCK.


```

166646 004767 177756      L.GWRD: JSR    PC,L.PTR      ;GET A CHARACTER,
166652 010046              MOV    L,BYT,-(SP)         ;SAVE FOR A SECOND,
166654 004767 177750      JSR    PC,L.PTR      ;GET ANOTHER CHARACTER,
166660 000300              SWAB   L,BYT             ;NOW ASSEMBLE THE WORD,
166662 052600              BIS    (SP)+,L.BYT      ;AND RETURN WITH A 16 BITER.

166664 000207              RTS    PC

166666 004767 177754      L.JMP: JSR    PC,L.GWRD    ;GET A WORD
166672 010046              MOV    L,BYT,-(SP)         ;SAVE ON THE STACK,
166674 004767 177730      JSR    PC,L.PTR      ;GET A CHARCTER,
166700 105703              TSTB  L,CKSM           ;IS IT ZERO?
166702 001342              BNE   L,BAD            ;YEP. WHAT CRAP.
166704 032716 000001      BIT   #1,(SP)         ;IS IT ODD?
166710 001406              BEQ   L,JMP1          ;YEP. START PROGRAM GOING NOW.
166712 012700              MOV    (PC)+,RET1       ;TELL PDP-10 WE'VE LOADED OK.
166714      175      107
166716 004767 000006      JSR    PC,SENDIT
166722 000000              HALT
166724 000776              BR    ,-2

166726 000136      L.JMP1: JMP    @ (SP)+      ;AND AWAY WE GO.

166730 004767 177446      SENDIT: JSR    PC,CHECK    ;POLL THE OUTPUT DEVICE NOW.
166734 005767 027036      TST   P100C           ;OUTPUT CLEAR?
166740 001373              BNE   SENDIT          ;NOPE. LOOP AWHILE LONGER.
166742 010067 006650      MOV    RET1,P100B     ;SEND OUT THE CHARACTER,
166746 105000              CLRB  RET1            ;CLEAR THE BYTE,
166750 000300              SWAB  RET1            ;AND SWAP THEM NOW.
166752 001366              BNE   SENDIT          ;IF NOT EQUAL, REPEAT.
166754 000207              RTS    PC

;
;      THIS IS THE INITIALIZING VT40 PROGRAM WHICH WILL
;      JUMP TO THE PROGRAM AFTER THE POWER FAIL LOCATIONS
;      WHICH WILL JUMP TO ZERO WHICH WILL JUMP BACK TO HERE.

166756 170256      DISPRG: ,WORD 170256      ;LOAD STATUS REGISTER FOR NORMAL OPERATION.
166760 115124      ,WORD 115124          ;SET POINT MODE, "NORMAL".
166762 000000      ,WORD STARTX         ;X COORDINATE
166764 001360      ,WORD STARTY        ;Y COORDINATE
166766 100000      ,WORD 100000        ;SET CHARACTER MODE.
166770 160000      ,WORD JMPDIS        ;THEN JUMP TO THE POWERFAIL LOCATION.
166772 000030      ,WORD PWRFAL+4     ;TO DISPLAY USERS CHARACTERS.

000001      ,END

```

SYMBOL TABLE

CHECK	166402	CHECK1	166430	CHECK2	166450	CHECK3	166466
CHECK4	166516	COREND	= 016000	DISPRG	166756	DOCHAR	166110
GETCHL	166312	GETCHP	166304	GETCHR	166306	GETNP	166366
GETP84	166144	GETSIX	166262	GET8	166132	GET8P	= 166152
GET8TB	= 166250	GET81	166152	GET82	166200	GET83	= 166232
GET84	166142	INP1	=%000001	INP2	=%000002	JMPDIS	= 160000
KBDIB	= 177562	KBDIS	= 177560	LOAD	166520	L.ADR	=%000001
L.BAD	166610	L.BC	=%000005	L.BYT	=%000000	L.CKSM	=%000003
L.GWRD	166646	L.JMP	166666	L.JMP1	166726	L.LD2	166532
L.LD3	166576	L.LD4	166624	L.PTR	166630	MAJOR	166072
PC	=%000007	PWRFAL	= 000024	P10IB	= 175612	P10IC	= 015772
P10IS	= 175610	P10OB	= 175616	P10OC	= 015776	P10OS	= 175614
RESTR	166034	RET1	=%000000	ROMORG	= 166000	R0	=%000000
R1	=%000001	R2	=%000002	R3	=%000003	R4	=%000004
R5	=%000005	R6	=%000006	R7	=%000007	SCR1	=%000005
SENDIT	166730	SP	=%000006	START	166000	STARTX	= 000000
STARTY	= 001360	STKSRT	= 015770	VT40PC	= 172000	WORK1	=%000003
WORK2	=%000004	.	= 166774				

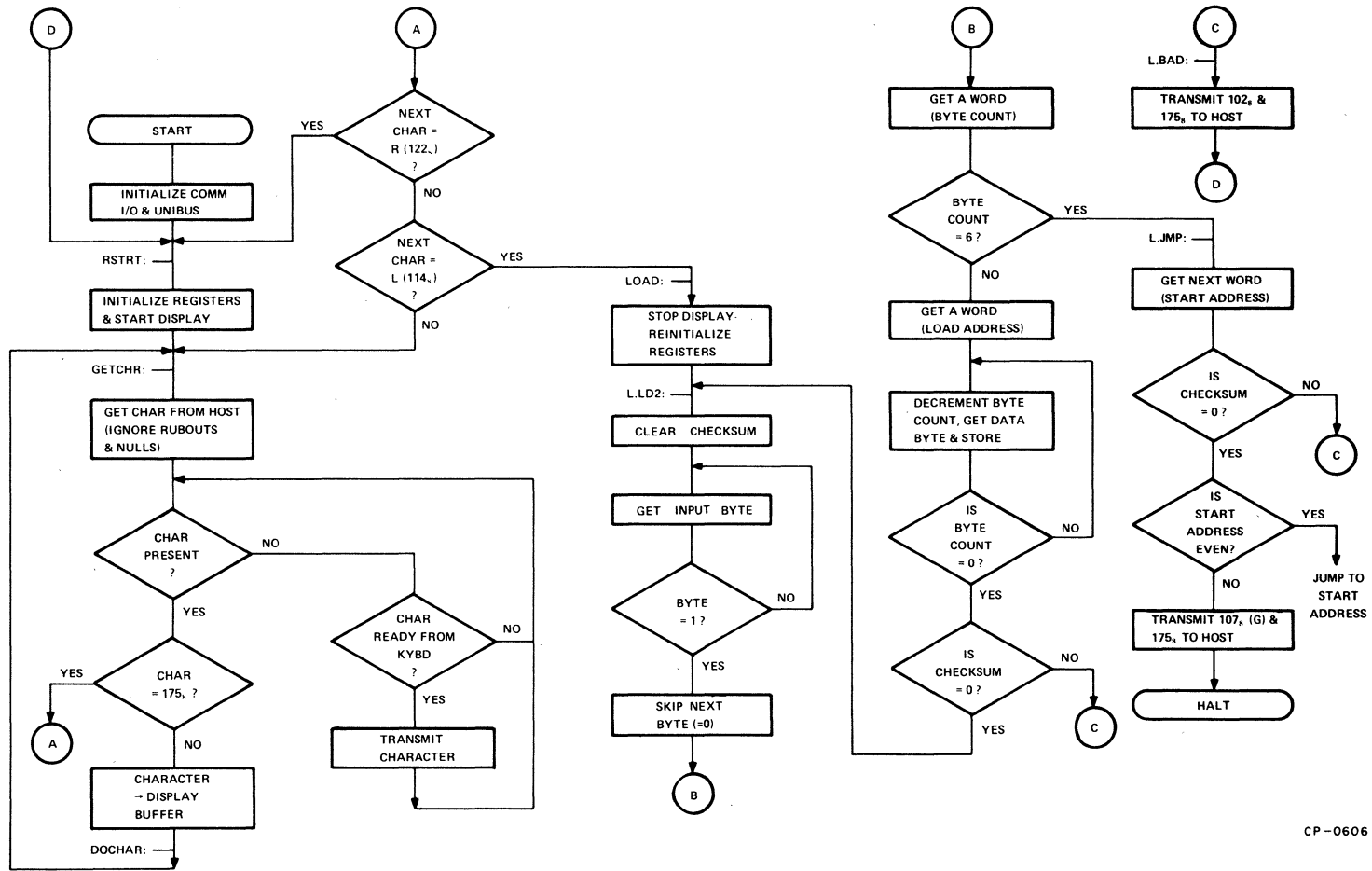


Figure D-1 Communications Bootstrap Loader Flow Diagram

APPENDIX E
SCROLLING ROM BOOTSTRAP
LOADER PROGRAM - GT42

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.TITLE SCROLLING ROM BOOTSTRAP FOR THE GT40

BOOTGT,T15 JUNE 24,1973

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146 MAIN STREET
MAYNARD, MASSACHUSETTS 01754

WRITTEN BY JACK BURNES,

THIS PROGRAM IS THE SECOND VERSION THE THE ROM BOOTSTRAP FOR
THE GT40 DISPLAY TERMINAL, IT INCLUDES SCROLLING AND AN END OF
MEMORY SEARCH FOR THE LOADER.

.ENABL ABS,AMA

!ASSEMBLER DIRECTIVES FOR ABSOLUTE BINARY OUTPUT
! NOTE! USE "MACDLX" TO ASSEMBLE THIS PROGRAM,

.SBTTL DEFINITION SECTION

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REGISTER DEFINITIONS

BASIC DEFINITIONS

000000	R0=X0	DEFINE STANDARD VALUES,
000001	R1=X1	
000002	R2=X2	
000003	R3=X3	
000004	R4=X4	
000005	R5=X5	
000006	SP=X6	
000007	PC=X7	

GT40 DEFINITIONS

000000	CHAR=R0	CONTAINS THE INPUT CHARACTER,
000001	POINTR=R1	POINTS TO NEXT INSERTION BYTE IN DISPLAY BUFFER
000002	TABCNT=R2	CHARACTER COUNTER FOR THE "TAB" FEATURE,
000003	SCAN=R3	GENERALLY CONTAINS A POINTER WHICH
		IS USED WHEN SCANNING MEMORY FOR SOMETHING,
000004	HOLD=R4	TYPICALLY A TEMPORARY WHICH IS USED TO RETAIN
		A VALUE FOR A SHORT TIME,
000005	COUNTR=R5	TYPICALLY USED AS A COUNTER,

LOADER DEFINITIONS

000000	L,BYT=CHAR	CHARACTER INPUT FOR THE LOADER,
000001	L,ADR=POINTR	CURRENT MEMORY ADDRESS TO BE LOADED,
000002	L,BC=TABCNT	NUMBER OF DATA ITEMS TO LOAD,
000005	L,CKSM=COUNTR	CHECKSUM ON THE INPUT DATA,
000003	INDEX=SCAN	INDICATES HOW TO ASSEMBLE THE 8 BIT CHARACTER,

E-3

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MAJOR SYSTEM DEFINITIONS

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166000      ORIGIN=166000      IORIGIN OF THE BOOTSTRAP,
175610      DL11IS=175610     IINPUT STATUS REGISTER OF DL11
175612      DL11IB=DL11IS+2   IINPUT CHARACTER FROM DL11
175614      DL11OS=DL11IB+2   IOUTPUT STATUS OF THE DL11
175616      DL11OB=DL11OS+2   IOUTPUT CHARACTER TO THE DL11
177560      KBDIS=177560     IKEYBOARD INPUT STATUS
177562      KBDIB=KBDIS+2     ICURRENT CHARACTER FROM KEYBOARD,
172000      GT40PC=172000     IGT40 PROGRAM COUNTER,
172002      GT40SR=GT40PC+2   IGT40 STATUS REGISTER ADDRESS,
001000      RSTART=1000      ISTART OF THE DISPLAY BUFFER
007000      BLIMIT=7000      IAPPROXIMATE END OF THE DISPLAY BUFFER,
007776      TMPEND=7776     ILOCATION OF INITIALIZATION STACK,
000004      CORSTR=4        ILOCATION OF PDP-11 TRAP VECTOR,
007012      JMPADD=BLIMIT+10, IWHERE THE POINTER IS TO FIRST CHAR ON SCREEN
000040      NUMLINE=32,     INUMBER OF LINES ON TEXT TO SHOW ON THE SCREEN
005015      CRLF=5015       ICARRIAGE RETURN = LINE FEED
000175      ALTMOD=175      ITHE "KEY" CHARACTER [I,E, ALTMODE],
160000      DISJMP=160000    ITHE GT40 JMP INSTRUCTION
173000      DISTOP=173000   ITHE GT40 STOP DISPLAY INSTRUCTION,
  
```

SBTTL INITIALIZATION AND RESTART CODE


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217
218
219
220
221 166060 052706 027776      RESTRTI BIS      #TMPEND,SP      !FORCE THE SP TO LIMIT OF EXISTING CORE,
222
223
224 166064 012703 006700      MOV             #BLIMIT-NUMLIN=NUMLIN,SCAN      !NOW WE WILL FILL THE KEY AREAS OF THE
225 166070 012702 000040      MOV             #NUMLIN,TABCNT      !DISPLAY BUFFER WITH INITIAL CR-LF'S,
226
227 166074 012723 005015      SETLP1: MOV      #CRLF,(SCAN)+      !INSERT A CRLF NOW,
228 166100 005302      DEC            TABCNT      !AND LOOP UNTIL DONE,
229 166102 003374      BGT            SETLP1      !THUS DISPLAY CORE IS ALMOST CORRECT,
230
231
232 166104 012703 166432      MOV             #SETUP,SCAN      !NOW WE WILL INITIALIZE CORE FOR THE
233
234
235 166110 012302      SETLP2: MOV      (SCAN)+,TABCNT      !GET NUMBER OF ITEMS TO INSERT,
236 166112 001405      BEQ            SETDUN      !IF ZERO, WE ARE DONE,
237 166114 012301      MOV            (SCAN)+,POINTR      !PICK UP FIRST CORE ADDRESS POINTER,
238
239 166116 012321      SETLP3: MOV      (SCAN)+,(POINTR)+      !MOVE OVER A DATA ITEM NOW,
240 166120 005302      DEC            TABCNT      !ALL DONE?
241 166122 003375      BGT            SETLP3      !NOPE, MOVE OVER THE NEXT,
242 166124 000771      BR             SETLP2      !YES, GET NEXT MAJOR LIST TO INSERT,
243
244
245 166126 012701 026776      SETDUN: MOV     #BLIMIT-2,POINTR      !ESTABLISH THE BUFFER POINTER NOW,
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    .SBTTL VT05 SIMULATOR
    
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E6

E-7

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267 166132 004737 166564      NXTCHR: JSR    PC,GETCHR      IGET A CHARACTER NOW.
268 166136 020027 000177      CMP    CHAR,#177           IIS IT OUT OF RANGE?
269 166142 002373              BGE    NXTCHR              IYEP, GET ANOTHER ONE.
270 166144 020027 000040      CMP    CHAR,#40           IIS IT A PRINTING CHARACTER?
271 166150 002020              BGE    NORMAL             IYES, IT'S A NORMAL PRINTING CHARACTER.
272 166152 010003              MOV    CHAR,SCAN         IMOVE IT OVER SO WE CAN PLAY WITH IT.
273 166154 162703 000007      SUB    #7,SCAN           IBIAS SO THAT BELL [7] IS ZERO.
274 166160 020327 000007      CMP    SCAN,#7           IIF CHARACTER IS LESS THEN BELL OR
275 166164 103362              BHS    NXTCHR            IGREATER THEN CR, THEN IGNORE.
276 166166 006303              ASL    SCAN              IIF GOOD, MAKE IT WORD INDEX.
277 166170 060307              ADD    SCAN,PC           IAND GO TO THE CORRECT ROUTINE.
278
279 166172 000426              BR     BELL              I7=BELL
280 166174 000406              BR     NORMAL           I10=BACKSPACE
281 166176 000411              BR     TAB              I11=TAB
282 166200 000437              BR     LF              I12=LINE FEED [LF]
283 166202 000420              BR     VT              I13=VERTICAL TAB [VT]
284 166204 000424              BR     FF              I14=FORM FEED [FF]
285
286
287
288 166206 012702 177777      CR:    MOV    #-1,TABCNT  IRESET TAB POSITION ON A CR, AND
289
290
291
292 166212 004737 166350      NORMAL: JSR    PC,INSERT   IINSERT THE CHARACTER IN THE BUFFER.
293 166216 005202              INC    TABCNT           IUPDATE TAB POSITION NOW.
294 166220 000744              BR     NXTCHR           IAND GET NEXT CHARACTER.
295
296
297
298
299 166222 012700 000040      TAB:   MOV    #40,CHAR    ION A TAB, INSERT BLANKS UNTIL THE
300 166226 004737 166350      JSR    PC,INSERT        INEXT CHARACTER POSITION IS A MULTIPLE
301 166232 005202              INC    TABCNT          IOF 8.
302 166234 032702 000007      BIT    #7,TABCNT       IARE WE DONE YET?
303 166240 001370              BNE    TAB             INOPE.
304 166242 000733              BR     NXTCHR          IYES.
305
306
307 166244 111705      VTI:   MOV    (PC),COUNTR ITHIS PUTS THE LOW BYTE OF THE
308
309 166246 000405              BR     FFLOOP          IBRANCH CODE IN COUNTR=SAVE A WORD
310
311 166250 005037 172002      BELL:  CLR    GT40SR     IRING BELL -WRITE IN GT40SR
312 166254 000726              BR     NXTCHR          IAND LOOP BACK

```


313						
314	166256	012705	000040	FFI	MOV #NUMLIN,COUNTR	IFORM FEED IS DONE BY INSERTING LFI'S;
315						
316	166262	012700	000012	FFLOOPI	MOV #12,CHAR	IMAKE THE CHARACTER A LINEFEED;
317	166266	004737	166304		JSR PC,LFSUB	IDO A LINEFEED;
318	166272	005305			DEC COUNTR	IDONE?
319	166274	003372			BGT FFLOOP	INOPE, KEEP SENDING THEM,
320	166276	000715			BR NXTCHR	IYES, NOW RETURN, DO NOT FALL THROUGH;
321						
322						
323	166300	012746	166132	LFI	MOV #NXTCHR,-(SP)	IRETURN TO NXTCHR AFTER PROCESSING
324						ITHE LF BY FAKING A JSR,
325						
326	166304	013703	007012	LFSURI	MOV JMPADD,SCAN	IGET POINTER TO FIRST CHAR ON SCREEN
327						
328	166310	12230F		LFLOOPI	CMPB (SCAN)+,CHAR	IAND LOOK FOR A LINEFEED,
329	166312	001476			REQ LFOUND	IGOT IT, SEARCH HAS ENDED,
330	166314	020327	007000		CMP SCAN,#BLIMIT	IARE WE AT END OF BUFFER?
331	166320	103773			RLO LFLOOP	INOPE, KEEP ON LOOKING;
332	166322	012703	001000		MOV #BSTART,SCAN	IIF AT TOP, RESET TO BOTTOM OF BUFFER
333	166326	000770			BR LFLOOP	IAND KEEP ON LOOKING,
334						
335	166330	005203		LFOUNDI	INC SCAN	IWE'VE GOT THE LINE FEED, STOP SHOWING
336	166332	042703	000001		BIC #1,SCAN	IFIRST LINE BY CHANGING THE "DISJMP"
337	166336	010337	007012		MOV SCAN,JMPADD	IINSTRUCTION TO FIRST CHAR BEYOND LF,
338	166342	004737	166350		JSR PC,INSERT	IINSERT THE LF IN THE BUFFER,
339	166346	005000			CLR CHAR	IAND THEN INSERT ONE NULL CHARACTER BECAUSE
340						ITHE "DISJMP" ADDRESS MUST BE EVEN, AND
341						IThis GUARANTEES WE WILL NOT LOSE A
342						IA GOOD DATA CHARACTER, WE FALL THROUGH
343						ITO INSERT THE NULL IN THE BUFFER,
344						
345						
346	166350	110021		INSERTI	MOVB CHAR,(POINTR)+	IJUSTICK IN THE CHARACTER NOW,
347	166352	032701	000001		BIT #1,POINTR	IIS NEXT POSITION EVEN OR ODD?
348	166356	001021			BNE INSRTX	IODD, NO PROBLEMS, SPACE IS ALLOCATED,
349	166360	020127	007000		CMP POINTR,#BLIMIT	I EVEN, ARE WE AT THE END OF THE BUFFER?
350	166364	103410			BLO INSRTL	I NO, JUST MAKE ROOM FOR ANOTHER WORD.
351	166366	010103			MOV POINTR,SCAN	IAT THE END, MOVE THE STUFF TO THE
352	166370	012701	001000		MOV #BSTART,POINTR	IBEGINNING OF THE BUFFER,
353	166374	004737	166406		JSR PC,INSRTL	ICALL THE ROUTINE TO SAVE SPACE,
354	166400	005023			CLR (SCAN)+	IAND CLEAR UP THE INSTRUCTIONS AT THE
355	166402	005013			CLR (SCAN)	IBEND OF THE BUFFER,
356	166404	000207			RTS PC	IAND THEN RETURN,
357						
358	166406	022171		INSRTL:	CMP (POINTR)+,(POINTR)+	IBYPASS THE "DISJMP" BY ADDING 4 TO POINTR,
359	166410	012711	166474		MOV #HEADER,(POINTR)	I NOW INSERT THE DISJMP INSTRUCTION TO OUR HEADER
360	166414	012741	160000		MOV #DISJMP,-(POINTR)	IAND IT'S ADDRESS (PUT THEM IN BACKWARDS),
361	166420	005041			CLR -(POINTR)	IMAKE AVAILABLE A NEW CHARACTER SPOT,
362						
363	166422	000207		INSRTX:	RTS PC	IFINALLY RETURN TO THE CALLER,
364						
365						
366						

```

347
348
349 166424 012737 001000 172000 GTBUSEI MOV #BSTART,GT40PC      ;ON A BUS ERROR, WE MERELY RESTART THE GT40 AT
370
371                                     ;THE RTI FOR THIS ROUTINE
372                                     ;IS THE FIRST WORD OF THE TABLE
373                                     ;BELOW-IT SAVES A WORD!
374
375
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386                                     ;
387                                     ;
388                                     ;
389
390 166432 000002          SETUP1 ,WORD 2          ;INITIALIZE 2 WORDS,--ALSO RTI FROM ABOVE
391 166434 000330          ,WORD 330             ;STARTING AT LOCATION 330
392 166436 166424          ,WORD GTBUSE         ;FIRST WORD IS POINTER TO BUS ERROR ROUTINE,
393 166440 000200          ,WORD 200             ;SECOND WORD IS NEW STATUS WORD ON INTERUPY,
394
395 166442 000007          ,WORD 7              ;INITIALIZE THE END OF THE BUFFER TO
396 166444 000776          ,WORD BLIMIT=2       ;A CLEAR SPACE TO INSERT THE CHARACTER,
397 166446 000000          ,WORD 0              ;THIS IS THE "RUNNING" START, THIS IS
398 166450 160002 166474   ,WORD DISJMP,HEADER ;FOLLOWED BY A DISJMP TO OUR HEADER BLOCK
399 166454 160000 001000   ,WORD DISJMP,BSTART ;AND THEN A DISJMP TO THE START OF THE BUFFER
400 166460 160000 006700   ,WORD DISJMP,BLIMIT-NUMLIN-NUMLIN ;AND A DISJMP TO THE FIRST CHAR ON SCREE
401
402 166464 000011          ,WORD 1              ;FINALLY START THE GT40 GOING AT
403 166466 172010          ,WORD GT40PC         ;THE POSITION INSTRUCTION IN THE
404 166470 166474          ,WORD HEADER        ;HEADER BLOCK,
405
406 166472 000000          ,WORD 0              ;END OF INIT CODE
407
408                                     ;
409                                     ;
410                                     ;
411                                     ;
412                                     ;
413                                     ;
414                                     ;
415                                     ;
416                                     ;
417                                     ;
418                                     ;
419                                     ;
420                                     ;
    
```

----- INITIALIZATION TABLE FOR THE SCROLLER -----

HEADER BLOCK FOR THE SCROLLER

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SCROLLING ROM BOOTSTRAP FOR THE GT40
ROOT,T15 VT05 SIMULATOR

MACDLX 622(622)-1 26-JUN-73 16111 PAGE 1-8

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.SHTTL COMMUNICATIONS AND MISC. SUPPORT ROUTINES

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COMMUNICATIONS HANDLING ROUTINES

THE DL-11 HANDLER

```

GETDLI  TSTB   DL11IS      ;CHECK THE HOST INPUT STATUS,
        BPL    GETDL1     ;HOST DID NOT SEND ANYTHING, YET,
        MOVB   DL11IB,CHAR ;HOST SENT US A CHARACTER, PROCESS IT,
        MOV    #7,DL11IS  ;REENABLE THE HOST TELECOMMUNICATIONS,
        BIC    #-200,CHAR  ;MAKE CHARACTER JUST SEVEN BITS,
        REQ    GETDL      ;IF NULL, IGNORE IT,
        RTS    PC         ;ELSE RETURN NOW,

GETDL1I TSTB   KBDIS      ;DID USER TYPE A CHARACTER?
        BPL    GETDL      ;NO, GO BACK AND CHECK HOST MACHINE,
        MOVB   KBDIB,DL110B ;MOVE THE CHARACTER TO THE HOST,
        BR     GETDL      ;AND CHECK AGAIN FOR INPUT,
    
```

THE "GET CHARACTER" ROUTINE

```

GETCHRI JSR    PC,GETDL   ;GET A CHARACTER FROM THE HOST NOW,
        CMP    CHAR,#ALTMOD ;IS IT AN "ALTMODE"
        BNE    GETEXT     ;NO, EXIT NOW,

        JSR    PC,GETDL   ;YES, GET ANOTHER ONE NOW,
        CMP    CHAR,#'L   ;IS IT AN "L"
        BEQ    LOADER     ;YES, START LOADING NOW,
        CMP    CHAR,#'R   ;IS IT AN "R"
        BNE    GETEXT     ;NO, IGNORE THE ALTMODE AND JUST RETURN THE CHAR

        MOV    #DSTOP,JMPADD=2 ;YES, RESET, STOP DISPLAY BY INSERTING A "DSTOP
PRESTRI JMP    RESTRT     ;INSTRUCTION IN THE BUFFER, AND RESTART,
    
```

E-11

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481
482
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486
487 166630 004737 166564 GETSIX: JSR PC,GETCHR ;GET A CHARACTER NOW,
488 166634 020027 000040 CMP CHAR,#40 ;IS IT A LEGAL PRINTING CHARACTER?
489 166640 022517 BLT L,BAD ;NOPE, ABORT
490 166642 020027 000137 CMP CHAR,#137 ;IT'S BIG ENOUGH, IS IT TOO BIG?
491 166646 033114 BGT L,BAD ;YEP, ABORT,
492
493 166650 030207 GETEXT: RTS PC ;RETURN TO THE CALLER,
494
495
496 ; THIS OUTPUTS TWO CHARACTERS VIA A
497 ; JSR SCAN,OUTLIT
498 ; 'TWO CHARACTERS'
499
500 166652 112337 175616 OUTLIT: MOVB (SCAN)+,DL110B
501 166656 112337 175616 MOVB (SCAN)+,DL110B ;DOUBLE BUFFERED
502 166662 000203 RTS SCAN ;RETURN
503
504
505
506
507
508
509
510
511 ; THE "GET AN EIGHT BIT CHARACTER" ROUTINE
512 ; ---
513
514
515 ; THIS ROUTINE DIFFERS FROM THE PREVIOUS ROUTINES
516 ; IN THAT IT WILL TAKE SIX BIT CHARACTERS AND ASSEMBLE
517 ; THEM FOR THE LOADER TO USE, NOTE THAT FROM THIS POINT
518 ; ON WE WILL SWITCH TO THE LOADER DEFINITIONS OF THE
519 ; REGISTERS, THUS THE CHARACTER IS RETURNED IN
520 ; REGISTER "L,BYT" RATHER THAN CHAR (THOUGH THEY ARE
521 ; PHYSICALLY THE SAME),
522
523
524
525 166664 004737 166630 GET8: JSR PC,GETSIX ;GET A SIXBIT CHARACTER,
526 166670 010046 MOV L,BYT,-(SP) ;SAVE IT ON THE STACK,
527 166672 005723 TST (INDEX)+ ;UPDATE INDEX TO NEXT ITEM (ALL ARE *2)
528 166674 000163 166676 JMP GET8TB=2(INDEX) ;AND DISPATCH ACCORDING TO THE INDEX,
529
530 166700 000404 GET8TB: BR GET81 ;INDEX#2: ASSEMBLE FIRST CHAR
531 166702 000416 BR GET82 ;INDEX#4: ASSEMBLE SECOND CHAR
532 166704 000432 BR GET83 ;INDEX#6: ASSEMBLE THIRD AND LAST CHAR
533 ;INDEX#8: RESET INDEX TO 0 [2] AND RETRY,
534

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535							
536	166706	012723	000002	GET841	MOV	#2,INDEX	THE FOURTH INDEX IS THE SAME AS THE FIRST INDEX, JUST RESET IT AND FALL THROUGH,
537							
538							
539							
540	166712	004737	166630	GET811	JSR	PC,GETSIX	GET ANOTHER CHARACTER NOW,
541	166716	010004			MOV	L,BYT,HOLD	AND PRESERVE IT FOR NEXT TIME THROUGH,
542	166720	006300			ASL	L,BYT	NOW THROW AWAY LEFT MOST BITS OF
543	166722	006300			ASL	L,BYT	THE 8 BIT CHARACTER, NOW MERGE IN
544	166724	106300			ASLB	L,BYT	THE LEFT TWO BITS OF THE
545	166726	106116			ROLB	(SP)	NEW SIX BIT CHARACTER WITH THE SIX
546	166730	106300			ASLB	L,BYT	BITS FROM THE CHARACTER ON THE
547	166732	106116			ROLB	(SP)	STACK, 1ST CHARACTER IS NOW ASSEMBLED,
548	166734	012600			MOV	(SP)+,L,BYT	SO WE'LL RETURN IT TO THE USER,
549	166736	000207			RTS	PC	AND THEN WE SHALL RETURN TO HIM,
550							
551							
552	166740	006300		GET821	ASL	L,BYT	THE SECOND CHARACTER IS CREATED FROM
553	166742	006300			ASL	L,BYT	THE 4 RIGHT BITS OF THE PREVIOUS CHARACTER
554	166744	106300			ASLB	L,BYT	AND THE FOUR MIDDLE BITS OF THE PRESENT
555	166746	106104			ROLB	HOLD	8 BIT CHARACTER,
556	166750	106300			ASLB	L,BYT	WE WILL CREATE THE NEW 8 BIT
557	166752	106104			ROLB	HOLD	IN THIS REGISTER, SINCE IT
558	166754	106300			ASLB	L,BYT	MORE CONVENIENT, WE WILL MOVE OVER THE
559	166756	106104			ROLB	HOLD	ANSWER AT THE END,
560	166760	106300			ASLB	L,BYT	ONE MORE TO GO
561	166762	106104			ROLB	HOLD	IDONE,
562	166764	010400			MOV	HOLD,L,BYT	BRING OVER THE VALUE,
563	166766	012604			MOV	(SP)+,HOLD	AND REMEMBER THE LAST CHARACTER WE RECEIVED,
564	166770	000207			RTS	PC	AND RETURN TO THE CALLER,
565							
566							
567	166772	006100		GET831	ROL	L,BYT	FINAL CHARACTER IS EASY, JUST A
568	166774	106100			ROLB	L,BYT	SIMPLE MERGER OF LEFT TWO BITS OF
569	166776	006004			ROR	HOLD	PREVIOUS VALUE WITH RIGHT SIX BITS
570	167000	106000			RORB	L,BYT	OF LAST (4TH) CHARACTER RECEIVED,
571	167002	006004			ROR	HOLD	
572	167004	106000			RORB	L,BYT	AND WE ARE DONE,
573	167006	005726			TST	(SP)+	FINALLY THROW AWAY STACK,
574	167010	000207			RTS	PC	AND RETURN TO THE CALLER,
575							
576							
577							
578							
579							
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SCROLLING ROM BOOTSTRAP FOR THE GT40. MACDLX 622(622)-1 26-JUN-73 16111 PAGE 1-12.
BOOT,715 COMMUNICATIONS AND MISC, SUPPORT ROUTINES

589
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595

.SBTTL THE LOADER

E-15

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597
598
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602
603
604
605
606 167012 012737 173000 007010 LOADER: MOV #DISTOP,JMPADD=2 ;STOP THE GT40 BY INSERTING A "DISTOP" IN THE LI
607
608 167020 005003 CLR INDEX ;RESET THE 8 BIT ASSEMBLER TO THE FIRST CHAR
609
610
611 167022 005005 L,LD2: CLR L,CKSM ;CLEAR THE CHECKSUM
612 167024 004737 167114 JSR PC,L,PTR ;GET A BYTE NOW,
613 167030 105300 DEC L,BYT ;IS IT A ONE (HEADER)?
614 167032 001373 RNE L,LD2 ;NO, WAIT FOR THE ONE,
615
616 167034 004737 167114 JSR PC,L,PTR ;YES, SKIP OVER THE NEXT CHARACTER NOW,
617
618 167040 004737 167126 JSR PC,L,GWRD ;ASSEMBLE A WORD NOW,
619 167044 010002 MOV L,BYT,L,BC ;MOVE OVER TO THE COUNTER,
620 167046 162702 000004 SUB #4,L,BC ;REDUCE TO ACTUAL DATA COUNT,
621 167052 022702 000002 CMP #2,L,BC ;ANY DATA AT ALL?
622 167056 001433 BEQ L,JMP ;NO, MUST BE END
623 167060 004737 167126 JSR PC,L,GWRD ;YES, ASSEMBLE A DATA WORD NOW,
624 167064 010001 MOV L,BYT,L,ADR ;AND THIS MUST BE THE FIRST ADDRESS,
625
626
627 167066 004737 167114 L,LD3: JSR PC,L,PTR ;GET A BYTE OF DATA NOW,
628 167072 002006 BGE L,LD4 ;ALL DONE?
629 167074 105705 TSTB L,CKSM ;YEP, COUNTER IS MINUS; CHECK CHECKSUM,
630 167076 001751 BEQ L,LD2 ;CHECKSUM GOOD; GET NEXT COMMAND,
631
632
633 167100 004337 166652 L,BAD: JSR SCAN,OUTLIT ;BAD LOAD INFORM HOST
634 167104 175 102 ,BYTE ALTMOD,B ;SEND ALTMOD B
635 167106 000646 BR PRESTR ;AND RESTART THE DISPLAY,
636
637
638 167110 110021 L,LD4: MOVB L,BYT,(L,ADR)+ ;INSERT BYTE INTO MEMORY,
639 167112 000765 BR L,LD3 ;AND GET THE NEXT BYTE,
640
641
642
643 167114 004737 166664 L,PTR: JSR PC,GETB ;ASSEMBLE AN 8 BIT CHARACTER NOW,
644 167120 060005 ADD L,BYT,L,CKSM ;UPDATE THE CHECKSUM NOW,
645 167122 005302 DEC L,BC ;DECREMENT THE CHARACTER COUNTER,
646 167124 000207 RTS PC ;AND RETURN TO THE CALLER NOW,
647
648
649
650 167126 004737 167114 L,GWRD: JSR PC,L,PTR ;ASSEMBLE A WORD, FIRST GET A CHARACTER
    
```


651	167132	010046		MOV	L,BYT,=(SP)	JAND SAVE IT,
652	167134	034737	167114	JSR	PC,L,PTR	JAND THEN GET ANOTHER ONE,
653	167140	000300		SWAB	L,BYT	JAND THEN REASSEMBLE THE MESS,
654	167142	252600		BIS	(SP)+,L,BYT	JWITH THE FEARSOME POWER OF THE 11,
655	167144	000207		RTS	PC	JAND RETURN TO THE CALLER,
656						
657						
658						
659						
660	167146	004737	167126	L,JMPI JSR	PC,L,GWRD	JALL DONE WITH THE LOAD, ASSEMBLE
661	167152	010046		MOV	L,BYT,=(SP)	JTHE STARTING ADDRESS NOW,
662	167154	004737	167114	JSR	PC,L,PTR	JAND DON'T FORGET TO CHECKSUM IT,
663	167160	105705		TSTB	L,CKSM	
664	167162	001346		BNE	L,BAD	J A BAD CHECKSUM, ALL IS EVIL,
665						
666	167164	004337	166652	JSR	SCAN,OUTLIT	JGOOD CHKSUM, INFORM HOST
667	167170	175	107	,BYTE	ALTMOD,G	JWITH ALTMOD G
668						
669	167172	032716	000001	BIT	#1,(SP)	JDO WE WANT TO START EXECUTION?
670	167176	001401		BEQ	L,JMPI	JYES, AWAY WE GO,
671						
672	167200	000000		L,HALT	HALT	JIF NOT, HALT,
673						
674	167202	000136		L,JMPI	JMP @ (SP)+	JIF GO, THEN GO ALREADY, WHEEEE!
675						
676						
677						
678						
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691					
692					
693					
694					
695	100000	CHAR=100000			
696	104000	SHORTV=104000			
697	110000	LONGV=110000			
698	114000	POINT=114000			
699	120000	GRAPHX=120000			
700	124000	GRAPHY=124000			
701	130000	RELATV=130000			
702					
703	002000	INT0=2000			
704	002200	INT1=2200			
705	002400	INT2=2400			
706	002600	INT3=2600			
707	003000	INT4=3000			
708	003200	INT5=3200			
709	003400	INT6=3400			
710	003600	INT7=3600			
711					
712	000100	LPOFF=100			
713	000140	LPON=140			
714	000200	BLKOFF=20			
715	000300	BLKON=30			
716					
717	000004	LINE0=4			
718	000005	LINE1=5			
719	000006	LINE2=6			
720	000007	LINE3=7			
721					
722	160000	DJMP=160000			
723	164000	DNOP=164000			
724	170000	STATSA=170000			
725	173400	DSTOP=173400			
726					
727	000300	LPLITE=300			
728	000200	LPDARK=200			
729	000040	ITAL0=40			
730	000060	ITAL1=60			
731	000004	SYNON=4			
732					
733					
734	174000	STATSB=174000			
735					
736	000100	INCR=100			
737	040000	INTX=40000			
738	001777	MAXX=1777			
739	001377	MAXY=1377			
740	020000	MINUSX=20000			
741	020000	MINUSY=MINUSX			
742	017600	MAXSX=17600			
743	000077	MAXSY=77			
744	000100	MINSUY=100			

THIS IS GT40 QUICK TEST
 GIVES QUICK VISUAL TEST
 OF CONDITION OF MACHINE
 WITHOUT READING IN DIAG.

IBRIGHTEST

I STOP INTERRUPT

ITALICS OFF
 I " ON
 ISYNC ON

I LOAD GRAPH INCR
 I INTENSIFY BIT
 I BIGGEST X VECTOR
 I BIGGEST Y VECTOR
 I THE MINUS BIT

I BIGGEST X IN SHORTVEC
 I " Y IN "
 I MINUS BIT FOR Y IN SHORTVEC

745						
746						
747	167204	012737	167214	172000	MOV #FILE0,GT40PC	JSTART THE GT40
748	167212	000001			WAIT	JAND WAIT
749						
750	167214	114020			FILE0: POINT:BLKOFF	JPOINT--INVISIBLE
751	167216	000000			0	
752	167220	001377			MAXY	
753						
754	167222	112004			LONGV:INT0:LINE0	JDRAW TOP LINE
755	167224	041777			INTX:MAXX	
756	167226	000000			0	
757						
758	167230	112405			LONGV:INT2:LINE1	
759	167232	040000			INTX	JDRAW LINE TO RIGHT
760	167234	021377			MINUSX:MAXY	
761						
762	167236	113006			LONGV:INT4:LINE2	
763	167240	061777			INTX:MINUSX:MAXX	JDRAW BOTTOM LINE
764	167242	000000			0	
765						
766	167244	113407			LONGV:INT6:LINE3	
767	167246	040000			INTX	
768	167250	001377			MAXY	JDRAW LINE TO LEFT
769						
770	167252	114000			POINT	
771	167254	000400			400	
772	167256	000500			500	
773	167260	106200			SHORTV:INT1	
774	167262	057677			57677	J+X+Y
775	167264	106600			SHORTV:INT3	
776	167266	077677			77677	J+X-Y
777	167270	107200			SHORTV:INT5	
778	167272	077777			77777	J-X-Y
779	167274	107600			SHORTV:INT7	
780	167276	057777			57777	J-X+Y
781						
782	167300	114000			POINT	
783	167302	001400			1400	
784	167304	000500			500	
785	167306	133030			RELATV:INT4:BLKON	
786	167310	057677			57677	J+X+Y
787	167312	077677			77677	J+X-Y
788	167314	077777			77777	J-X-Y
789	167316	057777			57777	J-X+Y
790						
791	167320	114000			POINT	
792	167322	000400			400	
793	167324	000100			100	
794	167326	174120			STATSB:INCR+20	JTRY GRAPH MODES
795	167330	114000			POINT	
796	167332	001000			1000	
797	167334	000200			200	
798						

799	167336	120000	GRAPHX
800	167340	001010	1010
801	167342	001020	1020
802	167344	001030	1030
803	167346	001040	1040
804	167350	001050	1050
805			
806	167352	114000	POINT
807	167354	001000	1000
808	167356	001200	1200
809			
810	167360	124000	GRAPHY
811	167362	001020	1020
812	167364	001030	1030
813	167366	001040	1040
814	167370	001050	1050
815	167372	001060	1060
816			
817	167374	160000	DJMP
818	167376	167214	FILE0
819			
820			

SCROLLING ROM BOOTSTRAP FOR THE GT40
BOOT.T15 THE LOADER

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849									
850									; PAPER TAPE BOOT
851									
852		177550							;HIGH SPEED READER ADDRESS
853		177560							;LOW SPEED READER ADDRESS
854		167400							;=ORIGIN+1400
855									
856	167400	012701	160000						PTBOOT: MOV #160000,R1 ;SET MEMORY CHECK LIMITS
857	167404	012702	000004						MOV #4,R2 ;TRAP ADDRESS IS LOC. 4
858	167410	012703	167500						MOV #DEV+4,R3 ;POINTER TO DEVICE ADDRESSES
859	167414	010712							MOV PC,@R2 ;PRESET TRAP ADDRESS IN LOC. 4
860	167416	012706	000024						MOV #24,SP ;STACK SET UP AT SPECIAL ADDRESS
861	167422	014304							DEV1: MOV -(R3),R4 ;GET DEVICE ADDRESS
862	167424	005714							TST @R4 ;CHECK AVAILABILITY OF DEVICE
863	167426	000775							RMI DEV1 ;CHECK DEVICE FOR ERRORS
864	167430	010712							MOV PC,@R2 ;RESET TRAP ADDRESS AT LOC. 4
865	167432	012706	000024						MOV #24,SP ;SPECIAL ADDRESS USED AS MASK LATER
866	167436	010441							MOV R4,-(R1) ;DO MEM CHK READER STATUS ADDRESS
867									;IS MOVED
868	167440	040601							BIC SP,R1 ;SET R1=X7752, MASK IN SP=24
869	167442	010111							MOV R1,@R1 ;STORE OWN ADDRESS IN POINTER
870	167444	011102							LOOP: MOV @R1,R2 ;GET BYTE POINTER
871	167446	005214							INC @R4 ;ENABLE READER
872	167450	005714							TSTB @R4 ;TEST DONE BIT
873	167452	000376							BPL ,-2 ;WAIT UNTIL READY
874	167454	116412	000002						MOVB 2(R4),@R2 ;THEN PICK IT UP AND STORE IT
875	167460	005211							INC @R1 ;BUMP POINTER
876	167462	000227	000375						CMPB R2,#375 ;STORED JUMP OFFSET?
877	167466	001366							BNE LOOP ;NOT YET
878	167470	005222							INCB (R2)+ ;YES, ALL DONE
879	167472	000142							JMP -(R2) ;GO EXECUTE AS BRANCH
880									
881									; DEVICE ADDRESSES FOLLOW - DO NOT CHANGE THE ORDER
882									
883	167474	177560							DEV1: LSR ;LOW SPEED READER
884	167476	177550							HSR ;HIGH SPEED READER

887								
888								
889								
890		177500						
891		167500						
892	167500	12700	177500					
893	167504	005010						
894	167506	410701						
895	167510	062701	000052					
896	167514	012702	000375					
897	167520	112103						
898								
899	167522	112110						
900	167524	100413						
901	167526	130310						
902	167530	001776						
903	167532	105202						
904	167534	100772						
905	167536	116012	000002					
906	167542	120337	000000					
907	167546	001767						
908	167550	000000						
909	167552	000755						
910								
911	167554	005710						
912	167556	100774						
913	167560	005007						
914								
915	167562	017640						
916								
917	167564	002415						
918								
919	167566	112024						
920								
921	167570	000000	000000					
922	167574	167500						
923	167576	000340						

```

;
; CASSETTE BOOT
;
TACS=177500
;ORIGIN+1500
TABOOT: MOV #TACS,R0
        CLR (R0)
RES:    MOV PC,R1
        ADD #TABLE,,R1
        MOV #375,R2
        MOVB (R1),R3
;
LOOP1:  MOVB (R1)+,(R0)
        BMI DONE
LOOP2:  BITB R3,(R0)
        BEQ LOOP2
        INCB R2
        BMI LOOP1
        MOVB 2(R0),(R2)
        CMPB R3,0#0
        BEQ LOOP2
STOP:   HALT
        BR RES
;
DONE:   TST (R0)
        BMI STOP
        CLR PC
;
TABLE:  .WORD 17640
        .WORD 2415
        .WORD 112024
        .WORD 0,0
        .WORD TABOOT
        .WORD 340
;
;TA=11 CONTROL AND STATUS REGISTER
;SELECT UNIT #0
;USE FOR PIC
;R1 HOLDS ADDR. OF COMMAND TABLE
;MEMORY PTR, AND DATA FLAG
;TEST BITS
;COMMAND FROM TABLE TO TACS
;WHEN COMMAND CODE NEG., QUIT
;TEST READY AND T=REQ BITS IN TACS
;LOOP 'TIL SOMETHING COMES UP
;ADVANCE MEMORY POINTER
;IF MINUS, TRY NEXT COMMAND
;READ DATA INTO MEMORY
;FIRST BYTE READ SHOULD BE '240'
;IF O.K., GO READ ANOTHER BYTE
;HALT ON ERROR
;RESTART ON CONTINUE
;CHECK FOR ERROR
;HALT ON ERROR
;= 'JMP 0#0'
;BYTE 240: READY+T=REQ,
;BYTE 37: ILBS+READY+GO
;BYTE 15: SFB+GO
;BYTE 5: READ+GO
;BYTE 24: READ+ILBS
;BYTE 224: READ+ILBS+E,O, TABLE
;THESE ARE FILLER WORDS
;POWER UP VECTOR AND PRIORITY
;
    
```

IR11=0B BULK STORAGE PROGRAM LOADER LISTING

925
 926
 927 167600
 928
 929 167600 010702
 930 167602 000451
 931 167604 177462
 932 167606 000005
 933
 934 167610 010702
 935 167612 000445
 936 167614 177406
 937 167616 000005
 938
 939
 940 167620 010702
 941 167622 000417
 942 167624 177344
 943 167626 000005
 944 167630 004003
 945 167632 100000
 946 167634 024000
 947
 948
 949 167636 010702
 950 167640 000410
 951 167642 172524
 952 167644 060003
 953 167646 060011
 954 167650 000200
 955 167652 100000
 956
 957
 958 167654 010702
 959 167656 000423
 960 167660 176716
 961
 962
 963 167662 000005
 964 167664 010200
 965 167666 005720
 966 167670 012001
 967 167672 005311
 968 167674 005720
 969 167676 012041
 970 167700 031011
 971 167702 001776
 972 167704 005720
 973 167706 031041
 974 167710 001406
 975 167712 000112
 976
 977
 978 167714 167600

IR11=0B BULK STORAGE PROGRAM LOADER LISTING
 ;ORIGIN=1600 ;KEEP TRACK OF ORIGIN
 RF11: MOV PC,R2 ;FIXED HEAD DISK (256 KW)
 BR OTHER
 177462
 5
 RK11: MOV PC,R2 ;MOVING HEAD DISK (CARTRIDGE)
 BR OTHER
 177406
 5
 TC11: MOV PC,R2 ;ADDRESS OF WORD COUNT
 BR TAPES ;LAST COMMAND
 177344 ;FIRST COMMAND
 5 ;DONE MASK
 4003 ;ERROR MASK
 100000
 24000
 TM11: MOV PC,R2 ;ADDRESS OF BYTE COUNT
 BR TAPES ;LAST COMMAND
 172524 ;FIRST COMMAND
 60003 ;DONE MASK
 60011 ;ERROR MASK
 200
 100000
 RP11: MOV PC,R2 ;MOVING HEAD DISK (PACK)
 BR OTHER
 176716
 TAPES: RESET ;GET THE ADDRESS OF THE BRANCH
 MOV R2,R0 ;R0 TO POINT AT LAST COMMAND
 TST (0)+ ;GET THE WORD COUNT ADDRESS
 MOV (0)+,R1 ;SET UP FOR ADVANCE 1 RECORD
 DEC (1) ;MOVE R0 TO FIRST COMMAND
 TST (0)+ ;COMMAND WORD TO COMMAND REG.
 MOV (0)+,-(1) ;LOOK FOR DONE INDICATORS
 BIT (0),(1) ;NONE SET, TRY AGAIN
 BEQ ,=2 ;DONE FIRST COMMAND, CHECK FOR ERROR
 TST (0)+ ;LOOK FOR SET ERROR BITS
 BIT (0),-(1) ;NO ERRORS - TRY THE READ
 BEQ OTHER ;RERUN FOR ERRORS
 AGAIN: JMP (2)
 RFEVC: RF11 ;RF11 POWER UP VECTOR

SCROLLING ROM BOOTSTRAP FOR THE GT40
BOOT.T15 THE LOADER

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979	167716	000340		340	
980					
981	167720	010702		RC111	MOV PC,R2
982	167722	000401			BR OTHER
983	167724	177450			177450
984					
985					
986	167726	000005		OTHER1	RESET
987	167730	010200			MOV R2,R0
988	167732	005720			TST (0)+
989	167734	012001			MOV (0)+,R1
990	167736	012711	177000		MOV #-1000,(1)
991	167742	011041			MOV (0),-(1)
992	167744	032711	100200		BIT #100200,(1)
993	167750	001775			BEO ,=4
994	167752	100757			BMI AGAIN
995	167754	005007			CLR PC
996					
997	167756	000000			0
998	167760	167610		RKVEC1	RK11
999	167762	000340			340
1000	167764	167720		RCVEC1	RC11
1001	167766	000340			340
1002	167770	167654		RPVEC1	RP11
1003	167772	000340			340
1004	167774	167620		TCVEC1	TC11
1005	167776	000340			340
1006					

;FIXED HEAD DISK (64KW)

;ADRS OF WORD COUNT (COMMAND*2)
;COMMAND WORD (5) IS THE RESET

;R0 TO POINT AT WORD COUNT ADRS
;POINT TO ADDRESS
;WORD COUNT ADDRESS TO R1
;LOAD WORD COUNT
;COMMAND TO COMMAND REGISTER
;CHECK FOR ERROR OR DONE
;IF NEITHER, KEEP LOOKING
;ERROR, TRY AGAIN

;FILLER
;RK POWER UP VECTOR

;RC POWER UP VECTOR

;RP POWER UP VECTOR

;TC11 POWER UP VECTOR

SCROLLING ROM BOOTSTRAP FOR THE GT40
BOOT.T15 THE LOADER

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*000-1

,END

SCROLLING ROM BOOTSTRAP FOR THE GT40
 ROOT,T16 CROSS REFERENCE TABLE

AGAIN	167712	974#	993																
ALTMOD =	001175	139#	465	632	666														
BELL	166250	278	310#																
BLIMIT =	007020	132#	135	223	244	329	348	395	399										
BLKOFF =	002020	713#	749																
BLKON =	001030	714#	784																
BSTART =	001020	131#	331	351	368	398													
CHAR =	101020	82#	102	267	269	271	298*	315*	327	338*	345	444*	446*	465					
		469	471	487	489	694#													
CORSTR =	201024	134#	192																
COUNTR =	000005	89#	105	306*	313*	317*													
CR	166205	207#																	
CRLF =	005215	138#	226																
DEV	167474	857	882#																
DEV1	167422	864#	862																
DISJMP =	167020	141#	359	397	398	399	415												
DISTOP =	170020	142#	474	605															
DJMP =	160020	721#	816																
DL1116 =	175612	120#	121	444															
DL1115 =	175610	119#	120	184*	442	445*													
DL1108 =	175616	122#	452*	499*	520*														
DL1105 =	175614	121#	122	188*	206	228*													
DNOP =	164020	722#																	
DONE	167554	899	913#																
DSTOP =	170020	724#																	
ENDCOR	166136	195#	196																
FF	166256	283	313#																
FFLAGOP	166262	308	315#	318															
FILE0	167214	746	749#	817															
GETCHR	166564	266	464#	486															
GETDL	166516	442#	447	451	453	464	468												
GETDL1	166546	443	450#																
GETEXT	166650	466	472	492#															
GETSIX	166630	486#	524	539															
GET8	166664	524#	642																
GET8TB	166700	527	529#																
GET81	166712	529	539#																
GET82	166740	530	551#																
GET83	166772	531	566#																
GET84	166706	535#																	
GRAPHX =	120000	698#	798																
GRAPHY =	124000	699#	809																
GTRUSE	166424	368#	391																
GT40PC =	172000	127#	128	368*	402	746*													
GT40SR =	172002	128#	310#																
HEADER	166474	358	397	403	409#														
HOLD =	000000	87#	540*	554*	556*	558*	560*	561	562*	568*	570*								
HSR =	177550	851#	883																
INCR =	000100	735#	793																
INDEX =	000003	106#	526	527	535*	607*													
INSERT	166350	291	299	337	345#														
INSRTL	166406	349	352	357#															
INSRTX	166422	347	362#																
INTX =	040000	736#	754	758	762	766													

NOTHER	166042	193	199#															
NUMLIN =	000040	136#	223	224	313	399												
NXTCHR	166132	266#	268	274	293	303	311	319	322									
ORIGIN =	166000	117#	173	853	890	926												
OTHER	167726	929	934	958	973	981	985#											
OUTLIT	166652	189	499#	632	665													
PC =	000207	74#	266*	276*	291*	299*	306	316*	337*	352*	355*	362*	448*	464*				
		468*	486*	492*	524*	539*	548*	563*	573*	611*	615*	617*	622*	626*				
		642*	645*	649*	651*	654*	659*	661*	858	863	893	912*	928	933				
		939	948	957	987	994*												
POINT =	114020	697#	749	769	781	790	794	805										
POINTR =	000071	83#	103	236*	238*	244*	345*	346	348	350	351*	357	358*	359*				
		362*																
PRESTR	166624	475#	634															
PTBOOT	167400	855#																
RCVFC	167764	999#																
RC11	167720	980#	999															
RELATV =	130000	707#	784															
RES	167506	893#	908															
RESTRT	160000	220#	475															
RFVEC	167714	977#																
RF11	167500	928#	977															
RKVEC	167760	997#																
RK11	167510	933#	997															
RPVEC	167770	1001#																
RP11	167654	957#	1001															
R0 =	000000	67#	82	891*	892*	818*	900	904	910	963*	986*							
R1 =	000001	68#	83	855*	865*	817*	868*	869	874*	893*	894*	896	898	965*				
		988*																
R2 =	000002	69#	84	856*	858*	813*	869*	873*	875	877*	878	895*	902*	904*				
		928*	933*	939*	948*	917*	963	980*	986									
R3 =	000003	70#	85	857*	867	806*	900	905										
R4 =	000004	71#	87	860*	861	865	870*	871	873									
R5 =	000005	72#	89															
SCAR =	000006	85#	106	189*	192*	193*	195*	199	204	223*	226*	231*	234	236				
		239	271*	272*	273	275*	276	325*	327	329	331*	334*	335*	336				
		350*	353*	354*	499	510	501*	632*	665*									
		235	244#															
SETJUN	166126	235	244#															
SETLP1	166074	226#	228															
SETLP2	166110	234#	241															
SETLP3	166116	238#	240															
SETUP	166432	231	389#															
SHORTV =	174200	695#	772	774	776	778												
SP =	000006	73#	187*	204*	220*	122*	525*	544*	546*	547	562	572	650*	653				
		660*	668	673	859*	164*	867											
START	166000	185#																
STATSA =	170000	723#																
STATSB =	174000	733#	793															
STOP	167550	907#	911															
SYNON =	000004	732#																
TAB	166222	280	298#	302														
TABCNT =	000002	84#	104	224*	227*	234*	239*	287*	292*	300*	301							
TABLE	167562	894	914#															
TABOOT	167500	891#	921															

SCROLLING ROM FOOTSTAP FOR THE GT40
 BOOT, T16 CROSS REFERENCE TABLE

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TACS	= 177500	889#	891						
TAPES	167662	940	949	962#					
TCVEC	167774	1003#							
TC11	167620	939#	1003						
TMPEND	= 007776	133#	187	220					
TK11	167636	948#							
VT	166244	232	306#						
.	= 172000	173#	853#	872	890#	194	926#	970	992

ADD	276	643	894													
ASL	275	541	542	551	552											
ASLB	543	543	553	555	557	559										
BEQ	235	328	447	470	621	629	169	901	906	970	973	992				
BGE	268	270	627													
BGT	228	247	318	490												
BMIS	274															
BIC	335	446	867													
BIS	220	653														
BIT	321	346	668	969	972	991										
BITB	900															
BLD	330	349														
BLT	468															
BMI	562	899	903	911	993											
BNE	302	347	466	472	613	663	176									
BPL	207	443	451	872												
BR	196	241	278	279	280	281	182	283	293	303	308	311	319	332	453	
	529	530	531	634	638	908	929	934	940	949	958	981				
CLR	195	200	315	338	353	354	360	607	610	892	912	994				
CMP	267	269	273	329	348	357	465	469	471	487	489	620				
CMPB	327	875	905													
DEC	227	239	317	644	966											
DECB	612															
HALT	671	927														
INC	188	292	300	334	870	874										
INCB	877	980														
JMP	475	527	673	878	974											
JSR	189	266	291	299	316	337	152	464	468	486	524	539	611	615	617	
	322	625	632	642	649	651	159	661	665							
MOV	186	187	192	193	204	223	124	226	231	234	236	238	244	271	287	
	298	313	315	322	325	331	136	350	351	358	359	368	445	474	525	
	535	540	547	561	562	605	118	623	650	660	746	855	856	857	858	
	859	860	863	864	865	868	169	891	893	895	928	933	939	948	957	
	963	965	968	980	986	988	189	990								
MOVB	326	345	444	452	499	500	137	873	896	898	904					
RESET	185	960	965													
ROL	566															
ROLB	544	545	554	556	558	560	167									
ROR	568	570														
RORB	569	571														
RTS	355	362	448	492	501	548	163	573	645	654						
SUB	272	619														
SWAB	652															
TST	199	526	572	861	910	964	967	971	987							
TSTB	206	442	450	628	662	871										
WAIT	747															
,BYTE	633	666														
,ENABL	36															
,END	1007															
,PAGE	55	109	162	257	425	595	189	820								
,SBTTL	54	161	256	424	594											
,TITLE	2															
,WORD	190	389	390	391	392	394	395	396	397	398	399	401	402	403	405	
	409	410	411	412	413	414	415	914	916	918	920	921	922			

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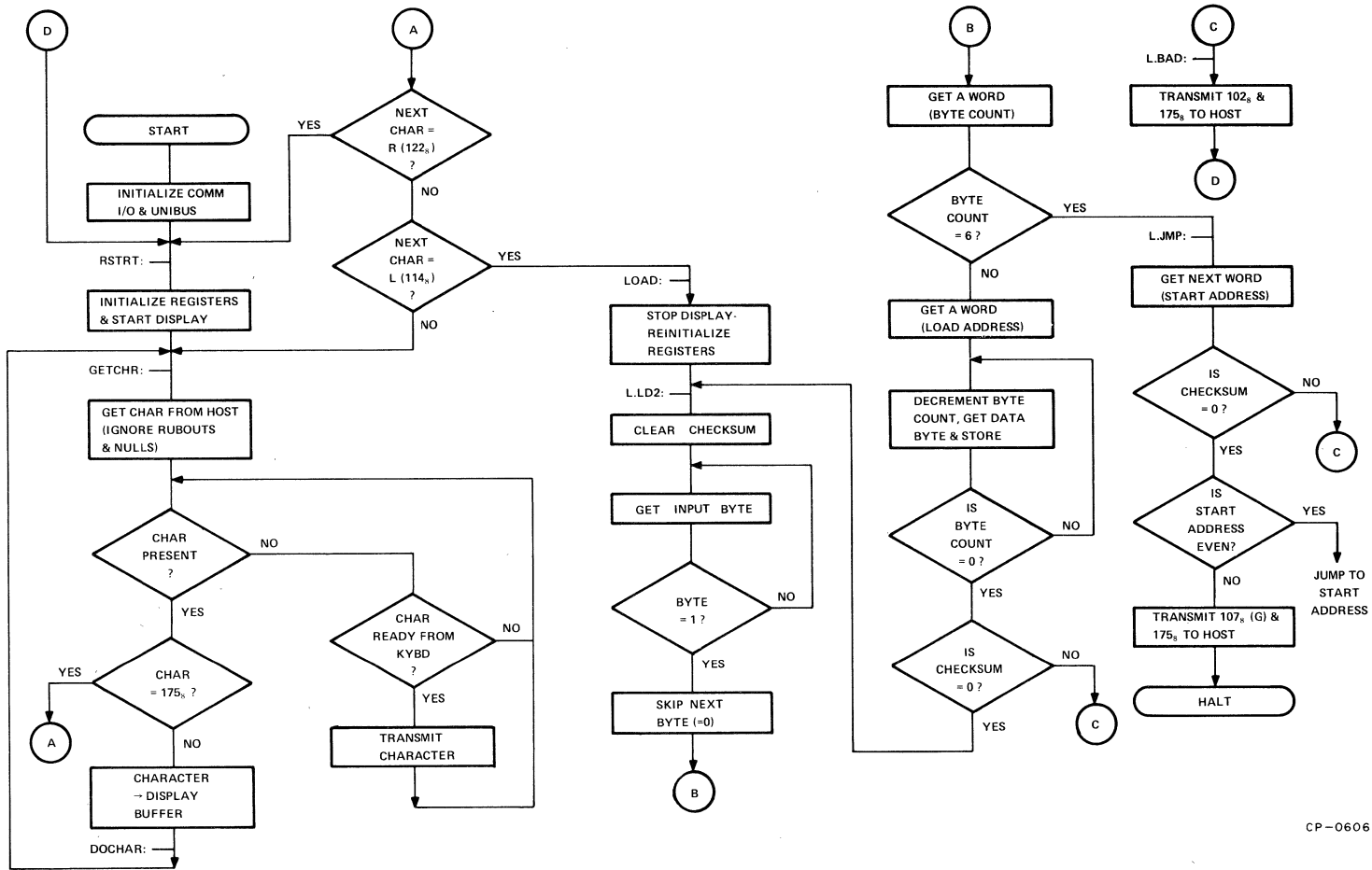


Figure E-1 Communications Bootstrap Loader Flow Diagram

Reader's Comments

GT40/42 USER'S GUIDE
EK-GT40-OP-002

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What is your general reaction to this manual? In your judgment is it complete, accurate, well organized, well written, etc.? Is it easy to use? _____

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What faults do you find with the manual? _____

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Does it satisfy *your* needs? _____ Why? _____

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Please describe your position. _____

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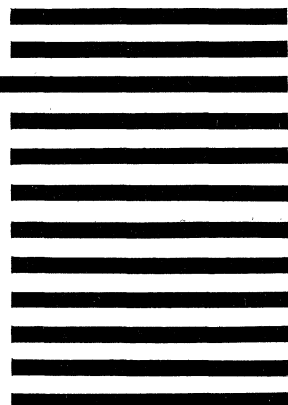
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