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PDP-X Technical Memorandum # 27

Title: Marketing Suggestions for First Implementations

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## I. Summary

After studying Technical Memoranda #12, #13, and #16, the following marketing conclusions have been reached:

1. The first models of PDP-X that should be offered are:
   a. Level II hardware (extended instruction set), with 8-32K fast (~0.75 μsec) memory, level II software, and optional priority interrupt system, and
   b. Level II hardware, with 4K memory, ASR-33, and modified level II assembler, level I FORTRAN (delayed), DDT, leader, etc.

   Both versions should be announced at the same time.
2. Memory speeds for the PDP-X should be around 0.75 μsec (fast) and 2.0 μsec (slow). The level II processors should all be fast, but capable of using the slower memories. The level I processor should only be offered with slow memory. It is not clear that there is a requirement for memory speeds slower than 2.0 μsec.
3. First deliveries should include high-speed paper tape, DECtape, and extra memory (up to 32K). Within 4 months of first deliveries, the following options should be in production: small display, API, all CPU options, disc, IBM magnetic tape, A/D and D/A.

card readers, line printers. Within 8 months of first deliveries, memory protection, all forms of bulk storage including disc packs, big displays, dataphones, and 360 interfaces should be available.

These conclusions are discussed in more detail in the body of this memorandum.

## II. Discussion

### A. Introduction

At the request of Ed DeCastro and Henry Burkhardt, we have examined the following questions:

1. What should the first PDP-X model(s) be?
2. What memory speeds should be offered?
3. What instruction sets should be implemented?
4. How many levels of API should be offered -- optional and standard?
5. How many accumulators should be offered?
6. What type of memory protection, and when?
7. What standard I/O should be offered?
8. When should software be available? Peripherals?

Our thoughts on these questions, and several others, are discussed below. In this discussion, we have

assumed familiarity with the following Technical Memoranda:

#12 - Detailed Model Specifications

#13 - PDP-X Processor Description

#16 - PDP-X System Architecture (Revised)

#23 - PDP-X Software Schedule

B. Possible Range of Models

In order to more clearly define the possibilities of models of the PDP-X that might be introduced, we started by expanding the table of models shown in Technical Memorandum #12. This resulted in Table I: Range of Possible Models.

The chief points of interest in Table I are the new possibilities shown. Model $I_s$ corresponds to $I_a$ of the original table, and $I_f$ is equal to $I_b$. $II_{2,f}$, $II_{3,f}$, and $II_{4,f}$ correspond directly to $II_a$, $II_b$, and $II_c$, respectively. But, a set of slow versions of these models ($II_{2,s}$, $II_{3,s}$, $II_{4,s}$) has been shown, and a new pair of models ($II_{1,f}$ and $II_{1,s}$) have been suggested. These latter models correspond to a suggested $II_{\emptyset}$ set once mentioned but never documented. Although a set of level III models was also considered, it was not documented at this time.

Table I: Range of Possible Models

| Model | Register Sets | Instruction Set | Speed | Sizes | Add Time | Standard I/O | Interrupt Structure | Protection System | Multiply Time | Index Time | Software System |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_s$ | 2 in core | basic | 2µsec | 4-32K | 8µsec | ASR-33 | 2 levels | none | sub-routine | 2µsec | Assembler-I<br>Basic FORTRAN<br>Loader-I |
| $I_f$ | | | .75µsec | 4-32K | 3µsec | | | | sub-routine | .75µsec | ODT or DDT-I<br>PIP<br>Subroutine Library<br>Editor |
| $II_{1,s}$ | 2 hard-ware | Extended | 2µsec | 4-32K | 4µsec | ASR-33 | 2 levels | none | <40µsec | 0 | Basic Version of Assembler-I<br>Basic FORTRAN<br>Loader-I |
| $II_{1,f}$ | | | .75µsec | 4-32K | 1.5µsec | | | | <14µsec | 0 | ODT or DDT-I<br>Editor<br>PIP<br>Subroutine Library<br>(8K and above systems can use next level software) |
| $II_{2,s}$ | | | 2µsec | 8-32K | 4µsec | ASR-33 will work, but high-speed paper tape reader and punch highly recommended | 8 levels fully nested | | <40µsec | 0 | Assembler-II (full version)<br>FORTRAN IV<br>Single User Monitor<br>Loader-II<br>DDT-II<br>Editor<br>PIP<br>JOSS<br>Subroutine Library<br>System Builder<br>Library Update |
| $II_{2,f}$ | | | .75µsec | 8-32K | 1.5µsec | | | | <14µsec | 0 | |
| $II_{3,s}$ | 8 hard-ware | | 2µsec | 8-32K | 4µsec | | | | <40µsec | 0 | |
| $II_{3,f}$ | | | .75µsec | 8-32K | 1.5µsec | | | | <14µsec | 0 | |
| $II_{4,s}$ | | | 2µsec | 16-128K | 4µsec | High speed paper tape reader and punch, bulk storage, and two teletypes | | User/Exec modes and paging | <40µsec | 0 | All of Level II, 2 (above) plus Background/ Foreground Monitor or Limited Time-Sharing Monitor |
| $II_{4,f}$ | | | .75µsec | 16-128K | 1.5µsec | | | | <14µsec | 0 | |

Table II: Implementation of Processor Models, was created to summarize the various possibilities and to indicate the probable order of implementation and/or announcement. In our opinion, this order should be:

1. First three fast-memory versions of model II ($II_{1,f}$, $II_{2,f}$, $II_{3,f}$), all announced and available at the same time.
2. Background/foreground version of Model II ($II_{4,f}$), available second, perhaps announced with previous three models.
3. Slow version of model I ($I_s$).
4. All slow versions of model II, implemented with slow memories on fast processors.
5. Any model III versions to be introduced.

We do not think it will prove necessary or profitable to introduce a fast version of model I.

C. Memory Speeds

We have examined the question of memory speeds in the light of known competition and anticipated advances, but in the absence of actual dollar figures for various speeds.

Table II: Implementation of Processor Models

| Model | Processor Characteristics | Memory Speed: Fast (~.75 μsec) | Memory Speed: Slow (~2μsec) |
|---|---|---|---|
| I | Basic instruction set<br>In-memory registers<br>Basic software | Probably never implemented | Third implementation |
| $II_1$<br>$II_2$<br>$II_3$ | Extended instruction set<br>Hardware registers<br>Powerful software for single users | All three versions in first implementation | Fourth implementation (slow memory w/ fast processor) |
| $II_4$ | Extended instruction set<br>Hardware registers<br>Protection hardware<br>Two-user software | Second implementation | Fourth implementation (slow memory w/ fast processor) |
| III | Extended instruction set plus double precision and floating-point hardware<br>Multi-user software | Fifth implementation | Never offered |

because a 36 μsecond add time could not be tolerated). In addition, an 80 μsecond cycle time may prove psychologically unacceptable, no matter what price, where 2.0 μseconds, well within today's technology, would prove acceptable.

D. What Should the First Products Be?

The first products to be announced, sold, and delivered should correspond to the fast-memory versions of model II hardware. A variety of configurations, from 4K with ASR-33 through 32K with high-speed I/O, bulk storage, and API, should be announced initially. The model used for background/foreground can be developed in its announcement, or it can be announced with the first configurations.

As stated above, the first models should have fast, state-of-the-art, memories and the extended instruction set to establish this architecture as best in the field. The software offered for all but the 4K version should include, initially, a stripped-down version of the assembler and loaders, editors, and debugging systems capable of operating in a stand-alone environment. FORTRAN can wait until later and probably can be the same version as offered on model I hardware.

All hardware except this basic FORTRAN should be ready for demonstration on announcement day.

Memory protection, in the form of user/executive modes and paging, is highly desirable and necessary for two-user or multi-user modes. But, does it provide the proper protection in a single-use industrial or process control environment, or whether another scheme should be offered?

Model II, with state-of-the-art hardware and memory speeds, has been chosen for first implementation because this model was felt to be most generally acceptable to all markets. However, if a version of model II can be produced with slower memories (2.0 μseconds) and processor at a significant cost savings (60% or less of the fast model II), then serious consideration should be given to its implementation as the first version.

E. Schedule (and Suggested Prices) for Options

At announcement time, we should like to demonstrate:

1. A PDP-X with 8-16K, high-speed paper tape, API, and bulk storage, and
2. A second PDP-X with 4K and ASR-33.

First deliveries should begin 3-4 months after an-

nouncement, with the availability of options as shown on the following schedule (suggested prices of options shown in some cases):

1. First deliveries should include:
   a. High-speed paper tape I/O
   b. Extra memory
   c. DECtape ($8-10K for control and two transports)
2. Within 4-6 months of first deliveries, we should ship:
   a. All CPU options
   b. Small display ($1-2K for control; large screen is desirable)
   c. A/D and D/A equipment
   d. IBM-compatible magnetic tape ($6K for control)
   e. Disc ($10-15K for control and 250-500K words, expandable to 2 million words)
   f. Card reader ($4-6K) and line printer ($5-10K)
3. Within 8-12 months we should be ready to ship:
   a. Memory protection
   b. Big, powerful displays
   c. 360 interfaces

d. Dataphone interfaces ($3-5K)

e. Large mass storage (disc paks or CRAM-typeunit)

F. Further Plans

The second announcements should concern background/foreground models of the level II hardware (if not announced initially) and the availability of model I processors. Subsequently, the availability of slower-memory model II processors can be announced if cost savings can be effected. These announcements should probably be 12-18 months after first introduction of the first PDP-X models.