KS10 Maintenance Guide

Company Confidential

Volume I

digital

EK-OKS10-MG-001

KS10 Maintenance Guide

Volume I

digital equipment corporation • marlboro, massachusetts

First Edition, June 1979

Printed in U.S.A.

To the Reader:

CONFIDENTIALITY - This guide contains Company Confidential information and is intended for use by DIGITAL field engineers only. Refer to the Field Service Methods and Procedures Manual for DIGITAL policy pertaining to handling confidential information.

OBJECTIVE - The objective of this guide is to organize and present that information which is most used during KS10 maintenance activities. This document is directed toward qualified KS10-trained technical personnel.

To maintain accuracy and improve this guide in subsequent revisions, we need feedback. Please forward any information or suggestions that would increase the usefulness of the guide to:

LCG Tools Supervisor
MR1-1 S35

RELATED KS10 DOCUMENTS

KS10-Based DECSYSTEM-2020 Technical Manual, EK-0KS10-TM-002

KS10-Based DECSYSTEM-2020 Installation Manual, EK-0KS10-IN-001

ORGANIZATION - The guide is divided into six sections.

1. GENERAL INFORMATION consists of miscellaneous maintenance information which cannot be classified and filed in any of the remaining four hardware sections.

2. SWITCHES/JUMPERS contains information pertaining to hardware switch positions and jumper connections.

3. TABLES/MAPS describes the process tables and bit maps associated with the KS10 mainframe and peripheral equipment.

4. CHECKS/ADJUSTMENTS consists of check and adjustment procedures performed during preventive and corrective maintenance.

5. DIAGRAMS/MULS contains power supply layouts and module utilization lists associated with KS10-based systems.

6. SOFTWARE contains standard boot procedure, pre-boot error messages, diagnostic program hierarchies, standard console messages, console commands, and console error messages.

The information in each hardware section is indexed and arranged according to unit and subsystem (i.e., CPU, memory, disk, tape, and I/O).

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NOTES

TELEPHONE NUMBERS

Digital Diagnostic Center (10/20/ 11/70, and VAX)

NORAM Colorado Springs, Colorado

800-525-6570 Use this number to log a service call for DDC response.

303-599-4000 Use this number to contact specific DDC engineers. This number should also be used by Canada to contact DDC.

Software Hot Line (10/20 only)
617-481-9511 Extension 6492 Marlboro, Massachusetts

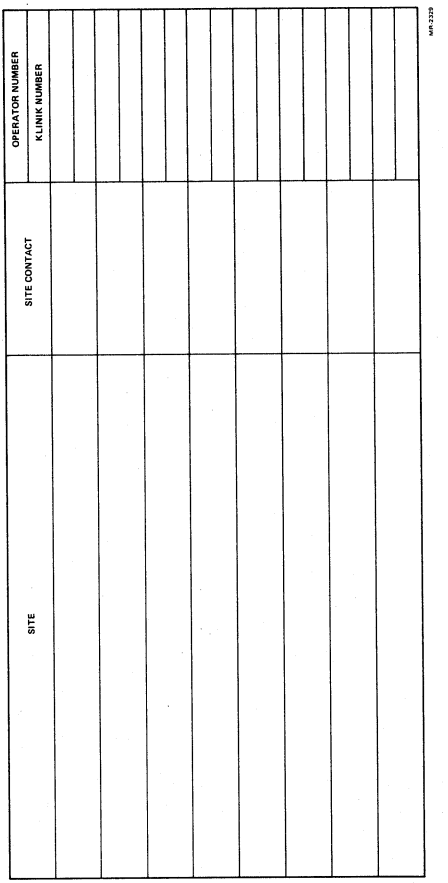
Diagnostic Hot Line (10/20 only)
617-481-9511 Extension 6556 Marlboro, Massachusetts

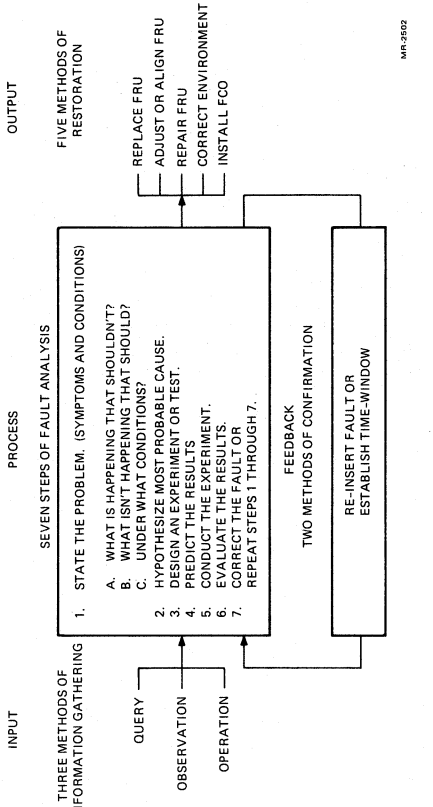
Technical Assistance Centers
Corporate (10/20 only)
617-481-9511 Extension 6903 or 6904 Marlboro, Massachusetts

Corporate (non-10/20)
617-897-5111 Extension 5901 Maynard, Massachusetts

Region

District


SITE
SITE CONTACT
OPERATOR NUMBER
KLINIK NUMBER


INPUT
PROCESS
OUTPUT
THREE METHODS OF INFORMATION GATHERING
SEVEN STEPS OF FAULT ANALYSIS
FIVE METHODS OF RESTORATION
QUERY
OBSERVATION
OPERATION
1. STATE THE PROBLEM. (SYMPTOMS AND CONDITIONS)
A. WHAT IS HAPPENING THAT SHOULDN'T?
B. WHAT ISN'T HAPPENING THAT SHOULD?
C. UNDER WHAT CONDITIONS?
2. HYPOTHESIZE MOST PROBABLE CAUSE.
3. DESIGN AN EXPERIMENT OR TEST.
4. PREDICT THE RESULTS
5. CONDUCT THE EXPERIMENT.
6. EVALUATE THE RESULTS.
7. CORRECT THE FAULT OR
REPEAT STEPS 1 THROUGH 7.
FEEDBACK
TWO METHODS OF CONFIRMATION
RE-INSERT FAULT OR
ESTABLISH TIME-WINDOW
REPLACE FRU
ADJUST OR ALIGN FRU
REPAIR FRU
CORRECT ENVIRONMENT
INSTALL FCO
MR-3502

Module Configuration Information

1. M7819 (DZ11) (Lowest Acceptable CS Rev E) - A fully configured KS10-System will have up to four M7819 (DZ11) modules. Their address and vector assignments will be according to the following chart.

2. M7867 (DUP11-DA) (Lowest acceptable CS Rev F) - A fully configured KS10 subsystem will have up to two M7867 (DUP11-DA) modules. Their address and vector assignments will be according to the following chart.

3. M8204 (KMC11) (Lowest acceptable CS Rev D) - A fully configured KS10 system will have one M8204 (KMC11) module. Its address and vector assignments will be according to the following chart.

Address and Vector Table

Device	#	Address	Vector	Unit	BR Level
RH11	1	776700	254	1	6
	2	772440	224	3	6
LP20	1	775400	754	3	4
	2	775420	750	3	4
DZ11	1	760010	340	3	5
	2	760020	350	3	5
	3	760030	360	3	5
	4	760040	370	3	5
KMC11	1	760540	540	3	5
	2	760550	550	3	5
DUP11	1	760300	570	3	5
	2	760310	600	3	5
CD11	1	777160	230	3	4

UNIBUS PIN ASSIGNMENTS
(BY PIN NUMBERS)

AA1	INIT L
AA2	POWER (+5 V)
AB1	INTR L
AB2	GROUND
AC1	DOO L
AC2	GROUND
AD1	DO2 L
AD2	DO1 L
AE1	DO4 L
AE2	DO3 L
AF1	DO6 L
AF2	DO5 L
AH1	DO8 L
AH2	DO7 L
AJ1	D10 L
AJ2	DO9 L
AK1	D12 L
AK2	D11 L
AL1	D14 L
AL2	D13 L
AM1	PA L (D16 L)
AM2	D15 L
AN1	GROUND
AN2	PB L (D17 L)
AP1	GROUND
AP2	BBSY L
AR1	GROUND
AR2	SACK L
AS1	GROUND
AS2	NPR L
AT1	GROUND
AT2	BR 7 L
AU1	NPG H
AU2	BR 6 L
AV1	BG 7 H
AV2	GROUND
BA1	BG6 H
BA2	POWER (+5 V)
BB1	BG 5 H
BB2	GROUND
BC1	BR 5 L
BC2	GROUND
BD1	GROUND
BD2	BR 4 L
BE1	GROUND
BE2	BG 4 H
BF1	ACLO L
BF2	DCLO L
BH1	AO1 L
BH2	AOO L
BJ1	AO3 L
BJ2	AO2 L
BK1	AO5 L
BK2	AO4 L
BL1	AO7 L
BL2	AO6 L
BM1	AO9 L
BM2	AO8 L
BN1	A11 L
BN2	A10 L
BP1	A13 L
BP2	A12 L
BR1	A15 L
BR2	A14 L
BS1	A17 L
BS2	A16 L
BT1	GROUND
BT2	C1 L
BU1	SSYN L
BU2	CO L
BV1	MSYN L
BV2	GROUND

UNIBUS PIN ASSIGNMENTS
(BY SIGNAL NAME)

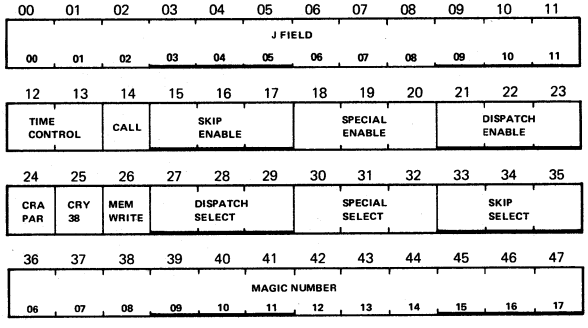
AOO L	BH2
AO1 L	BH1
AO2 L	BJ2
AO3 L	BJ1
AO4 L	BK2
AO5 L	BK1
AO6 L	BL2
AO7 L	BL1
AO8 L	BM2
AO9 L	BM1
A10 L	BN2
A11 L	BN1
A12 L	BP2
A13 L	BP1
A14 L	BR2
A15 L	BR1
A16 L	BS2
A17 L	BS1
ACLO L	BF1
BBSY L	AP2
BG4 H	BE2
BG5 H	BB1
BG6 H	BA1
BG7 H	AV1
BR4 L	BD2
BR5 L	BC1
BR6 L	AU2
BR7 L	AT2
CO L	BU2
C1 L	BT2
DOO L	AC1
DO1 L	AD2
DO2 L	AD1
DO3 L	AE2
DO4 L	AE1
DO5 L	AF2
DO6 L	AF1
DO7 L	AH2
DO8 L	AH1
DO9 L	AJ2
D10 L	AJ1
D11 L	AK2
D12 L	AK1
D13 L	AL2
D14 L	AL1
D15 L	AM2
GROUND	AB2
GROUND	AC2
GROUND	AN1
GROUND	AP1
GROUND	AR1
GROUND	AS1
GROUND	AT1
GROUND	AV2
GROUND	BB2
GROUND	BC2
GROUND	BD1
GROUND	BE1
GROUND	BT1
GROUND	BV2
INIT L	AA1
INTR L	AB1
MSYN L	BV1
NPG H	AU1
NPR L	AS2
PA L (D16 L)	AM1
PB L (D17 L)	AN2
+5 V*	AA2
+5 V*	BA2
SACK L	AR2
DCLO L	BF2
SSYN L	BU1

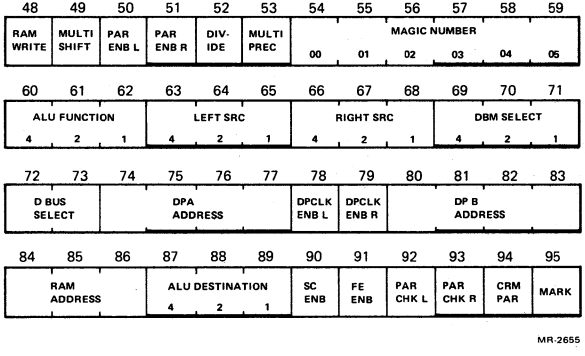
NOTES

1. +5 V is wired to these pins to supply power to the bus terminator only.

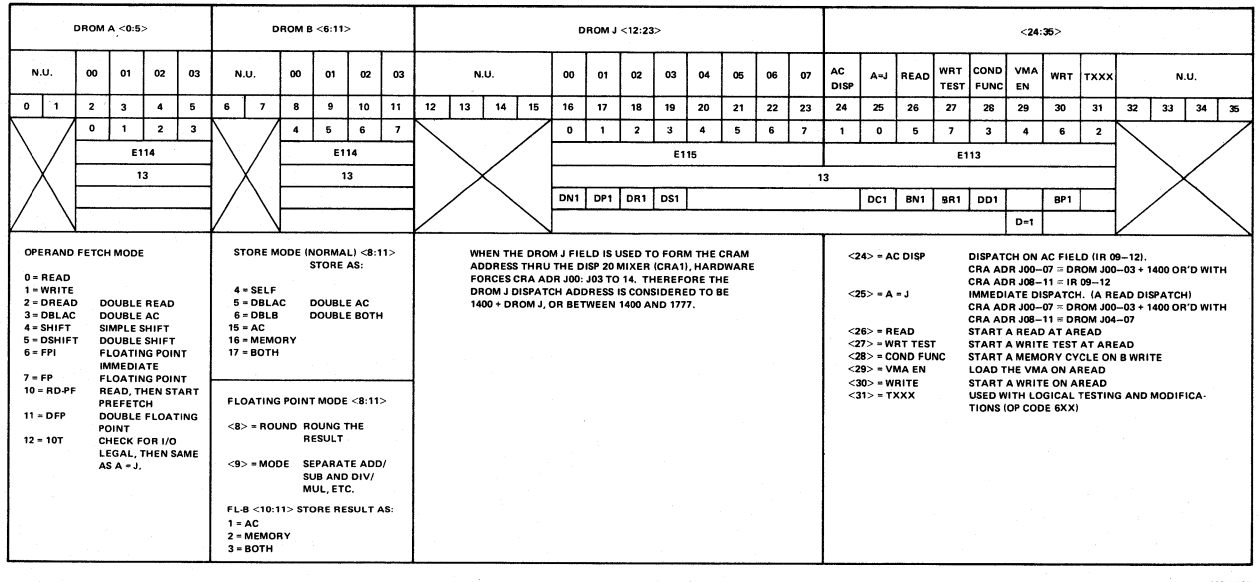
2. +5 V should never be connected via the Unibus between system units.

EC – COMMAND – BREAKDOWN





MR-2655



MR-2837

Dispatch Word Format

NOTES

FIELD	J <00:11>											DATA PATH <12:35> (DPE1 & 2)																							
												ALU FUNCTIONS <12:23>												DATA PATH ADDRESS <24:35>											
SIGNAL	J00	J01	J02	J03	J04	J05	J06	J07	J08	J09	J10	J11	FUNC			LSRC			RSRC			DEST			NU		DPA ADR				NU		DPB ADR			
													04	02	01	04	02	01	04	02	01	04	02	01			10	04	02	01			10	04	02	01
μWORD BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
CRAM BIT	00	01	02	03	04	05	06	07	08	09	10	11	60	61	62	63	64	65	66	67	68	87	88	89			74	75	76	77			80	81	82	83
SLOT	12												11														11						11			
PIN													AH2	AR2	BH2	BR2	CH2	CR2	DH2	DR2	EM2	BS2	CJ2	CS2			EJ1	ES1	FJ1	FS1			BJ1	BS1	CJ1	CS1
DEFAULT	(CRA1) NEXT MICROCODE ADDRESS												D = 44						F = LSRC			D = 3					2901						D = 0			

<00:35>

ALU FUNCTIONS: KS10 CODE = AMD 2901 FUNCTIONS

CODE	FUNCTION	SIMILAR CODES
00 A + Q	ADD	01 05 06
02 0 + Q = Q	PASS	03 04 07
10 Q - A = Q - A - .25	SUB (1S CPL)	11 15 16 20 21 25 26
12 Q - 0 = Q - .25	DECR	13 14 27
22 0 - Q = - Q - .25	1S CPL	17 23 24
30 Q ∨ A	OR	31 35 36
32 0 ∨ Q = Q	PASS	33 34 37
40 A ∧ Q	AND	41 45 46
42 0 ∧ Q = 0	ZERO	43 44 47
50 $\overline{A}$ ∧ Q	MASK	51 55 56
52 $\overline{0}$ ∧ Q = 1 B = B	PASS	53 54
57 $\overline{D}$ ∧ 0 = 0	ZERO	
60 A ∨ Q	EX-OR	61 65 66
62 0 ∨ Q = Q	PASS	63 64 67
70 Q ∨ $\overline{A}$ = Q = A	EX-NOR	71 75 76
72 Q ∨ 0 = Q	INVERT	73 74 77

0	R	+ S
1	S	- R
2	R	- S
3	R	OR S
4	R	AND S
5	R	AND S
6	R	XOR S
7	R	XNOR S

R	S
0	A Q
1	A B
2	0 Q
3	0 B
4	0 A
5	D A
6	D Q
7	D 0

DEST: DP Q B

SRC

0	A		AD
1	AD		AD
2	AD	AD	
3	AD		
4	AD	Q*2	AD*2
5	AD		AD*2
6	AD	Q*5	AD*.5
7	AD		AD*.5

A/B	REGISTER
00	MAG ONES IN 1–36 OTHERS 0
01	PC CURR INSTR ADDRESS +1
02	HR CURRENT INSTRUCTION
03	AR MEM OP AT INSTR START*
04	ARX LOW ORDER 1/2 OF DBL PREC *
05	BR *
06	BRX LOW ORDER 1/2 OF DBL PREC BR/BRX *
07	ONE THE CONSTANT 1
10	EBR EXEC BASE REGISTER
11	UBR USER BASE REGISTER
12	MASK ONES IN 0–35 OTHERS 0
13	FLG FLAG BITS,, PAGE FAIL CODE
14	PI PI SYSTEM STATUS REGISTER (RDPI)
15	XWD1 1 IN EACH 162
16	T0 *
17	T1 *

* TEMPORARY

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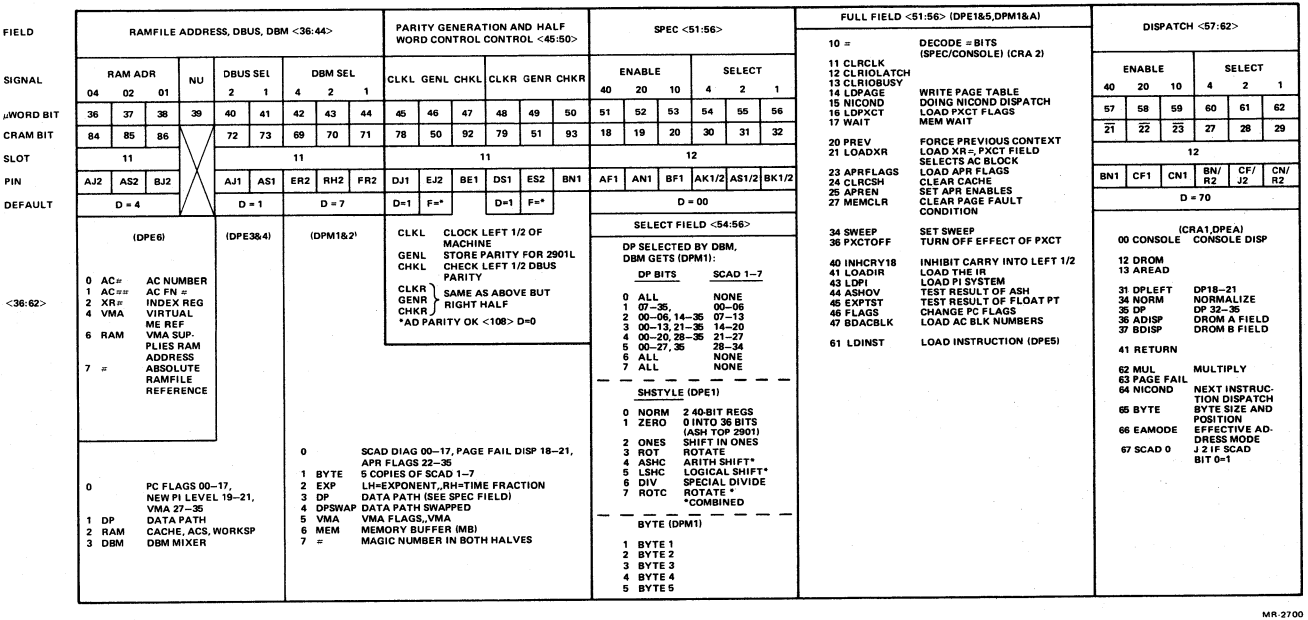
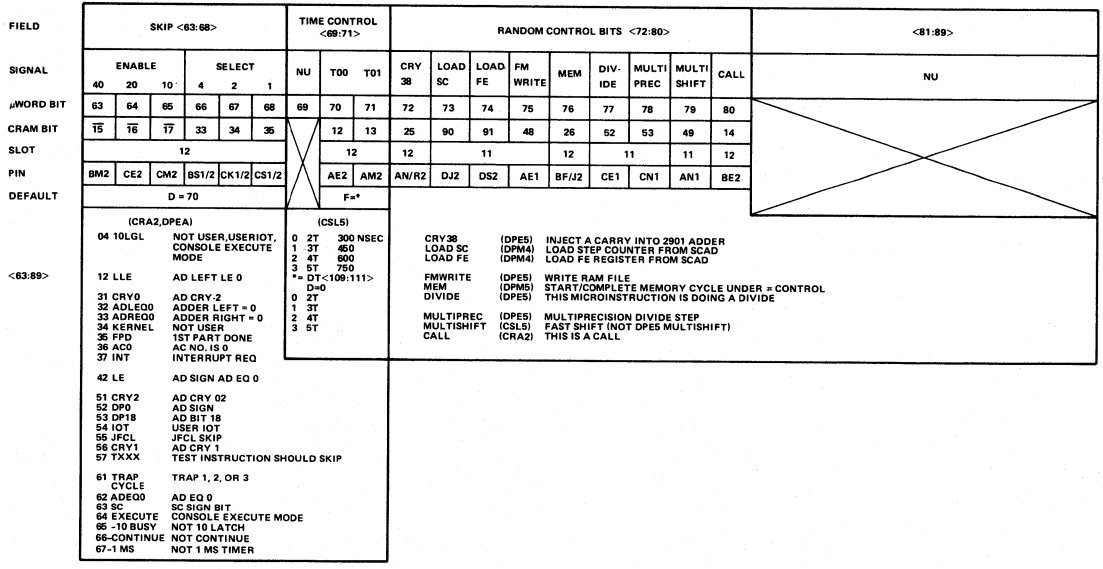
Microword Format (Bits 0-35)



MR-2700

Microword Format (Bits 36-62)



Microword Format (Bits 63-89)

FIELD	= MAGIC NUMBER <90:107>																
SIGNAL	=00	=01	=02	=03	=04	=05	=06	=07	=08	=09	=10	=11	=12	=13	=14	=15	=16	=17
μWORD BIT	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107
CRAM BIT	54	55	56	57	58	59	36	37	38	39	40	41	42	43	44	45	46	47
SLOT	11																	
PIN	DE1	DN1	EE1	EN1	FE1	FN1	AD1/2	AM1/2	BD1/2	BM1/2	CD1/2	CM1/2	DD1/2	DM1/2	ED1/2	EM1/2	FD1/2	FM1/2

STATE REGISTER CONTROL (NOT USED BY HARDWARE)

STATE <90:107> (PAGE FAIL CODE)

	0 SIMPLE	SIMPLE INSTRUCTIONS
	1 BLT	BLT IN PROGRESS
40000	2 MAP	MAP IN PROGRESS
	3 SRC	MOVE STRING SRC IN PROGRESS
	4 DST	MOVE STRING FILL IN PROGRESS
	5 SRC+DST	MOVE STRING DESTINATION IN PROGRESS
	6 DSTF	FILLING DESTINATION
	7 CVTDB	CONVERT DEC TO BIN
	10 COMP-DST	COMPARE DESTINATION
	11 EDIT-SRC	EDIT SOURCE
	12 EDIT-DST	EDIT DESTINATION
	13 EDIT-S+D	BOTH SRC AND DEST POINTERS

AC CONTROL (DPE6)

AC ALU <98:103>

25	B	C_{IN}	S8	S4	S2	S1	MOD	B8	B4	B2	B1
62	AC+N										

(74LS181 ON DPE6)

ACN <104:107> AC NAMES FOR STRING INSTRUCTIONS

0	SRCLEN	SOURCE LENGTH
1	SRCP	SOURCE POINTER
3	DLEN	DEST LENGTH
4	DSTP	DEST POINTER
3	MARK	POINTER TO MARK
3	BIN0	HIGH WORD OF BINARY
4	BIN 1	LOW WORD OF BINARY

<90:107>

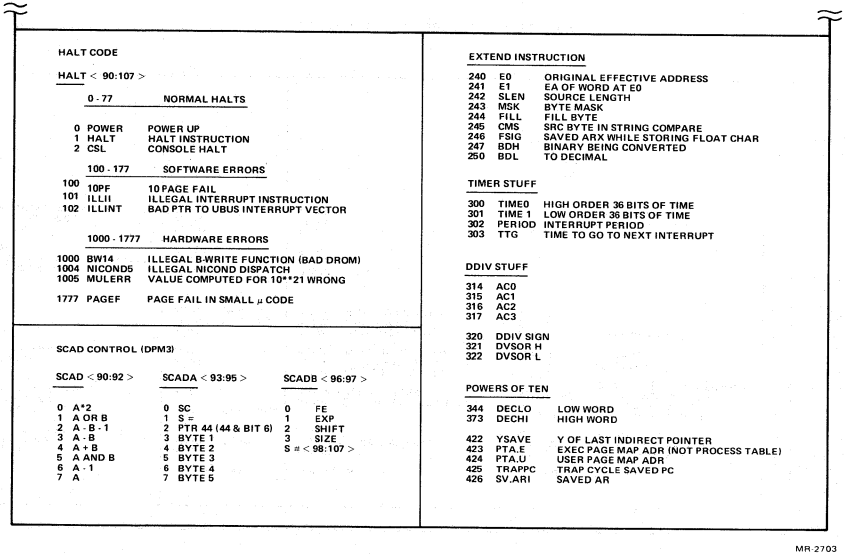
WORKSPACE ADDRESS IN RAMFILE

WORK <98:107>

160	BADW0	AC BLK7 WORD0 (BAD DATA FROM MEM)
161	BADW1	AC BLK7 WORD1 (BAD DATA FROM MEM)
200	MUL	TEMP FOR MULTIPLY
201	DIV	TEMP FOR DIVIDE
210	SVVMA	SAVE VMA
211	SVAR	SAVE AR
212	SVARX	SAVE ARX
213	SVBR	SAVE BR
214	SVBRX	SAVE BRX
215	SBR	SPT BASE REGISTER
216	CBR	CST BASE ADDRESS
217	CSTM	CST MASK
220	PUR	PROCESS USE REGISTER
221	ADJP	"P" FOR ADJBP
222	ADJS	"S" FOR ADJBP
223	ADJPTR	BYTE POINTER FOR ADJBP
224	ADJQ1	TEMP FOR ADJBP
225	ADJR2	TEMP FOR ADJBP
226	ADJBPW	BYTES/WORD FOR ADJBP
227	HSBADR	HALT STATUS BLOCK ADDRESS
230	APR	APR ENABLES

MR-2702

Microword Format (Bits 90-107)



MR-2703

Microword Format (Bits 90-107)

BIT	FUNCTIONS
BIT	MEMORY CYCLE CONTROL (MEM BIT 76)
90	FORCE USER — FORCE USER MODE REF
91	FORCE EXEC — FORCE EXEC MODE REF (PXCT)
92	FETCH — THIS IS AN INSTRUCTION FETCH
93	READ CYCLE — START A READ CYCLE
94	WRITE TEST — PAGE FAIL IF NOT WRITTEN
95	WRITE CYCLE — START A MEM WRITE CYCLE (DPM 5)
96	SPARE
97	DONT CACHE — DO NOT LOOK IN CACHE
98	PHYSICAL — DO NOT INVOKE PAGING HARDWARE (DPM 4)
99	PXCT < 99:101 > WHICH PXCT BITS TO LOOK AT:
100	0 CURRENT — 4 BIS-SRC-EA
101	1 E1 — 5 E2
	6 BIS-DST-EA
	3 D1 — 7 D2
102	AREAD — START A READ IF DROM ASKS
103	DPFUNC — IGNORE # 0:11, USE DP 0:13, DP9 = FORCE PREV
104	LDVMA — LOAD THE VMA (DPE 5)
105	EXT ADR — PUT VMA 14:17 ON BUS
106	WAIT — START A MEMORY CYCLE (DPM 5)
107	BWRITE — START A MEMORY CYCLE IF DROM ASKS

PI RIGHT BITS	
PI.ZER	
< 90:92 > ZERO	
PI.IP1	PI1 IN PROG
PI.IP2	
PI.IP3	
PI.IP4	
PI.IP5	
PI.IP6	
PI.IP7	
PI.ON	SYSTEM ON
PI.CO1	CHAN 1 ON
PI.CO2	
PI.CO3	
PI.CO4	
PI.CO5	
PI.CO6	
PI.CO7	

WRPI DATA	
PI.MBZ	
< 90:93 >	MUST BE ZERO
PI.DIR	DROP INTERRUPT REQUESTS
PI.CLR	CLEAR SYSTEM
PI.REQ	REQUEST INTERRUPT
PI.TCN	TURN CHANNEL ON
PI.TCF	TURN CHANNEL OFF
PI.TSF	TURN SYSTEM OFF
PI.TSN	TURN SYSTEM ON
PI.SC1	SELECT CHANNEL 1
PI.SC2	
PI.SC3	
PI.SC4	
PI.SC5	
PI.SC6	
PI.SC7	

PC FLAG CONTROL (DPE9)	
SETOV	SET ARITH OVERFLOW
SETFOV	SET FLOAT OVERFLOW
SETNDV	SET NO DIVIDE
CLRFPD	CLEAR 1ST PART DONE
SETFPD	SET 1ST PART DONE
HOLD USER	IF = 1 PREVENTS: SET USER IOT & CLR USER IN USER MODE
SPARE	
TRAP 2	SET TRAP 2
TRAP 1	SET TRAP 1
LD PCU	LOAD PCU FROM USER
SPARE	
SPARE	
SPARE	
SPARE	
JFCLFLG	DO A JFCL INSTRUCTION
LD FLAGS	LOAD FLAGS FROM DP
AD FLAGS	UPDATE CARRY FLAGS

BIT	FUNCTIONS
	ONLY TO SETUP DP DURING DP FUNCTION
99	PREVIOUS
100	10 CYCLE — THIS IS AN 10 CYCLE
101	WRU CYCLE — WHO ARE YOU CYCLE
102	VECTOR CYCLE — READ INTERRUPT VECTOR
103	10 BYTE — BYTE CYCLE
104	
	FLG BITS
94	FLG.W — W BIT FROM PAGE MAP
95	FLG.P1 — PI CYCLE
96	FLG.C — CACHE BIT FROM PAGE MAP
97	FLG.SN — SPECIAL NEGATE IN FDV & DFDV
	RIGHT 1/2 OF FLG USED TO RECOVER FROM PAGE FAILS
	APR ID DATA < 90:107 >
	MICROCODE OPTIONS < 90:98 > OPT 0
	MICROCODE VERSION < 99:107 > UCV 101

MR-2704

Microword Format (Bits 90-107)

ECC (MOS MEMORY ERROR CORRECTION) BITS
C-Field is "hidden" as (Memory status register):

MOS DATA BIT	Meaning
36	Check Bit CP
37	Check Bit C40
38	Check Bit C20
39	Check Bit C10
40	Check Bit C4
41	Check Bit C2
42	Check Bit C1

C-Field	Meaning	C-Field	Meaning
0	Unknown ECC-CODE 0	40	ECC Bit C40 failed
1	ECC-Bit C1 failed	41	Bit 18 failed
2	ECC-Bit C2 failed	42	Bit 19 failed
3	Unknown ECC-CODE 3	43	Bit 20 failed
4	ECC-BIT C4 failed	44	Bit 21 failed
5	Unknown ECC-CODE 5	45	Bit 22 failed
6	Unknown ECC-CODE 6	46	Bit 23 failed
7	Unknown ECC-CODE 7	47	Unknown ECC-CODE 47
10	ECC-Bit C10 failed	50	Unknown ECC-CODE 50
11	Bit 0 failed	51	Bit 24 failed
12	Bit 1 failed	52	Bit 25 failed
13	Bit 2 failed	53	Bit 26 failed
14	Bit 3 failed	54	Bit 27 failed
15	Bit 4 failed	55	Bit 28 failed
16	Bit 5 failed	56	Bit 29 failed
17	Unknown ECC-CODE 17	57	Unknown ECC-CODE 57
20	ECC-Bit C20 failed	60	Unknown ECC-CODE 60
21	Bit 6 failed	61	Bit 30 failed
22	Bit 7 failed	62	Bit 31 failed
23	Bit 8 failed	63	Bit 32 failed
24	Bit 9 failed	64	Bit 33 failed
25	Bit 10 failed	65	Bit 34 failed
26	Bit 11 failed	66	Bit 35 failed
27	Unknown ECC-CODE 27	67	Unknown ECC-CODE 67
30	Unknown ECC-CODE 30	70	Unknown ECC-CODE 70
31	Bit 12 failed	71	Unknown ECC-CODE 71
32	Bit 13 failed	72	Unknown ECC-CODE 72
33	Bit 14 failed	73	Unknown ECC-CODE 73
34	Bit 15 failed	74	Unknown ECC-CODE 74
35	Bit 16 failed	75	Unknown ECC-CODE 75
36	Bit 17 failed	76	Unknown ECC-CODE 76
37	Unknown ECC-CODE 37	77	Unknown ECC-CODE 77

MEMORY ADDRESS MAP

Double spaced at 16K
Triple spaced at 64K

FROM	START	STOP	TO
0K	00	07777	4K
4K	10000	17777	8K
8K	20000	27777	12K
12K	30000	37777	16K
16K	40000	47777	20K
20K	50000	57777	24K
24K	60000	67777	28K
28K	70000	77777	32K
32K	100000	107777	36K
36K	110000	117777	40K
40K	120000	127777	44K
44K	130000	137777	48K
48K	140000	147777	52K
52K	150000	157777	56K
56K	160000	167777	60K
60K	170000	177777	64K
64K	200000	207777	68K
68K	210000	217777	72K
72K	220000	227777	76K
76K	230000	237777	80K
80K	240000	247777	84K
84K	250000	257777	88K
88K	260000	267777	92K
92K	270000	277777	96K
96K	300000	307777	100K
100K	310000	317777	104K
104K	320000	327777	108K
108K	330000	337777	112K
112K	340000	347777	116K
116K	350000	357777	120K
120K	360000	367777	124K
124K	370000	377777	128K
128K	400000	407777	132K
132K	410000	417777	136K
136K	420000	427777	140K
140K	430000	437777	144K
144K	440000	447777	148K
148K	450000	457777	152K
152K	460000	467777	156K
156K	470000	477777	160K
160K	500000	507777	164K
164K	510000	517777	168K
168K	520000	527777	172K
172K	530000	537777	176K
176K	540000	547777	180K
180K	550000	557777	184K
184K	560000	567777	188K
188K	570000	577777	192K

FROM	START	STOP	TO
192K	600000	607777	196K
196K	610000	617777	200K
200K	620000	627777	204K
204K	630000	637777	208K
208K	640000	647777	212K
212K	650000	657777	216K
216K	660000	667777	220K
220K	670000	677777	224K
224K	700000	707777	228K
228K	710000	717777	232K
232K	720000	727777	236K
236K	730000	737777	240K
240K	740000	747777	244K
244K	750000	757777	248K
248K	760000	767777	252K
252K	770000	777777	256K

ASCII CODE

INPUT-OUTPUT CODES

Even Parity Bit	7-Bit Decimal	7-Bit Octal	Character	Remarks
0	000	000	NUL	Null, tape feed. Control shift P.
1	001	001	SOH	Start of heading [SOM, start of message]. Control A.
1	002	002	STX	Start of text [EOA, end of address]. Control B.
0	003	003	ETX	End of text [EOM, end of message]. Control C.
1	004	004	EOT	End of transmission; shuts off TWX machines and disconnects some data sets. Control D.
0	005	005	ENQ	Enquiry [WRU, "Who are you?"]. Triggers identification ("Here is...") at remote station if so equipped. Control E.
0	006	006	ACK	Acknowledge [RU, "Are you...?"]. Control F.
1	007	007	BEL	Rings the bell. Control G.
1	008	010	BS	Backspace. Control H.
0	009	011	HT	Horizontal tab. Control I.
0	010	012	LF	Line feed. Control J.
1	011	013	VT	Vertical tab. Control K.
0	012	014	FF	Form feed to top of next page. Control L.
1	013	015	CR	Carriage return to beginning of line. Control M.
1	014	016	SO	Shift out; change character set or change ribbon color to red. Control N.
0	015	017	SI	Shift in; return to standard character set or color. Control O.
1	016	020	DLE	Data link escape [DCO]. Control P.
0	017	021	DC1	Device control 1, turns transmitter (reader) on. Control Q (X ON).
0	018	022	DC2	Device control 2, turns punch or auxiliary on. Control R (TAPE, AUX ON).
1	019	023	DC3	Device control 3, turns transmitter (reader) off. Control S (X OFF).
0	020	024	DC4	Device control 4 (stop), turns punch or auxiliary off. Control T (AUX OFF).

ASCII CODE (CONT)

INPUT-OUTPUT CODES

Even Parity Bit	7-Bit Decimal	7-Bit Octal	Character	Remarks
1	021	025	NAK	Negative acknowledge [ERR, error]. Control U.
1	022	026	SYN	Synchronous idle [SYNC]. Control V.
0	023	027	ETB	End of transmission block [LEM, logical end of medium]. Control W.
0	024	030	CAN	Cancel [S_0]. Control X.
1	025	031	EM	End of medium [S_1]. Control Y.
1	026	032	SUB	Substitute [S_2]. Control Z.
0	027	033	ESC	Escape, prefix [S_3]. Control shift K.
1	028	034	FS	File separator [S_4]. Control shift L.
0	029	035	GS	Group separator [S_5]. Control shift M.
0	030	036	RS	Record separator [S_6]. Control shift N.
1	031	037	US	Unit separator [S_7]. Control shift O.
FIGURES				
1	032	040	SP	Space.
0	033	041	!	
0	034	042	"	
1	035	043	#	£ on some (non-DIGITAL) units.
0	036	044	$	
1	037	045	%	
1	038	046	&	
0	039	047	'	Accent acute or apostrophe - ' before 1965, but used until recently on DIGITAL units.
0	040	050	(	
1	041	051	)	
1	042	052	*	
0	043	053	+	
1	044	054	,	
0	045	055	-	
0	046	056	.	
1	047	057	/	
0	048	060	Ø	
1	049	061	1	

ASCII CODE (CONT)

Even Parity Bit	7-Bit Decimal	7-Bit Octal	Character	Remarks
1	050	062	2	
0	051	063	3	
1	052	064	4	
0	053	065	5	
0	054	066	6	
1	055	067	7	
1	056	070	8	
0	057	071	9	
0	058	072	:	
1	059	073	;	
0	060	074	<	
1	061	075	=	
1	062	076	>	
0	063	077	?	
UPPER CASE				
1	064	100	@	1965-67, but never on DIGITAL units.
0	065	101	A	
0	066	102	B	
1	067	103	C	
0	068	104	D	
1	069	105	E	
1	070	106	F	
0	071	107	G	
0	072	110	H	
1	073	111	I	
1	074	112	J	
0	075	113	K	
1	076	114	L	
0	077	115	M	
0	078	116	N	
1	079	117	O	
0	080	120	P	
1	081	121	Q	
1	082	122	R	
0	083	123	S	
1	084	124	T	
0	085	125	U	

ASCII CODE (CONT)

Even Parity Bit	7-Bit Decimal	7-Bit Octal	Character	Remarks
0	086	126	V	
1	087	127	W	
1	088	130	X	
0	089	131	Y	
0	090	132	Z	
1	091	133	[	Shift K.
0	092	134	\	~ 1965-67, but never on DIGITAL units. Shift L.
1	093	135	]	Shift M.
1	094	136	^	Circumflex - ↑ before 1965, but used until recently on DIGITAL units.
0	095	137	_	Underscore - ← before 1965, but used until recently on DIGITAL units.
LOWER CASE				Codes 140-173 first defined in 1965. For a full ASCII character set, the monitor accepts codes 140-176 as lower case. For a character set that lacks lower case, the monitor translates input codes 140-174 into the corresponding upper case codes (100-134) and translates both 175 and 176 into 033, escape. Early versions of the monitor used 175 as the escape code and translated both 176 and 033 to it.
0	096	140		Accent grave - @ 1965-67, but never on DIGITAL units.
1	097	141	a	
1	098	142	b	
0	099	143	c	
1	100	144	d	
0	101	145	e	
0	102	146	f	
1	103	147	g	
1	104	150	h	
0	105	151	i	
0	106	152	j	
1	107	153	k	
0	108	154	l	
1	109	155	m	
1	110	156	n	

ASCII CODE (CONT)

Even Parity Bit	7-Bit Decimal	7-Bit Octal	Character	Remarks
0	111	157	o	
1	112	160	p	
0	113	161	q	
0	114	162	r	
1	115	163	s	
0	116	164	t	
1	117	165	u	
1	118	166	v	
0	119	167	w	
0	120	170	x	
1	121	171	y	
1	122	172	z	
0	123	173	{	
1	124	174	|	Control character ACK before 1965; 1965-67, but never on DIGITAL units. Vertical bar may or may not have gap, depending on font design, but generally does not on DIGITAL units.
0	125	175	}	Unassigned control character (usually ALT MODE) before 1965. Code generated by ALT MODE key on most DIGITAL units.
0	126	176	~	Control character ESC before 1965; |1965-67, but never on DIGITAL units. Code generated by ESC key on some DIGITAL units.
1	127	177	DEL	Delete, rub out (not part of lower case set).

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NOTES

CONSOLE BOARD UARTS SWITCH CONFIGURATIONS

CTY - Bottom Berg Connector - Switch pack ~~E508~~ E9 for baud rate selection.

KLINIK - Top Berg Connector - Switch pack E509 for baud rate selection.

Baud Rate	Switches 1	2	3	4	5*	6
110	0	0	0	0	0	0
300	0	0	1	0	1	0
600	1	0	0	0	1	0
1200	0	1	0	0	1	0
1800	0	1	0	1	1	0
2400	0	0	1	1	1	0
4800	0	1	1	0	1	0
9600	0	1	1	1	1	0

*NOTE: Switch 5 = stop bit selection
0 = 2 stop bits
1 = 1 stop bits.

RH11-C JUMPERS

RH11-C MASSBUS CONTROLLER

Lowest acceptable wire list Revision C

M7294-YA DATA BUFFER AND CONTROL LOCATION ABCDEF03

Lowest acceptable revision etch Rev N/A CS Rev*

Jumper	State Disk	State Tape	Comments
W1	OUT	OUT	Sense Unibus A Parity Error
W2	IN	IN	Sense Unibus B Parity Error
E66, Pins 1-16	IN	IN	Start Count YR Words
E66, Pins 5-12	OUT	OUT	Start Count 32 Words
E66, Pins 7-10	OUT	OUT	Start Count 16 Words
E66, Pins 2-15	IN	IN	Disable Bus B HOG Mode
E66, Pins 3-14	OUT	OUT	Enable Back-to-Back MEM Cycles
E66, Pins 4-13	OUT	IN	For Tape Subsystem Only, Otherwise Out
E66, Pins 6-11	IN	OUT	For Disk Subsystem Only, Otherwise Out

M7295 BUS CONTROL LOCATION ABCDEF02

Lowest acceptable revision etch Rev N/A CS Rev D

Jumper	State Disk	State Tape	Comments
W1	OUT	OUT	Address Bit 12
W2	OUT	IN	Address Bit 11
W3	OUT	OUT	Address Bit 10
W4	IN	IN	Address Bit 09
W5	OUT	OUT	Address Bit 08
W6	OUT	IN	Address Bit 07
W7	OUT	IN	Address Bit 06
W8	IN	OUT	Address Bit 05
E3, Pins 1-16	OUT	IN	16-32 Registers
E3, Pins 2-15	OUT	IN	16-32 Registers
E3, Pins 3-14	IN	OUT	1-16 Registers
E3, Pins 4-13	IN	OUT	1-16 Registers
E3, Pins 5-12	IN	OUT	16 Registers
E3, Pins 6-11	OUT	OUT	8 Registers
E3, Pins 7-10	IN	OUT	4 Registers
E3, Pins 8-9	OUT	IN	2 Registers
W11	IN	IN	Vector Bit V2
W12	IN	OUT	Vector Bit V3
W13	OUT	IN	Vector Bit V4
W14	IN	OUT	Vector Bit V5
W15	OUT	OUT	Vector Bit V6
W16	IN	IN	Vector Bit V7
W17	OUT	OUT	Vector Bit V8
W18	OUT	OUT	NPR Latency
W19	IN	IN	Maintenance (MXF Errors)

W1-18: Correspond to a base address of 776700 for disks and 772440 for tapes.
W11-W17: Correspond to a vector address of 000254 for disks and 000224 for tapes.
Jumpers on E3 are set for 20 registers for disks and 14 for tapes.
DIPS site E57 should contain priority plug BR6 (54-08780).

CAUTION
Board may not be received with proper BR plug if it is a spare.

M7296 CONTROL AND STATUS REGISTERS LOCATION EF01

Lowest acceptable revision etch Rev N/A CS Rev B.

Install jumper W1 to allow only Unibus A to be selected.

M7297 PARITY CONTROL LOCATION CD01

Lowest acceptable revision etch Rev N/A CS Rev A.

No jumpers or other configurable components.

There are two visual indicators (LEDs) for MASSBUS parity error display on this board (lit if parity error detected).

M9300 UNIBUS B TERMINATOR LOCATION AB08

Lowest acceptable revision etch Rev N/A CS Rev 0.

Jumper	State	Comments
W1	IN	Beginning of bus
W2	OUT	Not end of bus
W3	OUT	Not end of bus

There is a visual indicator (LED) for an illegal jumper configuration check (lit if illegal).

M5904 CONTROLLER TRANSCEIVER LOCATIONS CD04, CD05, CD06

Lowest acceptable revision etch Rev N/A CS Rev D.

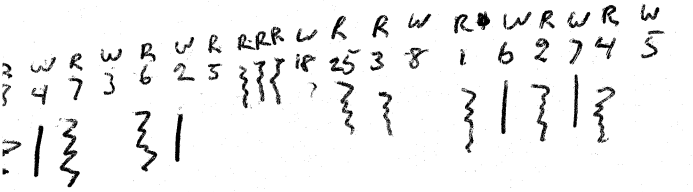
No jumpers or other configurable component.

M688 UNIBUS POWER FAIL DRIVERS LOCATIONS E04 AND E05

Lowest acceptable revision etch Rev N/A CS Rev N/A.

No jumpers or other configurable component.

Remove M688 module from BA11-K box slot #E15 only. M688 in slot #E14 to remain.



LP20-Switches

M8586 Control Location ABCDEF02

Jumper	State	Function	
W1	IN(#1),OUT(#2)	ADR BIT 4	
W2	IN	ADR BIT 5	
W3	IN	ADR BIT 6	
W4	IN	ADR BIT 7	If Rev E M8586 with switch
W5	OUT	ADR BIT 8	packs instead of jumpers 775400 address = 5,6,8,9,10
OFF			754 Vector = 3 OFF
W6	OUT	ADR BIT 9	
W7	IN	ADR BIT 10	
W8	OUT	ADR BIT 11	
W9	OUT	ADR BIT 12	
W10	IN(#1),OUT(#2)	VEC BIT 2	
W11	IN	VEC BIT 3	
W12	OUT	VEC BIT 4	
W13	IN	VEC BIT 5	
W14	IN	VEC BIT 6	
W15	IN	VEC BIT 7	
W16	IN	VEC BIT 8	

W1-W9 Correspond to base ADR 775400 (UNIT #1) and 775420 (UNIT #2)
W10-W16 Correspond to Vector 754 (#1) and 750 (#2)
Dip site E6 contains priority plug BR4 54-08776

M8587 Data Paths

W1	OUT	Install to enable parity
W2	IN	Install for DAVFU

NOTE

Cable BC06R is connected from Berg connector J1 on the M8587 module, ribbed side toward the module (red line away from handle), to the center slot of the receptacle housing mounted in the connector tray (red line towards the connector fastener).

DUP 11 Switches

There are two switch packs on each M7867 (DUP11-DA) module. Their switch settings are as follows in order to properly configure the above address and vector assignments.

	DUP11 #1			DUP11 #2	
Pack	Switch	State	Pack	Switch	State
E59	1	ON	E59	1	ON
E59	2	OFF	E59	2	ON
E59	3	ON	E59	3	OFF
E59	4	ON	E59	4	OFF
E59	5	ON	E59	5	OFF
E59	6	ON	E59	6	OFF
E59	7	N/A	E59	7	N/A
E59	8	N/A	E59	8	N/A
E113	1	ON	E113	1	OFF
E113	2	ON	E113	2	ON
E113	3	ON	E113	3	ON
E113	4	OFF	E113	4	OFF
E113	5	OFF	E113	5	OFF
E113	6	ON	E113	6	ON
E113	7	ON	E113	7	ON
E113	8	ON	E113	8	ON
E113	9	ON	E113	9	ON
E113	10	ON	E113	10	ON

There are seven jumpers on each M7867 (DUP11-DA) module. They are all factory settable for compatibility with Bell 201, Bell 208 and 209 series modems and should not have to be changed unless another type modem is used.

Should another type modem be used, the jumpers must be reconfigured so that they are compatible with the type modem used. Refer to the DUP11-DA bit synchronous interface maintenance manual (EK-DUP11-MM).

As a quick verify, the standard factory settable jumper settings are as follows.

W1	IN	W5	OUT
W2	OUT	W6	IN
W3	IN	W7	IN
W4	IN		

BR priority level 5 (priority jumper P/N 5408778).

RM03 JUMPER

This jumper should be installed during system installation.

MBA BACKPLANE
E06E1 TO E09C2

NOTE
If the jumper is not installed, the diagnostics will fail and the drive will not format a pack. This jumper grounds signal BP 144 ENB H on page D56 of the MBA print set.

DZ11 Switches

DZ11 #1

Pack	Switch	State
E11	1	N/A
E11	2	ON
E11	3	ON
E11	4	OFF
E11	5	OFF
E11	6	OFF
E11	7	ON
E11	8	N/A
E81	1	ON
E81	2	OFF
E81	3	OFF
E81	4	OFF
E81	5	OFF
E81	6	OFF
E81	7	OFF
E81	8	OFF
E81	9	OFF
E81	10	OFF

DZ11 #2

Pack	Switch	State
E11	1	N/A
E11	2	OFF
E11	3	ON
E11	4	OFF
E11	5	OFF
E11	6	OFF
E11	7	ON
E11	8	N/A
E81	1	OFF
E81	2	ON
E81	3	OFF
E81	4	OFF
E81	5	OFF
E81	6	OFF
E81	7	OFF
E81	8	OFF
E81	9	OFF
E81	10	OFF

DZ11 #3

Pack	Switch	State
E11	1	N/A
E11	2	ON
E11	3	OFF
E11	4	OFF
E11	5	OFF
E11	6	OFF
E11	7	ON
E11	8	N/A
E81	1	ON
E81	2	ON
E81	3	OFF
E81	4	OFF
E81	5	OFF
E81	6	OFF
E81	7	OFF
E81	8	OFF
E81	9	OFF
E81	10	OFF

DZ11 #4

Pack	Switch	State
E11	1	N/A
E11	2	OFF
E11	3	OFF
E11	4	OFF
E11	5	OFF
E11	6	OFF
E11	7	ON
E11	8	N/A
E81	1	OFF
E81	2	OFF
E81	3	ON
E81	4	OFF
E81	5	OFF
E81	6	OFF
E81	7	OFF
E81	8	OFF
E81	9	OFF
E81	10	OFF

BR Priority Level 5 (Priority Jumper P/N 5408778)

There are two switch packs on each M8204 module. Their switch settings are as follows.

NOTE

Each backplane slot which has an M8204 (KMC11) module installed must have the backplane wire from pin CA1 to pin CB1 of that slot removed. Should the KMC11 be removed from that slot, the wire must be re-inserted in order to guarantee that the NPG signal will be passed along the Unibus.

DD11-DK (lowest acceptable Rev B). All slots which have no quad or hex module installed must have a grant continuity card (G727) installed in row D of that slot.

KMC11 #1

Pack	Switch	State
E65	1	OFF
E65	2	OFF
E65	3	ON
E65	4	ON
E65	5	OFF
E65	6	ON
E65	7	N/A
E65	8	N/A
E116	1	ON
E116	2	ON
E116	3	OFF
E116	4	OFF
E116	5	ON
E116	6	OFF
E116	7	ON
E116	8	ON
E116	9	ON
E116	10	ON

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NOTES

NOTES

READ (0)

07	06	05	04	03	02	01	00
READ DATA							
28	29	30	31	32	33	34	35

MR-2662

READ (1)

07	06	05	04	03	02	01	00
READ DATA							
20	21	22	23	24	25	26	27

MR-2663

READ (2)

07	06	05	04	03	02	01	00
READ DATA							
12	13	14	15	16	17	18	19

MR-2664

READ (3)

07	06	05	04	03	02	01	00
READ DATA							
04	05	06	07	08	09	10	11

MR-2665

READ (100)

07	06	05	04	03	02	01	00
REC PE	UBA3 PE		CRAM PE	MEM PE	DP PE	CRA PE	UBA2 PE

07 IF 0, CONSOLE RECEIVE PARITY ERROR
06 IF 0, UNIBUS ADAPTER 3 PARITY ERROR
04 IF 0, CRAM PARITY ERROR
03 IF 0, MEMORY PARITY ERROR
02 IF 0, DATA PATH PARITY ERROR
01 IF 0, CRA PARITY ERROR
00 IF 0, UNIBUS ADAPTER 2 PARITY ERROR

MR-2666

READ (101)

07	06	05	04	03	02	01	00
PRIORITY INTERRUPT REQUEST							REFSH ERROR
01	02	03	04	05	06	07	

07 PRIORITY INTERRUPT REQUEST 1
06 PRIORITY INTERRUPT REQUEST 2
05 PRIORITY INTERRUPT REQUEST 3
04 PRIORITY INTERRUPT REQUEST 4
03 PRIORITY INTERRUPT REQUEST 5
02 PRIORITY INTERRUPT REQUEST 6
01 PRIORITY INTERRUPT REQUEST 7
00 MEMORY CONTROL REFRESH ERROR B

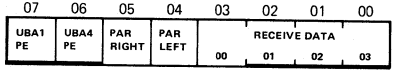
MR-2667

READ (102)

07	06	05	04	03	02	01	00
AC LO	RESET	MEM BUSY	I/O BUSY	BAD DATA	COM ADR	I/O DATA	DATA

05 MEMORY BUSY
02 COMMAND ADDRESS

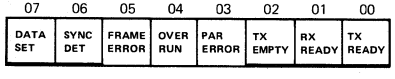
MR-2668



07 IF 0, UNIBUS ADAPTER 1 PARITY ERROR
06 IF 0, UNIBUS ADAPTER 4 PARITY ERROR
05 PARITY RIGHT
04 PARITY LEFT

MR-2669

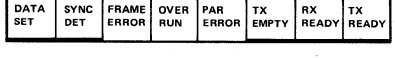
CTY UART READ STATUS REGISTER (DATA BUFFER IS I/O 201)



07 DATA SET READY
06 SYNC DETECT
05 FRAMING ERROR
04 OVERRUN ERROR
03 PARITY ERROR
02 TRANSMITTER EMPTY
01 RECEIVER READY
00 TRANSMITTER READY

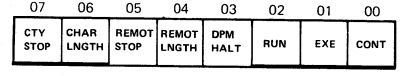
MR-2689

REMOTE UART READ STATUS REGISTER (DATA BUFFER IS I/O 203)



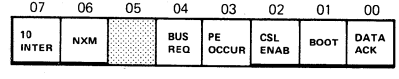
07 DATA SET READY
06 SYNC DETECT
05 FRAMING ERROR
04 OVERRUN ERROR
03 PARITY ERROR
02 TRANSMITTER EMPTY
01 RECEIVER READY
00 TRANSMITTER READY

MR-2691



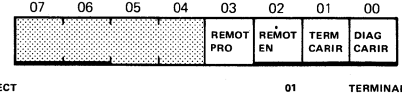
07 CTY STOP BIT
06 CTY CHARACTER LENGTH
05 REMOTE DIAGNOSIS STOP BIT
04 REMOTE DIAGNOSIS CHARACTER LENGTH
03 DPM HALT LOOP
01 EXECUTE
00 CONTINUE

MR-2670



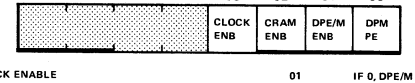
07 10 INTERRUPT
04 BUS REQUEST
03 PARITY ERROR OCCURRED
02 CONSOLE ENABLE
00 DATA ACKNOWLEDGE

MR-2671



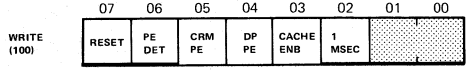
03 REMOTE PROTECT
02 REMOTE ENABLE
01 TERMINAL CARRIER
00 REMOTE DIAGNOSIS CARRIER

MR-2672



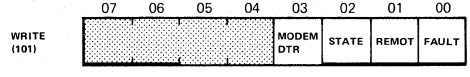
03 RECEIVE CLOCK ENABLE
02 CRAM CLOCK ENABLE
01 IF 0, DPE/M CLOCK ENABLE
00 IF 0, DPM PARITY ERROR

MR-2673



06 PARITY ERROR DETECT ENABLE
05 CRM PARITY ERROR DETECT
04 DATA PATH PARITY ERROR DETECT
03 CACHE ENABLE
02 1 MSECOND ENABLE

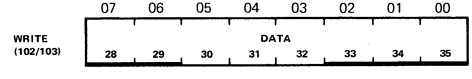
MR-2679



03 MODEM DATA TRANSFER
01 REMOTE

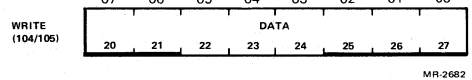
MR-2680

DATA/ADDRESS



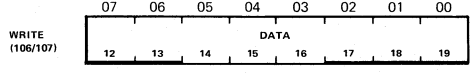
MR-2681

DATA/ADDRESS



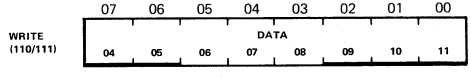
MR-2682

DATA/ADDRESS



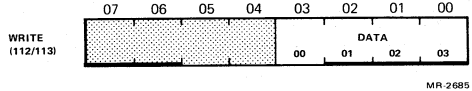
MR-2683

DATA/ADDRESS



MR-2684

DATA/ADDRESS

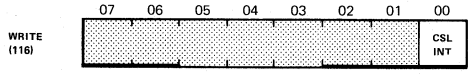


MR-2685

ADDRESS/DATA

03 BAD DATA CYCLE
02 COMMAND ADDRESS CYCLE
01 I/O DATA CYCLE
00 DATA CYCLE

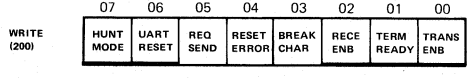
MR-2686



00 CONSOLE INTERRUPT THE 10

MR-2687

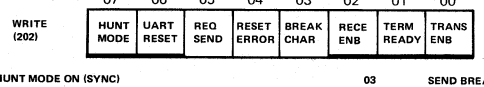
CTY UART WRITE STATUS REGISTER (DATA BUFFER IS I/O 201)



07 HUNT MODE ON (SYNC)
05 IF 0, REQUEST TO SEND
04 RESET ERRORS
03 SEND BREAK CHARACTER
02 RECEIVE ENABLE
01 IF 0, TERMINAL READY
00 TRANSMIT ENABLE

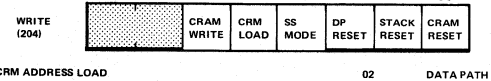
MR-2688

REMOTE UART WRITE STATUS REGISTER (DATA BUFFER IS I/O 203)



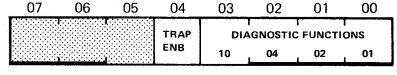
07 HUNT MODE ON (SYNC)
06 UART RESET
05 IF 0, REQUEST TO SEND
04 RESET ERRORS
03 SEND BREAK – CHARACTERS
02 RECEIVE ENABLE
01 IF 0, TERMINAL READY
00 TRANSMIT ENABLE

MR-2690



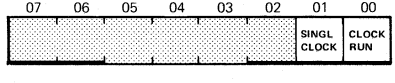
04 CRM ADDRESS LOAD
03 SINGLE STEP MODE
02 DATA PATH RESET

MR-2674



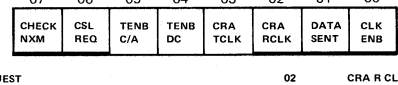
04 TRAP ENABLE

MR-2675



01 SINGLE CLOCK

MR-2676

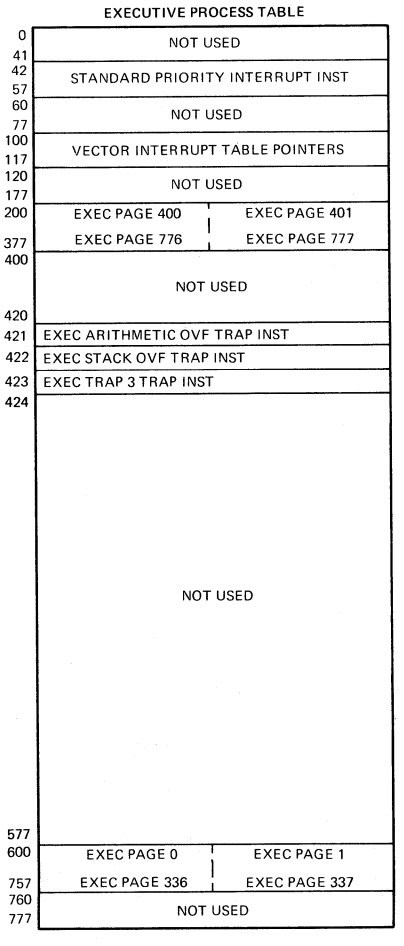


06 CONSOLE REQUEST
05 T ENABLE FOR COMMAND ADDRESS CYCLE
04 T ENABLE FOR DATA CYCLE
03 CRA T CLOCK
02 CRA R CLOCK
01 LATCH DATA SENT
00 IF 0, R CLOCK ENABLE

MR-2678

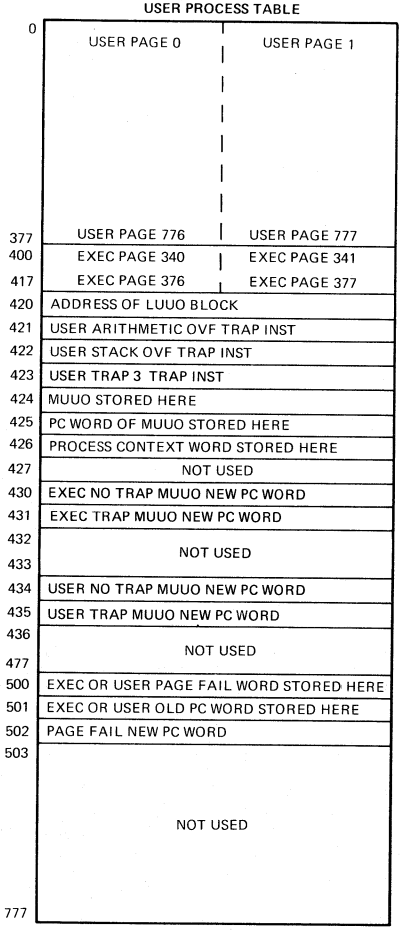
01 EXECUTE
00 CONTINUE

MR-2677

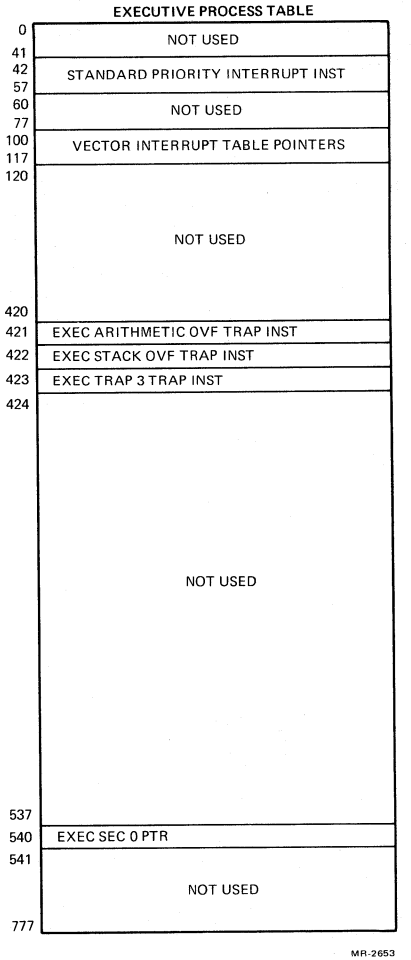


TOPS-10 PROCESS TABLE CONFIGURATION

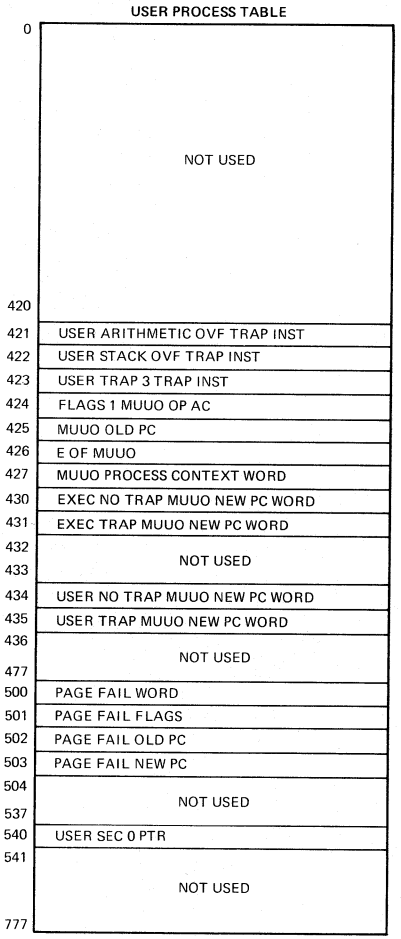
USER PROCESS TABLE



TOPS-10 PROCESS TABLE CONFIGURATION (CONT)

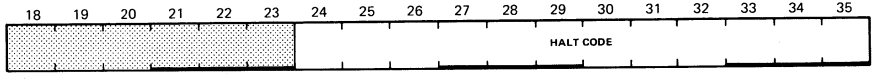


TOPS-20 PROCESS TABLE CONFIGURATION



TOPS-20 PROCESS TABLE CONFIGURATION (CONT)

HALT STATUS WORD (MEMORY LOCATION 0)



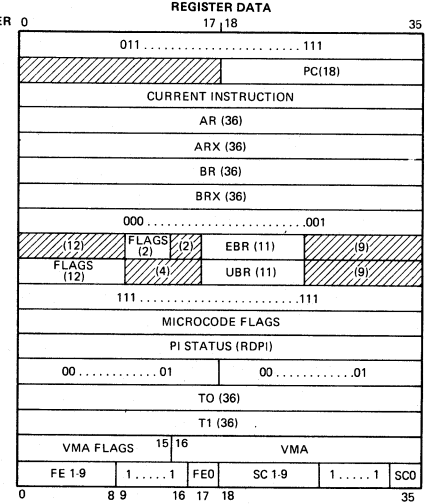
24–35 HALT CODE

0000	MICROCODE JUST STARTED
0001	HALT INSTRUCTION EXECUTED
0002	CONSOLE PROGRAM HALTED CPU
0100	I/O PAGE FAILURE
0101	ILLEGAL INTERRUPT INSTRUCTION
0102	POINTER TO UNIBUS VECTOR IS ZERO
1000	ILLEGAL MICROCODE DISPATCH
1005	MICROCODE STARTUP CHECK FAILED

MR 2829

HALT STATUS BLOCK

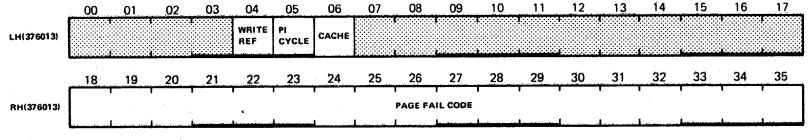
MEMORY LOCATION	TOPS-20 BOOT	TOPS-10 BOOT	REGISTER
376000	400	424	MAG
376001	401	425	PC
376002	402	426	HR
376003	403	427	AR
376004	404	430	ARX
376005	405	431	BR
376006	406	432	BRX
376007	407	433	ONE
376010	410	434	EBR
376011	411	435	UBR
376012	412	436	MASK
376013	413	437	FLG
376014	414	440	PI
376015	415	441	X1
376016	416	442	T0
376017	417	443	T1
376020	420	444	VMA
			FE/SC



NOTE: MEMORY LOCATION BASE ADDRESS MAY BE CHANGED WITH WHSB INSTRUCTION.

MR-2654

MICROCODE FLAGS



NOTE: ADDRESS MAY BE CHANGED WITH WHSB INSTRUCTION.

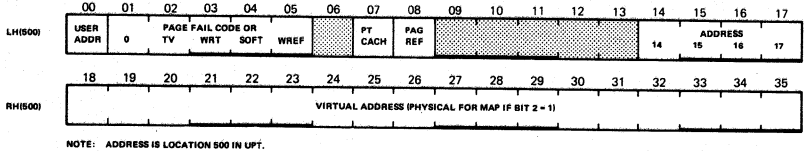
4	WRITE REFERENCE BIT FROM PAGE MAP
5	PI CYCLE
6	LOOK IN CACHE BIT FROM PAGE MAP

18–35 PAGE FAIL CODE

000000	SIMPLE INSTRUCTIONS
000001	BLT IN PROGRESS
400002	MAP IN PROGRESS
000003	MOVE STRING SOURCE IN PROGRESS
000004	MOVE STRING FILL IN PROGRESS
000005	MOVE STRING DESTINATION IN PROGRESS
000006	FILLING DESTINATION
000007	EDIT SOURCE
000010	EDIT DESTINATION
000011	CONVERTING DECIMAL TO BINARY
000012	COMPARING DESTINATION

MR-2825

PAGE FAIL WORD (OR MAP AC)



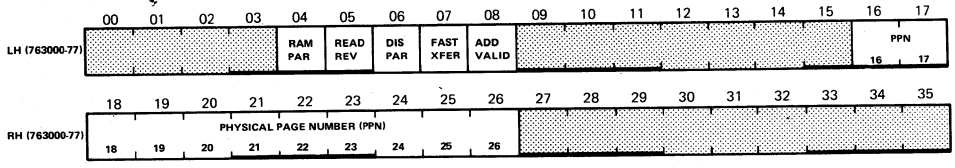
NOTE: ADDRESS IS LOCATION 500 IN UPT.

0	USER ADDRESS
2-5 (BIT 1 = 0)	
2	TRANSLATION VALID
3	WRITABLE (KL PAGING MODE = 0) WRITTEN (KL PAGING MODE = 1)
4	SOFTWARE (KL PAGING MODE = 0) WRITABLE (KL PAGING MODE = 1)
5	WRITE REFERENCE

2-5 (BIT 1 = 1)	PAGE FAIL CODE
20	AN I/O INSTRUCTION SELECTED A NONEXISTENT DEVICE OR REGISTER. (BITS 14-35 = I/O ADDRESS)
36	HARD MEMORY ERROR
37	NXM
7	PAGE TABLE CACHE
8	PAGE REFERENCE
18-35	VIRTUAL ADDRESS (PHYSICAL FOR MAP IF BIT 2 = 1)

MR-2828

UBA PAGING RAM (READ)

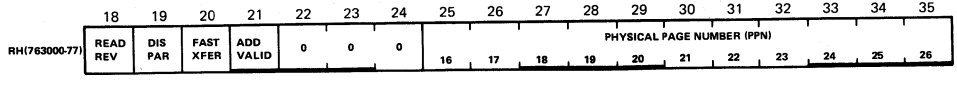


NOTE: ALL BITS READ ONLY.

BIT(S)	FUNCTION
04	PAGING RAM PARITY BIT
05	READ REVERSE
06	DISABLE PARITY BIT XFER TO UNIBUS
07	FAST TRANSFER MODE
08	ADDRESS IS VALID
–	MBZ (MUST BE ZERO)
16–26	PHYSICAL PAGE NUMBER

MR-2657

UBA PAGING RAM (WRITE)

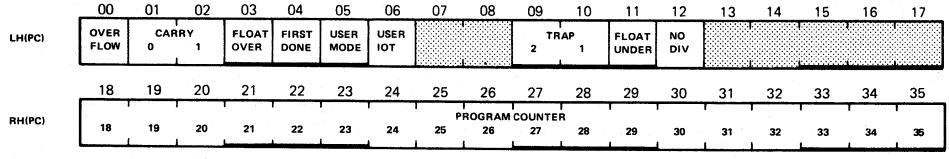


NOTE: ALL BITS WRITE ONLY.

18	READ REVERSE
19	DISABLE PARITY BIT TRANSFER TO UNIBUS
20	FAST TRANSFER MODE
21	ADDRESS IS VALID
<22-24>	MUST BE ZERO

MR-2656

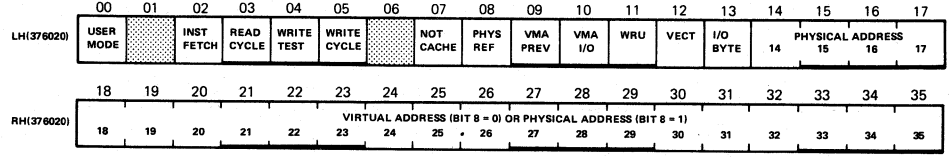
PC WORD



0 OVERFLOW
1 CARRY 0
2 CARRY 1
3 FLOATING OVERFLOW
4 FIRST PART DONE
5 USER MODE
6 USER IOT (ALSO PCU)
9 TRAP 2
10 TRAP 1
11 FLOATING UNDERFLOW
12 NO DIVIDE
18–35 PROGRAM COUNTER

VMA

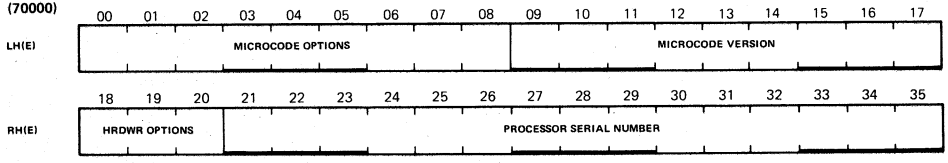
MR-2827



0 USER MODE
2 INSTRUCTION FETCH
3 READ CYCLE
4 WRITE TEST
5 WRITE CYCLE
7 DO NOT LOOK IN CACHE
8 PHYSICAL REFERENCE
9 VMA PREVIOUS
10 VMA I/O
11 WHO ARE YOU
12 VECTOR
13 I/O BYTE INSTRUCTION
14–17 BITS 14–17 OF PHYSICAL ADDRESS (OR 0S)
18–35 BITS 18–35 OF VIRTUAL ADDRESS (BIT 8 = 0) OR PHYSICAL ADDRESS (BIT 8 = 1)

MR-2826

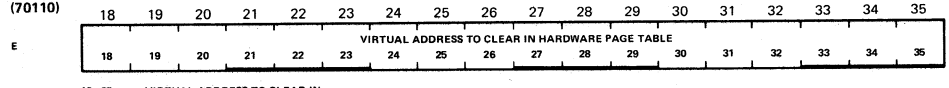
APRID – Read Processor ID
(70000)



0–8 RESERVED FOR MICROCODE VERSION
9–17 MICROCODE VERSION NUMBER
18–20 HARDWARE OPTIONS (BITS CURRENTLY = 0)
21–35 PROCESSOR SERIAL NUMBER.

MR 2801

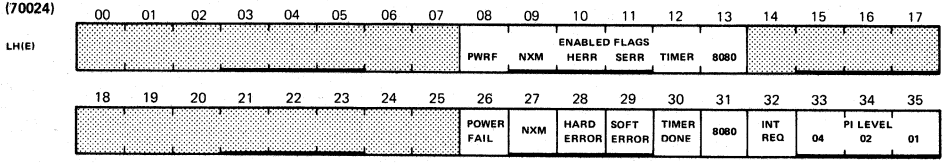
CLRPT – Clear Page Table
(70110)



18–35 VIRTUAL ADDRESS TO CLEAR IN HARDWARE PAGE TABLE.

MR-2807

RDAPR – Read Processor Conditions (70024)

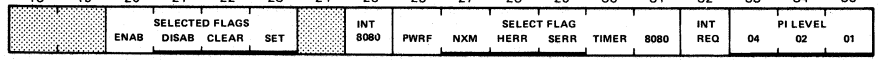


NOTE: PAGE FAIL OCCURS IF ERROR IS RESULT OF CPU MEMORY REQUEST. NXM FLAG ALSO SETS IN UNIBUS DEVICE IF ERROR IS RESULT OF UNIBUS NPR REQUEST.

08	POWER FAIL ENABLED
09	NONEXISTENT MEMORY ERROR ENABLED
10	HARD MEMORY ERROR INTERRUPT ENABLED
11	SOFT MEMORY ERROR INTERRUPT ENABLED
12	INTERVAL TIMER ENABLED
13	8080 CONSOLE INTERRUPT ENABLED
26	POWER FAIL ERROR
27	NONEXISTENT MEMORY ERROR
28	HARD MEMORY ERROR (CANNOT BE CORRECTED BY ECC).
29	SOFT MEMORY ERR (CORRECT DATA PLACED ON BUS)
30	INTERVAL TIMER DONE
31	8080 CONSOLE INTERRUPT
32	INTERRUPT REQUESTED
33–35	PIA

MR-2803

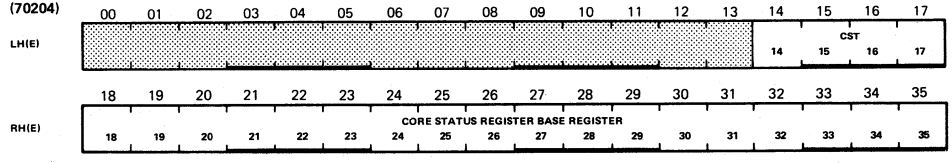
WRAPR – Write Processor Conditions (70020)



20	ENABLE CONDITIONS SELECTED BY BITS 26–31 TO CAUSE INTERRUPTS.
21	DISABLE INTERRUPTS FOR CONDITIONS SELECTED BY BITS 26–31.
22	CLEAR FLAGS INDICATED BY BITS 26–31.
23	SET FLAGS INDICATED BY BITS 26–31.
25	INTERRUPT 8080 CONSOLE
26	POWER FAIL
27	NONEXISTENT MEMORY ERROR
28	HARD MEMORY ERROR (CANNOT BE CORRECTED BY ECC)
29	SOFT MEMORY ERROR (CORRECT DATA PLACED ON BUS)
30	INTERVAL TIMER
31	8080 CONSOLE
32	GENERATE INTERRUPT REQUEST
33–35	PIA

MR-2802

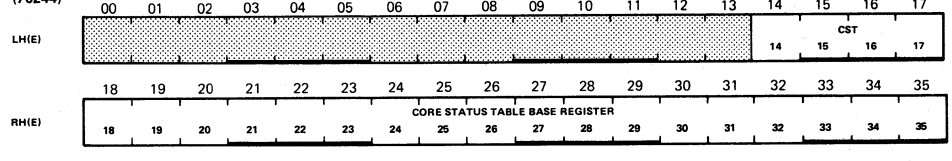
RDCSB – Read Core Status Table Base Register
(70204)



14–35 CST (CORE STATUS TABLE) BASE REGISTER

MR-2811

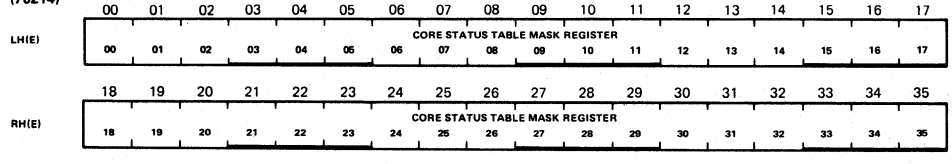
WRCSB – Write Core Status Table Base Register
(70244)



16-35 CST (CORE STATUS TABLE) BASE REGISTER

MR-2821

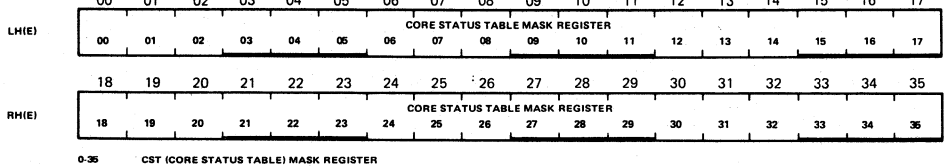
RDCSTM – Read Core Status Table Mask Register
(70214)



0–35 CST (CORE STATUS TABLE) MASK REGISTER

MR 2816

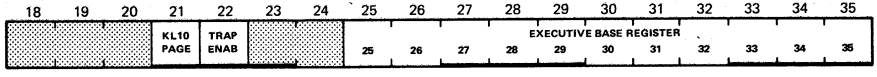
WRCSTM – Write Core Status Table Mask Register
(70254)



0-35 CST (CORE STATUS TABLE) MASK REGISTER

MR-2823

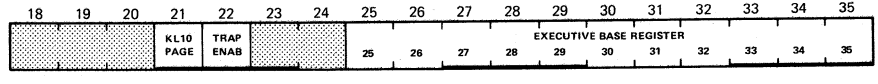
RDEBR – Read Executive Base Register
(70124)



21 KL10 PAGING MODE
22 TRAP (AND PAGING) ENABLE
25–35 EXECUTIVE BASE REGISTER (PHYSICAL PAGE NUMBER OF EPT)

MR-2810

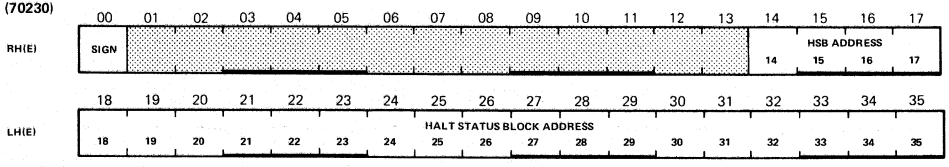
WREBR – Write Executive Base Register
(70120)



21 KL10 PAGING MODE
22 TRAP (AND PAGING) ENABLE
25–35 EXECUTIVE BASE REGISTER (PHYSICAL PAGE NUMBER OF EPT)

MR-2809

RDHSB – Read Halt Status Block Address
(70230)

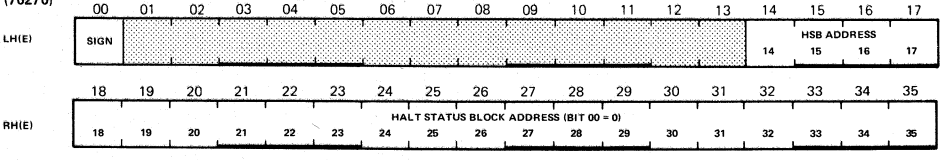


0 SIGN BIT = 0 = STORE HALT STATUS
SIGN BIT = 1 = DO NOT STORE HALT STATUS

14–35 HSB (HALT STATUS BLOCK) ADDRESS (BIT 00 = 0)

MR-2819

WRHSB – Write Halt Status Block Address
(70270)

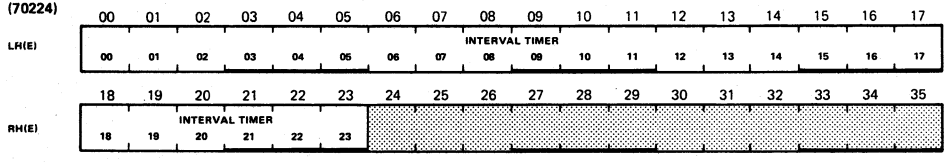


0 SIGN BIT = 0 = SOTRE HALT STATUS
SIGN BIT = 1 = DO NOT STORE HALT STATUS

14–35 HSB (HALT STATUS BLOCK) ADDRESS IF BIT 00 = 1

MR-2824

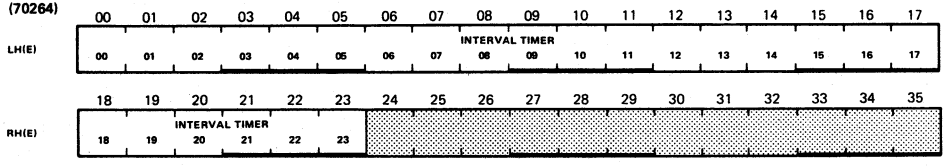
RDINT – Read Interval Timer
(70224)



0 INTERVAL TIMER PERIOD REGISTER (PERIOD = n MILLISECONDS)

MR-2818

WRINT – Write Interval Timer
(70264)

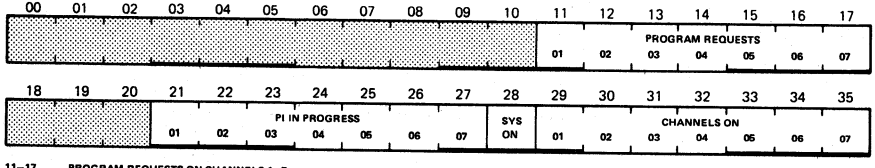


0–23 INTERVAL TIMER PERIOD REGISTER (PERIOD = N MILLISECONDS)

MR-2815

RDPI — Read PI System Status

(70064)

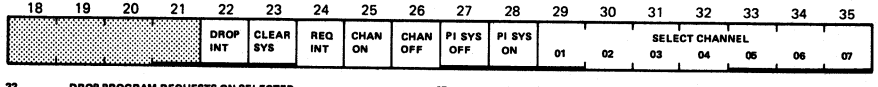


11–17	PROGRAM REQUESTS ON CHANNELS 1–7
21–27	INTERRUPTS HOLDING (IN PROGRESS) ON CHANNELS 1–7
28	PI SYSTEM ON
29–35	ACTIVE CHANNELS 1–7.

MR-2805

WRPI — Write PI System Conditions

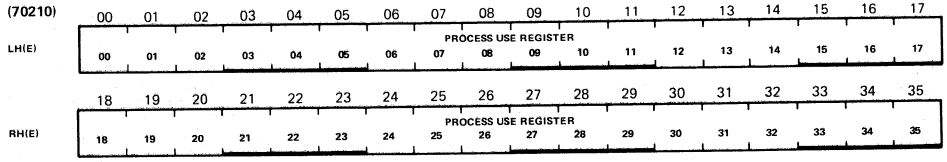
(70060)



22	DROP PROGRAM REQUESTS ON SELECTED CHANNELS.
23	CLEAR PI SYSTEM
24	INITIATE INTERRUPTS ON THE SELECTED CHANNELS.
25	TURN ON THE SELECTED CHANNELS.
26	TURN OFF THE SELECTED CHANNELS.
27	DEACTIVATE THE PI SYSTEM.
28	ACTIVATE THE PI SYSTEM.
29–35	SELECT CHANNELS FOR BITS 22, 24, 25, AND 26.

MR-2804

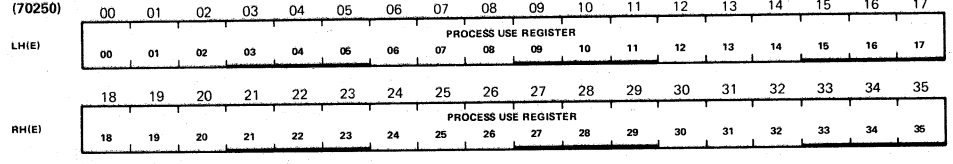
RDPUR – Read Process Use Register
(70210)



0–35 PUR (PROCESS USE REGISTER)

MR-2813

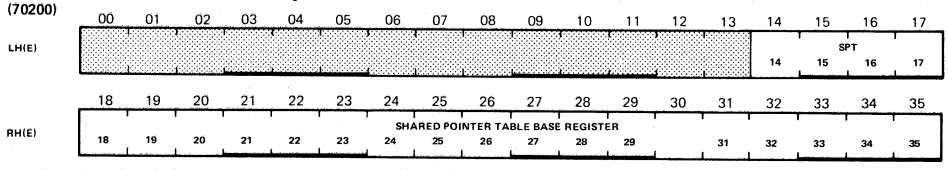
WRPUR – Write Process Use Register
(70250)



0-35 PUR (PROCESS USE REGISTER)

MR-2822

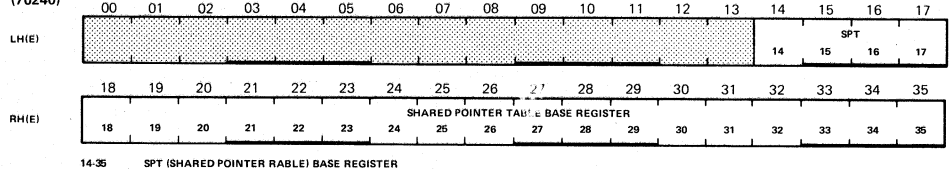
RDSPB – Read Shared Pointer Table Base Register
(70200)



14–35 SPT (SHARED POINTER TABLE) BASE REGISTER

MR-2812

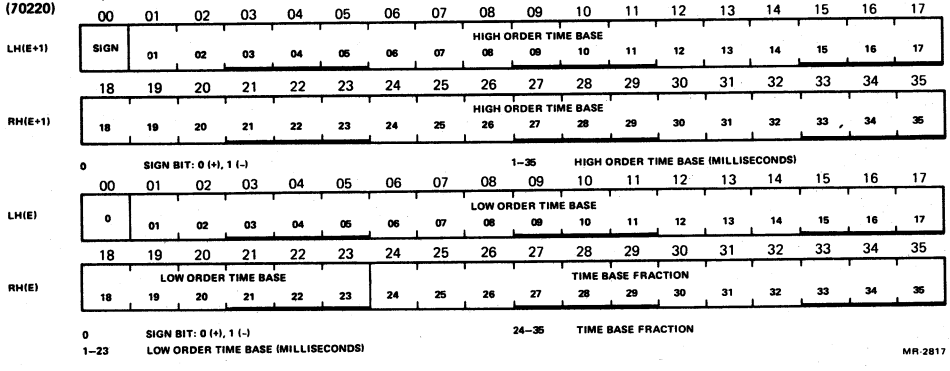
WRSPB – Write Shared Pointer Table Base Register
(70240)



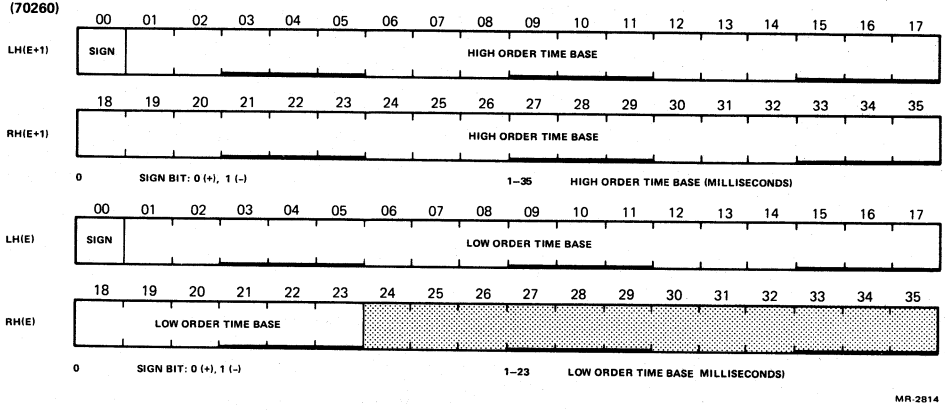
14-35 SPT (SHARED POINTER RABLE) BASE REGISTER

MR-2820

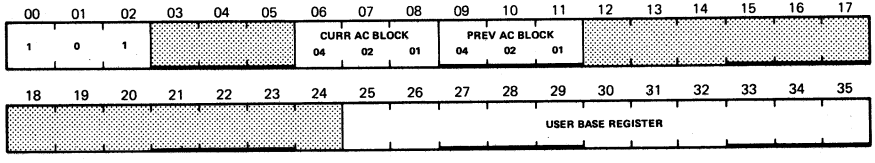
RDTIME – Read Time Base
(70220)



WRTIME – Write Time Base
(70260)



RDUBR – Read User Base Register
(70104)

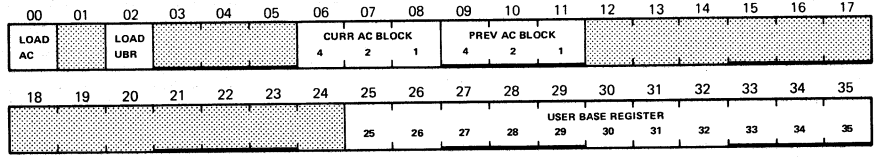


0	1
1	0
2	1

6–8	CURRENT AC BLOCK
9–11	PREVIOUS AC BLOCK
25–35	USER BASE REGISTER (PHYSICAL PAGE NUMBER OF UPT)

MR-2806

WRUBR – Write User Base Register
(70114)

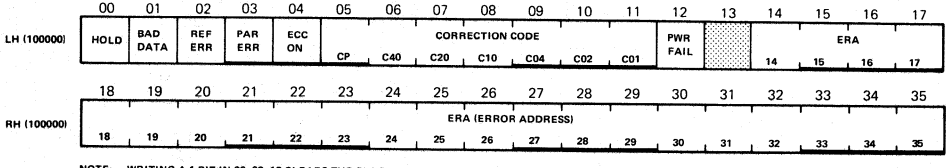


0	LOAD AC BLOCK NUMBERS
2	LOAD UBR
6–8	CURRENT AC BLOCK

9–11	PREVIOUS AC BLOCK
25–35	USER BASE REGISTER (PHYSICAL PAGE NUMBER OF UPT).

MR-2808

MEMORY STATUS REGISTER

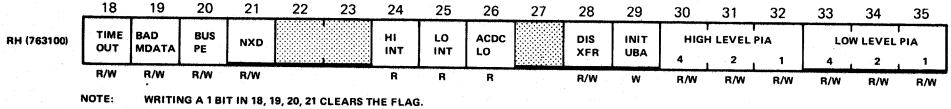


NOTE: WRITING A 1 BIT IN 00, 02, 12 CLEARS THE FLAG.
WRITING A 1 BIT IN 03 SETS THE FLAG, WRITING A 0 BIT CLEARS THE FLAG.

- 00 ERROR HOLD (ERROR CONDITION DETECTED BY CONTROLLER)
- 01 BAD DATA (UNCORRECTABLE READ ERROR)
- 02 REFRESH ERROR (INCOMPLETE WRITE CYCLE)
- 03 BUS PARITY ERROR DETECTED
- 04 ERROR CORRECTION ENABLED
- 05–11 CORRECTION CODE BITS
- 12 POWER FAIL (LOSS OF POWER OR BATTERY BACKUP LOW)
- 14–35 ERROR ADDRESS

MR-2660

UBA STATUS REGISTER

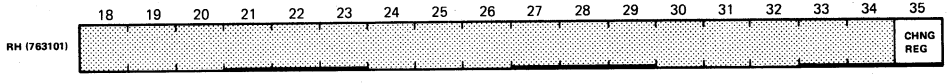


NOTE: WRITING A 1 BIT IN 18, 19, 20, 21 CLEARS THE FLAG.

- 18 UNIBUS ARBITRATOR TIME-OUT OR NONEXISTENT MEMORY ADDRESS.
- 19 BAD MEMORY DATA
- 20 KS10 (BACKPLANE) BUS PARITY ERROR
- 21 NONEXISTENT DEVICE
- 24 HIGH LEVEL INTERRUPT PENDING (BR7 AND BR6).
- 25 LOW LEVEL INTERRUPT PENDING (BR5 AND BR4).
- 26 AC OR DC LOW
- 28 DISABLE TRANSFER IF BMD (BIT 19 = 1).
- 29 INITIALIZE UBA AND UNIBUS DEVICES
- 30–32 HIGH LEVEL PIA.
- 33–35 LOW LEVEL PIA.

MR-2659

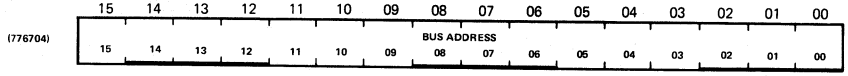
UBA MAINTENANCE REGISTER



BIT	FUNCTION
35	CHANGE REGISTER. MODIFIES 4 X 4 MEMORY ADDRESS.

MR-2658

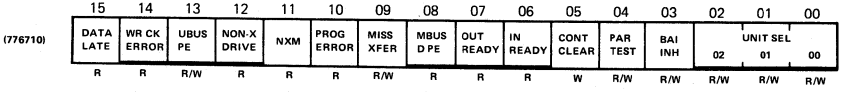
RH11 – RMBA – Bus Address Register



NOTE: ALL BITS READ/WRITE

MR-2579

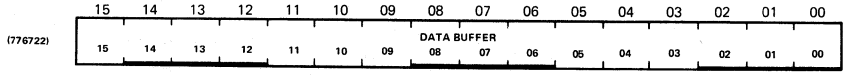
RH11 – RMCS2 – Control and Status Register 2



15	DATA LATE
14	WRITE CHECK
13	UNIBUS PARITY ERROR
12	NON-EXISTENT DRIVE
11	NON-EXISTENT MEMORY
10	PROGRAM ERROR – RH BUSY
09	MISSED TRANSFER
08	MASSBUS DATA PARITY ERROR
07	OUTPUT READY
06	INPUT READY
05	CONTROLLER CLEAR
04	PARITY TEST
03	BUS ADDRESS INCREMENT INHIBIT
<02:00>	UNIT SELECT

MR-2580

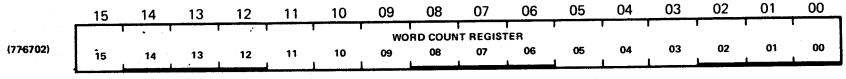
RH11 – RMDB – Data Buffer Register



NOTE: ALL BITS READ/WRITE

MR-2581

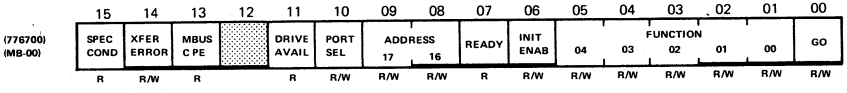
RH11 – RMWC – Word Count Register



NOTE: ALL BITS READ/WRITE

MR-2582

RH11 – RMCS1 – Control and Status Register 1

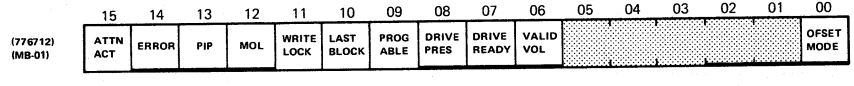


NOTE: SHARED REGISTER BITS <15:13> AND <10:06> ARE IN RH.
REFER TO DCL PRINT RG3 AND RG6.

15	SPECIAL CONDITION
14	TRANSFER ERROR
13	MASSBUS CONTROL PARITY ERROR
11	DRIVE AVAILABLE
10	PORT SELECT
<09:08>	UNIBUS ADDRESS EXTENSION BITS 17 AND 16
06	INTERRUPT ENABLE

MR-2583

RH11 – RMDS – Drive Status



NOTE: ALL BITS READ ONLY.
REFER TO DCL PRINT RG6.

15	ATTENTION ACTIVE
13	POSITIONING IN PROGRESS
12	MEDIUM ON LINE
10	LAST BLOCK TRANSFERRED
09	PROGRAMMABLE
08	DRIVE PRESENT
06	VALID VOLUME

RH11 – RMER1 – Error Register 1

(776714)
(MB-02)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DATA CHECK	UN SAFE	OPER INC	DR T ERROR	WR LK ERROR	I ADR ERROR	A OV ERROR	H CRC ERROR	H COM ERROR	ECC ERROR	WR CK FAIL	FMT ERROR	PAR ERROR	RMR	ILL REG	ILL FUNC

NOTE: ALL BITS READ/WRITE.
REFER TO DCL PRINT RG0.

13	OPERATION INCOMPLETE	06	ECC HARD ERROR
12	DRIVE TIMING ERROR	05	WRITE CLOCK FAIL
11	WRITE LOCK ERROR	04	FORMAT ERROR
10	INVALID ADDRESS ERROR	03	PARITY ERROR
09	ADDRESS OVERFLOW ERROR	02	REGISTER MODIFICATION REFUSED
08	HEADER CRC ERROR	01	ILLEGAL REGISTER
07	HEADER COMPARE ERROR	00	ILLEGAL FUNCTION

MR-2584

RH11 – RMMR1 – Maintenance Register ONE

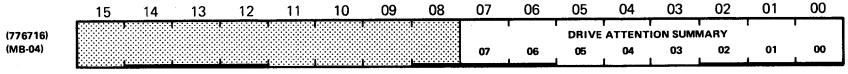
(776724)
(MB-03)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OCCUP	RUN GO	END BLOCK	RX EXCPT	ENB SERCH	LOOK SYNC	CRC OUT	PACK DATA	PACK HEADR	CONT	PROM STROB	ENB ECC	WRITE DATA	LAST SECTR	LAST S&T	DIAG MODE

15	OCCUPIED	07	PACK HEADER AREA
14	RUN AND GO	06	CONTINUE
13	END OF BLOCK LEVEL	05	PROM STROBE
12	RECEIVED EXCEPTION	04	ENABLE ECC OUT
11	ENABLE SEARCH	03	WRITE DATA
10	PACK LOOKING FOR SYNC	02	LAST SECTOR
09	ENABLE CRC OUT	01	LAST SECTOR AND TRACK
08	PACK DATA AREA	00	DIAGNOSTIC MODE

MR-2588

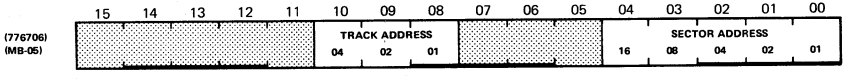
RH11 – RMAS – Attention Summary



NOTE: ALL BITS READ/WRITE.
REFER TO DCL PRINT DP.

MR-2589

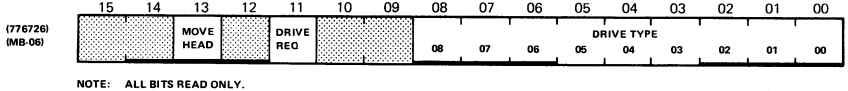
RH11 – RMDA – Desired Track/Sector Address



NOTE: ALL BITS READ/WRITE.

MR-2590

RH11 – RMDT – Drive Type

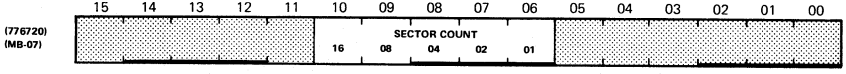


NOTE: ALL BITS READ ONLY.
REFER TO DCL PRINT EC8.

15 NOT BLOCK ADDRESSED
14 TAPE DRIVE
13 MOVING
11 DRIVE REQUEST REQUIRED

MR-2591

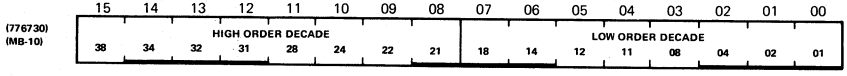
RH11 – RMLA – Look Ahead



NOTE: ALL BITS READ ONLY.

MR-2592

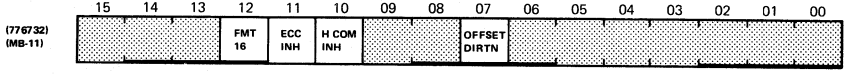
RH11 – RMSN – Serial Number



NOTE: ALL BITS READ ONLY.

MR-2593

RH11 – RMOF – Offset



NOTE: ALL BITS READ/WRITE.
REFER TO DCL PRINT RG1.

12	FORMAT 16 SECTORS	10	HEADER COMPARE INHIBIT
11	ECC INHIBIT	07	OFFSET DIRECTION

MR-2594

RH11 – RMDC – Desired Cylinder

(776734)
(MB-12)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
						DC 512	DC 256	DC 128	DC 64	DC 32	DC 16	DC 08	DC 04	DC 02	DC 01

NOTE: ALL BITS READ WRITE.
REFER TO DCL PRINT SS1.

MR-2595

RH11 – RMHR – Current Cylinder Address

(776736)
(MB-13)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

NOTE: UNUSED

MR-2596

RH11 – RMMR2 – Maintenance Register Two

(776740)
(MB-14)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
REQ A	REQ B	CONTR TAG	COMND BRNCH	CONTR TAG	HEAD TAG	BUS IN LINES									
						09	08	07	06	05	04	03	02	01	00

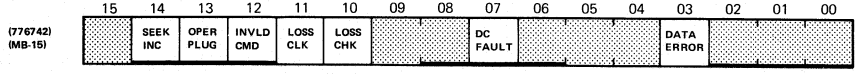
15	REQUEST ON PORT A
14	REQUEST ON PORT B
13	CONTROL SELECT TAG
12	COMMAND SEQUENCER IS BRANCHING
11	CONTROL SELECT OR CYLINDER SELECT TAG
10	CONTROL SELECT OR HEAD SELECT TAG

NOTE:

BUS IN BITS	CYLINDER ADDRESS TAG	HEAD SELECT TAG	CONTROL SELECT TAG
0	1	1	WRITE GATE
1	2	2	READ GATE
2	4	4	SERVO OFFSET PLUS
3	8	NOT USED	SERVO OFFSET PLUS
4	16	NOT USED	FAULT CLEAR
5	32	NOT USED	NOT USED
6	64	NOT USED	RETURN TO ZERO
7	128	NOT USED	NOT USED
8	256	NOT USED	NOT USED
9	512	NOT USED	NOT USED

MR-2597

RH11 – RMMR2 – Error Register 2

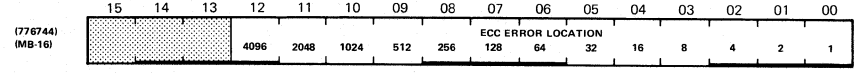


NOTE: ALL BITS READ/WRITE

12	INVALID COMMAND	07	DC OF HEAD SELECT FAULT
11	LOSS OF SYSTEM CLOCK	03	DATA PARITY ERROR RECEIVED
10	LOSS OF BIT CHECK		

MR-2598

RH11 – RMEC1 – ECC Position Register 1

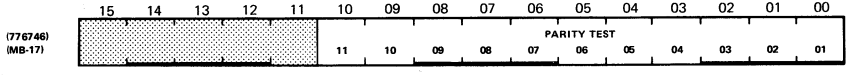


NOTE: ALL BITS READ ONLY.

<12:00> BURST LOCATION CODE FOR ECC

MR-2586

RH11 — RMEC2 — ECC Pattern



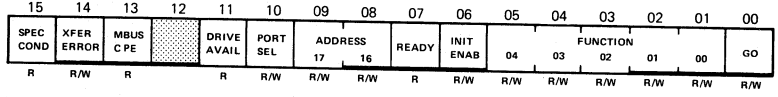
NOTE: ALL BITS READ ONLY.
REFER TO DCL PRINT EC1.

<10:00> PARITY TEST

MR-2587

RH11 – RPCS1 – Control and Status Register 1

(776700)
(MB-00)



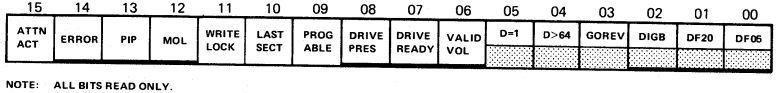
NOTE: SHARED REGISTER BITS <15:13> AND <10:06> ARE IN RH.

15	SPECIAL CONDITION
14	TRANSFER ERROR
13	MASSBUS CONTROL PARITY ERROR
11	DRIVE AVAILABLE
10	PORT SELECT
<09:08>	UNIBUS ADDRESS EXTENSION BITS 17 AND 16
06	INTERRUPT ENABLE

MR-2599

RH11 – RPDS – Drive Status

(776712)
(MB-01)

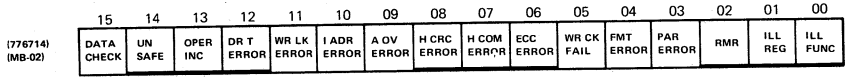


NOTE: ALL BITS READ ONLY.

15	ATTENTION ACTIVE
13	POSITIONING IN PROGRESS
12	MEDIUM ON LINE
10	LAST SECTOR TRANSFERRED
09	PROGRAMMABLE
08	DRIVE PRESENT
06	VALID VOLUME
05	RP04 – DIFFERENCE EQUALS ONE
04	RP04 – DIFFERENCE LESS THAN 64
03	RP04 – GO REVERSE
02	RP04 – DRIVE TO INNER GUARD BAND
01	RP04 – DRIVE FORWARD 20 INCH/SEC
00	RP04 – DRIVE FORWARD 5 INCH/SEC
<05:00>	RP06 UNUSED

MR-2600

RH11 – RPER1 – Error Register 1

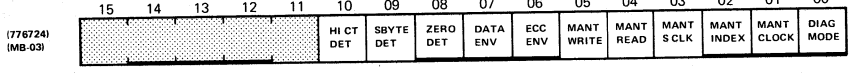


NOTE: ALL BITS READ/WRITE.

13	OPERATION INCOMPLETE
12	DRIVE TIMING ERROR
11	WRITE LOCK ERROR
10	INVALID ADDRESS ERROR
09	ADDRESS OVERFLOW ERROR
08	HEADER CRC ERROR
07	HEADER COMPARE ERROR
06	ECC HARD ERROR
05	WRITE CLOCK FAIL
04	FORMAT ERROR
03	PARITY ERROR
02	REGISTER MODIFICATION REFUSED
01	ILLEGAL REGISTER
00	ILLEGAL FUNCTION

MR-2601

RH11 – RPMR – Maintenance Register

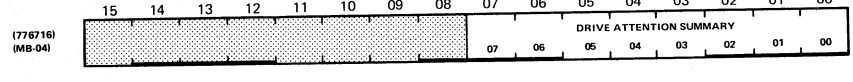


NOTE: ALL BITS READ/WRITE.

10	HIGH COUNT DETECT
09	SYNC BYTE DETECTED
08	ZERO DETECT
07	DATA ENVELOPE
06	ECC ENVELOPE
03	MAINTENANCE SECTOR CLOCK
00	DIAGNOSTIC MODE

MR-2602

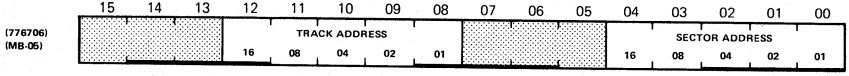
RH11 – RPAS – Attention Summary



NOTE: ALL BITS READ/WRITE.

MR-2603

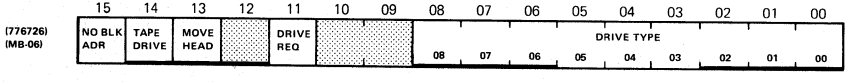
RH11 – RPDA – Desired Track/Sector Address



NOTE: ALL BITS READ/WRITE.

MR-2604

RH11 – RPDT – Drive Type

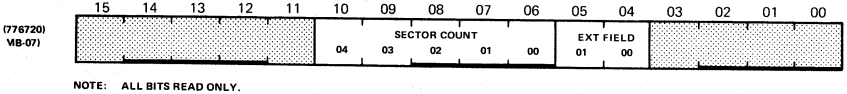


NOTE: ALL BITS READ ONLY.

15 NOT BLOCK ADDRESSED
14 TAPE DRIVE
13 MOVING HEAD
11 DRIVE REQUEST REQUIRED

MR-2605

RH11 – RPLA – Look Ahead

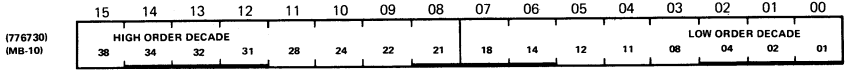


NOTE: ALL BITS READ ONLY.

<05:04> EXTENSION FIELD
05 04 HEAD LOCATION
0 0 = <20% (IN FIRST 20% OF SECTOR)
0 1 = 20 – 40%
1 0 = 40 – 80%
1 1 = >80% (IN LAST 20% OF SECTOR)

MR-2606

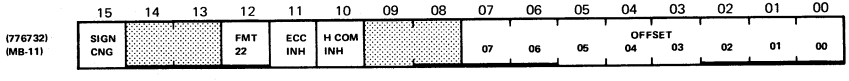
RH11 – RPSN – Serial Number



NOTE: ALL BITS READ ONLY.
REFER TO DCL PRINT EC8.

MR-2607

RH11 – RPOF – Offset

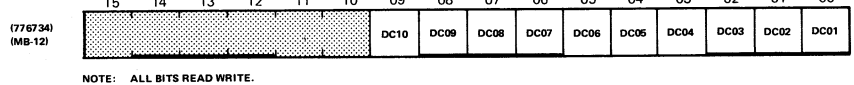


NOTE: ALL BITS READ/WRITE.

15 SIGN CHANGE
12 FORMAT 22 SECTORS
11 ECC INHIBIT
10 HEADER COMPARE INHIBIT

MR-2608

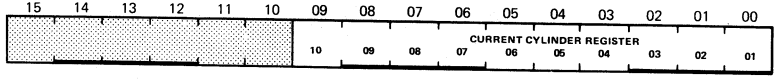
RH11 – RPDC – Desired Cylinder



NOTE: ALL BITS READ WRITE.

MR-2610

RH11 – RPCC – Current Cylinder Address

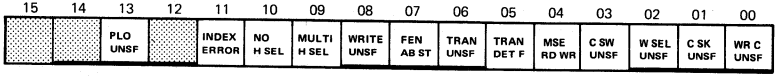


NOTE: ALL BITS READ ONLY.

RP06 – CURRENT CYLINDER BIT 10

RH11 – RPER2 – Error Register 2

MR-2609

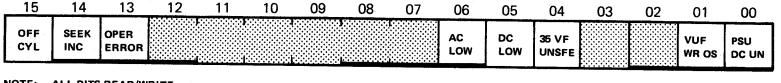


NOTE: ALL BITS READ/WRITE

13 PHASE LOCKED OSCILLATOR UNSAFE
11 INDEX ERROR
10 NO HEAD SELECT
09 MULTIPLE HEAD SELECT
08 WRITE READY UNSAFE
07 FAILSAFE ENABLE
RP06 – ABNORMAL STOP
06 TRANSITION UNSAFE
05 TRANSITION DETECTOR FAILURE
04 MONITOR SEQUENCE ERROR
RP06 – READ AND WRITE
03 CURRENT SWITCH UNSAFE
02 WRITE SELECT UNSAFE
01 CURRENT SINK FAILURE
00 WRITE CURRENT UNSAFE

RH11 – RPER3 – Error Register 3

MR-2611

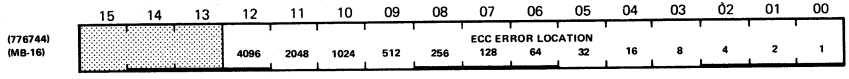


NOTE: ALL BITS READ/WRITE.

15 OFF CYLINDER
14 SEEK INCOMPLETE
13 RP06 – OPERATOR PLUG ERROR
06 AC VOLTAGE UNSAFE
05 DC VOLTAGE UNSAFE
05 DC VOLTAGE UNSAFE
04 RP06 – 35 VOLTS UNSAFE
01 VELOCITY UNSAFE
PR06 – WRITE AND OFFSET
00 PACK SPEED UNSAFE
RP06 – DC VOLTAGE UNSAFE

MR-2612

RH11 – RPEC1 – ECC Position Register

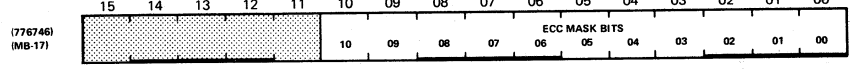


NOTE: ALL BITS READ ONLY.

<12:00> BURST LOCATION CODE FOR ECC

MR-2613

RH11 – RPEC2 – ECC Pattern

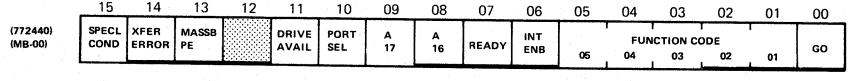


NOTE: ALL BITS READ ONLY.

<10:00> ERROR BURST AT COMPLETION OF ECC

MR-2614

MTCS1 — Control Register 1

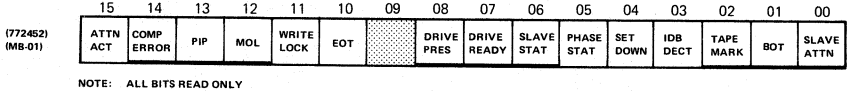


NOTE: ALL BITS READ/WRITE.

15	SPECIAL CONDITION
14	TRANSFER ERROR
13	MASSBUS CONTROL BUS PARITY ERROR
11	DRIVE AVAILABLE
10	PORT SELECT
<09–08>	ADDRESS 17–16
06	INTERRUPT ENABLE

MR-2615

MTDS — Status Register



NOTE: ALL BITS READ ONLY

15	ATTENTION ACTIVE
14	COMPOSITE ERROR
13	POSITIONING IN PROGRESS
12	MEDIUM ON LINE
10	END OF TAPE
08	DRIVE PRESENT
06	SLAVE STATUS CHANGE
05	PHASE ENCODED STATUS
04	SETTLE DOWN
03	IDENTIFICATION BURST DETECTED
02	TAPE MARK DETECTED
01	BEGINNING OF TAPE
00	SLAVE ATTENTION

MR-2620

MTER – Error Register

(772454)
(MB-02)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CORR CRC	UN SAFE	OPER INC	DR T ERROR	NXF	CS ITM	FC ERROR	N-STD GAP	PFE LRC	NDE VPE	D BUS PE	FMT ERROR	CBUS PE	REG MOD	ILL REG	ILL FUNC

NOTE: ALL BITS READ ONLY

15 CORRECTABLE DATA ERROR OR CRCC READ DOES NOT MATCH COMPUTED CRCC
14 UNSAFE
13 OPERATION INCOMPLETE
12 DRIVE TIMING ERROR
11 NONEXECUTABLE FUNCTION
10 CORRECTABLE SKEW OR ILLEGAL TAPE MARK (NRZI)
09 FRAME COUNT ERROR
08 NONSTANDARD GAP TAPE CHAR
07 PE-FORMAT ERROR OR NRZI CHECK CHART ERROR
06 PE-NONCORRECTABLE DATA ERROR NRZI – VERTICAL PARITY ERROR
05 DATA BUS PARITY ERROR
04 FORMAT ERROR
03 CONTROL BUS PARITY
02 REGISTER MODIFICATION REFUSED
01 ILLEGAL REGISTER
00 ILLEGAL FUNCTION

MR-2621

MTMR – Maintenance Register

(772464)
(MB-03)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
MAINTENANCE DATA FIELD									SEL SCLK	MAINT CLK	MAIN OP CODE				MAINT MODE
08	07	06	05	04	03	02	01	00			03	02	01	00	

NOTE: ALL BITS READ/WRITE.

06 SELECTED SLAVE CLOCK: WRT CLOCK SIG GEN BY SEL SLAVE
05 MAINTENANCE CLOCK
<04-01> MAINTENANCE OPERATION CODE
00 MAINTENANCE MODE

MR-2626

MTAS – Attention Summary

(772456)
(MB-04)

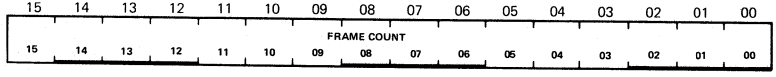
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
								ATTENTION SUMMARY							
								07	06	05	04	03	02	01	00

NOTE: ALL BITS READ/WRITE

MR-2622

MTFC – Frame Count

(772446)
(MB-05)

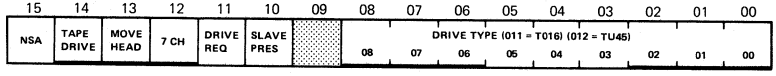


NOTE: ALL BITS READ/WRITE

MR-2618

MTDT – Drive Type

(772466)
(MB-06)

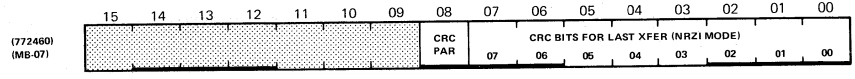


NOTE: ALL BITS READ ONLY

15 NOT SECTOR ADDRESSED
14 TAPE DRIVE
13 NONMOVING HEAD UNIT
12 7 CHANNEL UNIT – NEGATED ON
9 CHANNEL DRIVE OR POWER LOSS
11 DRIVE REQUEST REQUIRED
10 SLAVE PRESENT

MR-2627

MTCK – Check Character

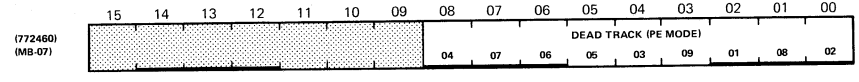


NOTE: ALL BITS READ ONLY

08 CONTROL BUS PARITY

MR-2623

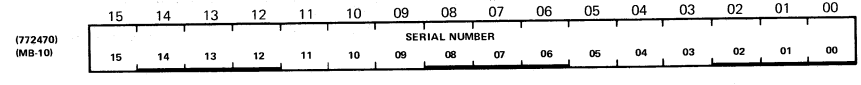
MTCK – Check Character



NOTE: ALL BITS READ ONLY

MR-2624

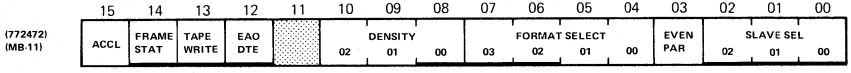
MTSN – Serial Number



NOTE: ALL BITS READ ONLY

MR-2628

MTTC – Tape Control

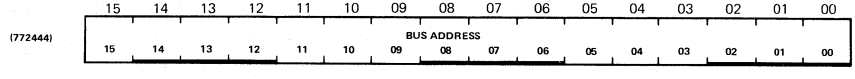


NOTE: ALL BITS READ/WRITE

15 ACCELERATION
14 FRAME COUNT STATUS
13 TAPE CONTROL WRITE
12 ENABLE ABORT ON DATA TRANSFER ERROR
03 EVEN PARITY

MR-2629

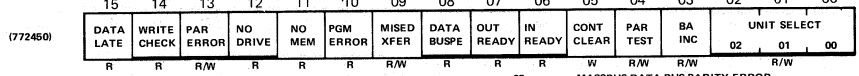
MTBA – Unibus Address



NOTE: ALL BITS READ/WRITE

MR-2617

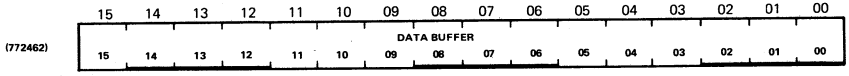
MTCS2 – Control Register 2



14 WRITE CHECK ERROR
13 PARITY ERROR
12 NONEXISTENT DRIVE
11 NONEXISTENT MEMORY
10 PROGRAM ERROR
09 MISSED TRANSFER
08 MASSBUS DATA BUS PARITY ERROR
08 MASSBUS DATA BUS PARITY ERROR
07 OUTPUT READY
06 INPUT READY
05 CONTROLLER CLEAR
04 PARITY TEST
03 BUS ADDRESS INCREMENT INHIBIT

MR-2619

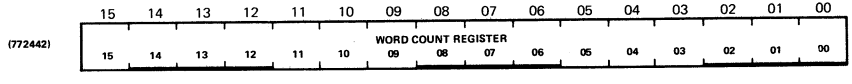
MTDB — Data Buffer



NOTE: ALL BITS READ/WRITE

MR-2625

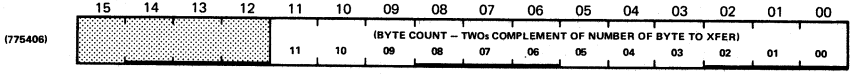
MTWC — Word Count



NOTE: ALL BITS READ/WRITE.

MR-2616

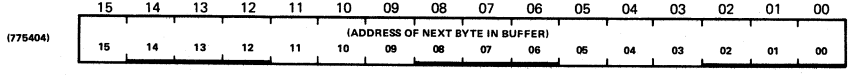
LPBCTR – DMA Byte Count Register



NOTE: ALL BITS READ/WRITE.

MR-2015

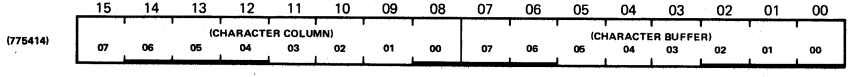
LPBSAD – DMA Bus Address Register



NOTE: ALL BITS READ/WRITE

MR-2014

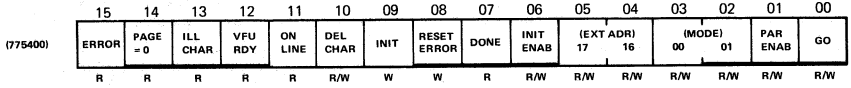
LPCCTR – Column Count Register (High Byte)
LPCBUF – Character Buffer Register (Low Byte)



NOTE: BITS <15:08> READ/WRITE

MR-2018

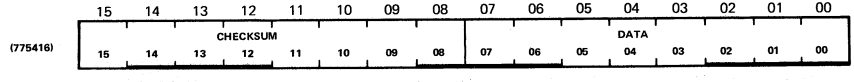
LPCSRA – Control and Status Register "A"



15	LOGICAL "OR" OF ALL ERRORS
14	PAGE COUNTER INCREMENTED TO ZERO
13	ILLEGAL CHARACTER
12	DAVFU READY (SET IF OPTICAL VFU)
11	PRINTER READY AND ON LINE
10	DELIMITER CHAR HELD
09	INITIALIZE - RESET FLAGS SET DONE
08	RESET ERROR, SET DONE, RESET GO
06	INTERRUPT ENABLE
<05:04>	EXTENDED UNIBUS ADDRESS BITS 17 AND 16
<03:02>	MODE BITS 00 = NORMAL 01 = TEST MODE (INHIBIT PRINTING) 10 = VFU LOAD (DMA TO VFU) 11 = RAM LOAD (DMA MODE ONLY)
01	PARITY ENABLE (RAM AND MEMORY)

MR-2012

LPCKSM – Checksum Register
LPTDAT – Printer Data Register



NOTE: ALL BITS READ ONLY

MR-2013

LPCSRB – Control and Status Register "B"

(775402)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VALID DATA	LA180	NOT RDY	PAR BIT	OP VFU	02	(TEST) 01	00	OFF LINE	VFU ERROR	PAR ERROR	MEM ERROR	RAM ERROR	SYNC T O	DEM T O	GO ERROR
R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R	R	R/W

14 SET IF LA180 TYPE PRINTER
13 NOT READY (OTHER THAN TAPE FAULT)
12 DATA PARITY BIT (AS SENT TO PRINTER)
11 OPTICAL VFU (ZERO IF DAVFU)
05 PARITY ERROR AT PRINTER
04 MEMORY PARITY ERROR
03 RAM PARITY ERROR DURING DMA XFER
02 MASTER SYNC TIME OUT (NO SSYNC)
01 DEMAND TIME OUT
00 GO SET AND "ERROR" OR "DEMAND

<10:08> FORCE ERROR CONDITIONS

02	01	00	
0	0	0	NORMAL
0	0	1	DEMAND TIME OUT
0	1	0	M SYNC TIME OUT
0	1	1	RAM PARITY ERROR
1	0	0	MEM PARITY ERROR
1	0	1	LPT DATA PAR ERROR
1	1	0	DECREMENT PAGE COUNT
1	1	1	NOT USED

MR-2016

LPPCTR – Page Count Register

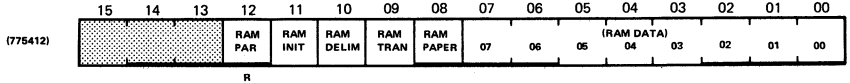
(775410)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
				(PAGE COUNT)											
				11	10	09	08	07	06	05	04	03	02	01	00

NOTE: ALL USED BITS READ/WRITE

MR-2017

LPRAMD – RAM Data Register

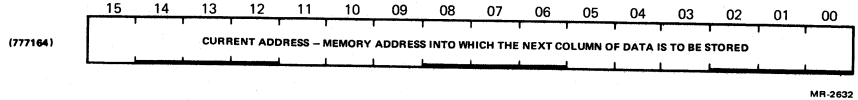


NOTE: ALL USED BITS EXCEPT 12 READ/WRITE

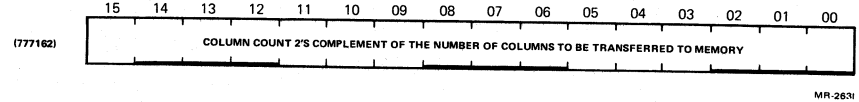
12	RAM PARITY BIT	09	TRANSLATION BIT – RDAT TO PRINTER
11	INTERRUPT BIT – GEN A BR	08	PAPER INSTRUCTION RDAT TO DAVFU
10	DELIMITER – TAKE DATA FROM RAM	<07:00>	RAM DATA – ADDRESS IS IN LPCBUF

MR-2019

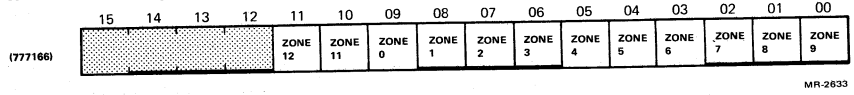
CDBA – Current Address Register



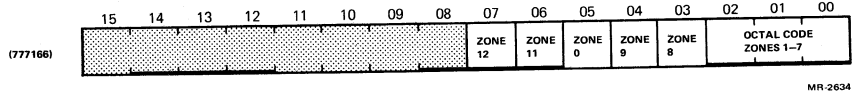
CDCC – Column Count Register



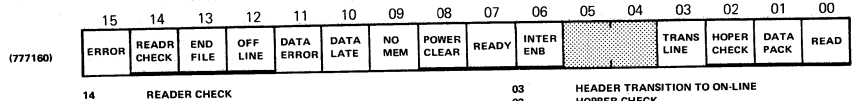
CDDB — Data Buffer Register — Nonpacking Mode



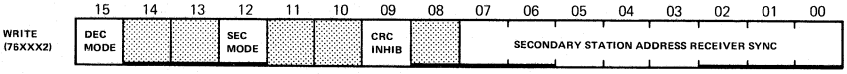
CDDB — Data Buffer Register — Packing Mode



CDST — Status and Control Register



PARCSR — Parameter Control and Status Register



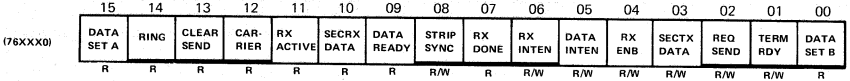
NOTE: XXX = 030 (DUP 0), 031 (DUP 1)

12 SECONDARY MODE SELECT

09 CRC INHIBIT

MR-2637

RXCSR — Receiver Control and Status Register



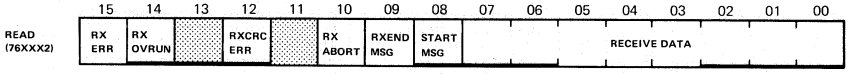
NOTE: XXX = 030 (DUP 0), 031 (DUP 1)

15 DATA SET CHANGE A
13 CLEAR TO SEND
11 RECEIVER ACTIVER
10 SECONDARY RECEIVED DATA
09 DATA SET READY
07 RECEIVER DONE

06 RECEIVER INTERRUPT ENABLE
05 DATA SET INTERRUPT ENABLE
04 RECEIVER ENABLE
03 SECONDARY TRANSMIT DATA
02 REQUEST TO SEND
01 DATA TERMINAL READY
00 DATA SET CHANGE B

MR-2635

RXDBUF — Receiver Data Buffer Register



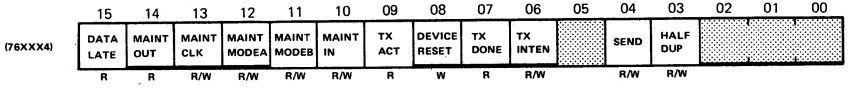
NOTE: XXX = 030 (DUP 0), 031 (DUP 1)

15 RECEIVER ERROR
14 RECEIVER OVERRUN
12 RECEIVER CRC ERROR

10 RECEIVER ABORT
09 END OF RECEIVED MESSAGE
08 START OF RECEIVED MESSAGE

MR-2636

TXCSR — Transmitter Control and Status Register

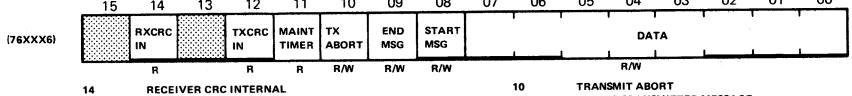


NOTE: XXX = 030 (DUP 0), 031 (DUP 1)

15	TRANSMITTER DATA LATE ERROR
14	MAINTENANCE TRANSMIT DATA OUT
13	MAINTENANCE CLOCK
12	MAINTENANCE MODE SELECT A
11	MAINTENANCE MODE SELECT B
10	MAINTENANCE INPUT DATA
09	TRANSMITTER ACTIVE
08	DEVICE RESET
07	TRANSMITTER DONE
06	TRANSMITTER INTERRUPT ENABLE
03	HALF DUPLEX FULL DUPLEX

MR-2638

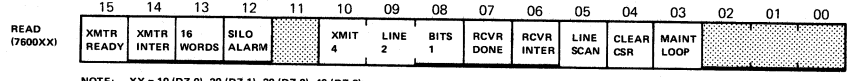
TXDBUF — Transmitter Data Buffer Register



14	RECEIVER CRC INTERNAL
12	TRANSMITTER CRC INTERNAL
11	MAINTENANCE TIMER
10	TRANSMIT ABORT
09	END OF TRANSMITTED MESSAGE
08	TRANSMIT START OF MESSAGE

MR-2639

CSR – Control and Status Register

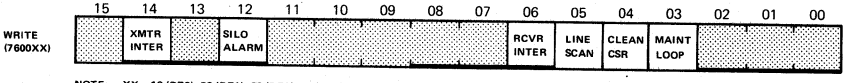


NOTE: XX = 10 (DZ 0), 20 (DZ 1), 30 (DZ 2), 40 (DZ 3)

15	TRANSMIT READY
14	TRANSMIT INTERRUPT ENABLE
13	SILO HAS 16 WORDS
12	SILO ALARM INTERRUPT WHEN BIT 13 ON
<10:08>	TRANSMSIT LINE BITS
07	RECEIVER DONE
06	RECEIVER INTERRUPT
05	TURN ON LINE SCAN
04	CLEAR UARTS, SILO, CSR, 15 MS LONG
03	MAINTAIN LOOP TRANSMIT TO RECEIVE

MR-2642

CSR – Control and Status Register

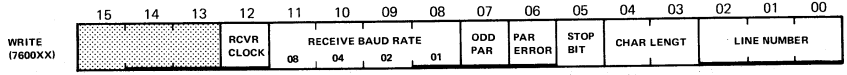


NOTE: XX = 10 (DZ0), 20 (DZ1), 30 (DZ2), 40 (DZ3)

14	TRANSMIT INTERRUPT ENABLE
12	ENABLE SILO ALARM INTERRUPT
06	RECEIVE INTERRUPT ENABLE
05	TURN ON LINE SCAN
04	CLEAN UARTS, SILO, CSR
03	MAINTAIN LOOP TRANSMIT TO RECEIVE

MR-2641

LPR — Line Parameter Register



NOTE: XX = 12 (DZ 0), 22 (DZ 1), 32 (DZ 2), 42 (DZ 3)

12 TURN ON RECEIVE CLOCK

<11:08> RECEIVE BAUD RATE

00 = 50	05 = 300	12 = 2400
01 = 75	06 = 600	13 = 3600
02 = 110	07 = 1200	14 = 4800
03 = 134	10 = 1800	15 = 7200
04 = 150	11 = 2000	16 = 9600
		17 = 192K

07 USE ODD PARITY WHEN SET

06 PARITY ERROR ENABLE

05 STOP BIT 0 = 1 1 = 1.5 OR 2

<04:03> CHARACTER STOP LENGTH

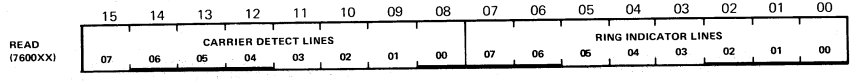
00 = 5 10 = 7

01 = 6 11 = 8

<02:00> LINE NUMBER TO LOAD IF BIT 12 IS SET ALLOWS RECEIVE

MR-2643

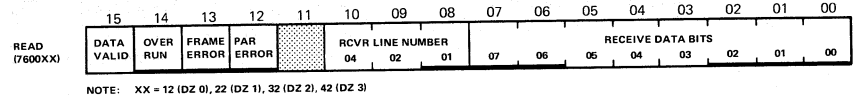
MSR — Modem Status Register



NOTE: XX = 16 (DZ 0), 26 (DZ 1), 36 (DZ 2), 46 (DZ 3)

MR-2648

RBUF — Receiver Buffer



NOTE: XX = 12 (DZ 0), 22 (DZ 1), 32 (DZ 2), 42 (DZ 3)

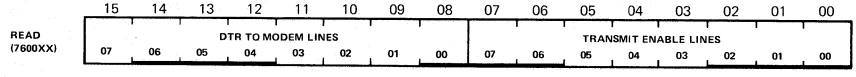
15 RECEIVE DATA VALID

14 OVER RUN ERROR

<10:08> RECEIVER LINE NUMBER

MR-2644

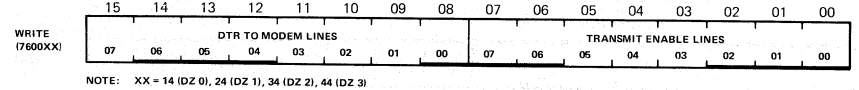
TCR – Transmit Control Register



NOTE: XX = 14 (DZ 0), 24 (DZ 1), 34 (DZ 2), 44 (DZ 3)

MR-2646

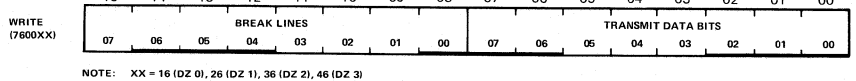
TCR – Transmit Control Register



NOTE: XX = 14 (DZ 0), 24 (DZ 1), 34 (DZ 2), 44 (DZ 3)

MR-2645

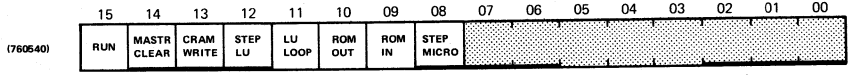
TDR – Transmit Data Register



NOTE: XX = 16 (DZ 0), 26 (DZ 1), 36 (DZ 2), 46 (DZ 3)

MR-2647

KMC – BSEL 1 – Maintenance Register



MR-2640

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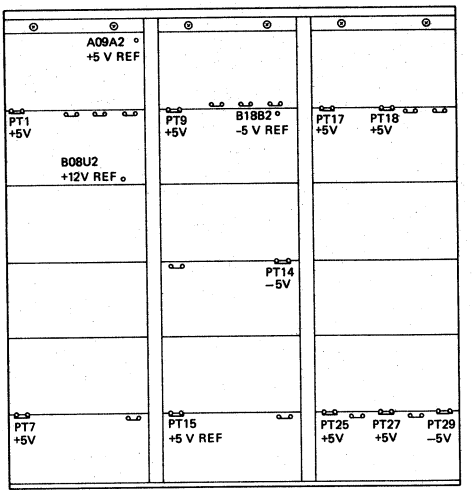
UNIBUS ADAPTER MINI CHECK

If you are having problems booting from either your disk or magtape, try this Unibus wraparound test.

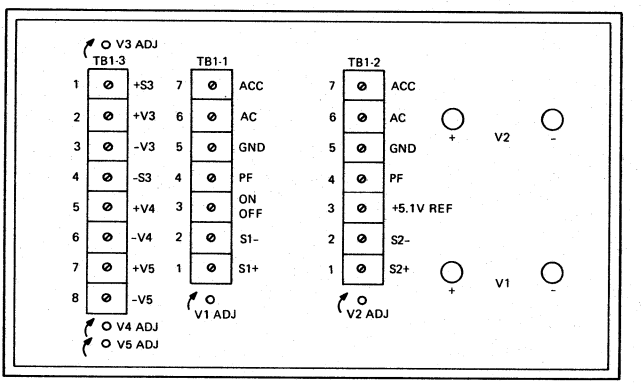
```
     EI UBA#,763000              ;ADDRESS OF PAGING RAM FOR LOCATION
                                  ZERO
     DI 40000 (18 BIT VALID),140000 (36 BIT,VALID),240000
                               (16 BIT,VALID)
     EI UBA#,763101              ;ADDRESS OF UBA MAINTENANCE REGISTER
     DI 1                        ;BIT 35 FOR WRAP AROUND
     EI UBA#,ADR                 ;LOAD MEMORY ADDRESS TO BE WRITTEN
            ;LOW ORDER UNIBUS ADDRESS BITS ARE DISCARDED
            ;C00 SAYS 8 BIT UNIBUS BYTE MODE OR NOT
            ;C01 SAYS RIGHT HALF OR LEFT HALF

                                  3,,0=LH MEMORY LOCATION 0
                                  3,,2=RH MEMORY LOCATION 0
                                  3,,4=LH MEMORY LOCATION 1
                                  3,,6=RH MEMORY LOCATION 1
DI XXXXXX(DATA PATTERN)           ;DATA WILL LOOP THROUGH UBA TO
                                  MEMORY LOCATION
EM MEMORY LOCATION                ;CHECK TO SEE IF IT GOT THERE


EXAMPLE 1:   EI 1763000
             DI 140000
             EI 1763101
             DI 1
             EI 1000100
             EI 555333
             EI 1000102
             DI 121212
             EM 20
     CORRECT DATA SHOULD BE   000000,,000020/555333,,121212


EXAMPLE 2:   EI 1763000
             DI 40000
             EI 1763101
             DI 1
             EI 1000100
             DI 777777
             EM 20
     CORRECT DATA SHOULD BE   000000,,000020/777777,,000020

EXAMPLE 3:   EI 1763000
             DI 240000
             EI 1763101
             DI 1
             EI 1000100
             DI 743216
             EM 20
     CORRECT DATA SHOULD BE   000000,,000020/143216,,000020
```



PIN	REFERENCE	ADJUSTMENT	
A09A2	+5 V REF	ADJ V1	ADJUSTMENTS MADE
B08U2	+12 V REF	ADJ V3	ON LH POWER SUPPLY
B18B2	-5 V REF	ADJ V5	
PT 15	+5 V REF	ADJ V2	

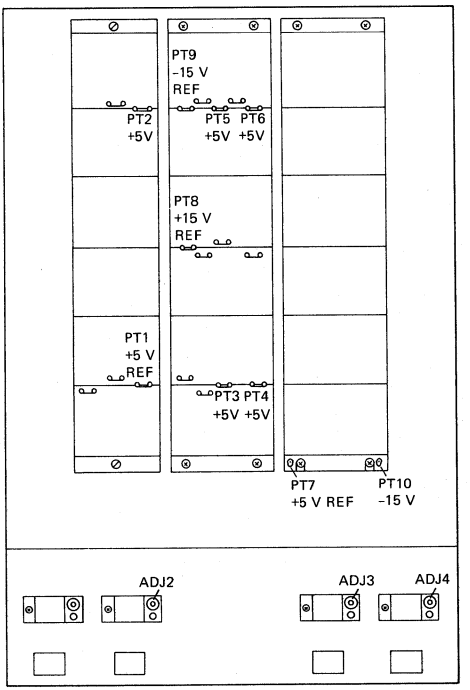
KS10 BACKPLANE

MR-2708



H7130 POWER SUPPLY

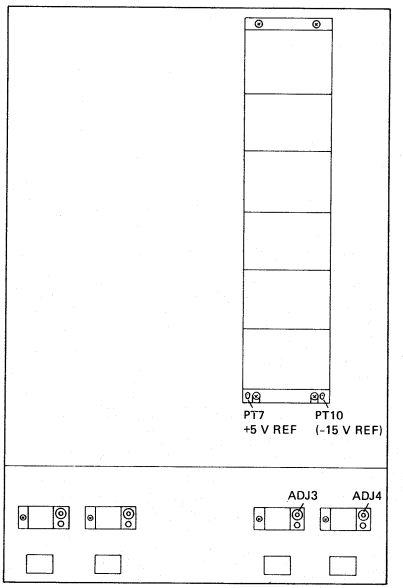
MR-1916



PIN	REFERENCE	ADJUSTMENT
PT1	+5 V REF	ADJ2
PT7	+5 V REF	ADJ3
PT8	+15 V REF	NO ADJ
PT9	-15 V REF	ADJ4

BA11-K BACKPLANE

MR-2707



PIN	REFERENCE	ADJUSTMENT
PT7	+5 V REF	ADJ3
PT10	-15 V REF	ADJ4

MR-3115

BA11-K Power Tab and Adjustment Locations
(DNHXX Cabinet)

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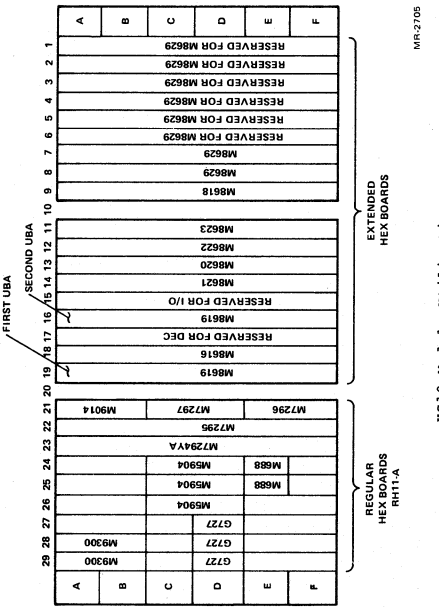
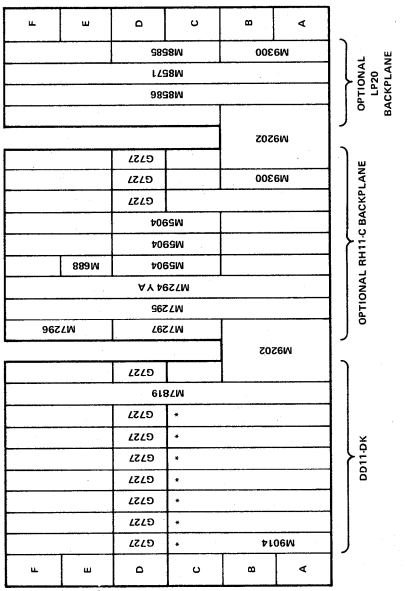

KS10 Module Utilization
MR-2705
EXTENDED HEX BOARDS
REGULAR HEX BOARDS RH11-A
FIRST UBA
SECOND UBA
A B C D E F
1 RESERVED FOR M8629
2 RESERVED FOR M8629
3 RESERVED FOR M8629
4 RESERVED FOR M8629
5 RESERVED FOR M8629
6 RESERVED FOR M8629
7 M8629
8 M8629
9 M8618
10
11 M8623
12 M8622
13 M8620
14 M8621
15 RESERVED FOR I/O
16 M8619
17 RESERVED FOR DEC
18 M8616
19 M8619
20
21 M9014 M7297 M7296
22 M7295
23 M7294YA
24 M5904 M688
25 M5904 M688
26 M5904
27 G727
28 M9300 G727
29 M9300 G727
A B C D E F



OPTION VARIATIONS*

SLOTS	ASYNC LINES 8–15	ASYNC LINES 16–23	ASYNC LINES 24–32
2			
3			
4			
5			M7819 DZ11
6		M7819 DZ11	
7	M7819 DZ11		
8	M7819 STD		

SLOTS	1ST SYNC	2ND SYNC
2	M8204 KMC11	
3		M7867 DUP11
4	M7867 DUP11	
5		
6		
7		
8		

MR-2706

BA11-K Module Utilization (Module Side)

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NOTES

STANDARD BOOT PROCEDURE
The KS10 is automatically booted 30 seconds after power-up. Booting may also be accomplished by the console BT command.

PRE-BOOT Error Messages
PRE-BOOT is loaded from disk or magtape (see 8080 commands DS, MS, BT, BT1, MT, MT1).

PRE-BOOT is written onto the disk using "SMFILE.EXE". It also is written on "standard" diagnostic tapes and onto the "Monitor Distribution" tapes.

PRE-BOOT is loaded by the 8080 into memory locations 1000 and up, and starts at 1000. The ERROR halts are:

1001 Found "bad" core-transfer address (page 1 is illegal -- can't overload PRE-BOOT)

1002 Disk retry error or magtape read error

1003 No RH11 base address

1004 Magtape skip failure

At ERROR halt time the following memory locations contain the following information.

Location	Disk Booting	Magtape Booting
100	8080 disk address	Not used
101	Memory transfer address	same
102	T3, selection pickup pointer	same
103	RPCS1-register	MTCS1-register
104	RPCS2-register	MTCS2-register
105	RPDS - register	MTDS -- register
106	RPER1-register	MTER1-register
107	RPER2-register (RP06 only)	Not used
110	RPER3-register	Not used
111	UBA Page RAM loc 0	same
112	UBA-status register	same
113	Version Nr of PRE-BOOT	same

NOTE
The 8080 disk address is in the form "CY SA TA".

DIAGNOSTIC PROGRAM HIERARCHIES
The following tables describe the 10-Based 10 Maintenance Library diagnostic hierarchies.

Table 1 KS10 Maintenance Library Utility Programs

Table 2 KS10 Processor Diagnostic Hierarchy

Table 3 KS10 Memory Diagnostic Hierarchy

Table 4 Disk Subsystems Diagnostic Hierarchy

Table 5 Magtape Subsystems Diagnostic Hierarchy

Table 6 Hardcopy Equipment Diagnostics

Table 7 Communications Equipment Diagnostics

Table 8 Unibus Adapter Diagnostic

Table 9 Miscellaneous Diagnostic

MODE:

E indicates that the program may be run in Executive mode.

U indicates that the program may be run in the User mode.

Table 1 KS10 Maintenance Library Utility Programs

Utility	Mode	Title
SMAPT.SAV	E	Special Program
SMBC2.SAV	E U	KS10 Boot Check 2
SMDDT.SAV	E U	KS10 DDT
SMFILE.EXE	U	Special Program
SMMAG.SAV	E U	KS10 Magtape Monitor
SMMON.SAV	E U	KS10 Diagnostic Monitor
		SMCPU Processor Diagnostics Run File
		SMFLT Processor Diagnostics Run File (FLT)
		SMUSR Processor Diagnostics Run File (TS)
SMTAPE.SAV		Magtape Creator
SUBSM.SAV	E	KS10 Executive Subroutine Program
SUBUSR.SAV	U	KS10 User Subroutine Program

Table 2 KS10 Processor Diagnostic Hierarchy

Diagnostic	Mode	Title
Basic, Advanced, and Reliability		
DSKAA.SAV	E U	Basic Instruction Diagnostic 1
DSKAB.SAV	E U	Basic Instruction Diagnostic 2
DSKAC.SAV	E U	Basic Instruction Diagnostic 3
DSKAD.SAV	E U	Basic Instruction Diagnostic 4
DSKAE.SAV	E U	Basic Instruction Diagnostic 5
DSKAF.SAV	E U	Basic Instruction Diagnostic 6
DSKAG.SAV	E U	Basic Instruction Diagnostic 7
DSKAH.SAV	E	Basic Instruction Diagnostic 8
DSKAI.SAV	E U	Basic Instruction Diagnostic 9
DSKAJ.SAV	E U	Basic Instruction Diagnostic 10
DSKAK.SAV	E U	Basic Instruction Diagnostic 11
DSKAL.SAV	E U	Basic Instruction Diagnostic 12
DSKAM.SAV	E U	Basic Instruction Diagnostic 13
DSKBA.SAV	E U	Basic Instruction Reliability 1
DSKCA.SAV	E U	Advanced Instruction Diagnostic 1
DSKCB.SAV	E U	Advanced Instruction Diagnostic 2
DSKCC.SAV	E U	Advanced Instruction Diagnostic 3
DSKCD.SAV	E U	Advanced Instruction Diagnostic 4
DSKCE.SAV	E U	Advanced Instruction Diagnostic 5
DSKCF.SAV	E U	Advanced Instruction Diagnostic 6
DSKCG.SAV	E U	Advanced Instruction Diagnostic 7
DSKDA.SAV	E U	Arithmetic Reliability
Paging And Cache Tests		
DSKEA.SAV	E	Paging Diagnostic
DSKEB.SAV	E	Cache Diagnostic
Supplementary Tests		
DSKFA.SAV	E	Instruction Timing Diagnostic

Table 3 KS10 Memory Diagnostic Hierarchy

Diagnostic	Mode	Title
DSMMA.SAV	E	Memory Diagnostic
DSMMD.SAV	E U	Memory Diagnostic
Supplementary Tests		
DSMMB.SAV	E U	BLT/FLT I/O Memory Diagnostic
DSMMC.SAV	E U	FAST AC Diagnostic

Table 4 Disk Subsystems Diagnostic Hierarchy

Diagnostic	Mode	Title
DSRMA.SAV	E	RM03 Basic Diagnostic
DSRMB.SAV	E U	RM03/RP06 Reliability
DSRPA.SAV	E	RP06 Basic Diagnostic

Table 5 Magtape Subsystems Diagnostic Hierarchy

Diagnostic	Mode	Title
DSTUA.SAV	E U	RH11 TM03/TU45 Basic Diagnostic
DSTUB.SAV	E U	Magtape Reliability

Table 6 Hardcopy Equipment Diagnostics

Diagnostic	Mode	Title
DSCDA.SAV	E U	Card Reader Diagnostic
DSLPA.SAV	E U	Line Printer Diagnostic
DSLTA.SAV	E U	Teletype Diagnostic

Table 7 Communications Equipment Diagnostics

Diagnostic	Mode	Title
DSDUA.SAV	E	DUP-11 Diagnostic
DSDZA.SAV	E	DZ-11 Diagnostic
DSKMA.SAV	E	KMC-11 Diagnostic

Table 8 Unibus Adapter Diagnostic

Diagnostic	Mode	Title
DSUBA.SAV	E	Unibus Adapter Diagnostic

Table 9 Miscellaneous Diagnostic

Diagnostic	Mode	Title
DSRHH.SAV	E	RH11 TB Diagnostic (manufacturing)

GENERAL INFORMATION

CODE: KNS10
TITLE: CONSOLE PROGRAM
ABSTRACT: Console program resides in the 8080 PROMs and supports the KS10 based system. The console operates in either of two modes.

1. User Mode - The CTY is a user terminal and commands are passed to and from the KS10 CPU under control of the console program.

2. Console Mode - Commands are directed to (and executed by) the 8080 console hardware. The console program initialized the CTY-to-console mode at power-up.

NOTE: NONE

LOADING AND STARTING PROCEDURE: KS10 is automatically booted 30 seconds after power-up.

OPERATIONAL CONTROL
The KS10 is directed by the commands listed in Table 2.

Table 1 lists standard console messages.

ERROR MESSAGE SUMMARY
Table 3 lists the standard console error messages.

Table 1 Standard Console Messages

Message	Meaning
BT AUTO	Beginning automatic boot procedure after power-up.
BT SW	Beginning boot procedure as a result of BOOT switch being pressed (LOCK switch in UNLOCK position).
BUS 0-35	Message header for EB command.
CYC	Cycle type for DB command.
ENABLED	Entering CTY mode from user mode. (CTY mode is entered as a result of a "control-\" in user mode with LOCK switch in UNLOCK position.)
HLTD	Halt in KS10 processor program execution.
KS10>	Command prompt.
OFF	Current state is off. (Response to CE, TE, TP, and KL commands when current state of enable is requested and it is a 0.)
ON	Current state is on. (Response to CE, TE, TP, and KL commands when current state of enable is requested and it is a 1.)
RCVD	Data received from bus. (Indicates bus data received if failure occurred during EB command.)
SENT	Data sent to bus. (Indicates bus data transmitted if failure detected during DB command.)
USR MOD	Entering user mode. (User mode is entered as a result of a "control-Z" or the successful completion of a CO, ST, BT, or MT command.)
>>UBA?	Query for UBA number.
>>UNIT?	Query for unit number.
>>TCU	Query for tape controller unit number.
>>RHBASE?	Query for RH11 base register address.
>>DENS?	Query for tape density.
>>SLV?	Query for tape slave number.

Table 2 Console Commands

Command	Description	Notes
Special Control Characters		
^\	Enter console mode.	NA
^\\	Used in conjunction with the KL1 command for KLINIK mode.	NA
^U	Rub out current line.	NA
^O	Switch: first one stops CTY output, second one resumes CTY output.	NA
^S	Stop TTY output and 8080 waits for control Q.	NA
^Q	Resumes TTY output.	NA
^C	Stop the 8080.	NA
^Z	Enter User mode.	NA
RUB-OUT	Rub out previous character typed.	NA
Load Commands		
LAxx	LAxx <CR> - Set KS10 memory address xx (0000000-1777777).	NA
LCxx	LCxx <CR> - Set CRAM address xx (0000-3777).	NA
LFxx	LFxx <CR> - Load diagnostic write function xx (0-7). The function specifies a 12-bit group within a CRAM address. LF CRAM LF CRAM 0 00-11 4 48-59 1 12-23 5 60-71 2 24-35 6 72-83 3 36-47 7 84-95	NA
LIxx	LIxx <CR> - Set I/O address xx	1
LKxx	LKxx <CR> - Set 8080 memory address xx (PROM address = 00000-17777; RAM address = 20000-21777).	NA
Deposit Commands		
DBxx	DBxx <CR> - Deposit xx (36 bits) onto KS10 bus.	NA
DCxx	DCxx <CR> - Deposit xx (96 bits) into CRAM. Address previously loaded by LC command.	NA
DFxx	DFxx <CR> - Deposit xx (12-bit group) into CRAM Address and diagnostic function previously loaded by LC and LF commands.	NA
DIxx	DIxx <CR> - Deposit xx (16, 18 or 36 bits) into an I/O register. Address previously loaded by LI command.	NA
DKxx	DKxx <CR> - Deposit xx (8 bits) into 8080 memory. Address previously loaded by LK command (Data cannot be deposited in PROM addresses; only in RAM addresses).	NA
DMxx	DMxx <CR> - Deposit xx (36 bits) into KS10 memory. Address previously loaded by LA command or EM.	NA
DNxx	DNxx <CR> - Deposit xx into next (KS10, 8080, I/O, CRAM) address.	NA

Table 2 Console Commands (Cont)

Command	Description	Notes
Examine Commands		
EB	EB <CR> - Examine KS10 Bus. Prints contents of console registers 100-103 and 300-303.	NA
EC	EC <CR> - Examine contents of CRAM control register.	NA
ECxx	ECxx <CR> - Examine contents of CRAM address xx.	NA
EI	EI <CR> - Examine contents of I/O register. Address previously loaded by LI command.	NA
EIxx	EIxx <CR> - Examine contents of I/O address xx.	NA
EJ	EJ <CR> - Examine current CRAM address, next CRAM address, jump address, and subroutine return address.	NA
EK	EK <CR> - Examine contents of 8080 memory. Address previously loaded by LK command.	
EKxx	EKxx <CR> - Examine contents of 8080 memory address xx.	NA
EM	EM <CR> - Examine contents of KS10 memory. Address previously loaded by LA command.	NA
EMxx	EMxx <CR> - Examine contents of KS10 memory address xx.	
EN	EN <CR> - Examine contents of next (KS10, 8080, I/O, CRAM) address.	
Start/Stop Clock		
CH	CH <CR> - Halt CPU clock.	NA
CP	CP <CR> - Pulse CPU clock.	NA
CPxx	CPxx <CR> - Pulse CPU clock xx times.	NA
CS	CS <CR> - Start CPU clock.	NA
Start/Stop Microcode		
PM	PM <CR> - Pulse microcode. Performs a CP command to execute a microinstruction followed by an EJ command to print current CRAM address, next CRAM address, jump address, and subroutine return address.	NA
SM	SM <CR> - Reset and start microcode at CRAM address 0.	NA
SMxx	SMxx <CR> - Reset and start microcode at CRAM address xx.	NA
TR	TR <CR> - Trace. Repeats PM command until any CTY key is depressed.	NA
TRxx	TRxx <CR> - Trace. Repeats PM command until CRAM address xx is reached or until and CTY key is depressed.	NA

Table 2 Console Commands (Cont)

Command	Description	Notes
Start/Stop Program		
HA	HA <CR> - Halt KS10 program. Microcode enters halt loop.	NA
CO	CO <CR> - Continue KS10 program execution. Console program enters user mode.	NA
SH	SH <CR> - Shut down command. Deposits nonzero data into KS10 memory location 30 to allow orderly shut down of the monitor.	NA
SI	SI <CR> - Single instruct. Executes next KS10 instruction.	NA
STxx	STxx <CR> - Start KS10 program at address xx. Console program enters user mode.	NA
Select Device		
DS	DS <CR> - Select disk for bootstrap or microcode verification. Console program asks for UBA number (default = 1), RH11 base address (default = 776700), and disk unit number (default = 0).	2
MS	MS <CR> - Select tape for bootstrap or for microcode verification. Console program asks for UBA number (default = 3), RH11 base address (default = 772440), tape controller unit number (default = 0), tape density (default = 1600 BPI), and slave number (default = 0).	3
Boot Commands		
BC	BC <CR> - Check the KS10 boot path.	NA
BT	BT <CR> - Bootstrap the KS10 from disk. Loads and starts microcode and monitor boot program from drive 0 on UBA 1 (default address) or drive selected by last DS command; starts KS10 at memory address 1000. The BT command is performed automatically 15 seconds after power-up. A "control C" aborts the automatic boot process.	NA
BT1	Same as BT command except that diagnostic boot program (not monitor boot program) is loaded and started.	
B2	B2 <CR> - Bootcheck 2. This loads in a separate PRE-BOOT which loads in the Bootcheck 2.	NA
LB	LB <CR> - Load the monitor boot program from disk selected last. Does not load microcode. Program must be started at 1000.	NA
LB1	Same as LB command except that diagnostic boot program (not monitor boot program) is loaded. Program must be started at 1000.	
MB	MB <CR> - Load the monitor boot program from the tape selected last. Does not load microcode. Program must be started at 1000.	NA
MT	MT <CR> - Bootstrap the KS10 from tape. Loads and starts microcode and monitor boot program from tape unit 0, slave unit 0 on UBA 3 (default address) or drive selected by last MS command; starts KS10 at memory address 1000.	NA

Table 2 Console Commands (Cont)

Command	Description	Notes
Verify Microcode		
VD	VD <CR> - Verify CRAM against disk. Compares microcode in CRAM with microcode found on disk unit 0 on UBA 1 (default address) or disk selected by last DS command.	NA
VT	VT <CR> - Verify CRAM against tape. Compares microcode in CRAM with microcode found on tape unit 0, slave unit 0 on UBA 3 (default address) or tape selected by last MS command.	NA
Mark/Unmark Microcode		
MKxx	MKxx <CR> - Mark microcode word (set bit 95) at CRAM address xx.	NA
UMxx	UMxx <CR> - Unmark microcode word (clear bit 95) at CRAM address XX.	NA
Master Reset		
MR	MR <CR> - Master reset. Issue bus reset.	NA
Execute Command		
EXxx	EXxx <CR> - Execute the single KS10 systems - level instruction xx.	NA
Enable/Disable		
CExx	CExx <CR> - Enable (xx = 1) or disable (xx = 0) cache.	NA
PExx	PExx <CR> - Enable or disable parity detection as follows. xx 0 Disable all parity detection 4 Enable KS10 bus parity detection 5 Enable DPE/DPM parity detection 6 Enable CRA/CRM parity detection 7 Enable all parity detection	NA
TExx	TExx <CR> - Enable (xx = 1) or disable (xx = 0) CPU interval timer interrupts.	NA
TPxx	TPxx <CR> - Enable (xx = 1) or disable (xx = 0) CPU traps. Following an enable/disable command with a carriage return gives the current value.	NA
SCxx	SCxx <CR> - Enable (xx = 1) or disable (xx = 0) automatic recovery from soft CRAM parity errors.	NA
Read Cram		
RC	RC <CR> - Read CRAM data. Performs diagnostic read functions 0-17 to read CRAM addresses and contents (of current address) as follows. 0 CRAM bits 00-11 1 Next CRAM address 2 CRAM subroutine return address 3 Current CRAM address 4 CRAM bits 12-23 5 CRAM bits 24-35 (Copy A) 6 CRAM bits 24-35 (Copy B) 7 0's 10 Parity bits A-F 11 KS10 Bus bits 24-35 12 CRAM bits 36-47 (Copy A) 13 CRAM bits 36-47 (Copy B) 14 CRAM bits 48-59 15 CRAM bits 60-71 16 CRAM bits 72-3 17 CRAM bits 84-95	NA

Table 2 Console Commands (Cont)

Command	Description	Notes
Zero Memory		
ZM	ZM <CR> - Zero memory. Deposit 0's into all KS10 memory locations.	NA
Repeat Command		
RP	RP <CR> - Repeat last command, or last command string, until any CTY key is depressed.	NA
RPxx	RPxx <CR> - Repeat last command, or last command string, xx times.	NA
Lamp Test		
LT	LT <CR> - Lamp test. Momentarily lights (1-2 seconds) and turns off (1-2 seconds) STATE, FAULT, and REMOTE indicators. The indicators are then returned to their original state.	NA
Password Command		
PWxx	PWxx <CR> - Set password xx (xx = maximum of 6 alphanumeric characters). Following a PW command with a carriage return clears the password storage area.	NA
Klinik Command		
KLxx	KLxx <CR> - Enable remote link with access to system to operate in mode 2 but not in mode 3 (xx = 0). Enable remote link with access to system to operate in mode 2 or in mode 3 (xx = 1). Following a KL command with a carriage return gives the current value.	NA
TT	TT <CR> - Force REMOTE DIAGNOSIS line from mode 3 to mode 2.	NA
8080 Register Commands		
LR	LR <CR> - Command to set into the 8080 RAM, the I/O register, to be either deposited or examined.	NA
DR	DR <CR> - Command to deposit a number into the last specified 8080 I/O register.	NA
ER	ER <CR> - Command to examine one of the 8080 internal registers and display the contents of that register.	NA

NOTES

1. LIxx - The address consists of a control number and a register address. If the console attempts to access its own register, no response occurs.

CTL	Register Address	Register
0	100000	Memory status register
1, 3	763000-77	UBA paging RAM
1, 3	763100	UBA status register
1, 3	763101	UBA maintenance register
1, 3	7XXXXX	Unibus device register

2. DS - The default value for the RH11 base address is currently the only value permitted. Also, a carriage return in response to any question retains the current value.

```
>>UBA? 1 <CR>
>>RHBASE?, 776700 <CR>
>>UNIT? 0 <CR>
```

3. MS - The default value for the RH11 base address is currently the only value permitted. Also, a carriage return in response to any question retains the current value.

```
>>UBA? 3 <CR>
>>RHBASE? 772440 <CR>
>>TCU? 0 <CR>
>>DENS? 1600 <CR>
>>SLV? 0 <CR>
```

Table 3 Console Error Messages

Message	Meaning
?A/B	A not equal to B. (A and B copies of a microcode field did not match.)
?BC xx	BC command failed. BOOTCHECK error messages are of the form: "?BC WWYYYY"
	WW=10 Indicates a failure during the CRAM check portion of BOOTCHECK. YYYY will be failing CRAM address.
	WW=04 Indicates a failure during the memory check. BOOTCHECK is trying to verify page 1 of MOS memory, and tests address 1000-1777 for ability to hold all ones, all zeroes, and to sequence through that page of memory correctly. YYYY will be the failing memory address.
	WW=00 Indicates a failure during the KS10 bus check. BOOTCHECK is floating a one, then a zero across the KS10 bus.
	YYYY These are the failing bits in octal. Numbers will range from 0 to 43, which corresponds to decimal 0-35.
?BFO	Buffer overflow. (Too many characters typed; console's 80 character input buffer is full.)
?BN	Bad number. (Character typed is not an octal number.)
?BT xx	BT command failed. 8080 error messages of the type "?BT XXXYYY". These messages can occur anytime the 8080 is trying to access either a disk or tape.
	A message of the form "?BT XXXYYY" should be interpreted as follows:
	XXX=001 Means for disk that an error was encountered while trying to read the home blocks. Just about anything can cause this error, including no disk pack in the drive, wrong unit selected, incorrect RH base specified, wrong UBA selected, or bad disk drive. This message also occurs if both the home block and alternate home blocks can be read, but neither has the home block ID ("HOM" in six bit).
	Means for tape that an error was encountered while trying to read the first page of microcode from the magtape. Anything could be wrong in the CP11 to magtape path, including wrong unit selected, wrong RH base address, wrong UBA, wrong slave, wrong density, bad tape drive, bad TM02, bad magnetic tape, or tape in the wrong format.
	This error can occur on any 8080 command or process that accesses disk or tape.
	XXX-002 Means that a disk error was encountered while trying to read the page of pointers which makes up the 8080 file system. If you get this far, the home blocks may have been read successfully. The problem could be a pack that is not in the format required for 8080 loading, the home blocks are bombed, or bad disk drive or pack.
	This error can occur on any 8080 command or process that accesses disk or tape.

Table 3 Console Error Messages (Cont)

Message	Meaning
	XXX=003 Means that a disk error was encountered while trying to read a page of the microcode. If you get this far, the problem could be a pack not in 8080 format, or bad disk drive or pack. This error can occur on PWR FAIL recovery, SCE soft CRAM error recovery, VD, BT, or MT commands.
	XXX-004 Means that the microcode did not successfully start running after a BT, MT, MB, or LB command. This error will always occur when you do an LB, before the system microcode is loaded.
	XXX=010 Means that an error was encountered while trying to read in the PRE-BOOT program. Problems could be the same as 003 above. If accessing the tape, failure could have occurred while doing a skip over the microcode file, or in the reading of the PRE-BOOT program itself. Tape could be in the wrong format. This error can occur on LB, MB, or FORCED RELOAD.
	YYY Indicates the lower 8 bits of the 8080 address of the failing "Channel Command List" operation. Do not waste your time looking in the listing, unless you are positive that the RH11 or disk drive is bad. Instead, type EI on the CTY. It will print out the contents of the RH11 register that has the error bits set. That will give you more information than an 8080 listing. If you do find your way through the 8080 listing, you will do an EI anyway, so do the EI first.
?BUS	Bad KS10 bus. (All bus lines not zero after power-up or reset.)
?CCYC	Command/address cycle failed. (KS10 bus data failure detected during DB command; good and bad data printed.)
?CHK xx	PROM checksum error. (Bad checksum for PROM chip xx where xx = 1, 2, 3, or 4.)
?DCYC	Data cycle failed. (KS10 bus data failure detected during DB command; good and bad data printed.)
?DNC	Did not complete. (HA or SM command did not cause microcode to enter halt loop.)
?DNF	Did not finish. (ST, CO, or EX command did not complete.)
?FRC	Forced reload. (Monitor has requested reload; 8080 halts the KS10, reloads the PRE-BOOT program, and starts in KS10 memory location 1000.)

Table 3 Console Error Messages (Cont)

Message	Meaning
?IA	Illegal address. (Address typed is out of range.)
?IL	Illegal command. (Command typed is not valid.)
?IL	Incorrect password. (Password entered via KLINIK line does not match password entered at CTY.)
?KA	Keep-alive error. (During timesharing, the monitor failed to update the keep-alive count for a period of approximately 15 seconds.)
?MRE	Memory refresh error. (Incomplete KS10 MOS memory cycle. Error occurs when memory must be refreshed in hung state.)
?NA	Not available. (Console not enabled to receive KLINIK line input.)
?NBR	No bus response. (Console did not receive GRANT after requesting KS10 Bus.)
?NDA	No data acknowledge. (Console did not receive DATA CYCLE signal after a data request.)
?NR-SCE	Nonrecoverable soft CRAM error. This message is followed by the standard "?PAR ERR" message.
?NXM	Nonexistent memory. (Deposit or examine command referenced nonexistent KS10 MOS memory location.)
?PAR ERR xx	System parity error. (CPU clock stopped due to system parity; xx = contents of the following console status registers in the order indicated: 100, 303, 103
?PWL	Password length error. (Password longer than six alphanumeric characters.)
?RA	Requires argument. (Command typed requires an argument.)
?RUNNING	Clock running. (Command typed requires CPU clock to be stopped.)
?UI	Unknown interrupt. (Console received interrupt but CTY or KLINIK line has no character.)
%SCE XXXXXX	Soft CRAM error. XXXXXX represents the error address. 8080 is attempting to recover by reloading the CRAM and continuing the instruction that got the parity error.