THE LSI-11 - A SYSTEM MICROCOMPUTER

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Abstract

By combining N channel MOS technology for the Microprocessor and RAM memory combined with a PDP-11 instruction set and architecture, the LSI-11 was designed to be a system's Microcomputer. The machine has been microprogrammed to emulate the basic instruction set of the 11/35/40 including extended fixed and floating point instructions. The LSI-11 has also been microprogrammed to perform an ASCII communication dialogue with the operator, refresh all dynamic MOS memories in a system, and provide for microcode expansion. The LSI-11 opens a new dimension in Microcomputer cost/performance.

I. Introduction

This paper will present the design criteria for the LSI-11 system, describe its specifications and features, and demonstrate how the LSI-11 system can be used to solve a variety of Microprocessor and Minicomputer system application problems.

The LSI-11 was designed to satisfy a broad range of computing needs with a single product offering. To provide minicomputer performance at a microcomputer price, the LSI-11 was designed to optimize system costs rather than component costs.

The LSI-11 processor can be viewed as either a high performance multifeature microprocessor or a very low end minicomputer with large system capabilities. It has incorporated the advantages of the single BUS architecture and the instruction set of Digital Equipment Corporation's PDP-11 family of 16 bit computers, but is available at microcomputer prices.

The basic component of the LSI-11 system is a processor module containing a multichip microprogrammed microprocessor, 4K words of 16 bit RAM memory and a parallel asynchronous 16 bit BUS interface. The processor module is built on a 8 X 10 inch (21.6cm X 26.7cm) printed circuit board. [Fig. 1] The processor module executes the same instruction set as the PDP-11/40 without memory management instructions. An optional microprocessor chip is available to expand the instruction set of the processor to include fixed point muliply and divide instructions plus floating point instructions. The performance of the LSI-11 processor is close to that of the PDP-11/05, but the additional 11/40 instructions and the optional fixed and floating instruction set more than compensate for this difference.

II. The Micromachine

The design of the LSI-11 Processor gives the user all of the tools necessary to implement a cost effective system. These tools are usually not available with most "computer on a chip" systems. There were no "don't care" design decisions. Every circuit was evaluated as to its cost and utility. To this end, the first decision was the selection of a microprogrammed microprocessor for maximum design flexibility. For maximum performance and manufacurability, N channel silicon gate MOS technology was chosen.

The actual microprocessor, designed jointly with Western Digital Corporation, Newport Beach, California, includes many design features found only in larger, more complex computer systems. The nature of the multiphase MOS technology allowed pipelining of the micromachine and efficient communication between the three different devices in the Microprocessor set (Arithmetic Chip, Control Chip, Control Store). At any one time, while the Arithmetic Chip is

operating on microinstruction N, the Control Store is accessing Microinstruction N + 1, and the Control Chip is evaluating the address of microinstruction N + 2. The use of PLA's (programmable logic arrays) throughout the design for decoding microinstructions, macroinstructions, address and status bits increased device performance and reduced the silicon real estate necessary for each function.

Other micromachine features such as a 26 X 8 bit dual port register file, 8 or 16 bit micro-operations with a single microinstruction and an extremely efficient micro and macro branch capability all enhanced the efficiency of emulating the PDP-11/40 instruction set. Trading off PLA address translations for Control Store words further enhanced the performance of this target macromachine. Even the decision as to what macroinstruction performance to optimize was not randomly chosen. A dynamic mix analysis of the instructions most frequently used in PDP-11 software was done before the microcode was even written!

The instruction repertoire of the micromachine is a highly encoded, very efficient register transfer set. The actual microinstruction is only 16 bits wide (the microword is 22 bits). Because of highly encoded structure, the tasks of building software and hardware simulators for debugging and testing were greatly simplified. The structured nature of the micromachine and microcode simplified the incorporation in 1024 Control Store words, the complete 11/40 emulation routine, and the capability to expand the Macro level instruction set by the addition of more Control Store devices. Included with the emulation routines are a dynamic MOS memory refresh routine and a Real Time Clock routine. Also available are a user oriented ASCII console dialogue and bootstrap loader routines.

The micromachine in the LSI-11 is composed of four custom LSI devices (one Data Chip, one Control Chip, and two Microcode Read Only Memory (MICROM) chips). The following section describes each of the devices in greater detail. The micromachine has the capability of supporting up to four Microms, even though only two are used in the basic LSI-11 processor configuration. The micromachine configuration is shown in Fig. 2. Note that all of the devices communicate with each other over a common time shared BUS called the MIB (Microinstruction BUS).

Data Chip

The Data Chip contains 26 eight bit dual port registers and an eight bit Arithmetic Logic Unit (ALU) in its internal paths. A sixteen bit bidirectional TTL interface port is incorporated to allow communications between the micromachine and system memories and interfaces. The LSI-11 BUS is built upon this sixteen bit port referred to as the DAL (Data Address Lines) port. A second sixteen bit port, MIB interface, allows communication with the other microprocessor chips.

Of the 26 eight bit registers, 16 are used to realize the 8 PDP-11 sixteen bit registers R0 through R7 and the remaining 10 are used for temporary storage during microprogram execution. Eight status flags reflect the status of the previous ALU operation. Microinstruction jumps, conditioned on these status flags, can be executed for efficient microprogram flow. Four of these flags serve as the PDP-11 condition codes.

Control Chip

The Control Chip contains an 11 bit microcode location counter and all of the branching logic necessary to generate microaddresses for the MICROMS. This chip also generates the LSI-BUS control and interrupt signals that are used in Bus Data and Interrupt Transactions.

The major portion of the control chip is a Programmable Translation Array (PTA) used to generate a new microprogram address as a function of 1. the current contents of the microcode location counter, 2. the PDP-11 instruction in the Macro instruction register, 3. external interrupt conditions and 4. state registers which have been loaded from previous PTA translations. It is largely through this mapping structure that the efficient emulation of the PDP-11/40 instruction set has been accomplished. In one microcycle, multiway branches are used to decode the many different PDP-11 instructions and individual instruction modes. This same type of mapping unit will probably be used in the next generation of minicomputers, as bipolar Programmable Logic Arrays become available from the semiconductor manufacturers.

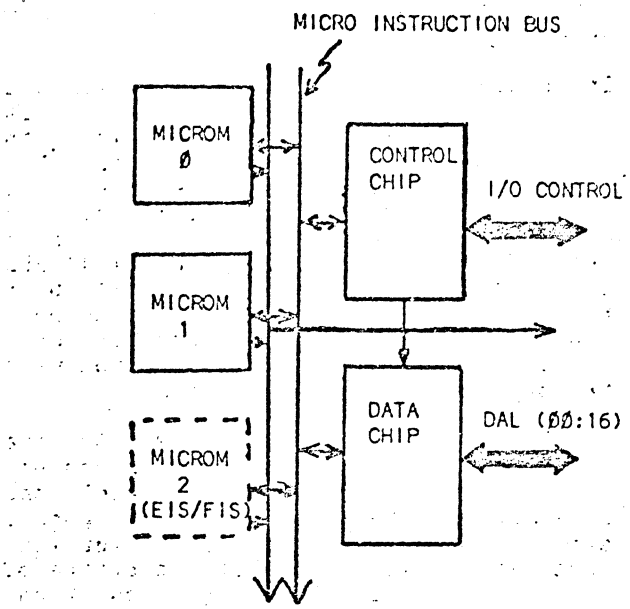


Figure 2. Microprocessor Configuration

MICROM Chip

The MICROM Chip is a 512 X 22 bit read only memory, with a built in interface to the MIB. Each MICROM device in the system contains its own address decode logic so that only one device responds to any address in the 2048 word address space. Of the twenty-two bit field, sixteen bits are dedicated to the microinstruction, two bits are used for direct Control Chip communication and four bits are encoded for explicit control of functions external to the Microprocessor.

The MICROM receives addresses on the MIB lines during one phase of the four phase cycle and, if selected, outputs data two phases later onto the MIB. MICROM data is read into both Control Chip and Data Chip to conserve time and reduce interchip communication.

III. The Processor Module

Most system designers find out that even with high performing Microprocessor chips, there are usually support circuits and interface circuits necessary to build a microprocessor system. A basic microprocessor set must be able to support a wide variety of memories or interface devices. A System BUS must be capable of reliable operation in a variety of configurations. The addition of a Bus must not degrade the microprocessor performance.

To realize the LSI-11 processor module, the microprocessor, a 4K X 16 dynamic MOS RAM memory and a sixteen bit TTL asynchronous interface were implemented on one printed circuit card (KD11F). Also on the printed circuit card is a four phase clock generator, MOS memory control and BUS arbitration logic. The design trade offs for the components on the processor module were made to lower systems implementation cost and retain maximum system flexibility.

The following sections describe the processor module from a system architectural view and the features that were included to make the system designer's task easier. Fig. 3 shows the Microprocessor with the other major portions of the Processor Module.

The DAL lines from the Data Chip are buffered with open collector bus drivers to form the major data path in the LSI-11 system BDAL (00:15). Sixteen bit address and data are time multiplexed on these bidirectional lines and are only valid while the appropriate BUS control signals are asserted. The sixteen bit address width allows direct access to 64K bytes (32K 16 bit words). Electrically the LSI-11 BUS is lightly terminated on the processor module with a 250 ohm Thevenin impedance.

The I/O control signals are similarly buffered from the Control Chip to provide the high drive open collector Bus Control and Synchronization signals. As indicated in figure 3, these lines are also received on the processor module to control data transfers to or from the local 4K MOS RAM.

The 4K X 16 bit MOS RAM is physically located on the processor module and functionally on the LSI-11 BUS. The memory is accessible by either the microprocessor or BUS devices which can initiate or control BUS transfers (DMA devices), with very little processor module overhead. A jumper wire on the processor module allows the local 4K RAM to respond to either the first or the second 4K address bank in the total 32K address space.

Logic on the processor module arbitrates between the microprocessor and DMA devices requesting use of the LSI-11 BUS. The Microprocessor is BUS master until the arbitration logic relinquishes control to a requesting DMA device.

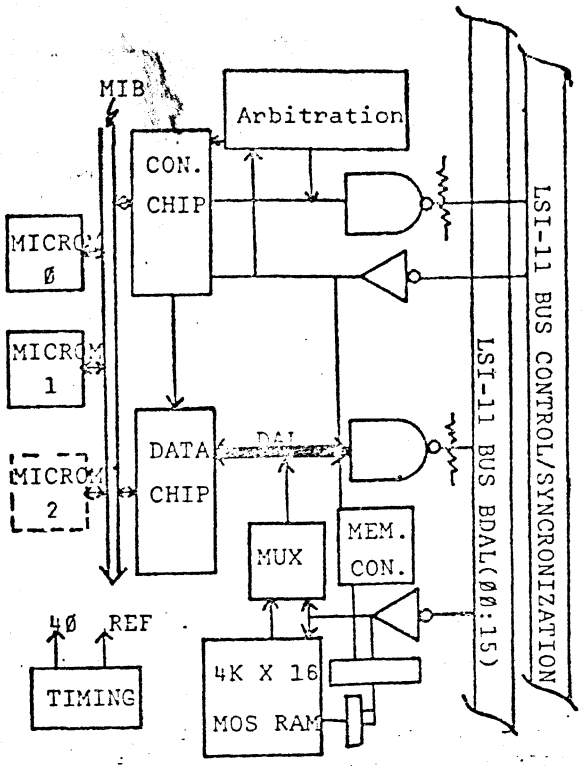


Figure 3. Processor Module Configuration

IV. LSI-11 BUS

In almost all computer systems the system interface BUS and its complexity is what adds most to system hardware cost. The BUS not only must specify to the user its functional and electrical characteristics but also the mechanical system configuration constraints. The items that must be considered cover the gamut from where the console is placed to how much a mass storage controller will cost to implement. Local optimization does not solve system problems.

The LSI-11 BUS is the medium for all system communication. This BUS consists of thirty three lines and utilizes the same drivers and receivers that are used in the PDP-11 Unibus. Data transactions are asynchronous and require a response from a selected device. The LSI-11 user need only interface to the BUS lines necessary to perform his job. (See Fig. for all bus signal names and functions).

The LSI-11 BUS signals can be grouped into four distinct transaction categories:

A. Data transactions use BDAL (00:15) for address and data information and six control signals which sequence the transaction. The six control signals indicate the start of a transaction (BSYNC), the type of transfer (BDIN or BDOUT), a word or byte transfer (BWTBT), a transfer to the upper 4K I/O space (BBS7) or the acceptance or availability of data by a device or memory (BRPLY).

B. Interrupts are accomplished through a request line (BIRQ) and a daisy chained grant line (BIAK) originating at the processor. DMA operations use a similar request line (BDMR) and daisy chained grant line (BDMG) plus an additional signal (BSACK) which marks the BUS as being in use. The daisy chained nature of the grant signals allow device priority to be determined by electrical distance from the processor.

C. The power control signals (BPOK and BDCOK) are generated by the power supply and initiate system Power Up and Power Down sequences in the LSI-11 processing system. The processor module will perform its described power up or power fail routines if these signals are properly sequenced. BINIT is generated by the processor to preset all system device registers to their value at Power Up.

Four jumper selectable power up options are provided on the processor module. These options allow the processor to power up as other PDP-11 processors by loading the Program Counter and PSW from locations 24 and 26, or directly to a user specified bootstrap or to the ASCII console dialogue. A fourth option is available to allow future power up user microroutines. For example, in a remote network application it may be desirable to have the LSI-11 power up to either a special communications bootstrap or to the ODT microcode.

D. Three system function lines (BHALT, BREF, and BEVNT) have been included in the LSI-11 BUS to facilitate the building of cost effective small systems. These BUS lines provide the user a direct communication path to the processor module.

BHALT

BHALT is a bus line that, when asserted, causes the microprocessor to cease emulation of the PDP-11 instruction set and enter a user oriented ASCII dialogue. Assertion of this line is exactly analogous to a user depressing the physical halt/run switch on most conventional processor consoles. The dialogue is a subset of ODT-11 (Octal Debugging Technique) and gives the user all of the functions previously performed by lights and switches on a programmers console, without the associated cost.

This ASCII dialogue can be performed with a parallel or serial communications device at up to 9600 baud from a local or remote site. This remote capability will enhance the network usage of LSI-11 systems. Down line loading and remote diagnostics have little cost impact to a basic LSI-11 system.

BREF

Dynamic MOS memory refresh can cost seven to ten chips in every memory unit. In the LSI-11 microcode there is a routine that can be used to refresh all dynamic MOS memories in a system. The feature can be disabled by a jumper on the processor module, if only non volatile memories are present in a system.

If enabled this routine is executed approximately once very 1.6 milliseconds. The routine performs a burst of 64 data input transactions on the Bus asserting BREF for each transaction. The microprocessor increments the address portion of BDAL (01:06) so that all rows in dynamic MOS memories are read. The BREF line overrides local bank selection circuits on each memory unit.

The refresh function is a BUS specification. In larger systems any other device on the BUS may perform this task, thereby relieving the processor of this responsibility.

BEVNT

A real time clock funtion is also implemented in the processor microcode. Assertion of the BEVNT line will cause a processor interrupt to vector location 100 octal. This interrupt feature is compatible with the PDP-11 KW11L real time clock interface module. Connection of a sixty cycle source or other timing signal, available on most power supplies, through a bus driver, completes the total function.

V. Other Options and Configurations

Along with a flexible Bus for interconnecting the procesor module with other system devices, additional memories and peripheral interface modules are available to make the system designer's task easier. All available options utilize the LSI-11 Bus and can communicate over this medium. All of these will shorten system design time.

Memories

Four memory options are available to accommodate varying System requirements:

Add-on RAM is available in either 1K X 16 or 4K X 16 units. The 1K X 16 unit (MSV-11A) using static semiconductor devices is available on a 8.5 X 5 inch printed circuit card. 4K X 16 bit RAM memory can be either dynamic MOS (MSV-11B) on an 8.5 X 5 inch printed circuit card or if non volatility is required, a 4K X 16 bit (MMV-11A) core option is available.

Frequently accessed routines, table or special bootstrap routines can be programmed into bipolar semiconductor PROMS or ROMS in a 4K X 16 PROM module (MRV-11). This PROM module,available with 32 16 pin sockets, can accept either 256 X 4 or 512 X 4 devices up to 2K X 16 bits or 4K X 16 bits on an 8.5 X 5 inch card.

Note that all of these memory options have address decode circuitry and can be logically placed anywhere within the 32K address space of the LSI-11. Since the LSI-11 BUS is asynchronous all of these memories operate at their maximum speed.

Peripheral Interface Options

Several standard interface modules are available for either system prototyping or production use. A serial line interface (DLV-11), built on an 8.5 X 5 inch card, performs asynchronous serial data communication at crystal controlled speeds of 50 to 9600 baud. It can communicate with either 20ma or EIA devices.

A sixteen bit buffered parallel Input/Output interface (DRV-11) can be used in any application that requires stable TTL outputs or has TTL type levels that need to be input to the processor.

These basic interface tools will be joined by mass storage interfaces, special communication interfaces and other systems devices in the very near future. All option modules that make up the LSI-11 system are BUS compatible.

System Design Aids

The system designer also requires mechanical connectors and brackets to build his system or else he will have to adapt his system to the product he purchases. An etched backplane connector assembly (H9270) can be used to interconnect LSI-11 modules. This backplane assembly provides the mechanical and electrical environment for the LSI-11 BUS and provides a simple mechanical structure that can be mounted in the user's environment. Peripheral and interfacing cables are also available for the user who needs them.

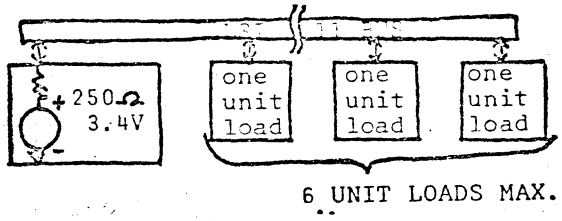
For the system designer who requires a package processing system, the LSI-11 is available in a 3-1/2 inch rack mounted enclosure with power supply (PDP-11/03). In this case only a 110V AC outlet and terminal device is necessary for system operation.

Configuration Flexibility

A simple building block approach was taken to allow the user to configure LSI-11 systems. The LSI-11 processor module contains an equivalent of 250 ohm termination on its BUS drivers. In most small configurations this is adequate for reliable system operation. The processor with 6 memory or interface options will not need additional BUS termination.

Larger systems with more devices will require end termination and/or interconnecting cables. A typical or large system may require 16K to 28K of memory and many interface devices. All of these system configurations are possible in an LSI-11 system by choosing the proper cables and end termination as required. Fig. 5 shows an example of a typical small and large system configurations.

SMALL CONFIGURATION



LARGE CONFIGURATION

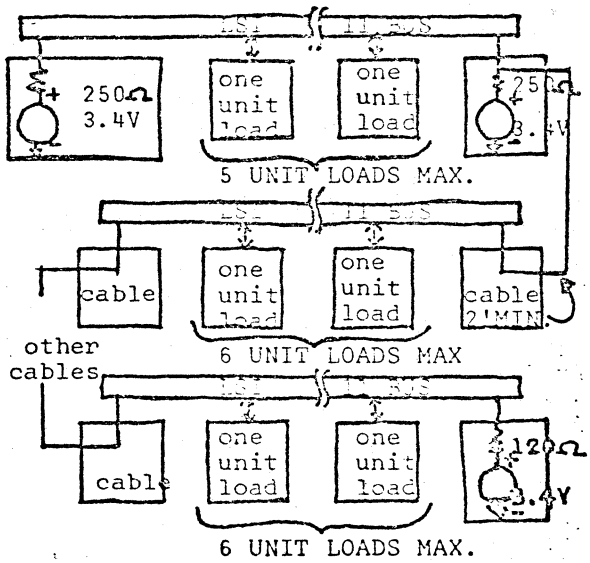


Figure 5. Small and Large BUS Configurations

VI. Summary

The LSI-11 is the newest member of the PDP-11 family. Its software as well as its peripherals are compatible with larger, higher performing PDP-11 systems. Software developed on other PDP-11 systems is directly transportable to the LSI-11. Its features and its small size will make networks and distributed small local processing a cost effective system solution.

The LSI-11 should open up a new class of solutions to problems that previously required the computational power and performance only available in higher priced minicomputers. The LSI-11 also offers the potential microprocessor user a true microcomputer system on a single printed circuit card, with the full range of PDP-11 development and application software.

Bus Signal		Signal Function
BDAL 00:15	L	Buffered Data/Address Lines (time-multiplexed).
BDIN	L	Data input transfer control line.
BDOUT	L	Data output transfer control line.
BSYNC	L	Synchronizing control signal; asserted by bus master (normally CPU).
BRPLY	L	Reply control signal; returned by bus slave (memory or peripheral device).
BWTBT	L	Write/Byte control: at address time, specifies a write; at data time, a byte output.
BBS7	L	Marks an address in the range 28-32K, the "I/O page".
BREF	L	Signals a refresh transaction; overrides normal memory addressing for dynamic memories.
BIRQ	L	Interrupt request from device.
BIAK I	L	Interrupt grant in.
BIAK O	L	Interrupt grant out; used with BIAK I to arbitrate interrupt priority.
BDMR	L	Direct Memory Access (DMA) request line.
BDMG I	L	DMA grant in.
BDMG O	L	DMA grant out; like BIAK.
BSACK	L	Bus DMA acknowledge.
BHALT	L	Forces entry to ASCII console microcode.
BEVNT	L	External event line; used with real-time clock.
BINIT	L	Bus initialize signal.
BPOK	H	Power OK line from supply.
BDCOK	H	DC power ok, from supply.

Figure 4. The LSI-11 BUS

REFERENCES

[1] Zvi Soha and William Pohlman, "A High Performance, Microprogrammed NMOS-LSI Processor for 8- and 16-Bit Applications," NEREM 74 Record, Part 2, Boston, Massachusetts, October 1974.

[2] The LSI-11 Processor Handbook, Maynard, Massachusetts: Digital Equipment Corporation, 1975.

[3] The LSI-11 INTERFACING HANDBOOK, MAYNARD, MASSACHUSETTS: DIGITAL EQUIPMENT CORPORATION, 1975.

[4] INTRODUCTION TO MINICOMPUTER NETWORKS, MAYNARD, MASSACHUSETTS: DIGITAL EQUIPMENT CORPORATION, 1974.

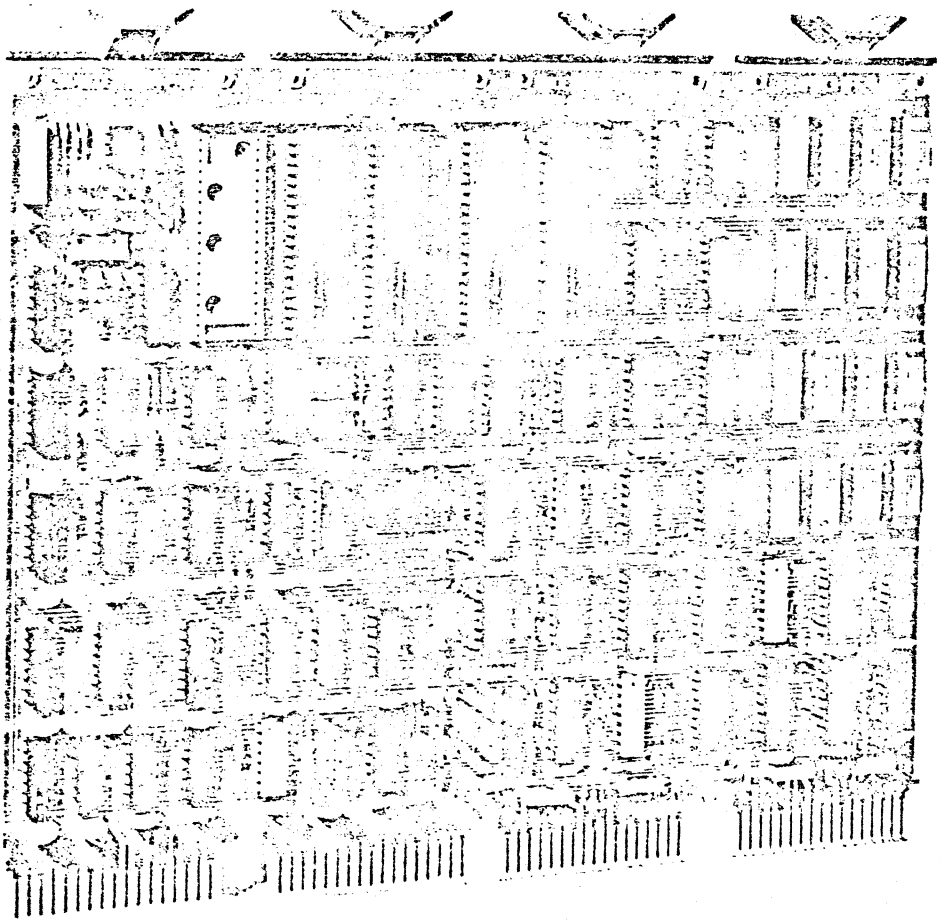


Figure 1. The DEC LSI-11 Microcomputer Module