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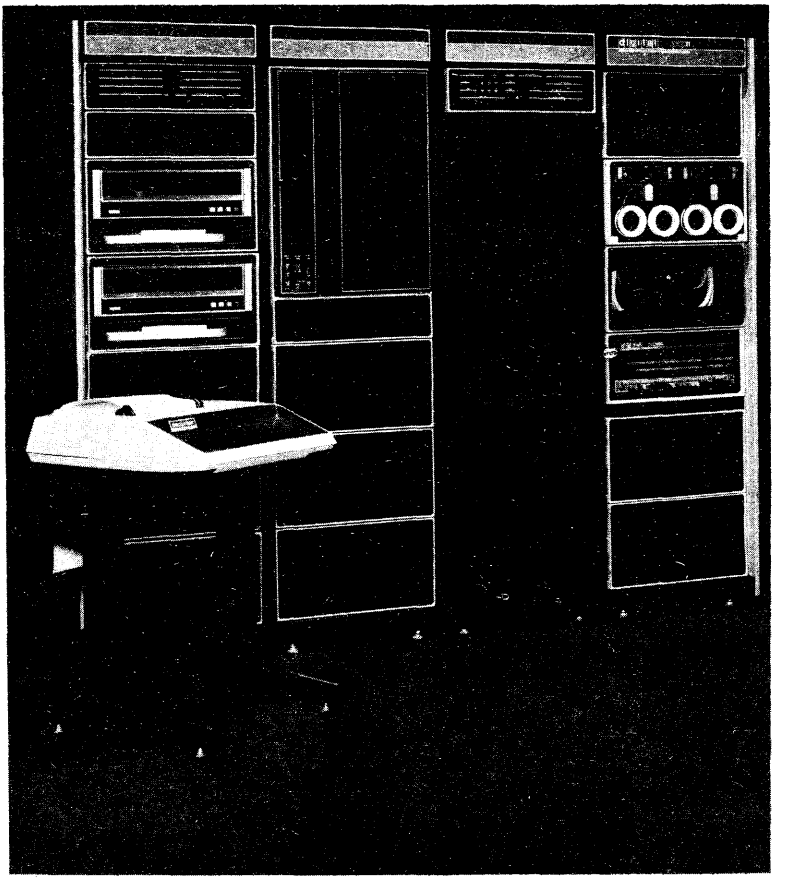
CONTENTS

INTRODUCTION

This Handbook is intended for users of any PDP-11 family system. It describes standard PDP-11 peripherals and options and provides detailed information on interfacing to the PDP-11 UNIBUS.

This Handbook supplements information contained each of the PDP-11 family *processor handbooks.*

Part I describes each PDP-11 peripheral device and includes programming information. Part II covers the operation of the PDP-11 UNIBUS and describes interfacing techniques.



part 1

PERIPHERALS AND OPTIONS

PART I

PART I
Chapter 1

Programming Peripherals

1.1 PROGRAMMING

Programming of peripherals is extremely simple in the PDP-11 -- a special class of instructions to deal with input/output operations is unnecessary. The UNIBUS permits a unified addressing structure in which control, status, and data registers for peripheral devices are directly addressed as memory locations. Therefore all operations on these registers, such as transferring information into or out of them or manipulating data within them, are performed by normal memory reference instructions.

The use of all memory reference instructions on peripheral device registers greatly increases the flexibility of input/output programming. For example, information in a device register can be compared directly with a value and a branch made on the result:

```
CMP PRB, #101
BEQ SERVICE
```

In this case, the program looks for 101_8 in the paper tape reader data buffer (PRB), and branches if it finds it. There is no need to transfer the information into an intermediate register for comparison.

When the character is of interest, a memory reference instruction can transfer the character into a user buffer in core or to another peripheral device. The instruction:

```
MOV PRB,LOC
```

transfers a character from the paper tape buffer into a user-defined location.

All arithmetic operations can be performed on a peripheral device register. For example, the instruction ADD #10, DSX will add 10_8 to a display's x-deflection register.

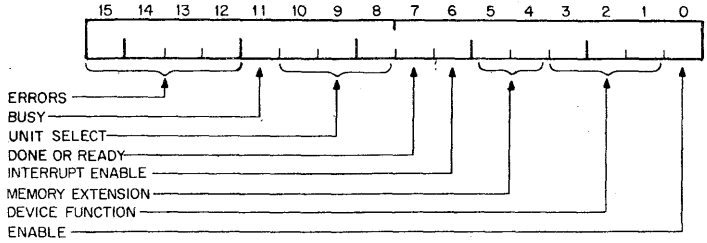
All peripheral device registers can be treated as accumulators. There is no need to funnel all data transfers, arithmetic operations, and comparisions through a single or small number of accumulator registers.

1.2 DEVICE REGISTERS

All peripheral devices are specified by a set of registers which are addressed as core memory and manipulated as flexibly as an accumulator. There are two types of registers associated with each device: 1) control and status registers: 2) data registers.

1.2.1 Control and Status Registers

Each peripheral has one or more control and status registers that contain all the information necessary to communicate with that device. The general form, shown below does not necessarily apply to every device, but is presented as a guide.



Many devices require less than sixteen status bits. Other devices will require more than sixteen bits and therefore will require additional status and control registers.

The bits in the control and status registers are generally assigned as follows:

BIT	NAME	DESCRIPTION
15-12	Errors	Generally there is an individual bit associated with a specific error. When more bits are required for errors, they can be obtained by expanding the error section in the word or by using another status word. Generally Bit 15 is the inclusive OR of all other error bits (if there is more than one). Most devices will have "hard"error conditions which will cause an interrupt if bit 6 is set. Some may also have "soft"errors (warning types) which do not cause immediate interrupts. All errors are generally indicated by individual status bits.
11	Busy	Indicates that a step is being performed.
10-8	Unit Select	Some peripheral systems have more than one device per control. For example, a disk system can have multiple surfaces per control and an analog-to-digital converter can have multiple channels. The unit bits select the proper surface or channel.
7	Done or Ready	The register can contain a DONE bit, a READY bit or a DONE-BUSY pair of bits, depending on the device. These bits are set and cleared by the hardware, but may be queried by the program to determine the availability of the device. For example, the teleprinter status register (TPS) has a READY bit (7) that is cleared on request for output and then set when output is

		complete. The keyboard status register (TKS) has a DONE-BUSY pair (bits 7 and 11) that distinguish between no input (DONE = BUSY = 0), input under way (DONE = 0, BUSY = 1), AND INPUT COMPLETE (DONE = 1, BUSY = 0). The DONE bit could be used to control an input loop for reading from the paper tape reader as follows: LOOP: TSTB PRS ;test low byte ;of paper tape ;status ;register BPL LOOP ;branch back if ;DONE (bit 7) ;is not set
6	Interrupt Enable	Independently programmable. If bit 6 is set, an interrupt will occur as a result of a function done or error condition. To initiate an interrupt routine to read from the paper tape reader, the instruction MOV #101,PRS could be used. This sets bit 0 and bit 6 of the paper tape reader control and status register (PRS). Setting bit 0 starts the read operation and setting bit 6 enables an interrupt to occur when the read operation is complete.
5-4	Memory Extension	Will allow devices to use a full 18 bits to specify addresses on the bus.
3-1	Device Function Bits	Specify operations that a device is to perform. For example, a paper tape read function could be "read one character". An operation for a disk could be "read a block of words from memory and store them on the disk."
0	Enable	When set, enables the device.

NOTE

The "unused"and "load"only bits are always read as zeroes. Loading "unused"or "read only" bits has no effect on the bit position. The mnemonic "INIT"refers to the initialization signal issued by the processor.

Data Buffer Registers

Each device has at least one buffer register for temporarily storing data to be transferred into or out of the computer. The number and type of data registers is a function of the device. The paper tape reader and punch use single 8-bit data buffer registers. A disk would use 16-bit data registers and some devices may use two 16-bit registers for data buffers.

1.2.2 Interrupt Structure

If the appropriate interrupt enable bit is set, in the control and status register of a device, transition from 0 to 1 of the READY or ERROR bit causes an interrupt request to be issued to the processor. Also if READY or ERROR is a 1 when the interrupt enable is turned on, an interrupt request is made. If the device makes the request at a priority greater than that at which the processor is running and no other conflicts exist, the request is granted and the interrupt sequence takes place:

a. the current program counter (PC) and processor status (PS) are pushed onto the processor stack;

b. the new PC and PS are loaded from a pair of locations (the interrupt vector) in addressed memory, unique to the interrupting device.

Since each device has a unique interrupt vector which dispatches control to the appropriate interrupt handling routine immediately, no device polling is required. Furthermore, since the PS contains the processor priority, the priority at which an interrupt request is serviced can be set under program control and is independent of the priority of the interrupt request. The Return from Interrupt Instruction (RTI) is used to reverse the action of the interrupt sequence. The top two words on the stack are popped into the PC and PS, returning control to the interrupted sequence.

1.2.3 Programming Example

A paper tape reader interrupt service could appear as follows:

First the user must initialize the service routine by specifying an address pointer and a word count

```
INIT:   MOV #BUFADR,POINTER     ;set address pointer
        MOV #COUNT,COUNTR       ;set counter
        MOV #101,PRS            ;enable reader program continues until interrupt
```

When the interrupt occurs and is acknowledged, the processor stores the current PC and PS on the stack. Next it goes to the interrupt vector and picks up the new PC and PS beginning at location 70. When the program was loaded the address of PRSER would be put in location 70 and 200_8 in 72 (to set priority at 4). The next instruction executed is the first instruction of the device service routine at PRSER.

```
PRSER:  TST PRS             ;test for error
        BMI ERROR           ;branch if bit 15 set
        MOVB PRB,@POINTR    ;move character to buffer
        INC POINTR          ;increment pointer
        DEC COUNTR          ;decrement character count
        BEQ DONE            ;branch when input done
        INC PRS             ;start reader for next character
DONE:   RTI                 ;return to interrupt program
```

PART I
Chapter 2

Basic I/O Terminals

2.1 INTRODUCTION

This chapter describes the simplest and most common devices for entering data to and receiving data from a PDP-11 system: teleprinters, paper tape punches and readers, line printers and card readers.

The ASR 33 Teletype (DEC model number LT33-DC) is provided as standard equipment with some basic PDP-11 Family systems. It will type or print information at a rate of up to 10 characters per second and is equipped with low speed paper punch and reader (10 cps). A Teletype with keyboard and printer but without paper tape reader and punch (KSR) is also available. The LA30 DECwriter, a teleprinter completely designed by DEC, answers the need for a fast reliable, low-cost terminal and is particularly appropriate for systems requiring large numbers of highly reliable printer/terminals. It prints at speeds of up to 30 characters per second with low noise levels.

The PC11 High Speed Paper Tape Reader and Punch is available for users who need faster paper tape reading speeds than those offered by the standard ASR 33 Teletype. The PC11 reads perforated tape at rates of up to 300 characters per second and punches tape at 50 characters per second.

The LP11 high speed line printer, one of the few line printers available with 80-column width, will print a maximum of 356 full lines per minute (80-column, 64-character model). A 132 column model is also available as are 96 character sets giving upper and lower case printing.

Any combinations of these devices may be used with a PDP-11. For example, the RSTS-11 BASIC-PLUS timesharing system can accommodate up to 16 teleprinter terminals, in addition to other I/O devices.

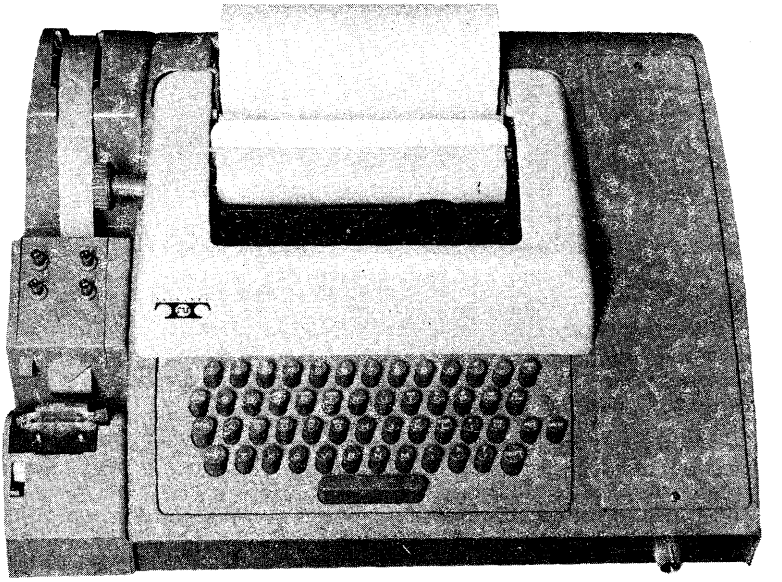
DEC devices utilize American National Standard Code for Information Interchange (ANSCII), 1968 version, code.

The eight-bit code used by the Model ASR Teletype is ASCII modified. To convert ANSCII code to Teletype code, add 200 octal (ASCII + 200_8 = Teletype). This code is read in the normal octal form used in the computer.

On paper tape, bits are numbered from right to left, from 0 through 7, with bits 0 through 2 containing the least significant octal number. Holes corresponding to bits 2 and 3 are separated by a row of small feed holes for moving the tape.

2.2 TELETYPE

The standard ASR 33 Teletype can be used to type in or print out information, or to read in or punch out perforated paper tape. Printing, punching and reading are



ASR 33 TELETYPE

performed at rates of up to 10 characters per second. The KL11-A Teletype Control assembles or disassembles Teletype serial information for parallel transfer to, or from, the UNIBUS.

2.2.1 Operation

When the processor addresses the bus, the Teletype Control decodes the address to determine if the Teletype is the selected device and, if selected, whether it is to perform an input or output operation. Signals transferred between the Teletype and the control logic are standard serial, 11-unit code Teletype signals. They consist of "marks" and "spaces" which correspond to bias and idle current in the Teletype serial line, and 1's and 0's in the control and computer. The 11-bit code consists of a start bit, 8 data bits, and 2 halt bits.

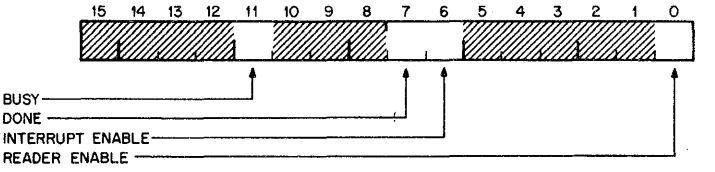
2.2.2 Programming

The Teletype Control has four addressable registers. They have memory addresses and can be read or loaded using any PDP11 instruction that refers to their address.

REGISTER	ADDRESS
Reader Status Register (TKS)	777560
Reader Buffer Register (TKB)	777562
Punch Status Register (TPS)	777564
Punch Buffer Register (TPB)	777566

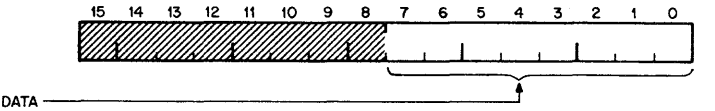
The bit assignments for the registers are shown below. The "unused" and "load only" bits are always read as zeros. Loading "unused" or "read only" bits has no effect on the bit position. The mnemonic "INIT" refers to the initialization signal issued by on, power up, console start, or RESET.

Reader Status Register



BIT	NAME	DESCRIPTION
15-12		Not Used
11	Busy	Indicates that the Teletype Control is receiving a start bit or information bits. Cleared by INIT, set by start bit, cleared after reception of first halt bit. Read only.
10-08		Not used
7	Done	Character available in buffer. Cleared by INIT, cleared by referencing data buffer, causes interrupt when INTR ENB = 1. Read only. Cleared when RDR ENB is set.
6	Reader Interrupt Enable	Interrupts Enable. Enables Error or Done to cause an interrupt. Cleared by INIT.
5-1		Not used
0	Reader Enable	Enables reader (not keyboard) to read one character. Cleared by INIT; cleared when legitimate start bit is detected. Load only.

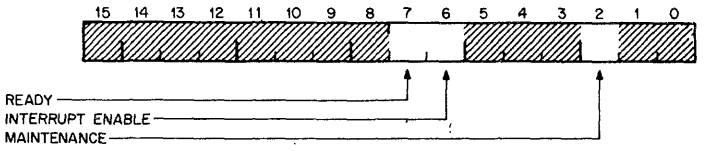
Reader Buffer (TKB)



BIT	NAME	DESCRIPTION
15-8		Not used
7-0	Data	Holds character read. Cleared by start bit. Read only.

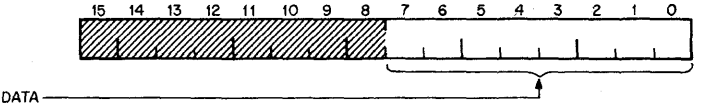
Any reference to TKB (as word or byte) or TKB + 1 clears DONE.

Punch Status Register (TPS)



BIT	NAME	DESCRIPTION
15-8		Not used
7	Ready	Punch available. Set by INIT, cleared when buffer is loaded, set when punching complete. Caused interrupt if INTR ENB = 1. Read only.
6	Interrupt Enable	Enables READY to cause interrupt. Cleared by INIT.
5-3		Not used
2	Maintenance	Maintenance function. Disables serial line input from Teletype unit and enables serial output of punch to feed into reader buffer. Cleared by INIT.
1-0		Not used

Punch Buffer Register (TPS)



BIT	NAME	DESCRIPTION
15-8		Not used
7-0	Data	Holds character to be punched. Cleared by INIT. Load only.

Any instruction that could modify TPB as a byte or word, clears READY and initiates punching. Other reference to either byte or word have no effect on the punch.

2.2.3 Programming Examples

Reading a Character (from reader or keyboard):

```
READ:   INC TKS              ;Set RDR ENB
LOOP:   TSTB TKS             ;Look for DONE
        BPL LOOP             ;Wait if DONE = 0
        MOVB TKB,R0          ;Read character
```

Programming Example: Punching a Character

```
PUNCH:  TSTB TPS             ;Test for READY
        BPL PUNCH            ;Wait if READY = 0
        MOVB R0,TPB          ;Punch character
```

Programming Example: Echoing Keyboard

```
ECHO:   TSTB TKS             ;Character available?
        BPL ECHO             ;Wait if DONE = 0
LOOP:   TSTB TPS             ;Is punch ready?
        BPL LOOP             ;Wait if READY = 0
        MOVB TKB,TPB         ;Punch character
        BR ECHO              ;Repeat for next character
```

Programming Example: Reading 10 Characters (by means of an interrupt)

```
START:  MOV #10,R0           ;Set up counter
        MOV #2000,R1         ;Set up buffer pointer
        MOV #101,TKS         ;Set INTR ENB and RDR ENB
STALL:  BR STALL             ;Hang up here until
                             ;block is read
        .
        .
        .
        .
        .
        .
60:     RDRINT               ;Start of reader service
                             ;routine
62:     000200               ;Raise processor to priority
                             ;level 4
```

```
RDRINT:  MOVB TKB,(R1)+      ;Put character into buffer
         DEC R0              ;Decrement counter
         BEQ END             ;If count = 0, get out
         INC TKS             ;Enable reader again
         RTI                 ;Return from interrupt
END:     TST (SP)+,(SP)+     ;Reset stack
         CLR TKS             ;Clear INT ENB
         JMP  STALL+2        ;Back to program
```

2.2.4 Specifications

Space Requirement:	Requires a floor space of approximately 22 1/2 inches wide by 18 1/2 inches deep. The standard Teletype cable length restricts its location to within 8 feet of the side of the computer.
Weight:	70 lbs
Interrupt Vector Address:	Keyboard/ printer: 60 Teleprinter/punch: 64
Priority Level:	BR4 (Teletype keyboard has precedence over Teletype printer.
Operating Temperature:	50 -110 F
Humidity:	20% to 80%
KL11A Control:	Humidity: 20% to 90% Temperature: 55 to 100 F.

The KL11A is capable of driving up to to 1,500 feet of cable if necessary.

Model	Type	Power	Description
LT33-DC LT35-DC	33 ASR 35 ASR	115, 60Hz	Automatic send/receive unit. Includes keyboard and a reader/punch for paper tapes.
LT33-DD LT35-DD	33 ASR 35 ASR	230V, 50Hz	same as above.
LT33-CC LT35-CC	33 KSR 35 KSR	115V, 60Hz	Keyboard only. Does not include paper tape capability.
LT33-CD LT35-CD	33 KSR 35 KSR	230V, 50Hz	Same as above

2.4 HIGH SPEED READER PUNCH-PC11

The High Speed Reader & Punch is capable of reading eight-hole unoiled perforated paper tape at 300 characters per second, and punching tape at 50 characters per second. The system consists of a High Speed Paper Tape Reader/Punch and the PC11 Control. A unit containing a reader only (PR11) is also available.

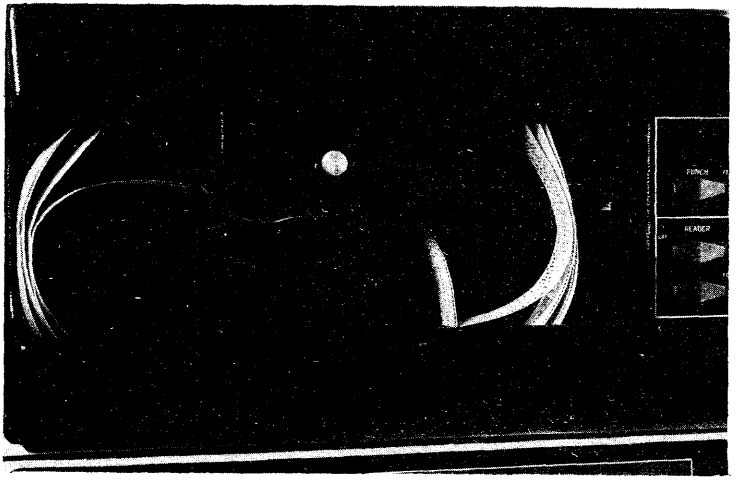
2.3.1 Operation

In reading tape, a set of photodiodes translate the presence or absence of holes in the tape to logic levels representing Is and Os. In punching tape, a mechanism translates logic levels representing Is and Os to the presence or absence of holes in the tape. Any information read or punched is parallel-transferred through the Control. When an address is placed on the UNIBUS, the Control decodes the address and determines if the reader or punch has been selected. If one of the four device register addresses have been selected, the Control determines whether an input or an output operation should be performed. An input operation from the reader is initiated when the processor transmits a command to the Paper Tape Reader Status register. An output operation is initiated when the processor transfers a byte to the Paper Tape Punch Buffer Register.

The Control enables the PDP-11 System to control the reading or punching of paper tape in a flexible manner. The reader can be operated independently of the punch, either device can be under direct program control or can operate without direct supervision through the use of interrupts, to maintain continuous operation.

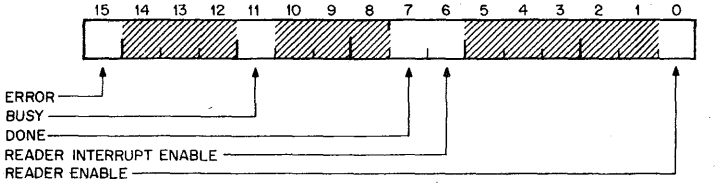
2.3.2 Programming

REGISTER	ADDRESS
Papertape Reader Status Register (PRS)	777550
Papertape Reader Buffer (PRB)	777552
Papertape Punch Status (PPS)	777554
Papertape Punch Buffer (PPB)	777556



High Speed Paper Tape Reader/Punch

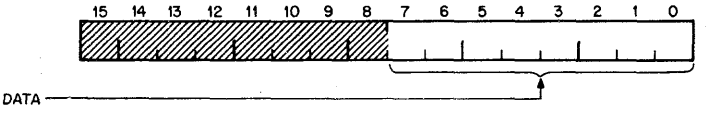
Papertape Reader Status Register (PRS)



BIT	NAME	DESCRIPTION
15	Error	Indicates one of three possible error conditions: no tape in reader, reader is off-line, or reader has no power. Disables RDR ENB; causes interrupt if RDR INT ENB = 1.
14-12		Not used.
11	Busy	Indicates that a character is in the process of being read. Cleared by INIT, set by RDR ENB, cleared when character is available in buffer. Read only.
10-8		Not used
7	Done	Character available in buffer. Cleared by INIT, set when character available, cleared by referencing reader buffer (PRB),

		cleared by setting RDR, ENB; causes interrupt when RDR INT ENB = 1. Read only.
6	Reader Interrupt Enable	Interrupts enable. Enables ERROR or DONE to cause an interrupt Cleared by INIT.
5-1	Not used.	
0	Reader Enable	Enables reader to fetch one character. Clears DONE, sets BUSY, and clears reader buffer (PRB). Operation of this bit is disabled if ERROR = 1; attempting to set it when ERROR = 1 will cause an immediate interrupt if RDR INT ENB = 1. Load only.

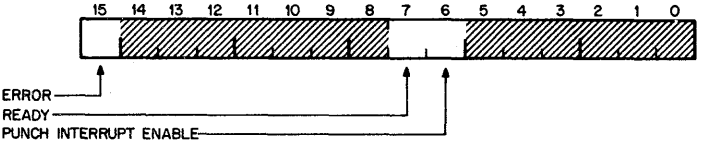
Papertape Reader Buffer (PRB)



BIT	NAME	DESCRIPTION
15-8		Not used
7-0	Data	Holds character to be read. Cleared by RDR ENB. Read only.

Note: Referencing either high byte or low byte or both bytes clears DONE. Referencing is any operation (read, load, test, compare).

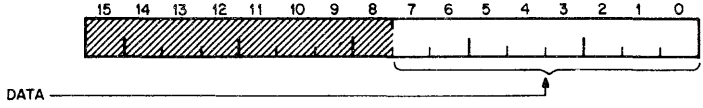
Papertape Punch Status (PPS)



BIT	NAME	DESCRIPTION
15	Error	Indicates one of two error conditions in punch: no tape in punch or punch unit out of power. Causes interrupt if PUN INT ENB (of PPS) = 1.
14-8		Not used.

7	Ready	Ready to punch character. Set by INIT, cleared by loading data buffer (see note under PPB), set when punching complete. Causes interrupt when PUN INT ENB = 1. Read only.
6	Punch Interrupt Enable	Interrupts enable. Enables ERROR or READY to cause interrupt. Cleared by INIT.
5-0		Not used.

Papertape Punch Buffer Register (PPB)



BIT	NAME	DESCRIPTION
7-0	Data	Write-only. Any instruction that could modify bits 7-0 of PPB clears Ready and initiates punching. An immediate interrupt will occur when punching is initiated if ERROR = 1 and PUN INT ENB = 1.

2.3.3 Programming Examples

Reader Interrupt Service

The PDP-11 System can combine PC11 operations with other processing by using the interrupt mode of device operation. When a device operation has been initiated, the PC11 continues without supervision until the operation is complete (or an error occurs); the remainder of the PDP-11 System if free to perform other operations. When the PC11 Control requires further service, the processor is notified by an interrupt.

Each device that is operated in an interrupt mode must be initialized by commands from the processor. An interrupt service routine and an interrupt vector (at the address corresponding to the vector address selected by the jumpers on the M782 Module) must be provided.

The program that follows can be used to read a block of 128 characters from the paper tape to a buffer.

```
START:  MOV #-200,R0        ;INITIALIZE COUNTER
        MOV #101,PRS        ;SET INTR ENB AND RDR ENB
HANG:   BR HANG             ;HANG UP HERE UNTIL BLOCK
                            ;IS READ
70:     RDRINT              ;VECTOR TO INTERRUPT ROUTINE
72:     200                 ;SETS STATUS TO PRIORITY 4
```

```
RDRINT: TST PRS              ;TEST FOR ERROR
        BMI ERR              ;TYPE OUT MESSAGE IF ERROR
        MOVB PRB,BUFEND(R0)  ;FILL BUFFER STARTING AT
                             ;BUFEND-200(OCTAL)
        INC R0               ;COUNT ONE BYTE AND MOVE
                             ;POINTER
        BEQ OUT              ;WHEN COUNT IS ZERO, EXIT LOOP
        INC PRS              ;ENABLE READER AGAIN
        RTI                  ;RETURN FROM INTERRUPT
OUT:    ADD #4,SP            ;UNSTACK INTERRUPT PC AND PS
        CLR PRS              ;INHIBIT FURTHER INTERRUPTS
        JMP HANG+2           ;CONTINUE MAIN PROGRAM
```

NOTE

The position of the buffer used by this program is specified by the end of the buffer, not the beginning. The indexed address uses the negative counter values to access bytes at decreasing distances from this base address.

Two operations performed by this program require caution. When a program accesses the same or contiguous locations, the program operating speed increases if the locations are addressed through a register. If this is done either no other use can be made of this register or: a) the interrupt service routine must stack the former contents of the register, b) the counter must be moved from a temporary storage location to the register, c) the register must be used, and d) the storage operations reversed. In this example where the processor does not do any other processing, no conflicts with the use of the register occur.

A second caution refers to the terminating exit from the service routine. When the exit does not occur through an RTI instruction, the main program PC (Program Counter) and PS (Processor Status) words that are stacked by the interrupt must be removed from the stack. The ADD instruction at OUT performs the operation. If this operation is not performed, the values stacked by other operations previous to the interrupt are not properly accessible.

Punch Programmed Service

The sequence of instructions that follows transfers one byte from register 0 to the paper tape. When controlling the punch, the READY bit of the PPS register is checked before the transfer; when controlling the reader, the DONE bit of the PRS register is checked after a command.

```
PUNCH: BIT #100200,PPS       ;CHECK PUNCH STATUS
       BEQ PUNCH             ;IF NOT READY OR ERROR, WAIT
       BMI ERROR             ;PROCESS ERROR IF ANY
       MOV R0,PPB            ;OUTPUT CHARACTER
```

Punch Interrupt Service

This interrupt service routine outputs 8-bit codes to the paper tape, unless they are ASCII representations of the formatting characters Line Feed, Rubout, or Form Feed. Line Feeds and Rubouts are ignored (not punched), and the program stops punching when the character read from the buffer is a Form Feed. The Form Feed is not punched. The program transfers the contents of a buffer: a) starting at a preselected address to paper tape, b) stopping automatically when it reads an end-of-buffer character, and c) performing simple character editing.

The interrupt service routine is called into operation when the following sequence of instructions is encountered in the main program:

```
R0 = %0                    ;REGISTER ZERO
SP = %6                    ;REGISTER SIX
PC = %7                    ;REGISTER SEVEN
PS = 177776                ;PROCESSOR STATUS WORD
CLR PUNDON                 ;CLEAR SOFTWARE FLAG
MOV #BUFFER POINTER        ;SET UP BUFFER POINTER
MOV #100,PPS               ;SET PUNCH INTR ENB
```

This instruction sequence sets up the system by initializing the service routine and enabling interrupts from the punch.

If the punch is idle, an interrupt occurs immediately; otherwise, the first interrupt is delayed until the current operation is completed. The software flag is used by the main program to provide a check on the progress of the output. This occurs in the following manner: The main program continues with other processing until the use of the punch is required, or further processing is dependent on completion of the output. At this point the sequence of instructions shown below is executed.

```
LOOP: TST PUNDON           ;CHECK SOFTWARE FLAG
      BPL LOOP
```

If the interrupt service routine has not set the flag, the processor stays in this wait loop, allowing interrupts for further output operations, until the routine signals that it is finished.

In this example, the interrupt routine to service the punch requires the following sequence of instructions:

```
74:   PCHINT               ;VECTOR TO ROUTINE
76:   200                  ;NEW STATUS WORD

PCHINT:
      MOV R0,-(SP)         ;SAVE REGISTER ZERO
```

```
        MOV POINTER,R0          ;SETUP REGISTER
        TST PPS                 ;CHECK NO ERRORS
        BMI ERROR               ;IF ERROR, EXIT WITH LAST
                                ;BUFFER POSITION IN R0
RETEST:
        CMPB (R0), #212         ;LINE FEED?
        BNE TEST2               ;NO, CONTINUE
        INC R0                  ;YES, IGNORE CHARACTER
        BR RETEST               ;AND TEST NEXT CHAR.
TEST2:  CMPB (R0), #377         ;RUBOUT?
        BNE TEST3               ;NO, CONTINUE
        INC R0                  ;YES, IGNORE
        BR RETEST
TEST3:  CMPB (R0), #214         ;FORM FEED?
        BEQ OUT                 ;YES, EXIT
        MOVB (R0)+,PPB          ;NO, OUTPUT CHARACTER
        MOV R0,POINTER          ;SAVE REGISTER
        MOV (SP)+,R0            ;UNSTACK PREVIOUS CONTENTS
        RTI                     ;NORMAL RETURN
OUT:    MOV (SP)+,R0            ;RESTORE TO PREVIOUS STATUS
        COM PUNDON              ;SET SOFTWARE FLAG
        CLR PPS                 ;CLEAR INT ENB
        RTI
POINTER: 0

PUNDON: 0
```

2.3.4 Specifications

READER/PUNCH

Reader:	Photoelectric 300 Characters Per Second Includes: light source, set of photodiodes, tape transport, bins to hold and collect tape
Punch:	50 Characters Per Second Includes: Punch Drive Motor, Punch Mechanism, Mechanism to advance and position tape

PC11 CONTROL	
Consists of:	3 IC modules mounted on one-fourth of a DD11-A system unit or general purpose slot of an 11 Family processor
INTERRUPT	
Vector Addresses:	Reader 70; Punch 74;
Priority Level:	BR4 (Reader has higher priority than punch if both request service simultaneously)
PAPER TAPE	
Type:	Unoiled fanfold, 8 holes per column
Code:	All bits are read and written
OPERATING TEMPERATURE:	55 ° to 100 °F
HUMIDITY:	20 to 95% (noncondensing)
SIZE/MOUNTING:	Fits in 10 1/2 - inch frame that mounts in a standard 19-inch rack
MODELS:	PC11 READER/PUNCH = 60Hz, 117-V PC11A Reader Punch = 50 Hz 117 V PR11 Reader only = 50/60 Hz 117 V

2.4 HIGH SPEED LINE PRINTER - LP11

The LP11 High Speed Line Printer is available in several models, ranging from an 80-Column, 64-character model (LP11-FA) to an 132-column, 96-character model (LP11-HB). Either column-width printer can be ordered with 64- or 96- character print sets. The printer is an impact type using a revolving character drum and a hammer per column. Forms up to six-parts, may be used for multiple copies. Fanfold paper from 4-inch to 14-7/8 inches wide may be used with adjustment for pin-feed tractors. The print rate is dependent upon the data and the number of columns to be printed. Characters are printed 20 (24 on 132-col. model) at a time and if 20 (24) or less are used the rate can be as high as 1100 lines per minute.

2.4.1 Operation

Characters are loaded into the printer memory via the LPB (Line Printer Buffer) serially by character. When the memory becomes full (20 characters) they are automatically printed. This continues until the full 80 columns have been printed or a special character is recognized. The 132-column model prints 24 characters at a time. The special characters (non-printing) are:

CR (015) Carriage Return. Causes the currently-stored characters to be printed, and resets the column counter to 1 (the next printing character loaded would print in column 1). Does not advance the paper.

LF (012) Line Feed. Causes the currently-stored characters to be printed, then resets the column counter to 1 and advances the paper one line.

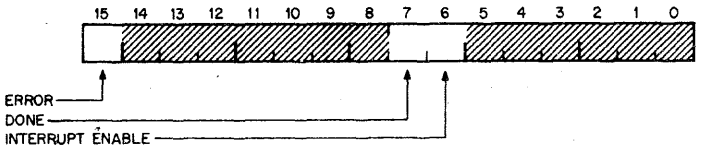
FF (014) Form Feed. Causes the currently-stored characters to be printed, then resets the column counter to 1 and advances the paper to top of next page.

LP11 HIGH SPEED LINE PRINTER

2.4.2 Programming

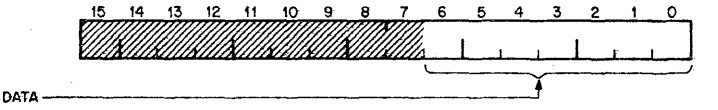
REGISTER	ADDRESS
Line Printer Status (LPS)	777514
Line Printer Data Buffer (LPB)	777516

Line Printer Status Register (LPS)



BIT	NAME	DESCRIPTION
15	Error	Set when an error condition exists in the printer. Errors are: a) Power off b) No paper c) Printer drum gate open d) Over temperature alarm e) Printer placed OFF-LINE May be read only. Reset only by manual correction of error condition.
14-8	Not Used	
7	Done	Set whenever printer is ready for next character to be loaded. Indicates that previous function is either complete or has been started and continued to a point when the printer may accept the next command. May be read only. Set only by printer condition. Will not be set if printer is OFF-LINE.
6	Interrupt Enable	May be set or cleared under program control. Cleared by INIT signal on UNIBUS (RESET instruction or START console function). When set, an interrupt will be requested when DONE or ERROR becomes a 1.
5-0		Not used

Line Printer Data Buffer Register



BIT	NAME	DESCRIPTION
15-7		Not used
6-0	DATA	7-bit ANSCII character buffer. Characters are transferred to the printer by loading this buffer. The data in this buffer cannot be read - it will always read 0.

2.4.3 Programming Example
INTERRUPT SERVICE ROUTINE

```
200:    LPSERV          ;VECTOR TO SERVICE ROUTINE
242:    200             ;SERVICE AT PRIORITY 4
MAIN:   BIS #100,LPS    ;ENABLE INTERRUPT

LPSERV: TST LPS         ;CHECK FOR ERROR
        BMI ERROR
        MOV R0,-(SP)    ;SAVE R0
        MOV BUFADR,R0   ;GET BUFFER POINTER
LOAD:   MOVB (R0)+,LPB  ;LOAD PRINTER BUFFER
        CMP R0,BUFEND   ;END OF DATA?
        BHI PRCOMP      ;YES, GO TO PRINT COMPLETE.
        TSTB LPS        ;NO, CHECK DONE
        BMI LOAD        ;NOT FULL, GET ANOTHER CHAR.
EXIT: MOV R0,BUFADR     ;SAVE BUFFER POINTER
        MOV (SP)+,R0    ;RESTORE R0
        RTI
```

2.4.4 Specifications
Printable Characters:

Character Set:	64 or 96
Type:	Open Gothic print
Size:	Typically 0.095 inches high and 0.065 inches wide
Characters:	64-character set 96-Character set
Code format:	ANSCII
Characters per line:	80 or 132
Character drum:	1760 rpm(64 character drum)
Speed:	1180 rpm(96 character: drum)

Print Rate:	
80-column Model	
64 character:	356 Lines/minute, columns 1-80 460 Lines/minute, columns 1-60 650 Lines/minute, cloumns 1-40 1110Lines/minute, columns 1-20
96 character:	253 Lines/minute, columns 1-80 330 Lines/minute, columns 1-40 478 Lines/minute, columns 1-20
132-Column Model	
64 character:	245 Lines/minute, columns 1-132 290 Lines/minute, columns 1-120 356 Lines/minute, columns 1-96 460 Lines/minute, columns 1-72 650 Lines/minute, columns 1-48 1110 Lines/minute, columns 1-24
96 character:	173 Lines/minute, columns 1-132 205 Lines/minute, columns 1-120 253 Lines/minute, columns 1-96 330 Lines/minute, columns 1-72 478 Lines/minute, columns 1-48 843 Lines/minute, columns 1-24

	80 column	132 column
Height:	46 inches	46 inches
Width:	24 inches	48 inches
Depth:	22 inches	25 inches
Weight:	200 pounds	220 pounds

Control:	The LP11 controller is a "small peripheral controller" which occupies 1/4 of a DD11-A or equivalent space in a PDP-11 Family processor.
Operating Temperature:	50 - 110 degrees F
Humidity:	10%-80% (non-condensating)
Power Requirements Printer:	117 Vac ±10%; 60 Hz ± or 3 Hz, single phase or 234 Vac ± 10%; 50 Hz ± + Hz, single phase 250 Watts
Control:	Supplied by H720 in mounting box where the control is mounted.
Signal Cable:	25 foot interconnecting signal cable is supplied with system. Maximum allowable cable length is 100 feet.

2.5 PUNCHED CARD READER - CR11 AND MARK SENSE CARD READER - CM11

Model CR11 Card Reader reads EIA standard 80-column punched data cards at 300 cards per minute; model CM11 reads 40-column mark-sense cards, which can have punched holes, at 200 cards per minute.

The punched card reader uses a vacuum picker which works in conjunction with riffle air so that card wear is insignificant, card jam virtually impossible and the reader extremely tolerant of damaged cards. The riffling action separates the cards in the input hopper to prevent sticking. The picker uses a strong vacuum to grasp the bottom card and deliver it to the read station on demand. The picker and associated throat block prevent the unit from multiple picking to the extent that taped or stapled cards are not allowed to enter the card track. In such cases the reader stops with pick check alarm. The operator can separate the cards and enter them into the input hopper for normal reading. The card track is very short, so that, only one card is in motion at a time. The combination of damaged card tolerance, gentle card handling and short card track provide virtually jam-proof operation.

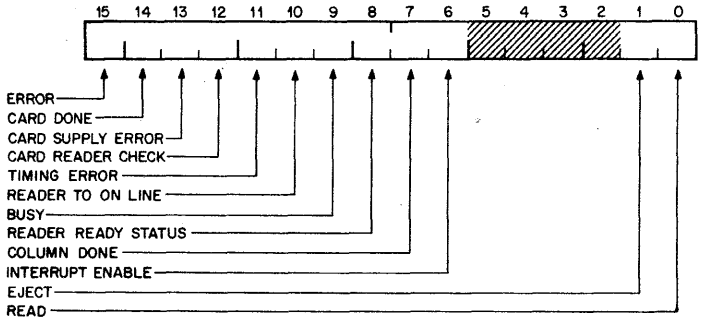
2.5.1 Operation

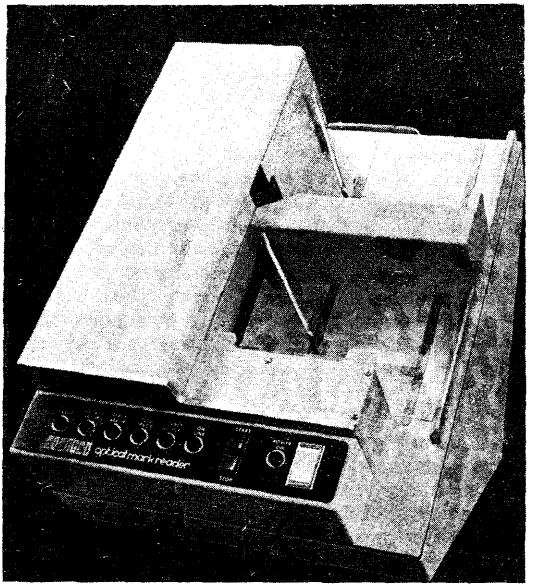
Cards are read by column, beginning with Column 1. A select instruction starts the card moving past the read station. Once a card is in motion, all 80 columns are read. Column information is read in one of two program-selected modes: card image or compressed code. In the card image mode 12 information bits in one column are loaded into the data buffer and are available to the program at CRB1 address. In the compressed code mode, the card image is encoded into 8-bit bytes and is available to the program at CRB2 address. A punched hole is interpreted as binary 1, and the absence of a hole as binary 0

2.5.2 Programming

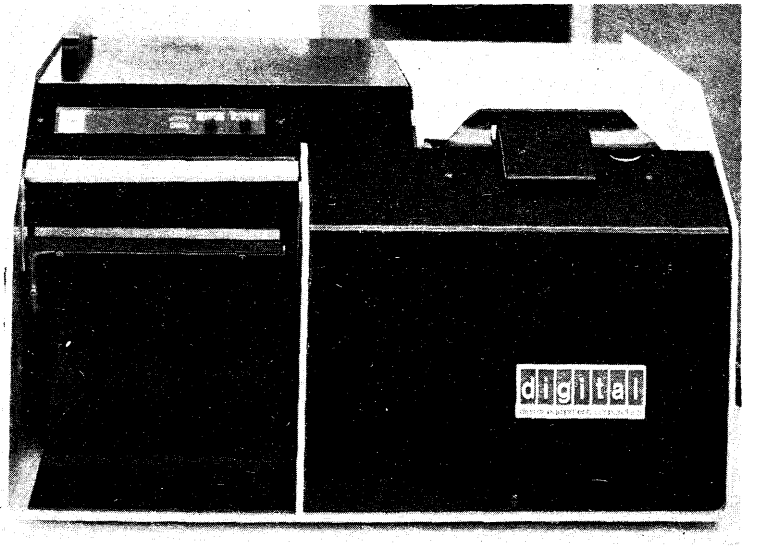
REGISTER	ADDRESS
Card Reader Status (CRS)	777160
Card Reader Data Buffer (CRB1)	777162
Card Reader Data Buffer (CRB2)	777164

Card Reader Status Register (CRS)





CM11 MARK SENSE CARD READER



CR11 PUNCHED CARD READER

BIT	NAME	DESCRIPTION
15	Error	When set, it indicates that an error has occurred.
14	Card Done	When set, indicates that one card has passed through the read station and another one may be demanded from the input hopper.
13	Card Supply Error	When set indicates that the input hopper is empty or output stack is full. This signal is provided by mark sense card readers only and is not normally available with punched card units.
12	Card Reader Check	Set to indicate abnormal condition in the card reader. Four conditions can cause this bit to be set: a)Feed error b)Motion error c)Stack Fail d)Dark Light Check These signals are only available from mark sense readers.
11	Timing Error	When set it indicates that a new column of data arrived into the CRB before the previously loaded column was attended to by a program.
10	Reader To on Line	Indicates that the reader went on-line. Sensing an error or operating the stop switch on the card reader panel causes the reader to go off-line. Operating the start switch brings the reader on-line providing no error causing condition exists.
9	Busy	Indicates that a card is being read.
8	Reader Ready Status	When set, indicates the reader is off line; O indicates on-line and hence ready to accept read commands.
7	Column Date	Indicates that a column of data is ready in CRB.
6	Reader Interrupt Enable	If declared as "1" while loading the status register, this bit allows the CARD DONE, COLUMN DONE, or ERROR bit, to cause a program interrupt.

5-2		Not used
1	Eject	When set, column ready flag is inhibited from setting. However, data transfers between card reader and data buffer do take place.
0	Read	If declared as "1"while loading the status register, this bit allows the feed mechanism to deliver a card to the read station.

A program can load and read information from the Card Reader Status (CRS) register using appropriate instructions and considering the following limitations:

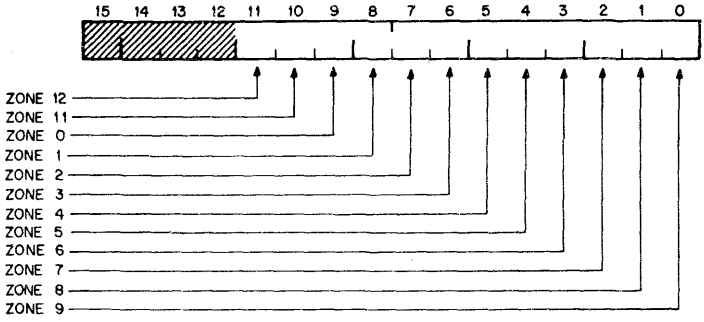
a. Bits 15-7 can only be read on the bus.

b. COLUMN DONE bit is automatically cleared by reading the Data Buffer.

c. Bits 15-8 are automatically cleared when an attempt to load the status register is made. However, if this loading is to read a card, and an error condition requiring manual intervention has not been attended by the operator, appropriate error bit will be set again to cause an interrupt.Commands to READ CARD under these circumstances is not honored.

d. BIT 0 is always read as zero on the bus.

Card Reader Data Buffer Register (CRB1, CRB2)



No information can be loaded into the Card Reader Data Buffer (CRB1) by any program; the content of this register can only be read.

Data from one column at a time of the card is loaded into this register.

BIT	DESCRIPTION
15-12	NOT USED
11	ZONE 12
10	ZONE 11
9	ZONE 0
8	ZONE 1
7	ZONE 2
6	ZONE 3
5	ZONE 4
4	ZONE 5
3	ZONE 6
2	ZONE 7
1	ZONE 8
0	ZONE 9

If the data buffer is addressed at CRB2, the 12-bit content is compressed into an 8-bit character by an encoding network before getting on to the bus as low order byte. The 8-bit code is:

BIT	DESCRIPTION
15-8	NOT USED
7	ZONE 12
6	ZONE 11
5	ZONE 10
4	ZONE 9
3	ZONE 8
2-0	DATA encoded as follows: 000 = ZERO ZONE 1-7 001 = ZONE 1 010 = ZONE 2 011 = ZONE 3 100 = ZONE 4 101 = ZONE 5 110 = ZONE 6 111 = ZONE 7

In case of multiple zones twice, bits will be the inclusive OR of the octal codes of the zones.

2.5.3 Specifications

Speed:	Up to 300 cards per minute (punched) Up to 200 cards per minute (mark)
Hopper Capacity:	600 cards (400 cards mark sense)
Size (complete unit):	19 1/4 inches wide x 11 inches high x 14 inches deep
Weight:	60 lbs
Environmental:	+50 degrees to +122 degrees F. 10-90% humidity, non-condensing
Input Power:	117± 10% 60 Hz 234 ±10% 50 Hz Single Phase
Power Consumption:	950 VA starting 400 VA running
Interrupt Priority:	BR 6 (may be changed by jumper)
Interrupt Vector Address:	230

2.6 DECWRITER LA30

The LA30 DECwriter is a fast, reliable and low cost data terminal. It prints from a set of 64 characters at speeds up to 30 characters per second. Data entry is made from either a 97- or 128-character keyboard. It produces an original and one copy on a standard 9 7/8-inch wide, tractor-driven continuous form.

The DECwriter is delivered with an attractive stand. The noise generated by the terminal is less than that of an electric typewriter, a feature, welcomed in an office environment. Because of its low price, the DECwriter is particularly appropriate for systems requiring large numbers of highly reliable printer/terminals.

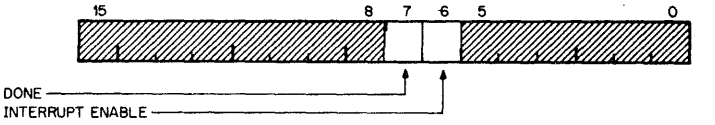
High reliability has been achieved through reduction of the number of mechanical parts. Clutches, brakes, dashpots and other similar parts have been eliminated from the printing mechanism. Instead, the DECwriter generates a 5 x 7 matrix. Seven solenoid-driven, spring-loaded pins are arranged vertically in the printing head. The head is advanced by solid-state logic; drive circuitry actuates selected pins to generate characters.

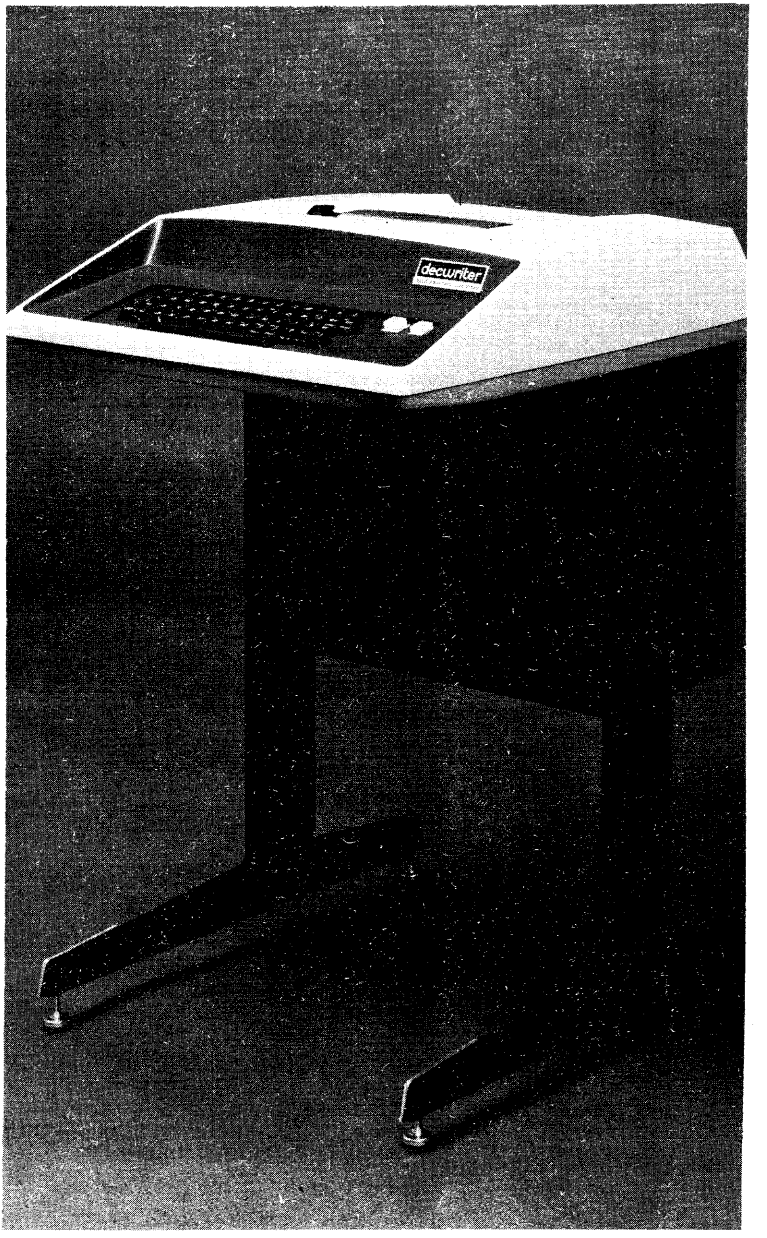
2.6.1 Programming

The LA30 interfaces to the PDP-11 via the LC11A Controller. All software control of LC11A is accomplished via four device registers. These are assigned memory addresses and can be read or loaded (with the exceptions noted) using any instruction that refers to their address.

REGISTER	ADDRESS
Keyboard Status Register (KBS)	777560
Keybuffer Register (KBB)	777562
Printer Status Register (PRS)	777564
Printer Buffer Register (PRB)	777566

Keyboard Status Register (KBS)

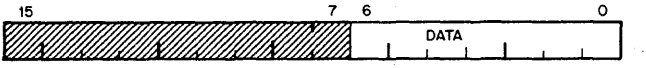




LA30-DECwriter

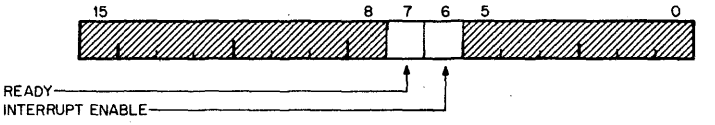
BIT	NAME	DESCRIPTION
15-8	Unused	
7	Done	Character available in Buffer cleared by INIT; cleared by referencing data buffer. Causes interrupt when ID = 1. Read only.
6	Interrupt Enable	When set, it enables done to cause interrupt. Cleared by INIT.
5-0	Unused	

Keyboard Buffer Register (KBB)



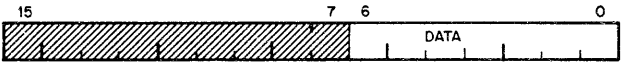
BIT	NAME	DESCRIPTION
15-7	Unused	
6-0	Data Buffer	Holds character keyed in from keyboard. Read only.

Printer Status Register (PRS)



BIT	NAME	DESCRIPTION
15-8	Unused	
7	Ready	Printer available. Set on power of printer, reset or print. Strobe leading edge. Is set when printing is complete. Note READY is set 2μs after CR is received by printer. This is to alow receipt of non-printing characters during carriage return time, i.e. LF. If a printing character is received during carriage return time, READY is reset and will be set after CR and printing are complete. READY will cause interrupt if ID = 1. Read only.
6	Interrupt Enable	When set, enables READY to cause interrupt. Cleared by INIT.
5-0	Unused	

Printer Buffer (PRB)



BIT	NAME	DESCRIPTION
15-7	Unused	
6-0	Data Buffer	DATA BUFFER - Transfers the data from the UNIBUS to the printer. Printer holds character strobed in to print. Load only.

Any instruction that could modify PRB as a byte or word clears READY and initiates printing.

2.6.2 Programming Examples
Read a character (from keyboard)

```
LOOP:  TST TKS          ; look for DONE
       BPL LOOP         ; Wait if DONE = 0
READ:  MOV TKB; R0      ; Read character
```

ECHO keyboard

```
ECHO:  TSTB TKS         ; Character available?
       BPL ECHO         ; Wait if DONE = 0
STALL:  TSTB TPS        ; Is punch readyff
       BPL STALL        ; Wait if READY = 0
       BR ECHO          ;
```

2.6.3 LA30 Specifications

Printing Speed:	30 characters per second, asynchronous, 300ms carriage return 30 line feeds/sec
Line Length:	80 character positions
Character Spacing:	10 characters per inch
Line Spacing:	6 lines per inch
Paper:	9 7/8 inches wide - tractor driven continuous form original plus one copy. With adjustment, up to 6 copies.
Typeface:	5 x 7 dot matrix
Printing Characters:	64 upper case ASCII subset (lower case codes print as upper case)

Ribbon:	1/2 inch x 120 feet, nylon
Code:	USASCII-1968 characters
Temperature:	50°F. - 130°F.
Humidity:	5-90% (noncondensing)
Dimensions:	20 1/2 inches wide x 31 inches high x 24 inches deep
Interface:	LC11A
DC Power:	Self-contained
Types:	LA30 PA 115V/60Hz LA30 PB 234V/60Hz LA30 PC 115V/50Hz LA30 PD 234V/50Hz

Magnetic Tape Options

Two types of magnetic tape options are available to PDP-11 users:

- Small, dual 3.9-inch reel DECtape systems
- Large single 10 1/2-inch reel Magtape systems (industry compatible)

Both types of devices offer high performance at low cost. DECtapes are ideal for applications which do not require writing, reading or storage of large volumes of data. Magtapes, however, are suitable for handling large volumes of data.

3.1 DECTAPE TC11/TU56

3.1.1 Introduction

The TC11/TU56 is a dual-unit, bidirectional magnetic-tape transport system for auxiliary data storage. Low cost, low maintenance and high reliability are assured by:

- simply designed transport mechanisms which have no capstans and no pinch rollers.
- hydrodynamically lubricated tape guiding (the tape floats on air over the tape guides while in motion)
- redundant recording
- Manchester recording techniques (virtually eliminate drop outs)

Each transport has a read/write head for information recording and playback on five channels of tape. The system stores information at fixed positions on magnetic tape as in magnetic disk or drum storage devices, rather than at unknown or variable positions as in conventional magnetic tape systems. This feature allows replacement of blocks of data on tape in a random fashion without disturbing other previously recorded information. In particular, during the writing of information on tape, the system reads format (mark) and timing information from the tape and uses this information to determine the exact position at which to record the information to be written. Similarly, in reading, the same mark and timing information is used to locate data to be played back from the tape.

The DECtape system consists of the TU56 dual transport, the TC11 Control (which will buffer and control information for up to four dual transports) and DECtape 3/4-inch magnetic tape on 3.9-inch reels.

3.1.2 Operation

The system utilizes a 10-track read/write head. On a tape the first five tracks include a timing track, a mark track, and three data tracks. The other five tracks are identical counterparts and are used for redundant recording to increase system reliability. The redundant recording of each character bit on non-adjacent tracks materially reduces bit dropout and minimizes the effect of skew. The use of Manchester phase recording, rather than amplitude sensing techniques, virtually eliminates dropouts.

The timing and mark channels control the timing of operations within the control unit and establish the format of data contained on the information channels. The timing and mark channels are recorded prior to all normal data reading and writing on the information channels. The timing of operations performed by the tape drive and some control functions are determined by the information on the timing channel. Therefore, wide variations in the speed of tape motion do not affect system performance.

The standard format tape is divided into 578 blocks. The structure of each block is symmetric: block numbers and checksums are recorded at both ends of a block and thus searching, reading, or writing can occur in either direction. However, a block read in the opposite direction than it was written will have the order of the data words reversed.

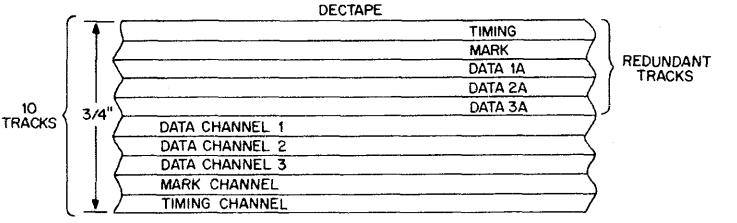


Figure 3-1 - DECtape Format

Information read from the mark channel is used during reading and writing data to indicate the beginning and end of data blocks and to determine the functions performed by the system in each control mode. The data tracks are located in the middle of the tape where the effect of skew is minimum. The data in one bit position of each track is referred to as a line or as a character. Since six lines, or characters, make up a word, the tape can record 18-bit data words. During normal data writing, the Controller disassembles the 18-bit word and distributes the bits so they are recorded as six 3-bit characters. Since PDP-11 words are 16 bits long, the Controller writes the extra two bits 0's and ignores them when reading. However, during special modes, the extra two bits can be written and recovered.

A 260-foot reel of DECtape is divided into three major areas: end zones (forward and reverse), extension zones (forward and reverse), and the information zone. The two end zones (each approximately 10 feet) mark the end of the physical tape and are used for winding the tape around the heads and onto the take-up reel. These zones never contain data.

The forward and reverse extension areas mark the end of the information region of the tape. Their length is sufficient to ensure that once the end zone is entered and tape motion is reversed, there is adequate distance for the transport to come up to proper tape speed before entering the information area.

The information area, consists of blocks of data. The standard is a nominal 578 blocks, each containing 256 data words (nominally). In addition each block contains 10 control words.

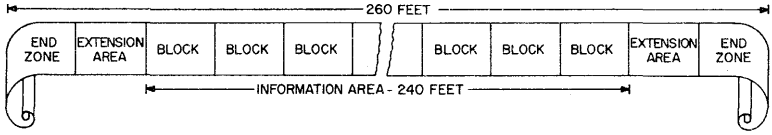
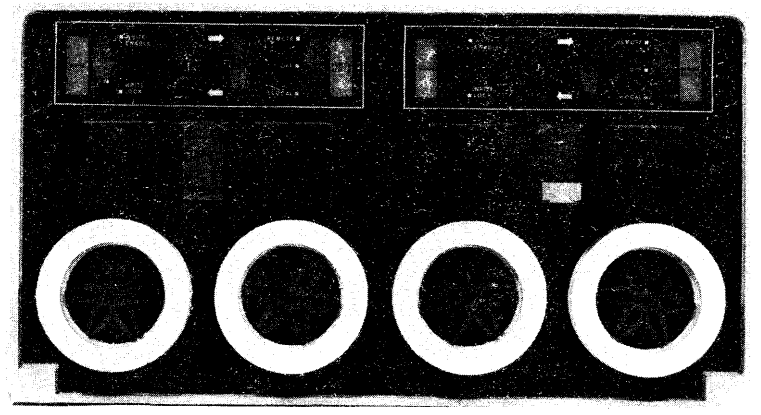


Figure 3-2 - DECtape Block Arrangement

The blocks permit digital data to be partitioned into groups of words which are interrelated while at the same time reducing the amount of storage area that would be needed for addressing individual words. A simple example of such a group of words is a program. A program can be stored and retrieved from magnetic tape in a single block format because it is not necessary to be able to retrieve only a single word from the program. It is necessary, however, to be able to retrieve different programs which may not be related in any way. Thus, each program can be stored in a different block on the tape.

Since DECtape is a fixed address system, the programmer need not know accurately where the tape has stopped. To locate a specific point on tape he must only start the tape motion in the search mode. The address of the block currently passing over the head is read into the DECtape control and loaded into an interface register. Simultaneously, a flag is set and a program interrupt can occur. The program can then compare the block number found with the desired block address and tape motion continued or reversed accordingly.



TU56 DECtape Unit

3.1.3 Programming

All transport operations are controlled by the controller from program instructions. The controller selects the transport, controls tape motion and direction, selects a read or write operation and buffers data transferred.

The controller can select any one of eight commands that control operation of the DECtape system. When the system is operated on-line, these commands are used for reading or writing data on the tape and for controlling tape motion. The desired command is selected by the program which sets or clears bits 03, 02, and 01 in the command register (TCCM) to specify an octal code representing the desired command.

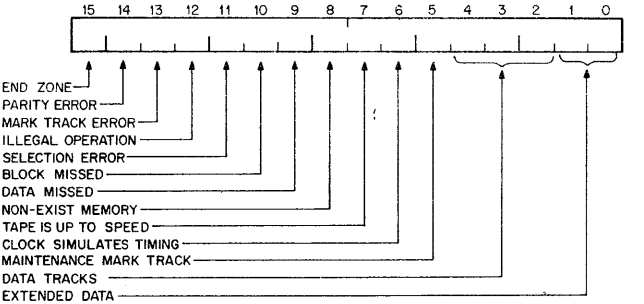
The commands are:

OCTAL CODE	MNEMONIC	FUNCTION
0	SAT	Stops all tape motion.
1	RNUM	Finds the mark track code that identifies the block number on the tape in the selected tape unit. Block number found is available in the data register (TCDT).
2	RDATA	Assembles one word of data at a time and transfers it directly to memory. Transfers continue until word count overflow, at which time data is read to the end of the current block and parity is checked.
3	RALL	Reads information on the tape that is not read by the RDATA function.
4	SST	Stops all tape motion in selected transport only.
5	WRTM	Writes timing and mark track information on blank DECtape. Used for formatting new tape.
6	WDATA	Writes data into the three data tracks. 16 bits of data are transferred directly from memory.
7	WALL	Writes information on areas of tape not accessible to WDATA function.

All software control of the TC11 DECtape system is performed by means of five device registers. They can be read or loaded using any PDP-11 instruction that refers to their address.

REGISTER	ADDRESS
Control and Status Register (TCST)	777340
Command Register (TCCM)	777342
Word Count Register (TCWC)	777344
Bus Address Register (TCBA)	777346
Data Register (TCDT)	777350

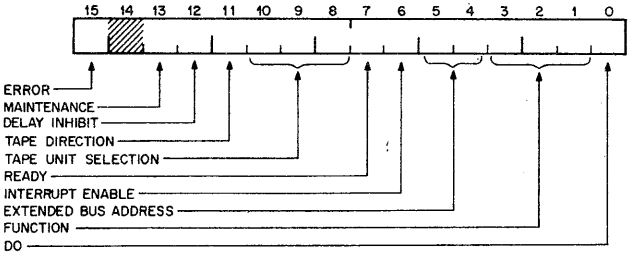
Control and Status Register(TCST)



BIT	NAME	DESCRIPTION
15	End Zone (ENDZ)	Indicates that the selected tape unit is in an end zone region of the tape. Cleared by INIT; cleared by loading a 0 into bit 15 (ERROR) of command register; cleared by loading a 1 into bit 00 (DO) of the command register. Stops selected tape unit.
14	Parity Error (PAR)	Indicates a parity error. The parity error occurs during RDATA function if the calculated and written checksums disagree, Cleared in the same manner an ENDZ.
13	Mark Track Error(MTE)	Indicates that an error occurred during decoding of the mark track. Stops selected tape unit. Cleared in the same manner as ENDZ (bit 15).
12	Illegal Operation(ILO)	Indicates an illegal operation caused by a conflict in switch positions of the WRITE ALL, WRITE T&M, and WRITE ENABLE/WRITE LOCK switches. These conflicts are: a. WRITE LOCK on during WRTM, WALL, or WDATA modes b. WRITE T&M switch off during WRTM mode c. WRITE ALL switch off during WALL mode
11	Selection Error(SELE)	Stops selected tape unit. Cleared when switches reset to valid positions and oper-

		ation repeated. Indicates that the program has either selected a non-existent tape unit or has attempted to select more than one tape unit. Stops selected tape unit. Disabled if MAINT bit (bit 13 in TCCM) is set or if function is SAT (bits 03, 02, and 01 in TCCM cleared). Cleared when unit selection switches set to valid positions and selection repeated.
10	Block Missed (BLKM)	Indicates a block was missed. The transfer from read block number (RNUM) to read data (RDATA) or write data (WDATA) functions occurred too late. Also, indicates switch from RDATA to WDATA was too late. Cleared in the same manner as ENDZ (bit 15).
9	Data Missed (DATM)	Indicates data was missed. Request for data transfer not honored in time during RDATA, WDATA, WALL, or RALL. Cleared in the same manner as ENDZ (bit 15).
8	Non-Existent Memory(NEX)	Indicates non-existent memory. This occurs when TC11 Controller is bus master and does not receive a SSYN response within 20 μs after asserting MSYN. Cleared in the same manner as ENDZ (bit 15).
7	Tape Is Up To Speed(UPS)	Indicates that selected tape unit is up to speed required for proper operation. Cleared by INIT; cleared when UNIT SELECT or REV bit is changed. Set when unit is up to speed; set when MAINT bit (bit 13 in command register) is set.
6	Clock Simulates Timing (CLK)	Used to simulate timing track. May be loaded when MAINT bit is set. When CLK is set, produces TP1; when cleared, produces TPO.
5	Maint Mark Track (MMT)	Used to simulate the bit read from the mark track. May be loaded when MAINT bit is set. Cleared by INIT.
4-2	Data Tracks (DT)	Used to simulate output of the read amplifer. When MAINT bit is set, DTO loads into RWB2 and reads as RWB5; DT1 loads into RWB1 and reads as RWB4; DT2 loads into RWB0, reads as RWB3.
1-0	Extended Data (XD)	Extended data bit 17 or 16, which allow reading and writing on areas of the tape not accessible during 16-bit word transfers. Cleared by INIT.

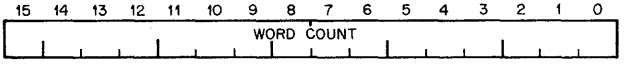
Command Register (TCCM)



BIT	NAME	DESCRIPTION
15	Error	Indicates an error condition which is the inclusive OR of all error conditions (bits 15-8 in TCST). Causes an interrupt if enabled (see bit 6). Clears errors (except ILO and SELE) when loaded with zero. Sets READY bit (bit 7).
14	Unused	
13	Maintenance (MAINT)	Used for maintenance functions. When set, enables operation of bits 6-2 in the TCST. Cleared by INIT.
12	Delay Inhibit(DINHB)	Set to inhibit the delay associated with bringing a tape unit up to speed when reselecting a tape unit known to be up to speed by a previous command. Cleared by INIT.
11	Tape Direction (REV)	Specifies direction of tape motion. When set, specifies reverse motion; when cleared, specifies forward motion. Cleared by INIT.
10-8	Unit Select	Specify the number of the tape unit which is to receive the desired command. These three bits are set or cleared to represent an octal code which corresponds to the unit number of the tape unit to be used. Cleared by INIT.
7	READY	Indicates that the TC11 controller is ready to receive a new command. Cleared when DO (bit 00) is set. Set when command execution is complete; set by INIT or ERROR (bit 15). Read only.
6	Interrupt Enable (IE)	Allows an interrupt to occur provided either READY (bit 07) or ERROR (bit 15) is set. Cleared by INIT.
5-4	Ext Bus Address (XBA)	Used to specify address line 17 (XBA17)

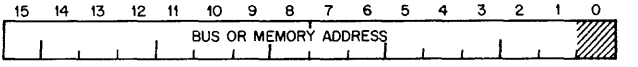
		or address line 16 (XBA16) in direct memory transfers. Increments with the TCBA. Cleared by INIT.
3-1	Function Bits	Specify a command to be performed upon the selected transport. Cleared by INIT to SAT.
0	DO	Loaded with a 1 when a new function is given. Clears READY

Word Count Register (TCWC)



BIT	NAME	DESCRIPTION
15-0	Word Count	Contains two's complement of the number of words to be transferred. This register counts the number of word transfers made during RDATA (read data) and WDATA (write data) functions. When one of these functions is initiated, the word count register is loaded. The register is incremented by 1 after each transfer. When the contents of the register equals all zeros, further transfers are inhibited. Cleared by INIT. (Note: This register must not be modified by using byte instructions. Use only word instructions when loading).

Bus Address Register (TCBA)



BIT	NAME	DESCRIPTION
15-1	Address	Specify the bus or memory address to or from which data is to be transferred during RDATA (read data) and WDATA (write data) operations. These bits are used in conjunction with bits XBA17 and XBA16 in the command register. After each transfer (during RDATA and WDATA) is made, this register is incremented to advance it to the next word location. The BA bits participate in the incrementation; they are a logical extension to this register. Cleared by INIT. (Note: the bus address register must not be modified by using byte instructions when loading this register).
0	Unused	

Data Register (TCDT)

BIT	NAME	DESCRIPTION
15-0	Data	Contains data word to be read from or written on the magnetic tape. These bits and bits XD17 and XD16 in the status register form three six-bit shift registers which are active during control operations. These 18 bits correspond one to one with the six three-bit characters read or written on the tape. The data register accepts information under program control during WALL (write all) and WRTM (write timing and mark) operations. During RALL (read all) and RNUM (read block number) operations, the data register contains data read from the tape. During WDATA (write data) and RDATA (read data) operations, the data register is used to buffer information between the controller and memory. Cleared by INIT. Note: The data register must not be modified by using byte instructions. Use only word instructions when loading this register.

3.1.4 Programming Examples

The following two examples represent typical methods of programming the TC11 Controller. The first example finds a specified block. The second example is a routine for writing data into a specific block.

a. Routine to find a specified block

```
;ENTER WITH R0 = BLOCK WANTED
;FINDS BLOCK IN FORWARD DIRECTION

SEARCH:   MOVE R0, BWANT
          SUB #3, BWANT          ;OFFSET
          MOV #4003, TCCM        ;UNIT 0,REVERSE, RNUM, DO

LOOP1:    BIT #100200, TCCM      ;CHECK READY AND ERROR
          BEQ LOOP1
          BMI ERROR
          SUB TCDT, #BWANT       ;CHECK BLOCK FOUND
          BLT SEARCH

FORWRD:   MOV R0, BWANT
          MOV #3, TCCM           ;UNIT 0, FORWARD, RNUM
                                  DO

LOOP2:    BIT #100200, TCCM      ;CHECK FOR READY AND ER-
                                  ROR
          BEQ LOOP2
          BMI ERROR
          SUB TCDT, BWANT        ;CHECK BLOCK FOUND
```

```
                BGT FORWRD
                BLT SEARCH
                RTS PC          ;RETURN WHEN BLOCK IS
                                 FOUND

ERROR:          TST TCST        ;TEST FOR ENDZ
                BMI LOOP3
                HALT            ;HALT ON ERROR OTHER
                                 THAN
                                ;ENDZ

LOOP3:          BIT #4000, TCCM ;CHECK DIRECTION
                BNE FORWRD      ;IF REV, NOW SEARCH FOR-
                                 WARD
                BR SEARCH       ;IF FOR, NOW SEARCH RE-
                                 VERSE
```

b. Routine to write 100 words into block 47 on unit 0

```
                MOV #47, R0     ;SET UP R0 FOR SUBROUT-
                                 INE
                                ;CALL
                JSR PC, SEARCH  ;GO FIND BLOCK
                MOV #-100, TCWC ;SET UP WORD COUNT
                MOV #BUFFER, TCBA ;SET UP BUS ADDRESS
                MOV #15, TCCM   ;GIVE COMMAND: WDATA, DO
                                ;UNIT 0, FORWARD

LOOP4:          BIT #100200, TCCM ;CHECK READY AND ERROR
                                   ROR = 0
                BEQ LOOP4       ;BRANCH ON READY AND ER-
                BMI ERR         ;BRANCH TO ERROR SERVICE
                .
                .
                .               ;CONTINUE WITH PROGRAM
                .
                .
BUFFER:         0               ;START OF BUFFER
```

3.1.5 Specifications

Tape Characteristics

Size, type:	260 feet of 3/4 inch, 1 mil, Mylar sandwich tape, Mylar protected on both sides
Reel Size:	3.9 inches diameter
Handling:	Direct drive hubs and specially designed guides float the tape over the head. No capstans or pinch rollers.
Speed:	97 ±14 inches per second Reading and writing performed at rate of 5000 16-bit words per second

Density:	350 ±55 bits per inch
Data Capacity:	147,968 16-bit words in blocks of 578 blocks of 256 words each
Tape Motion:	Bidirectional (forward and reverse)
Word Transfer Rate:	Three bits are read or written together every 33 1/3 microseconds; one 16-bit word is read and assembled or disassembled and written in 200 microseconds
Addressing:	Mark and timing tracks allow searching for a specific block (under program control; no auto- search capability) by number in either the forward or reverse direction.
Tape Motion Timing:	Start Time: 150 ±15ms Stop Time: 100 ±10ms Turnaround Time: 200 ±20ms

Interrupt

Priority Level:	6
Vector Address:	214

TU56 DECtape Transport

Mounting:	Mounts in standard 19-inch rack
Size:	10 1/2 inches high, 19 inches wide, 9 3/4 inches deep
Cooling:	Internally mounted fan
Controls:	Front panel mounted. Includes: unit select, write/enable lock, forward/reverse, remote-off-local

TC11 Controller

Mounting:	Mounts in standard 19-inch rack
Size:	10 1/2 inches high, 18 inches wide
Controls:	Mounted behind blank front panel; includes: write all and write timing and mark enable/disable switches; error, ready, interrupt enable, and function indicators

Environmental Conditions

Temperature:	40 ° to 90 ° F for system 60 ° to 80 ° F for magnetic tape

Humidity:	15% to 80% (non-condensation) for system 40% to 60% (non-condensation) for tape
	Power and Cabling:
Input Power:	115 Vac ± 10%, 50/60 Hz@6A 230 Vac ± 10%, 50/60 Hz@3A for TC11 Controller 115/220 Vac ± 10%, 50/60 Hz for each TU56@3A
TC11 Power:	System power supplied by one H720 power supply mounted at back of cabinet. Provides + 5V at 22 A and -15 V at 10 A for use by both TC11 and up to four TU56s.
TU56 Power:	Tape transport power provided by internal power supply except for + 5 V and -15 V.
Power Usage:	TC11 uses: 5 A at + 5V, 0.5 A at -15 V. TU56 (one) uses: 800 mA at + 5V, 550 mA at -15V
Cabling:	BC11-A cable to connect controller to Unibus M908 ribbon connector to connect command signals between controller and TU56 and between TU56 units W032 connector to connect analog signals between controller and TU56 and between TU56 units

3.2 MAGTAPE - TM11/TU10

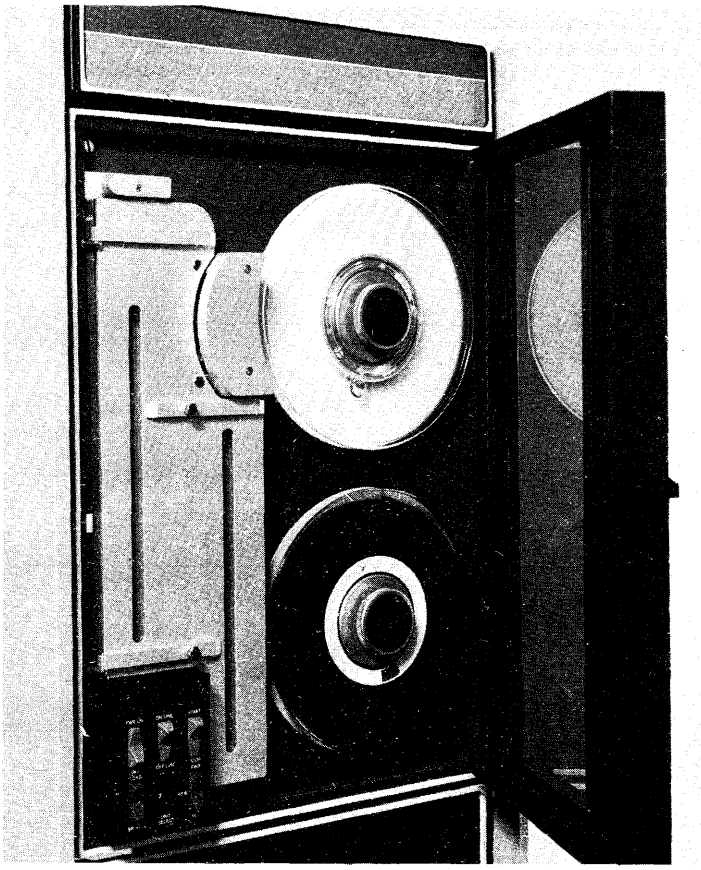
3.2.1 Introduction

The TM11/TU10 is a high-performance, low-cost magnetic tape system ideally suited for writing, reading, and storing large volumes of data and programs in a serial manner. Because the system reads and writes in industry-compatible format, information can be transferred between a PDP-11 and other computers. For example, a PDP-11 might be used to collect data and record it for later processing on a large-scale computer. The 10 1/2-inch tape reels contain up to 2400 feet of tape upon which over 96 million bits of data can be stored on high density 9-track tape or over 72 million bits can be stored on high density 7-track tape.

The TM11/TU10 employs read after write error checking to check that proper data is written on the tape. Should a tape dropout be detected, appropriate action can be taken to assume no loss of data.

Tape motion is controlled by vacuum columns and a servo-controlled single capstan. Long tape life is possible because the only contact with the oxide surface is at the magnetic head and at a rolling contact on one low-friction, low-inertia bearing.

A Magtape System consists of up to eight TU10 transports and a TM11 Control Unit. Transports are capable of operation with seven or nine-track tape and a system can contain any combination of 7- and 9-track units.



TU10 MAGTAPE UNIT

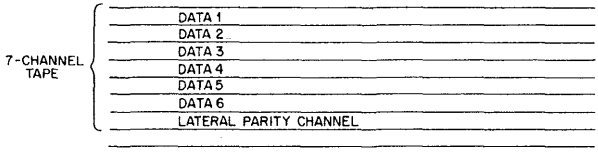
3.2.2 Operation

Reading and writing occurs when the tape is moving forward, but the control can move the tape to new positions in forward or reverse. For writing on tape, 8-bit data words are transferred from core memory to a data buffer in the controller. The data buffer logic supplies the character to the tape transport write logic. For reading, the sequence is reversed; and information is read from tape as 6-bit characters (for 7 track tape; 8 bits for 9 track tape) which are sent to the data buffer. When a complete 8-bit word has been assembled in the data buffer, a data channel word transfer is initiated to transfer the data buffer word into core memory.

The 7- and 9-track system use 1/2-inch mylar base tape which is coated on one side with an iron oxide composition. The method of recording is non-return-to-zero (NRZ). A seven track tape includes six data channels and a lateral parity channel. Density modes of 200, 556, and 800 bytes per inch are selectable. Nine-

track tape is similar to the 7-track tape, but operation is only in the 800 bpi mode and it has the industry standard cyclic redundancy character at the end of each word. The load and end points of the tape are marked by reflective strips which are detected by photo diodes. About 10 inches of blank tape is wound on a reel and precedes the BOT and EOT strips; a gap of about 3 inches is left from the load point before writing can begin.

Since each computer word contains two eight-bit tape characters, a record contains Nx2 characters, where N is the number of words that the processor transfers. Record blocks are separated by 3/4 inch gaps. A record can vary in length from two words (4 data characters) to 4096 words.



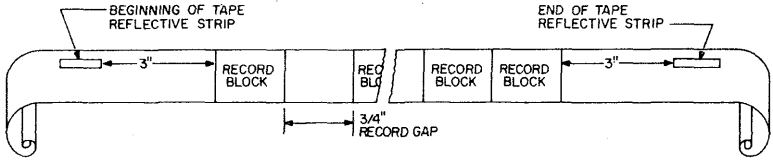
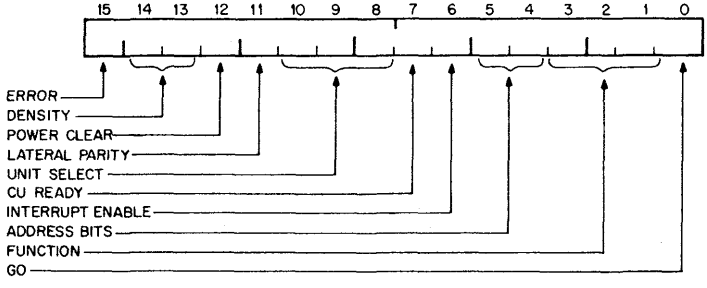


Figure 3-3 - Magtape Format

3.2.3 Programming

REGISTER	ADDRESS
Status Register (MTS)	772520
Command Register (MTC)	772522
Byte Record Counter (MTBRC)	772524
Current Memory Address Register (MTCMA)	772526
Data Buffer Register (MTD)	772530
TU10 Read Lines (MTRD)	772532

Command Register (MTC)



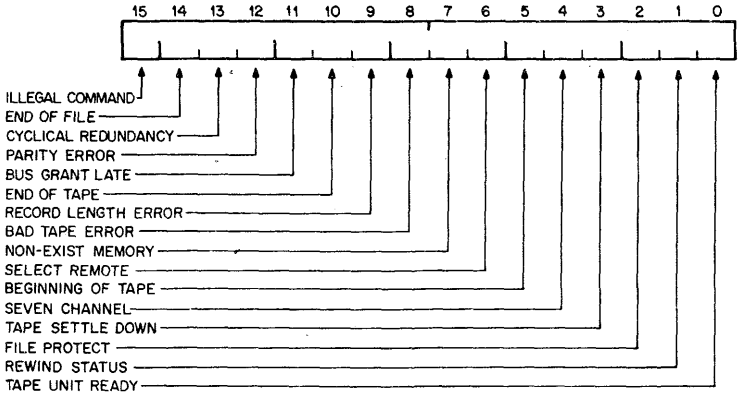
BIT	NAME	DESCRIPTION
15	Error	Set as a function of bits 7-15 of the MTS. Cleared on of INIT or on the GO command to the tape unit.
14-13	Density *	Cleared on INIT.
12	Power Clear	Power clear provides the means for the processor to clear the the control unit and tape units without clearing any other device in the system. The PCLR bit is always read back by the processor as 0.
11	Lateral Parity (PEVN)	Set for the controller to read and write even lateral parity on tape. Cleared from the controller to read and write odd lateral parity from tape . A search for parity error is made in all tape moving operations except space forward, space reverse, and rewind.
10-8	Unit Select	These bits are used to select one of the eight possible magnetic tape units. All operations defined in the MTC and all status conditions defined in the MTS pertain to the MTU indicated by these bits. Cleared on INIT.
7	CU Ready	Cleared at start of a tape operation, and set at end of tape operation. The control unit accepts as legal all commands it receives while the CU Ready bit is 1.
6	Interrupt Enable	When set, an interrupt occurs whenever either the CU ready bit or the ERR bit change from 0 to 1 or whenever a tape unit that was set into rewind has arrived at the beginning of tape. In addition, an interrupt occurs on an instruction that changes the INT ENB from 0 to 1 and does not set the GO bit. (i.e. CU READY or ERROR = 1)
5-4	Address Bits	Extended memory bits. The bits correspond to bits 16 and 17 respectively of the bus address. They are an extension of the MTCMA, and increment during a tape operation if there is a carry out of MTCMA.
3-1	Function Bits	The eight functions (programmable commands) as defined by the three function bits are listed below in the order of the function decodes with function bit 1 the least significant bit:

		0: Off line 1: Read 2: Write 3: Write EOF 4: Space Forward 5: Space Reverse 6: Write with Extended Interrecord Gap 7: Rewind
0	Go	When set, begins the operation defined by the function bits.

*The combinations of bits 14 and 13 and their definitions are:

BIT 14	BIT 13		
0	0	200 bpi	7 channel
0	1	556 bpi	7 channel
1	0	800 bpi	7 channel
1	1	800 bpi	9 channel

Status Register (MTS)



BIT	NAME	DESCRIPTION
15	Illegal Command	Is set by any of the following illegal commands: 1. Any DATO or DATOB to the MTC during the tape operation period 2. A Write, write EOF, or write with extended IRG operation when the FILE PROTECT bit is a 1 3. A command to a tape unit whose SELECT REMOTE bit is a 0 4. The SELECT REMOTE (SELR) bit becoming a 0 during an operation.

In error conditions 1 through 3, the command is loaded into the MTC, but the GO pulse to the tape unit is not generated. In addition the CU ready bit remains set.

14	End of file	An EOF character is detected during a read, space forward or space reverse operation. During the read or space forward operation, the EOF bit is set when the LPC following the EOF character is read. During a space reverse operation, the EOF bit is set when the EOF character following its LPC character is read. The ERR bit sets when the LPC character following the EOF character is detected. The EOF character and its associated LPC character are read into memory during a read operation
13	Cyclical Redundancy	Cyclical Redundancy error is detected only during a read operation. It compares the CRC character read from tape with that regenerated during the same read operation. If they are not the same, CRC ERROR from the tape unit becomes a 1 which forces the CRE bit to a 1. However, the ERR bit does not become a 1 until the LPC character is detected.
12	Parity Error (PAE)	Parity error is the OR of the lateral and longitudinal parity errors. A lateral parity error is indicated on any character in the record while a longitudinal parity error occurs only when the LPC character is detected. A lateral parity error does not affect the transfer of data; that is, in a write operation, the entire record is transferred to tape and in a read operation, the entire record is written into core memory. For all parity errors, the ERR bit sets only when the LPC character is detected. Both lateral and longitudinal parity errors are detected during a read, write, write EOF, and write with extended IRG operations. The entire record is checked including the CRC and LPC characters. Longitudinal parity error occurs when an odd number of 1's is detected on any track in the record. A lateral parity error occurs when an even number of 1's is detected on any character when PEVN is a 0, or an odd number of 1's is detected on any character when PEVN is a 1.
11	Bus Grant Late	A bus grant late error occurs when the control unit, after issuing a request for the bus, does not receive a bus grant before

		the control unit receives the bus request for the following tape character. The condition is tested only for NPR (non-processor request) operations. The ERR bit sets simultaneously with BGL, thus terminating the operation. If the BGL occurred during a write or write with extended IRG operation, the control unit does not send the signal WDS to the master, while the master writes the CRC character (if required) and LPC character onto the tape, terminating the record.
10	End of Tape (EOT)	Set to 1 as the EOT marker is read while the tape is moving in the forward direction. The bit is cleared as soon as the same point is read while the tape is moving in the reverse direction. The ERR bit, as a result of the EOT bit at a 1, sets only in the tape forward direction and coincidentally with the reading of an LPC character.
9	Record Length Error	This error is detected only during a read operation. It occurs for long records only and is indicated as soon as MTBRC increments beyond 0, at which time both data transfer into memory and incrementing of the MTCMA and MTBRC stop. However, the control unit reads the entire record and sets the ERR bit when the LPC character is read. CU ready remains at 0 until the LPC character is read.
8	Bad Tape Error	This error occurs when a character is detected (RDS pulse) during the gap shutdown or settling down period for all operations (except rewind). a new GO command is sent to the tape unit.
7	Non-Existent Memory (NXM)	This error occurs during NPR operations when the control unit is bus master, and is performing data transfers into and out of the bus and when the control unit does not receive a slave SYNC signal within 10 micro seconds after it had issued a master sync signal. The operations which occur when the error is detected are identical to those indicated for the BGL error.
6	Select Remote (SELR)	Cleared when the tape unit addressed

		does not exist, is off line, or has its power turned off.
5	Beginning Of Tape (BOT)	Set when the BOT marker is read, and cleared when the BOT marker is not read. BOT at a 1 does not produce a 1 in the ERR bit.
4	Seven Channel (7 CH)	When set it indicates a 7-channel tape unit. When clear it indicates a 9-channel unit.
3	Tape Settle Down (SDWN)	Set whenever the tape unit is slowing down. The master will accept and execute any new command during the SDWN period except if the new command is to the same tape unit as the one issuing SDWN and if the direction implied in the new command is opposite to the present direction. Also set as soon as the BOT marker is detected while tape is moving forward.
2	File Protect	Set to prevent the control unit from writing information on tape. Controlled by presence or absence of the write protect ring on the tape reel.
1	Rewind Status	Set by the master as soon as it receives a rewind command from the control unit. Cleared by the master as soon as the tape arrives at the BOT marker.
0	Tape Unit Ready	TUR is true when the selected tape unit is stopped and when the SELECT REMOTE is false. Cleared when the processor sets the GO bit and the operation defined by the function bit occurs.

Byte Record Counter (MTBRC)

The MTBRC is a 16-bit binary counter which is used to count bytes in a read, write, or write with extended IRG operation, or records in a space forward or space reverse operation. When used in a write or write with extended IRG operation, the MTBRC is initially set by the program to the 2's complement of the number of bytes to be written on tape. The MTBRC becomes 0 after the last byte of the record has been read from memory. Thus, when the next WDR (Write Data Request) signal occurs from the master, the control unit will not send the WDS (Write Data Strobe) to the master indicating that there are no more data characters in the record.

When the MTBRC is used in a read operation, it is set to a number equal or greater than the 2's complement of the number of words to be loaded into memory. A record length error (RLE) occurs for long records only, and is indicated when a read pulse for data (RDS occurring when CRCS or LPCS does not occur) occurs when the MTBRC is 0. The MTBRC increments by 1 immediately after each memory access.

When the MTBRC is used in a space forward or space reverse operation, it is set to the 2's complement of the number of records to be spaced. It is incremented by a 1 at LPC time, whether the tape is moving in the forward or reverse direction. A new GO pulse is sent to the tape unit during the SDWN time if the MTBRC is not 0 during that time. When the tape unit is moving in reverse, the LPC character is detected before SDWN, but after the entire record has been traversed. Thus, both SDWN and LPC character appear to be in different positions on tape from those when the tape unit is moving forward.

Current Memory Address Register (MTCMA) The MTCMA contains 16 of the possible 18 memory address bits. It is used in NPR operations to provide the memory address for data transfers in read, write, and write with extended IRG operations. Prior to issuing a command, the MTCMA is set to the memory address into which the first byte is loaded in a read operation, or from which the the first byte is read in a write, or write extended IRG operation. The MTCMA is incremented by 1 immediately after each memory access. thus, at any instant of time, the MTCMA points to the next higher address than the one which had most recently been accessed. When the entire record has been transferred, the MTCMA contains the address plus 1 of the last character in the record. In the error conditions Bus Grant Late (BGL) and Non-Existent Memory (NXM), the MTCMA contains the address of the location in which the failure occurred.

The MTCMA is available to the processor on a DATI. The bits are set or cleared on a processor DATO. INIT clears all bits in the MTCMA.

Data Buffer (MTD)
The data buffer is a nine-bit register which is used during a read, write, or write with extended IRG operation. In a read operation, the data buffer is a temporary storage register for characters read from tape before being stored into memory. In a processor read, all nine bits are stored into memory. Bits 0 through 7 in memory correspond to channels 7 through 0 respectively from tape, and bit 8 corresponds to the parity bit. In an NPR operation only the data bits are read into memory, and are alternately stored into the low and high bytes. In a write or write with extended IRG operation, the data buffer is a temporary storage register for characters read from core memory before they are written on tape. The polarity of the parity bit is determined by the PEVN bit in the MTC.

In a read operation, the LPC character enters the data buffer when bit 14 of MTRD is a 1, and inhibited from doing so when bit 14 is a 0. Thus, after reading a nine-channel tape, the data buffer contains the LPC character when bit 14 is a 1 and the CRC character when bit 14 is a 0. After reading a seven-channel tape, the data buffer contains the LPC character when bit 14 is a 1 and the last data character when bit 14 is a 0. After reading a EOF character, the data buffer contains all 0's when bit 14 is a 1 and the LPC character when bit 14 is a 0. The MTD is available to the processor on a DATI. Bits 9 through 15 are read identically to bits 1 through 7 respectively. Bits 0 through 8 are set or cleared on a processor DATO. Bits 9 thru 15 are not affected by a processor DATO. INIT clears all bits in the MTD.

TU10 Read Lines - (MTRD)
The memory locations allocated for the TU10 read lines are:

Bits 0-7 for the channels 7-0 respectively.

Bit 8 for the parity bit.

Bit 12 for the gap shutdown bit.

Bit 13 for the BTE error generation.

Bit 14 for the CRC, LPC character selector.

Bit 15 for the timer.

For correct longitudinal parity, bits 0-8 are 0 after writing a record or reading a record from tape. For a longitudinal parity error, one or more of the bits 0-8 remains at a 1, the bit(s) at a 1 indicating the channel(s) containing the error which sets the CU ready bit. Thus, if the pulse is set during a tape operation, CU ready sets prematurely thus producing the gap shudown period when characters are still being read. Bits 0-8 are set and cleared by the tape unit. Bit 13 is a pulse generated by the processor. Bit 14 is set and cleared by the processor and cleared by INIT. Bit 15 is uniquely controlled by the 100 microsecond timer. The MTRD is available to the processor on a DATI except that bit 13 reads back as a 0.

TIMER

TIMER is a 10 KHz signal with a 50% duty cycle. The signal is used for diagnostic purposes in measuring the time duration of the tape operations. The timer is read as bit 15 in the MTRD.

3.2.4 Specifications

	Tape Characteristics
Size, type:	2,400 feet of 1/2-inch, Mylar-base, iron-oxide coated
Reel size:	10 1/2 inches
Handling:	Direct-drive reel motors, servo-controlled single capstan, vacuum tape buffer changers with constant tape winding tension. There are no dancer arms to cause nonuniform tape tension and stretching
Speed:	45 inches per second, reading and writing Rewind speed: 150 IPS
Density:	7-channel: 800, 556, and 200 bpi; selectable under program control. 9 channel: 800 bpi.
Data Capacity:	12 million characters
Maximum Transfer Rate:	36,000 characters per second
Interrecord Gap:	Will read tape with gap of 0.48 in. or more; will write tape with gap of 0.52 in. or more (compatible with industry standard)
Magnetic Head:	Dual gap, read after write
Recording Mode:	NRZI, industry-compatible
Data Transfer Method:	Non Processor Request (DMA 'cycle stealing')
BOT, EOT Detection:	Photelectric sensing of reflective strip, industry compatible
Skew Control:	Deskewing electronics included in TU10 transport to eliminate static skew
Write Protection:	Write protect ring sensing on TU10 transport
Data Checking Features:	Read after write parity checking of characters; Longitudinal Redundancy Check (7- and 9-channel); Cyclic Redundancy Check (9-channel)
Extended Features:	Self-test of TM11 control with TU10 offline; core dump for 7-channel units.

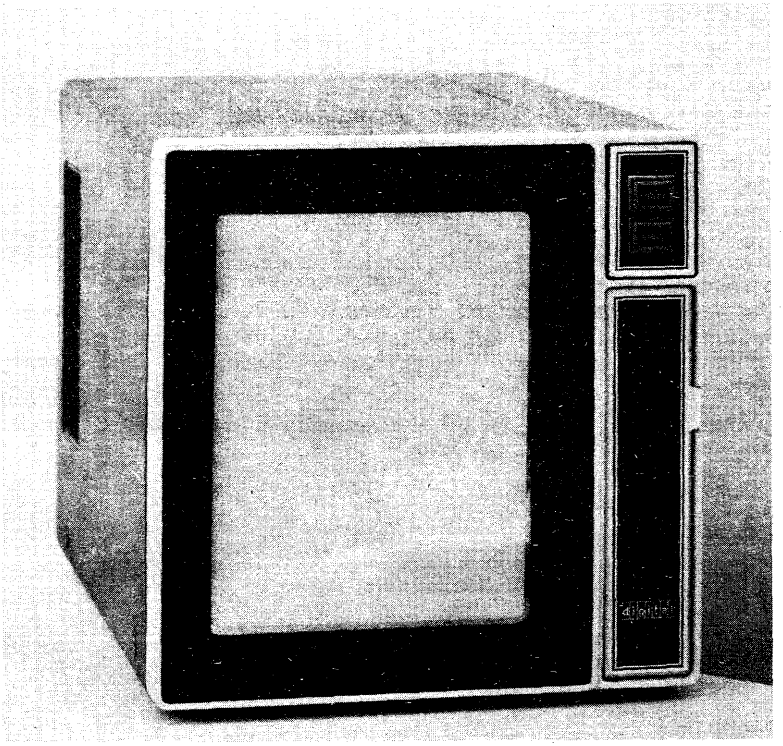
PART I
Chapter 4

Display Terminals

Several display options are available from Digital Equipment Corporation, including a storage display unit (VT01A), an oscilloscope (VR01A), a point plot display (VR14), and an alphanumeric display terminal (VT05).

Each of the units must be interfaced to the PDP-11 UNIBUS via an interface and control subsystem.

General characteristics and specifications of the various displays are included in this chapter. For information on the controls and programming see Chapter 9 for AA11-D control and Chapter 2 for the KL11 control.



VT01A Storage Display

4.2 STORAGE DISPLAY VT01A

The VT01A is a Tektronix Model 611 direct-view storage tube with a resolution of 400 stored line pairs vertically and 300 stored line pairs horizontally. Dot writing time is 20 μs, with a full screen erase time of 500 ms. The VT01 can display 30,000 discrete resolvable points.

The VT01A is interfaced to the UNIBUS and controlled via the AA11-A and AA11-D conversion subsystem (see Chapter 9).

4.2.1 Specifications

Resolution:	Equivalent to 400 stored line pairs along the vertical axis; 300 stored line pairs along the horizontal axis.
Erase Time:	0.5 seconds
Display Time:	Storage Mode-- 80 μs deflection time, 20 μs intensification time Non-Storage Mode-- 80 μs deflection time, 2 μs intensification time
Display Size:	8 1/4 Vertical x 6 5/8 Horizontal
Display Rate:	10 kHz max. (storage mode)
Dimensions:	11 5/8 inches wide 11 7/8 inches high 22 3/8 inches deep
Weight:	51 pounds
Environmental:	+32° F to 122° F operating temperature range 0% to 80% operating humidity range
Power:	120 VAC, 240 VAC-- 60Hz 210 VAC, 230 VAC-- 50Hz
Power Dissipation:	250 Watts

4.3 OSCILLOSCOPE VR01A

The VR01A, a modified Tektronix type Rm504 oscilloscope, provides accurate measurements in DC-to-450 kHz applications. It is a low-frequency, high sensitivity display and can be used for accurate curve plotting in the X-Y mode of operation.

For information concerning the control and programming see Chapter 9, (AA11-D subsystem).

4.3.1 Specifications

Display Area:	8 x 10cm
Height:	7 in.
Width:	19 in.
Rack depth:	17 in.
Net Weight:	30 lbs.
Display Rate:	45 kHz max. 50 Hz min.
Display Time:	20 μs deflection time 2 μs intensification time
Intensification Levels:	2

4.4 POINT PLOT DISPLAY VR14

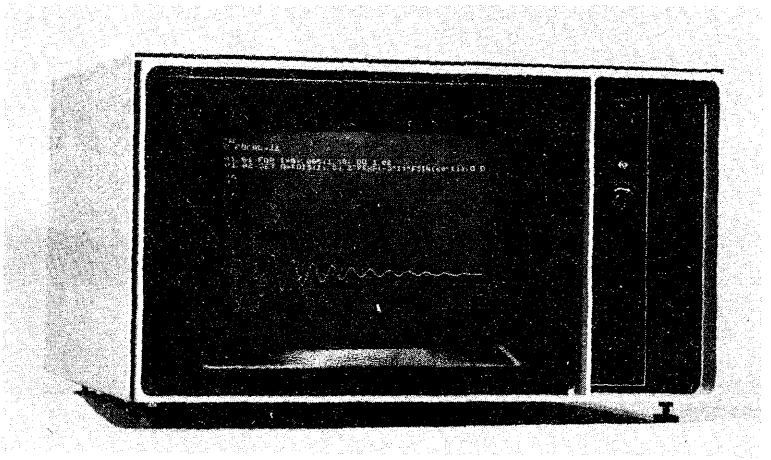
The VR14 is a completely self-contained CRT display with a 6.75 x 9-inch viewing area in a compact 19-inch package. The VR14 requires only analog X and Y position information with an intensity pulse to generate sharp, bright point plot displays. Except for the CRT itself, the unit uses all solid state circuits with high speed magnetic deflection to enhance brightness and resolution. The intensity pulse may be time multiplexed or gated by a separate input to allow the screen to be timeshared between two inputs. The display unit is available in rack-mountable or stand alone models.

The VR14 is interfaced to the UNIBUS and controlled through the AA11-D digital/analog conversion subsystem (See Chapter 9).

A two-color display (VR20) is also available. It is used with the AA11-E and AA11-D d/a conversion subsystems.

4.4.1 Specifications

Physical:	Height 10 1/2 in. Width 19 in. Depth 17 in. Weight 75lbs. Viewable Area 6-3/4 X 9 in.
Spot Size:	≤20 mils inside the usable screen area at a brightness of 30 foot-lamberts.
Jitter:	≤± 1/2 spot diameter
Repeatability:	≤± 1 spot diameter (Repeatability is the deviation from the nominal location of any given spot)
Gain Change:	From a fixed point on the screen, less than ± 0.3 percent gain change for each ± 1 percent line voltage variation.
Temperature Range:	0° to 50° C operating
Relative Humidity:	10% to 90% percent noncondensing



VR14 POINT PLOT DISPLAY

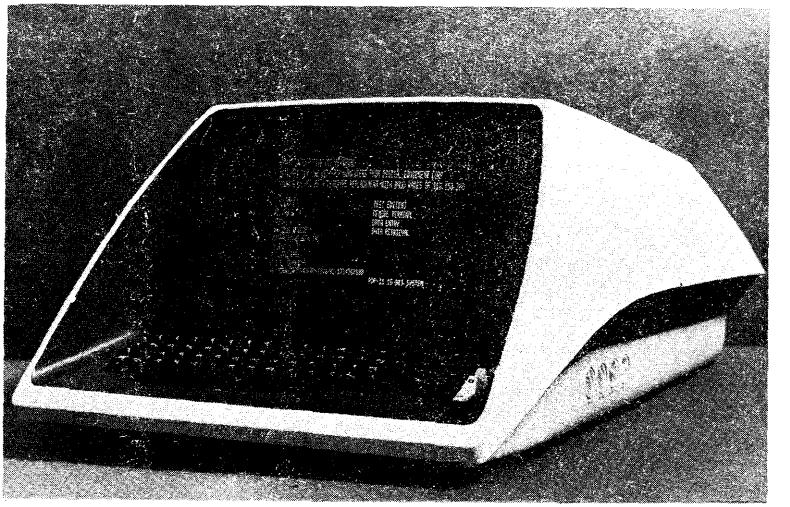
Brightness:	≥ 30 footlamberts: measured using a shrinking raster technique.
Linearity:	Maximum deviation of any straight line will be ≤ 1 percent of the line length measured perpendicular to a best fit straight line.
Deflection Method:	Magnetic (70° diagonal deflection angle)
Focus Method:	Electrostatic
Shielding:	CRT is fully enclosed in a magnetic shield.
Overload Protection:	Unit is protected against fan failure or air blockage by thermal cutouts.

Power:	115V ± 10% 230Vac ± 10% 50 or 60 CPS
Power Dissipation:	400 Watts

4.5 ALPHANUMERIC VT05 TERMINAL

The VT05 is a flexible, high-performance alphanumeric display terminal with a cathode ray tube display and communications equipment capable of transmitting data over standard phone lines and data sets at half or full duplex at rates up to 300 Baud.

It is controlled by the KL11, the same controller used with Teletype terminals. (See Chapter 8), or it may be used over a Bell 103A or equivalent modem.



VT05 ALPHANUMERIC TERMINAL

4.5.1 Specifications

	DISPLAY
Screen Size:	10 1/8' 7-5/8' 8 3/4 x 6 5/8
Characters/Line:	72
Number of Lines:	20
Characters Displayable:	1440
Contrast Ratio:	12:1
Type of Phosphor:	P4
Character Generator Method:	5 x 7 dot matrix
Deflection Type:	Magnetic
Deflection Method:	Raster Scan
Character Generator:	Read Only Memory (ROM)
Type of Memory:	MOS
Memorize Size:	ROM - 2240 bits Refresh Buffer 9816 bits
Display Refresh Rate:	60 times/sec or 50 times/sec synchronized to power line frequency
Character Set:	Upper case ASCII
Character Size:	.23 in. x .11 in.
Cursor:	Non-destructive, blinking

	KEYBOARD/CONTROLS
Type:	Electronic (wafer switch) USASCII 67 Layout Switch Selectable to transmit as a Model 33. 35 or as a Model 37
Controls	
Cursor:	Up, down, left, right, home up, home down
Erase:	to end of frame
Power:	On, off
Mode:	Remote, local
Transmission:	Full, half duplex

	MECHANICAL/ENVIRONMENTAL
Dimensions:	19"wide 12"high 30"deep
Weight:	55 lbs
Heat Dissipation:	800 BTU/hr. maximum
Operating Temperature:	40° -100° F 4.4° -37.8° C
Humidity:	10 to 95%

Weight:	55 lbs
Heat Dissipation:	800 BTU/hr. maximum
Operating Temperature:	40° -100° F 4.4° -37.8° C
Humidity:	10 to 95%

POWER INPUT

VT05A:	95-130 VAC, 60Hz ±2Hz, single phase
VT05B:	190-260 VAC, 60Hz ±2Hz
VT05C:	95-130 VAC, 50Hz ±2Hz
VT05D:	190-260 VAC, 50Hz ±2Hz
Power Consumption:	130 watts

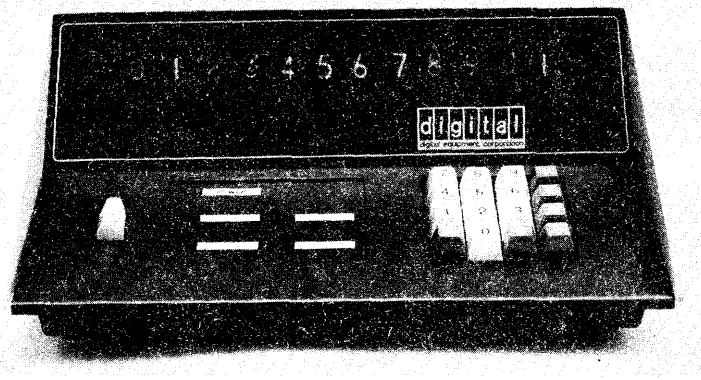
DATA TRANSMISSION

Type:	crystal-controlled, selectable speed; send receive 110, 150, 300 Baud
Controller:	KL11-A (110 Baud) KL11-B (150 Baud) KL11-C (300 Baud)

4.6 DEC-LINK TERMINAL RT01

DEC-link is a low-cost, self contained data entry device which is remotely locatable. It features Teletype and EIA serial line compatibility. DEC-link offers 16 unique keyboard characters which a monitoring computer may use for either numeric data or control functions. It can display up to 12 digits of decimal data (plus decimal point) as well as status indicators.

Data is entered via an integral 16-character keyboard; numeric data is displayed on "Nixie" * TUBES. The status indicators are used to indicate no n-numeric information such as 'repeat transmission", 'computer ready", etc. Four programmable status indicators are standard on DEC-link. The KL11 Control may be used with the RT01 for direct connection (see Chapter 2) or it may be used over a Bell 103A or equivalent Modem.



DECLINK TERMINAL

DEC-links usage may be defined entirely by software. Each character may be given significance according to the application. For instance, a key which represents 'Part Number"in a stockroom application may represent 'Employee Number " in a security system. DEC-links small size and weight (about the size of a typewriter) allow it to be moved from one location to another. DEC-links all solid-state design, coupled with a keyboard rated at 20 million operations guarantees long, trouble-free operation.

Connection to the computer may be made via standard 22 ga. 4-wire twisted pair cable or with a user supplied modem, over voice-grade telephone lines. DEC-link is hardware compatible with all of DECs comprehensive line of data communications equipment making available the full range of DEC computer power. The elimination of electro-mechanical parts and paper and ribbon replacements makes routine maintenance unnecessary.

4.6.1 Specifications

Line Voltage:	115 VAC, 230 VAC 47-62 Hz.
Power:	30W
Size:	15"W x 12"D x 6"H
Weight:	12 lbs.
Aux. Switches:	on-off
Display Options	
Lamps:	4 Status Indicators (programmed control)
Digits:	4,8, or 12 Nixie tubes
Decimal Point:	Programmable over 12 digits
	Control Functions
Clear Display:	Code $(100)_8$
Load Status Indicators:	Code $(120)_8$ to $(137)_8$
Input Levels:	20 MA TTY Isolated Current Loop or EIA RS232C
Receive Rate:	110 or 300 Baud
Character Format:	8 level asychronous serial ASCII 1 or 2 stop bits.
Data Output	
Output Levels:	Isolated Transistor switch capable of passing 20MA
EIA RS232 Signals:	Data Terminal Ready
	Transmitted Data
	Received Data
	Protective Ground
	Signal Ground
Transmission Rate:	110 or 300 Baud
Character Format:	8 level asynchronous serial ASCII
Character Rate:	10 Character/Second (110 Baud)
	30 Characters/Second (300 Baud)
Output Connectors:	4 lug Jones Strip (current loop)
	Cinch DB 25P (EIA)
Character Set	
Number of Characters:	16
Code:	ASCII 8 level
Character Codes:	ASCII 0 through 9
	A through F

PART I
Chapter 5

Disk Storage Devices

5.1 DISK ALTERNATIVES

Many mass storage alternatives are available to the PDP-11 user. Whether requirements are for fast access and fast storage, or for large storage with slower access times, DEC has a suitable disk system. For example DEC's fixed-head disk systems are suited for swapping type devices and scientific applications where fast access and fast transfer are important. The moving head systems are ideal for large storage requirements where fast access times are less vital.

Expandable disk-type mass storage systems are available for use with PDP-11 family computers. Any number of disk systems in any combination may be used with a PDP-11. Disk systems range from the RC11/RS64 which has basic storage of 65K words (expandable to 262K) to the RP11/RP02 which will store up to 80 million words in the 8-drive configuration. Each system consists of one or more disk drives and a control unit.

5.2 DECDISK MEMORY RC11/RS64

5.2.1 Introduction

The RC11/RS64 is a fast, low-cost, random access, bulk storage system. One RC11/RS64 combination provides 65,536 16-bit words of storage. Up to four RS64 disks can be controlled by one RC11 Controller for a total of 262,144 words of storage. Disk functions include: look ahead, read, write, and write check, as well as a "look ahead" register which indicates current disk position.

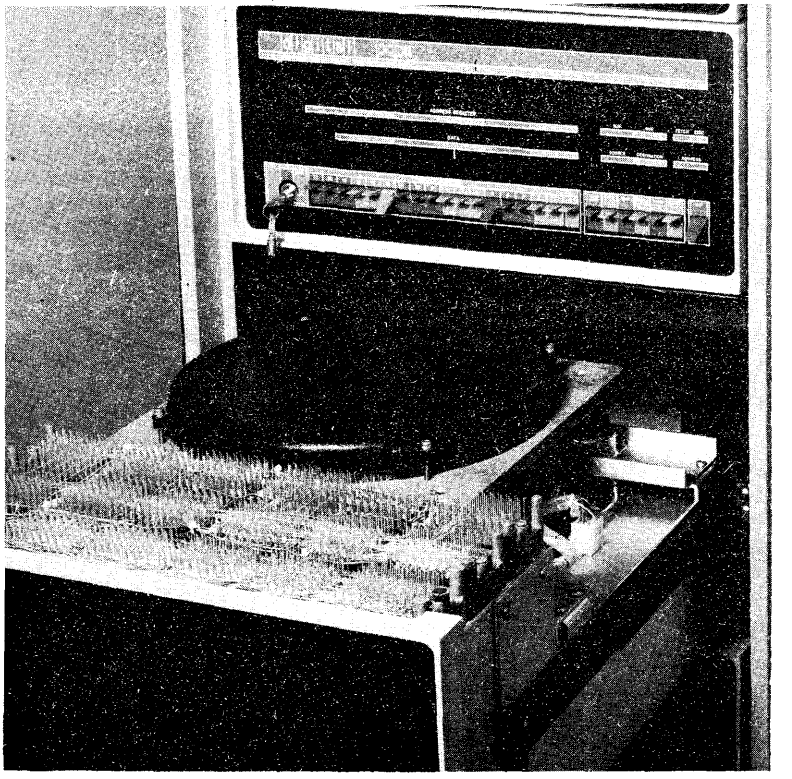
5.2.2 Operation

The RS64 disk stores data in a 32 x 16-bit word block format. Cyclic Redundancy Check (CRC) error detection is performed automatically by the controller on a block basis, the blocks being randomly addressable. A self-synchronizing, phase-lock clock recovery system is used to ensure exceptional data reliability. This technique facilitates data recovery in the event of restart after a power failure or during periods of high shock or vibration.

Fast track switching time permits spiral read and write. Data may be read or written as 32-word blocks from one to 65,536 words. When the last address on a track or surface has been used, the RC11 Controller will automatically advance to the next track or to the first track of a new disk surface.

Each RS64 disk unit has a set of switches for Write protecting the disk. The Write Lock ENABLE/DISABLE switch determines whether protection is desired or not. If this switch is in ENABLE position, writing data on tracks selected by five switches is not allowed. The setting of five switches below the ENABLE/DISABLE switch forms a binary number that corresponds to the number of a track; when write protection is in effect, all tracks numbered from zero to the selected number (both inclusive) are write protected. Any attempt to write in a write protected area will result in an error indication by the controller.

Real-time look ahead is provided by the RC11 Controller for the processor. This feature lets the processor continuously monitor the current position of the disk and minimize latency.



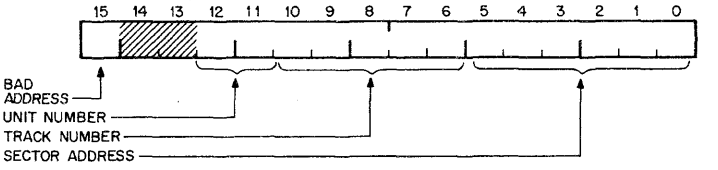
RC11/RS64 DECdisk

5.2.3 Programming

REGISTER	ADDRESS
Look Ahead Register (RCLA)	777440
Disk Address Register (RCDA)	777442
Disk Error Status Register (RCER)	777444
Command and Status Register (RCCS)	777446
Word Count Register (RCWC)	777450
Current Address Register (RCCA)	777452
Maintenance Register (RCMN)	777454
Data Buffer Register (RCDB)	777456

Look Ahead Register (RCLA)
This register always points to the sector address currently passing under read/write heads. Track number and unit number are copied from the disk address register (RCDA) into this register. RCLA is a real time register and the controller constantly updates it with new sector address read from the disk at appropriate times.

In order to insure that its contents do not change while being read by the processor the controller may skip updating RCLA when necessary. All sector address codes recorded on the disk are sequential and should appear in RCLA sequentially. However, if the time of update happens to coincide with the time of reading this register, the controller will skip updating and will correct itself at the next sector.

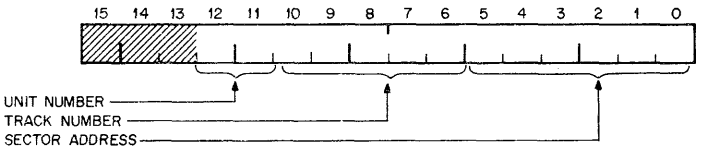


BIT	NAME	DESCRIPTION
15	Bad Address	Set at the time of sector address update if unit or track switching is in progress or an address error is encountered. RC11 takes approximately 8 milliseconds to switch from unit to unit and 300 microseconds to switch from track to track on a unit. This bit is read only and has no known initial state.
14-13	Not Used	
12-11	Unit Number	Indicates which of 4 disk units has been selected as follows: BIT 11 — BIT 12 — UNIT 0 — 0 = 0 1 — 0 = 1 0 — 1 = 2 1 — 1 = 3 These bits are same as RCDA 12-11 and read only at this address. They are cleared by initialize.
10-6	Track Number	Indicate which of the 32 tracks on currently selected disk is active. These bits are identical to RCDA 10-6. They are read only at this address and cleared by initialize.
5-0	Sector Address	Indicate the sector address just read from the selected disk. These bits are read only and have no known initial state.

Disk Address Register (RCDA)

Before any transfer between UNIBUS and RS64, RC11 must select and confirm a particular area on the disk. Each disk surface is divided into 64 sectors. Each sector has 32 data words. The disk address register is loaded with a number that selects one of four disk units, specific track and sector for transfer. To effect those transfers which require more than one sector, RCDA is incremented automatically after each sector has been transferred. After the last sector of a track $(77)_8$ has been operated on, first sector (sector 0) of the next track is selected due to incrementing. In a similar fashion after the last sector of the last track (track 37_8), first sector on the first track (track 0) of the next unit is selected automatically.

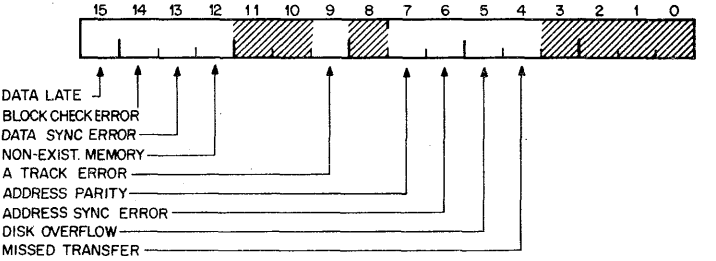
The program can specify or the controller may increment to a nonexistent disk unit. Response of the controller to such a situation is in the command and status register, RCCS.



BIT	NAME	DESCRIPTION
15-13	Not Used	
12-11	Unit Number	Decoded by the controller to select one of four disk units. Unit number is incremented by track number overflow. Unit number overflow sets disk overflow condition and indicates a non-existent disk status in RCCS if the word count did not overflow, i.e., desired number of transfers are not complete. This prevents wrap-around transfers from disk 3 to disk 0. These bits are read/write and are cleared by initialize.
10-6	Track Number	These bits are transmitted to the disk units for selecting a track; the track number is incremented by sector address overflow. When track number overflows, unit number in RCDA 12-11 is incremented. These bits are read/write and cleared by initialize.
5-0	Sector Address	Specify a sector for transfers. After the sector has been transferred RCDA is incremented. Sector address overflow increments track number in RCDA 10-6 These bits are read/write and cleared by initialize.

Disk Error Status Register

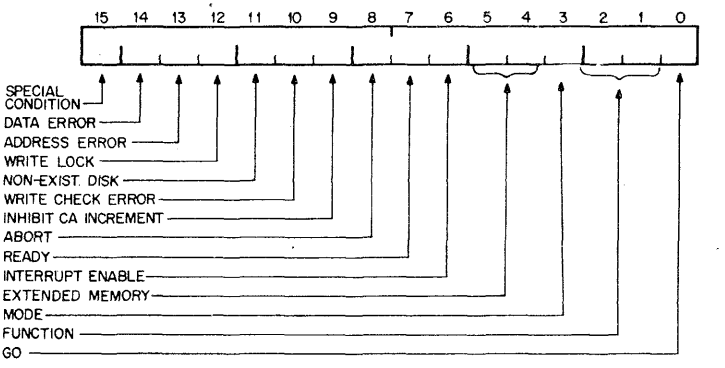
This register indicates error conditions that result from improper programming or equipment malfunction. When error conditions are sensed by the controller, any current operation in progress is aborted at appropriate time. This will cause an interrupt if interrupt enable bit (RCCS 6) is set. All error bits in this register are read only and cleared when a new RC11 operation is started. Initialize also clears this register.



BIT	NAME	DESCRIPTION
15	Data Late	RC11 requests control of the UNIBUS to conduct transfers. Such requests are made for each word. If, for any reason, request is not granted in time and RC11 requests another transfer, then this bit is set to indicate loss of data. Because RC11 operates on block structured data, word count and current address registers must be reinitialized and transfer restarted at the beginning of the sector.
14	Block Check Error	Set if the cyclic redundancy check (CRC) that is read back from the disk does not agree with the computed check on the data just read.
13	Data Sync. Error	Data formats on RC11 are chosen such that data block occurs between two markers on the mark track; data mark should be sensed first on mark track and data for that block should be complete before sensing an address mark on mark track. This bit is set if a violation is sensed by the controller.
12	Non-Existent Memory (NEM)	Set if RC11 initiates a UNIBUS data transfer and does not receive a slave sync. signal within a predetermined time after it asserted Master sync. This condition usually indicates no register or memory has been assigned to that address.

11-10	Not Used	
9	A Track Error	RS64 unit employs NRZI recording tech-inque that can be used to determine if a bit has been lost or extra bit read. If this happens on the clock track (A-track) then bit is set.
8	Not Used	
7	Address Parity	Set to indicate parity failure of the sector address code.
6	Address Sync	Set to indicate that a data mark signal from Mark track is received and the controller still has not detected end of sector address assembly. This situation may be due to missing the sync mark which precedes all sector address codes or spurious response from the Mark track.
5	Disk Overflow	If the disk address register (RCDA) overflows, the unit number changes from 3 to 0. This bit is set to indicate this situation. If word count overflow did not occur (i.e. more data transfers are to be made), this bit will also indicate non-existent disk (NED) condition by setting bit 11 in RCCS.
4	Missed Transfer	Set to indicate that RC11 did not make a non-processor request for data transfer since initiating a function and the disk revolved more than once.
3-0	Not Used	

Disk Control and Status Register (RCCS)



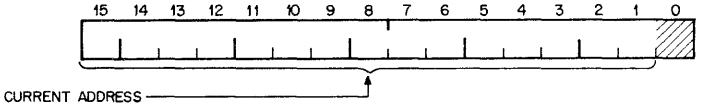
BIT	NAME	DESCRIPTION
15	Special Condition	Set to indicate that controller sensed an error condition. The exact error causing this bit to set can be found in bits 10-14 of this register and RCER. This bit is read only.
14	Data Error	Set to indicate that controller sensed a data error. Data error may be due to sync or cyclic redundancy check (CRC). The exact error can be found in RCER. This bit is read only and initialized to zero.
13	Address Error	Set to indicate that controller sensed an address parity or sync error. The exact error can be found in RCER. This bit is read only and initialized to zero.
12	Write Lock	Set to indicate that a write attempt was made on a write-protected area of the disk. This bit is read only and initialized to zero.
11	Non-Existent Disk	Set to indicate that disk address register (RCDA) is pointing to a non-existent unit or the disk unit number in RCDA has overflowed. Note that this bit will be "1"only when the word count register did not overflow so that last sector of the last disk unit can be operated on without getting an error status. This bit is read only and initialized to zero.
10	Write Check Error	Set if data read from the disk does not compare with the data on the bus during a write check function. Incrementation of RCCA and RCWC are inhibited as soon as failure occurs. However, controller reads the whole block (32 words) for cyclic redundancy check (CRC). This bit is read only and initialized to zero.
9	Inhibit CA Increment	If declared as "1,"data transfers with the UNIBUS will be performed without incrementing RCCA. This bit is read/write and initialized to zero.
8	Abort	If declared as "1,"any operation in progress is aborted. This bit is write only and initialized to zero.
7	Ready	Controller sets this bit to indicate completion (or abortion) of an operation and is ready for the next operation. This bit is read only and initialized to "1."

6	Interrupt Enable	Program interrupt will be allowed to occur only when this bit is "1." This bit is read/write and initialized to zero.
5-4	Extended Memory	Two most significant bits when 18 bit address is in effect. These two bits are logical extension of the current address register (RCCA). These are read/write and initialized to zero.
3	Mode	If declared as "1,"controller switches to maintenance mode. Signals received from RS64 are inhibited from activating the controller. Instead these signals will be taken from RCMN. This bit is read/write and initialized to zero.
2-1	Function	Specify the desired operation. Controller decodes these bits as follows:

Bit 2	Bit 1	Function
0	0	Look Ahead
0	1	Write
1	0	Read
1	1	Write Check

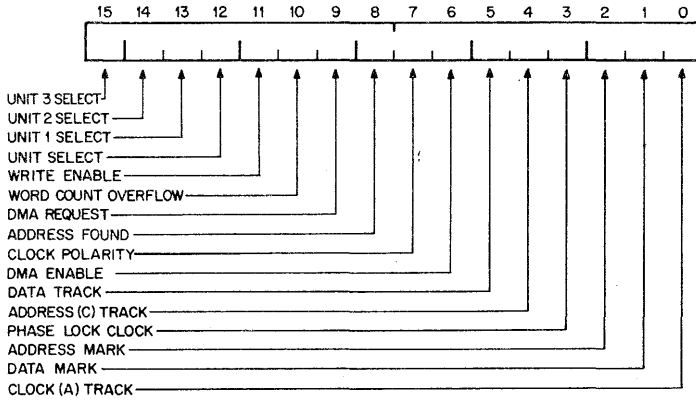
		These bits are read/write and initialized to zero.
0	Go	Setting initiates the function specified. Write only and initialized to zero.

Current Address Register (RCCA)



Before initiating an RC11 function program declares the address of the UNIBUS location with which the controller should start data transaction. All data transfers take place at even address boundaries (no byte capability). After each data transfer this register is incremented by two. When this register overflows, extended memory bits in RCCS are incremented. Bit 0 of this register is not used and remaining bits are read/write. Initialization clears this register.

Maintenance Register (RCMN)



This register is provided for diagnostic purposes only and does not participate in normal disk operations.

Data Buffer Register (RCDB)
All data transactions between RC11 and the UNIBUS take place through this register. All data read from the disk appears in this register either for transfer to the bus during read or comparison during write check. During write, data from the UNIBUS is first loaded into this register prior to writing on the disk.

As the last word obtained from the disk during read or write check operation is the block check or CRC word, this register contains the CRC word of the last block read when the operation is complete. This register is read only and cleared by initialize. It is not normally addressed except for maintenance and diagnostic programming.

5.2.5 Specifications

	Data Storage Capacity
Disks:	One RC11 can control up to four RS64 disks
Tracks:	Each RS64 has 32 data tracks
Blocks:	Each data track has 64 addressable blocks
Words:	Each block has 32 data words
Density:	Maximum recording density is 1800 BPI
Recording Method:	Self clocking one out of N. NRZI code
Words per disk:	63,536
Total Words:	262,144

	Data Transfer Rate	
	60Hz	50Hz
Word Transfer Rate:	16.0μs nominal	20.0μs nominal
Minimum Access Time: (read amp settling and track switching)	258μs nominal	258μs nominal

Average Access Time:	16.9ms	20.3ms
Maximum Access Time:	33.6ms	40.3ms

Priority Interrupt

Priority Level:	BR5 (selectable by plug in circuit chip)
Interrupt Vector Address:	210
Interrupt Caused by:	Function Complete Error Condition

NPR Transfer

Maximum Latency:	12μs; DRL is set and no further transfers occur
Environmental:	40°-120°F. operating temperature 20-80% relative humidity (non-condensing)
Shock:	5 g's, half-sine, 10ms
Vibration:	Suitable for office, industrial and large vessel operation. Disk unit is shock mounted.

Power Requirements

Voltage:	117/235 VAC ± 15%, single-phase, 47-63 Hz
Current:	For a 1-disk system: Starting current, 6 Amps; Nominal current, 2.2 Amps. For a 4-disk system: Starting current, 24 Amps, Nominal current, 8.8 Amps.
Power Supply:	Self-contained (+5VDC available in each RS64 for RC11).

Miscellaneous

Timing Tracks:	3, plus 3 spare (pre-recorded; can be used for data recovery if primary timing tracks are lost)
Write Lock Switches:	5 switches on each RS64 provide write protection of all binary track addresses up to and including the binary track address indicated by the switches.
Motor Bearing Life:	Expected operating life of at least 20,000 hours, under a standard computer operating environment.
Data Transfer Path:	UNIBUS (DMA); RC11 is bus master
Shipping Weight:	RC11, RS64, Power Supply: 50 pounds (uncrated).
Cable Length:	RC11/RS64 maximum bus length is 35 feet.
Installation:	
RS64:	10-1/2-inch panel height; mounts in DEC-type H960 cabinet. Self-contained; includes one RS64, one RC11, write lock, unit select, motor power control, and electronics power supplies.
RC11:	One system unit which mounts in the RS64 disk assembly. Power is supplied by the RS64.

5.3 DISK AND CONTROL RF11/RS11

5.3.1 Introduction

The RF11 Controller and RS11 Disk combine as a fast, low-cost, random-access bulk-storage package for the PDP-11. One RS11 and the RF11 provide 262,144 17-bit words (16 data bits and 1 parity bit) of storage. Up to eight RS11 disks can be controlled by one RF11 for a total of 2,047,152 words of storage.

The RF11/RS11 is unique in fixed head disks because each word is addressable. Data transfers may be as small as one word or as large as 65,536 words. Individual words or groups of words may be read or rewritten without any limits of fixed blocks or sectors, providing optimum use of both disk storage and main memory in the PDP-11 system.

The RS11 contains a nickel-cobalt-plated disk driven by a hysterisis synchronous motor. Data is recorded on a single disk surface by 128 fixed read/write heads.

5.3.2 Operation

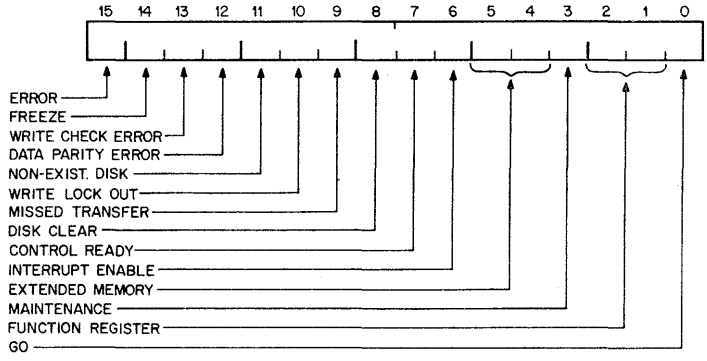
Fast track switching time permits spiral read or write. Data may be written in blocks from 1 to 65,536 words. The RF11 control automatically continues on the next track, or on the next disk surface, when the last address on a track or surface has been used.

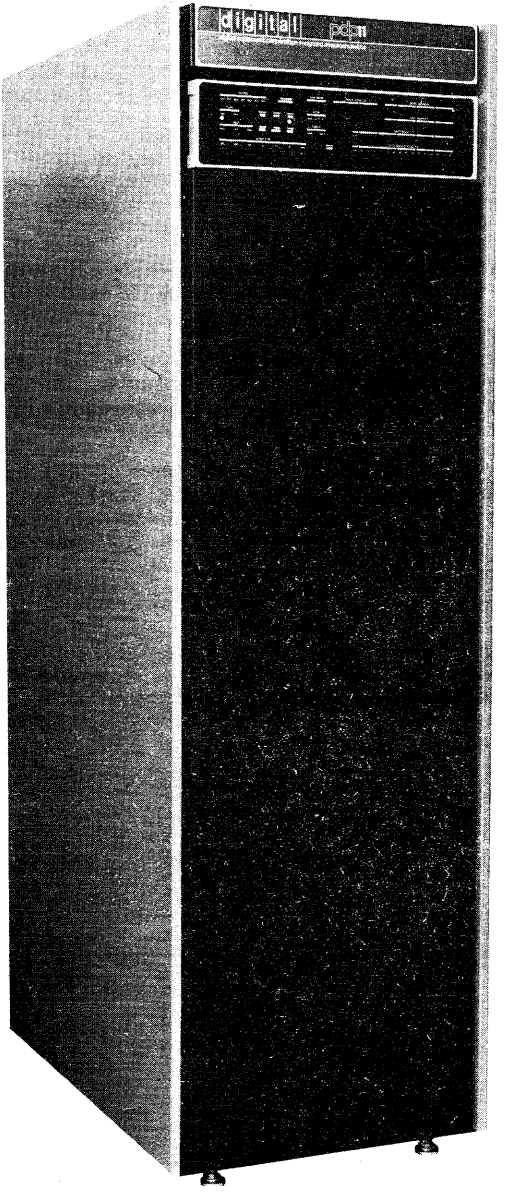
The Disk stores data words in a 22-bit format which includes guard bits and a sync bit to operate the self-clocking logic of the RS11 Disk logic. The sync bit adjusts the timing of the data strobing to ensure proper recovery of each word of data. The RS11 has a redundant set of timing tracks, recorded exactly in phase with the primary timing tracks.

5.3.3 Programming

REGISTER	ADDRESS
Disk Control Status (DCS)	777460
Word Count (WC)	777462
Current Memory Address (CMA)	777464
Disk Address (DAR)	777466
Disk Address Ext. Error (DAE)	777470
Disk Data Buffer	777472
Maintenance (MA)	777474
Address of Disk Segment (ADS)	777476

Disk Control Status Register (DCS)





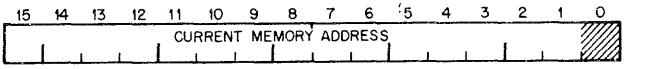
RF11/RS11 DECDISK

BIT	NAME	DESCRIPTION
15	Error (ERR)	Logical OR of DCS 14-9; Read only
14	Freeze (FRZ)	Logical OR of DAE 15-10; Read only
13	Write Check Error (WCE)	Set if the word read from memory and the word read from the disk differ during a Write Check. Read only.
12	Data Parity Error (DPE)	Set if the parity bit computed for a word does not agree with bit read from the disk. Read only.
11	Non Existent Disk (NED)	Set if DAE 4-2 are set (by the program or by sequencing from the previous value) to an address for which no disk is implemented, or if the disk address overflows (DAE 5 is set). Read only.
10	Write Lock Out (WLO)	Set if the control attempts to write into a disk segment with the write lock switch ON. Read only.
9	Missed Transfer (MXF)	Set if the control has held NPR asserted for 3 revolutions and has not received bus control. Read only.
8	Disk Clear	Initilizes (PWR CLR) the disk control. Clears all bits of DCS, CMA, WC, DAT, DAE, and DBR. Write only.
7	Control Ready (RDY)	Set if the control is ready to perform function. Can be examined by a TSTB instruction. Read only.
6	INTR ENB	If set, allows ERR (DCS 15) or Ready to cause an interrupt. Read/Write
5-4	Extended Memory (XM)	Drive BUS A 17-16 to select memory locations not in the first 32K words (64K locations). Read/Write
3	Maintenance (MA)	If set, causes the control to accept inputs from maintenance register instead of from disk. Read/Write
2-1	Function Register (FR)	Select one of three functions as shown in table. Remain unchanged during error halt for restarting. Read/Write

Bit 2	Bit 1	Function
0	0	No operation
0	1	Write
1	0	Read
1	1	Write Check

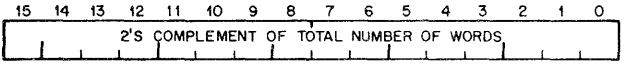
0	Go	Causes the processor to execute the function selected by the function register. Clears DCS15 unless FRZ (DCS14) is set, and clears DCS(13-9) Write only

Current Memory Address (CMA)



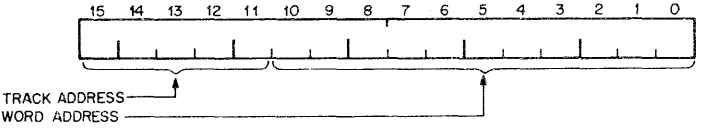
BIT	NAME	DESCRIPTION
15-1	Current Memory Address (CMA)	Selects the UNIBUS locations for the next data transfer. Must point to an even (word) location, so CMA00 is unimplemented and CMA01 is incremented after each transfer. Extended to full 18-bit addresses by XM bits (DCS 5-4.) Initially loaded with the starting address minus two. Read/Write

Word Count Register (WC)



BIT	NAME	DESCRIPTION
15-0	Word Count (WC)	Loaded with the 2's complement of the block length and incremented by 1 before each transfer. Overflow ends the function and causes Ready to be set. Limits block size to 65,536 words. Read/write.

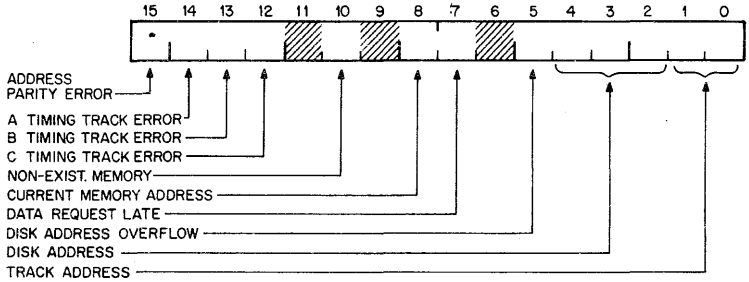
Disk Address Register (DAR)



BIT	NAME	DESCRIPTION
10-0	Word Address (WA)	Selects word on disk track for next transfer. Incremented after each transfer. Overflows into TA0 to cause spiral read or write last word of one track followed by the first word of the next track. Read/Write.

15-11	Track Address (TA)	Selects track on disk for current transfers. Initially set by program and incremented by WA overflow. Extended by TA 6-5 (DAE 1-0) to select one of 128 tracks. Read/Write

Disk Address Extension Error Register (DAE)



BIT	NAME	DESCRIPTION
15	Addr. Parity Error (APE)	Set if the computed address parity differs from the address parity read from the disk. Read only
14	A Timing Track Error (ATER)	Set if missing or extra bits are detected on timing track A. Read only
13	B Timing Track Error (BTER)	Same as ATER (DAE14) for timing track B. Read only
12	C Timing Track Error (CTER)	Same as ATER (DAE14) for timing track C. Read only
11	Unused	

NOTE

The NRZI recording method provides two-bit streams from each read head. In normal operation, bits are read alternately in the two streams; however, if a bit is dropped or an extra bit is read, two bits will appear in sequence in the same bit stream. DAE 14-12 indicates such an error on the corresponding tracks.

10	Non-Existent Memory (NEM)	Set when UNIBUS data transfer is made to a non-existent memory location or when the bus address register sequenced to a non-existent memory location and did not receive SSYN within 10μs. Read only
9	Unused	
8	Current Mem. Addr. (CMA INH)	Prevents CMA from incrementing to allow transfers to single-address devices. Read/Write

7	Data Request Late (DRL)	Set when the RF11 control is ready to transfer data and the previous data has not been transferred (the RF11 has had NPR asserted for 12 sec but is not Bus Master). Cleared when the control becomes Bus Master, or may be set or cleared by the program. DRL does not stop the current function and does not cause an interrupt; it is an indicator only. Read/Write
6	Unused	
5	Disk Addr. Overflow (DA OVFL)	Set if DA 02:00 overflows (Disk Address = 10). Causes NED (DCS11) to be set. Read only
4-2	Disk Address (DA)	Select one of eight disks. Incremented when TA 6-0 overflow, to continue spiral transfers on next disk.
1-0	Track Address (TA)	Extend TA 4-0 (DAR 15-11). Read/Write

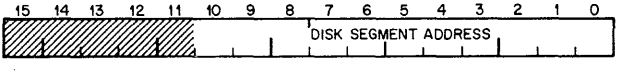
Data Buffer Register (DBR)

BIT	NAME	DESCRIPTION
15-0	Data Buffer Register (DBR)	Under RF11 control, used to transfer data on the UNIBUS. Accessible for program transfers for maintenance programs only. Read/Write

Maintenance Register (MA)

This register is provided for diagnostic purpose only and does not participate in the normal disk operations.

Address of Disk Segment Register (ADS)



BIT	NAME	DESCRIPTION
15-11	Unused	
10-0	Address of ADS	This register allows the user to read the real-time word address of the disk. The contents of the ADS will indicate the address or the address + 1 of the data passing under the heads. The ADS register will contain the last address of the track while while the disk is passing through the gap and buffer region. Read only

5.3.5 Specifications

Data Storage Capacity

Disks:	One RF11 can control eight RS11 disks
Tracks:	Each RS11 has 128 data tracks.
Words:	Each data track includes 2048 data words.
Word format:	Data words are recorded in 22 bits
Density:	Maximum recording density is 1900 BPI
Recording Method:	NRZI
Words per Disk:	262,144
Total Words:	2,097,152

Data Transfer Rate

	60-Hz Power	50-Hz Power
Word Transfer Rate:	16.0μsec	19.2μsec
Minimum Access Time: (read amp settling for track switching)	258μsec	258μsec
Average Access Time: (approximately 1/2-revolution)	16.9ms	20.3 ms
Maximum Access Time:	33.6ms	40.3 ms

Priority Interrupt

Priority Level:	BR5 (selectable by plug in circuit chip)
Interrupt Vector Address:	204
Interrupt Caused by:	Function Complete Error (DCS 15 Set)
Maximum Latency:	12μs: DRL (DAE7) is set and no further transfers occur for one disk revolution.
Maximum Delay:	3 disk revolutions: MXF (DCS9) is set and operation halts.

Environmental Requirements

Temperature (Operating):	65° to 90° F
Relative Humidity (Operating):	20% to 55% relative
Condensation (Operating or Storage):	none
Vibration/Shock (Operating):	Good isolation is provided. To prevent data errors, extreme vibrations should be avoided while the RS11 is transferring information.

Power Dissipation:

Dependent on the number of disks in the system. Varies from 0.75 kW (2550 BTU/hr) for a 1-disk system to 2.42 kW (8230 BTU/hr) for an 8-disk system.

Power Requirements

	RS11 Motor Power
Voltage: 117/235 ± 10%VAC	117 VAC

(A stepdown autotransformer is provided for 235-VAC operation.)

Phase:	Single
Frequency:	50 ± 2Hz or 60 ± 2Hz
Frequency Stability:	0.1 Hz/sec maximum drift (A constant-frequency motor-generator set or static AC/AC inverter should be provided for installation with unstable power sources.)
Current:	For a 1-disk system: Starting current, 14 Amps; Nominal current, 6.5 Amps. For an 8-disk system: Starting current, 81 Amps; Nominal current, 21 Amps. Lower starting currents can be realized if disks are sequenced.
Power Supplies:	Self contained in cabinet with controller. Also includes line filter with each disk.

Miscellaneous

Self Clocking:	The RS11 disk employs self-clocking logic for reliable data recovery. Each word is logically located relative to the timing track.
Timing Tracks:	3 plus 3 spare (pre-recorded; can be used for data recovery if the primary timing tracks are lost).
Write Lock Switches:	Sixteen switches on each RS11. Each switch controls the write protection for one 8-track (16,384 word) segment. WLO (DCS 10) is set if a write function addresses a locked-out segment.
Data Transfer Path:	UNIBUS (DMA); RF11 is Bus Master
Shipping Weights:	RF11, RS11, power supplies and cabinet: 590lbs (crated), 500lbs (uncrated) RF11, RS11, RS11B, power supplies and cabinet: 690lbs (crated), 600lbs (uncrated) RS11D, RS11B, RS11C, motor controllers and cabinet: 690lbs (crated), 600lbs (uncrated)

Number of Disks Desired	RS11	RS11B	RS11C	RS11D
1	1	0	0	0
2	1	1	0	0
3	1	1	0	1
4	1	2	0	1
5	1	2	1	1
6	1	2	1	2
7	1	3	1	2
8	1	3	2	2

The RS11 includes a standard mounting cabinet (71-7/16 in.hx30 in.dx21-11/16 in.w) and 855 Power Control Unit. RS11B designates the second disk in a cabinet, RS11C designates the third. The RF11 control and all power supplies mount in the first cabinet. Other devices should not be mounted in disk cabinets. The suffix (A) designates 50-Hz power. The RS11D includes a standard mounting cabinet and is the first disk in the second or third cabinet (cabinet has full front door; no indicator panels).

5.4 DECPACK DISK CARTRIDGE SYSTEM - RK11-C/RK02, RK03

5.4.1 Introduction

The DECpack cartridge disk drive and control is a complete mass storage system, offering an economical solution for large volume, random-access data storage. The system includes a modular mass storage device utilizing removable disk cartridges and a complete easy-to-program control.

The DECpack is available in two models: The RK02 drive with over 600,000 words per drive; and the RK03 drive with over 1.2 million words of storage per drive.

The DECpack is ideal where a large volume of programs and data are developed and maintained for one or more users. When used with PDP-11 software such as the Disk Operating System or RSTS-11 System, DECpack offers the flexibility of permitting each member of a group of users to maintain his own private program and data files. It is expandable up to 4.8 million words (RK02) or 9.6 million words (RK03) per controller.

5.4.2 Operation

The removable disk cartridge offers the flexibility of virtually unlimited off-line capacity with rapid transfers of files between on-line and off-line without copying operations. It utilizes a cartridge similar to the IBM 2315, but with 12 sectors.

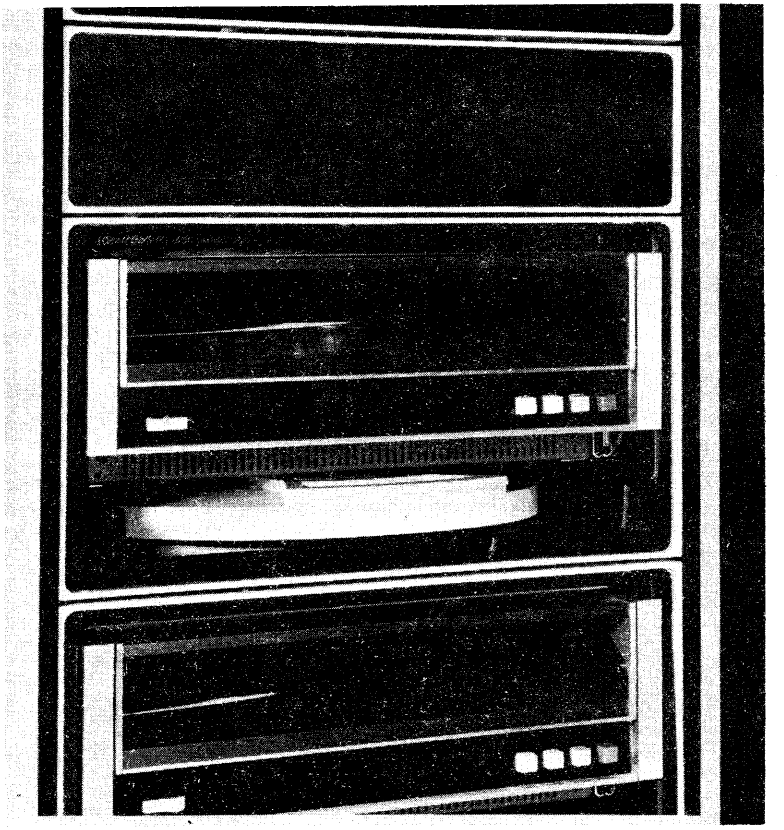
Average total access time on each drive is 90 milliseconds. On expanded systems, operations are overlapped for efficiency; one drive may read or write while one or more additional drives are seeking new head positions for the next transfer. All data transfers utilize the Non-Processor Request facility during transfers.

Each disk is permanently mounted inside a protective case that automatically opens when inserted in the disk drive. While on-line, dust contamination is prevented by a highly-efficient continuous "absolute" air filtration system.

The DECpack provides accurate data storage and transfers by means of a write check function, correct cylinder verification by hardware, hardware checksum, and hardware maintenance features. There are no mechanical detents, thus a major source of wear and critical adjustment is eliminated.

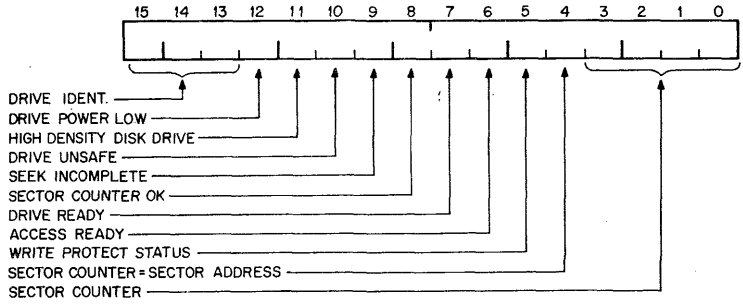
5.4.3 Programming

REGISTER	ADDRESS
Drive Status Register (RKDS)	777400
Error Register (RKER)	777402
Control Status Register (RKCS)	777404
Word Count Register (RKWC)	777406
Current Bus Address Register (RKBA)	777410
Disk Address Register (RKDA)	777412
Maintenance Register (RKMR)	777414
Data Buffer Register (RKDB)	777416



DECPACK DISK CARTRIDGE SYSTEM

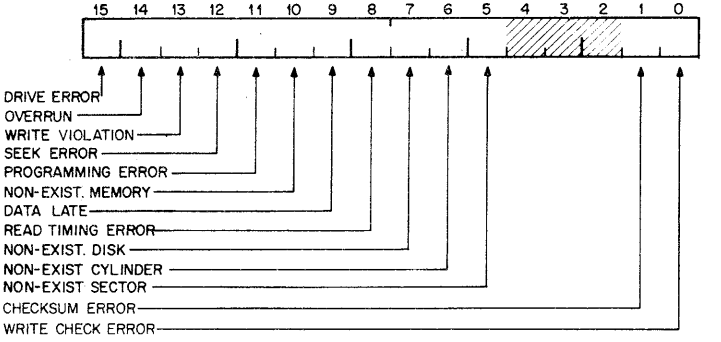
Drive Status Register (RKDS)
Contains the current selected drive status and current sector address. It is a read only register.



BIT	NAME	DESCRIPTION
15-13	Ident. of Drive (ID)	If an interrupt is caused as a result of a SEARCH COMPLETE (Bit 13 RKCS) or a SEEK INCOMPLETE (Bit 9 RKDS) these bits will contain the binary representation of the logical drive number that caused the interrupt.
12	Drive Power Low (DPL)	Set when an attempt is made to initiate a new function or a function was actively in progress when the control sensed a loss of power to one of the disk drives. This bit is normally accompanied by bit 15 RKER (DRE) and is reset by a BUS INIT or a CONTROL RESET function.
11	High Dens. Drive (HDEN)	Set to identify the selected disk drive as an RK03 and reset to identify the selected disk drive as an RK02.
10	Drive Unsafe (DRU)	Indicates that an unusual condition has occurred in the drive and it is unable to properly perform any operations. Putting the RUN/LOAD switch in the LOAD position will reset the condition. If, upon putting the RUN/LOAD switch back to the RUN position the condition reoccurs the drive or associated power supply is inoperative and corrective maintenance procedures should be begun. Normally accompanied by bit 15 RKER.
9	Seek Incomplete (SIN)	Indicates that due to some unusual condition a SEEK function was not completed within 180ms of initiation. A DRIVE RE-

		SET function clears this condition. This bit is normally accompanied by bit 15 RKER
8	Sector Counter OK (SOK)	Indicates that the selected drive sector counter (Bits 0-3 RKDS) is not in the process of changing and is ready for examination.
7	Drive Ready (DRY)	Indicates that the selected disk drive is in the following condition: a) properly supplied with power b) loaded with a disk cartridge c) door is closed d) LOAD/RUN switch is in the RUN condition e) the disk is spinning f) the heads are properly loaded g) the disk is not in a DRU condition (Bit 10 RKDS)
6	Access Ready (ARDY)	Indicates that the selected drive head mechanism is not in motion and the drive is ready to accept a new function.
5	Write Protect Status (WPS)	Set when the selected disk is in WRITE PROTECTED mode
4	SC = SA	Indicates that the disk heads are currently positioned over the disk addresses currently held in bits 0-3 RKDA
3-0	Sector Counter (SC)	Indicates the current sector address of the selected drive. This is the look ahead and will work for any disk cartridge with up to 16 sectors. Sector address 00 is defined as the sector which follows the sector that contains the index pulse. This is an important consideration when using the R/W ALL mode of operation.

Error Register (RKER)
(This is a read only register)

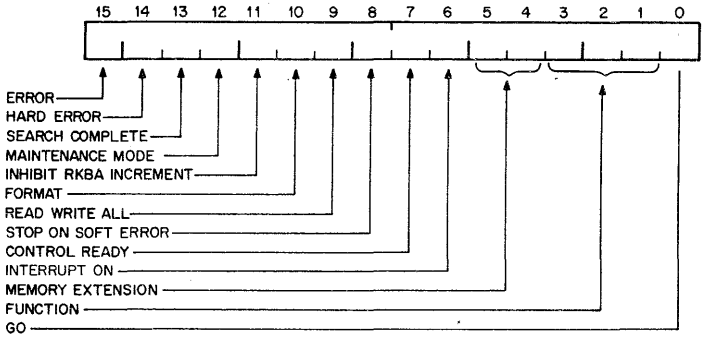


BIT	NAME	DESCRIPTION
15	Drive Error (DRE)	Set when an attempt is made to initate a function, or when a function is actively in progress, while the selected drive is not ready or in some error conditon or if any of the drives in the system senses a loss of either AC or DC power. If this bit is found set the RK03 should immediately be referenced to discover the cause of the conditon.
14	Overrun (OVR)	During a READ, WRITE, RD/CHK or WT/CHK, operations on sector 13_8 surface 1 of cylinder address 312_8 were finished and the RKWC had not yet overflowed. This essentially is an attempt to overflow out of a disk drive.
13	Write Violation (WLO)	Set if an attempt is made to write on a disk which is currently being write protected.
12	Seek Error (SKE)	Set if the disk head mechanism is not properly positioned while executing a normal READ, WRITE, RD/CHK or WT/CHK function.
11	Programming Error (PGE)	The R/W ALL bit (Bit 9 RKCS) or the FMT bit (Bit 10 RKCS) were set while initiating some function other than a READ or WRITE.
10	Non-Existent Memory (NXM)	Set if memory does not respond within 20μs of the time when the RK11 becomes Bus Master during a DATI or DATO NPR sequnce. Because of the speed of the RK03 disk drive, it is likely that if a NXM does occur it will be accompanied by a DLT (Bit 7 RKER).
9	Data Late (DLT)	Set when an NPR sequence is initiated before the previous one has completed.
8	Read Timing Error (RTE)	Two or more consecutive read clock pulses were dropped by the disk drive.
7	Non-Existent Disk (NXD)	An attempt was made to initiate a function on a non-existent drive.
6	Non-Existent Cylinder (NXC)	An attempt was made to initiate a function on a cylinder larger than 312_8 .
5	Non-Existent Sector (NXS)	An attempt was made to initiate a transfer on a sector larger than 13_8.
4-2	Unused	
1	Checksum Error (CSE)	Set while performing a RD/CHK or READ

		function as a result of faulty recalculation of the checksum. Cleared at the initiation of any new function. This is a soft error.
0	Write Check Error (WCE)	Indicates that an error was encountered during a WT/CHK function as a result of faulty bit comparison between disk data and memory data. Clears at the initiation of a new function. This is a soft error.

Note: Bits 5 through 15 are all hard errors. They clear only by a BUS INIT or a CONTROL CLEAR function.

Control Status Register (RKCS)

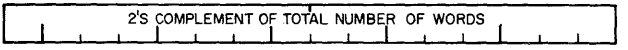


BIT	NAME	DESCRIPTION
15	Error	Set when any bit in the RKER is set. Processor reaction is dictated by Bits 6 and 8 RKCS. This read-only bit clears if all the bits in the RKER are cleared and if Bit 14 RKCS is cleared.
14	Hard Error (H.E.)	Set when any of Bits 5-15 RKER are set by the control. Stops all controller action and processor reaction as dictated by bit 6 RKCS. This READ ONLY bit, along with bits 5-12 RKER, is cleared only by a BUS INIT or a CONTROL RESET function.
13	Search Complete (SCP)	Signifies that the previous interrupt was caused as a result of some previous SEEK or DRIVE RESET function. READ ONLY bit. Clears at the initiation of any new function.
12	Maintenance Mode	When set, will inhibit any signals from being transmitted to or from any disk drive and will permit diskless operation of the RK11. Used in conjunction with the RKMR.

11	Inhibit Inc. (INH BA)	Setting this bit inhibits incrementing the RKBA during a data transfer. This allows data to be transferred to or from any one bus address for the entire operation.
10	Format (FMT)	FORMAT Mode must be used only in conjunction with the normal READ and normal WRITE function. This mode is used to format a new disk pack or to reformat any sector that may have been erased or damaged due to control or drive failure. In the FORMAT mode the normal WRITE operation is altered only in that the servo positioner is not checked for proper position before the write operation. Under a normal WRITE the header is re-written each time the associated sector is written. In this mode, the normal READ operation is altered in that only one word is transferred to memory per sector; the header word. Therefore, a 3-word READ function in the FORMAT mode will transfer 3 contiguous header words to 3 consecutive memory locations for software checking. For a 200-word transfer, 200 consecutive header words from 200 consecutive sectors will be read, and so on.
9	Read Write All (R/W A)	Must be used only in conjunction with a READ or WRITE function. The drive performs part 1 of a normal SEEK function after which it searches for SC = SA. When found, the read amplifiers or write drivers are turned on and every 16-bits a word is transferred to or from memory until the RKWC overflows. This mode is used to simulate formats to be written or read on controllers other than the RK11.
8	Stop on Soft Error (SSE)	If a soft error is encountered while this bit is set: a. and Bit 6 RKCS (IDE) is reset, all controller action will stop at the end of the current sector). b. and Bit 6 RKCS (IDE) is set, all controller action will stop and a Bus Request will occur at the end of the current sector.
7	Control Ready (RDY)	Signifies that the control is no longer engaged in actively executing a function and is ready to accept a command.
6	Int. on Done Enable (IDE)	The control will issue a Bus Request and interrupt to vector address 220 if: 1. A function has completed its activity;

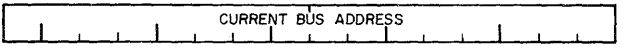
		2. A hard error is encountered; 3. A soft error is encountered and bit 8 RKCS is set.
5-4	Memory Extension (MEX)	Reserved for extended bus addresses and is used in conjunction with the RKBA. These bits make up a two-bit counter that increments each time the RKBA overflows. A bus DATO to these bits overrides any overflow from the RKBA. They are read/write.
3-1	Function	These bits indicate the binary representation of the function to be performed. The functions are: CONTROL RESET (000) WRITE (010) READ (010) WRITE CHECK (011) SEEK (100) READ CHECK (101) DRIVE RESET (110) WRITE LOCK (111)
0	Go	Write only bit. Indicates the function encoded in bits 1 through 3 of RKCS. Stays set until one control actually begins to respond to the go command.

Word Count Register (RKWC)



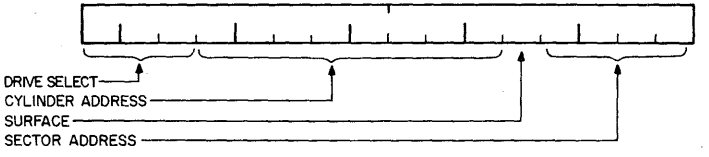
Contains the two's complement of the total number of words to be affected by a given function. It increments by one after each word transfer.

Current Bus Address Register (RKBA)



Contains the Bus Address to or from which data will be transferred. The register is incremented by two at the end of each transfer.

Disk Address Register (RKDA)



15-13	Drive Select (DR SEL)	Contains binary representation of the logical drive number currently being selected.
12-5	Cylinder Address (CYL ADD)	Contains binary representation of the cylinder address currently being selected. The largest valid number is 312_8.
4	Surface (SUR)	When active lower disk head is enabled.
3-0	Sector Address (SA)	Binary representation of the disk sector to be addressed.

This register maybe loaded only while the RK11 is in the ready state.

Maintenance Register (RKMR)
This register is provided for diagnostic purposes only and does not participate in the normal disk operations.

5.4.4 Cross Cylinder Operation
Surface 0 is defined as the upper surface and is active when RKDA 04 is reset. If a transfer is initiated that requires an overflow from surface 0, the control will automatically change to sector 0 of surface 1. If a transfer is initiated that requires an overflow from surface 1, the control will automatically move the heads to the next contiguous cylinder, check for proper head positioning, and continue the transfer on sector 0 and surface 0 of the new cyclinder. An attempt to overflow out of the last sector of the last cylinder will result in an error condition.

At the end of any transfer the RKDA is automatically incremented.

5.4.5 Hardware Poll
The control is capable of having any or all of the drives performing a SEEK or DRIVE RESET operation at any one time. A HARDWARE POLL feature will identify the logical drive number in bits 13, 14 and 15 of the RKDS of any drive that has completed a SEEK or DRIVE RESET operation and cause an interrupt if bit 6 RKCS is set (IDE) and the control is in the READY state (bit 7 RKCS is set) and the control was not already attempting to cause an interrupt as a result of some other operation. This will occur even if Bit 6 RKCS (IDE) was not set when first initiating the SEEK or DRIVE RESET function. If two or more drives complete the function simultaneously, the control will interrupt once for each drive and identify each one in turn in the RKDS. Care should be taken in this situation to raise the processor interrupt status to a level equal to or greater than that currently held by the RK11 or else a second interrupt will occur immediately after the first and the end result will be that the interrupt service routine has been interrupted. This situation will also occur if an attempt is made to initiate a SEEK to an address that the drive is already at since one interrupt will occur as a result of the SEEK or DRIVE RESET function having been successfully initiated and another to report that the heads have reached their destination, which will occur immediately because the heads are already there.

5.4.6 Interrupts
Because of the format structure of the RK11-C, any interruption of a write sequence cannot be tolerated until the end of the sector because this would result in essentially an unformatted disk. Therefore, any outside intervention of this operation is held off until the end of the current sector, which includes the CONTROL RESET function and the PROCESSOR or BUS INITIALIZE signals. Therefore, all

those functions, such as CONTROL RESET, SEEK and WRITE LOCK, which normally take only a few microseconds to initiate can actually take up to 3.3ms if initiated while writing. For this reason the SEEK and WRITE LOCK functions will cause an interrupt (if bit 6 RKCS is set) as soon as the function has been successfully initiated. The CONTROL RESET, which cannot cause an interrupt under any circumstances, can, therefore, take up to 3.3ms to complete.

5.4.7 Specifications

	RK02 Drive	RK03 Drive
1 disk/drive 203 cylinders/drive:	128 data words/sector	256 data words/sector
2 surfaces/drive:	1536 data words/track	3072 data words/track
12 sectors/track:	307,200 data words/ surface	614,400 data words/surface
1 to 8 drives/control:	614,400 data words/ drive	1,228,800 data words/ drives

Access Times (including head settling; typical):

Track to track:	15ms
Average random move:	70ms
Average rotation delay:	20 ms
Data Transfer Rate:	22.2 μ sec per word for RK02 drive 11.1 μ sec per word for RK03 drive
Transfer Path:	Non-Processor Request (NPR) Direct Memory Access
Minimum Block Size:	One sector (128 words for RK02 drive; 256 words for RK03 drive)
Minimum Transfer:	1 word
Density:	1100 BPI max. for RK02 drive 2200 BPI max. for RK03 drive
Speed:	1500 RPM
Environmental Requirements:	60° to 90° F and 20% to 80% relative humidity
Control:	Model Designations RK11-CA 117V +10% 50/60Hz RK11-CB 235V +10% 50/60Hz
Bus Priority Level:	BR5
Interrupt Vector Address:	220

Clocks

6.1 PROGRAMMABLE REAL TIME CLOCK KW11-P

The KW11-P provides programmed real time interval interrupts and interval counting in several modes of operation. Its major feature's are a 16-bit synchronous binary counter, a 16-bit data buffer, a 9-bit control register, four program-selectable count rates (including 2 crystal-controlled rates of 100 KHZ and 10KHZ line frequency, and one external clock input with a Schmitt trigger input.)

6.1.2 Operating Modes

MODE 0, the single interrupt mode, resets the Counter to zero and stops the clock on underflow or overflow.

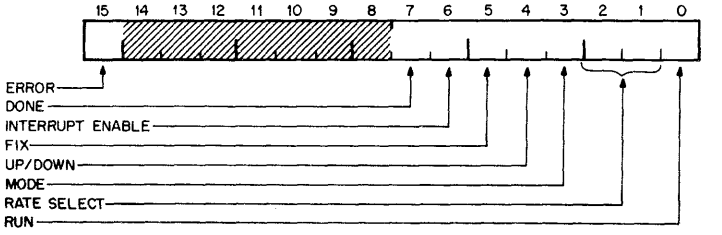
MODE 1, the repeated interrupt mode, reloads the Counter from the Count Set Buffer and restarts the clock on underflow or overflow. This allows repeated interrupts at program specified time intervals.

A third mode utilizes the Counter as an external event Counter with the count-up and external count rate enabled.

6.1.3 Programming

REGISTER	ADDRESS
Control and Status Register	772540
Count Set Buffer Register	772542
Counter	772544

Control and Status Register



BIT	NAME	DESCRIPTION
15	Error	Detects an error condition in Mode 1 operation where a second underflow or overflow of the COUNTER occur before the interrupt of a preceding underflow has been serviced. This bit is cleared by program It cannot be set by program.
14-8	Unused	
7	Done	Indicates an underflow has occurred. Set on underflow or overlfow and cleared by program or INIT.
6	Interrupt Enable	Provides a signal to the interrupt control logic of the KW11-P to allow generation of a bus request of COUNTER underflow or overflow. Set by program and cleared by program or INIT.
5	Fix	Maintenance bit, allowing single clocking of the counter. Setting clocks the counter by one count. CLOCKED by program control. Write only.
4	Up/Down	Selects count-up or count-down input of the COUNTER. When cleared, as for normal interrupt operation (single or repeated), the count-down input is selected. When set, the count-up input is used.
3	Mode	Selects one of two interrupt modes. When set, enables MODE 1: the repeated interrupt mode. When cleared, MODE 0 is selected for single interrupts. Set by program and cleared by program or INIT.
2,1	Rate Select	The RATE SELECT bits provide the selection of 1 of 4 available clock rates. The two bits are set by program and cleared by program or INIT.

BIT 02	BIT 01	Rate
0	0	100K Hz
0	1	10K Hz
1	0	Line Freq
1	1	External

0	Run	The RUN BIT controls the strobe input of the count rate multiplexer. When set, it gates the selected rate to the clock input of the COUNTER. RUN is cleared on underflow or overflow in MODE 0 operation and by INIT in all other cases.

Count Set Buffer Register (Write Only)
This is a 16-bit register used for storage of the interval count. It allows automatic reloading of the COUNTER in MODE 1 operation. This buffer is set by program and cleared by program or INIT. (MODE 0 operation clears the buffer on underflow.)

Counter (Address: 772544)
The Counter is a 16-bit, synchronous, binary counter clocked at one of four program-selectable rates. It serves in either a count-up or count-down mode. Underflow or overflow initiates the interrupt sequence. The Counter contents may be read while in operation. The contents are cleared on clock underflow or overflow in MODE 0 operation and by INIT.

A third mode utilizes the Counter as an external event counter with the count-up mode and external count rate enabled.

Priority Level:	BR6 (standard)
Interrupt Vector:	104
Programmable	
Count Rates:	2 crystal-controlled rates of 100 KHZ and 10 KHZ
	1 line frequency
	1 external clock input
Operating Modes:	Single Interrupt
	Repeated Interrupt
	External Event Counter
	Non-Interrupt

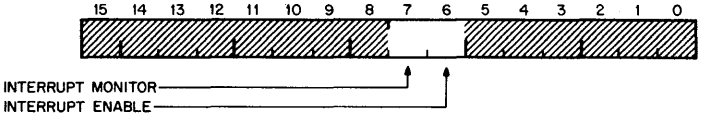
6.2 LINE TIME CLOCK KW11-L

The KW11-L accurately divides time into intervals for more efficient use of PDP-11 computer time. The intervals are determined by the line frequency, either 50 or 60 Hz. The accuracy of the clock period is that of the frequency source.

6.2.1 Programming

REGISTER — ADDRESS

Clock Status Register (LKS) — 777546



BIT	NAME	DESCRIPTION
15-8	Unused	
7	Interrupt Monitor	Set when line time clock changes from one to 0, and clears on a processor DATO to the LKS when D06 is clear. Set on processor INIT.
6	Interrupt Enable	Set on processor DATO to the LKS when D06 is a 1 and cleared on processor DATO to LKS when D06 is 0. Cleared on processor INIT. When set, enables interrupt. Monitor goes from 0 to 1. Program may read or write. Cleared by INIT.

6.2.2 Interrupt

During an interrupt, the interrupt monitor bit is at 1 (it had become a 1 either during the same line time clock transition that caused the interrupt, or during a previous transition.

Shown below is a program using the LKS in the interrupt mode. Its purpose is to enter the routine TIME after every N interrupts. When the main program is interrupted, it is directed to the vector address LKV which is 100, and then to LKV + 2 which is 102. The word in 100 is the adddress of the first instruction in the interrupt routine, and is consequently transferred into the processors program counter. The word in 102 is the new status register. The new status word contains the number 300 which indicates a priority level BR6 with all five condition codes, T, Z, N, V, and C equal to 0.

```
LKS = 777546

LKV = 100

MAIN:   MOV # N, CNTR
        MOV # 100, LKS          ENB INTR
        ...
        ...
LKV:    LK SERV
         300
LKSERV: DEC CNTR
        BEQ TIME
        RTI
TIME    MOV #N, CNTR
        ...
        RTI
```

6.2.3 Non Interrupt

The LKS may be used in the non-interrupt mode as well as in the interrupt mode. Shown below is a routine using the LKS in the non-interrupt mode. The program is designed to alternate between two program routines, each lasting for approximately the time periods between line clock changes which are either 16.67 or 20 ms. Each routine contains a program loop which lasts for a considerably shorter time duration than the period between line clock changes.

```
LKS = 777546

START:  CLRB LKS
SYNC:   TSTB LKS
        BPL SYNC
        CLRB LKS
```

```
ON:     TSTB LKS
        BPL ON
        CLRB LKS

OFF:    TSTB LKS
        BPL OFF
        CLRB LKS
        JMP ON
```

6.2.4 Specifications

Priority Level:	BR6
Vector Address:	100
Rate:	Same as line frequency; 50 or 60 Hz
Modes:	Interrupt and noninterrupt

The information on the DT11 bus switches is preliminary and subject to change.

System organization and option requirements are configuration-dependent. DEC engineering assistance is available and generally advisable in determining optimum utilization of this product and complete system requirements.

PART I
Chapter 7

Bus Extension Options

Because of the PDP-11's advanced UNIBUS architecture, a great variety of PDP-11 systems (shared peripherals, multiple processors) may be easily configured. Extending the UNIBUS so that any number of devices may be attached is accomplished with DB11-A bus extenders. Connecting two or more UNIBUSes, so that several concurrent uses may be made of one processor, is accomplished with a DT11-A bus switch. Shared peripheral or multiple-processor configurations are possible with a DT11-B switch.

7.1 INTRODUCTION

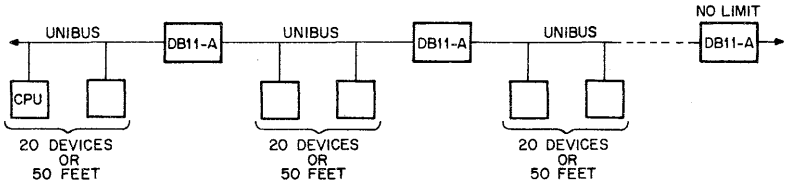


Figure 7-1 DB11 Bus Repeater

The Bus Repeater allows physical and electrical extension of the UNIBUS. Each Repeater allows a 50-foot extension in bus length, and will drive 18 extra unit loads (most PDP-11 options are one unit load).

The bus switches are basically either single throw or double throw switches for the UNIBUS. A section of bus, called the switched bus, containing any devices but a processor, can be connected to a main processor bus.

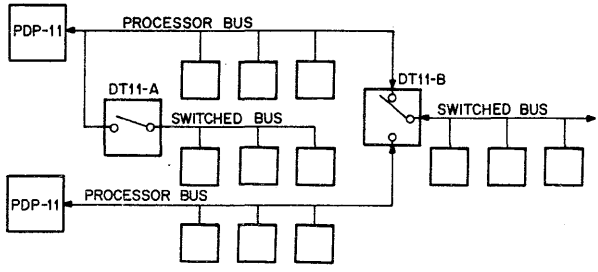
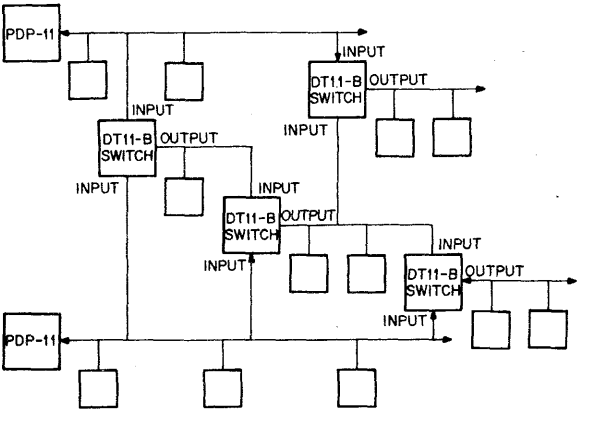


Figure 7-2 DT11 Bus Switches

The switches do not allow two processors to be connected together.

The switched bus may be thought of as the "output"of a bus switch, and the "inputs"are buses that may contain processors. One bus may be an input to more than one switch, putting the switches in parallel. The output of one switch may be the input to another, putting the switches in series. However, two outputs may never be connected together. For example:



Any of the following can be easily configured with the DT11 bus extension options:

Back-up. A back-up processor or peripheral device or even an entire back-up system, automatically takes over in the event of a failure.

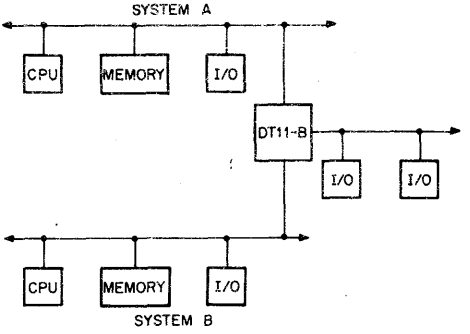
Subsystems monitoring. While a subsystem is collecting data, the processor is free to perform other tasks.

Processor failure detection. A "time-out"feature inside the switch automatically detects a failure and switches to another processor.

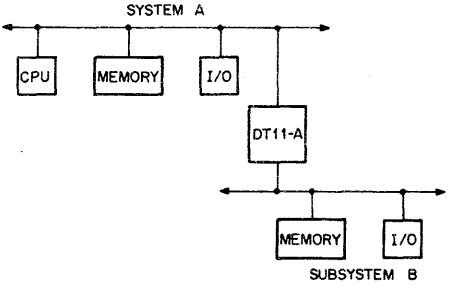
Multi-processor systems. Two or more processors can operate concurrently, with access to the same data base.

Shared peripheral systems. Costs can be reduced by having two or more processors share peripherals. For example, a line printer, used infrequently, is shared by several PDP-11 processors. When needed by one of the processors it is accessed quickly and efficiently with no waste of processor power.

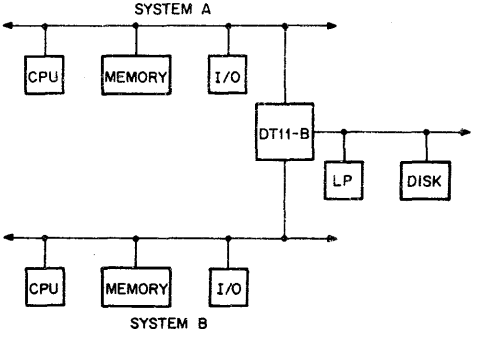
Examples:



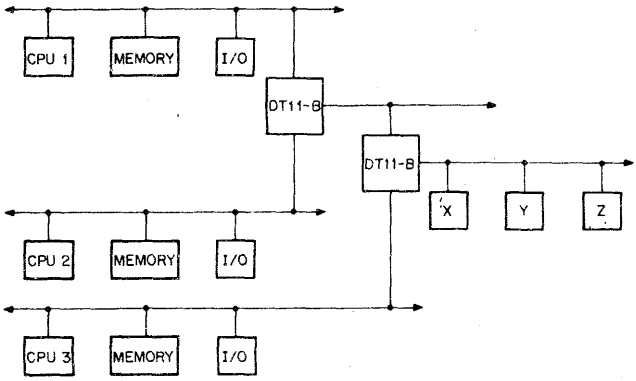
System B takes over in case System A fails.



Subsystem B collects data and connects to System A processor only when ready to transfer data or use processor. Meanwhile processor A is completely free to perform other tasks.



System A and System B share the same data base (disk) and the same line printer (LP).



Dual backup. Either CPU1, CPU2 or CPU3, can run devices X, Y and Z.

7.2 BUS SWITCHES DT11-A and DT11-B

The DT11-B bus switch is used in configurations with two processors, while the DT11-A switch is used in single processor configurations. Since both switches are very similar, the following description applies to both. Features which apply to the DT11-B only marked with as asterisk (*).

7.2.1 Switch Positions

The bus switch has the following five positions:

1. Connected to processor A.
2. Controlled by processor A, but not connected.
3. Neutral. Disconnected from both processors.
4. *Controlled by processr B, but not connected.
5. *Connected to processor B.

Each processor has an identical interface, and there are no differences between positions 1 and 5 or 2 and 4.

Connected

The Connected position means that the switched bus is connected to that processor bus and all the devices on the switched bus are available to that processor. The switch is almost completely transparent, except for a small delay added to each signal. The only difference is that executing a RESET instruction or depressing the START switch on the console causes the switched bus to be disconnected and the switch put in the Neutral position, and the processor interface and control register to be initialized. The devices on the switched bus, however, can be reset by a command to the bus switch control register (see section 7.2.8).

The signal on the UNIBUS that causes a power fail trap in the processor (AC LO) is passed through the switch. Therefore, a power failure on the switched bus while the switch is connected will cause a power failure trap in the processor (to location 24). For a complete discussion of power failure causes see the section on Fail-Soft Operation.

Controlled
The Controlled positions allow simultaneous, independent operations on the switched and processor buses. In this position, the switched bus is not connected to the processor bus, and any attempts to reference devices across the switch will cause non-existent memory errors in the processor (trap to location 4) and devices. The bus switch will, however, honor NPR requests from DMA devices. This allows a DMA device to transfer to a memory on the switched bus without stealing cycles from the processor. If any device on the switched bus makes an interrupt request, the switch will automatically go to the connected position of the processor that is controlling it. Thus, when a DMA device finishes its transfer on the switched bus and attempts to interrupt, the switch will automatically close and the DMA device will interrupt the processor.

The only signal that is passed through the switch in the Controlled positions is the power fail trap signal, so the processor will be warned if power is about to be lost on the switched bus.

Executing a RESET instruction or depressing the START switch will cause the switch to be placed in the Neutral position and the processor interface and control register on that side of the switch will be initialized.

Neutral
The Neutral position means that the switched bus is disconnected from both processors, and the bus switch will ignore everything on the switched bus. When power is first applied to the bus switch, it automatically goes to the neutral position.

7.2.2 Requesting the Bus Switch
Each processor gains control of the switch by requesting that it go into either the connected or controlled position associated with that processor. Should both processors make a request at the same time, the switch will honor whichever processor had the switch last. If one processor requests the switch while the other processor has control of it, an internal timer will be started (See Operation of the Internal Timer, below).

Once a processor has the switch, it can request that it go between its own Connected and Controlled positions or go back to Neutral, and these changes always happen immediately. If a processor requests that the switch go from Connected to Controlled at the same time that a device on the switched bus is attempting to interrupt, the request is ignored, so the switch will remain connected.

The switch has the ability to cause an interrupt when it changes state. If the interrupt enable bit in the bus switch control register is set, the switch will cause an interrupt whenever the state changes from Neutral to either Connected or Controlled. It will never cause an interrupt when going into the Neutral position or between the Connected and Controlled positions. An interrupt will not occur if the interrupt enable bit is set after the switch has changed between the states noted above.

7.2.3 Fail-Soft Operation

The bus switch is designed so that a greater system reliability may be achieved. An internal timer allows for processor backup, (see below) and the ability to completely disconnect a bus allows for peripheral backup.

The bus switch is built so that one processor cannot force the switch to the other processor or cause an interrupt on the other processor's bus unless the other processor permits it. This means that a non-working processor cannot cause anything to happen to a working processor.

To prevent a device that has been started by one processor from causing any interrupts or DMA transfers on the other processors bus, an Initialize signal is generated on the switched bus every time the switch goes into the Neutral position. The length of this signal is the major factor in how long it takes to switch from one processor to the other, and is, therefore, set for 10 microseconds. It is possible to inhibit this initialization by a switch on the manual panel, if desired. However, in this mode the bus switch cannot really be used for fail-soft operation. It does allow one processor to start a device and then let the other have the switched device without stopping the device. Great care must be taken if running in this mode to make sure a DMA device does not transfer into an area of the other processor's memory that should be protected.

As noted earlier, the warning signal on the UNIBUS that causes a power failure trap in the processor is passed through the bus switch in both the connected and controlled states. There is also a bit in the bus switch control register that is set whenever this warning signal is on the switched bus, independent of the position of the switch. Thus, whenever the switched bus is connected and a power fail trap occurs, the power fail trap routine can examine the bus switch control register to find out if the failure is on the switched bus.

Just before power actually fails (and at least 2ms after the warning bit is set, and trap, if any) the switch will automatically go to the Neutral position if in either the connected or controlled states.

Depending on the source of the power failure, the switch may do several things:

1. A processor or device on its bus has a power failure. In this case, the switch automatically disconnects from that processor and will not honor any requests from that processor until the power is restored. The bus switch bus interface and control register associated with that processor will be initialized. The other processor, however, can use the switch normally.

2. A device on the switched bus has a power failure. In this case, the switch will always go to Neutral and remain there until the power is restored. Both control registers are initialized. Each processor can run the devices on its own bus.

3. The bus switch may be powered by a system of three power supplies. If any one supply fails, the switch will continue to operate normally, and there will be a visual indication of which supply failed. If more than one supply fails, the switch will act as in case 2, above.

7.2.4 * Operation of the Internal Timer

A timer is included in the bus switch to help in the detection of processor hardware or software failures. Basically, the timer must be referenced every so often by the processor that has the switch.

The internal timer is started every time one processor has the switch in either the Connected or Controlled positions, and the other processor requests the switch. If the processor that is requesting the switch removes its request, the timer is stopped. If the processor that has the switch lets it go to Neutral, the other processor's request will then be honored and it will get the switch. If the processor that has the switch re-requests it, the timer will be restarted. Should the timer ever time-out, the switch is forced to the neutral position, and then, if a request for the switch is waiting, the switch will honor it. Thus, if the processor that has the switch re-requests it at the same time that the timer times out, the switch will go to Neutral and then return to the first processor, since that processor had the switch last.

If the timer is running and a processor stops or hangs because of a failure, the switch will not be referenced within this time and will automatically go to the neutral position, when the other processor can get the switch.

The way that the timer works means that the following rules should be followed to prevent a processor that is hung in a program loop from holding on to the switch by re-requesting it.

1. The re-request of the switch should not be put in basic interrupt service routines, program loops, or done using the T-bit trap.
2. The re-requests should be put in the main-line program, to check that it is getting executed as often as expected.
3. The placing of the re-requests must be carefully considered to make sure that no legal combination of interrupts, traps and subroutine calls that cause leaving the main-line program could result in not re-requesting the switch often enough.

If the switch is in the connected state (as opposed to Controlled) when the timer times out, the bus switch will wait up to 5 microseconds to synchronize with the processor before disconnecting. If nothing is happening on the switched bus, the bus switch will automatically switch to Neutral after that time. Thus, if the machine is halted or hung, the switch will change position without waiting to synchronize. This might, however, cause the processor to hang. To cause a working processor to hang, the timer must time out and the processor must be doing a Wait instruction. About 5 microseconds after the time-out, a device on the switched bus must then request use of the bus (for either a DMA transfer or interrupt). If the switch disconnects just as the processor starts to service the bus request, the processor may hang. The way to prevent this is to make sure the timer never times out. It should be noted that timeouts are fatal errors, and should never occur in a correctly functioning system (the system being the combined software and hardware).

7.2.5 * Interprocessor Communication

To enable a minimum of communication between the two processors, two bits are provided for each processor. One bit is an interrupt enable bit; the other is a communication bit. A processor gets an interrupt when its interrupt enable is set and the other processor's communication bit is set. The interrupt occurs only when the "AND"of the two bits becomes true.

In a non-fail-soft environment, these bits, in conjunction with the not-neutral bit can be used by two processors to control the switch without having the timer go-

ing. Thus, re-requesting the switch is not necessary. When one processor wants the switched bus, it causes an interrupt in the other processor and waits for the switch to go to Neutral. Once in Neutral, the processor can request the switch and will get it. The timer will never be started because there will never be a request for the switch while one processor has it.

7.2.6 Address And Vector Assignments

Each bus switch requires one address on each processor bus. There are eight addresses reserved for bus switches, from 777420 to 777436, where the first switch is assigned address 777420. On two processor switches, the same address does not have to be assigned to both sides.

The interrupt vector of the bus switch depends on the other devices in the system. Each switch has a different vector. On two processor switches, the vectors for each side are completely independent, and the vector for the interprocessor communication interrupt is different from the vector for the switch position interrupt.

The standard priority level of the bus switch is 7. On dual processor switches the communications interrupt and position interrupt always occur on the same level. However, the communications interrupts will always be serviced last if they occur at the same time.

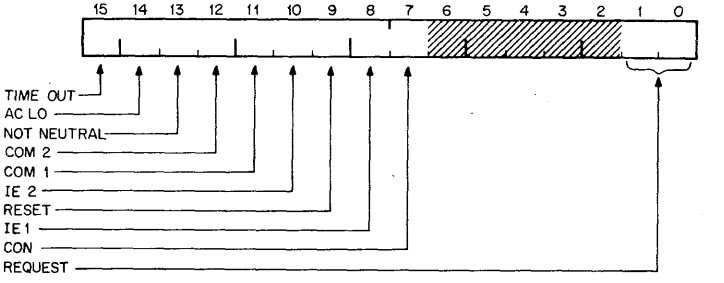
7.2.7 Manual Control

The manual control panel can be used to force the bus switch into the Neutral or Connected positions. One switch selects either programmable or manual mode; and the other switch, if in manual mode, selects either connected to processor A, in Neutral, or connected to processor B. When the switched bus is manually connected, all signals are passed through the switch and it ignores everything on the bus.

There is also a switch on the panel that inhibits initialization of the switched bus when entering the Neutral state (see Fail-Soft Operation).

7.2.8 Control Register

Each processor has access to a control register:



BIT	NAME	DESCRIPTION
*15	Time Out (TO)	This bit, when set, means that the timer timing out caused the last position change. Therefore, if CON (bit 7) and TO (bit 15) are both set, it means that the processor gained control because of a timeout. If only TO is set it means that the processor lost control because of a time-out. In the case of a processor that loses a switch because of a timeout but then re-requests it and gets the switch back immediately, the TO bits in both control registers will be set. This bit is cleared by writing into either byte of the control register, a power up or down, RESET, or START. This bit is read-only.
14	AC LO	This bit is the same as AC LO on the switched bus. AC LO is the warning signal to the processor that causes the power fail trap. This bit is read only.
13	Not Neutral (NN)	This bit is set whenever the switch is not in the NEUTRAL position. This bit is read only.
*12	COM2	This bit is set by the other processor setting its COM1 (bit 11). If IE2 (bit 10) is set when COM2 becomes set, an interrupt will occur. This bit is read only, and is always the same as the other processor's COM1.
*11	COM1	When this bit is set, COM2 (bit 12) of the other processor's control register is set causing an interrupt on its bus if its IE2 (bit 10) is set. This bit is cleared by a power up or down, RESET, or START.
*10	IE2	This bit allows the other processor to cause an interrupt. Setting this bit when bit 12 is set causes an interrupt. Another interrupt does not occur until either IE2 (bit 10) or COM2 (bit 12) gets cleared and then sets again. This bit is cleared by a power up or down, RESET or START.
9	Reset	Setting of this bit causes a 10 μs Initialize signal on the switched bus if the switch is in the connected or controlled positions on this side. This bit remains set for as long as the initialize signal is on the switched bus. Whenever this bit is set by the program, a loop should be executed that guarantees the bit is off before any references are made to the switced bus. If

this procedure is not followed, the bus may hang because many UNIBUS devices do not expect a bus data cycle to occur while the initialize signal is on the bus.

8	IE1	This bit, when set, means that the switch will cause an interrupt on leaving the neutral position for either the connected or the controlled positions on this side. To cause an interrupt this bit must be set when the switch changes state; therefore, the same instruction which requests the switch should set this bit. Bit 8 is cleared by a power up or down, RESET or START.
7	CON	This bit, when set, means that the switch is either connected or controlled, as determined by CR bits 0 and 1. Bit 7 is cleared by a power up or down, RESET or START. When changing between the connected and controlled states, bit 7 remains set. This bit is read only.
6-2	Not Used	Always read as zero.
1,0	Request	These bits are used to request that the switch go to a specific state and in conjunction with bit 7, to indicate what state the switch is in. They are coded as follows: Bit: 1 0 0 0: Neutral 0 1: Connected 1 1: Connected 1 0: Controlled Since there are no other writeable bits in the low byte, many of the byte instructions can easily be used to manipulate these bits. These bits are always cleared by a power-up or down condition, RESET instruction or depressing START on the console. Bit 0 is set by the switch when an interrupt causes the switch to change from controlled to connected. This bit is then held set until the program reads the control register, even if the program attempts to turn it off. This prevents a re-request from causing the switch to be sent back to the controlled position if the switch made the change from controlled to connected just before the request. Thus, a MOV instruction should not be used to re-request the switch; however, a NEGB would work. These bits are FOT effected by the timer timing out.

7.2.9 Specifications

Bus Address:	777420
Priority Level:	7
Vector Address:	System Dependent
Environmental:	10-50° C, 20-90% humidity without condensation
Physical:	10 1/2"panel space, standard 19"rack
Electrical:	Switching Time: Typically 500-1000 nanoseconds Internal Timer Range: up to up to 1/2 second

Power Used:

Version	AC Voltage, (50/60 cycles)	AC Current
DT11-AA	115	1.5
DT11-AB	230	.75
DT11-BA	115	2.0
DT11-BB	230	1.0
DT11-BC	115	2.5
DT11-BD	230	1.75

NOTE: The DT11-BC and BD versions have three power supplies for reliability.

PART I
Chapter 8

Communications Options

8.1 COMMUNICATIONS INTERFACES

DIGITAL has extended the PDP-11's adaptability to various communications applications with a variety of interfaces. These devices enable the PDP-11 to be connected both locally and remotely to serial asynchronous and serial synchronous lines. The interfaces allow both full and half duplex operations with connections to communications terminals via the standard EIA RS232-C and CCITT interface. The devices are summarized below and explained in detail in this chapter.

DEVICE	INTERFACES PDP-11 WITH:	TYPICAL USES:
DC11	Serial Asynchronous Line	Connects PDP-11 to various asynchronous terminals, or to another computer via a common carrier communications facility. Has program controlled Baud rates, character lengths, and stop codes.
DP11	Serial Synchronous Line	Connects PDP-11 to local or remote computers and terminals via high speed serial line.
DN11	Autocalling Unit	To dial remote computer or terminal.
DM11	Up to 16 serial Asynchronous Lines	Terminal-oriented systems for time-sharing, message switching, store and forward, data collection, remote concentrators.
KL11	Serial 8-bit Asynchronous Line	Connects PDP-11 to local teletype connections and local 8-bit current mode devices.
KL11 + DE11A	Serial 8-bit Asynchronous Line	Connects PDP-11 to local or remote 8-bit EIA-compatible asynchronous terminals such as CRTs, plotters, card readers, and line printers.

8.2 ASYNCHRONOUS LINE INTERFACE DC11

8.2.1 Introduction

The DC11 series of character-buffered interfaces are used between the PDP-11 and a serial asynchronous line. They can be used to connect the PDP-11 to a vari-

ety of asynchronous terminals or to another computer through a common carrier communications facility. Also the communications facility can be bypassed and asynchronous terminal devices and other computers can be connected locally to the PDP-11. The DC11 has the flexibility to handle many different types of terminals. The line speed, character size, stop-code length, and the data set control lines may be set under program control. Input and output line speeds can be varied independently.

The DC11 provides the necessary control signals and levels to interface to BELL 103 and 202 type modems or equivalent. The levels are EIA RS-232-C and CCITT compatible.

The PDP-11 UNIBUS serves as a multiplexer for adding multiple DC11s. Each two interfaces require one PDP-11 system unit's worth of mounting space. The prewired system unit and clock module are designated as the DC11-AA, DC11-AB, DC11-AC, DC11-AD, DC11-AE, DC11-AG, DC11-AH, or DC11-AX depending on the baud rates desired. The DC11-DA is the module set that interfaces the PDP-11 to a serial asynchronous line. Two DC11-DA's will mount in each DC11-A type unit. The DC11-A unit contains the clock for both DC11-DA module sets.

8.2.2 Operation

The DC11 is a character-buffered communications interface designed to translate asynchronous serial-bit stream data to parallel-character data. The units contain two independent character buffers (transmit and receive) capable of simultaneous two-way communication. Proper programming of each unit will allow it to operate in a half-duplex or full-duplex mode.

The receiver section offers serial to parallel conversion of 5-, 6-, 7-, or 8-level codes. The code size is under control of the program and appears right-justified in the data buffer without start or stop bits. Four different crystal-controlled clocking rates are available. When the character has been received, its parity is available to the programmer for testing. An interrupt request is generated in the middle of the last data bit of a character being received. If the program does not remove the character from the data buffer before the middle of the next start bit, a data overrun error bit is set in the device. Both the receiver and transmitter character length and stop-code size are simultaneously controlled by the program (i.e., they are always the same). The receiver interprets a break as a series of nulls.

The transmitter section offers parallel-to-serial conversion of 5-, 6-, 7-, or 8-level code. The transmission rate can be set by program control to one of four rates independent of the receive rate. An interrupt request is generated in the middle of the last data bit being set. Also included is the ability to transmit a continuous space (break).

The control section provides connection to all the leads from Bell 103 and 202 type data sets, with the exception of data set ready. Control of the data set is done by the program. Interrupt requests are generated when ring appears or at the transition of carrier detect.

The control leads are fail-safe; i.e., they will appear off if the data set loses power.

8.2.3 Programming

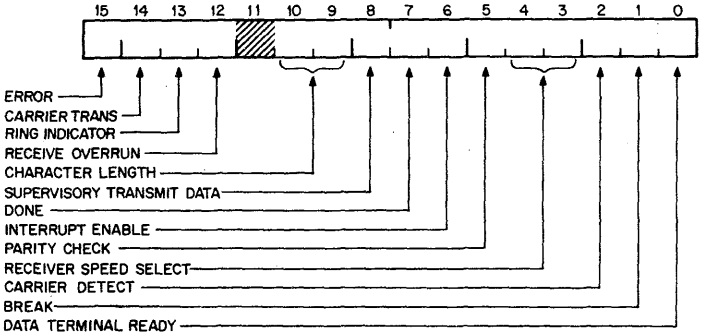
Each line unit contains four registers and, hence, requires four addresses. Address space has been assigned for 32 line units. Line unit number 1 starts at 174000, line unit 2 is at address 174010, up to line unit 32 at addresses 174370. The four registers and their address for line unit xx are:

REGISTER	ADDRESS
Receiver Status Register (RCSR)	174XX0
Receiver Buffer Register (RBUF)	174XX2
Transmitter Status Register (TSCR)	174XX4
Transmitter Buffer Register (TBUF)	174XX6

Each asynchronous modem interface requires one interrupt vector. The vector addresses are assigned from 300 to 777. The DC11 follows the KL11 in contiguous vector address assignments from 300 (i.e. the DC11's first vector address starts where the KL11 leaves off. If there are no KL11's other than the console Teletype, the first DC11 is assigned vector address 300).

Each DC11 has a bus request level assignment. All units will be shipped with the bus request line set to BR5. These levels are field changeable with a priority jumper plug.

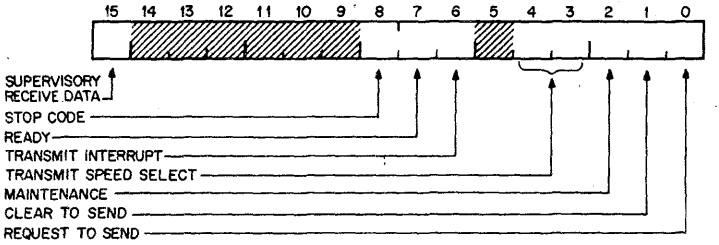
Receiver Status Register (RCSR)



BIT	NAME	DESCRIPTION
15	Error	The logical or of bits 12, 13, 14, causes an interrupt and is read only.
14	Carrier Transition	Set when carrier detect changes state. Cleared on read of receiver CSR. Read only.
13	Ring Indicator	Set when data set rings. Cleared on read of receiver CSR. Read only.
12	Receive Overrun	Signals an error condition. Set when start pulse is received and done flag is still set. Cleared on read of receiver CSR. Read only.
11	Not Used	

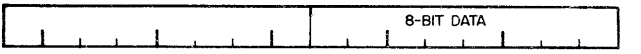
10,9	Character Length	Specify the number of bits per character: 10 9 0 0 8 bits/char. 0 1 7 bits/char. 1 0 6 bits/char. 1 1 5 bits/char. Read and Write.
8	Superv. Transmit Data	Provides signalling capability on reverse channel of 202C/D modems. Read and Write.
7	Done	Indicates character available, and is cleared by reading the receiver buffer. Read only.
6	Interrupt Enable	Enables the receiver interrupt facility. Read and Write.
5	Parity Check	Provides a parity check to incoming data: Bit 5 = 1 Odd parity checks Bit 5 = 0 Odd parity fault Bit 5 = 0 Even parity checks Bit 5 = 1 Even parity fault Bit is read on,y and is valid until next character start pulse is received.
3,4	Receiver Speed Select	Specify the Baud rate of the receiver: 4 3 0 0 Lowest 0 1 1 0 1 1 Highest (or a nonstandard Baud rate - DC11-AX) These bits are both read and write.
2	Carrier Detect	Control lead from modem. Indicates status of carrier and is asserted when channel is established. This bit is read only.
1	Break	When asserted, pulls the output data line to a space. This bit is read and write.
0	Data Terminal Ready	Control lead to modem. This bit conditions automatic answer and is both read and write.

Transmitter Status Register (TSCR)

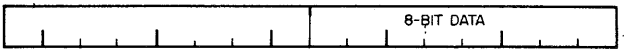


BIT	NAME	DESCRIPTION
15	Supervisory Receive Data	Provides receive capability on reverse channel of 202 C/D modems. Read only.
14-9	Not Used	
8	Stop Code	Sets the stop code sent by the transmitter: 0 - Set stop code to 2 bits 1 - Set stop code to 1 bit Read and write.
7	Ready	Indicates transmitter ready to output data. Cleared by loading transmitter buffer, set by having transmitter buffer zero'd. Read only.
6	Transmit Interrupt	Enables the transmitter interrupt facility. Read and Write.
5	Not Used	
4,3	Transmitter Speed Select	Specify the Baud rate of the transmitter 4 3 0 0 Lowest 0 1 1 0 1 1 Highest (or a nonstandard Baud Rate - DC11-AX) Read and Write.
2	Maintenance	Maintenance function which connects transmitter serial output to receiver serial input. Read and Write.
1	Clear to Send	Control lead from modem; required that this bit must be asserted for transmit interrupt. Read only.
0	Request to Send	Control lead to modem; required for transmission of data. Read and Write.

Receiver Buffer Register (RBUF)



Transmitter Buffer Register (TBUF)



8.2.4 Specifications

Operating mode:	Full- or half-duplex selected under software control.
Data Rates:	50, 75, 110, 134.5, 150, 300, 600, 1200, 1800 Baud or one user specified Baud rate between 600 and 10,000. Four speeds are available to the user under program control. Transmitting and receiving rates are independent. See DC11 models for specific combinations available.
Data Format:	One start bit. Character size is variable under program control to 5, 6, 7, or 8 data bits. Stop code is programmable to one or two bits.
Order of Bit Transmission:	Low order bit first.
Parity:	Computed on incoming data.
Distortion Input:	Can tolerate up to 40% per character.
Output:	Less than 3% per character.
Data Signals:	Conforms to EIA RS-232-C and CCITT specifications.
Control Signals:	All control leads from the Bell 103, 202 or equivalent modems are brought into the unit with the exception of data set ready. All leads are EIA RS-232-C and CCITT compatible.
Program Interrupts:	Receive done, transmit done, receive overrun, ring, and carrier transition. (If appropriate enable bits are set.)
Bus Load:	One line unit represents a one unit load to the PDP-11 UNIBUS. The UNIBUS can handle 18 unit loads. For more than 18 unit loads a bus extender, DB11-A, must be used.
Physical Connection:	25-foot cable with EIA RS-232-C-Compatible 25-Pin male connector.
Space Required:	1 systems unit for either one or two line interfaces.
Power Required:	2.2 amps of +5 Volts for the first interface in a systems unit. 2.0 amps of +5 Volts for the second interface in a systems unit.
Temperature/Humidity:	10° -50° C with 20 to 90% noncondensing humidity.

8.2.5 Ordering Information

DEC. NO.	PREREQUISITE	DESCRIPTION
DC11-AA	PDP-11	Dual Serial Asynchronous Line System Unit and Clock. Provides space for mounting two DC11-DA Line Units. Clock gives 110, 134.5, 150 and 300 baud signals.
DC11-AB	PDP-11	Same as DC11-AA except Clock gives 110, 300, 1200, 1800 Baud signals.
DC11-AC	PDP-11	Same as DC11-AA except Clock gives 110, 150, 600, 1200 Baud signals.
DC11-AD	PDP-11	Same as DC11-AA except Clock gives 50, 110, 134.5, 150 baud signals.
DC11-AE	PDP-11	Same as DC11-AA except Clock gives 75, 110, 134.5, 150 baud signals.
DC11-AG	PDP-11	Same as DC11-AA except Clock Gives 134.5, 150, 300, 1200 baud signals.
DC11-AH	PDP-11	Same as DC11-AA except Clock Gives 110, 134.5, 600, 1200.
DC11-AX	PDP-11	Same as DC11-AA except Clock Gives 110, 134.5, 150 plus one non-standard baud rate above 600 Baud and below 10,000 Baud.
DC11-DA	DC11-A	Full Duplex serial module set for DC11-A (DC11-A accommodates 2 ea) with EIA/CCITT termination suitable for direct use with 103 or 202 modem. Handles 5, 6, 7 or 8 bit codes with 1 or 2 stop bits.
H312A		Asynchronous-Synchrounous Null Modem - allows direct connection of any peripheral having an EIA 232 interface with a DC11-DA or a DP11-DA. (A DP11-KA is generally required when using the H312A with a DP11-DA).

8.3 Automatic Calling Unit Interface DN11

8.3.1 Introduction

With the DN11 and a Bell 801 Automatic Calling Unit (ACU), any PDP-11 can dial any telephone number in the Direct Distance Dial Network and establish a data link. The DN11 is a digit-buffered interface, and digits to be dialed are presented as four-bit binary numbers. The interface drives the ACU with EIA-232-C voltages and is connected via a standard 25-pin plug.

The programmer has access to all lines of the 801 through the DN11. The 801 presents the following leads to the DN11: Power Off and Indicator, Data Line Occupied, Abandon Call and Retry, Data Set Status and Present Next Digit. The DN11 provides the following leads to the 801: Digit Present, Call Request and four Digit Leads.

Because the PDP-11 UNIBUS serves as a multiplexer, multiple automatic calling units can be added to the PDP-11. One PDP-11 System Unit accepts up to four 801 ACU Interfaces. Each interface looks like one device to the UNIBUS.

8.3.2 The Sequence of Operation

The following describes the use of the DN11 to originate a DDD call. This is an automated version of the procedure that everyone goes through when placing a telephone call.

1. Check for 801 power on (PWI = 0).
2. Check for unoccupied data line (DLO = 0).
3. Set Call Request bit (FCRQ = 1).
4. The 801 will seize the line on receiving the dial tone and assert Present Next Digit which causes a PDP-11 program interrupt (FPND = 1).
5. The line is now in use and the Data Line Occupied bit is set (DLO = 1).
6. The first digit to be dialed is provided by loading the four least significant bits of the byte into the digit bits (8 to 11) of the DN11 status register. The upper four bits of the byte are read-only and can have any value during the loading of the four low-order bits.
7. The 801 is informed that the 1st digit has been loaded by asserting the Digit Present Bit (FDPR = 1).
8. The 801 then reads Digit leads 1 through 4 and lowers Present Next Digit Lead (FPND = 0).
9. The hardware responds and lowers Digit Present Lead (FDPR = 0).
10. The 801 then dials the first digit and again raises Present Next Digit Lead (FPND = 1).
11. The next digit is loaded and the Digit Present bit is asserted (FDPR = 1).
12. Sequences 6 through 10 are repeated until all digits have been dialed.
13. When the last digit has been dialed, one of two procedures must be used to complete the call.

    a) If "handshaking signals" are used (Bell 100 series modems or equivalent):

A Detect Answer option is used. The 801 retains line control and looks for an answering tone, from the called station. Upon receiving the tone the modem is connected to the line, Data Set Status is asserted and a program interrupt is generated (DSS = 1). This stops the Abandon Call and Retry timer which would have been initiated had no tone been received. These, in turn, would have generated a signal to the DN11 and cause a program interrupt with the Abandon Call and Retry bit set (ACR = 1). The program would then either retry or drop the call.

b) If using modems without the automatic handshaking feature:

The End-of-Number (EON) mode must be used. EON is sent after the last digit has been dialed. This causes the 801 to connect the modem to the line and assert Data Set Status (DSS = 1). However, the modem and its controller must be able to determine when the called station has answered and is sending data. To do this, it is necessary to use an 801 with option "Y"(available from the Telephone Company). This option lets the Abandon Call and Retry timer continue running even after the DSS bit has been set. When the ACR timer times out it will notify the user of the line to check if data is being received by the modem.

14. There are two options available when terminating a call:

a) The Call Request bit is set to zero (FCRQ = 0). This will remain until the Data Line Occupied bit also goes to zero (DLO=0), which is a necessary condition before a new call can be initiated.

b) If the 801 option "Z"is used, the call can be terminated by clearing Data Terminal Ready in the modem. In this case, dropping Call Request will not terminate the call. However, it must be dropped before a new call can be attempted.

15. Should the 801 lose power during a call an interrupt will be generated and the Power Off bit will be set (PWI = 1). The interface will not return an interrupt if the Call Request bit is set with the power off (FCRQ = 1).

8.3.3 Programming

Each ACU interface contains one register and therefore requires one 16-bit address. Address space has been assigned for 64 interfaces. The four addresses for the four interfaces that can be plugged into one system unit must be consecutive addresses starting with 175XX0 where XX = 20 for the first line. If only one line is in use, it uses address 175200. Interface number 2 has address 175202, and interface number 64 has address 175376.

Note: In addition to the individual Interrupt Enable bit for each interface, there is a master enable bit associated with line number 1 of a given system unit. It enables the interrupts for the entire group. The master enable bit on lines 2 through 4 of a given system unit are ignored by the interface.

Each set of four DN11's requires one interrupt vector. The vector address for communications options are assigned in the range from 300 to 777 according to the following convention:

1. The first DC11 assigned in a system will be given vector address 300, the next one (if any) will be given vector 310 etc.

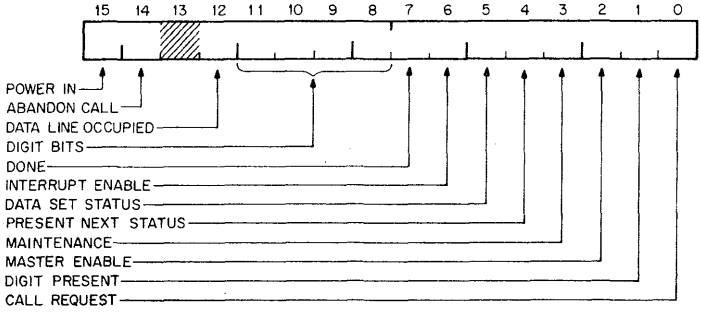
2. Then KL11's will be assigned in order.

3. Then DP11's will be assigned in order.
4. Then DM11's will be assigned in order.
5. Then DN11's will be assigned in order.

This implies that programs using communications options will have to be assembled for specific systems. Also, systems containing many communications options will have vector addresses above 400.

All units are shipped with the bus request line set to BR4. This can be changed in the field with a Bus Request Priority Jumper Plug.

ACU Interface Status Register



The detailed description of bits follows:

BIT	NAME	DESCRIPTION
15	Power Indicate (FPWOF)	This bit is normally zero and is set by the ACU whenever power is switched off at the unit. If a call is in progress at that time, DONE is set. This causes an interrupt if INTENB and MINAB = 1 (Read only).
14	Abandon Call and Retry (FACR)	A control lead from the ACU. This bit is set by the ACU whenever an internal timer times out. The timer is reset by the ACU whenever it gives PND and is for detecting wrong numbers and busy signals. It is inhibited by the presence of DSS except if the 801 option "Y" is in use; it times out even then and gives an interrupt (by setting DONE). This is used when the programmer wants a timer to detect wrong numbers and busy signals.
13	Not Used	
12	Data Line Occupied (FDLO)	This bit is set by the ACU whenever the line to the telephone central office is being

		used by the ACU. It allows the programmer to test the ACU to see if the last call was successfully terminated before he tries to use it for the next one (Read only).
11-8	Digit Bits (NB1-4)	These four bits are control leads to the ACU. These low order bits of the second byte make up the BCD digit to be dialed. Since the high-order four are read only, it does not matter what is in them during a load, and the programmer may use them as he wishes. In MAINT mode, these bits are used to drive the four control lines that can cause interrupts. See bit 03 for description (Read /Write).
7	DONE	This bit is set to indicate that the ACU is done with the previously requested action and ready to accept new data, usually the next digit in a sequence to be dialed. The conditions that set DONE are listed (CRQ must be a one): 1. Transition of PND to one (after CRQ set or previous DPR set). 2. Transition of DSS to one (after last DPR or EON). 3. Transition of ACR to one (if timeout error - - anytime). 4. Transition of DLO to one (if power switched off) (Read/Write)
6	Interrupt Enable (INTENB)	This bit allows the setting of done to cause an interrupt if the master enable bit (bit 02 line #1 of a system unit) is set (Read/Write).
5	Data Set Status (FDSS)	Control lead from ACU. This is a statement by the ACU that the called party has answered and that the associated data set now has control of the line. It is accompanied by the setting of DONE to obtain an interrupt. It remains set until after the end of the call (Or until the data terminal ready lead to the associated modem is dropped which then drops FDSS). If the associated modem answers a call while the dialer is in use (CRQ = 1), then DSS will be enabled and DONE set. If interrupt Enable is set there will be an interrupt (Read only).
4	Present Next Digit (FPND)	Control lead from the ACU. This is a request by the ACU for the program to load another digit during dialing. It is accompanied by the setting of DONE to ob-

tain an interrupt. It is cleared by the ACU when the digit is accepted (after DPR is set) and will remain off at least 600 ms before coming up for the next request (Read only).

3 Maintenance (MAINT)

This bit, when set, allows checking of the interface without a connected ACU. It allows FCRQ to be read and switches the ACU response lines - - PND, DSS, PWI and ACR to the output of the digit lines for testing purposes.

Bit	Digit	ACU Line		Ctl Bit
08	BN1	PND	FPND	04
09	NB2	DSS	FDSS	05
10	NB4	PWI	PWO	13
11	NB8	ACR	FACR	14

This bit also forces CRQ (to ACU) off and forces FDLO (Bit 12) on. (Read/Write).

2 Master Enable (MINAB)

Allows the program to disable then reenable all 4 ACU interrupts easily with one bit. This bit is connected for only one of the four possible lines which mount in one system unit (Read/Write).

1 Digit Present (FDPR)

Control lead to the ACU. This bit must be set by the program after it loads the next digit (in response to a PND request) to inform the ACU to continue dialing. The interface automatically clears this bit when the ACU clears PND to indicate acceptence of the digit (Read/Write).

0 Call Request (FCRQ)

Control lead to ACU. This bit starts the Automatic Calling Sequence (Write only).

8.3.4 Specifications

Control Signals: All control leads are brought into the DN11 from the Bell 801 (See Figure 8-3 for pin numbers). All leads are EA RS-232-C and CCITT compatible. All leads are failsafe (i.e., they appear off if the 801 loses power).

Bus Load: One DN11 interface represents one unit load to the PDP-11 UNIBUS. Thus, four controls in one System Unit represent four unit loads. The UNIBUS provides 18 unit loads. To add more than 18 unit loads a bus extender, DB11-A, must be used.

Program Interrupts: Normal interrupts are caused during a call by:
1. Transition of PND to a one. Sets DONE. Digit desired.
2. Transition of DSS to a one. Sets DONE. Data set connected.

3. Transition of ACR to a one. Sets DONE. Busy or wrong number.

Error interrupts are caused during a call by:

1. Transition of PWI to off. Sets DONE. Power to ACU was switched off.

(Note: Appropriate Enable bits must be set.)

Physical Connection: 25-foot cable with RS-232-C compatible 25-pin male connector.

Power Required: I.4 Amps of +5V for the first line 0.4 Amps of +5V for the second through the fourth lines.

Temperature/Humidity: 0°-40°C with Relative Humidity of 20% to 90%, non-condensing.

Output

Pin	Designation	Abbr.
4	Call Request	CRQ
5	Digit Present	DPR
14	Digit Lead	NB1
15	Digit Lead	NB2
16	Digit Lead	NB4
17	Digit Lead	NB8

Input

Pin	Designation	Abbr.
5	Present Next Digit	PND
6	Power Indication	PWI
22	Data Line Occupied	DLO
1	Frame GND	FGD
7	Signal GND	SGD

Figure 8-3 Pin Numbers on the 801 Cable

8.3.5 Ordering Information

DEC NO.	PREQUISITE	DESCRIPTION
DN11-AA	PDP-11	Prewired System Unit for up to four Bell 801 Automatic Calling Unit interfaces. (DN11-DA)
DN11-DA	DN11-AA	One Line Interface for a Bell 801 Automatic Calling Unit. Includes 25' Cable (Up to four DN11-DA's may be mounted in a DN11-AA).

8.4 SYNCHRONOUS INTERFACE DP11

8.4.1 Introduction

The DP11 provides a double-buffered program interrupt interface between, a PDP-11 and a serial synchronous line. This interface allows the PDP-11 to be used in remote batch and remote concentrator applications. With the DP11, a PDP-11 can also be used as a front end synchronous line controller to handle remote and local synchronous terminals.

The DP11 interface offers flexibility. It handles a wide variety of terminals and line disciplines (i.e., line control procedures and error control techniques). A programmer can vary sync character, character size, and modem control leads. Automatic sync character stripping and automatic idling are also program selectable. While idling, the DP11 transmits the contents of the sync buffer.

The DP11 design provides individual interrupt vectors and hardware interrupt priority assignments for the transmitter and receiver. Interrupt priority is jumper selectable. This feature, coupled with the automatic transmit idle capability, enables dynamic system adjustment to peak message activity. For example, the programmer can temporarily ignore the transmitter if receive activity is high.

Because the PDP-11's UNIBUS serves as a multiplexer, multiple synchronous lines can be added to a PDP-11. One PDP-11 system unit's worth of mounting space is used for each independent synchronous line interface unit.

8.4.2 Operation

The DP11 is a fully character-buffered synchronous serial line interface capable of two-way simultaneous communications. The DP11 translates between serial data and parallel data. Output characters are transferred in parallel from the computer to a buffer register where they are serially shifted to the communication line. Input characters from the modem are shifted into a register, transferred to a buffer register, and made available to the PDP-11 on an interrupt basis.

Both the receiver and the transmitter are double buffered. This allows a full character time in which to service transmitter and receiver interrupts.

The clocking necessary to serialize the data is normally provided by the associated high-speed synchronous modem. Alternately, the internal clocking option can be used for local terminals when no external clocking is available.

Receiver

Synchronization between the DP11 and the transmitting terminal is extablished by a sync character code. Since the sync code and character size are programmable, the programmer must load them in the receiver status register prior to synchronization. After this is done, the controller will scan the incoming bit stream until it finds two sequential sync characters. Then, it sets a receive active flag. The standard sync character for eight-bit ASCII is 026(8)(00010110) and eight-bit IBM BISYNC is 32(16)-(000110010).

Once synchronization is achieved, serial data can be transmitted and received continuously (no start or stop bits are required as in asynchronous communications).

The DP11 can be in one of two modes while receiving data:

1. All sync characters will be automatically stripped from the incoming data stream, if the receive active bit is set and the strip sync bit is set.

2. Sync characters will be treated as normal data and cause an interrupt request, if the receive active bit is set and the strip sync bit is not set.

Incoming characters appear right justified in the receive data buffer. The first bit received appears as the right-most bit in the buffer. When the character has been received, its parity is available for testing by the programmer.

There are two independent interrupt request levels and interrupt vectors associated with the DP11. One is for the receiver and the other is for the transmitter and the DP11 status.

A receive interrupt request is generated as the received character is transferred into the receive data buffer. If the program does not remove the character from the data buffer before the next character is transferred, a data overrun error bit is set in the DP11 status register. If the status interrupt enable bit is set, this error condition will cause a DP11 status interrupt request.

In half-duplex operation, setting the half-duplex bit will disable the receive logic when request to send is on. This prevents the transmitted character which appears on the receive data lead from also causing a receive interrupt.

Transmitter

The transmitter has two modes of operation:

1. When the idle sync bit is not set the transmitter must be refreshed approximately once a character time (i.e., (1/Baud) (bits per character-1/2) seconds) or the DP11 will stop transmitting (hold the transmitted data line in the binary 1 mark condition) and set the Request-to-Send to the modem to the off state.

2. When the idle sync bit is set the logic will transmit from the sync buffer if the programmer does not refresh the transmitter in approximately one character time (i.e., (1/ Baud) (bits per character-1/2) seconds).

The transmitter has a separate interrupt enable control bit from the receiver and the DP11 status. When the transmitter interrupt is enabled, an interrupt request is generated when the leading edge of each character is presented to the line.

Control Leads

The modem control leads are provided to interface the DP11 to Bell 201,303 or equivalent modems. These leads allow the DP11 to be used in switched or dedicated, full- or half-duplex configurations. The DP11 status interrupts have a separate interrupt enable bit but share the same bus request level and interrupt vector as the transmitter. If the status interrupt is enabled, a carrier flag, data overrun, or ring will generate interrupt requests. The control leads are fail-safe, i.e., they will appear off if the modem loses power.

The DP11-DA is connected to a Bell model 201 modem (or equivalent) by a 25-ft. cable terminated at the modem end with a 25-pin male connector. Standard interface signals are bipolar (EIA/CCITT). Interface signals versus connector pin assignments are given in Figure 8-1.

Pin	Signal
1	Signal or Protective Ground
2	Send Data
3	Receive Data
4	Send Request
5	Clear to Send
6	Interlock
7	Signal Ground
8	Carrier On-Off
15	Serial Clock Transmit
17	Serial Clock Receive
20	Remote Control
22	Ring indicator 1
24	External Timing

Figure 8-1 Connector Pin Assignments for Bell Series 201 Modems

The DP11-DC is connected to a Bell 303 modem (or equivalent) by a 25-ft. cable terminated at the modem end by a male 12-pin coaxial connector. Standard interface signals are the current mode type where a mark is 5 milliamperes or less and a space is 23 milliamperes or greater. However, there are two exceptions: data terminal ready and ring indicator. These signals are normally bipolar levels (EIA/CCITT). Interface signals and connector pin assignments for the Bell 303 modem are given in Figure 8-2.

Pin	Signal
E	Send Data
K	Receive Data
D	Send Request
C	Clear to Send
F	(Center Conductor) AGC Lock
M	(Center Conductor) Carrier On-Off
J	Serial Clock Transmit
L	Serial Clock Receiver
M (Outer Conductor)	Data Terminal Ready*
F (Outer Conductor)	Ring Indicator*
H	Serial Clock Transmit (External)

*EIA Levels

Figure 8-2 Connector Pin Assignments for Bell Model 303 Interface

The DP11 has on-line diagnostic capabiltiy. When the maintenance mode is set, the transmitter output is connected to the receiver input. Additionaly, the clear-to-send lead is simulated and the transmit receive clocks are replaced by a 3000 Hz clock. This allows the DP11 diagnostics to be run without operator intervention (i.e., No cables must be removed).

8.4.3 Programming

Each line unit contains five registers and, hence, requires five addresses. Address space has been assigned for 32 line units. Line unit number 1 starts at 174770, line unit 2 is at address 174760, up to line unit 32 at address 174400.

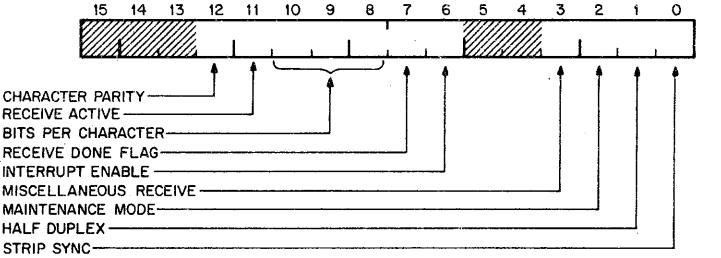
The five registers and their addresses are listed below (Note the XX = 77 for the first line unit and decreases to 40 for the 32nd line unit).

REGISTER	ADDRESS
Receiver Status Register	174XX0
ReceiverBuffer	174XX2
Sync Register	174XX3
Transmitter Control and Status Register	174XX4
Transmitter Buffer	174XX6
Extended Sync Register (4 bits)	174XX7

Each synchronous modem interface requires two interrupt vectors: one for receive done and the other for transmit done and status. The vector addresses are assigned from 300 to 777. The DP11 follows the KL11 and the DC11 in contiguous vector address assignments from 300 (i.e., the DP11's first vector address starts where the KL11 and the DC11 leave off. If there are no KL11's other than the console Teletype or DC11's, the first DP11 is assigned vector address 300).

Each DP11 has two independent bus request levels. All units will be shipped with both bus requests lines set to BR5. These levels are field changeable with a priority jumper plug.

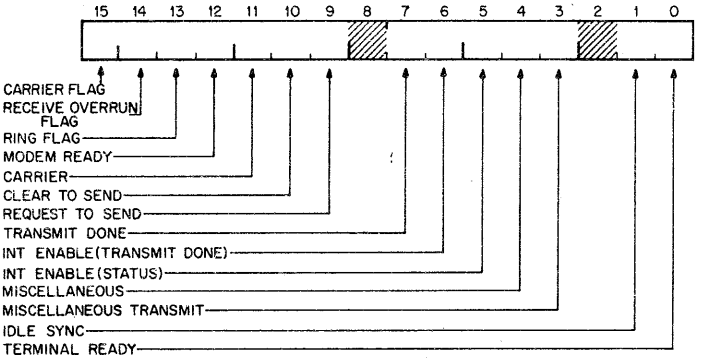
Receiver Status Register



BIT	NAME	DESCRIPTION
15-12	Not Used	
12	Character Parity	The character parity (VRC) bit indicates the parity of the last character assembled and contained in the receive buffer. A "one" indicates "odd"character parity, while a "zero"indicates "even" parity. This bit is changed at the same time the receive done flag is set
11	Receive Active	Receive active is set when the hardware recognizes two consecutive sync characters. This bit is read/write.

10-8	Bits Per Character	Selects 6, 7, 8, 10, 11 or 12 bits per character as follows: 000 8 bits per character 001 7 bits per character 010 6 bits per character 011 Not Used Optional with DP11-CA: 100 12 bits per character 101 11 bits per character 110 10 bits per character 111 Not Used These bits are write/read and initialize selects 8 bits per character.
7	Receive Done Flag	The receive done flag indicates that the receive buffer contains an assembled character. If the program does not respond to this flag in 1/Baud X bits per character seconds, the receive overflow flag will be set (causes a transmit status interrupt). This bit it read/write and is cleared by: a. Initialize b. By gating the receive buffer to the UNIBUS.
6	Interrupt Enable (Receive Done)	The receive done interrupt enable allows a receive interrupt to occur when the receive done flag is set. This bit is read/write.
5	Not Used	
4	Not Used	
3	Miscellaneous Receive	Miscellaneous receive is provided to monitor any non-standard modem status required by the user. Changes can be implemented by computer special systems or by the user. Standard units will be wired to secondary receive data (i.e. 202). This bit is read only.
2	Maintenance Mode	Maintenance mode provides an internal data loop which connects the transmitter output to the receive input. Additionally, the clear-to-send lead is simulated by the hardware. This mode of operation provides its own clock which will handle data at approxiametely 3000 Baud.
1	Half Duplex	If set, request to send on will inhibit the receive logic. This bit is read/write.
0	Strip Sync	If set, all sync characters following receive active will be stripped from the incoming serial data. This bit is read/write.

Transmit Status Register



BIT	NAME	DESCRIPTION
15	Carrier Flag	This bit is set if the modem carrier lead made an on to off transition. A transition occuring on this lead while data is being received, indicates a high probability of data errors. Also, the receive synchronism with the incoming data bits is no longer reliable and a new sync sequence should be established. This is done by writing a zero into the receive active bit and requesting a re-sync (i.e., sync, sync) from the remote terminal.
14	Receive Overrun Flag	This bit is set if the receive buffer was not read in 1/Baud x bits per character time following the receive done flag. This flag indicates a loss of at least one data character and suggests that a re-transmission be requested. This bit is read/write.
13	Ring Flag	A one indicates that a ring signal has been received by the modem. Also the flag will cause a transmit status interrupt if interrupt enable (status) is set. This bit is read/write.
12	Modem Ready	This bit reflects the current state of the data set ready (also interlock) lead. This bit indicates that the modem is powered and not in test, talk, or dial mode. This bit is read only.
11	Carrier	This bit reflects the current state of the modem carrier (agc if 300 series) control lead. An off indicates that no signal is

		being received or that the received signal is unsuitable for demodulation. In half-duplex operation, the carrier lead is clamped off (in the modem) when request-to-send is on. This bit is read only.
10	Clear to Send	This bit reflects the current state of modem clear-to-send lead. A "one" indicates that the modem is ready to transmit data. This signal is a result of the request- to-send lead in a half-duplex configuration. Read only.
9	Request to Send	Request to send is a hardware function. This bit is set on the second positive transition of the transmit clock if the transmit buffer is loaded or if the idle sync bit is set. This bit is read only and is cleared: a. By initialize b. If idle sync is not set and the transmit buffer was not refreshed in 1/Baud x (bits per character-1/2) seconds after transmit done was set. Request to send will go to zero on the second positive transition of the transmit clock following the end of bit presented to the line.
8	Not Used	
7	Transmit Done	The transmit done flag is set to a one when the leading edge of the first bit of each character is presented to the line. Additionally, this flag will cause a transmit/status interrupt if interrupt enable (transmit done) is set. This bit is read/write and is cleared by: a. Initialize b. By loading the transmit buffer
6	Interrupt Enable (Transmit Done)	The interrupt enable (transmit done) if set allows the transmit/ status interrupt to be generated by transmit done. This bit is read/write.
5	Interrupt Enable (Status)	Interrupt enable (status) if set allows the transmit/status interrupt to be generated by carrier flag, receive over run flag and by ring flag. This bit is read/write.
4	Miscellaneous	Provided to satisfy a variety of needs; such as: new sync rate selector, etc. This lead is expected to be wired by Computer Special Systems or the end user. This bit is write only.

3	Miscellaneous Transmit	Provided to satisfy a variety of needs such as: new sync, rate selector, etc. This lead is expected to be wired by Computer Special Systems or the end user. Standard units will be wired for secondary transmit data (i.e. 202). Additionally, the secondary transmit data line is used to generate the receive and transmit clock in the external loop test configuration. Note: The external loop configuration will not operate if the miscellaneous transmit lead is reassigned. This bit is read/write.
2	Not Used	
1	Idle Sync	Allows transmit from the sync buffer. Note: Transmit done is set (if enabled) as the first bit of each character as presented to the line. If the idle sync bit is set when the transmit is inactive, the logic will raise request to send and begin transmitting from the sync register. Once active, the transmit shift register will be loaded from the sync register if the program has not responded to transmit done in 1/Baud x (bits per character-1/2) seconds. This bit is read/write.
0	Terminal Ready	Controls switching of the data communication equipment to the communication channel. Auto dial and manual call origination: maintains the established call. Auto answer: allows handshaking in response to a ring signal. This bit is read/write.

8.4.4 Specifications

Type:	Double-buffered transmit and receive
Operating Mode:	Full- or half-duplex selected under software control
Maximum Data Rate:	50,000 bits per second (9600 bits per second with the DP11-DA)
Data Format:	Character size is variable under program control to 6, 7, or 8 bits (10, 11, or 12 bits optional)
Clocking:	Synchronous clock from the modem (internal clock optional)
Sync Character:	Programmable
Sync Detection:	Two successive sync characters required to activate the unit.
Bit Transmission:	Low order bit first
Parity:	Parity check bit provided on incoming characters

Modem Compatibility (Typical)

Type	Speed (Baud)	Communications Channel
Bell 201A	2000	direct distance dialing network Type 3002(C2)
Bell 201B	2400	leased line only; Type 3002 (C2)
Bell 303B	19,200	leased line only; half group (6 voice-band lines)
Bell 303C	50,000	leased line only; group (12 voice-band lines)

Data and Modem Control Signals:	All leads of Bell 201 and 303 modems are brought into the unit. All leads are EIA RS-232-C and CCITT compatible for the 201 modem. All leads for the 300 Series are current mode as defined in the appropriate reference manual.
Program Interrupts:	Receive Done, Transmit Done, Carrier Flag, Receive Overrun, and Ring (If appropriate Enable bits set)
Bus Load:	One line unit represents one unit load to the PDP-11 UNIBUS. The UNIBUS provides 18 unit loads. To add more than 18 unit loads a bus extender (DB11-A) must be used.
Physical Connection:	For 201 modems. 25-foot cable with RS-232-C compatible 25-pin male connector. For 303 modems, 25-foot coaxial cable with appropriate connector.
Space Required:	1 System Unit for one interface.
Power Required:	2.5 Amps of +5 Volts
Temperature/Humidity:	0°40° C with 20 to 90% noncondensing humidity.

8.4.5 Ordering Information (Models Available)

DEC NO	PREREQUISITE	DESCRIPTION
DP11-DA	PDP-11	Full/half duplex synchronous line module set. Double buffered. 6, 7, or 8 bit characters. EIA/CCITT termination suitable for direct use with 201 modems. Includes 25-foot modem cable.
DP11-DC	PDP-11	Same as above except suitable for direct use with 303 modems. includes 25-foot modem cable.
DP11-CA	DP11	Allows the DP11 to handle 10, 11, or 12 bits per character.

DP11-KA	DP11	Internal clock option. Clocking source to be used for direct connection of DP11 to a local synchronous terminal or a local synchronous computer interface. The following Baud rates are available: 2000, 2400, 4800, 9600,19.2K, 40.8K and 50K Baud. If no rate is specified, 40.8K Baud will be supplied.
H312A	DP11-DA	Synchronous/asynchronous null modem jumper box. Allows direct connection of a PDP-11 to any peripheral with a modem type interface which conforms to EIA RS-232-C and CCITT specifications. (A DP11-KA is generally required when the HB312A is used with the DP11-DA).

8.5 ASYNCHRONOUS 16-LINE SINGLE SPEED MULTIPLEXER DM11

8.5.1 Introduction

The DM11 is a full- or half-duplex 16-line aynchronous multiplexer. All lines operate at a common code length and Baud rate. The unit will operate at speeds up to 1200 Baud for the full 16 lines. Multiple DM11's can handle over 160 lines at 110 Baud. The DM11 uses the PDP-11 NPR (DMA) facility to assemble and to transmit characters directly to or from core memory. The applications of the DM11 vary widely. They include terminal-oriented systems for time sharing, store and forward message switching, data collection, and remote concentrators. The prime advantages of the DM11 in these applications is the high level of price/ performance that it offers for interfacing multiple terminals or modems to a PDP-11 system.

Receiver

The receiver control automatically performs character start bit synchronization, data bit assembly and direct DMA (NPR) character storage in a 64-word Receiver Circular Buffer.

The Circular Buffer contains data characters in the low order byte; the line number and character status are contained in the high order byte of each word entry. The characters are stored right-justified; the first bit received is in the least significant position. The character status indicates if the character ended with a legal stop bit (mark) and provides an indication of parity of the received character.

Transmitter

The transmitter control performs NPR (DMA) message transmission under the control of program-settable Byte Count and Byte Address locations. The Start Bit and Stop Units are provided by the control thus allowing data in core to be byte processed. The characters are serialized right most bit first. The DM11 does not disturb the data in core during transmission. This allows a single message to be transmitted on multiple DM11 lines simultaneously. A program interrupt request at the specified priority level will be generated when the transmit Byte Count on any line decrements to zero. The program then determines the affected line (by testing the hardware activity register) and initiates the proper transmit action.

The multiplexer provides two interrupt priorities and two vector addresses. The receiver control will be assigned a higher priority than the transmitter. This enables the time-critical incoming data to be handled before transmit done interrupts. This approach increases the line-handling capacity of the system.

Modem Control Multiplexer DM11BB
In cases where the DM11 is used in the public switched networks such as DDD, or TWX, the modem control multiplexer DM11BB should be used. The control multiplexer provides the necessary control leads to interface with the Bell 103 and 202 type modems or equivalent. All leads meet EIA RS-232-C and CCITT specifications.

Line Adapters and Physical Configuration
The DM11 provides proper interfaces for Teletype, private line modems, switched network modems, Telex, and Telegraph. The DM11-AA consists of a dual PDP-11 system unit, a cable, and 5 1/4"x 19"distribution panel and Power Supply for the distribution panel for 110V.60Hz. The DM11-AC is identical to the DM11-AA except that its power supply is for 230V 50Hz. A DM11-DA provides line conditioning for four 20-ma. Teletype lines. Up to four DM11-DA's can be added to each DM11-AA or DM11-AC.

A DM11-DB provides line conditioning for four EIA RS-232-C lines (data only) plus four 25-foot modem cables. Up to four DM11-DB's can be added to a DM11-AA.

For switched network modems and private lines where modem control is required a DM11-BB is needed in addition to a DM11-AA or DM11-AC. The DM11-BB mounts in the DM11-AA or DM11-AC and provides control for all 16 lines. A DM11-DC provides line conditioning for four EIA RS-232-C lines with modem control plus four 25-foot modem cables. Up to four DM11-DC's can be added to the DM11-AA or DM11-AC, DM11-BB combination.

For interfacing to Telegraph and Telex Lines, the DM11-AB Dual Systems Unit and DC08CS Telegraph distribution panel combination is required. The DM11-AB Dual Systems Unit consists of the multiplexor logic for 16 lines, and a cable which connects to the DC08CS distribution panel. The DC08CS distribution panel is a 5 1/4" x 19" panel which provides mounting space for up to 32 telegraph line interfaces. The actual Telegraph Line interface is provided by the DC08CM which provides solid state line driving capability for two Telegraph lines. (Note that two DM11-AB's can share a single DC08CS distribution panel).

If power for the Telegraph Lines is externally provided, the DC08D 32 Line Terminal Strip is used to connect to the external power and leads. The DC08D mounts on the rear door of any standard DEC cabinet.

If power for the Telegraph lines is not provided externally (by the network), then a combination of the DC08D 32 Line Terminal Strip, 793 or 793A Power Supply and 893 32 line fuse panel, and DC08EB line current monitoring panel is required. The 793 is a line driving power supply for 110V and the 793A provides line driving power for 230V. The DC08EB mounts in 21" x 19" of cabinet mounting space. The 793 or 793A mounts on the rear of any standard DEC cabinet. The 893 mounts on the left side of the cabinet.

DM11-DA's, DB's and DC's can be intermixed on a DM11-AA or DM11-AC (and DM11-BB if required for modem control) in groups of four lines up to a maximum of 16 lines (i.e.: four groups). DC08CM Telegraph Interface modules are available

only for use with the DC08CS distribution panel. The DC08CS Telegraph distribution panel will not accommodate any of the DM11DA, B, or C line interface modules.

8.5.2 Operation
A. User View

1. Status and Control Registers.

Each DM11 contains four 16 bit registers. One register contains command and status information about the DM11 (e.g. receiver enable, full or half duplex select, etc.) Another register, the BUFFER Active Register (BAR), contains one bit per line. Setting a bit in the BAR initiates transmission on the associated line. The bit is cleared by the hardware when transmission is complete. A third register, the Break Control Register (BCR), contains one bit per line. Setting a bit will force that line's output to a space, causing a break condition. Clearing the bit returns the appropriate line to a normal condition (mark if the transmitter is inactive). The final register is the Base Address Register (BADR). It selects the base address of the four core tables associated with each DM11. The base address is settable to even 400 (octal) word boundaries.

2. Software Tables.

Four tables are required to be set up in the software. The base address of these tables is set by writing into the Base Address Register in the DM11. The four tables are contiguous, and require 128 (decimal) words of core, beginning on an even 400 (octal) word boundary. Two tables are required for transmit, and two for receive. The format is as follows:

Where X is the contents of the Base Address Register

X is the address of the Current Address Table (CAT - 16 decimal words)

X +20 (octal) is the Word Count Table (WCT - 16 decimal words)

X +40 (octal) is the Bit Assembly Table (BAT - 16 decimal words)

X +100 (octal) is the Circular Buffer (CB - 64 decimal words)

Figure 8-4 shows a core map of these tables, and their word formats.

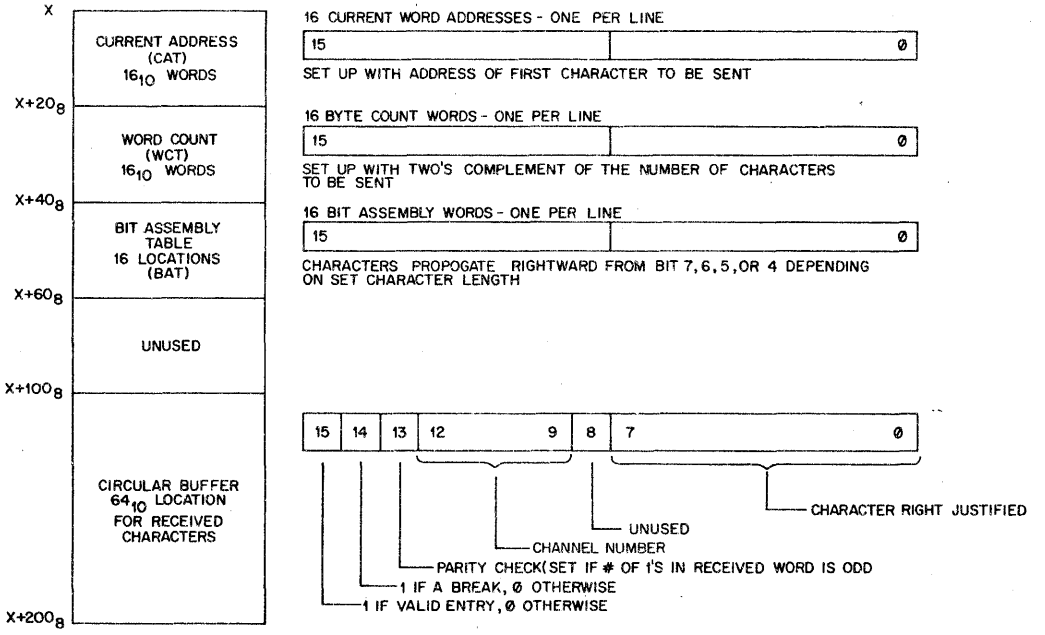


Figure 8-4 Software Table

3. Receive Procedure.

The programmmer initializes the receiver by setting the Receiver Enable bit. The Bit Assembly Table (BAT) and the Circular Buffer (CB) are used for receiving. Neither table need be set up by software. BAT need not be referenced by software; as it is merely the place in which incoming characters are assembled. Once a character is completely assembled it will be placed in the Circular Buffer and a character done interrupt will occur, if the receive interrupt is enabled. The program must then go to the Receiver Service Routine and service any entries in the Circular Buffer. Bits 0-7 of the CB entries contain the received data character right justified. The line number is contained in Bits 9-12. Bit 13 will contain a one if the received character contained an odd number of one's and this can be used for parity checking. Bit 14 will be set if the first stop bit on a character is a space; software then must determine by inspecting the character whether it is a valid break or a dropped bit. Bit 15 is the Flag Bit for the word. If Bit 15 is set then the core word contains a received character. The program must clear this bit after servicing the character in the Circular Buffer. Therefore, the Receive Service Routine sequentially processes characters until it discovers a 0 in Bit 15 of a word in the Circular Buffer. This indicates that all characters have been processed.

4. Transmit Procedure.

The Current Address Table (CAT) and the Byte Count Table (BCT) are used for transmitting. Software must create an output buffer containing each message somewhere in core. The starting address of this buffer is loaded into the word of the CAT which corresponds to the line on which the message is to be transmitted. The two's complement of the total number of characters to be transmitted is loaded into the corresponding word of the BCT as two's complement. Characters in the buffer are packed one per byte, right justified, in sequential bytes. Once the BCT and CAT entries are loaded, the appropriate bit of the Buffer Active Register (BAR) is set and transmission will proceed until all characters have been transmitted. At the end of the transmission an interrupt is generated and software checks the BAR to see which lines have completed message transmission.

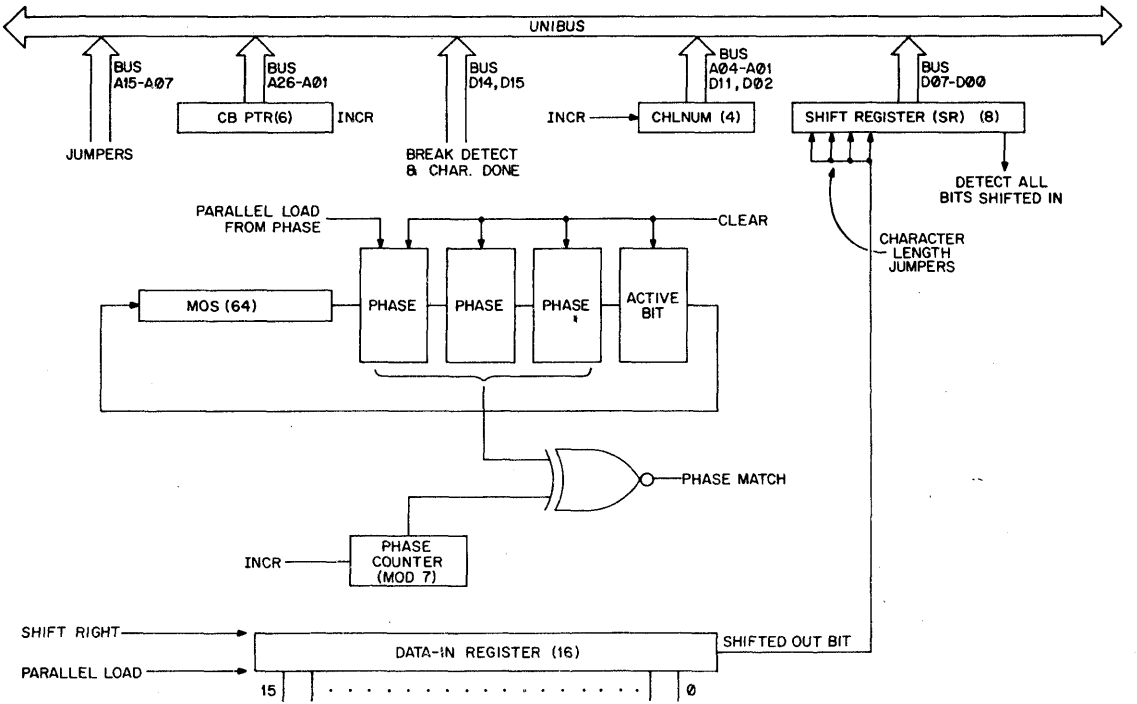


Figure 8-5 Receiver Hardware

B. Internal Operation
1. Receiver Hardware

The receiver hardware consists of seven inter-dependent sections. These registers are not directly addressable by the processor (see Figure 8-5.)

1. The DATA-IN Register is a 16-bit register which is loaded from the incoming data lines in parallel at 7 times the bit rate. The bits which contain the state of each receive line are shifted out sequentially and processed by the multiplexer.
2. The Phase Counter Register is a 3-bit register which contains the current state of the multiplexer's seven state counter.
3. The MOS Register is a 64-bit register which contains four bits of information per line.
4. The Shift Register (SR) is an 8-bit register which receives the partially assembled characters from the BAT and the new bit from the Data-In Register.
5. The Channel Number Register (CHLNUM) is a 4-bit register which is used as an Index for the BAT to obtain the proper character. It is also used to place the proper line number in a Circular Buffer entry.
6. The Circular Buffer Pointer Register (CBPNTR) is a 6-bit register which is the pointer to the next entry in the circular buffer.
7. There are also three bits of information that are used to indicate character parity, break detect, and character done.

All the incoming data lines are strobed at seven times the bit rate, and the data is stored in the 16-bit Data-In Register. For each line, four status bits are stored in a 64-bit MOS shift register (MOS). One bit indicates that the line is active, i.e., a character is in the process of being received. The other three are used as a phase recorder to determine on which of the 7-samples-per-bit-time the line is receiving, in order to insure bit sampling in the center of the received data bit.

Once the 16 samples have been taken in the Data-In register the channel 0 input bit and the four status bits for channel 0 from MOS are checked. If the channel was inactive and a mark sensed, it is still inactive. If a space is sensed a 1 is placed in the most significant phase bit but the active bit is left zero. In successive sampling 1's are propagated to the right through the four status bits until it sets the active bit which is the right most bit. In this manner four successive zero samples indicate a valid start bit and also "find"the center of the bit. At this point the contents of the phase counter (modulo 7) are loaded into the phase bits. The four-bit Channel Number Register increments from zero through fifteen (Modulo 16) and points to the line currently being serviced.

All 16 input bits are checked in this manner, every 1/7 bit time. Once a line is active then the saved phase bits are compared with the phase counter, and if a match is detected the current state of the sampled line bit is transferred from the appropriate bit of the Data-In register into the Shift Register (SR). At the same time the DM11 gets the appropriate entry from the BAT via a DATIP operation and after adding the new bit from the Data-In Register returns the updated entry to the BAT with a DATO operation. The timing for this operation depends on the

memory used. For the MM11-F 950 nanosecond core memory, the entire BAT updating process requires 1.54 microseconds and consists of a DATIP, DATO and 250 nanoseconds. The Channel Number (CHLNUM) Counter is used by the hardware as an index from the beginning of the BAT to fetch the appropriate entry. A new bit comes every seven sample times, and the characters are obtained from the BAT, assembled in the SR and re-written in core. The bits are shifted in the BAT from the most significant bit position to the least. Therefore the first bit received becomes the least significant bit of the assembly character. A one is initially placed in the most significant bit position. When this one shifts out of bit zero all the data bits have been assembled. On the next access to the BAT for that line the state of the stop code is sampled. The character is then written into the Circular Buffer, instead of the BAT, with the following format: The low-order byte contains the character, bits 9-12 contain line number, bit 13 contains a 1 if number of ones in received character is odd, bit 14 is one if no valid stop bit sensed, and bit 15 is 1 to indicate valid data entry. This operation requires a DATI to fetch the BAT entry and a DATO to make the entry into the CB plus 200 nanoseconds. For the MM1-F core this operation requires 1.9 microseconds.

Whenever any line has a completely assembled character it will place the character into the Circular Buffer and cause a character done interrupt if interrupt enable is set. The software must then sevice the CB, processing all characters found. Note that even though only one interrupt occurs more than one character may be in the CB (i.e. several lines have completed characters).

The beginning of a character will not be sensed if the start bit (spacing condition) does not exist for 4/7 of a bit time, and the four status bits in MOS will be cleared. The Circular Buffer Pointer (CBPTR) counter is the pointer in CB which indicates where the next character is to be inserted. The CBPTR increments from 0 to 77(8) and then returns to zero. Since only 60 bits of the MOS shift register carry data (the other four data bits are held in flip flops), an extra four shift pulses are generated before sampling channel 0. MOS is shifted asynchronously at a 2 mhz rate four bits before sampling each line in order to retrieve the four status bits per line. (Phase counts (3) and Line Active (1)).

2. Received Character Distortion

Received characters may contain up to 42% distortion on any bit, due to the seven times clock rate sampling. The long-term transmission bit rates may be 5% slow without affecting performance. If at least 1 1/2 stop bits are received, the speed may be 5% fast; however, if only one stop bit exists the hardware will not keep up with continuous character transmission if the characters are 5% faster than the clock rate. The DM11 clock speed is dependent on a crystal clock, and is accurate to better than .05%.

3. Transmitter Hardware

For the transmitter, one 16-bit register, the Buffer Active Register (BAR), is accessible (read/write) from the UNIBUS. Each bit corresponds to one line, and each bit is set by the software using the BIS instruction when its tables and pointers are ready. The bit is cleared by the hardware upon the completion of transmission (word count overflow). The BAR is double buffered in the hardware so that bits may be set asynchronously. (Figure 8-6)

The transmitter has associated with it two 64-bit shift registers. When the status bits associated with a particular line number are in the FF's and also if the line number is in its proper slot the hardware examines the corresponding bit in the

BAR. If it is set the hardware forces a one into one of the status bits. This indicates the active status of the line. On the next start of the bit time a space will be put on the line. On the next pass of the four bits associated with that line, with proper slot, the hardware requests the bus and on an NPR gets the current address for the line from the current address table. It then uses this address to get the character from core and gates one bit into the output register. Both of these are DATI UNIBUS operations which require 0.95μs for the MM11-F plus 300 ns for the DM11.

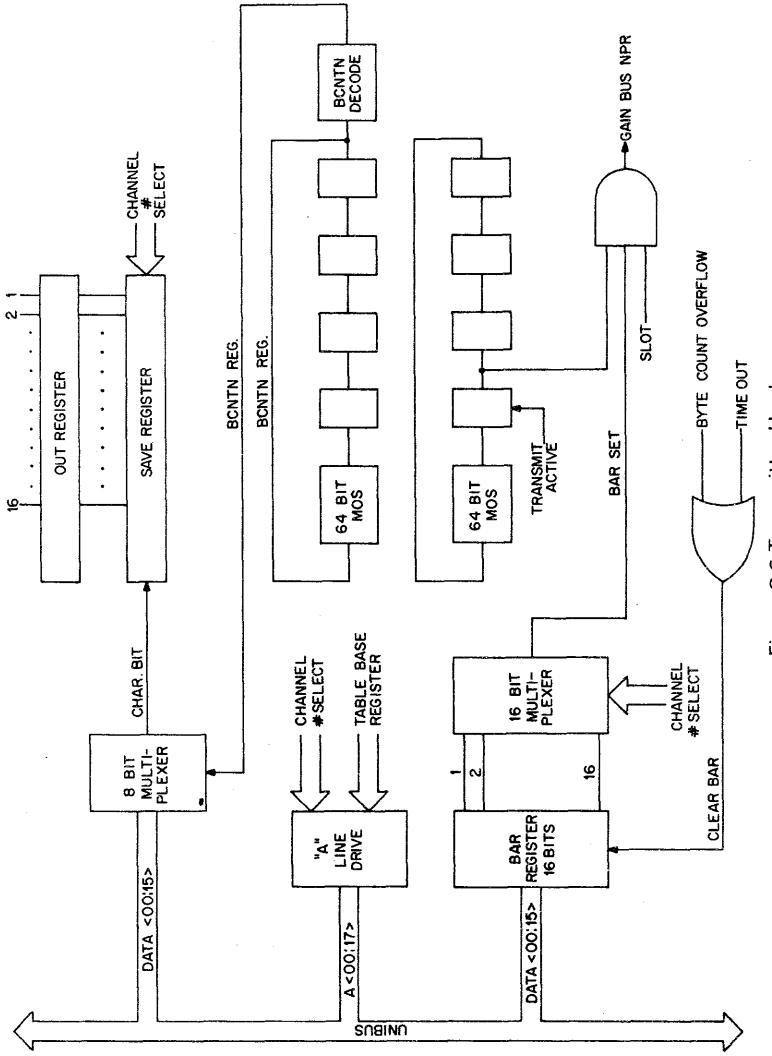


Figure 8-6 Transmitter Hardware

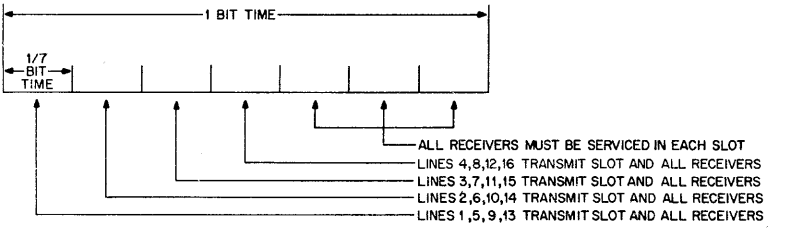


Figure 8-7 Line Service Times

Note that characters are not shifted in core memory as they are being transmitted.

This allows a single message to be transmitted on all lines. The second 64-bit register is used to count the number of bits that have been transmitted so that the end of the character may be sensed. This information is found in four bits of the MOS for each line. The transmission of characters is done asynchronously with the rest of the lines in the multiplexer, but synchronous on bit times. Maximum delay between setting BAR and start of transmission is two bit times.

During the transmission of the last data bit, the DM11 fetches the Byte Count from the Byte Count Table and increments it by one. During the transmission of the last stop bit, the DM11 fetches the Byte Address Register and increments it by one. Both of these operations require a DATIP and a DATO plus 300 nanoseconds. For the MM11-F this time is 1.9 μs. Once the word count goes to zero, the hardware clears the active bit in the BAR and signals for an interrupt. The program must then check the BAR to see which lines have finished transmission.

Breaks may be transmitted by setting the proper bit in the break control register and timing out the length of the break by some means such as line time clock.

4. Transmitter Character Distortion

Transmitted characters may be distorted by the fault condition that NPR's may not be granted quickly enough to gather data before the end of a bit time. This possibility, however, is remote because less than 4% of the processor time is used even at 1200 Baud. Overall character speed is dependent only on the crystal clock, and should be within $\pm .05$.

C. UNIBUS Utilization

The performance characteristics of the DM11 and amount of UNIBUS time which is used is a function of the processor latency and the memory cycle time. These numbers vary from processor to processor in the PDP-11 family. The numbers given here are for the MM11-F 950 nanosecond cycle memory (required for 1200 baud operation) on the PDP-11/20 or the PDP-11/15 processors.

Maximum UNIBUS Latency	3.5 microseconds
UNIBUS Time Used Per Bit (MM11-F:950 nanoseconds x2) + (300	

nanoseconds for the DM11)	2.2 microseconds
UNIBUS Time Used Per Character (8 bits of data plus 1 stop bit)	17.1 microseconds
DM11 Bit Service Time (One Latency plus 2 Memory Cycles)	5.7 microseconds

In the DM11 the critical timing is 1/7 of a bit time since all lines are sampled at seven times the baud rate. In the worst case all lines must be serviced in 1/7 of a bit time to avoid violating the distortion specification. Therefore the number of lines that the DM11 can handle is a function of the Baud rate. The number of lines as a function of the baud rate are:

Baud Rate	1/7 of a Bit Time (Microseconds)	Number of Full Duplex Lines	Number of Half Duplex Lines
1200	119	16	20
600	238	32	40
300	476	64	80
150	952	128	160
110	1298	160	216
75	1904	256	320
50	2857	420	527

The maximum percentage of UNIBUS Time used by the DM11 is different for full or half duplex operation, but independent of the Baud rate. (Note that MM11-F memory is required for 1200 Baud operation).

Assume Baud rate equal 1200; therefore the bit time is 833μs. For half duplex operation, a DM11 can service 20 lines and at 1.9 μs per service requires 38.0μs per bit time or 4.6% of the UNIBUS time. For full duplex operation, a DM11 can service 16 lines and a 1.9μs per service for receive and transmit requires 60.8μs per bit time or 7.3% of the UNIBUS time.

Note that the maximum Baud rate for the DM11 is 1200 Baud. It will not service a smaller number of lines at a higher Baud rate.

8.5.3 Programming

a. Data Selection

Each DM11-AA, DM11-AB or DM11-AC multiplexer contains four registers and hence, requires four addresses. Address space has been assigned for 16 DM11 multiplexers.

The four registers and their address are listed below for DM11A Unit xx, where xx ranges from 00 to 17.

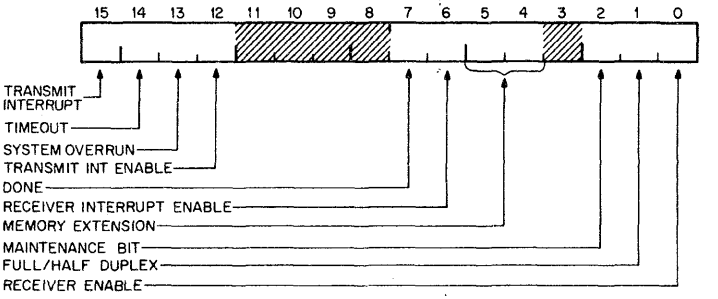
REGISTER	ADDRESS
Status Register	175xx0
Buffer Active Register	175xx2
Break Status Register	175xx4
Base Address Register	175xx6

Each DM11-AA, DM11-AB or DM11-AC requires two interrupt vectors; one for the receiver and one for output done and error. The vector addresses are assigned from 300 to 777. The DM11-A follows the KL11s, the DC11s and the DP11s in contiguous vector address assignments from 300 (i.e. the DM11-A's first vector address starts where the KL11, DC11, and DP11 leave off. If there are no KL11's

other than the console Teletype, or DC11s, or DP11s, the first DM11 (AA, AB or AC) is assigned vector address 300 and 304.

All units are shipped with the bus request line set to BR5. This can be changed in the field with a Bus Request Priority Jumper Plug.

Status Register



BIT	NAME	DESCRIPTION
15	Transmit Interrupt	Bit is set when any line buffer active register bit goes to 0. Causes an interrupt if Bit 12 is set. Bit must be cleared by the program. Cleared by reset.
14	Timeout	When set by the DM11 indicates that the DM11 tried to address non-existent memory. Causes interrupt if bit 12 is set. Read and write. Bit may be set for checking purposes. Cleared by reset.
13	System Overrun	Set by hardware when DM11 has not gained bus in time for transfers. Causes interrupt if bit 12 is set. Read and write. Cleared by reset. Bit may be set for checking purposes.
12	Transmit Interrupt Enable	Must be set for transmitter, DM11 timeout or system overrun bit to cause an interrupt. Read and write. Cleared by reset.
11-8	Not Used	
7	Done	Set when character placed in the Circular Buffer. Bit is set by the hardware and must be cleared by the program. Cleared by reset. Causes interrupt when bit 6 is set.
6	Receiver Interrupt Enable	Must be set for receiver to cause an interrupt. Read and write. Cleared by reset.

5-4	Memory Extension	Memory extension bits, are used as Bus Address A16, A17, for all transfers. Implies that data buffers and core tables must be in the same 32K bank. Read and write. Cleared by reset.
3	Not Used	
2	Maintenance Bit	When set returns the line 00 transmitter to the line 00 receiver. This has no effect on other lines. Read and write. Cleared by reset.
1	Full/Half Duplex Select	When set, disables receivers of DM11 lines that are transmitting. Read/write. Cleared by reset.
0	Receiver Enable	When clear, disables all 16 lines of the receiver by disabling receiver NPR requests, and resets Circular Buffer pointer. When set receiver is enabled. Read and write. Cleared by reset.

Buffer Active Register (BAR)
This contains one bit for each line. It is set only by using the BIS instruction. Setting a bit initiates transmission on the associated line. The bit is cleared by the hardware upon transmission of the last message character, (i.e. when the line's transmit byte count increments to zero). It may be also cleared by software to abort transmission on the associated line using the BIC instruction. All bits are read and write, and are cleared by reset.

Break Control Register (BCR)
This contains one bit for each line. Setting the bit will force that line output to space, causing a break condition. The condition remains until the bit is cleared by the processor. BIS and BIC instructions are to be used. Break timing must be done by the software. All the bits are read and write, and are cleared by reset.

Base Address Register (BADR)
This is an 8-bit register which selects the base address of all tables in core. The Base Address Register is only capable of setting the upper eight bits of the word thus only even 400 word boundaries can be used. Bits are read and write and are not cleared by reset.

B. Modem Control Section
Each DM11-BB modem control multiplexer contains two registers and requires two addresses. Address space has been assigned for 16 DM11-BB modem control multiplexers. The first DM11-BB is at 170500. The second starts at 170670, etc. to the 16th at 17. The two registers and their addresses are listed below for DM11-BB unit xx.

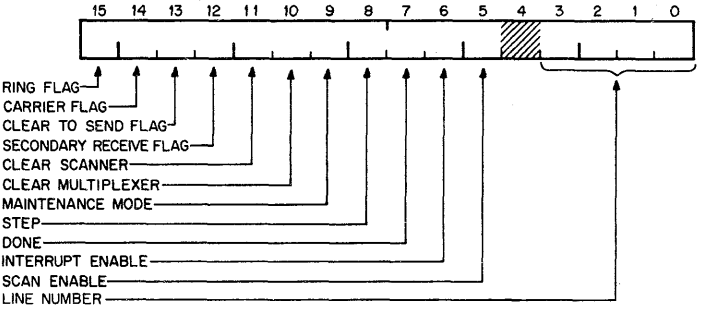
REGISTER	ADDRESS
Control and Status Register	170XX0
Line Status Register	170XX2

Each DM11-BB requires one interrupt vector. The vector addresses are assigned from 300 to 777. The DM11-BB follows the KL11s, DC11s, DP11s, DM11-As, DN11s in contiguous vector address assignments from 300. If there are no KL11s

other than the console Teletype, or DC11s or DP11s, or DN11s, the first DM11A is assigned vector addresses 300 and 304 and the first DM11-BB is assigned vector address 310.

All units are shipped with the bus request line set to BR4.

Control and Status Register (XX0)



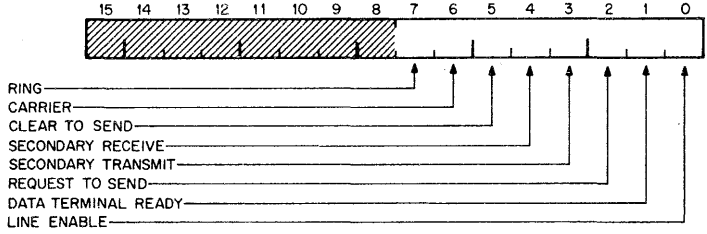
BIT	NAME	DESCRIPTION
15	Ring Flag	When DONE is set this flag indicates that a Ring OFF to ON transition has been detected at line number. This bit is read only and is cleared by Initialize and clear scan
14	Carrier Flag	When DONE is set this flag indicates that a Carrier Flag transition has been detected at line number. This bit is read only and cleared by Initialize and clear scan.
13	Clear to Send Flag	When DONE is set this flag indicates that a clear to send transition has been detected at line number. This bit is read only and cleared by Initialize and clear scan.
12	Secondary Receive Flag	When DONE is set this flag indicates that a Secondary Receiver transition has been detected at line number. This bit is read only and cleared by Initialize and clear scan.
11	Clear Scanner	Clears all Read/Write functions- -additionally the Scan Decoder is set to 0 and the scan memory logic is cleared. This function is useful for having the hardware test and interrupt on all lines that have an on condition. Clear occurs when a one is written into this bit position.

10	Clear Multiplexer	Clear Multiplexer clears the request to send, Terminal Ready, Secondary Transmit and Line Enable flip flops when a ONE is written into this bit position.
9	Maintenance Mode	This bit, if set to a ONE, conditions the SCAN Input (Ring, Clear to Send, Carrier, and Sec Rx) to a ONE or ON state. Utilizing Step or SCAN EN with Maint Mode will exercise 100% of the Scan Logic (not the data multiplexers.) This includes the Interrupt Circuits (M7820) and the Address Selector (M105). This mode provides a diagnostic feature, as well as an On-Line test facility for the DM11-BB's interaction with the UNIBUS. This bit is read/write and is cleared by Initialize or Clear Scan.
8	Step	Step, when set to a ONE, causes the SCAN to increment the line number and test that line for interrupts causing transitions. Step may be used in place of Scan Enable but care should be exercised that the scan rate is great enough (milliseconds) such that double carrier transitions will be detected. Additionally, DONE does not inhibit STEP. A STEP requires 1μ + 10% to excute. This bit is WRITE ONE'S only.
7	Done	The DONE flag set to a ONE indicates that the hardware SCAN has detected a transition requiring an Interrupt to the program. An Interrupt will occur if Interrupt Enable is On (a ONE). Additionally, DONE set to a ONE inhibits the SCAN clock and makes availabe to the programmer: a. The line number that caused the interrupt b. The status of the flag (4 bits). c. Modem Status (8 bits) The SCAN will be released again when DONE is reset. This bit is R/W and cleared by initialize.
6	Interrupt Enable	Allows interrupts on Priority four if set to a ONE. This bit is Read/Write and cleared by Initialize.
5	Scan Enable	A ONE allows the scan to test all lines for RING, CARRIER. CLEAR TO SEND, and Sec. Receive Interrupts. If the Scan En filp flop is negated while the ring counter is cycling (i.e. DONE not SET) the Ring Counter will come to rest in 1 μ +10% (MAX). The LINE register must not be

changed during this period or line number transitions may be lost. This bit is Read/Write and cleared by Initialize.

4	Not Used	
3-0	Line Number	The Line Number bits are the Binary Addresses for the DM11-BB's 16 lines (0-15) as follows: Bit 3210 — Line Number 0000 — 0 0001 — 1 etc. — etc. 1111 — 15 If the Scan is cleared by initialize or Clear Scan, the Line Number Register will settle in 16 μ + 10% When settled, the Line Number Register will be set to Line Number 0 (0000). Note when the SCAN is enabled (or STEP) the next line to be tested will always be line #1. These bits are READ/WRITE and are cleared by INITIALIZE and by Clear Scan.

Line Status (170XX2)



BIT	NAME	DESCRIPTION
7	Ring	Modem status of the RING lead. This bit is Read only.
6	Carrier	Modem status of the carrier lead. This bit is read only.
5	Clear to Send	Modem status of the clear to send lead. This bit is ready only.
4	Secondary Receive	Modem status of the secondary receive lead. This bit is read only.
3	Secondary Transmit	When set, presents a MARK to the Modem's Secondary Transmit lead. This lead is Read/Write and is cleared by Initialize and Clear MUX.

2	Request to Send	This lead is used to condition the modem for transmit if all other conditions are met. This bit is read/write and cleared by Initialize and Clear MUX.
1	Data terminal Ready	This lead allows the modem to enter and maintain data mode. This Bit is Read/Write and cleared by Initialize and Clear MUX.
0	Line Enable	This bit Enables the state of Ring, Carrier, Clear to Send and Sec Rx to be sampled by the program and for being tested for transitions. This bit is Read/Write and is cleared by Initialize and Clear MUX.

8.5.4 Specifications

Operating Mode:	Full or half duplex operation selected under software control.
Data Rate:	From 45 to 1200 Baud Jumper selectable per 16 lines. Baud rate must be specified with order.
Data Format:	One start bit. Character size jumper selectable for 5-, 6-, 7-, or 8- level code. Stop code is jumper selectable for one or two stop bits. (Must be specified with order)
Order of Bit Transmission:	Low order bit first.
Parity:	Computed on incoming data.
Mode of Operation:	DMA (NPR) character assembly in core memory for received characters. DMA (NPR) message transmission from core memory.
Data Buffering:	One 64-character circular Buffer per DM11.
Distortion:	Input: can tolerate up to 42% per character. Output: less than 2% per character.
Bus Load:	Complete mulitplexer represents a 1 unit load to the PDP-11 UNIBUS. The UNIBUS can handle 18 unit loads. For more than 18 unit loads, a bus extender, DB11-A, must be used.
Data Signals:	Line Adapter Type — Output Signals DM11-DA — 20mA. Current loop for four teletypes, maximum distance 1500 feet. DM11-DB — EIA RS-232-C and CCITT for four lines (data only)

DM11-DC EIA RS-232-C and CCITT for four lines, data and modem control signals.
DC08 CM ±80Volts; ± 100 mA for two lines.

Control Signals:

Line Adapter Type Control Signals
DM11DA Data only
DM11DB Data only
DM11DC All control leads from the Bell 103, 202 and 811B or equivalent modems. (Except Data Set Ready). All leads are EIA RS-232-C and CCITT compatible.
DC08CM Data only.

Physical: Two system units for up to 16 lines all operating at the same speed, plus a 5 1/4"x 19"external mounting panel.

Environment: Temperature is +40°F - 120°F and relative humidity is up to 95% non-condensing.

Power: 4.9 Amps of +5V and 50 ma of -15V from the PDP-11. All power for the DM11-DA, DM11-DB and DM11-DC are provided by an external power supply which is provided with the DM11-AA. Logic power for the DC08CS is provided by an external power supply which is included with the DC08CS. Line driving power if needed is supplied by an optional 793 or 793A power supply.

8.5.5 Ordering Information
A. Local Teletypes

DEC NO.	PREREQUISITE	DESCRIPTION
DM11-AA	PDP-11	Asynchronous 16-line single speed multiplexer and distribution panel. Includes space for mounting up to four line adaptors (16 line interfaces). Order must specify Baud rate, character length, and number of stop bits desired. If not specified, unit will be shipped with 110 Baud, 8 bits per characters, and 2 stop bits (standard model 33/35 Teletype configuration.) Power supply is 110v, 60Hz, 600w, requirement.
DM11-AC		Same as DM11-AA except 230V, 50Hz, 600w.
DM11-DA	DM11-AA or DM11-AC	Line Adapter for four Teletype lines (data only).

B. Private Line Modems (No Control) or Local EIA Terminals

DEC NO.	PREREQUISITE	DESCRIPTION
DM11-AA	PDP-11	Same as above
DM11-AC		Same as above
DM11-DB	DM11-AA or DM11-AC	Line Adapter which implements four EIA/CCITT lines (data only). Includes four 25-foot modem cables.

Note that the DM11-DB can be used on a switched network system. This requires that the modem have Data Terminal Ready strapped on. The modem will answer a call automatically. Not provided in this type of operation is the ability to not answer a call, the ability to initiate a disconnect by the computer and the ability to sense an intermittent carrier.

C. Switched Network Modems

DEC NO.	PREREQUISITE	DESCRIPTION
DM11-AA	PDP-11	Same as above
DM11-AC		Same as above
DM11-BB	DM11-AA or DM11-AC	16-line modem control multiplexer provides control leads for 103, 202 or equivalent modems. Mounts the DM11-AA.
DM11-DC	DM11-BB, -AA, or -AC	Line Adapter which EIA/CCITT lines equipped with modem features includes four 25-foot modem cables.

D. Telegraph Line Interfaces

DEC NO.	PREQUISITE	DESCRIPTION
DM11-AB	PDP-11	Asynchronous 16-line single speed multiplexer and connecting cable to DC08CS mounting panel. (Does not include the DC08CS) Order must specify the Baud rate (up to 1200 Baud for 16 lines.) If no speed is specified 110 Baud, will be supplied. Up to 2 DM11-AB plug into one DC08CS.
DC08CS	DM11-AB	Telegraph and Telex line Adapter distribution panel. Mounts line adapters for interfacing between the DM11-AB and telegraph or Telex lines. Accommodates up to 16 dual solid state telegraph line adapters, type DC08CM. (Each DC08CM provides two Telegraph line interfaces).
DC08CM	DC08CS	Dual solid state telegraph line adapter. This unit is used with either externally supplied neutral or polar line power or internally supplied line power (793 or 793A).
DC08EB	DC08CS, DC08CM 793 or 793A and 893	Line Current Adjusting Option. Provides rheostats on each send and receive lines for adjusting send and receive line current. Meter is provided for current monitoring. Can drive unipolar or bipolar lines ± 45v to ±80v and ±80ma. per line
DC08D	DC08CS, DC08CM	Line Terminator Panel. Provides screw terminal connection points for interfacing the DC08CM Telegraph Line Adapters to telegraph lines. Can accommodate up to 32 lines, with four connections provided for each. Cabling allows unipolar or bipolar operation in groups of 16 lines.
793	DC08CS, DC08CM	Line Power Supply and power supply for driving a maximum of 32 telegraph lines, (transmit only). Output is ± 80 volts at 400 watts. Power requirements are 115v, 60Hz, 700 w,
793A	DC08CS, DC08CM	Same as 793 except 230V, 50Hz, 700 watts.
893	DC08CS, DC08CM 793 or 793A	Fuse panel for up to 32 lines. Fusing is for the transmit lines.

8.6 FULL DUPLEX 8-BIT ASYNCHRONOUS LINE INTERFACE UNIT-KL11

The KL11 will connect the PDP-11 with full duplex 8-bit asynchronous serial lines and is used with Teletypes or other terminals. The standard interface provides a 20 milliamp. current loop output and a contact closure input for interfacing to standard Teletype circuits. The KL11 can be modified to interface to local EIA terminals by using the DE11A. The DE11A provides E1A data leads and connects to the local terminal via a 25-pin female connector. This allows EIA terminals which have a 25-pin male connector to plug directly into the DE11-A. (Note that the 25-pin female connector of the DE11-A will not plug directly into modems which also have 25-pin female connectors. To interface to asynchronous modems use the DC11 or DM11.)

8.6.1 Programming

Each KL11 contains four requests and hence, requires four addresses. Address space has been assigned for 16 KL11s. In addition to the console Teletype which is discussed in Chapter 2. The four registers and their addresses are listed below for KL11 unit XX where XX ranges from 50 to 67.

REGISTER	ADDRESS
Receiver Status Register	776XX0
Receiver Buffer Register	776XX2
Transmitter Status Register	776XX4
Transmitter Buffer Register	776XX6

The bit assignments are the same as the console Teletype described in Chapter 2. Each KL11 interface requires one interrupt vector. The vector addresses are assigned from 300 to 777.

All KL11s are shipped with their bus request line attached to BR4. This is changeable in the field by using a Priority Jumper Plug.

8.6.2 Specifications

MODELS AVAILABLE

KL11A:	Control for ASR and KSR Teletypes - Full Duplex 110 Baud.
KL11B:	Full Duplex Asynchronous Line Interface Unit 150 Baud
KL11C:	Full Duplex Asynchronous Line Unit 300 Baud
KL11D:	Full Duplex Asynchronous Line Unit 600 Baud
KL11E:	Full Duplex Asynchronous Line Interface Unit 1200 Baud Send, 100 Baud Receive
KL11F:	Full Duplex Asynchronous Line Interface Unit 2400 Baud
DE11A:	EIA Level, RS-232-C Line Adapter for VT05,VT06 or other 8-Bit EIA Level Devices. (Requires KL11 Interface). Mounts on KL11
Data Format:	One Start Bit. 8 Data Bits, 2 Stop Bits on KL11-A and 1 Stop Bit on KL11B through KL11F.
Order Transmission:	Low order bit first
Bus Load:	One line unit represents a one unit load to the PDP-11 UNIBUS. The UNIBUS can handle unit loads. For more than unit loads a Bus Extender, DB11-A must be used.
Data Signals:	For KL11 20 ma. output contact closure input. For KL11 plus DE11A. Conforms to EIA RS-232-C

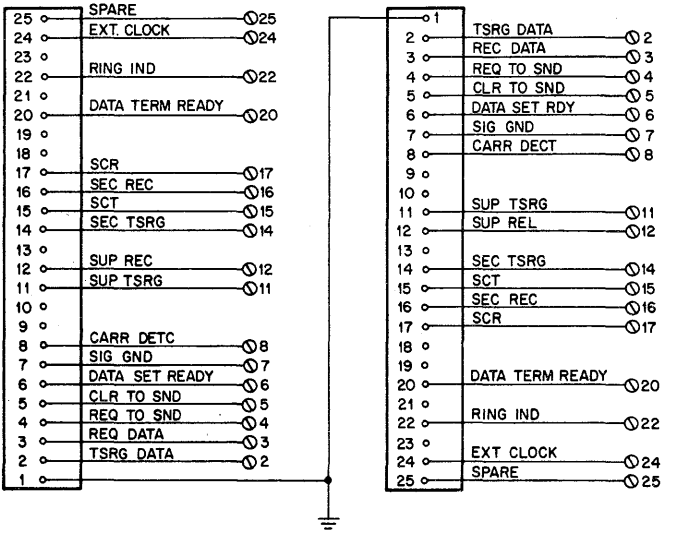
Physical Connection:	For KL11 pin Mate-N-Lock connector mounted on the KL11. For KL11 plus DE11A 25-foot cable with 25-pin female connector (Accepts 25-pin EIA RS-232-C compatible 25-pin male connector from terminals such as a VT05, VT06 or any other 8 bit terminal which are designed to plug into a modem.)
Space Required:	DD11A small peripheral interface slot. (1/v of a DD11A)
Power Required:	1.6 Amps of +5 volts
Temperature/Humidity:	100 Ma. of +15 Volts 0-40° C with 20 to 90% noncondensing humidity

8.7 ASYNCHRONOUS NULL MODEM H312A

The H312 null modem allows a user to connect a terminal device to a computer without the use of two modems as would be normally required. It consists of two female 25-pin data-phone sockets mounted on a printed circuit board with the 15 most commonly used wires brought out to split lugs in the center of the board. The split lugs allow the user to interconnect the two sockets in any way he wishes as long as the pins used are on the split lug interconnection points.

To use the H312 the user determines the proper handshaking procedure that is used between his two terminals and then wires the H312 to deliver the proper procedure. Usually the transmit and receive leads of the opposite sides are interchanged and the control loads are strapped to give the proper handshake.

The following leads are available to the user:



PART I
Chapter 9

Data Acquisition and Control Options

9.1 LOW LEVEL ANALOG INPUT SUBSYSTEM - AFC11

9.1.1 Introduction

The AFC11 is a flexible, high performance, differential analog input subsystem for IDACS-11 industrial data acquisition control systems.

The AFC11 system multiplexes up to 1024 differential input analog signals, selects gain, and performs a 13-bit analog-to-digital conversion at a 200 channel per second rate under program control. Three signal conditioning modules and eight program-selectable gains allow the system to intermix and accept a wide range of signals: low level (10mv f.s.), high level (100.0v f.s.), and current inputs (1 to 50 ma f.s.).

Designed for accurate and reliable operation in demanding industrial environments, the AFC11 achieves high isolation and common mode noise rejection through relay switched capacitor multiplexing. The subsystem also simplifies input wiring, requiring only simple twisted pairs which connect to screw terminals.

Modularly constructed in eight-channel standard hardware units, the AFC11 is easy to configure to user applications, and simple to expand.

The analog input subsystem is particularly suited for data acquisition in the high bnoise environments encountered in process monitoring and control, production testing and laboratory applications. In such environments common and normal mode noise, cabling and grounding problems can greatly affect the operation of such transducers as thermocouples, strain gages, analytical bridges, and industrial milliamp current transmitters. These problems can also affect the accuracy and performance of the measuring system.

In typical applications, use of ungrounded sensors could cause common mode voltages of up to 150 volts peak-to-peak (at power line frequency) to appear on the input signal leads to the measuring system. For example, if thermocouples become ungrounded during operation, large common mode voltages can appear in coincidence with the signal. The design features of the AFC11 allow either floating or grounded signal sources thus insuring reliable, trouble-free operation. Due to the flying capacitor design, the system tolerates common mode voltages in excess of 200 volts. FET solid-state multiplexers, in contrast, can be seriously damaged with common mode voltages over 25 volts.

9.1.2 System Organization

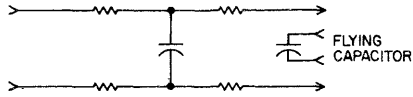
The AFC11 system is completely modular for ease of system configuration and expansion. For applications requiring 128 channels or less the system is available in a single cabinet configuration. Systems requiring greater than 128 but less than 512 channels are housed in a dual cabinet configuration - one cabinet to mount the electronics and one for the screw terminal connectors. Two dual cabinet con-

figurations, each containing 512 channels, are required to implement a maximum system of 1024 channels.

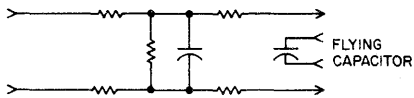
The sytem's electronics cabinets are organized in files. The first file in the system is a master file which contains the computer interface, system timing and control, an A/D converter, a programmable gain differential amplifier, and address decoding hardware for selection of up to 32 channels. The master file may also contain three additional file units, each providing address decoding and analog bus isolation for up to 32 channels. The hardware for each 32 channel group is implemented by adding up to four eight-channel pairs of multiplexer/signal-conditioning modules and the required screw terminal cable assemblies - one for each module pair. Fully implemented, the master file contains 128 channels.

Expansion beyond 128 channels is by addition of expander files. Each expander file contains a programmable gain amplifier and provision for a total of 192 channels in six file units.

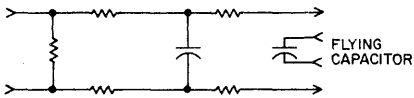
A file unit contains from one to four eight-channel Multiplexer Modules (Model BA150), each of which requires an eight-channel input signal conditioning module. The conditioning modules, which connect to screw terminal blocks via cable assemblies, are available in three types:



Direct Input Module (Model BA903) provides eight-channels of normal mode input filtering with a break frequency of 2.5 Hz. Attenuation at 60 Hz is greater than 50 db.



Voltage/Voltage Input Module (Model BA904) provides 8 channels of 10:1 attenuated input with the same normal mode filtering as direct input. Maximum full scale input is +100 volts.



Current/Voltage Input Module (Model BA905) scales eight-channels of 50, 20, or 5 m.a. full scale current inputs to 0.5, 0.2, or 0.05 volts full scale and provides the same normal mode filtering as the direct input module.

9.1.3 Flying Capacitor Multiplexing

The flying capacitor multiplexing technique permits micro-volt signals to be isolated, switched and digitized by an analog-to-digital converter with a high degree of noise immunity.

The Flying Capacitor is a two pole RC filter network in which a second or "flying" capacitor is charged, then isolated and switched to the measuring circuit. Since the source is never directly connected to the measuring circuit, extremely high isolation is achieved.

Lo-pass filtering per point (2.5 Hz cutoff) plus the high isolation of the flying capacitor technique provide high common mode noise rejection (120 db at 60 Hz) without requiring expensive individually-shielded input wiring.

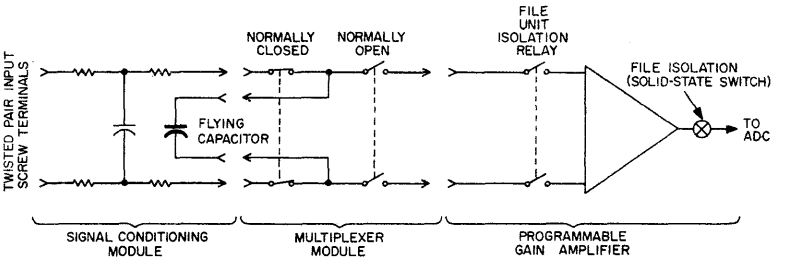


Figure 9-1 - Typical File Unit Channel

9.1.4 Programmable Gain Control Channel Selection

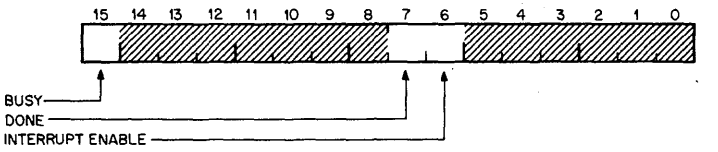
Both gain and channel are under program control. A 16-bit Channel Address Gain/ Select Control word is transferred from the IDACS-11 processor to the AFC11 Channel/Gain Register (AFCG). The multiplexer channel address is contained in bits 0-10 and decoded to select 1 out of 64 File Units (6 bits) and 1 out of 32 channels (5 bits) within the File Unit. The programmable gain control on the input amplifier is buffered and FET switched for reliability. Amplifier gain is selected by bits 13-15. For the Gain vs Bit Table, see Programming, Paragraph 9.1.5.

When a channel is selected, the input signal is isolated and the File Unit isolation relay closes to connect the charged capacitor to the Programmable Gain Amplifier. The amplifier is connected to the analog bus and ADC by closing the file isolation switch. Timing is initiated which allows the switches to settle and conversion to begin.

9.1.5 Programming

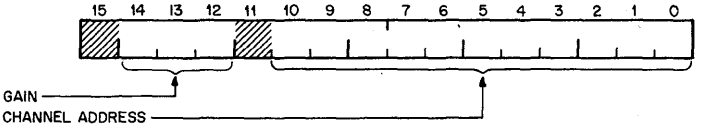
REGISTER	ADDRESS
Control and Status Register (AFCS)	772570
Data Buffer Register (AFBR)	772572
Maintenance Register (AFMR)	772576

Control and Status Register (AFCS)



BIT	NAME	DESCRIPTION
15	Busy	Set by INIT or LOADING MX Channel Gain Register. Reset by A/D DONE.
14-8	Unused	
7	Done	Set by A/D DONE. Reset by reading Data Buffer Register.
6	Interrupt Enable	Set under program control. Reset by INIT or under program control.
5-0	Unused	

Multiplexer Channel/Gain Register (AFCG)



BIT NAME DESCRIPTION

15 Unused

14-12 Gain — Sets amplifier gain according to the following table. Cleared by INIT. (READ/WRITE).

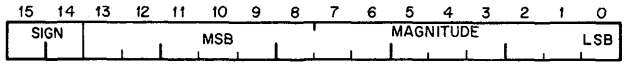
Bit/Gain Table

15	14	13	Gain
0	0	0	1000
0	0	1	200
0	1	0	100
0	1	1	50
1	0	0	20
1	0	1	10
1	1	1	2

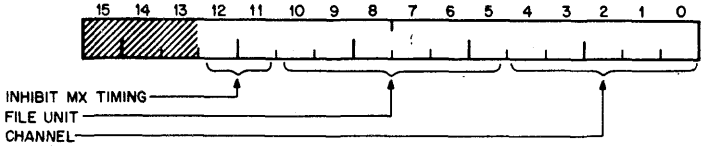
11 Unused

10-0 Channel Address — Selects multiplexer channel. Bits 10-05 select 1 or 64 file units. Bits 04-00 select 1 of 32 channels in a file unit. Cleared by INIT. (READ/WRITE).

Data Buffer Register (AFBR)



Maintenance Register (AFMR)



This Read/Write Register is for diagnostic purposes only. Permits checking of channel address by reading back decoded bits.

9.1.5 Specifications

Analog Input Specifications

Number of Inputs:	8 to 1024, in groups of 8
Type:	differential, 2 wire twisted pair
Connection:	solder lug, or screw terminal

System Performance

Resolution:	Sign + 12 bits (2's complement)
Accuracy: (for direct input)	±.025 of f.s. or ±15 μV (whichever is larger) ±1/2 l.s.b.
Repeatability: (3 sigma)	±3 v, same channel or ±15 ±v, channel-to-channel (whichever is larger) ±1/2 l.s.b.
Scan Rate, Including A/D Conversion:	200 channels/second, maximum (20 samples/second, same channel)
Normal Mode Rejection:	>50 db for frequencies 60 Hz or above
Common Mode Rejection:	>120 db DC to 60 Hz
Common Mode Voltage Tolerance:	200 volts
Input Overload:	Amplifier fused against overload
Effects of Overload:	Recovers to within stated accuracy for next channel.
Channel-to-Channel Isolation:	10^{12} ohms at DC, Channel-to-channel. 10^{12} ohms at DC, channels on same multiplexer module.

Gain Accuracy: ±0.02%
Gain Linearity: ±0.01%
Temperature Coefficient: ±.005%/ °C or better

Priority Level: BR4
Vector Address: 134

Environment/Mechanical

Operating Temperature:	10 °C to 55 °C
Cooling/Filtering:	Dust filters BLOWER FANS, BOTTOM EXHAUST.
Size:	Each cabinet has a 21 inch Wx30 inch Dx72 inch H
Weight:	750 pounds approx. = Dual Cabinet (512 channels)
Power:	115/230 volts, 40 to 440 Hz, single phase 30 amps.

9.2 ANALOG TO DIGITAL CONVERSION SUBSYSTEM AD01-D

9.2.1 Introduction

The AD01-D is a flexible, low-cost multichannel analog data acquisition option which interfaces directly to PDP-11 computers. When it is under computer or external clock control, the AD01-D provides 10-bit digitization of unipolar high-level analog signals having a nominal full-scale range of 0 to + 1.25, + 2.5, + 5.0 or + 10.0 volts. An optional sign-bit addition allows 11-bit bipolar operation. Programmable input range selection extends the AD01-D's dynamic range at moderate sampling rates to the equivalent of 13 bits for unipolar signals or 14 bits for bipolar signals.

An optional sample-and-hold amplifier reduces the conversion aperture to 100 nanoseconds.

Available as a factory or field-installed PDP-11 option, the standard AD01-D consists of an expandable solid-state input multiplexer, programmable input range selector, A/D converter, control, and bus interface in a single 5-1/4-inch rack-mountable assembly plus a separate logic power supply. The multiplexer can be expanded by adding 4-channel modules up to 32 channels. An expansion multiplexer may be added to provide a maximum configuration of 64 channels.

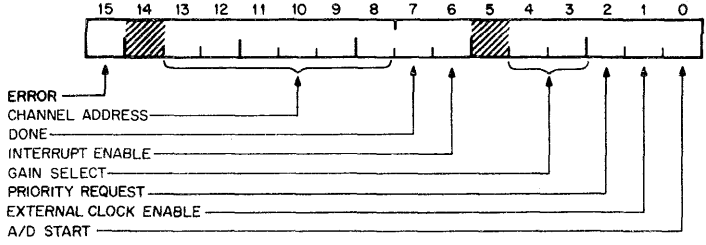
The subsystem is well suited to a variety of tasks - testing, monitoring, logging, and analytical instrument data reduction - in both laboratory and manufacturing environments. It is also a first choice with OEM's and system contractors as an economic and efficient system component for sophisticated data acquisition systems.

9.2.2 Programming

REGISTER	ADDRESS
Control and Status Register	776770
Data Register	776772

Control and Status Register

Transfer of a 16-bit control word from the PDP-11 to the Control and Status Register (ADCS 776770) establishes the operating conditions of the AD01-D.



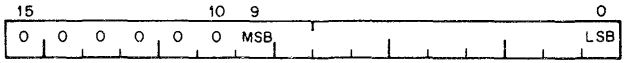
BIT	NAME	DESCRIPTION
15	Error	Set when new conversion is initiated while a conversion is being performed. Interrupt is produced when interrupt bit (bit 6) is enabled.
14	Unused	
13-8	Channel Address	Selects 1 of 32 multiplexer channels.

7	Done	Set upon completion of conversion and reset upon reading data register.
6	Interrupt Enable	Program selectable interrupt mode. Interrupt produced on A/D done (bit 7) or error (bit 15) when selected.
5	Unused	
3-4	Gain Select	Selects input gain range of 1, 2, 4, or 8.
2	Priority Request	Program can select priority request BR7 or BR6,5,4.
1	External Clock Enable	Conversion initiated by external clock when bit is set.
0	A/D Start	Conversion initiated by program when bit is set. (Conversion is also started when a new multiplexer channel (and gain) is selected, except when external clock is enabled.)

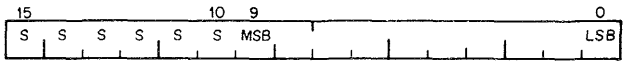
One input channel is selected by the multiplexer and connected to a highly-linear programmable gain slector, which scales the input range to +10 volts full-scale.

The scaled 10 volt output is directed to the summing junction of the A/D converter input through the sample-and-hold and sign-bit options, if installed. In 10 μ sec, the A/D converter degitizes the analog voltage at its input into a 10-bit binary code, using the successive-approximation technique. The sign-bit option permits conversion of bipolar inputs (0 to ± 1.25, ± 2.5, ± 5.0, or ±10.0 volts) to an 11-bit 2's complement code with an extended sign format.

The A/D converter Data Register (ADDB-776772) transfers data to the PDP-11 in the following format.



OUTPUT WORD FORMAT-UNIPOLAR OPERATION



OUTPUT WORD FORMAT-BIPOLAR OPERATION

Bits 15 to 10 are tied together, and are "0"in the standard unipolar configuration. With the sign bit option, bits 15 to 10 indicate the sign of the input voltage.

OUTPUT NOTATION TABLE

Analog Input Voltage	Unipolar	Bipolar
-10.0		176000
-5.0		177000
0.0	000000	000000
+ 5.0	001000	001000
+ 9.9902	001777	001777

*For 10 volt full scale input range. Divide by appropriate gain factor for other input ranges.

Each multiplexer channel switch consists of an enhancement mode MOSFET, which is normally open when unselected or when system power is removed. These switches provide overload protection up to ± 20 volts, and signal protection against electrical short-circuit.

Specifications

Resolution:	Unipolar 10 bits, or 1 part in 1024 Bipolar (option) sign + 10 bits.
System Accuracy:	0.1% of f.s. input
Quantizing Error:	±1/2 least significant bit
System Conversion Time: includes Channel and gain	Unipolar: 22 μsec Bipolar: 29 μsec
Sample Hold:	Acquisition: 5 μsec to ±0.01% of f.s. step Aperture: 100 nanoseconds
Analog Input Channels:	4 minimum, expandable to 32 in groups of 4
Input voltage range: (program selectable)	Unipolar: 0 to + 1.25, + 2.5, + 5.0, + 10.0v.f.s. Bipolar (option): 0 to ± **1.25**, ± 2.5v, ± 5.0, ± 10.0v.f.s.
Input Impedance:	1000 megohms in parallel w/20 p.f.
Input Isolation:	Enhancement mode MOSFET switches, "off' when unselected or power off.
Analog Input Connectors:	Plug-in cable-module
Channel Selection: (program selectable)	6 bit address
Cross channel attenuation:	78 db, DC-80Hz for 20 volts p-p signals, 100 ohm source impedance
Input Gain:	Program selectable
Modes of Operation:	Interrupting/non-interrupting (program selectable) Synchronous (Program control) Asynchronous (external clock enable + 2.0v minimum into Schmidt trigger, repetition rate, 60k Hz maximum.)

Environment

Temperature	0 to + 55 °C operating -25 to + 85° C storage
Humidity:	to 90% w/o condensation

Power Requirement

AC Input Voltage:	115/230 volt ± 10%
AC Input Frequency:	47 to 63 Hz, single phase
Power dissipation:	less than 75 watts

Packaging

Size:	5-1/4"H x 19"W x 12"D rack mounted panel (plus separate power supply)
Weight:	15 pounds

Expansion/Installation

Multiplexer expansion or option inclusion in the basic AD01-D is by module insertion into prewired slots.

Priority level:	**BR 7,6,5,4**
Vector Address:	**130**

9.3 DIGITAL TO ANALOG CONVERSION SUBSYSTEM AA11-D

9.3.1 Introduction

The AA11-D is a low cost, high performance multichannel digital to analog conversion subsystem for PDP-11 computers.

Interfacing directly to the PDP-11 UNIBUS, the AA11-D controls up to four single buffered, 12 bit bipolar digital to analog converters. Each BA614 converter, which includes output amplifier and reference voltage source, is contained on a plug-in module and provides 10 ma current output at ± 10 volts. Full scale output voltage is trimpot adjustable from ± 1v to ± 10v in two ranges.

Storage scope, display scope, and light pen control options are available for the AA11-D. These options provide Z axis blanking for intensity control and require two D/A converters to control X and Y trace coordinates.

Available as a factory or field installed option, the AA11-D fully implemented with four digital to analog converters and a scope control option, is contained in a single System Unit. A rack mountable power supply is separate.

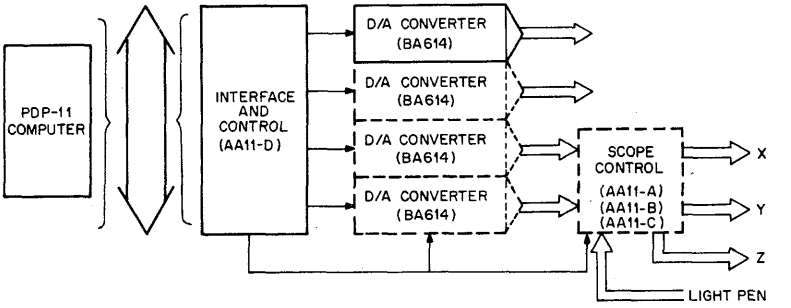
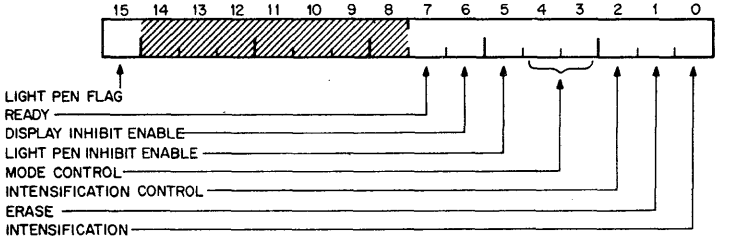


Figure 9-2 - AA11-D Subsystem

9.3.2 Programming

REGISTER	ADDRESS
Command and Status Register (CSR)	776756
Data Register DAC1	776760
Data Register DAC2	775762
Data Register DAC3	776704
Data Register DAC4	776766

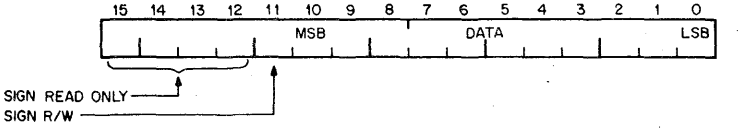
Control of the digital to analog converters is through the Command and Status Register.



BIT	NAME	DESCRIPTION
15	Light Pen Flag	If bit 05 is "1", light pen signal causes interrupt. Cleared by INIT and reading the register. Read only.
14-8	Not Used	
7	Ready	Scope is ready for service, because of INTEN or ERASE commands or X or Y has been loaded. Interrupt occurs if bit 06 is "1." Bit 07 is set by INIT and cleared by displaying new point. Read only.
6	Display Inhibit Enable	Permits interrupts to occur when intensification or erasure is completed. This bit is set by program control and cleared by INIT. Read/Write.
5	Light Ien Inhibit Enable	Permits interrupts to occur when signal is received from light pen. This bit is set by program control and cleared by INIT. Read/Write.
4-3	Mode Control	Determines intensification on loading X or Y.
2	Intensification Control	Selects Stored Mode or High Intensity Mode depending on scope used. Read/Write
1	Erase	Erases storage scope display. Sets READY bit 7 at end of erase.
0	Intensification	Delays display until scope deflects to new X,Y values. Then strobes intensification (Z axis) and sets READY bit 7.

Data Registers (DAC)

DAC1 and 2 may be used either in conjunction with the scope or for D/A channels. DAC3 and 4 may be used for additional D/A channels.



BIT	NAME	DESCRIPTION
15-12	Sign	Read only (2's complement)
11	Sign	Read/Write (2's complement)
10-0	Data	Read/Write.

9.3.3 Specifcations For D/A Converter (BA614)

Digital Input:	11 bits + sign, 2's complement code.
Digital Storage:	Single buffered.
Update Rate/Channel:	50KHz
Analog Output Voltage:	2 continuously adjustable full scale ranges: 1v to 5v and 5v to 10v
Current:	+ 10ma
Gain Accuracy:	±0.025% of full scale (25 C)
Linearity:	±1/2 l.s.b.
Zero Offset:	Adjustable to zero
Settling Time:	20 μs max. to within 1/2 l.s.b. for full scale step change(at output connector with zero capacitance loading).
Output Impedance:	Less than 1 ohm.
Temp Coefficient:	±50 μv/ °C- zero offset and
(after 5 min. warmup)	±.003%/ °C - gains accuracy

Scope Control Options

The following scope controls each require two BA614 digital to analog converters:

AA11-A Scope Control for Tektronix 611 Storage Display Unit

Display Rate:	30 Hz (min) to 10 KHz (max)
Display Time:	deflection time 80 μs intensification time 20 μ s Non-storage mode: deflection time 80 μs intensification time 2 μs
Erase Time:	0.5 sec

AA11-B Scope Control for Tektronix RM503 Oscilloscope

Display Rate:	45 KHz (max)
Display Time:	deflection time 20 μs intensification time 2 μs
Intensification: (program selectable)	two levels

AA11-C Scope Control for VR12 Point Plot Display

Display Rate/point:	40 Hz (min) to 40 KHz (max)
Display Time:	deflection time 20 μs intensification time 2 μs
Intensification: (program selectable)	two levels

9.4 UNIVERSAL DIGITAL CONTROL SUBSYSTEM - UDC11

9.4.1 Introduction

The UDC11 is a unique, highly flexible digital information input/output option for industrial and process control applications that use the PDP-11 computers.

The UDC11 interrogates or drives up to 252 directly addressable digital sense and control functional I/O modules or up to 4032 individual digital points. I/O functions include relay output, contact sense/interrupt counters, D/A converters, etc.

Automatic hardware logic within the UDC11 rapidly identifies interrupting inputs according to input module type and address, typically within 5 μsec.

The subsystem has been designed to take full advantage of the PDP-11 processor including the UNIBUS, and permits data to be read or loaded with a single move instruction.

Modular design and industrial packaging, including provisions for two wire, screw terminal input connectors, permit the UDC11 to be configured and modified according to application needs. The UDC11 is normally supplied as part of an IDACS-11 system however it may be easily field added to existing PDP-11 systems.

9.4.2 Operation

The UDC11 operates under computer program control as a high level digital multiplexer, interrogating digital inputs and driving digital outputs located on directly addressable functional modules.

Sixteen bit data words are transferred directly between a functional module and a preassigned address location in the PDP-11 core memory by a single MOVE instruction when reading data in, or conversely from core to a module when sending data out.

Depending upon the module type selected, a 16-bit data output word can represent the single 16-bit digital word required by a D/A converter or 16 individual points for contact closures, pulse outputs, etc.

9.4.3 Signal Conditioning and Functional I/O Modules

Each UDC11 system is tailored to meet a specific application by modularly assembling the appropriate modules.

Functional Input/Output Modules include Contact Interrupt, Contact Sense, Single Shot Driver, Flip-Flop Driver, Latching Relay, Single Shot Relay, Flip-Flop Relay, D/A Converters, and I/O Converters. Each of these modules plug interchangeably into the DD02 File Units which serve as universal interface units. The logical address of each unit can be determined by simple jumper wire connections, so that addresses are completely independent of the unit's physical location. Thus hardware additions or system program changes do not require the rewiring of input terminals.

Each Functional I/O Module requires a Signal Conditioning Module to normalize input voltages, provide fusing, and distribute field-supplied excitation and control power to the Functional I/O Modules.

9.4.4 Signal Conditioning Modules

a. Isolated Power BW400 - Provides the interface between individual points on the functional I/O modules and field signals. Differential pair field wiring is terminated on screw terminals, one pair for each of the 16 points on the functional module.

b. Common Power BW402 - Is similar to the BW400 except that a 17th input pair permits field supplied excitation or control power to be brought directly to the Signal Conditioning Module and distributed in parallel (common) to each of the 16 circuits on the module. The input is fused for 4 amperes. As with the BW400, the BW402 can supply signal conditioning and arc suppression, if required.

c. Output Driver Module BW403 - Is similar to the BW402 Common Power Module except that a common ground return is provided for the open collector devices of the Single Shot Driver and Flip-Flop Driver. (used with BW85 and BW87 only)

d. Contact Sense BW731 - Provides electrically isolated, differential inputs for 16 external customer contacts or voltages. Isolation of up to 250 volts is achieved by a miniature read relay buffer on each input point. This module provides reliable and trouble free digital sensing in high noise environments. Also, its differential input characteristics are particularly suited for those applications where the ground of the customer's excitation voltage power supply may be different from (i.e., not directly strapped to) computer system ground.

e. Contact Interrupt BW733 - provides 16 electrically isolated, differential inputs for external customer contacts or voltages. It is electrically and mechanically similar to the BW731 Contact Sense Module. The BW733 is used to economically and reliably interface asynchronous devices requiring fast service from the processor because of priority or short duration.

9.4.5 Functional I/O Modules

a. Flip Flop Driver BM685 - Provides 16 solid state buffered driver circuits for control of solenoid valves, relays, lamps, displays, etc. Capable of switching control voltages of up to +55 VDC, the BM685 will switch up to 250 ma of field supplied power per point, when set by a logical "1." The driver includes diode protection for inductive loads.

b. Single Shot Relay BM807 - provides 16 electrically isolated normally open mercury wetted contact ouputs for initiating alarms, controls, and field relays. Normally closed operation can be achieved through a module jumper change performed in the field by the customer or at the factory on a special order basis. The duration of the output is trimpot adjustable from 2 msec to 2 seconds. A logical "1" energizes the relay coil for the pre-set pulse duration.

c. Single Shot Driver BM687 - Provides a solid state pulse output to activate up to 16 field circuits such as lights, buzzers, or external control relays. Capable of switching control voltages of up to +55 VDC, the BM687 will switch up to 250 ma of field supplied power per point, when set by a logical "1." The driver also provides diode protection against inductive loads.

d. Latching Relay BM803 - Provides "fail-safe" operation of 16 electrically isolated mercury wetted relay outputs. Magnetically latched, the relays remain set in the event of power failure, insuring the continuity and integrity of field circuits. Change of state can be effected only by a logical "1" or "0." Relay contacts are open when the relay is set by a logical "0,"and closed when set by a logical "1." Contacts are rated at 2 amps, 250 volts, the product not to exceed 100 va.

e. Flip Flop Relay BM805 - Provides 16 electrically isolated normally open mercury wetted relay output contacts for buffered control of relays, contactors, displays, lamps, etc. Normally closed operation is possible by a module jumper change performed in the field by the customer or at the factory on a special order basis.

f. BW734 Counter Module - Is a 16 bit asynchronous binary up counter. An output buffer register is included which is updated after each counter increment. When the buffer is read (under program control), the update is inhibited, pre-

venting any data change. The counter is parallel loading, enabling it to be preset under program control. Count down is accomplished by presetting 2's complement. May be used for Input or Output counting functions, stepping motor control, etc.

g. BA633 Digital-to-Analog Converter - Is interchangeable with any functional I/O module in the UDC11. It contains four complete channels of 10 bit digital-to-analog conversion. Single-ended output current or voltage is provided by one of the four signal conditioning modules listed below. Selection of a channel (1 of 4) and loading of data into the D/A buffer is accomplished by a single move instruction. The analog output remains constant until the channel is readdressed with new data. A separate H738A analog power supply is required for each group of up to four (16 channels) BA633. Power fail backup can be provided to maintain the analog output at its constant last value in the event of system or line power failure.

h. Digital-to-Analog Converter BA633 Signal Conditioning Modules A signal conditioning module is required for each BA633. Each module contains four channels of signal conditioning and scales the four analog outputs of the BA633 to the required current or voltage range.

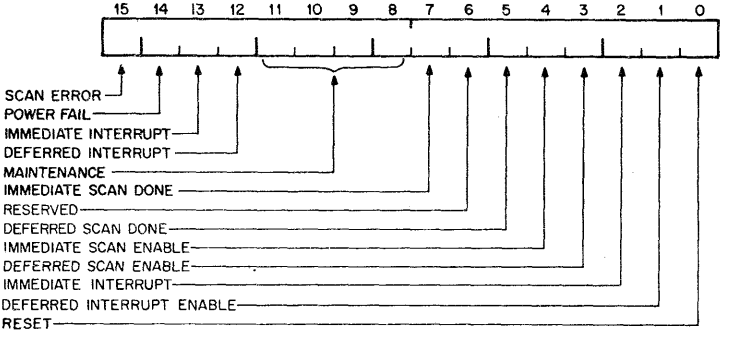
BA233	0 to +10v @ 15ma
BA234	+1v to +5v @ 15ma
BA235	4ma to 20 ma into 750 ohms
BA236	10ma to 50 ma into 300 ohms

9.4.6 Programming

The following UDC registers bit assignment and function are used to operate and exercise the subsystem in the programmed or interrupting modes. I/O functional modules can be programmed by a single MOV instruction and each module is assigned an address from the PDP-11 memory map. Addresses assigned to the UDC11 are:

REGISTER	ADDRESS
Control Status Register (UDCS)	771776
Scan Register (UDSR)	771774

Control And Status Register (UDCR)

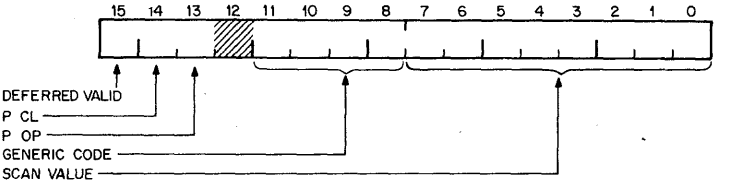


BIT	NAME	DESCRIPTION
15	Scan Error	Set by scan overflow in x, y, or wd; reset by initialize. Read only.
14	Power Fail	Set by power fail from expander H721B power supply; reset by initialize. Read only.
13	Immediate Interrupt (IM INT)	Set by interrupt class I/O module; reset when interrupt class I/O module is reset; Immediate. Read only.
12	Deferred Interrupt (DEF INT)	Same as IM INT but for deferred interrupt. Read only.
11	Maintenance Mode Word (M STP WD)	Maintenance mode of generating an interrupt module word address stop to test scanner. Read/Write.
10	Maintenance Mode Y (M STP Y)	Same as M STP WD but for Y address stop. Read/Write.
9	Maintenance Mode X (M STP X)	Same as M STP WD but for X address stop. Read/Write.
8	Maintenance Mode (M MODE)	Maintenance mode bit when set enables bit 02 to cause an IM INT or Bit 01 a DEF INT. Read/Write.
7	Immed. Scan Done	Set by an end of scan and IM INT; reset by initialize, clear done, or RIF. Read only.
6	Reserved	
5	Deferred Scan Done	Set by an end of scan and DEF INT; reset by initialize, clear done, or RIF.
4	Immed. Scan Enable (IM SCAN)	Bit enables immediate scan when set. Read/Write.
3	Deferred Scan Enable (DEF SCAN ENABLE)	Bit enables immediate scan when set. Read/Write.
2	Immediate Interrupt (IM INT)	Bit enables immediate interrupt when set; reset-set transition generates clear done signal. Read/Write.
1	Deferred Interrupt Enable (DEF INT ENABLE)	Bit enables deferred interrupt when set; reset-set transition generates clear done signal. Read/Write.

0	Reset (RIF)	Reset-set transition generates clear done and resets interrupting module; reset by initialize or delayed clear done. Read/Write.

NOTE: Initialize Resets All Bits.

Scan Register (UDSR)



BIT	NAME	DESCRIPTION
15	Deferred Valid	When set indicates a deferred scan done was displaced by an immediate scan.
14	P CL	When set indicates interest in contact closures from interrupt module.
13	P OP	Same as P CL but for contact openings.
12	Reserved	
11-8	Gen 3, 2, 1, 0	Generic code of interrupt module.
7-0	Scan Value	Address of interrupt module found as result of scan.

Two types of service requests exist fo interrupt producing functional I/O modules. These are "immediate"and "deferred."

The type of request serviced by the UDC11 is governed by program selection. If both requests are enabled the UDC11 will always service the immediate requests before servicing deferred requests.

Upon receipt of a service request by a functional module, the UDC11 controller determines the type of request and automatically intiates a scan to determine the address of the interrupt. Since the search is completely asynchronous and software overhead to test the controller with each data transfer prohibitive, programmed data transfer will take precedence over the hardware search.

Upon locating the address of the I/O module requesting service a hard-wired four bit generic code is transferred to the scan register.

When the address and generic code are located the PDP-11 is interrupted on level BR6 if immediate service is required, or BR4 if deferred service is required. In either case the address and code may be read to the preassigned vector address to determine and call the appropriate subroutine for processing of the interrupt.

9.4.7 Specifications

Modes of Operation:	Programmed Digital Output Programmed Digital Input Interrupt Controlled Input Interrupt Controlled Counting
Data Format:	16-bit I/O Data Words
Digital Inputs/Outputs:	252 16-bit words (4032 digital points) maximum
Type of Input/Output:	(see Functional I/O Modules and Signal Conditioning Modules)
I/O Module Selection:	Directly addressable
Interrupt Module:	Module type code and Module address
Interrupt Scan:	Locates address and type in 5 μsec typical (20 μ sec, worst case)
I/O Data Rate:	10^5 16-bit words/sec
Computer Interface:	UNIBUS Compatible
System Clock Rates:	3 available to each I/O word Line frequency, 6.3v AC 175 Hz - 1.75 KHz adjustable 1.75 KHz - 17.5 KHz adjustable
Operating Temperature:	40 °F to 120 °F
Cooling/Filtering:	Dust filters and blower fans in system cabinet.
Input Cabling:	Top or bottom entry, screw terminal connections. #18 A.W.G. 2 wire twisted pair/pt. max. size for fully wired cabinets. (Screw terminals will accomodate 14 A.W.G. wires).
Size:	Each H964A Cabinet 21"W x 30"D x 72"H
Weight:	750 pounds - dual cabinet (64 words or 768 points).
Power:	115/230 volts, 40 to 440 Hz, single phase, 30 amps.
Priority Level:	Immediate Level: BR6 Deferred Level: Br4
Interrupt Vector Address:	234

part 2

UNIBUS AND INTERFACING

PART II

PART II
INTRODUCTION

This section describes detailed operation of the UNIBUS and methods for interfacing to the UNIBUS for the addition of custom-designed peripheral equipment to the PDP-11 System. It is assumed that the reader is familiar with the PDP-11 System and has a thorough understanding of the principles and concepts introduced in the PDP-11 Processor Handbook.

The following documents used in conjunction with this Handbook will help the reader understand interface techniques and the overall PDP-11 System:

a. PDP-11 Processor Handbook

b. Processor Manual

c. Digital Logic Handbook

All communication between PDP-11 system components is accomplished by a single high-speed bus called the UNIBUS. Four concepts are extremely important for an understanding of the hardware and software implications of the UNIBUS. Each concept is covered separately in subsequent paragraphs.

Single Bus
The UNIBUS is a single, common path that connects the processor, memory, and all peripherals. Addresses, data, and control information are transmitted along the 56 lines of the bus. Figure 1 is a simplified block diagram of the PDP-11 System and UNIBUS.

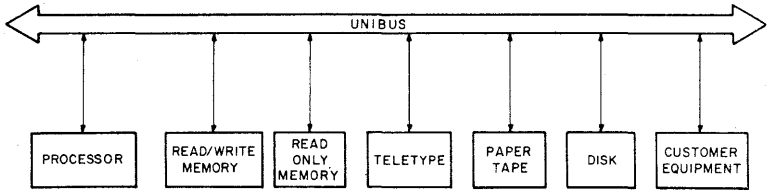


Figure 1 PDP-11 System Simplified Block Diagram

The form of communication is the same for every device on the UNIBUS. The processor uses the same set of signals to communicate with memory and peripheral devices. Peripheral devices also use this set of signals when communicating with the processor, memory, or other peripheral divices.

All instructions applied to data in memory can be applied equally well to data in peripheral device registers. Therefore, peripheral device registers may be manipulated as flexibly as memory by the processor. This is an especially powerful feature, considering the special capability of PDP-11 instructions to process data in any memory location as though it were an accumulator.

Bidirectional Lines
Most UNIBUS lines are bidirectional: therefore, the input lines can also be driven as output lines. This means that a peripheral device register can be either read or can be used for transfer operations. Thus, the same register can be used for both input and output functions.

Master-Slave Relation
Communication between two devices on the bus is in a master-slave relationship. During any bus operation, one device has control of the bus. This device, the bus master, controls the bus when communicating with another device on the bus, called the slave. A typical example of this relationship is the processor, as master, transferring data to memory, as slave. Master-slave relationships are dynamic. The processor, for example, passes bus control to a disk. The disk, as master, then communicates with a slave memory bank.

The UNIBUS is used by the processor and all I/O devices; thus, a priority structure determines which device obtains control of the bus. Consequently, every device on the UNIBUS capable of becoming bus master has an assigned priority. When two devices which are capable of becoming bus master, have identical priority values and simultaneorusly request use of the bus, the device that is electrically closest to the bus receives control.

Interlocked Communication
Communication on the UNIBUS is interlocked between devices. Each control signal issued by the master device must be acknowledged by a response from the slave to complete the transfer. Therefore, communication is independent of the physical bus length and the response time of the master and slave devices. The maximum transfer rate on the UNIBUS with optimum device design, is one 16-bit word every 400 ns, or 2.5 million 16-bit words per second.

PERIPHERAL DEVICE ORGANIZATION AND CONTROL
Registers in peripheral devices are assigned addresses similar to memory; thus, all PDP-11 instructions that address memory locations can become I/O instructions. Data registers in devices can take advantage of all the arithmetic power of the processor. The PDP-11 controls devices differently than most computer systems. Control functions are assigned to a register address, and then the individual bits within that register can cause control operations to occur. For example, the command to make the paper-tape reader read a frame of tape is provided by setting a bit (the reader enable bit) in the control register of the device. Instructions such as MOV and BIS may be used for this purpose. Status conditions are also handled by the assignment of bits within this register, and the status is checked with TST, BIT, and CMP instructions. In addition, there is no limit to the number of registers that a device may have, providing an unlimited flexibility in the design and control of peripheral equipment.

TRANSFER OF BUS MASTER
A device (other than the processor) that is capable of becoming bus master generally requests use of the bus for one of two purposes:

a. to make a non processor transfer of data directly to or from memory, or

b. to interrupt program execution and force the processor to branch to a specific address where an interrupt service routine is located.

Subsequent paragraphs discuss priority structure and the two main uses of the bus: non-processor transfers and interrupts.

Transfer Request Handling
The request and granting of bus mastership is performed in parallel with data transfers on a completely independent set of bus lines. Thus, while one device is using the bus, the next request is being checked for priority and the next user is being assigned. Because of this time parallelism, successive data transfers by different master devices can occur at the full UNIBUS speed.

Priority Structure
When a device capable of becoming bus master requests use of the bus, the handling of that request depends on the location of that device in the priority structure. The following factors must be considered to determine the priority of the request:

a. The processors priority is set under program control to one of eight levels using bits 7,6, and 5 in the processors status register. These three bits set a priority level that inhibits granting of bus requests on the same or lower levels.

b. Bus requests from external devices can be made on any one of five request lines. A non-processor request (NPR) has the highest priority, and its request is granted by the processor between bus cycles of an instruction execution. Bus request 7 (BR7) is the next highest priority and bus request 4 (BR4) is the lowest. The four lower level priority requests (BR7 to BR4) are granted by the processor between instructions. When the processor priority is set to a specific level, all bus requests on that level and below are ignored. For example, if the processor priority is 6, requests on BR6 or any other lower level are not granted.

c. When more than one device is connected to the same bus request line, the device electrically nearer the processor has a higher priority than the device further away. Any number of devices can be connected to a specific BR or NPR line.

When a device other than the processor gains control of the bus, it uses the bus to perform either a data transfer or an interrupt request as described in the following paragraphs.

Data Transfer
Direct memory or device access data transfers can be accomplished between any two peripherals without processor supervision. These are called NPR level data transfers. Normally, NPR transfers are made between the memory and a mass storage device, such as a disk.

During NPR transfers, it is not necessary for the processor to transfer the information between the memory and the mass storage device. The bus structure enables device-to-device transfers, thereby allowing customer-designed peripheral controllers to directly access other devices (such as disks) on the bus. This direct access capability permits operations such as a disk directly refreshing a CRT display.

An NPR device provides extremely fast access to the bus and can transfer data at high rates once it gains control. The processor state is not affected by this type of transfer; therefore, the processor can relinquish bus control while an instruction is in progress. This release of the bus can normally occur at the end of any bus. However, the bus can never be released between cycles of a read-modify-write sequence. (This is described more fully in Chapter 1). An NPR device in control of the bus transfers 16-bit words or 8-bit bytes to memory at the same speed as the memory cycle time.

Interrupt Requests

Devices that gain bus control with one of the bus request lines (BR7, BR6, BR5, BR4) can take full advantage of the power and flexibility of the processor by requesting an interrupt. The entire instruction set is then available for manipulating data and status registers. When a device servicing program is to be run, the task being performed by the processor is interrupted, and the device service routine is initiated. After the device request has been satisfied, the processor returns to its former task. Note that interrupt requests can be made only if bus control has been gained through a BR priority level. An NPR level request can not be used for an interrupt request.

Interrupt Procedure

This paragraph provides an example of an interrupt operation. Assume that a peripheral requires service and requests use of the bus at one of the four BR levels. The operations required to service the device are as follows:

a. Priorities permitting, the processor relinquishes bus control to the device.

b. When the device gains control of the bus, it sends the processor an interrupt command and a unique address of a memory location which contains the starting address of the device service routine. (This is called the interrupt vector address.) Immediately following this pointer address is a word (located at vector address + 2) to be used as the new processor status (PS) word.

c. The processor pushes the current processor status word and then the program counter (PC) value on the processor stack. The stack is pointed to by register R6.

d. The new PC and PS (the interrupt vector) are taken from the address specified by the device, and the device service routine is initiated.

NOTE

These operations are performed automatically and no device polling is required to determine which service routine to execute.

e. The device service routine can cause the processor to resume the interrupted process by executing the return from interrupt (RTI) instruction which pops the two top words from the processor stack and transfers them back to the PC and PS registers.

f. A device service routine can, in turn, be interrupted by a higher priority bus request any time after the first instruction of the routine has been executed.

g. If such an interrupt occurs, the PC and PS of the current device service routine are automatically pushed onto the stack, and the new device routine is initiated as before. This nesting of priority interrupts can continue to any level; the only limitation is the amount of memory available for the processor stack.

UNIBUS Theory and Operation

This section provides detailed theory of UNIBUS operation and includes descriptions of bus signal lines, bus transactions, bus timing, and bus interfacing characteristics. In addition, this section contains discussions of address allocations and device registers.

1.1 UNIBUS SIGNAL LINES

The PDP-11 UNIBUS consists of 56 signal lines. All devices, including the processor, are connected to these lines in parallel (see Figure 1-1). The bidirectional nature of 51 signal lines permits signals to flow in either direction. The remaining five unidirectional lines are used for priority bus control.

UNIBUS pin assignments are listed in Appendix B.

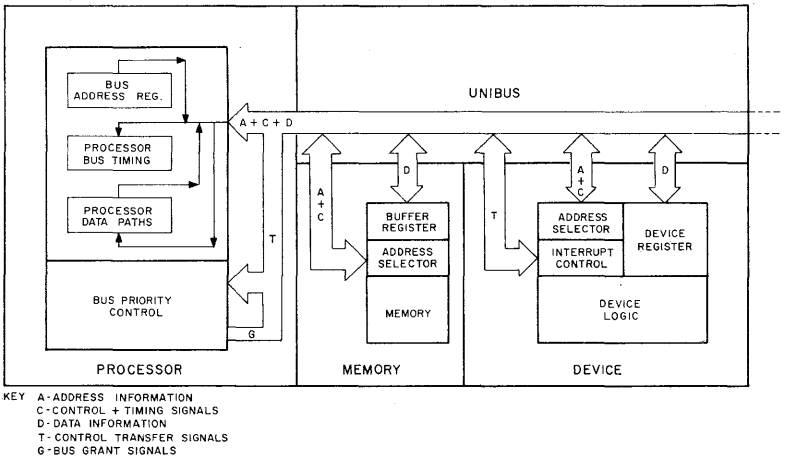


Figure 1-1 PDP-11 Interface Block Diagram

1.1.1 Data Transfer Lines

Forty bidirectional bus lines are used for data transfer. In a data transfer, one device is a bus master and controls the transfer of data to or from a slave device. The processor is always bus master when no other device is using the bus, and it is master for all data transfers involved in normal instruction processing.

Data transfer signals are listed in Table 1-2

NOTE

Signals on the Unibus are asserted when low (except for the unidirectional bus grant lines). All timing diagrams in this manual reflect the asserted and cleared levels of Unibus lines as described in Paragraph 3.2.2.

Table 1-2 Data Transfer Signals

Name	Mnemonic	No. of Lines
DATA	D<15:00>	16
ADDRESS	A<17:00>	18
CONTROL	C<1:0>	2
MASTER SYNC	MSYN	1
SLAVE SYNC	SSYN	1
PARITY BIT LOW	PA	1
PARTY BIT HIGH	PB	1
	TOTAL:	40

Simplified and standardized control logic is made possible by using separate dedicated lines for all signals. In any data transfer, data is transmitted and received; the master device provides the address of the slave device; and control and timing signals are provided. Each of these three functions occurs on a distinct set of bus lines, eliminating the use of additional hardware and extra timing states to distinguish between address, control information, and data.

1.1.1 Data Lines (D<15:00>) - The 16 data lines are used to transfer information between master and slave. The bit format is shown in Figure 1-2.

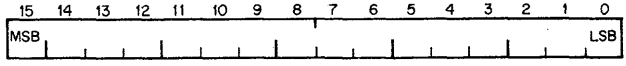


Figure 1-2 Data Line Bit Format

1.1.2 Address Lines (A<17:00>) - The 18 address lines are used by the master device to select the slave (a unique memory or device register address) with which it will communicate. The reason for 18 address lines is to extend the total memory capability of future members of the PDP-11 family to 262,144 bytes. The bit format of the 18 signals is shown in Figure 1-3.

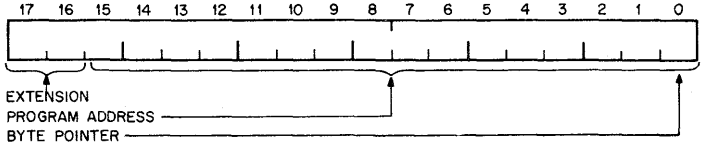


Figure 1-3 Address Line Bit Format

Lines A<17:01> specify a unique 16-bit word. In byte operations, A00 specifies the byte being referenced. If a word is referenced at X (X must be even, since words can be addressed on even boundaries only), the low-order byte can be referenced at X and the high-order byte at X + 1.

Only 16 bits are normally supplied by programs as memory reference addresses. In the processor lines A17 and A16 are asserted (forced to 1) whenever the processor attempts to reference an address between 160000 and 177777; i.e., where A15 = A14 = A13 = 1. Thus, the processor converts this 16-bit address to a full 18-bit bus address.

Peripheral devices are normally assigned an address from within the bus address allocations from 760000-777777 (program addresses, 160000-177777).

1.1.1.3 Control Signals- The control signals are divided into three groups: signals that select data transfer operations, signals that allow the master and slave device to communicate, and signals used for parity checking.

a. Control Lines (C<1:0>)- These two bus signals are coded by the master device to control the slave in one of four possible data transfer operations shown in Table 1-3.

b. Master and Slave Synchronization - Master synchronization (MSYN) is a control signal used by the master to indicate to the slave that address and control information is present. Slave synchronization (SSYN) is the slave's response to the master (usually a response to MSYN).

c. Parity Bit Low (PA) and Parity Bit High (PB) - These signals are for devices on the UNIBUS that use parity checks. PB is the parity of the high-order byte (that transferred on D<15:08>, and PA is the parity of the low-order byte (D<07:00>). These lines are used by the MP11 Parity Option in conjunction with parity memories such as the MM11-FP. Future uses of PA and PB for total system (UNIBUS) parity is also reserved for high security applications.

Table 1-3 Data Transfer Operations

C1	C0	Operation
0	0	DATI-Data In
0	1	DATIP-Data In, Pause
1	0	DATO-Data Out
1	1	DATOB-Data Out, Byte

1.1.2 Priority Transfer Lines

The UNIBUS contains 13 lines classified as priority transfer lines. Five of these are priority bus request lines (BR<7:4>,NPR) and five are the corresponding grant lines (BG<7:4>,NPG) which the processor uses to respond to a specific bus request. Each device of the same priority level passes a grant signal to the next device on the line, unless it has requested bus control; in this case, the requesting device blocks the signal from the following devices and assumes bus control. A discussion of physical chaining of devices to create priority levels is presented in Paragraph 1.3.3. In addition, there are three other control lines: SACK, BBSY, and INTR. All 13 lines are described below.

a. Bus Request Lines (BR<7:4>) - These four bus signals are used by peripheral devices to request control of the bus.

b. Bus Grant Lines (BG<7:4>) - These signals are the processor's response to a bus request. They are asserted only at the end of instruction execution, and in accordance with the priority determination.

c. Non-Processor Request (NPR) - This signal is a bus request from a peripheral device to the processor.

d. Non-Processor Grant (NPG) - This signal is the processor's response to an NPR. It occurs at the end of a bus cycle.

e. Selection Acknowledge (SACK) - SACK is asserted by a bus-requesting device that has received a bus grant. Bus control passes to this device when the current bus master completes its operation. (If SACK is not received by the processor within 10μs of issuing a bus grant, time out occurs and the bus grant is cleared automatically by the processor.)

f. Interrupt (INTR) - This signal is asserted by the bus master to start a program interrupt in the processor.

g. Bus Busy (BBSY) - This signal is asserted by the master devices to indicate bus is being used.

1.1.3 Miscellaneous Control Lines

There are three additional lines on the UNIBUS which may be used by all devices. These lines are: initialize, ac line low, and dc low:

a. Initialization (INIT) - This signal is asserted by the processor when the START key on the console is depressed, when a RESET instruction is executed, or when the power fail sequence occurs. In the latter case, INIT is asserted following the power fail service routine while power is going down, and again when power comes up. INIT may also be used to clear and initialize peripheral devices by means of the RESET instruction.

b. AC Line Low (AC LO) - This is an anticipatory signal which starts the power fail trap sequence, and may also be used in peripheral devices to terminate operations in preparation for power loss. When AC LO is cleared, the power up instruction sequence in the processor begins. It is the programmer's responsibility to make certain that the trap vector is loaded with a pointer to the power fail routine. If this is not done, an undefined sequence results.

c. DC Line Low (DC LO) - This signal, which emanates from the power supply, is wired from the power connector card slot to the UNIBUS on all system units. This signal remains cleared as long as all dc voltages are within specified limits. If an out-of-voltage condition occurs, DC LO is asserted by the power supply. Devices such as core memories use the DC LO signal to inhibit further operations. The DC LO signal is normally cleared before AC LO when power is coming up and is asserted after AC LO when power is going down. Note that the power fail trap is initiated by AC LO only and that the DC LO signal is used by the processor to cause INIT on the bus.

1.2 DATA TRANSFER BUS TRANSACTIONS

All bus activity is asynchronous and depends on interlocking of control signals. In every case, a signal from a slave device is generated in response to a signal from a master device, and the master signal is dropped in response to the slave signal. The complete elimination of critical self-timing gives the bus the flexibility to operate with devices running at different speeds.

NOTE

Signals on the UNIBUS are asserted when low (except for the unidirectional bus grant lines). All timing diagrams in this manual reflect the asserted and cleared levels of UNIBUS lines as described in Paragraph 2.1.2.

The four bus-data transfers are described in Table 1-4. The bus master determines one of the four data transfers by asserting the proper code on the C<1:0> lines.

NOTE

All data transfers are with reference to the master device; data-in is always from slave to master, and data-out is from master to slave. For example, when the processor (master) loads data into memory (slave), a data-out bus operation is performed.

Table 1-4 Bus-Data Transfer Transactions

Name	Mnemonic	C Lines C1	C Lines C0	Function	Octal Code
Data in	DATI	0	0	Data from slave to master	0
Data in, pause	DATIP	0	1	Inhibits restore cycle in destructive read-out devices; *Pause flip-flop* is set which inhibits clear cycle on following DATO (B). Must be followed by DATO or DATOB.	1
Data out	DATO	1	0	Data from master to slave.	2
Data out, Byte	DATOB	1	1	Transfers data from master to a single byte in slave. Data transferred on D<15:08> for A00 = 1 D<07:00> for A00 = 0.	3

The DATI and DATIP transactions request transfer of data from a slave, the address of which is specified by A<17:00>, to the master. Both transfers use the data lines to carry the data. There is no distinction made by the slave as to whether the transfer is used for byte or word data. The slave places the data on D<15:00>. It is the function of the master device to retrieve the data from the proper lines: low-order byte register with A00 = 0 from D<07:00>; high-order byte register with A00 = 1 from D<15:08>; or word register from D<15:00>. The DATIP operation is identical to the DATI, except DATIP is used to inform the slave device that this is the first part of an in-modify-out cycle. A DATIP normally sets a pause flag in the destructive read-out device (i.e., core memory) which inhibits the restore cycle. The DATIP must be followed by a data-out cycle (DATO or DATOB), and the master must retain bus control until it is completed. In nondestructive readout devices (i. e., flip-flops), the DATI and DATIP are treated identically.

The DATO and DATOB operations transfer data from the master to the slave. A DATO is used to transfer a word to the address specified by A<17:01>. The slave ignores A00 and the master places data on D<15:00>. A DATOB is used to

transfer a byte of data to the address specified by A<17:00>. Line A00 = 0 indicates the low-order byte, and the master places the data on lines D<07:00>; A00 = 1 indicates the high order byte, and master places the data on lines D<15:08>.

1.2.1 Data Transfer Timing

The design of the UNIBUS imposes certain timing restrictions although transfers are interlocked. Responsibility for these timing restrictions has been assigned to the master to simplify the slave design.

In all transfers, it is assumed that there can be a maximum 75-ns skew due to driver, receiver, and transmission line tolerances. In other words, the coincident assertion of two lines at the transmitter inputs of one device could result in a maximum difference of 75-ns in the occurrence of those signals at the receiver outputs in another device.

Because of this possible skew, the master always delays its MSYN signal to ensure that MSYN does not reach the slave device prior to valid data or addresses. In addition, the MSYN signal is further delayed to allow 75 ns for decoding by the slave device. The master also must not drop the A (address) or C (control) lines until 75 ns after MSYN has been dropped to guarantee that there are no spurious selections. Note, however, that when a slave transmits data to a master (DATI or DATIP), the deskew and decode time delay must be made by the master (refer to Paragraph 1.2.2f). Additional timing information can be found in Paragraph 1.4.

1.2.2 DATI and DATIP Bus Transactions (see Figure 1-4)

All data transfer functions are with reference to the master device; therefore, data-in (DATI) indicates data transfer from the slave to the master.

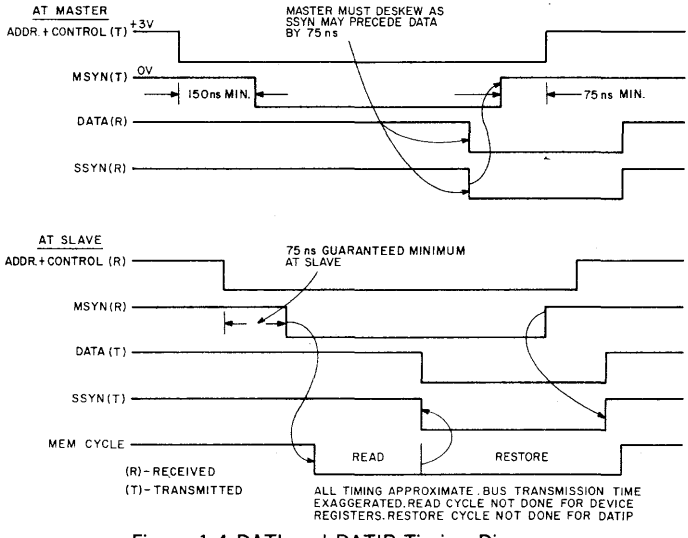


Figure 1-4 DATI and DATIP Timing Diagram

a. Master sets C<1:0> = 00 for DATI or C<1:0> = 01 for DATIP, and sets A<17:00> to specify the slave address.

b. Master waits 150 ns minimum: 75 ns to allow for worst case signal skew on the UNIBUS plus 75 ns for slave to decode address.

NOTE

This guarantees that at the output of the slave's bus receivers that A<17:00> and C<1:0> will precede MSYN by 75 ns min.

c. Master waits for bus to become inactive since SSYN may still be asserted from a previous cycle.

NOTE

This condition is automatically satisfied when first becoming bus master since SSYN must be negated before BBSY can be asserted (see M7820 circuit).

d. Master asserts MSYN

e. When the selected slave sees its address and MSYN, the slave device prepares the data for transmission to the master. For devices such as memory, this means performing a read cycle; for flip-flop registers, the data is available immediately.

f. When data is available, the slave places data on D<15:00> and asserts SSYN. If the slave is a destructive read-out device, it enters a restore cycle if the command was a DATI; for a DATIP, the slave can set a pause flag and wait for the subsequent DATO or DATOB with the modified data before perfoming a write cycle. The SSYN response must be made within 25μsec.

g. The master receives SSYN and waits 75 ns minimum to allow for skewing of data plus any additional time the master may need for internal gating.

h. Master strobes in data from D<15:00>.

i. When the data has been accepted by the master device, it drops MSYN.

j. After 75 ns minimum wait, the master removes or alters the A and C lines. If another DATI follows, then the master repeats the above sequence starting at step a. If an output operation follows, the next cycle starts at step a. of the DATO or DATOB operation. If this is the last bus cycle of the master's operation and when the A and C lines are all clear, then the master clears BBSY and relinquishes bus control.

k. The slave sees the negation of MSYN and removes data from the D lines and negates SSYN.

1.2.3 DATO and DATOB Bus Transactions (See Figure 1-5)

Because all data transfers are with reference to the master device, a data out (DATO) indicates data transfer from the master to the slave.

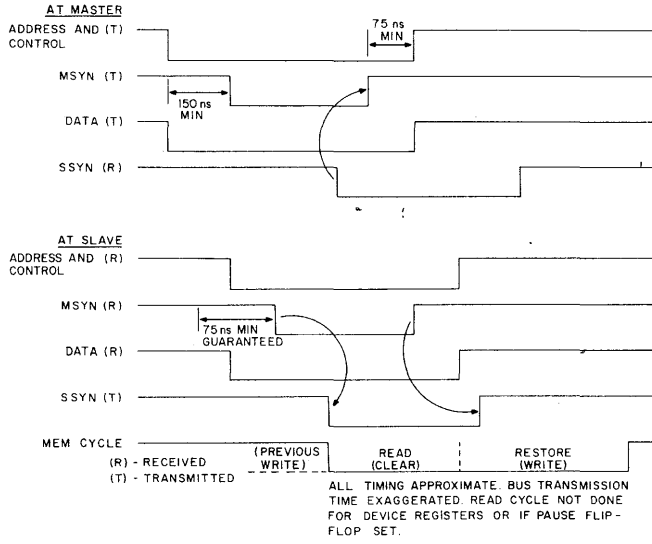


Figure 1-5 DATO or DATOB Timing Diagram

a. If previous cycle was DATI or DATIP, master must wait for SSYN to be negated.

NOTE

This condition is automatically satisfied when first becoming bus master since SSYN must be negated before BBSY can be asserted (see M7820 circuit).

b. Master sets C<1:0> = 10 for DATO or C<1:0> = 11 for DATOB, sets A<17:00> to specify the slave address, and D<15:00> for data to be sent to slave.

c. Master waits 150 ns minimum: 75 ns to allow for worst case signal skew on the UNIBUS plus 75 ns for slave to decode address.

NOTE

This guarantees that at the output of the slave's bus receivers, that A<17:00>, D<15:00>, and C<1:0> will precede MSYN by 75 ns minimum.

d. Master waits for bus to become inactive since SSYN may still be asserted from previous cycle.

NOTE

This condition may have been already satisfied by step a; it applies to consecutive DATO's or DATOB's.

e. Master asserts MSYN.

f. When the selected slave sees its address and MSYN, and it is ready to accept the data present on the D lines (slave may be busy completing a previous internal operation), it strobes in the data and asserts SSYN.

NOTE

Data on the D lines is guaranteed valid for 75ns minimum after SSYN is asserted. Data is not guaranteed valid when the slave receives negated MSYN. The processor times out and removes MSYN if no SSYN response is made within 25μsec.

g. The master receives SSYN and negates MSYN.

h. After 75 ns minimum wait, the master removes or alters the A, C, and D lines. If another DATO or DATOB follows, then the master repeats the above sequence starting at step b. If this is last bus cycle of the master operation and when A, C, and D lines are all clear, then the master clears BBSY and relinquishes bus control. If an input operation follows, the next cycle starts at step a of the DATI or DATIP operation.

i. The slave sees the negation of MSYN and negates SSYN.

1.3 PRIORITY TRANSFER TRANSACTIONS

Transfer of bus control from one device to another is determined by priority arbitration logic, which is part of the processor. Requests for the bus can be made at any time (asynchronously) on the bus request (BR) and non-processor request (NPR) lines. During each bus cycle, the arbitration logic first checks for an NPR request (since these requests take precedence over processor use of the bus). If an NPR is present, the logic issues an NPG signal and receives a selection acknowledge (SACK) signal in return. This procedure occurs simultaneously with the current data transfer. When the device scheduled to become the new bus master is selected, it waits for the present master to clear bus busy (BBSY); then, the newly selected device becomes bus master and asserts BBSY.

A similar procedure occurs at the end of each instruction when the priority arbitration logic checks the bus request lines against the processor priority (as determined by bits <7: 5> of the processor status register) and the priority logic issues a grant on the corresponding line. Thus, one of the four levels of BR requests is granted by the processor between instructions unless the instruction currently being executed causes an internal trap (either an error or trap instruction). In this case, BR requests are not granted until completion of the first instruction following the trap sequence. The highest request is always granted first (if the processor priority level is lower than the request level). The grant signals always pass serially through each device connected to the corresponding level in the system. If a device makes a request, it blocks the signal transmission to the next device on the line; otherwise, it passes the signal on.

This causes the device closest to the processor to be the highest subpriority on each request level.

1.3.1 Priority Transfer (PTR) Transaction (See Figure 1-6)

The signal sequence by which a device becomes selected as next bus master is the priority transfer (PTR) bus operation. This operation does not actually transfer bus control; it only selects a device as next bus master. The sequence of events is as follows:

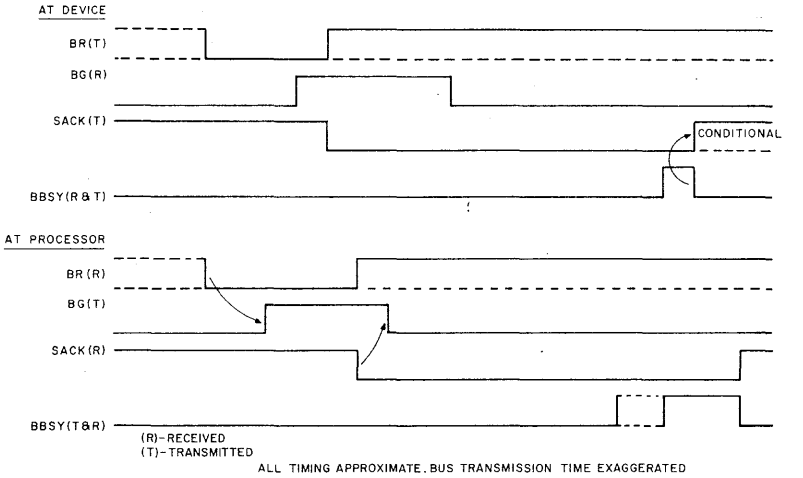


Figure 1-6 PTR Timing Diagram (nominally, for processor master)

a. The device that needs control of the bus asserts the BR (or NPR) line assigned to it.

b. The processor receives one or more BR signals. These signals enter a priority arbitration system, which compares BR levels with the processor priority levels and against the NPR. If a request has the highest priority entering the arbitration system, and the SACK line is clear, the processor asserts the corresponding BG (or NPG) line. NPG is asserted during the current bus transaction, while BG is asserted only at the end of the current instruction.

c. Each device on the asserted BG line passes the BG signal, unless it is requesting bus control.

d. The first device on the line which has BR asserted responds to the BG by asserting SACK, blocking the BG signal from following devices, and clearing BR.

e. The processor receives the SACK signal and clears BG, (If SACK, is not received within 10μs, time out occurs and the bus grant is cleared automatically by the processor.)

f. The current bus master completes a data transfer and clears BBSY at the same time it clears the Address and Control lines.

g. The selected device, which is the new bus master, asserts BBSY when BBSY, BG, and SSYN are clear at the end of the previous data transfer. INTR may be asserted at this time, if the new bus master is interrupting. (Refer to Paragraph 1.3.2)

h. SACK is dropped at the same time INTR is asserted if the device is interrupting. If the device is to transfer data first, the SACK signal is dropped prior to the start of the last bus cycle that the device uses.

i. When the new bus master has completed its last data transfer, it clears BBSY. A new bus master then takes control of the bus. If no device is selected (SACK is clear), the processor asserts BBSY and continues processing. If, instead of clearing BBSY in a passive release, the device asserts INTR, the processor conducts an INTR bus transaction. This is called active release of the bus.

CAUTION

Since an NPR is granted within an instruction, and the interrupt and following processor response would destroy information held in the processor, devices granted bus control through an NPR must not cause a processor interrupt (refer to Paragraph 1.4.2).

NOTE

During the time a master device has control of the bus, it must either issue MSYN or terminate with an interrupt to provide reclocking of the priority arbitration logic in the processor. This affects only certain models of the KA11 and KC11 processors.

1.3.2 Interrupt Transaction (See Figure 1-7)

A device may cause the interrupt operation to occur any time it gains bus control with one of the BR levels. It is usually accomplished immediately on becoming bus master; however, it may follow one or more data transactions on the bus.

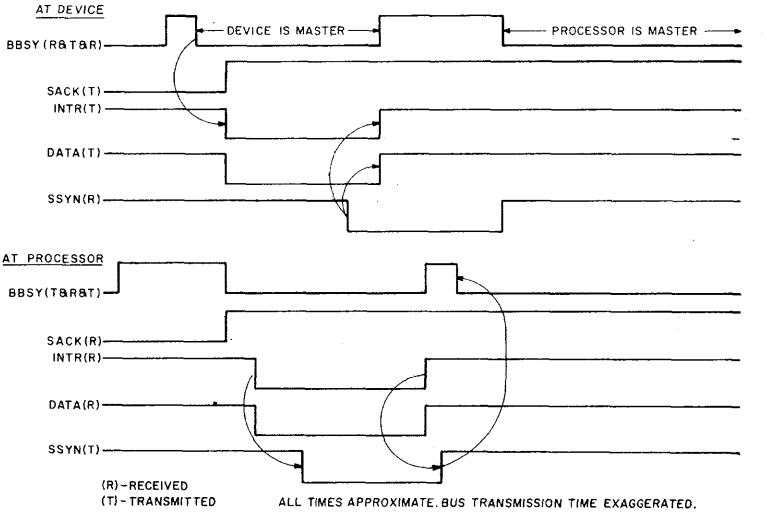


Figure 1-7 INTR Timing Diagram

a. If immediate interrupt operation is to be initiated, a device which has been selected as bus master asserts INTR and a vector address on the D lines, at the same time that it clears SACK and asserts BBSY. If data transfers occur prior to interrupt then SACK must remain asserted until INTR is asserted. If the device has been making data transfers prior to the interrupt, it should assert SACK through the last cycle.

b. The processor receives the INTR signal, waits 75 ns for deskew to ensure that all bits of the interrupt vector address are available, and asserts SSYN when the data is read in.

c. The bus master (interrupting device) receives SSYN and clears INTR, the D lines, and BBSY. This constitutes active release of the bus to the processor.

d. The processor clears SSYN when INTR is cleared, and enters the interrupt sequence to store the contents of the current PC and PS registers and replace them with the contents of the location specified by the vector address.

1.3.3 Priority Chaining

The PDP-11 uses electrical chaining of devices to assign minor priority levels. These levels separate devices of the same major priority level to provide a full array of priority servicing. Figure 1-8 illustrates the mode of operation and advantages of this system. Six devices are shown in order of their electrical distance from the processor. Three devices are at major priority level 4: device A, device C, and device D. The remaining three are at major priority level 5.

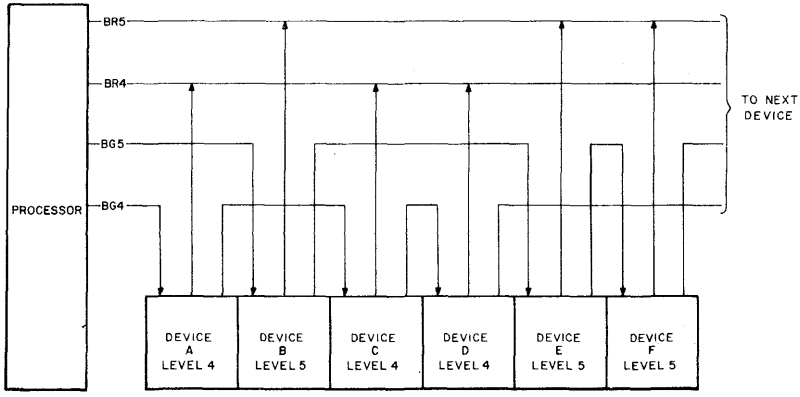


Figure 1-8 Priority Chaining Example

If the processor is at priority level 5 or above, no bus requests are granted from any of these devices. At a processor priority of 4, only requests from devices B, E, or F are granted. Assume that the processor priority is 2 and also that during one instruction cycle, devices C, E, and F assert bus requests. At the end of the instruction, the processor conducts a PTR operation. Since BR 5 is asserted, the processor does not respond to BR 4 (device C). When BG 5 is asserted, the signal first goes to device B. After a delay to clock the interrupt control shift register

(discussed in Paragraph 2.3.5), the signal is passed on, since device B was not asserting BR and does not block the pulse. Next, the signal goes to device E, which blocks the pulse, drops BR 5, and takes control of the bus. Device F still has BR 5 asserted, however, and device C has BR 4 asserted. These requests remain on the bus until granted or actively cleared by the processor. If device E does an INTR operation, device F gains control of the bus after the first instruction of the handling routine has been executed, unless the INTR operation raises the processor priority.

Changing the processor priority is accomplished easily since the trap sequence following the INTR operation provides a new PS word, which includes a new processor priority. If the priority is set to 5, the processor ignores the current bus request but grants requests from other devices with higher major priority levels (if there are any).

At the conclusion of the interrupt handling routine, the original processor priority is restored and normal processing is resumed. After one instruction, device F gains control of the bus. When normal processing resumes again, device C, which is still waiting for bus service, gains control in a similar manner.

Higher priorities are assigned to devices that require faster service to avoid destruction or loss of data. Slower devices, which can afford to wait, operate with low priorities. Therefore, service can be provided to all devices in an equitable manner, with no lost data and maximum speed and bus efficiency.

1.4 UNIBUS TIMING

Although all bits of an information signal are transmitted simultaneously, differences in bus path lengths and speeds of individual gate responses may cause variations in transmission time and in the elapsed time before reception. To allow for slow signals to arrive, and to permit settling of levels which have encountered transmission noise, the strobing or gating of this data is delayed a nominal 75 ns. This delay is greater than the worst case signal skew encountered in practice.

A further delay may be necessary to allow an information signal within a device to qualify gates that accept a strobing signal. A 75-ns delay allows for this gating and must be provided by any device which acts as bus master for a data transfer. Thus, a slave is always guaranteed that address and data are valid at its interface (the device side of the receivers) 75 ns in advance of the MSYN signal at the output of the MSYN receiver. If a slave requires more decoding time, it must provide its own delay for the MSYN signal, or trigger a delayed strobe from the MSYN signal.

To simplify slave device design in a DATI or DATIP sequence, the slave may place the data on the D lines coincident with the assertion of SSYN. The deskewing (75 ns) and decoding delay is the master's responsibility. In the INTR sequence, the interrupting device may place the vector address on the D lines coincident with the INTR signal. The processor allows for the 75-ns skew.

1.4.1 Timing Example

To illustrate the operating speed of the UNIBUS when performing a data transfer, assume a DATO operation to a device that has a flip-flop register. A typical transmitter-bus-receiver delay time is 75 ns. A flow diagram of the transfer procedure is shown in Figure 1-9 and is described below. A simplified logic diagram of the slave device is shown in Figure 1-10.

The bus master places address, control, and data information on the UNIBUS, waits 150 ns, and then asserts MSYN. After a worst case propagation delay of 75 ns, the slave recognizes MSYN and clocks the data into its register. Since the 75-ns propagation delay includes the transmitter and receiver delays, the time required to turn MSYN around into SSYN is literally 0. Also, since the data preceded MSYN by 150 ns (worst case skew is only 75 ns), there is ample preset time for the data input to the slave device flip-flop register.

When the master sees SSYN, it clears its MSYN control (nominal time, 25 ns) and then waits 75 ns before clearing or changing address, control, and data information. Additional cycles may proceed at this time provided SSYN is cleared before MSYN is again asserted. This means that a sustained DATO transfer rate of 400 ns/word may be maintained. This is equivalent to a transfer rate of 40 million bits per second.

Figure 1-11 is a typical timing flow diagram for a DATI transfer. The slave device logic is shown in Figure 1-12. The procedure for a DATI transfer is essentially the same as for a DATO transfer with four exceptions:

a. The master asserts only address and control information.

b. The slave gates data onto the bus simultaneously with the return of SSYN.

c. The master must wait 75 ns (to allow for skew between SSYN and DATA) before clearing MSYN and strobing data.

d. The slave clears data when it clears SSYN.

The DATI cycle allows sustained transfer rates of 450 ns-word which is equivalent to 35.2 million bits second.

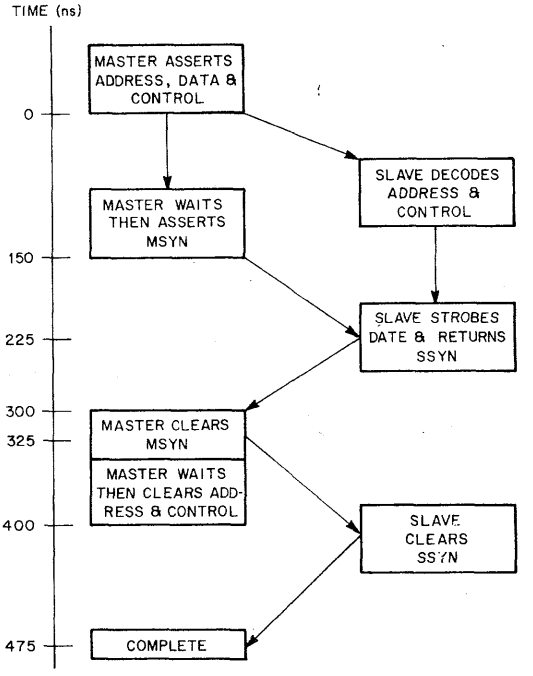
1.4.2 Time-Out Protection

A precaution must be taken when designing peripheral devices that gain control of the bus for the purpose of transferring data to another element on the UNIBUS. Normally, such a device contains a bus address register, which is loaded by the program as one of the initialization steps. This address must then be incremented by the device upon completion of each data transfer. If the program loads an erroneous address or if the register increments beyond the available core memory in the existing system, no SSYN response is generated for the data transfer. To prevent this problem from hanging up the system, it is recommended that a 10- to 25-μs integrating one-shot be triggered each time the master device asserts MSYN. If this one-shot times out before SSYN is received, the master should stop the transfer by clearing MSYN, BBSY, and any other signals it has asserted. The master should then set an error flag in its status register.

1.5 ADDRESS MAPPING

A PDP-Address Map is shown in Appendix A. Observe that, in the following discussion, all addresses are numbered in octal. The letter K, which is normally used to devote 1000 (decimal), is used in this discussion to denote 1024 (decimal).

The UNIBUS addresses 2^{18} locations ($262{,}144_{10}$ or 256K), and each location contains eight bits. On the basic PDP-11 systems only 16 bits of address information are under program control. This limits the processor to an address map of 64K locations. Since the word length and bus width are two bytes, most bus operations access two locations at once; the address supplied on the bus is that of the even-numbered location, and the next higher odd location is selected as well. Byte op-



NOTES:

Worst case propagation delay of 75ns is shown.
Total time = 475ns for a single transfer.
Next cycle may begin at 400ns when master may assert new address and control.
Maximum sustained transfer rate is 2.5 million words/sec.

Figure 1-9 Typical DATO Timing Flow

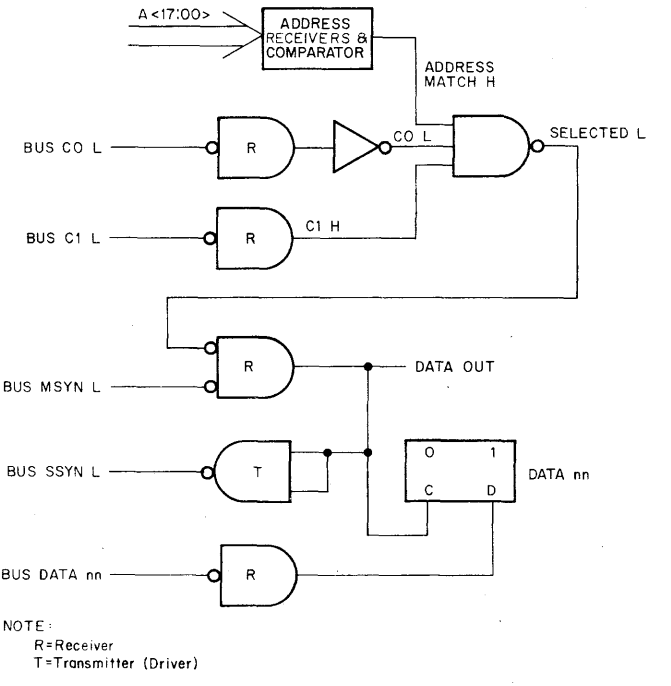
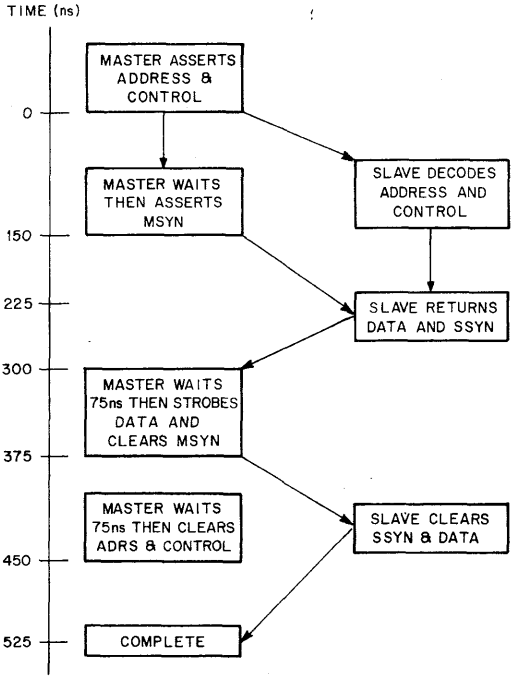


Figure 1-10 Slave Logic For DATO (Fast Response)



NOTES:

Worst case propagation delay of 75ns shown.

Total time = 525ns for a single transfer.

Next cycle may begin at 450ns when master may assert new address and control.

Maximum sustained transfer rate is 2.2 million words/second.

Figure 1-11 Typical DATI Timing Flow

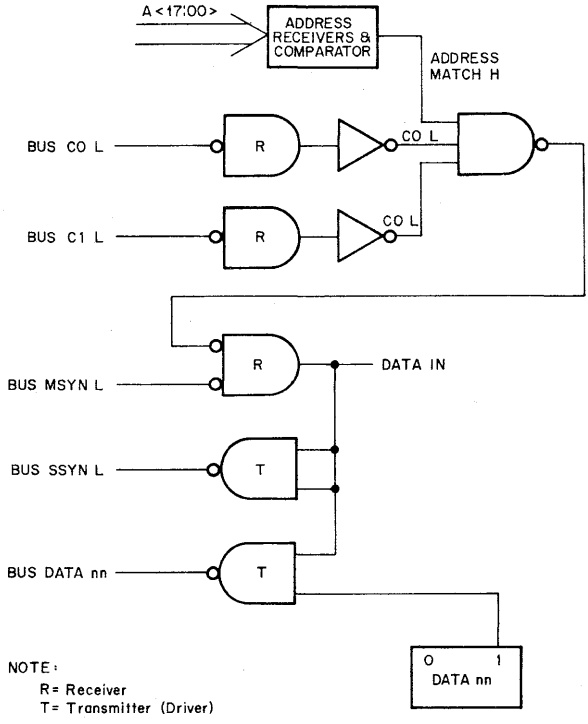


Figure 1-12 Slave Logic for DATI (Fast Response)

erations can explicitly address any byte. For example, a DATI to location 400 transfers the information in locations 400 and 401, while a DATOB to location 400 loads only location 400. In all cases, a full-word operation cannot address an odd-numbered location.

The address map (Appendix A) contains full, 18-bit wide bus addresses. Hardware in the processor forces A(17:16) to ones if A(15:13) are all ones when the processor is master; thus, the last 8K byte locations are relocated to be the highest locations accessible by the bus. All device addresses and internal processor locations are assigned in these 8K locations.

1.5.1 Interrupt and Trap Vector Locations

The first 400 locations in the address map are reserved for trap and interrupt vectors. The stack pointer overflow feature of the processor warns the user that the data in these locations may be subject to destruction if the system stack expands downward into this area. Locations 0 through 37 are used for trap vectors for internal processor use, locations 40 through 57 are reserved for use as system software communications words, and the remaining locations (up to location 400) are used for device interrupt vectors. There is no limit to interrupt vectors above 400 except that they are not protected from stack overflow.

To prevent customer-designed interfaces from interfering with standard DEC products, the vector addresses (170, 174, 270, and 274) are reserved for customer interfaces.

Each vector requires four locations (two words), and the vector addresses are constrained to even-word boundaries; that is, each vector must end in 4 or 0. (This is implemented by providing vector addresses which do not specify bits 0 or 1. Since the low bits are always 0, address bit 2 specifies either 0 or 4.)

1.5.2 Memory Locations

Memory locations, either read/write or ROM, begin at 0 and proceed to 157777. The highest numbered 8K-block in the map is used by device registers and by internal processor register addresses.

1.5.3 Device Register Locations

Each device has one or more device registers. Device register addresses are always even (A00 is 0), although byte operations may address either half of a register.

The top 8K byte locations are allocated for device register assignment. The top 4K byte (770000-777777) is reserved by DEC for processor addresses and standard peripheral devices. The 2K byte addresses (764000-767777) are reserved for customer allocation and are never assigned by DEC. It is recommended that customer-built interfaces be given addresses in this area. Starting at location 777550, the first eight locations are reserved for use with the first Teletype and first high-speed paper-tape device. Normally, the PDP-11 System is supplied with the Model 33 ASR Teletype or equivalent device. If a high-speed paper-tape device is used, it is a PC-11 Reader Punch. Specific addresses for each register are shown on the address map (see Appendix A).

1.5.4 Processor Locations

Only two processor data locations are explicitly addressable. The console switch register, at locations 777570 and 777571, is a read-only switch register on the PDP-11/20 or PDP-11/15 Console and may be used for program controlled data transfers. The processor status register (PS), at locations 777776 and 7777777

contains the processor priority level and the condition codes. The 16 processor storage locations are located at the 16 addresses from 777700 to 777717. Each address accesses a full word of data. These registers are not addressable from the bus, and the addresses are used only for deposit and examine functions from the console.

1.6 DEVICE REGISTERS

The actual transfer of data between a device and the UNIBUS takes place through one or more registers in the device. These registers may be either flip-flop storage registers or dynamic signals which are simply gated to the bus during a transfer. In addition, it is not necessary for the exact nature of the register bits to be the same. Some bits may be used for read/write (transferred on both DATI and DATO transactions); some may be write only (participate only in DATO transactions, and appear as 0s for DATI's); and some may be read only (participate only in DATI's, unaffected by DATO's). Exercise caution when assigning bit usage. For example, a BIS (Bit Set) instruction to a word containing a write-only bit does not set the bit, but clears it. This is because a BIS performs a DATIP, DATO sequence and, if the bit reads as a 0, it is rewritten as a 0. Examples of all three types are usually found in control and status registers. A typical example of a read write bit is an interrupt enable bit; an example of the write bit is a go command bit; an example of a read bit is an indicator of an error condition requiring operator intervention.

To standardize register format types, DEC has adopted some preferred bit assignments which are shown in Figure 1-13. The preferred order of register address assignments is given in Table 1-5. These preferences are included for reference only and should not be construed as mandatory requirements for interfacing to the UNIBUS. The exact nature of register assignments varies with each device. The general philosphy of this is illustrated and discussed in Chapter 3.

FUNCTION:	Device Function (read, write, punch, search, etc.) Single function devices should use bit 0 because INC CSR (an operate instruction) performs the command with less program storage and is also faster than a conventional MOV.
EXTENDED MEM:	Used to specify A(17:16) when doing device controlled data transfers to locations not in the first 65K block of addresses.
INTR ENB:	Interrupt Enable. Inhibits Interrupt on done or error if not set.
READY or DONE:	Bit set by device when internal processing is completed and the device is ready to participate in a transfer. Can be checked by the instruction sequence LOOP: TSTB CSR, BPL LOOP.
UNIT SELECT:	Used to select multiple devices connected to a single controller (such as DECtape units with operator set unit numbers).
BUSY:	Indicates that the device is doing internal processing and cannot participate in a new operation. Need not be used in many devices, READY may be adequate.
ERROR:	Indicates the source or cause of an Error Interrupt. Bit 15 is used for single-error conditions or may be the logical OR of several error conditions to allow the TST instruction to check error status.

Table 1-5 Preferred Order of Device Register Assignments

ADDRESS (OCTAL)		
N	CSR	CONTROL STATUS REGISTER
N+2	DBR	DATA BUFFER REGISTER
N+4	MAR	MEMORY ADDRESS REGISTER
N+6	WCR	WORD COUNT REGISTER

CSR—Device function, status and interrupt control
DBR—Data register for information transfer.
MAR—Memory location for block transfer. Incremented by device logic each word transfer.
WCR—Set by program to control length of block transfer.
DAR—Track or block number for mass storage devices.

When several registers are used for the same function, they should be assigned contiguous addresses, and be followed by registers of other functions in the same order as for single registers of each function.

CSR1
CSR2
DBR1
DBR2
DBR3
MAR
WCR
DAR

All register types are optional; only implemented registers should be assigned addresses.

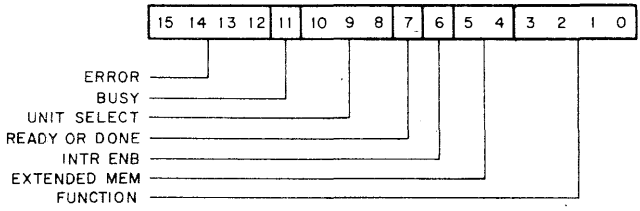


Figure 1-13 Preferred CSR Bit Assignments

PART II
Chapter 2

Interface Circuits and Hardware

This chapter discusses the specific circuits, modules, and hardware used for interfacing devices to the UNIBUS.

2.1 CIRCUITS

The UNIBUS, a high-speed data transmission facility, imposes certain restrictions when attaching other devices to it. The actual bus is a matched and terminated transmission line which must be received and driven with devices designed for that specific application. The following paragraphs describe bus transmission, bus signal levels, bus length, and bus receiver and transmitter circuits.

2.1.1 UNIBUS Transmission

The actual bus medium consists of several types of cable. The standard cabling is composed of short jumper modules that interconnect the system units within a mounting box. The M920 Module serves as the jumper module. Critical ground signals are also carried on this module. Cables used between BA11 Mounting Boxes consist of a Flexprint® cable assembly with alternating signals and grounds. The characteristics necessary for proper UNIBUS transmission are:

Characteristic Impedance:	120Ω ± 15 percent
Resistance:	0.135Ω / ft, maximum

Either twisted pair or coaxial cable laid for minimum crosstalk is recommended for long cable lengths and for applications requiring extreme physical durability of the cable.

The UNIBUS is terminated at each end by a resistive divider for each signal except the grant signals (see Figure 2-1). The grant signals are terminated with a single resistor. Two M930 Terminator Modules are included in every system to provide these functions.

2.1.2 UNIBUS Signal Levels

The rest state for all UNIBUS signal lines, except the grant lines BG< 7:4> and NPG, is a logic 0 of +3.4V. The asserted state (logic 1) is between ground and +0.8V, which is the saturation voltage of the device driving the bus. The rest state for the grant signals is ground (logic 0) and the asserted state (logic 1) is +3.4V. To guarantee operation under worst case conditions, receivers should have a switching threshold of approxiametely 2V.

Digital Equipment Corporation uses standard terminology to name signal lines to aid the reader in determining their active state. Either an H or L follows the signal name mnemonic and is separated by a space. This letter indicates the asserted (logic 1) state of the signal to be either high (approximately +3V) or low (ground). Thus, a UNIBUS data line is called BUS D00 L and a grant line is called BUS BG4 H.

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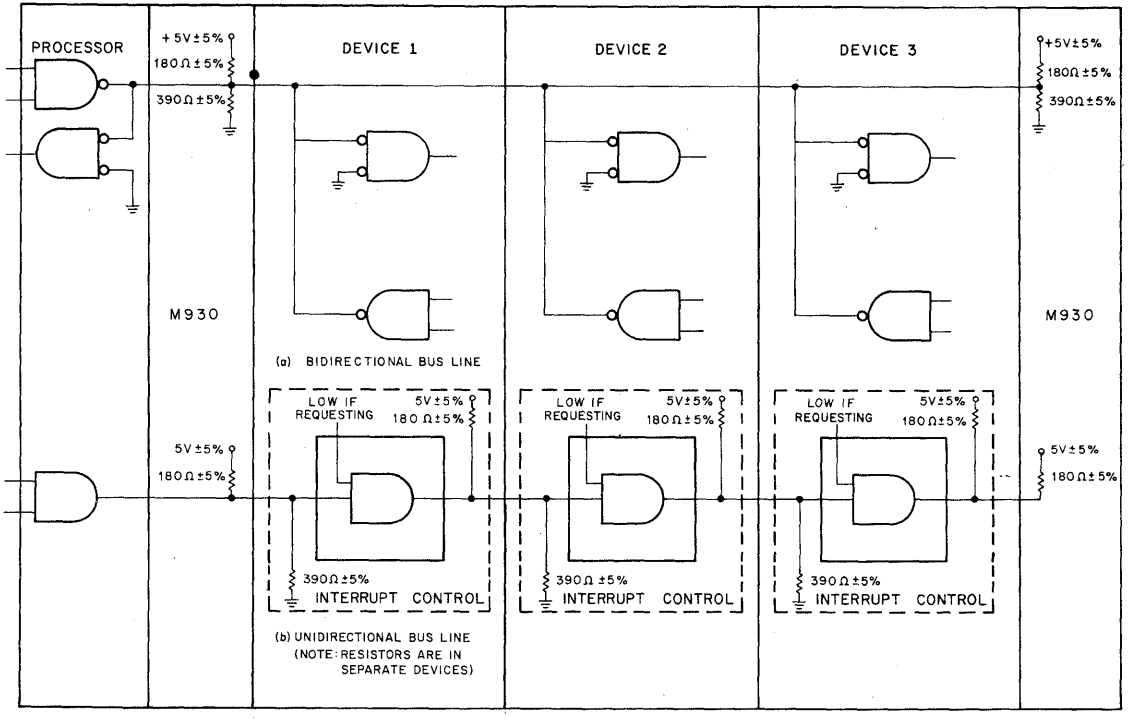


Figure 2-1 Bus Terminations for Bidirectional (a.) and Unidirectional (b.) Bus Lines

All signals which are not UNIBUS signals are characterized in terms of standard transistor-transistor logic (TTL) loads. These devices, which are similar to the 7400 Series, have a low state input load of -1.6 mA and a high state leakage current of 40μA. Outputs are characterized by the number of inputs they can drive (called fanout).

A standard TTL gate (as used in the M113) can drive 10 unit loads.

2.1.3 UNIBUS Length and Loading

The maximum length of the UNIBUS is a complex relationship involving the type of cable, the bus loading, and distribution of receiver and transmitter taps on the bus. Since the UNIBUS is a transmission line, and the transfers are asynchronous and interlocked, the electrical delay imposed by length is not a factor.

With Flexprint cable (Tape Cable S-1680), the maximum reasonable length is 50 ft. minus the combined length of all stubs or taps, which are those wires from the actual bus to the receivers and transmitters. This maximum length is obtainable only if the individual tap lengths are less than 18 inches and if the loading is not more than a standard of one receiver and two transmitters. If loads are concentrated at one end of the UNIBUS and a single load is at a distant point, the maximum length could change, provided that the crosstalk of the employed cable is low enough.

The UNIBUS is limited to a maximum of 20 unit loads. This limit is imposed because of the loading of receivers and leakage of drivers at the high state. This limit is set to maintain a sufficient noise margin. For more than 20 unit loads, a UNIBUS repeater option (DB11-A) may be used.

2.1.4 Bus Receiver and Transmitter Circuits

The equivalent circuits of the standard UNIBUS receivers and transmitters are shown in Figure 2-2. Any device which meets these requirements is acceptable. To perform these functions, Digital Equipment Corporation uses two monolithic integrated circuits with the characteristics listed in Table 2-1. Typical transmitter and receiver circuits are shown in Figure 2-3.

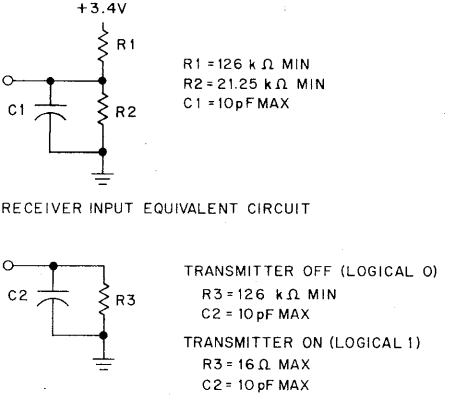


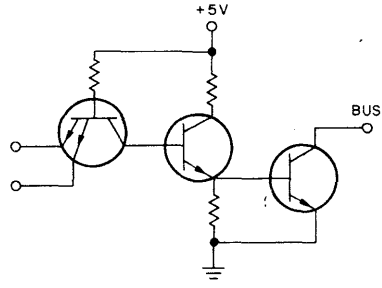
Figure 2-2 Transmitter and Receiver Equivalent Circuits

Table 2-1 Unibus Receiver and Transmitter Characteristics

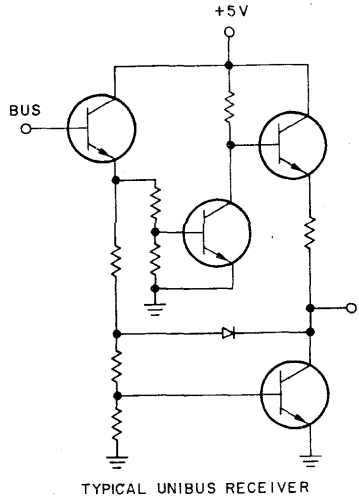
	Characteristics		Specifications	Notes
Receiver (DEC 380A)	Input high threshold	V_{IH}	2.5V min.	1
	Input low threshold	V_{IL}	1.4V max.	1
	Input current @ 2.5V	I_{IH}	160 uA max.	1, 3
	Input current @ 0V	I_{IL}	±25 μA max.	1,3
	Output high voltage	V_{OH}	3.5V min.	2
	Output high current	I_{OH}	-2 mA	2, 3
	Output low voltage	V_{OL}	0.6V max.	2
	Output low current	I_{OL}	μ -12.5 MA	2, 3
	Propagation delay to high state	T_{PDH}	10 ns min. 45 ns max.	4, 5
	Propagation delay to low state	T_{PDL}	10 ns min. 35 ns max.	4, 5
Transmitter (DEC 8881)	Input high voltage	V_{IH}	2.0V min.	6
	Input low voltage	V_{IL}	0.8V max.	6
	Input high current	I_{IH}	60μA max.	6
	Input low current	I_{IL}	-2.0 mA max.	6
	Output low voltage @ 50 mA sink	V_{OL}	0.8V max.	1
	Output high leakage current @ 3.5V	I_{OH}	25 μA max.	1, 3
	Propagation delay to low state	T_{PDL}	25 ns max.	5, 7
	Propagation delay to high state	T_{PDH}	35 ns max.	5, 8

NOTES:

1. This is a critical parameter for use on the Unibus. All other parameters are shown for reference only.
2. This is equivalent to being capable of driving seven unit loads of standard 7400 series TTL integrated circuits.
3. Current flow is defined as positive if into the terminal.
4. Conditions of load are 375Ω to +5V and 1.6KΩ in parallel with 15 pf to ground.
5. Times are measured from 1.5V level on input to 1.5V level on output.
6. This is equivalent to 1.25 standard TTL unit loading of input.
7. Conditions of 100Ω to +5V, 15 pf to ground on ouput.
8. Conditions of 1KΩ to ground on output.



TYPICAL UNIBUS DRIVER



TYPICAL UNIBUS RECEIVER

Figure 2-3 Transmitter and Receiver Typical Circuits

2.2 UNIBUS INTERFACE MODULES

The following paragraphs describe modules used for UNIBUS interfacing. These modules include the jumper module, cable, and transmitter and receiver modules that employ the circuits described in the previous paragraph. Descriptions of the address selector, bus and interrupt control, and general device interface modules are also included.

2.2.1 UNIBUS Cables

UNIBUS Jumper Module M920- The M920 Module (see Figure 2-4) is a double module that connects the UNIBUS from one system unit to the next. The printed circuit cards are on one-inch centers. A single M920 Module carries all 56 UNIBUS signals and 14 grounds.

UNIBUS Cable BC11A - The BC11A (see Figure 2-5) is a 120-conductor Flexprint cable used to connect system units in different mounting drawers or to connect a peripheral device removed from the mounting drawer.

The 120 signals include all the 56 UNIBUS lines plus 64 grounds. Signals and grounds alternate to minimize crosstalk. Cable types and lengths are listed below:

Type	Length (ft.)
BC11A-2	2.0
BC11A-5	5.0
BC11A-8f	8.5
BC11A-10	10.0
BC11A-15	15.0
BC11A-25	25.0

2.2.2 UNIBUS Terminations

The M930 UNIBUS Terminator Module is a short, double-size module that terminates all signal lines on the Unibus. This module requires 1.25 amps at 5v. All pins have a resistive divider termination of 180Ω to +5v and 390Ω to ground, except those listed below:

390Ωin parallel with 0.001 μf to +5 (for AC LO, DC LO)	180Ω to +5V (for grant lines)	Ground Pins		+5V Input Pins
BF1	AV1	AB2	BB2	AA2
BF2	AU1	AC2	BC2	
	BA1	AN1	BD1	BA2
	BB1	AP1	BE1	
	BE2	AR1	BT1	
		AS1	BV2	
		AT1		
		AV2		

2.2.3 UNIBUS Receivers and Transmitters

Various bus driver and receiver modules may be used in interfaces to provide signal levels compatible with the UNIBUS. These modules (M783 , M784,M785, and M798) are discussed separately in the following paragraphs.

2.2.3.1 M783 UNIBUS Transmitter - This transmitter module contains 12 drivers; 8 drivers have a common gate line, 4 have 2-input positive AND gating. Input loading is 1.25 standard TTL load. The module is a single-height, 8.5 inch-long Flip-Chip. A circuit schematic of the M783 Transmitter is shown in Figure 2-6.

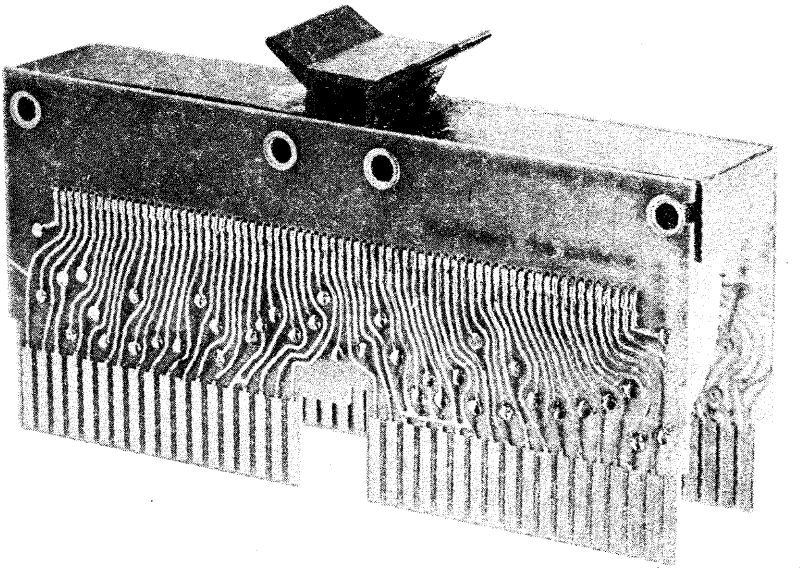


Figure 2-4 UNIBUS Jumper Module M920

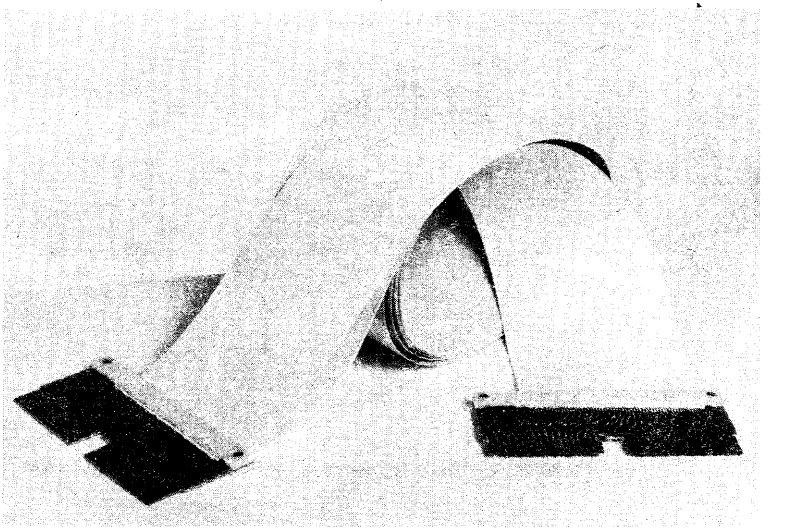


Figure 2-5 UNIBUS Cable BC11A

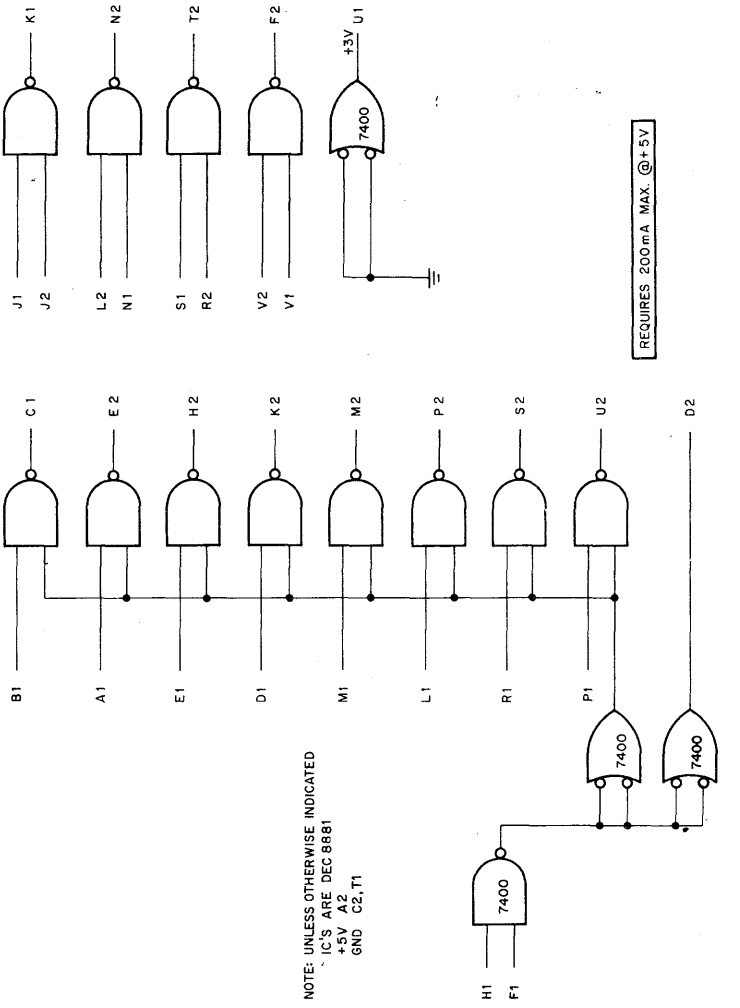


Figure 2-6 M783 UNIBUS Transmitter (schematic diagram)

2.2.3.2 M784 UNIBUS Receiver- This receiver module consists of 16 DEC 380A inverting circuits which receive bus signals and provide a buffered bus signal output. The output fanout is seven standard TTL unit loads. The receiver module is a single-height, 8.5-inch-long Flip-Chip. A circuit schematic of the M784 Receiver Module is shown in Figure 2-7.

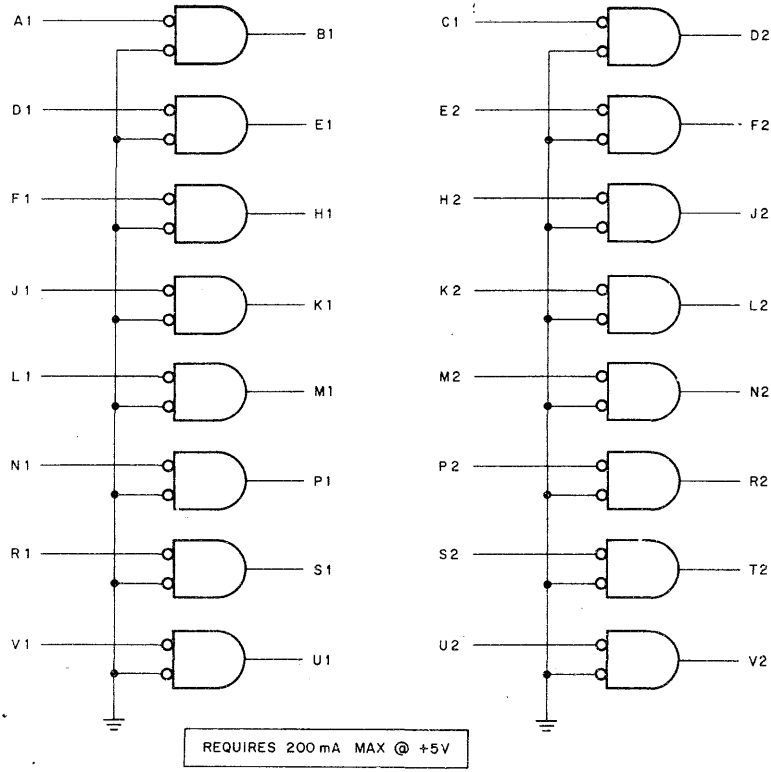


Figure 2-7 M784 UNIBUS Receiver (schematic diagram)

2.2.3.3 M785 UNIBUS Transceiver- This module consists of eight pairs of DEC 8881 Drivers and DEC 380 Receivers which are used for bidirectional interfacing to the UNIBUS. The drivers and receivers have two common gate lines: one for receivers, one for drivers. The driver input loading is 1.25 standard unit load and the receiver fanout is 7 standard TTL unit loads. The module is a single-height, 8.5-inch-long Flip-Chip. A circuit schematic of the M785 Transceiver Module is shown in Figure 2-8.

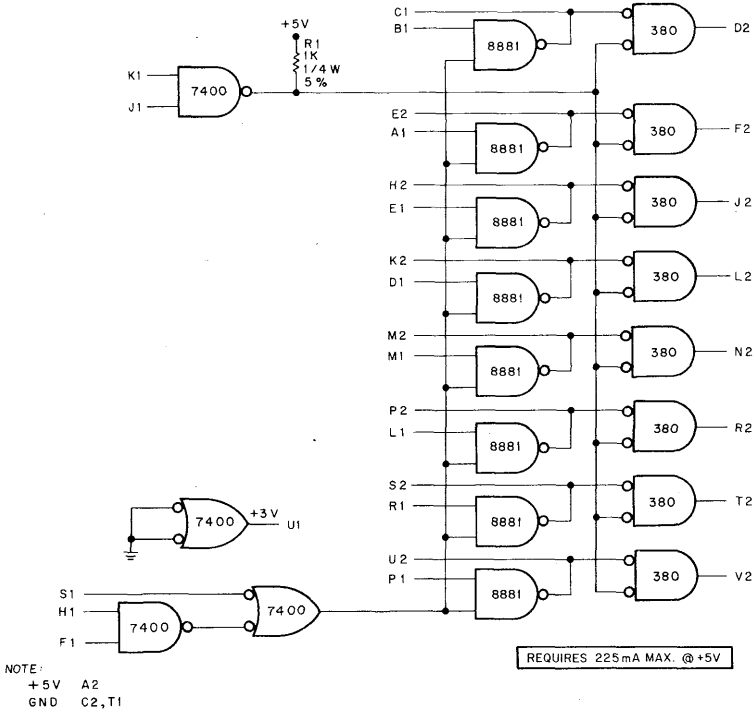


Figure 2-8 M785 UNIBUS Transceiver (schematic diagram)

2.2.3.4 M798 UNIBUS Drivers- This module consists of 16 non-inverting UNIBUS drivers. The module is used in device interfaces to minimize the loading effect caused by attaching several drivers to the same UNIBUS signal line, as in the case of a device containing multiple registers. A typical driver circuit is shown in Figure 2-9 a. Loading of signal lines on the UNIBUS is restricted to one unit load per device. A unit load is the equivalent of one receiver input and two driver outputs (210μA total).

In addition, the M798 module allows the UNIBUS to be driven by standard open collector TTL gates. The inputs to each M798 driver circuit are pulled to +5V through a 1 kΩ resistor. As shown in Figure 2-9b, an internal wire-ORed bus is created that is driven from standard open collector gates (available on M141 and M149 modules) or from UNIBUS drivers (available on M783 UNIBUS Transceiver modules). The driver input loading is 4.1 TTL loads for each of the 16 inputs. The output drive signal for each of the 16 outputs is 50 mA sink at 0.8V maximum. The open collector leakage is 25μ A. A circuit schematic of the M798 UNIBUS Drivers module is shown in Figure 2-10.

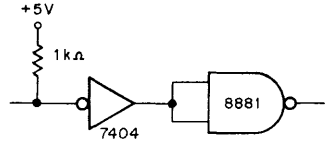


Figure 2-9 a. One of 16 Circuits on the M798

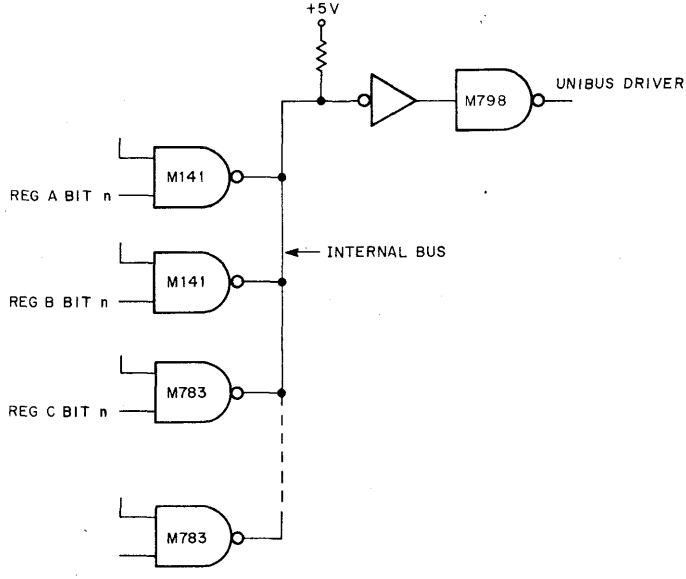
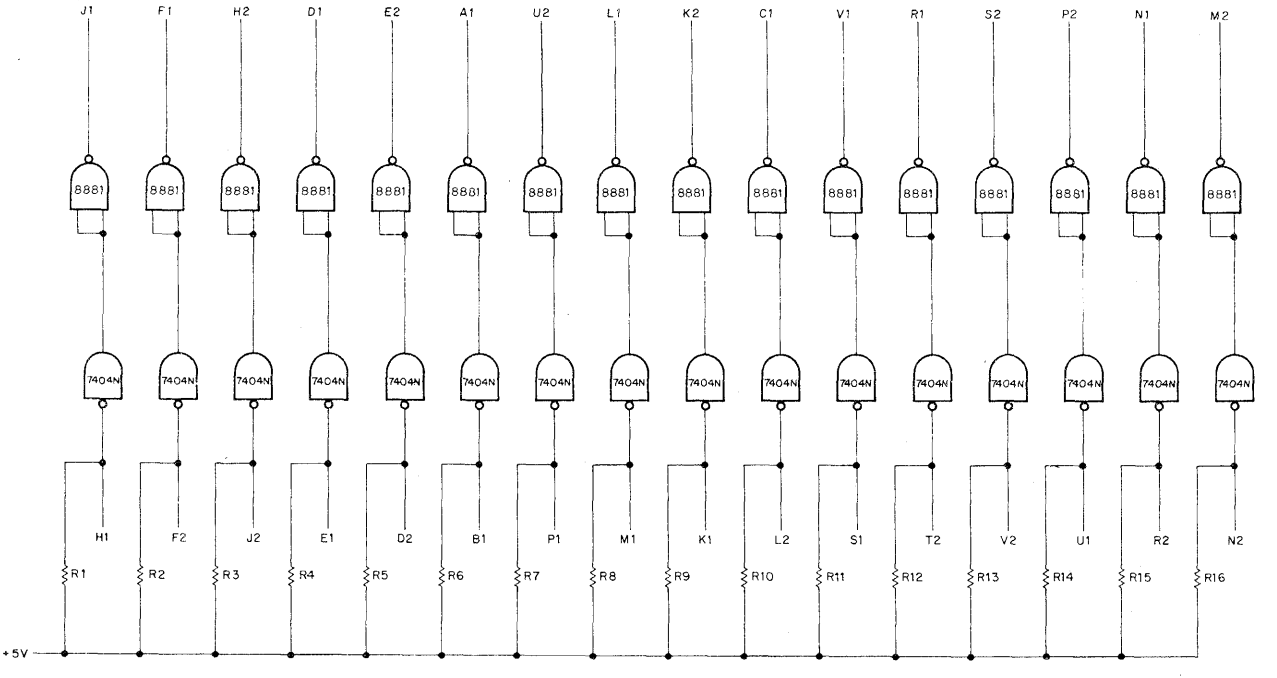


Figure 2-9 b. Typical Use of M798



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1K, 1/4W, 5%
+5V A2
GND C2, T1

Figure 2-10 M798 UNIBUS Drivers (schematic diagram)

2.2.4 M105 Address Selector Module

The M105 Address Selector Module provides gating signals for up to 4 full 16-bit device registers. A block diagram of this module is shown in Figure 2-11. Note that IN and OUT are always used with respect to the master (controlling) device. Thus, when the M105 is used in a peripheral device, an OUT transfer is a transfer of data out of the master (such as the processor) and into the device. Likewise, an IN transfer is the operation of the peripheral furnishing data to the processor. The M105 Module is described more fully in following paragraphs.

2.2.4.1 Inputs- The M105 Module input signals consist of 18 address lines, A <17:00>; 2 bus control lines, C <1:0>; and a master synchronization MSYN line. The address selector decodes the 18-bit address on lines A<17:00> as described below. This address format, used for selecting a device register, is shown in Figure 2-12. Note that all inputs are standard bus receivers.

a. Line A00 is used for byte control.

b. Lines A01 and A02 are decoded to select one of the four addressable device registers.

c. Decoding of lines A<12:03> is determined by jumpers on the module. When a given line contains a jumper, the address selector searches for a zero on that line. If there is no jumper, the address selector searches for a one.

d. Address lines A<17:13> must be all ones. This specifies an address within the top 8K byte address bounds for device registers.

2.2.4.2 Slave Sync (SSYN)- When SSYN INH is grounded, it inhibits the acknowledgment signal (SSYN) normally generated by the M105. In this case, the SSYN must be generated by another source. When SSYN INH is not grounded, SSYN is returned to the master 100 ns after register select becomes true. This time may be extended to a maximum of 400 ns by adding an external capacitor between SSYN INH and ground SSYN INH can also be driven with an open collector gate.

2.2.4.3 Outputs- The M105 Output Signals permit selection of four 16-bit registers and provide three signals used for gating information to and out of the master device. The M105 may be used instead to select up to eight 8-bit registers, or any appropriate combination of byte and word registers.

The input signals select the M105 control output line states as shown in Tables 2-2 and 2-3.

Table 2-2 M105 Select Lines

Input Lines A<02:01>	Select Lines True(+ 3V)
00	0
01	2
10	4
11	6

NOTE

1. Lines A<17:13> must be all 1s (0V on Unibus).
2. Lines A<12:03> are selected by jumpers.

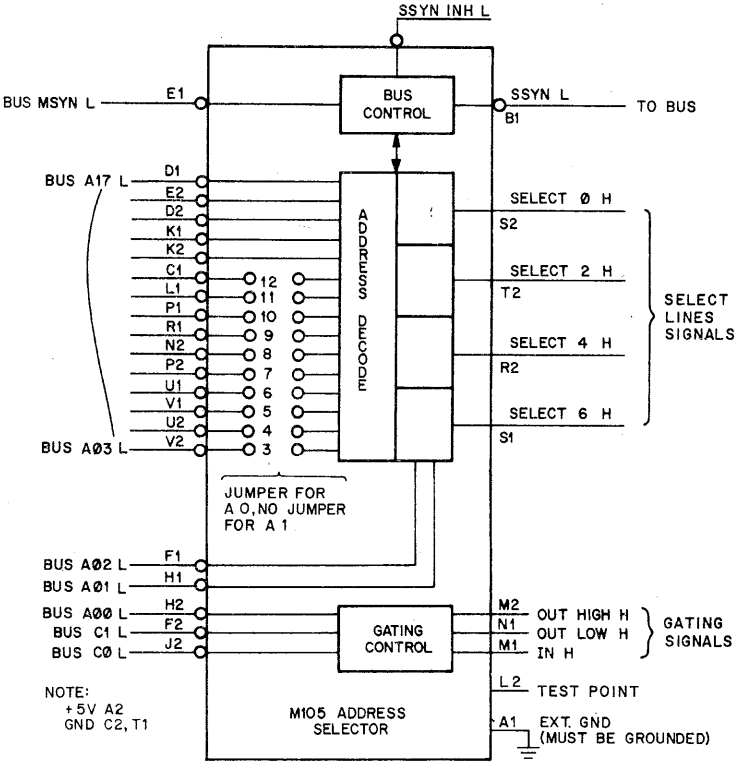


Figure 2-11 M105 Address Selector

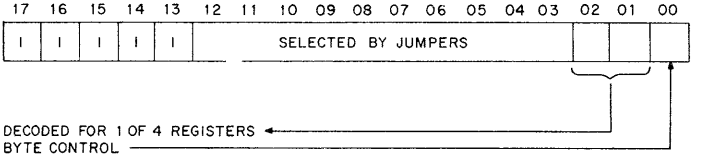


Figure 2-12 Device Register Select Address Format

Table 2-3 Gating Control Signals

Mode Control C<1:0>	Byte Control A00	Gating Control Signals True (+3V)	Bus Sequence
00	0	IN	DATI
00	1	IN	DATI
01	0	IN	DATIP
01	1	IN	DATIP
10	0	OUT LOW OUT HIGH	DATO
10	1	OUT LOW OUT HIGH	DATO
11	0	OUT LOW	DATOB
11	1	OUT HIGH	DATOB

NOTE

Gating control signals may become true although select lines are not.

2.2.4.4 Specifications- The M105 output fanout is ten standard TTL loads for register select lines and eight standard TTL Loads for gating control lines. The module is a single-height, 8.5-inch-long Flip-Chip. A circuit schematic for this module is shown in Figure 2-13. Note that pin A1 (EXT GND) must be grounded by the user.

When using the output signals of the M105 to load registers that comprise storage elements that are edge-triggered, insure that this edge is derived from the positive transition of the SELECT line, i.e. the leading edge of MSYN. A circuit example of this type is shown in Figure 3-2.

If the storage elements are loaded by a strobing pulse (not edge-triggered), then the entire pulse must be generated prior to the assertion of SSYN. The length of the loading pulse can be lengthened by adding capacitance to SSYN INHB on the M105.

2.2.5 M7820 Interrupt Control Module

The M7820 Interrupt Control Module provides the circuits and logic required to make bus requests and to gain control of the bus (become bus master). The module also includes circuits needed to generate an interrupt, if desired. The module contains two completely independent request and grant acknowledge circuits (channels A and B) for establishing bus control. The interrupt control circuit can be used with either, or both, of the request channels and provides a unique vector address for each channel. Figure 2-14 is a block diagram of the M7820 Module, which is a single-height, 8.5-inch wide Flip-Chip.

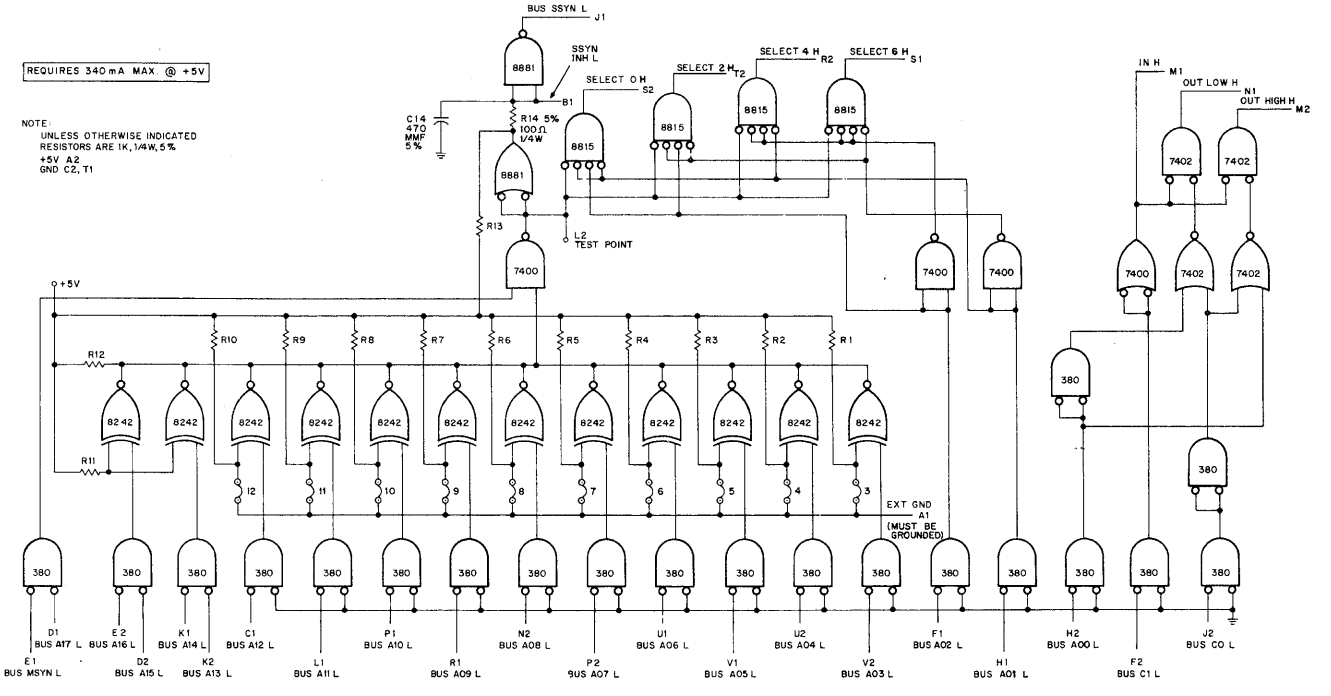


Figure 2-13 M105 Address Selector (schematic diagram)

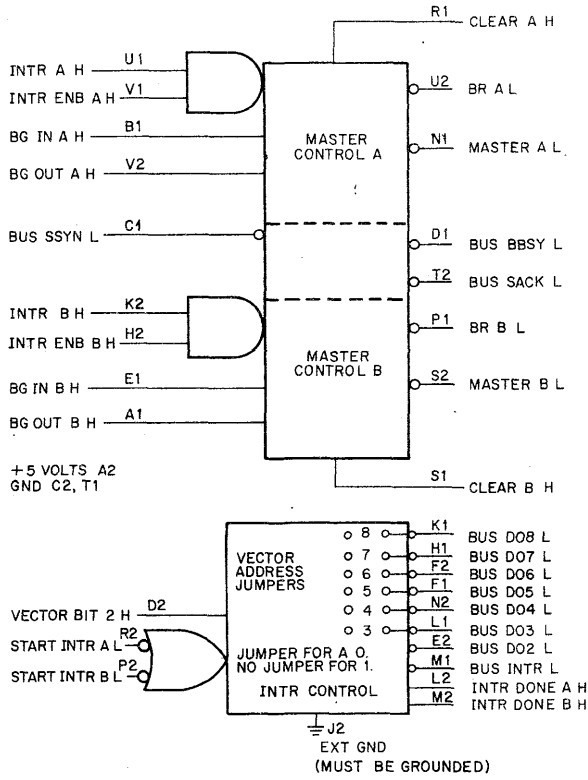


Figure 2-14 M7820 Interrupt Control (block diagram)

The master control section (either channel A or B) is used to gain control of the bus. When the INTR and INTR ENB requesting inputs are asserted, a bus request is made on the BR level corresponding to the level of the BR line wired to the BR pin of the module. When the priority arbitration logic in the system recognizes the request and issues a bus grant signal, the master control circuit acknowledges with a SACK signal. When the device has fulfilled all requirements to become bus master, the master control circuit asserts BBSY and then asserts a MASTER signal. (Refer to Section 1.3.1.)

Once the device has gained bus control by means of a BR request, an interrupt can be generated. If an interrupt is desired, the module is interconnected as shown in Figure 2-15. This figure illustrates the use of the two channels to first generate requests for bus control and then initiate interrupts. The request from channel A is a slightly higher priority than the channel B request because the bus grant signal first enters A, then enters B.

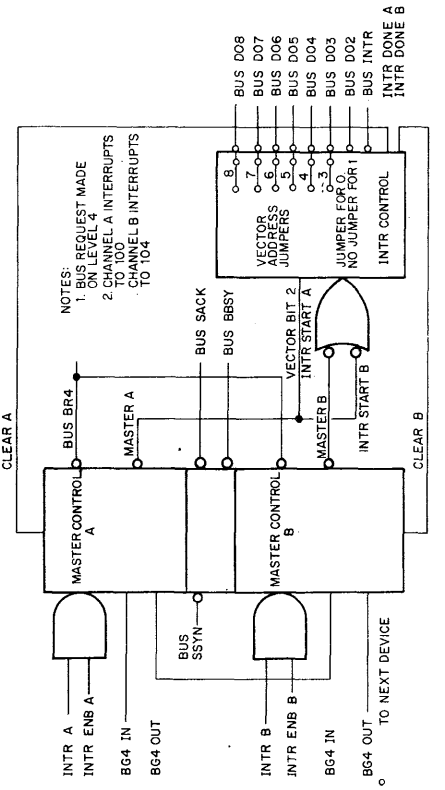


Figure 2-15 M7820 Interconnection for 2-Channel Interrupt

The vector address is selected by jumpers on the M7820 Module. Since the vector is a two-word (four-byte) block, it is not necessary to determine the state of bits 0 and 1. The seven selectable lines determine vector address. The least significant line is controlled by the VECTOR BIT 2 input signal. If this input is asserted, then bus line D02 is asserted. Thus, the interrupt on channel A uses a vector at location 100 and channel B uses a vector at location 104.

Figure 2-16 illustrates an M7820 Module used for bus control in a device that directly transfers data to memory and then causes an interrupt when the transfer is completed. Channel A is connected to the NPR and NPG lines and is used to gain bus control for direct to memory, or device-to-device, transfers. Channel B is used to gain bus control for an interrupt.

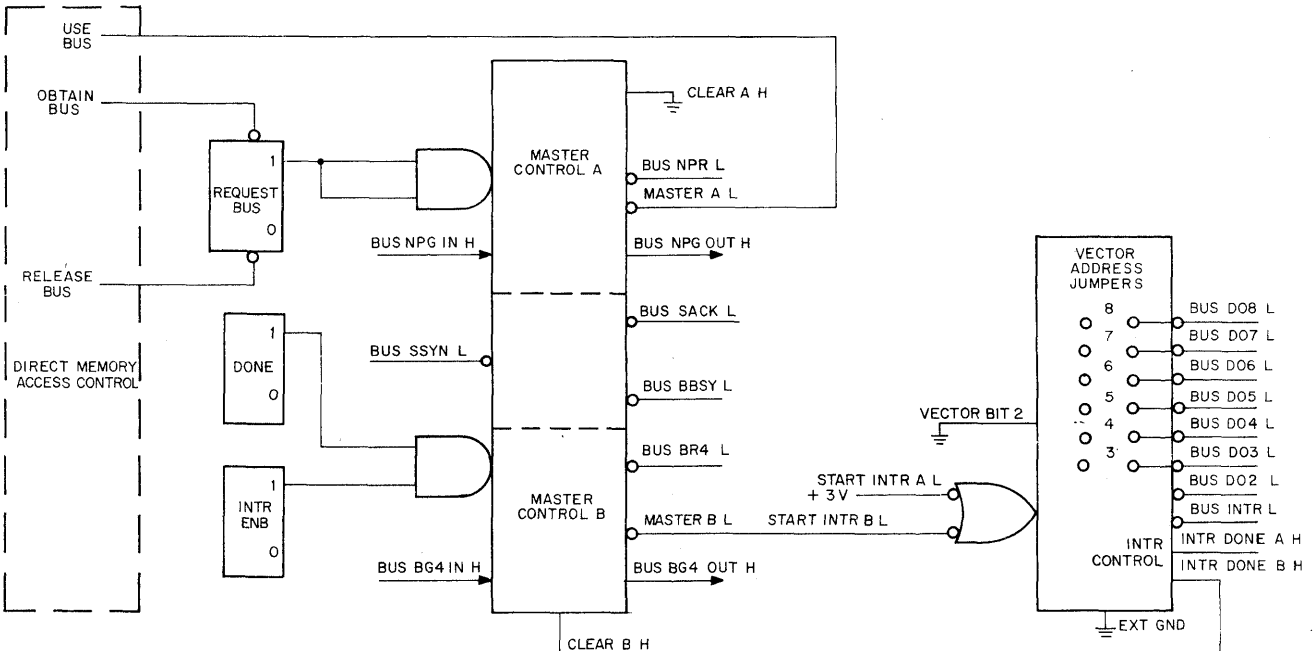


Figure 2-16 M7820 Interconnection for Direct Memory Access

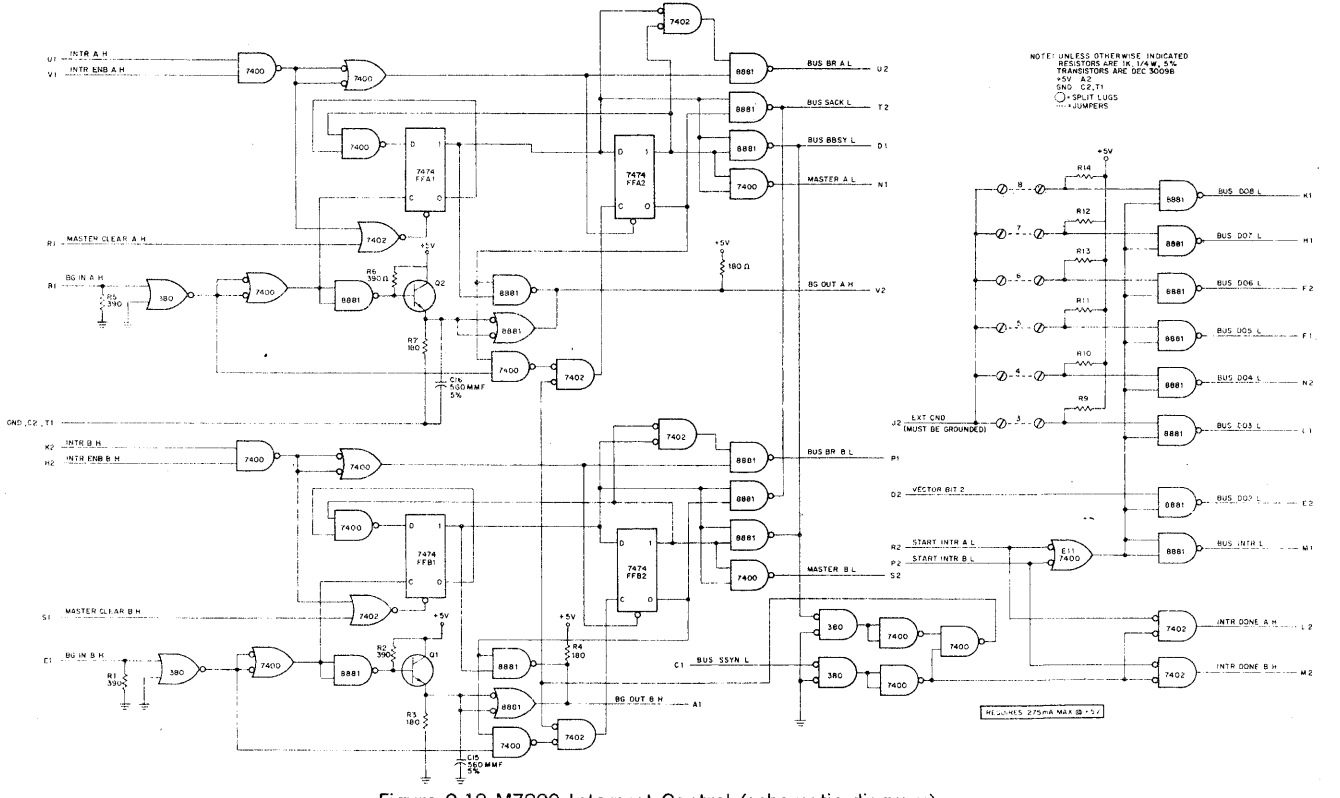


Figure 2-18 M7820 Interrupt Control (schematic diagram)

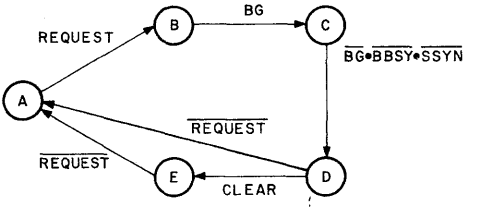


Figure 2-17 State Diagram of Master Control

Each M7820 Module master control section contains two flip-flops that sequence through four states, thereby controlling the request for bus control. Figure 2-17 is a state diagram of this sequence and Figure 2-18 shows a circuit schematic of the M7820. The BG IN signal is allowed to pass through the module to BG OUT when the device is not issuing a request (state A), is master (state D), or has had the request honored (state E). To request bus use, the AND condition of INTR and INTR ENB must be satisfied. These levels must be true at least until the request is granted. Once bus control has been attained, it can be released by either asserting CLEAR or by negating either INTR or INTR ENB. The first method leaves the master control in state E, thereby inhibiting further bus requests even if INTR and INTR ENB remain asserted. In order to make another bus request, INTR or INTR ENB must be dropped and then reasserted to cause the module to advance from state E through state A to state B where it asserts the request line. This prevents multiple interrupts when the master control is used to generate interrupts. The second method is used to release the bus after NPR use. Note that pin J2 (EXT GND) must be grounded by the user. A summary of all M7820 signals is listed in Table 2-4.

Table 2-4 Summary of M7820 Signals

Signal	Assertion Level	Input Loading	Output Drive
INTR A, B	H	1 TTL (each)	
INTR ENB A, B	H	1 TTL	
CLEAR A, B	H	1 TTL	
MASTER A, B	L		10 TTL
START INTR A, B	L	2 TTL	
INTR DONE A, B	H		10 TTL
BG IN A, B	H	1 R*	
BG OUT A, B	H		2 D**
BR A, B	L		1 D
VECTOR BIT 2	H	1 TTL	
BUS SSYN	L	1 R	
BUS BBSY	L	1 R	2 D
BUS SACK	L		2 D
BUS INTR	L		1 D
BUS D<08:02>	L		D

*R = Standard Unibus receiver load.
**D = Standard Unibus transmitter (driver) output.

2.2.5a The M7821 Interrupt Control Module

The M7821 Interrupt Control Module is a replacement for the M7820 that improves PDP-11 system performance. In almost all cases, it may be used directly in place of the M7820, without making any changes to hardware or software. A block diagram of the module is shown in Figure 2-17a

NOTE

The following description assumes the reader understands the function and operation of an M7820.

The M7821 does not have two identical Master Control halves. For devices which use one half of the module to become master with an NPR and one half for a BR, the top half (Request Bus pins U1 and V1) must be used for NPR and the bottom half (Request Bus pins H2 and K2) must be used for BR.

The NPR half of the module has the ability to prevent the un-assertion of BUS SACK for devices that do more than one data cycle each time they request the bus. (See section 1.4.1-h.) This is done by holding pin J2 high until the beginning of the last bus cycle. SACK will be unasserted as soon as pin J2 goes low, and the input on J2 can, therefore, be a pulse or a level. Pin J2 is active only when the Master signal is asserted (pin N1 is low), and, therefore, pin J2 may be permanently grounded if only one bus cycle is done for each request.

NOTE

The M7820 requires pin J2 to be grounded for the interrupt section of the module to work, so the M7821 is compatible.

The BR half of the module does not have the ability to hold BUS SACK asserted and always drops SACK when BUS BBSY is asserted. However, this section of the module does have some special circuitry that looks at the BUS NPR line, which must be wired to pin J1 on the M7821. This circuitry, if it sees the assertion of the bus grant line to which the module is wired while BUS NPR is asserted, will block the grant and return SACK. When BBSY becomes unasserted from the last bus master, the M7821 will then clear SACK off the bus. The processor will then be able to service the NPR, improving the latency time for NPR devices.

CAUTION

Only some PDP-11 processors will work with the special circuitry described above. There is a jumper on the M7821 module which, when cut, prevents the special circuitry from working.

NOTE

Pin J1 is unused on the M7820 module, and if BUS NPR is not wired to this pin, the special jumper noted above must be cut.

If both halves of the M7821 are used for BR requests, pin J2 must be grounded and the jumper may be cut as required. If both halves are used for NPR requests, pin J2 may be used as required, and the jumper must be cut. Please note that if the normally BR half (Request Bus pins H2 and K2) are used for NPR's, only one bus cycle may be done per request.

The interrupt section of the module has been changed slightly also. The jumpers on the M7821 module must be left in to generate a "one" in that bit position of

the vector, and cut out to generate a "zero." This is the reverse of the M7820. A jumper has also been added to vector bit 2. If the module is to be used the same way as a M7820, the jumper for bit 2 must be left in. However, if only one vector is being generated by the module, pin D2 should be permanently wired to a high level, and then the jumpers can be used to assign vectors to every vector location (4 bytes) without changing backpanel wiring. Note that the jumper for bit 2 must also be in for a one and cut for a zero.

Summary of Compatiblity Considerations

On the M7820, pin J2 must be grounded for the interrupt section to work. If pin J2 is grounded, then an M7821 module can be directly plugged in if the special jumper is cut, the vector bit 2 jumper is left in, and the rest of the jumpers are cut appropriately.

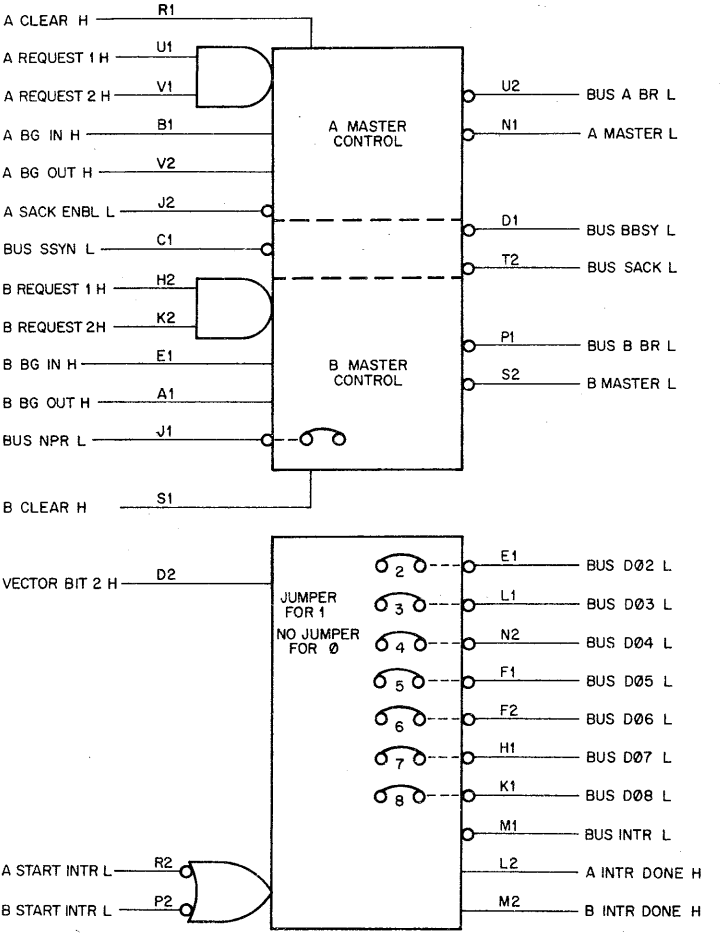


Figure 2-17b-M7821 Interrupt Control Block Diagram

2.2.6 M795 Word Count and Bus Address Module

The M795 Word Count and Bus address Module is used to interface direct memory access (DMA) devices to the UNIBUS. This module contains two 16-bit counters: one counter is used to count the number of data transfers that occur; the other counter is used to specify the bus address of the data to be transferred.

Block transfer devices that function as bus master during data transfers usually require two registers to hold the parameters of the transfer. One parameter is transfer count. Initially, a register is loaded with the 2's complement of the number of items to be transferred to or from memory. After each transfer is complete, the register is incremented. If the new value of the register is 0 (indicated by an overflow), further transfers are inhibited and the block transfer is complete. Since information can be transferred in words (16 bits each) on the UNIBUS the name Word Count (WC) is usually assigned to this register. However, the UNIBUS is also capable of transferring 8-bit bytes of data at a time, and this register may be used equally as well as a Byte Count register.

The second parameter used in block transfers is the transfer address. Initially, a register is loaded with an address that specifies the memory location to, or from, which data is to be transferred. The register is incremented after each transfer; thus, the register continually "points" to sequential memory locations. Since memories and devices have addresses on the UNIBUS, this register is usually called the Bus address (BA) register.

A simplified block diagram of the M795 module is shown in Figure 2-19. Both the word count (WC) and bus address (BA) registers consist of 16 flip-flops. These flip-flop registers can be loaded by placing data on the 16 data line inputs common to both registers and asserting the appropriate loading signal. There are four independent loading signals: WC high byte, WC low byte, BA high byte, and BA low byte. Each of the outputs of the 16 bits in the WC register are connected to a set of DEC 8881 UNIBUS drivers. The contents of the WC register can be gated to the data bus when the appropriate gate signal is activated. The BA register also has a set of UNIBUS drivers connected to each output so that the register contents can be gated to the data bus. Note that the driver outputs of both the WC and BA registers are wire ORd together. In addition, the BA register has a set of drivers with independent outputs to allow it to drive the address bus.

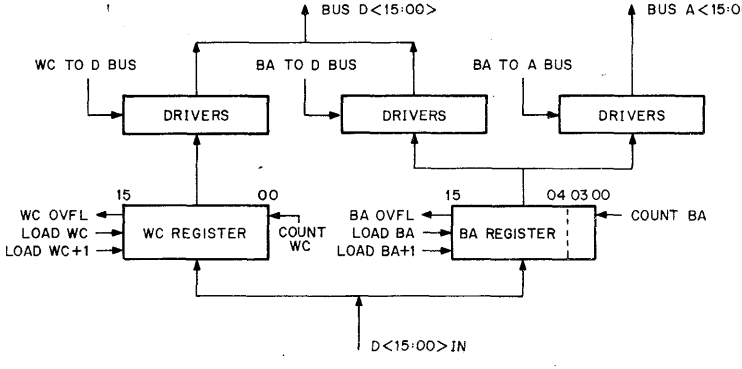


Figure 2-19 M795 Word Count and Bus Address (block diagram)

The storage element on the M795 is not an edge-triggered device; data must be established and held for the duration of the loading pulse. Refer to section 2.2.4.4 for circuit implementation details.

The BA register can be incremented by either 1 or 2 as a function of a control input (+3V = +1; ground = +2). This incrementation capability allows addressing of either sequential bytes or words. The register is incremented on the trailing edge of a positive pulse applied to the count input of the register. The carry between bits 03 and 04 is broken and brought out to pins on the module. Normally, these pins are jumpered together externally to allow for a full 16-bit count. However, they can be controlled to inhibit the carry and to force repeated addressing of 16 sequential byte addresses. This feature can be used in device-to-device transfers. An overflow pulse is provided as an output whenever the register is incremented from all 1s to all 0s.

The WC register is incremented by either 1 or 2 as a function of its control input. The register increments on the trailing edge of a positive pulse applied to the count input of the register. An overflow pulse is also available. Both registers are reset to all 0s whenever the CLEAR signal is asserted.

Table 2-5 M795 Input Signals

Signal Name	Assertion Level	No. of Signals	Loading	Operation
D<15:00>IN	+3V = 1	16	1.5	Data inputs to register.
LOAD WC LOAD WC + 1	0V	4	1	Loads data on input into selected byte of register.
LOAD BA LOAD BA + 1				Low pulse of 250 ns minimum duration
WC TO D BUS BA TO D BUS BA TO A BUS	0V	3	2	Gates selected register to bus.
CLEAR WC + BA	+3	1	2	Clears all bits. High level of 1 μs minimum duration.
BA INC CONTROL WC INC CONTROL	+3V = +1 0V = +2	2	3	Controls amount of incrementation.
COUNT WC COUNT BA	+3V	2	4	Trailing edge of positive pulse increments register (100 ns minimum).
BA CARRY IN	0V	1	3	Carry into upper bits of BA.

Table 2-6 M795 Output Signals

Signal Name	Assertion Level	No. of Signals	Drive Capability	Operation
BA CARRY OUT	OV	1	10	Carry out of low four bits.
BA OVFL WC OVFL	OV	2	10	Register over flow low level pulse.
BUS D<15:00>	OV = 1	16	UNIBUS	Drives data line.
BUS D<15:00>	OV = 1	16	UNIBUS	Drives address.

2.2.7 M796 UNIBUS Master Control Module

The M796 UNIBUS Master Control Module provides extremely flexible control logic that is used to control data transfer operations on the UNIBUS when a device is functioning as bus master. In addition to controlling the four transfer operations (DATI, DATIP, DATO, and DATOB), the M796 module generates strobe and gating signals which transfer both addresses and data to and from the bus; handles deskewing of data received from the bus; protects against data transfers to nonexistent devices by the use of time-out circuits; and provides a flip-flop and integrating one-shot that can be used by the customer for special control functions.

Any device in the PDP-11 system may have the capability of gaining control of the bus and, as bus master, of transferring data to and from other slave devices on the bus. This operation is performed independently of processor control and is usually referred to as Direct Memory Access (DMA). The logic neccessary to gain control of the bus is provided by the M7820 Interrupt Control Module. The M7820 module requests use of the bus (usually by means of an NPR request), receives the bus grant signal from the processor, asserts selection acknowledge (SACK), waits until the current bus master releases control of the bus, and then asserts BUS BUSY, thereby gaining bus control.

Upon becoming bus master, the device is free to conduct a data transfer. A DATI cycle is performed if the device needs data (either a word or byte) from memory; a DATO cycle is performed if the device is storing a word of data in memory (DATOB cycle for byte storage); a two-cycle DATIP, DATO(B) operation is performed if data held in memory is to be modified as in the case of increment memory or add to memory functions.

In order to execute one of these transfer cycles, the device must set BUS C<1:0>for the required type of data transfer, specify the address of the slave device participating in the transfer, assert the MSYN signal, and then wait for the SSYN response from the slave. Data must either be gated to D<15:00> on a DATO cycle or be received and strobed at the proper time on a DATI cycle. The M796 module performs these functions.

Figure 2-20 is a block diagram of the M796 UNIBUS Master control module. The BUS C1 and BUS C0 outputs can directly drive the UNIBUS and are asserted as a function of the control inputs. Table 2-7 lists the states of the control inputs for the four possible bus cycles.

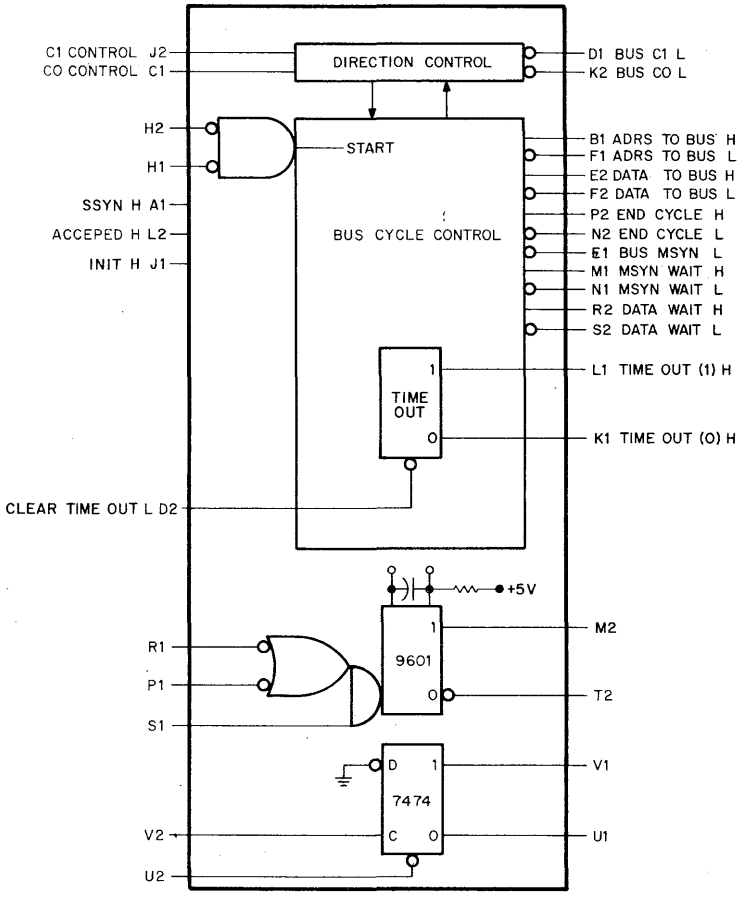


Figure 2-20 M796 UNIBUS Master Control (block diagram)

Table 2-7 Control Line Input States for M796

C1	C0	Bus Cycle
0	0	DATI
0	1	DATIP
1	0	DATO
1	1	DATOB

NOTE:0 = low level, 0V
1 = high level, +3V

The data transfer sequence is triggered by meeting the AND condition of two low levels. Usually these two inputs are tied together and are connected to the MASTER signal produced by the M7820 Interrupt Control Module. When the AND condition is met, it produces the START signal, which is an internal signal in the M796 module. At the transition of the START signal, both BUS C1 and BUS C0 are asserted as determined by their respective control inputs. The ADRS TO BUS signal is also asserted and is used to gate the address of the slave onto BUS A<17:00>. If an output cycle is specified (C1 = 1), the DATA TO BUS signal is asserted and is used to gate the data to be transferred to the slave onto BUS D<15:00> The BUS MSYN signal is asserted 200 ns after START becomes true. The master device then waits for a response from the slave.

In a data output cycle (DATO), assertion of SSYN causes BUS MSYN to be negated immediately. After a 100-ns delay, BUS C1, BUS C0, ADRS TO BUS, and DATA TO BUS are negated. When these signals drop, an END CYCLE pulse appears and is usually used to release control of the bus.

In a data input cycle (DATI), the assertion of SSYN produces a 200-ns pulse that appears as DATA WAIT. This delay allows time for the incoming data to deskew and settle. The trailing edge of the DATA WAIT pulse can be used to clock data from the slave into the master device. If a strobe pulse is necessary, the trailing edge of DATA WAIT can be used to trigger the one-shot provided on the module. In either case, once data is received, a positive-going edge is applied to DATA ACCEPTED, causing BUS MSYN to be negated initially, followed by negation of ADRS TO BUS, BUS C1, and BUS C0 100 ns later.

A TIME-OUT flip-flop on the module is set if a SSYN response fails to occur within 20μs after BUS MSYN is asserted. When this flip-flop is set, the bus cycle is not performed. The TIME-OUT flip-flop is cleared by asserting the CLEAR TIME-OUT signal.

The M796 module provides a special flip-flop that has the clock, reset, 1 side, and 0 side available to the customer. The flip-flop is clocked by a positive transition on the clock input.

An integrating one-shot is also provided on the module. This one-shot is triggered whenever the output of the gating input becomes true: $(\overline{R1} + \overline{P1}) \cdot S1$. The output pulse width of this one-shot is 150 ns but can be lengthened by adding capacitance across the pair of split lugs on the module.

Note that all times mentioned represent nominal values with a tolerance of $\pm 25\%$. The delays and pulses provided by the module are controlled by simple RC circuits. Therefore, if the customer has any special requirements, part substitutions can be made to alter these time constants.

Figure 2-21 illustrates a typical interconnection schematic for the M796 UNIBUS Master Control module used in conjunction with the M7820 Interrupt Control module. The read/write (R/W) flip-flop is part of the device interface logic and determines the direction of the data transfer (set for a DATO, clear for a DATI). The data transfer is initiated by pulsing SET REQUEST which sets REQUEST BUS. The REQUEST BUS signal generates an NPR request which, when granted, gives bus control to the device as indicated by the MASTER signal. The MASTER signal causes the internal START signal to be generated. This signal triggers the sequence of timing signals. Timing diagrams for DATO and DATI cycles are shown in Figures 2-22 and 2-23 respectively.

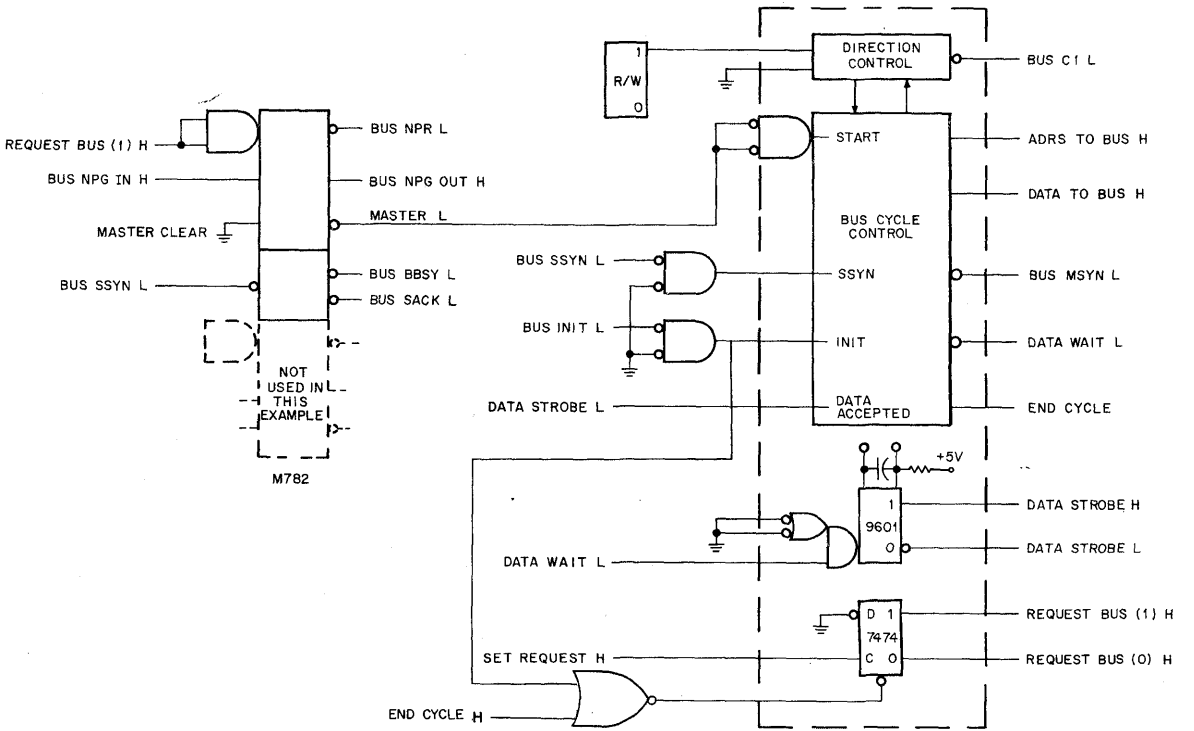


Figure 2-21 M796 UNIBUS Master Control (typical use)

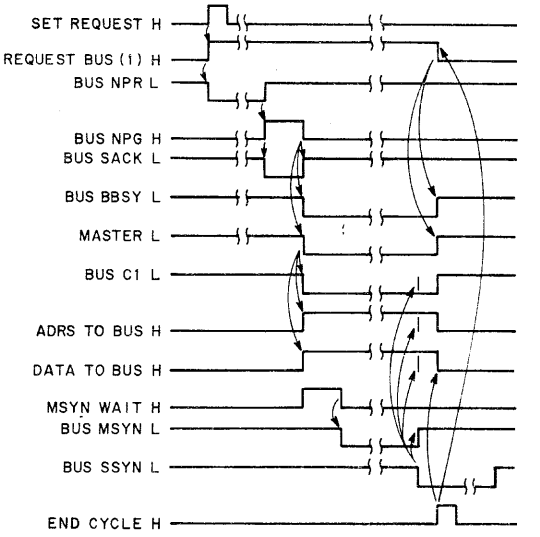


Figure 2-22 M796 Timing Diagram for DATO

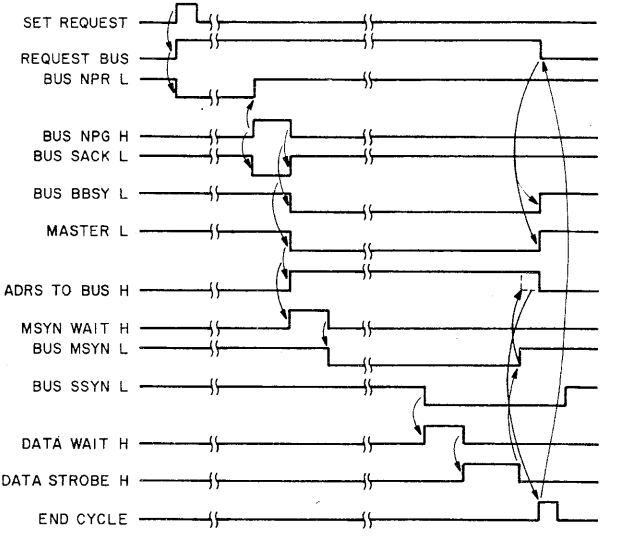


Figure 2-23 M796 Timing Diagram for DATI

Note that in a DATI operation, the DATA WAIT signal is generated when BUS SSYN is received. The trailing edge of DATA WAIT fires the one-shot that produces the DATA STROBE signal. This signal gates the data present on the bus data lines into the device. The trailing edge of DATA STROBE produces a positive transition at the DATA ACCEPTED input that results in the clearing of BUS MSYN.

Additional examples of the use of the M796 module are presented in paragraphs 3.5, 3.7, and 3.10. The input signals to the module are listed in Table 2-8, and the output signals are listed in Table 2-9.

Table 2-8 M796 Input Signals

Signal Name	Assertion Level	No. of Signals	Loading	Operation
C1 CONTROL		1	5	Controls Bus C1
C0 CONTROL		1	1	Controls Bus C0
PIN H2				
PIN H1	L	2	1	Produces START
SSYN	H	1	2	Negates MSYN on DATO
DATA ACCEPTED	H	1	2	Negates MSYN on DATI
INIT	H	1	1	Initializes control
CLEAR TIME OUT	L	1	2	Clears TIME-OUT Flip-Flop
PIN P1				
PIN R1	L	2	1	Negative edge triggers one-shot
PIN S1	H	1	2	Positive edge triggers one-shot
PIN V2	H	1	2	Clock input to flip-flop
PIN U2	L	1	2	Clears flip-flop

Table 2-9 M796 Output Signals

Signal Name	Assertion Level	No. of Signals	Drive Capability	Operation
BUS C<1:0>	L	2	UNIBUS	Drives Unibus control line
ADRS TO BUS	H	1	8	Gates BA to address bus
ADRS TO BUS	L	1	10	
DATA TO BUS	H	1	10	Gates data to bus on DATO or DATOB
DATA TO BUS	L	1	8	
END CYCLE	H	1	10	100 ns-pulse indicating end of bus cycle
END CYCLE	L	1	8	
BUS MSYN	L	1	UNIBUS	Drives Unibus MSYN line
MYSN WAIT	H	1	10	200 ns pulse that delays assertion of MSYN
MSYN WAIT	L	1	8	
DATA WAIT	H	1	10	Allows for deskewing of DATA on DATI. Approximately 200 ns
DATA WAIT	L	1	8	
TIME OUT (1)	H	1	10	1 and 0 side of TIME-OUT Flip-Flop
TIME OUT (0)	H	1	10	
PIN M2	H	1	10	Output of one-shot
PIN T2	L	1	10	Output of one-shot
PIN V1	H	1	10	Outputs of flip-flop
PIN U1	L	1	10	

2.3 DR11-A General Device Interface

The DR11-A General Device Interface (Figure 2-24) is a three-module set that plugs into either a small peripheral slot in the processor or into one of four slots in a DD11 Small Peripheral Mounting Panel. The DR11-A provides the logic and buffer register necessary for transfers of 16-bit input and output data between the PDP-11 System and an external device.

The DR11-A contains three functional sections: a 16-bit buffer register, a 16-bit data input circuit, and a 2-channel flag and interrupt control. These functional elements are shown in Figure 2-25. Address and bit assignments are shown in Figure 2-26. The DR11-A contains three physical modules: an M105 Address Selector, an M7820 Interrupt Control and an M786 General Device Interface with two M927 cable connectors.

The 16-bit buffer register is an addressable register that may be read or loaded by instructions transmitted through the UNIBUS (see Figure 2-26). The register outputs, together with a control signal pulse (NEW DATA READY) used to indicate that the register has been loaded from the UNIBUS, are available on a printed circuit edge connector #1 which is mounted on the M786 Module. All bits in the buffer register are cleared to 0s by the occurrence of an INIT signal on the UNIBUS. These signals are logic levels of either +3V (true) or 0V (false). The NEW DATA READY signal is a pulse which has a leading edge coincident with the loading of the buffer flip-flops. The connector accepts an M927 Cable Connector, which contains solder lugs and can be used with ribbon cable, twisted pair cable, or open wire. The M927 is electrically identical to the M904 Module described in the Logic Handbook.

The interface input circuits consist of 16 bus drivers gated to the bus when the input register is read by a DATI bus sequence (see Figure 2-26). The 16 input lines are +3V if true or 0V if false. These signals are also applied to the M786 Module through an M927 Cable Connector and a second printed circuit connector #2. When a DATI sequence occurs, a pulse signal (DATA TRANSMITTED) is applied to the external device.

Two additional request lines are furnished and may be asserted (+3V) by the external device to initiate an interrupt or to generate a flag that may be tested by the program. These request signals must be maintained as levels (can not be pulses). Whether these two request lines cause an interrupt is determined by two interrupt enable flip-flops which form part of the control and status register in the option (see Figure 2-26). The request lines form two more bits of the status register, independent of the status of the enable flip-flops; thus, they may be tested by the program.

The priority level of both interrupts must be the same, with interrupt A on a higher sublevel than interrupt B. The M786 contains a priority jumper plug which is normally set at BR 5. The interrupt enable flip-flops are cleared to 0 (inhibit interrupt) by the occurence of an INIT signal on the UNIBUS, or may be set or cleared by the program. Priority may be changed by the jumper plug.

The DR11-A pin assignments are listed in Table 2-10. All inputs are one standard TTL unit load. Inputs have diode protection clamps to ground and +5V. All signals are +3V if true. All outputs are TTL levels capable of eight unit loads. The NEW DATA READY and DATA TRANSMITTED signals are positive pulses, approximately 500 ns in duration.

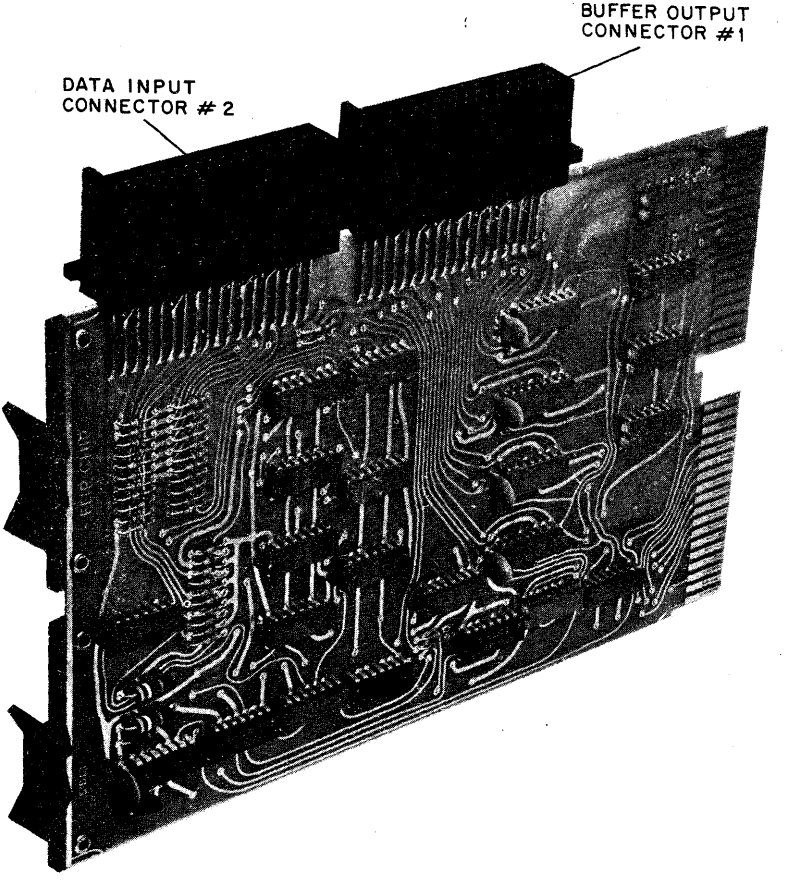


Figure 2-24 M786 Device Register Interface

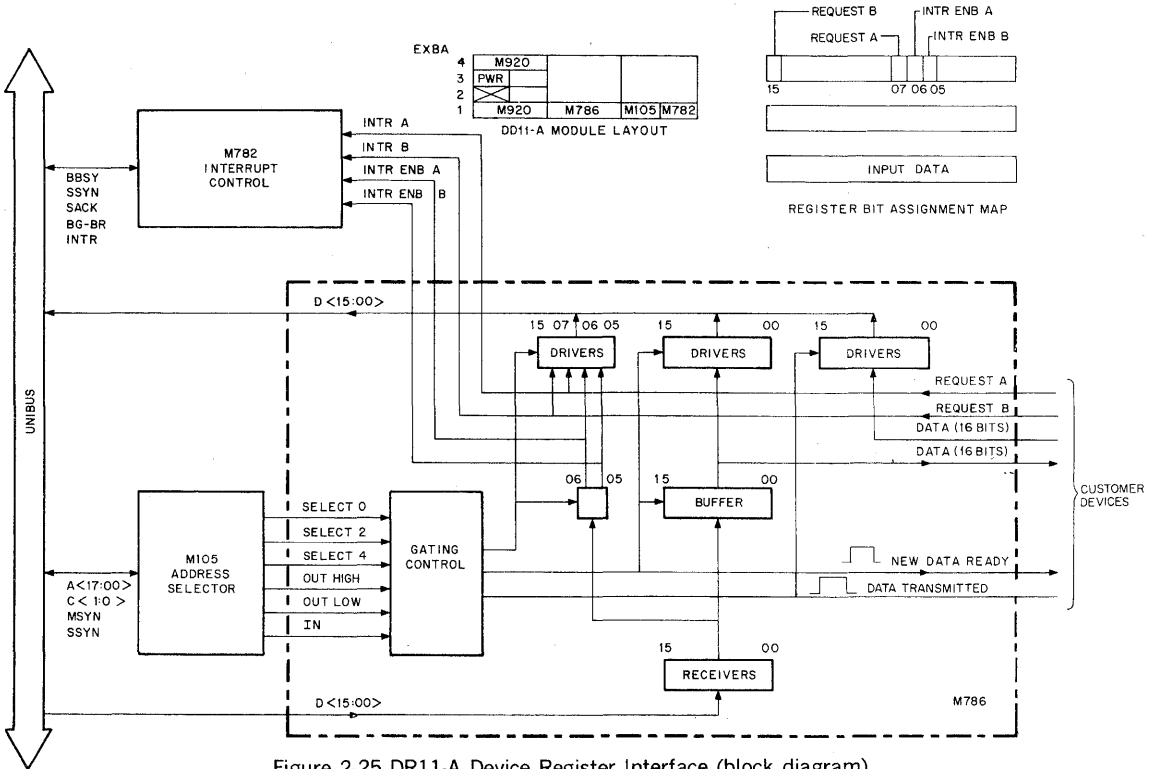


Figure 2-25 DR11-A Device Register Interface (block diagram)

Table 2-10 DR11-A Pin Assignments

Inputs			Outputs		
Signal	Connector	(Pin)	Signal	Connector	(Pin)
IN00	2	(S1)	OUT00	1	(P2)
IN01	2	(S2)	OUT01	1	(M2)
IN02	2	(P1)	OUT02	1	(S1)
IN03	2	(L1)	OUT03	1	(P1)
IN04	2	(P2)	OUT04	1	(K2)
IN05	2	(K2)	OUT05	1	(M1)
IN06	2	(M1)	OUT06	1	(S2)
IN07	2	(T2)	OUT07	1	(L1)
IN08	2	(M2)	OUT08	1	(J1)
IN09	2	(D2)	OUT09	1	(H2)
IN10	2	(E1)	OUT10	1	(E2)
IN11	2	(D1)	OUT11	1	(H1)
IN12	2	(H1)	OUT12	1	(D2)
IN13	2	(E2)	OUT13	1	(E1)
IN14	2	(B1)	OUT14	1	(D1)
IN15	2	(J1)	OUT15	1	(B1)
REQUEST A	1	(T2)	NEW DATA RDY	1	(V2*)
REQUEST B	2	(H2)	DATA TRANSMITTED	2	(V2*)

*Pulse signals, approximately 500ns wide.

Figure 2-27 shows the physical layout of the M786 and M927 modules. An application of the DR11-A Option is discussed in Chapter 3.

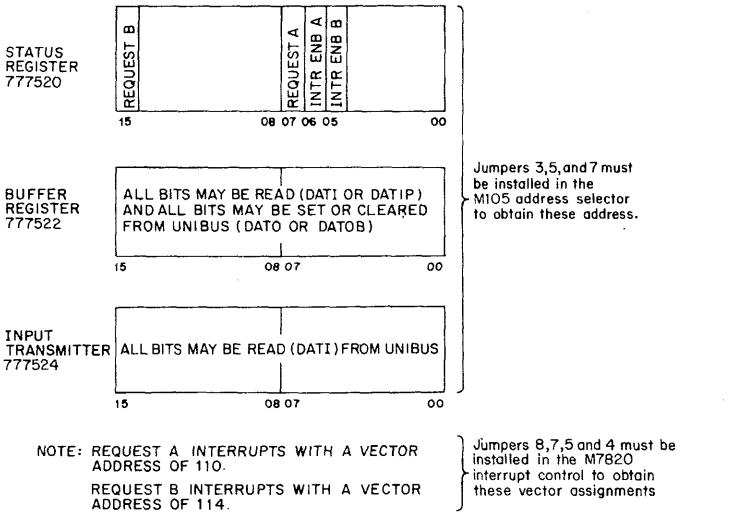


Figure 2-26 DR11-A Address and Bit Assignments

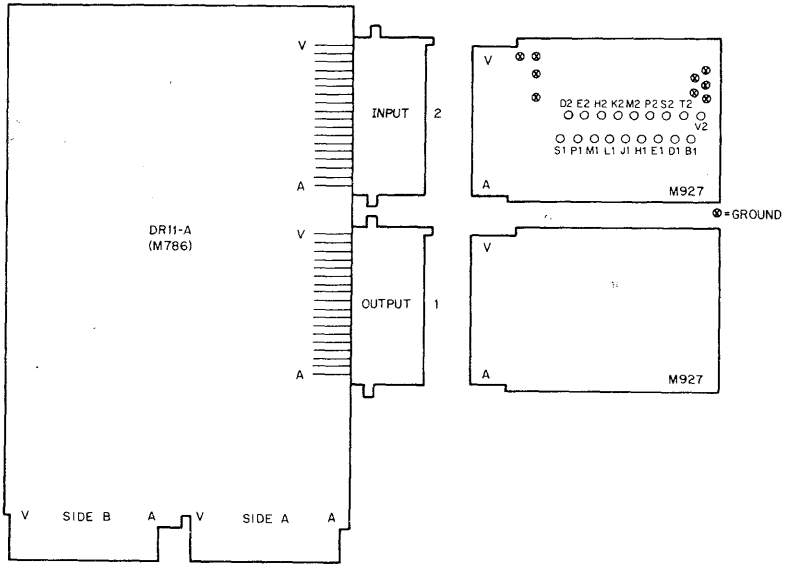


Figure 2-27 DR-11A Physical Layout

2.4 PDP-11 INTERFACE HARDWARE

The basic design of the PDP-11 System permits highly flexible and easily varied system configurations because of the modular construction. These advantages are available to the user when designing and building custom interface equipment.

The basic building block of the PDP-11 System is the system unit. The system unit is a die-cast zinc frame. Three 288-pin connector blocks are fastened to this frame and each block contains slots for mounting eighteen single-size Flip-Chip Modules. Peripheral devices and controllers may be made up from one or more of these assemblies. Up to six such system units can be mounted in a BA11 Mounting Box. In addition to space for the system units, the mounting box has space for an H720 Power Supply.

The UNIBUS is interconnected from system unit to system unit within a single mounting box by M920 UNIBUS Connectors. A BC11-A Cable Assembly carries the UNIBUS between mounting boxes.

The basic PDP-11/20 or PDP-11/15 System (see Figure 2-28) occupies four of the six positions within the mounting box. Three of these are system units for the processor, including space for two small peripheral controllers, and one is a system unit for the MM11 Core Memory. System units mounted in the BA11 Mounting Box can accept either the extended-length Flip-Chip modules (8.5 inches long) or standard-length Flip-Chip modules (5 inches long) if equipped with H850 Module Handle Extenders.

Users who prefer to mount the interface equipment directly into a rack can use H911 Mounting Panels and the BC11A Cable Assembly to extend the UNIBUS. Information on the H911 Panels as well as the M-Series Logic Modules is provided in the DEC Logic Handbook.

The following paragraphs provide a detailed description of available hardware specifically designed for the PDP-11 System as an aid in interfacing and building custom equipment.

2.4.1 BB11 Blank Mounting Panel

The BB11 Blank Mounting Panel (see Figure 2-29) is a prewired system unit designed for general interfacing. The unit contains three 288-pin blocks assembled end-to-end in a casting which can be mounted in either the basic PDP-11 Mounting Box or the extension box. Bus and power connectors, described below, use only 6 of the module slots, thereby leaving 18 slots available for customer use.

The BB11 is wired to accept the UNIBUS in slots A1 and B1 as shown in Figure 2-30. This connection can be made with an M920 UNIBUS Connector or a BC11-A UNIBUS Cable Assembly. All bus signals, including grant signals, are wired directly to corresponding pins in slots A4 and B4. From this point, the UNIBUS can be continued to the next unit by using an M920 or BC11-A. If the BB11 is the last unit on the bus, slot A4-B4 accepts the M930 Bus Terminator Module. Standard bus pin names are listed in Appendix C.

The bus grant signals are wired through the BB11. These grant signal wires must be removed and replaced with wires to and from the user's control circuits for the grant levels used by the customer-supplied device.

Slot A3 accepts the G772 Power Connector (furnished as part of the BA11 Mounting Box). Power of +5V is distributed to all A2 pins; −15V is distributed to all B2 pins except in slots A1, B1, A4, and B4; and ground is maintained through the frame and power connector on pins C2 and T1 of all slots.

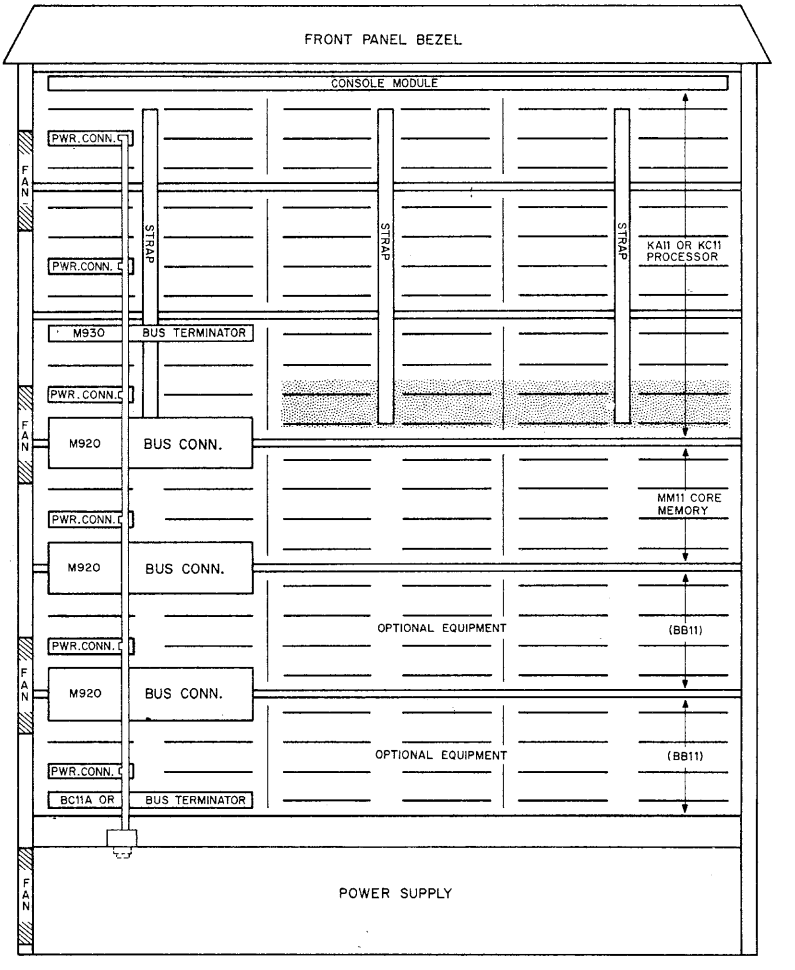


Figure 2-28 Basic PDP-11 Layout with Two BB11 Panels (from module side)

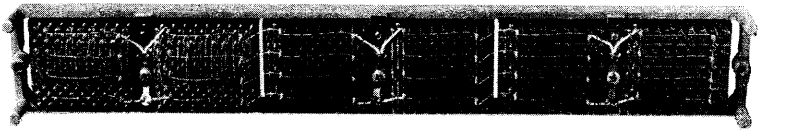


Figure 2-29 BB11 System Unit

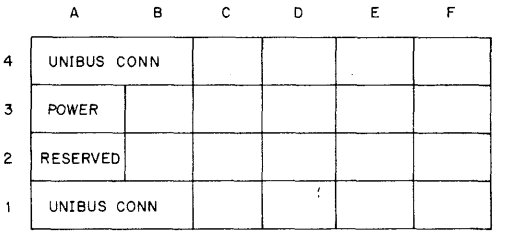


Figure 2-30 BB11 Module Layout

2.4.2 DD11-A Peripheral Mounting Panel

Peripherals may be divided into large and small categories based on the size of the associated interface logic. If the interface logic (including the M105 Address Selector and the M782 Interrupt Control) can fit into four module slots, then the associated device is referred to as a small peripheral. The DD11-A peripheral mounting panel is a pre-wired system unit designed for mounting up to four small peripheral interfaces. The physical construction of the DD11-A is similar to the BB11 blank mounting panel.

Use of the DD11-A requires specialized logic cards for the actual interface, since the pin assignments are fixed for the various control and data signals. Examples of such interfaces are the DR11-A General Interface (M786 module), LP11 Printer Control (M793 module), CR11 Card Reader (M829 module), M792 Diode Memory, and the KL11 Teletype Control (M780 module). Customers may design interfaces to go into a DD11-A by using the W943 module which allows wire-wrapping of the integrated circuit interconnections.

Figure 2-31 illustrates module allocation within a DD11-A unit. Slot A2 must be empty because of power cable overhang; slots B2 and B3 are unused. The DD11-A is wired to permit the installation of four M7820 modules in column F, four M105 modules in column E, and four double-height device interface modules in columns C and D. The unidirectional grant lines are wired to column D, and each device interface module must include jumper arrangements to allow selection of the device priority level at the time of installation. Only BR<7:4> levels are wired to this column; devices mounted in a DD11-A unit cannot be assigned to the NPR priority level without rewiring the panel. An additional constraint imposed on the interface is that each device may be on only one request level, since both interrupts available through one M7820 module are wired in series and must be at the same priority level.

If the device requires interface logic that occupies more than one full row of space in the DD11-A, columns C and D of the second row can be used by using wiring provided between rows 1 and 2 and rows 3 and 4. If this is done, it is no longer necessary to add another M105 and M782 module to slots E and F of the second row.

Additional considerations that must be noted when using a DD11-A as well as specific pin number information is covered in subsequent paragraphs.

2.4.2.1 UNIBUS—The Unibus enters through slots A1-B1 of the DD11-A. This connection can be made with either an M920 UNIBUS connector or a BC11-A UNIBUS cable. All bus signals (except grants) are wired directly to corresponding pins in slots A4-B4. Connection can be made with either an M920 connector or BC11-A cable to continue the UNIBUS to the next unit. If the DD11-A is the last unit on the bus, an M930 Bus Terminator must be placed in slots A4-B4.

2.4.2.2 Power—The G772 Power Connector plugs into slot A3. This connector distributes +5V power to all A2 pins and -15V power to all B2 pins except in slots A1, B1, A4, and B4. Ground is maintained through the frame and power connector on pins C2 and T1 of all slots.

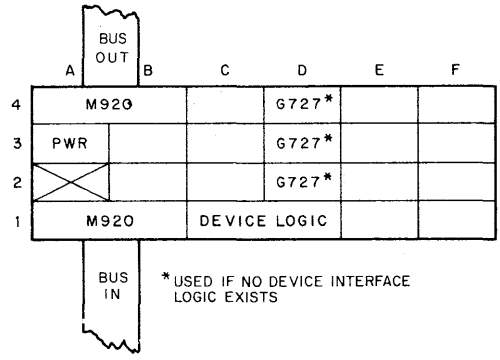


Figure 2-31 DD11-A Module Layout

Note that a G727 Grant Continuity module must always be installed in column D if there is no interface logic in that row. Figure 2-32 shows the wiring assignments that must be adhered to when using the DD11-A.

2.4.2.3 Extended Usage—Additional wiring provides 10 signal lines between slots C1-D1 and C2-D2 as well as between slots C3-D3 and C4-D4. This permits use of multiple board device controls. Thus, if device logic can be divided into two sections with less than 10 interconnections between sections, then one section can be mounted in slots C1-D1 and the other section in slots C2-D2.

NOTE

Interconnections can be made only between rows 1 and 2 or between rows 3 and 4. No connections can be made between 1 and 3, for example.

Other sections of divided logic can also be placed into slots E and F with the interconnections provided by the normal M105 and M7820 module- to-device control signals.

CAUTION

When designing special logic, it is necessary to prevent interference with bus signals prewired to the pins of a particular slot.

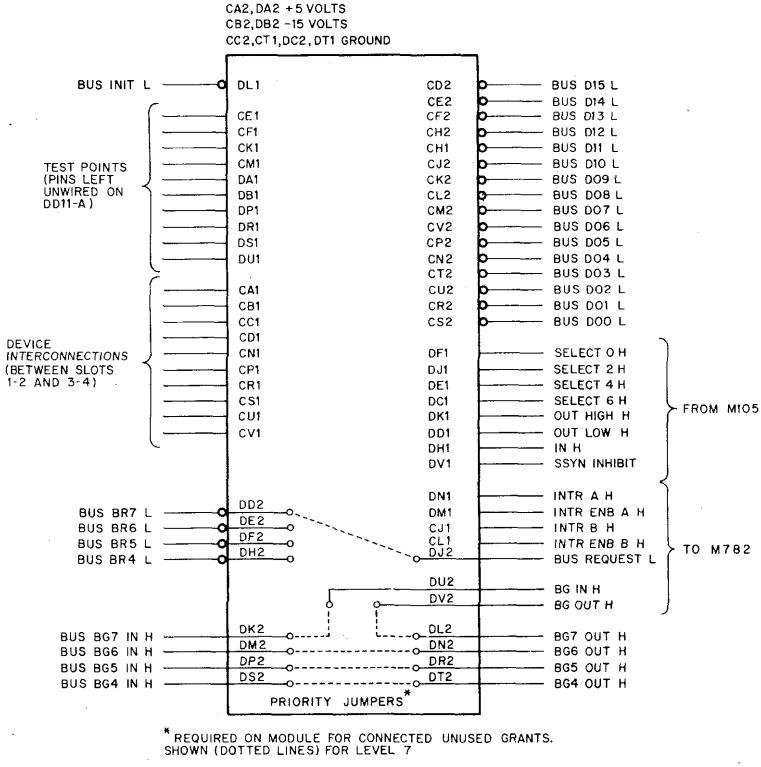


Figure 2-32 Device Control as Wired in the DD11-A

2.4.2.4 Grant Continuity—The device control module mounted in slots C1-D1 receives the bus grant signal from the UNIBUS. As a function of its interrupt priority level, this device control must switch the grant signal into its interrupt control (BG IN). After passing through both stages of the interrupt control, the signal (BG OUT) must be returned to the grant chain and passed on to the next device control (mounted in slots C2-D2). In addition, the device control must maintain the continuity of unused grant signals. The BG OUT signals of C1-D1 are wired to the BG IN lines of the next device control. This grant chain must be continued through each device control until the BG OUT signals of the last device control are wired to the outgoing UNIBUS in slots A4-B4.

Whenever slot D is not used by a device control, a G727 Grant Continuity module must be inserted in this slot. This module provides jumpers between pins K2 and L2, M2 and N2, P2 and R2, and S2 and T2. Three G727 modules and one M920 module are provided with the DD11-A unit.

2.4.2.5 External Device Cables—An edge connector mounted on the device control module permits connection to external devices. An H807 36-pin module socket may be mounted on the device control module and an M927 cable connector or M925 Flexprint ribbon connector may be used. The M927 is used for coaxial cables or twisted pairs and is electrically equivalent to the M904 connector; however, the cable is mounted at the edge of the module card rather than at the end. The M925 is similar to M903 and is used for Flexprint connectors.

2.4.3 BA11 Mounting Boxes

The BA11 Mounting Box (see Figure 2-33) is designed to house the system units that make up a PDP-11 System. The box also includes space for mounting the H720 System Power Supply. The mounting box contains fans for forced air cooling, an insulated top cover (not shown) to prevent debris from falling into the wire-wrap pins (this is necessary because the system units are mounted with the pins up and the modules down), and a foam-lined bottom cover, which serves as a module retainer and minimizes module vibration. The bottom cover serves as part of the air plenum to ensure adequate cooling.

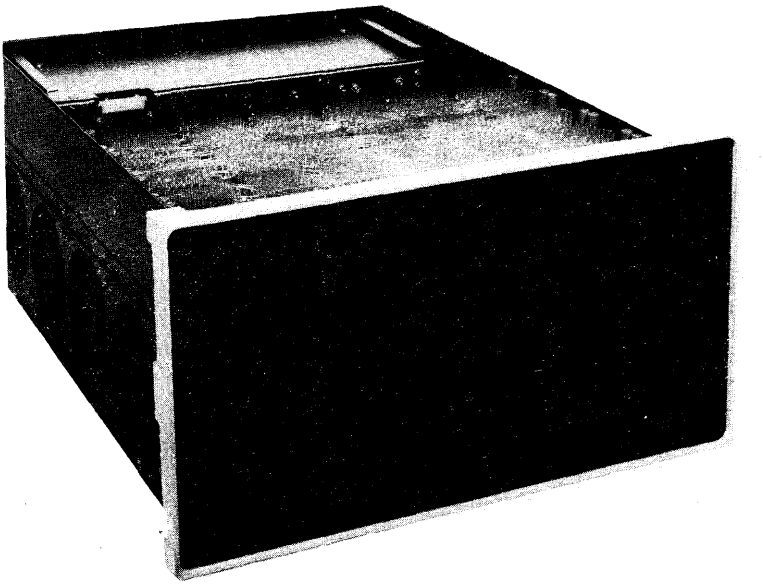


Figure 2-30 BA11 Mounting Box (with wired System Units and H720 Power Supply installed)

The mounting box is fabricated from zinc-plated steel to resist corrosion. The four available models are listed in Table 2-11.

Table 2-11 BA11 Mounting Box Models

Model No.	Description
BA11-CS	Basic box*, with tilt-slides for rack mounting
BA11-CC	Basic Box, with table-top decorative cabinet
BA11-ES	Extension box**, with tilt-slides
BA11-EC	Extension box, with table-top cabinet

*The basic box includes proper bezel for the console and a key-operated power switch.

**The extension box includes blank front with decorative bezel and does not include a power switch.

2.4.4 H720 Power Supply

The H720 Power Supply is specifically designed to provide power for PDP-11 Systems. It provides +5V and -15V regulated power as well as additional power for console functions. The +5V portion is protected by overvoltage circuits and both portions of the supply feature dynamic current limiting. The basic regulating element is a high efficiency switching regulator that keeps voltages within a ±3 percent tolerance. In addition to providing power, the H720 Supply generates three other signals: a line frequency signal that approximates a squarewave referred to as LTC (line time clock), and the AC LO and DC LO signals previously described in Paragraph 1.1.3. The low voltage detection circuits are interlocked so that -15V is not established until +5V is established. If the +5V fails, the -15V section is shorted to ground to prevent damage to system logic circuits. The power supply outputs are listed in Table 2-12.

There are two H720 Power Supply Models. The H720-E is designed for use with an input of 120V, ± 10 percent. The H720F is designed for an input of 230V, ± 10 percent. In addition, the H720-F has taps for lower voltages of 215 and 200, ± 10 percent. Both models are designed to operate within a 47- to 63-Hz frequency range. Alternate versions of the H720 (Models C and D) also provide local power control for multibox systems, but have identical dc characteristics.

Table 2-12 H720 Power Supply Outputs

Output	Regulation	Capacity	Remarks
+5V	±5%	22A	
-15V	±3%	10A	
+8V, rms	±15%	1.5A	Full-wave, unfiltered
-24V	±20%	1.0A	Unregulated, filtered
LTC L	0 to 5V		Line time clock
AC LO L	Logic level		ac line low
DC LO L	Logic level		dc line low

PART II
Chapter 3

Interface Examples

Examples of interface designs in Paragraphs 3.1 to 3.9 use the techniques and equipment described in previous chapters. To draw attention to the design features of each interface type, a series of related examples is presented. The first example is a simple basic interface. Each additional example implements several features by adding logic circuits to the previous example. Thus, the first example is the simplest possible read/write interface. This circuit is then used with additional logic to form a program-controlled interface, which in turn is used with additional circuits to form an interrupt-serviced interface, until finally, the circuit is used with additional circuits to form a direct-memory-access interface.

The examples cover input and output transfers and also illustrate techniques for combining the two functions into one interface. Each example includes a description of the operation and logic of the interface, a typical implementation, and programming methods that might be used to operate a device with the interface.

3.1 BASIC INTERFACE

The simplest possible interface, a basic read/write interface, is used when data is transferred to and from the register during bus operations. Applications of read/write, read-only, and write-only registers are discussed in Paragraph 1.6. This particular read/write interface consists of only a storage register and bus gating circuits. The register may be used either as a data register or may be used to drive an output device, such as a set of indicator lights.

3.1.1 Interface Operation

When the basic read/write is used, data transfers are under control of the program and the register is assigned an address on the UNIBUS. During execution of an instruction that addresses the interface, the processor conducts a bus data transfer with the interface register, which responds as a slave. Since a 16-bit register is used, it may be addressed as either a one word register or as two byte (8-bit) registers.

As shown in Figure 3-1, the basic interface uses an M105 Address Selector module to decode the UNIBUS address lines and to control the clocking of information into the register and the gating of output information from the register to the bus data lines. The register is interfaced to the bus input data lines by ungated receivers, and the inputs are clocked into the register by a strobing signal derived from the M105 Address Selector. The register outputs are gated through the drivers by the GATE REGISTER TO BUS signal. This output gating is necessary to prevent the register from affecting the UNIBUS data lines when the interface is not participating in a bus data transfer operation.

3.1.2 Data Transfer Operation

The read/write interface can participate in both DATI (or DATIP) and DATO (or DATOB) transfers. Whenever the processor conducts a DATO transfer to the bus

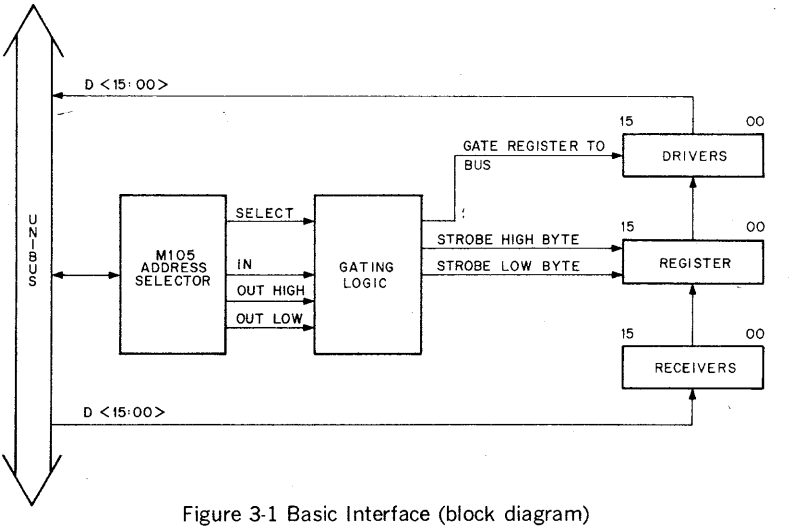


Figure 3-1 Basic Interface (block diagram)

address assigned to the read/write register, the data is applied through the bus receivers to the register input. At this time, both the OUT HIGH H and OUT LOW H signals are produced by the M105 Address Selector (see Figure 2-11). When MSYN is asserted by the processor, the decoded address causes the M105 to produce a SELECT 0 signal which is gated by the two OUT H signals to clock data into the register. The UNIBUS timing guarantees that at the slave device data is valid 75 ns prior to assertion of MSYN (refer to Paragraph 1.5). Therefore, the inputs have settled before the positive-going transition of the clock signal occurs.

A DATOB transfer functions in a similar manner, except that only one byte of the register is clocked. If address line A00 is 0, the M105 Module asserts OUT LOW H but not OUT HIGH H. If A00 is 1, then only OUT HIGH H is asserted. In either case, data is only strobed into the appropriate byte portion of the register.

When a DATI transfer occurs, the processor addresses the interface and asserts MSYN. In addition, the M105 Module asserts the same SELECT 0 signal. However, in this case, the SELECT 0 is gated by the IN rather than the OUT signals. The IN signal is generated by the state of the bus C lines. Gating of the SELECT 0 signal by the IN signal produces a GATE DATA TO BUS signal that gates the output data from the register to the UNIBUS. The M105 Module generates SSYN to indicate that data is ready on the output bus data lines.

CAUTION

In the KA11 and KC11 processors, the destination major state of most instructions consists of DATIP, DATO bus cycles unless the register address mode is used. When designing interfaces, make certain that the design is compatible with the instruction bus cycles.

3.1.3 Circuit Implementation

Figure 3-2 illustrates a possible method of implementing the circuits in the basic read/write interface. The types and quantities of modules used are: the M105 Address Selector Module (one); the M785 Bus Transceiver Module (two); the M206 General-Purpose Flip-Flop Module (three); and the M617 4-Input Power NAND Gate Module (one). The M105 and M785 Modules are described in Chapter 2 and the M206 and M617 Modules are described in the DIGITAL LOGIC HANDBOOK. The modules are interconnected and may be mounted in a BB11 System Unit as shown in the insert on Figure 3-2.

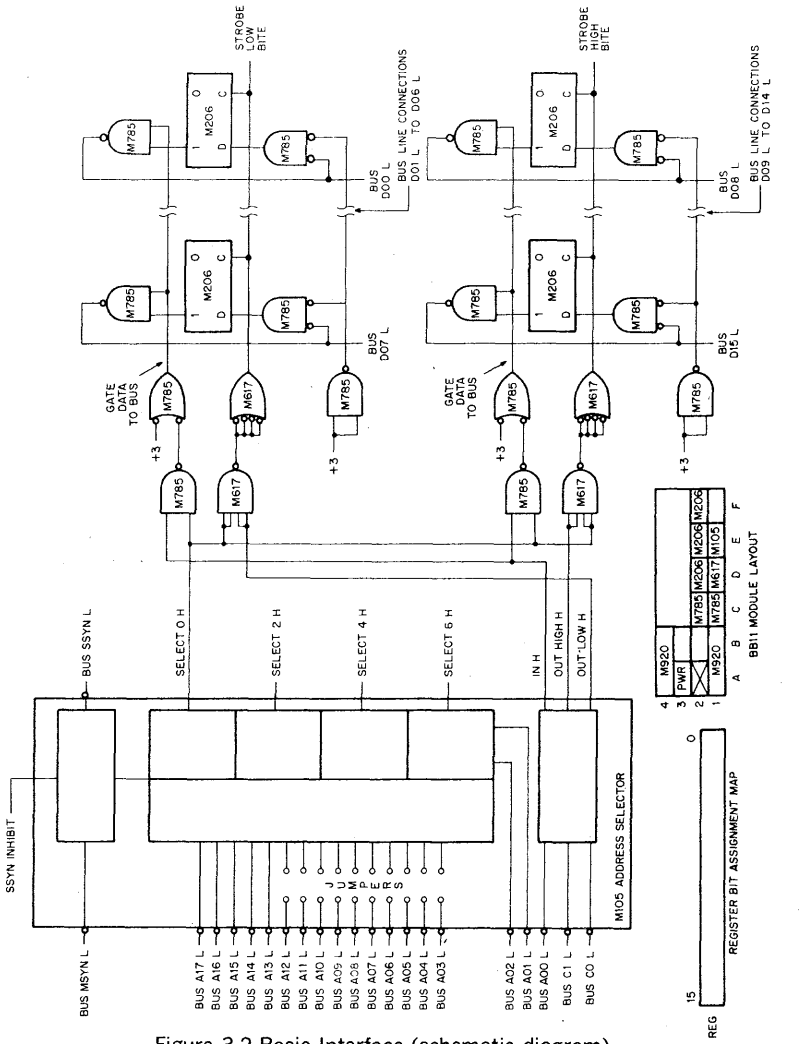


Figure 3-2 Basic Interface (schematic diagram)

Input data flows from the UNIBUS, through the input gates on the M785 Modules, to the data inputs of the M206 Flip-Flops comprising the register. The gating provided on the M785 Receivers is not used, and all gates are wired to continuously receive data. Data stored in the register is protected from these changing inputs by the requirement for a clocking signal to load data into the register.

The output data from the register is gated to the bus data lines through the driver sections of the M785 Modules. The M785 Modules are used in this example because the M785 provides the exact combination of input and output gates needed for an 8-bit read/write register. When the number of receivers differs from the number of drivers required in a specific interface, combinations of M783 Bus Driver Modules and M784 Bus Receiver Modules may be used. This example is devoted to illustrating the use and interconnection of bus drivers and receivers rather than indicating the specific modules used in implementation.

3.1.4 Programming the Interface

All data transfers in the basic read/write interface are under processor control, and all memory reference instructions may directly address the interface. If the mnemonic REG is assigned to the register address, the instruction MOV REG, R4 reads the data stored in the register (a DATI operation) and places the data in general register 4 of the processor. The instruction MOV R4, REG reverses the data flow so that the data in general register 4 is placed in the interface register (a DATIP, DATO operation). Any instruction that can access a bus address can conduct data transfers with the interface register. Therefore, the contents of the register may be incremented by an INC REG instruction or summed with an arbitrary value by an ADD VALUE, REG instruction.

3.2 PROGRAMMED DEVICE INTERFACE

A circuit similar to the one in the preceding example is used as the basis for the program controlled interface to an analog-to-digital converter (ADC). It is beyond the scope of this discussion to describe the logic or internal operation of the ADC. The ADC is simply a representative example of many possible external devices that may be interfaced with a design similar to the one discussed in this section. The ADC input and output signals, however, are covered in the following paragraph because of the requirements they place on the interface.

3.2.1 Analog-to-Digital Converter

The analog-to-digital converter used in this example consists of a multiplexer and converter, (See Figure 3-3). The multiplexer selects one of 64 analog inputs and applies it to the converter, which produces the digital equivalent of the analog input.

The interface must provide seven input control signals to the ADC. One input is the start conversion signal, which is a positive transition that causes the ADC to begin the conversion process. The other six control signals are applied to multiplexer address lines so the ADMUX register can be used to select one of the 64 analog inputs.

The interface receives 11 output signals from the ADC. One of these is the conversion complete signal. When the conversion process starts, the conversion complete signal becomes 0V and remains at that level until the conversion is finished. At that time, the signal becomes +3V to indicate that the digital output reflects the analog input (the conversion is complete).

The remaining ten output lines represent the digital equivalent to the analog input. A zero on any line is indicated by 0V and a one is indicated by +3V.

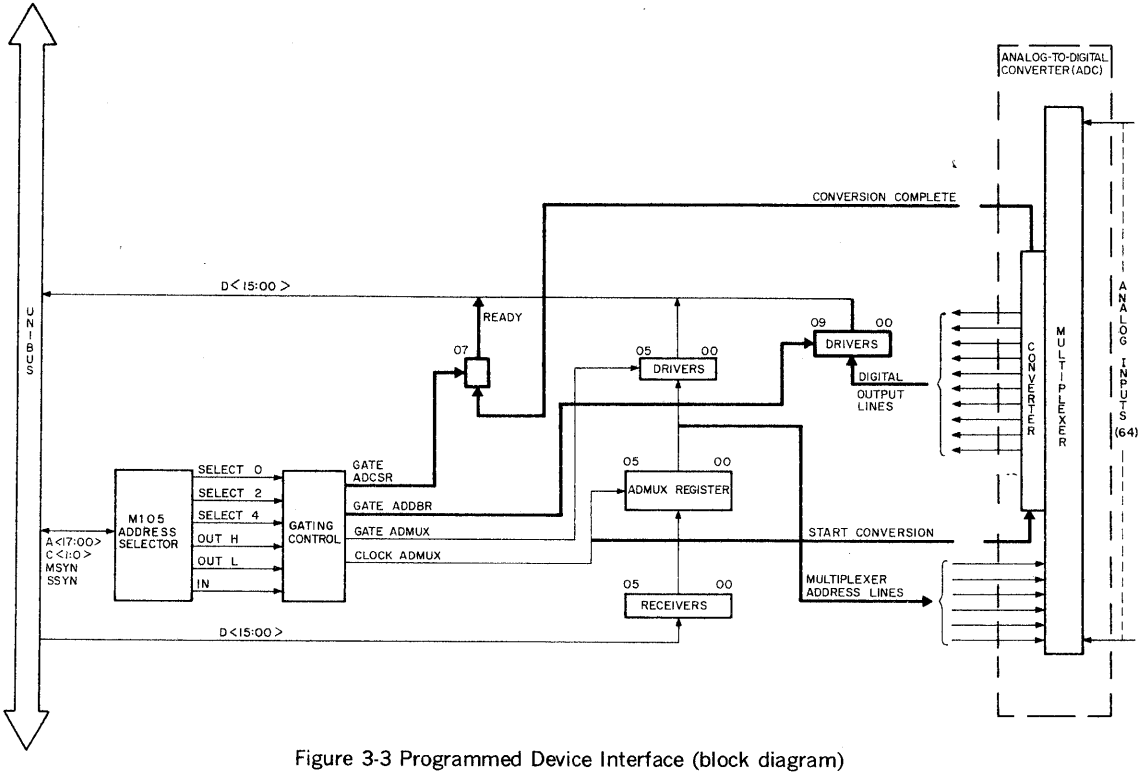


Figure 3-3 Programmed Device Interface (block diagram)

Signal levels used in the interface are standard DEC levels. Both these levels and the signal levels on the UNIBUS are discussed in Paragraph 2.1.2.

3.2.2 Interface Description

The program controlled interface allows the program to select a specified analog input for application to the ADC and then causes the resultant digitized output and conversion complete signal to be placed on the UNIBUS data lines to transfer data into the bus master.

The heavy lines in Figure 3-3 indicate logic added to the interface of the previous example. The interface functionally operates with three bus addresses. One address is assigned for the multiplexer (ADMUX) register, which is similar in design to the register in the previous interface example. The second address is for the converted digital output (ADDBR) of a read-only register, and the third address is assigned to a 1-bit control and status register (ADCSR).

The M105 Module decodes the bus address to produce one of three select signals depending on which register is being accessed. The three select signals are gated by IN H and OUT LOW H to produce the four signals (GATE ADCSR, GATE ADDBR, GATE ADMUX and CLOCK ADMUX) shown in Figure 3-3. Only the ADMUX register accepts inputs from the UNIBUS through the receivers. However, the outputs of all three registers are gated to the bus through separate sets of bus drivers.

Connections between the ADC and interface may be made by a cable connector such as the M908 Module described in the Digital Logic Handbook.

3.2.3 Transfer Operations

The program controlled interface participates in bus data transfers in substantially the same manner as the basic interface described in Paragraph 3.1. Each of the three interface registers can be read during a DATI operation. In addition, the multiplexer (ADMUX) register can be loaded by a DATO operation. Although only the multiplexer register accepts data during a DATO, the other two registers respond when a DATO cycle occurs. If any of the three registers is addressed during a DATO, the M105 Module produces SSYN to complete the bus operation. This is necessary to operate the interface with the processor because the destination operand of all instructions that reference data (except TST, CMP, and BIT) is transferred by a DATIP, DATO sequence of bus operations. If the interface does not respond to the DATO operation, the processor cannot continue with the program.

3.2.4 Circuit Implementation

Figure 3-4 includes a map of bit assignments for the three registers and a layout for mounting the logic modules in a BB11 System Unit. Neither the M105 Address Selector Module nor the ADC is shown on the figure, but the signals generated by these units are indicated. The connections to the UNIBUS can be implemented with one M785 UNIBUS Transceiver Module for the multiplexer register and one M783 UNIBUS Transmitter Module for the data and control registers. Separate gating must be supplied to use one of the four individual bus drivers on the M783 for a ready bit. The CONVERSION COMPLETE signal is renamed to READY after it passes through the bus transmitter.

3.2.5 Programming the Interface

The START CONVERSION signal, which begins the device cycle, is generated in this interface by the CLOCK ADMUX signal, which loads the multiplexer register. In normal operation, the processor loads the multiplexer register; this action

starts the ADC; tests the READY (CONVERSION COMPLETE) bit until the bit is set; and then transfers the data from the digital output line of the ADC to the processor. A possible sequence of instructions to perform this task is given below. This program selects an input, waits for the device to complete the conversion, and then transfers the result to register 4.

```
        MOV     INPUT,ADMUX         ;SELECT ANALOG INPUT
READY:  TSTB    ADCSR               ;CHECK FOR CONVERSION COMPLETE
        BPL     READY               ;NO,TEST AGAIN
        MOV     ADDBR,R4            ;YES,OBTAIN DATA

INPUT IS A LOCATION CONTAINING THE NUMBER OF THE DESIRED ANALOG
INPUT LINE.

A SUBROUTINE TO EXAMINE A SERIES OF INPUTS MIGHT BE WRITTEN AS FOLLOWS:

MUXSCN: MOV     BUFADR,R4           ;INITIALIZE DATA POINTER
        CLR     ADMUX               ;SELECT INPUT LINE ZERO
LOOP:   TSTB    ADCSR               ;CHECK FOR CONVERSION COMPLETE
        BPL     LOOP                ;NO,TEST AGAIN
        MOV     ADDBR,(R4)+         ;YES,PLACE DATA IN BUFFER
        CMP     ADMUX,#77           ;LAST LINE?
        BEQ     DONE                ;YES,GO TO DONE
        INC     ADMUX               ;NO,GO TO NEXT INPUT
        BR      LOOP                ;GO TO LOOP
DONE:   RTS     R7                  ;EXIT FROM SUBROUTINE

WHERE:  BUFADR IS A LOCATION IN CORE CONTAINING THE ADDRESS OF THE
               FIRST WORD ON A 64-WORD BUFFER
        ADCSR IS THE INTERFACE STATUS REGISTER
        ADMUX IS THE MULTIPLEXER REGISTER
        ADDBR IS THE DATA REGISTER
```

This subroutine is called by the instruction: JSR R7, MUXSCN. The subroutine initializes general register 4 as a pointer to the buffer; initializes the multiplexer register to zero; and sequentially reads the 64 inputs into the corresponding buffer location. When each input has been read once, control returns to the calling program with the contents of general register 4 as the address of the word after the last word of the buffer.

Since loading the multiplexer register starts operation of the device cycle, ADMUX should not be accessed as a destination operand except by a TST, BIT, or CMP instruction. In addition, the INC ADMUX instruction should follow the CMP instruction. This avoids initiating unwanted device operation and allows the subroutine to be immediately recalled.

3.3 INTERRUPT SERVICED INTERFACE

The interface to an analog-to-digital converter would be more versatile if it included an interrupt capability. An interrupt serviced interface with this capability can be formed simply by adding an M7820 Interrupt Control Module and one bit to one of the registers in the programmed device interface described in Paragraph 3.2.

The interrupt serviced interface allows the processor to concurrently execute instructions of another program while the analog-to-digital converter (ADC) performs a cycle of operation. The processor responds to a READY (CONVERSION COMPLETE) signal from the ADC by interacting with the device and analyzing the

data after it has been collected. This interface eliminates requiring the processor to spend time testing for a ready signal, such as in the case of the programmed device interface.

Whenever a device interface is required, the designer must compare the cost of additional interrupt hardware with the device requirements in terms of transfer speed, frequency of transfers, and amount of use, to determine whether a programmed device interface or interrupt serviced interface is more economical.

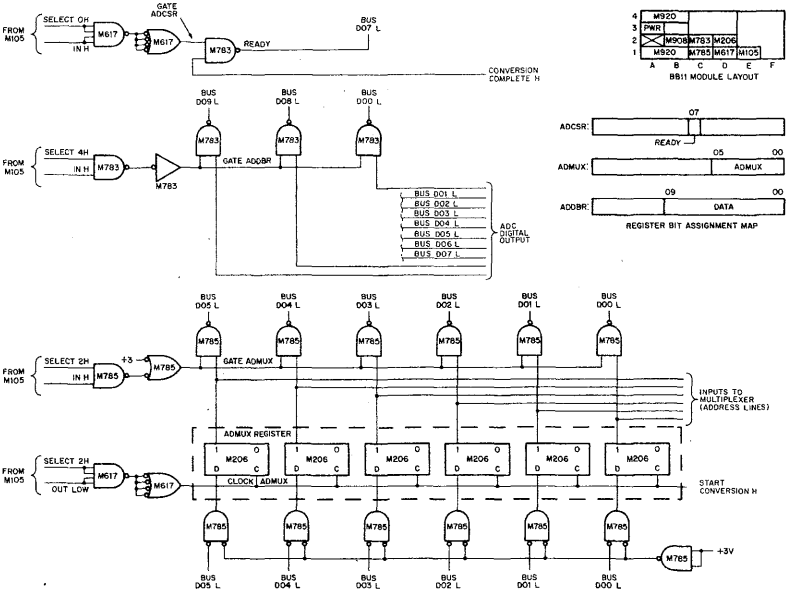


Figure 3-4 Programmed Device Interface (schematic diagram)

3.3.1 Interface Description

Figure 3-5 is a block diagram of the interrupt serviced interface which consists of the programmed device interface with the addition of an M7820 Interrupt Control Module, one flip-flop, and one bus driver. This interface can operate either in the same manner as the interface described in Paragraph 3.2 or in an interrupt mode. The additional flip-flop is used to enable or disable interrupt operations. If the flip-flop (which is bit 6 of the control status register) is set by the program, the CONVERSION COMPLETE signal from the ADC causes the M7820 Interrupt Control Module to initiate an interrupt. The interrupt operation is described in Paragraph 1.3.2.

3.3.2 DR11-A Implementation

A convenient method of implementing an interrupt serviced interface is to use an M786 General Interface Module to make a DR11-A 16-Bit General Interface. Figure 3-6, a layout of the modules mounted in a DD11-A System Unit, shows the savings in space and interconnections. The DD11-A System Unit is prewired to accept four DEC small peripheral interfaces; e.g., DR11-A. A discussion of the DR11-A, including specifications, is presented in Paragraph 2.2.6.

Figure 3-7 is similar to Figure 3-5 because the DR11-A logic is used in the same manner and with the same programs as any other logic used to implement an interrupt serviced interface. The M786 Module portion of the DR11-A provides cable connectors; therefore, no additional wiring or connectors are required.

Connections between the ADC and the M786 Module are made as follows:

CONNECTOR	DR11-A	ADC
1	OUT (06:00)	Multiplexer inputs
	NEW DATA READY	Start conversion
2	IN (09:00)	Digital outputs
	REQUEST A	Conversion complete

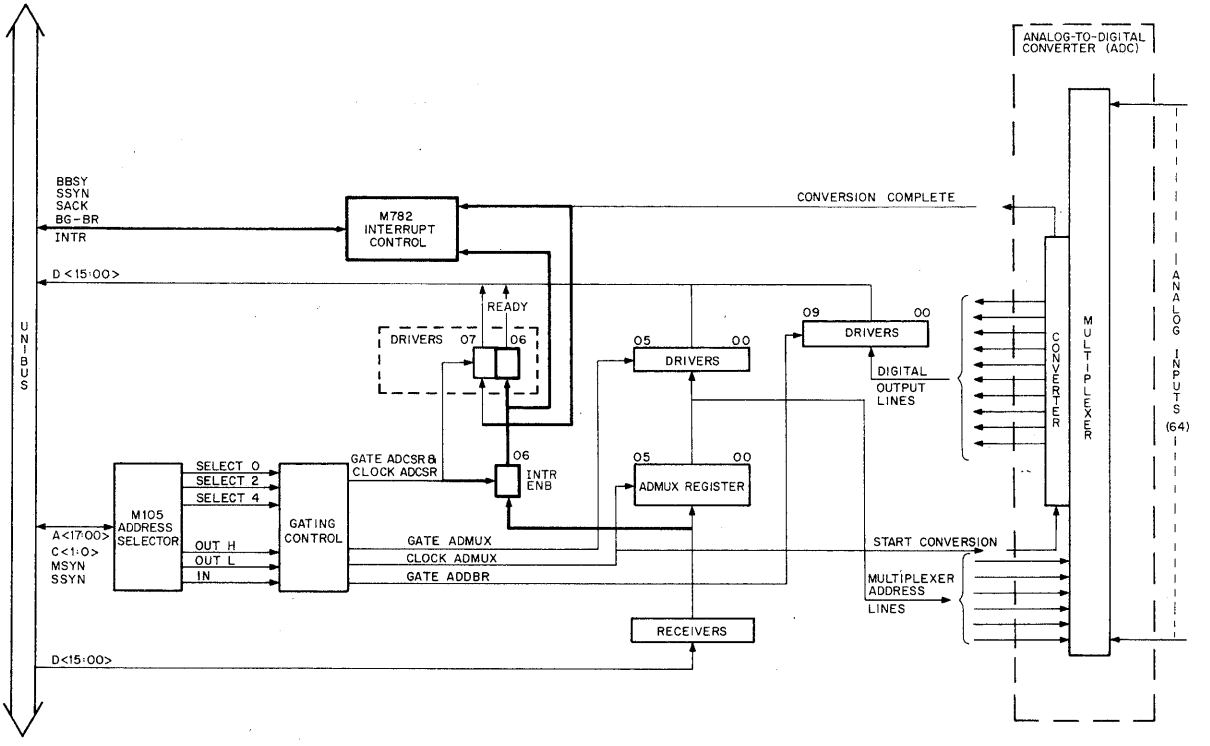


Figure 3-5 Interrupt Serviced Interface (block diagram)

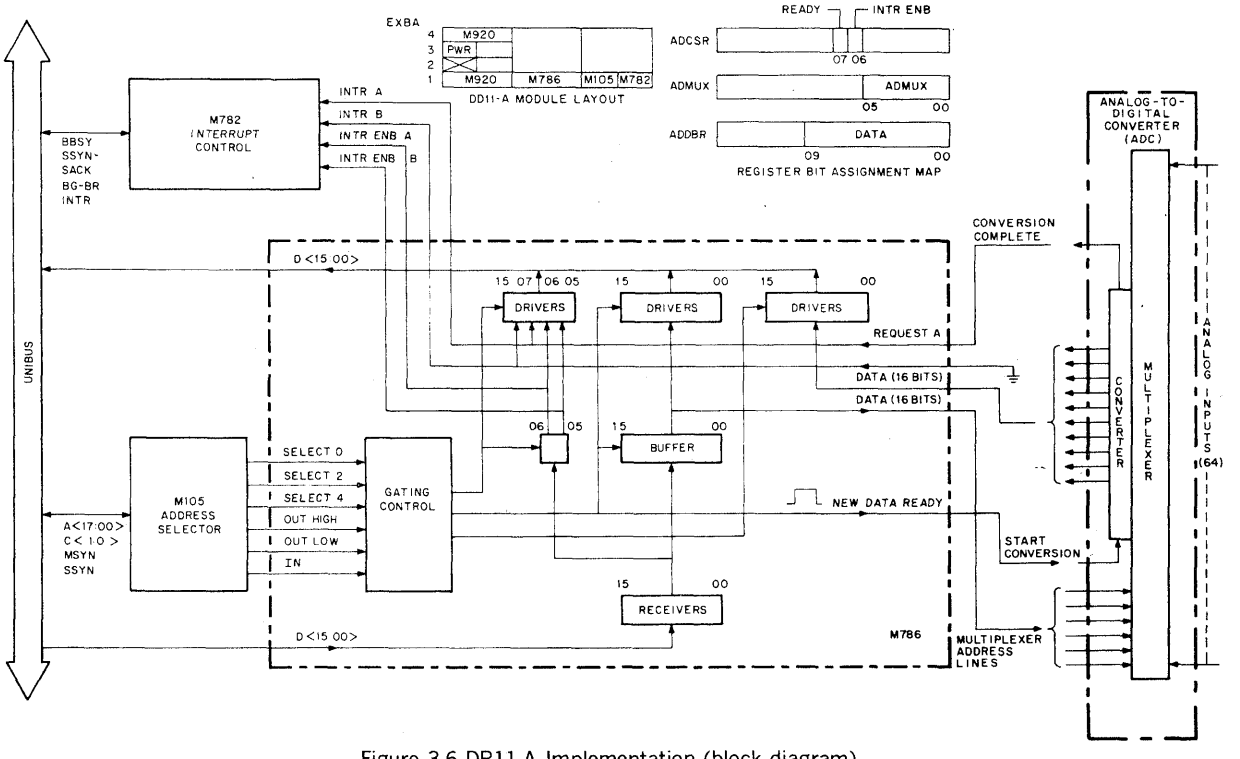


Figure 3-6 DR11-A Implementation (block diagram)

3.3.3 Interface Programming

The following program is a typical interrupt service routine that collects data from the ADC and enters an evaluation routine after the final conversion cycle.

```
ADCVEC:   ADCSER                      ;SET UP ADC VECTOR AREA
          240                         ;STATUS INCLUDES PRIORITY LEVEL 5
            .
            .
            .                         ;MAIN PROGRAM FOLLOWS
BEGIN:    MOV BUFSTRT,BUFADR          ;INITIALIZE BUFFER POINTER
          CLR ADMUX                   ;START MULTIPLEXER AT CHANNEL 0
          MOV #100,ADCSR              ;ENABLE INTERRUPT
            .
            .
ADCSER:   MOV ADDBR,@BUFADR           ;COLLECT DATA
          CMP BUFADR,BUFSTRT+174      ;LAST ONE?
          BEQ DONE                    ;YES,GO TO DONE
          ADD #2,BUFADR               ;NO,INCREMENT POINTER
          INC ADMUX                   ;INCREMENT MULTIPLEXER AND
                                      ;START CONVERSION
          RTI                         ;RETURN TO MAIN LINE
DONE:     CLR ADCSR                   ;CLEAR INTERRUPT ENABLE
            .
            .                         ;FOLLOW THIS WITH THE
                                      ;EVALUATION ROUTINES

WHERE:  ADCSR,ADMUX, AND ADDBR ARE THE DEVICE REGISTERS IN THE INTERFACE
        BUFSTRT CONTAINS THE STARTING ADDRESS OF A BUFFER
        ADCVEC IS THE ADDRESS SPECIFIED BY JUMPERS ON THE M782 MODULE
               AND CONTAINS THE ADDRESS OF THE DEVICE SERVICE ROUTINE
               TAGGED ADCSER
        ADCSER DEVICE SERVICE ROUTINE

BUFADR IS A LOCATION TO BE USED BY THE DEVICE SERVICE ROUTINE
```

After the initiation instructions in the main program are executed, the interrupts cause the processor to execute the ADCSER routine. The last time this is performed, the evaluation routine is also executed.

The CLR ADMUX instruction should precede the MOV #100, ADCSR instruction to prevent the interface from causing an immediate interrupt, which could occur if the interrupt enable bit is set when the device has the conversion complete (ready) signal asserted.

If the evaluation routine is to return control to the interrupted main program, this may be accomplished by terminating the evaluation routine with an RTI instruction. If any other type of return is used, the program must remove the old PC and PS that were placed on the stack by the interrupt operation. Removal is accomplished by executing an ADD #4, R6 instruction.

3.4 DIRECT MEMORY ACCESS (DMA) INTERFACE

The direct memory access (DMA) interface conducts data transfer operations to place data from the device directly into memory. A DMA interface performs a large number of transfers without any processor intervention thereby reducing program and execution time overhead. After the interface device registers are initialized, all transfers take place under control of the interface, thereby eliminating processing time. The processor is notified by an interrupt when all the data has been transferred and the program responds appropriately.

Figure 3-7 is a block diagram of a DMA interface for the Analog-to-Digital Converter (ADC). The DMA is designed by adding circuits to the interrupt serviced device interface. The Interface is composed of two interface registers: the ADCSR register, which contains flag and error bits; and the combined ADBAR/ADMUX register, which holds the bus address and multiplexer bits.

3.4.1 Interface Description

Interface operation begins when the program loads the bus address register (ADBAR) with the address of the first memory location where data is to be stored. The interface starts an ADC conversion cycle. When the digital data is available from the ADC, the interface requests bus use by asserting an NPR request. When the device becomes bus master, it transfers the data to core memory. Completion of the bus transfer causes the multiplexer register (ADMUX) to be incremented, thereby selecting the next input channel. The multiplexer register is part of the bus address register; therefore, the next memory location is also selected. At this point, a new conversion cycle begins. This process is repeated until each input channel is read and the digital data is stored in a core memory location. The interface then sets the ready flip-flop, which causes an interrupt.

3.4.2 Interface Implementaion

The DMA interface is constructed by adding one set of bus drivers and the bus transfer control logic to the interrupt serviced interface; therefore, the functions assigned to the registers differ in this case, and implementation differs accordingly. The multiplexer register, expanded to 15 bits, also serves as a bus address register. Nine of these bits (15:07) are under program control and serve as a base address for a series of locations used as a data collection buffer by the interface. The remaining six bits (06:01) are implemented as a counter that steps through the 64 inputs and also addresses 64 successive word locations in the core memory. The six multiplexer bits are not accesible from the bus and cannot be read nor altered by the program. Whenever the high or low byte of the address register is loaded, the six multiplexer bits are cleared to zero; therefore, transfers always start on 64 word boundaries.

The interface uses an interrupt to signal completion of the series of transfers. The interrupt enable (INTR ENB) and READY bits of the ADCSR operate similar to the interrupt serviced interface.

Loading the ADBAR register (SELECT 2 · OUT HIGH and/or SELECT 2 · OUT LOW) also clears the multiplexer counter and the READY flip-flop, thereby initiating a conversion cycle by causing START CONVERSION H to become asserted.

When the conversion is complete, the CONVERSION COMPLETE H signal sets the REQUEST BUS flip-flop, which causes the M7820 Interrupt Control to assert an NPR request. When bus control is granted, the M7820 asserts BBSY on the UNIBUS and asserts the MASTER A L signal. The MASTER A L signal is tied to the M796 UNIBUS Master Control module in order to produce the START signal. Since the C1 control line is high and the C0 control line is grounded, the M796 performs a DATO bus cycle. An ADRS TO BUS H is produced to gate the nine bits of the ADBAR register and the six bits of the ADMUX register to bus address lines A<15:01>. DATA TO BUS places the converted digital value on bus data lines D<09:00>. After a minimum delay of 150 ns, BUS MSYN L is asserted.

When the slave device responds with BUS SSYN L, both ADRS TO BUS and DATA TO BUS are negated and BUS MSYN L is dropped. The END CYCLE H pulse is

used to clear the REQUEST BUS flip-flop, which in turn causes the M7820 Interrupt Control to drop BUS BBSY.

END CYCLE L is used to trigger a one-shot to produce the COUNT DELAY H signal. This signal serves as the count input (COUNT IN) to the multiplexer counter (ADMUX). After 600 ns, the one-shot times out and its out-put returns to a low (0V) level. If the READY flip-flop has not been set by a count overflow from the ADMUX counter, START CONVERSION H is asserted to start the next conversion cycle. If, however, the ADMUX counter has overflowed and set the READY flip-flop, no ADC operation is started and an interrupt bus request is made.

A TIME-OUT flip-flop is provided on the M796 module. This flip-flop is set if the slave does not respond within 20μs to the BUS MSYN L signal that is produced by the M796 module. If TIME OUT becomes set, the bus cycle is stopped, READY is set, and further conversions are inhibited. The TIME-OUT ERROR is indicated by a 1 in bit 15 of the ADCSR. TIME-OUT is cleared by loading bit 15 of the ADCSR with a 0.

The modules required to implement this interface fit into one BB11 System Unit. All interface modules, including the M7820 Interrupt Control, M105 Address Selector, and a device cable connector, can be inserted into the logic slots of one system unit containing power and UNIBUS connectors. The BB11 System Unit is described in Paragraph 2.4.1.

3.4.3 Programming the Interface

The following is an instruction sequence to initiate device operation:

```
MOV   #BUFADR,ADBAR        ;LOAD ADDRESS AND START
MOV   #100,ADCSR           ;ENABLE INTERRUPT

WHERE:  BUFADR IS THE ADDRESS OF THE FIRST WORD OF A BUFFER AND IS
              RESTRICTED TO ALL 0'S IN BITS 0 THROUGH 6.
```

The interrupt routine for this interface is equivalent to the data evaluation routine suggested in the interrupt serviced interface. The routine should begin with a CLR ADCSR instruction to disable further interrupts (unless serviced at a higher priority level) and should terminate with an RTI instruction.

The ADBAR register can be read as a source operand without spurious clocking of the device operation cycle, but the ADMUX counter is not accessible from the bus.

The interrupt enable flip-flop (bit 6 of the ADCSR) is entirely under program control but the TIME-OUT flip-flop is set by TIME-OUT ERROR conditions in the interface. The ready bit of the ADCSR (bit 7) is not under program control. It may be read by the program but cannot be altered except by initiating operation of the device.

3.4.4 Interface Operation Timing

Figure 3-8 illustrates the timing relationships among signals in the DMA interface. The curved lines indicate the changes in signal level that generate the indicated results.

3.4.5 Interface Options

As described above, operation of the DMA interface is restrictive, because it must always scan 64 channels. A simple method of reducing the number of channels

scanned is to alter the set/reset inputs to the M211 Binary Counter module, thereby preloading it with a non-zero constant from which it can begin counting up.

An even more flexible arrangement could be designed by separating the ADBAR and ADMUX registers, thereby allowing independent bus addressing and multiplexer scanning.

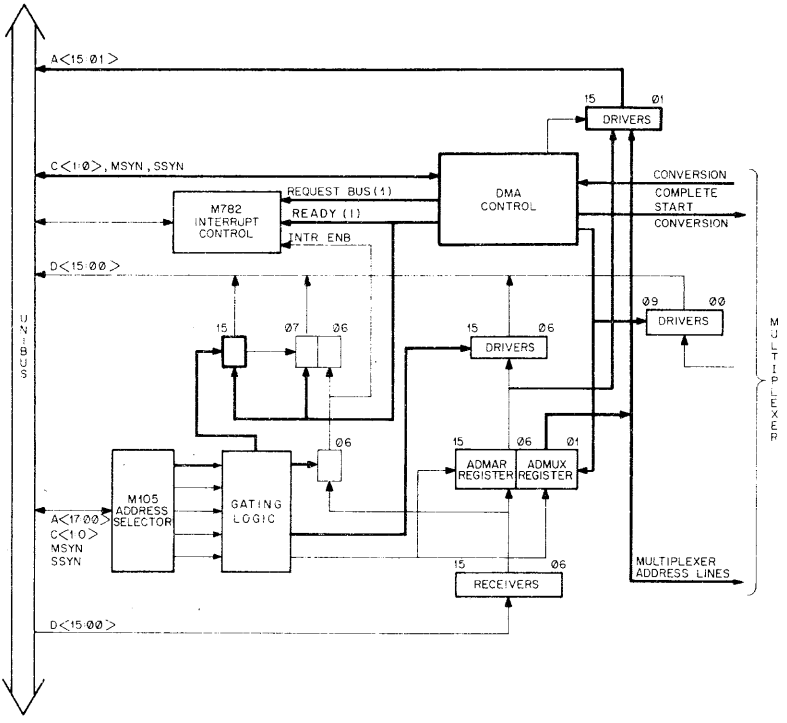


Figure 3-7 DMA Interface (block diagram)

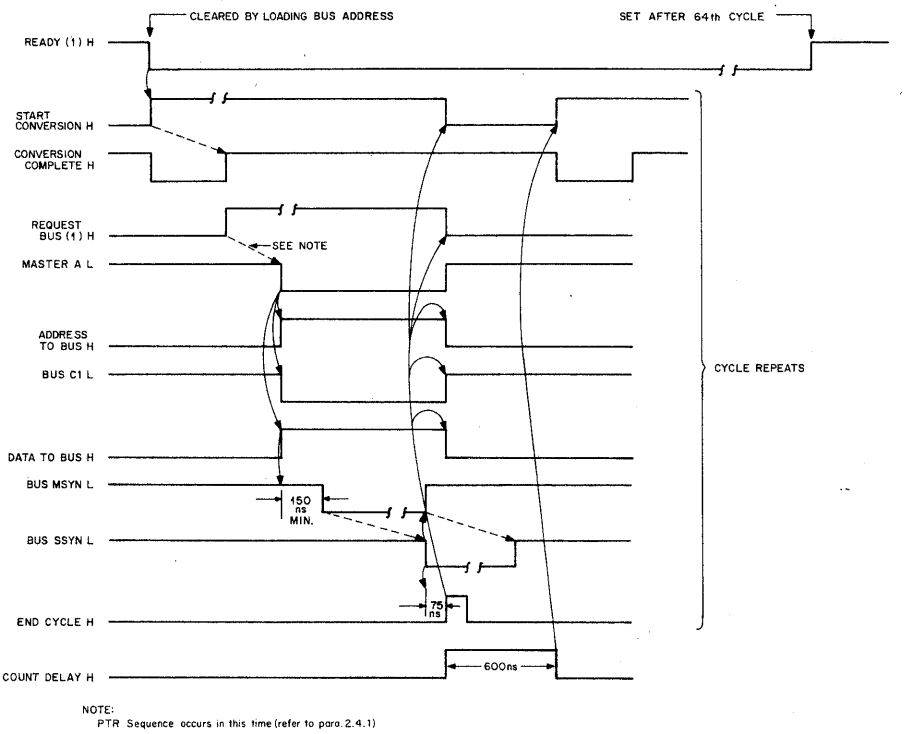


Figure 3-8 DMA Interface (timing diagram)

3.5 OUTPUT INTERFACE WITH INTERRUPT CONTROL

Preceding examples have illustrated various types of interfaces for peripheral devices that provide inputs to the UNIBUS data lines. This example, as well as the example in Paragraph 3.6, covers interface design for a device that accepts UNIBUS outputs. The device shown is meant to be typical of output devices which may be interfaced by designs similar to the following examples.

3.5.1 Device Description

A digital-to-analog converter (DAC) is a device that accepts UNIBUS outputs. The DAC converts a binary weighed number into a scaled analog voltage. The device is single-buffered and the analog output follows the digital input.

The interface provides 10 binary level inputs to the DAC. These inputs represent the digital value equivalent to the analog voltage desired as an output. The binary levels are 0V for binary 0 and +3V for binary 1.

The DAC provides an update request output signal for the interface. This signal requests a new digital input from the interface. At intervals determined by the DAC, a high level (+3V) pulse is provided as the update request signal. This level remains low (0V) between pulses.

3.5.2 Interface Description

The output interface with interrupt control provides a buffer register for outputs to the DAC and an interrupt control to service the DAC with an interrupt service routine. Figure 3-9 is a block diagram of the output interface.

The interface consists of two registers, an M105 Address Selector Module, an M7820 Interrupt Control Module, bus receivers, and two sets of bus drivers. The two registers are the data buffer register (DADBR) and the control status register (DACSR). The request bit (bit 7) of the DACSR can be read by the bus but cannot be loaded directly from the bus. All other register bits are under direct bus control.

3.5.3 Interface Operation

When the UNIBUS addresses the data buffer register during a DATO transfer, the interface clocks the information from the bus data lines into the register, which then applies the information to the DAC as the 10 binary level inputs. At the same time data is clocked into the register, the REQUEST flip-flop (bit 7 of the DACSR) is cleared. After this transfer is complete, when the peripheral device requests another value, the REQUEST flip-flop is clocked high by an UPDATE REQUEST signal from the DAC. If the interrupt enable flip-flop (bit 6 of the DACSR) is set, the interface asserts a bus request line. On becoming bus master, the interface performs an interrupt operation to transfer program control to a service routine. This routine loads new data into the buffer register and then returns control to the interrupted program.

During normal operation, data is loaded into the buffer register and transferred to the peripheral device. When an UPDATE REQUEST from the DAC starts an interface cycle, the interrupt vector is transferred to the processor. The processor again initiates the data flow by transferring a new word of data into DADBR.

3.5.4 Interface Programming

The programs described in this paragraph cause the DAC to output a time-varying signal by loading the DADBR with an initial value and then changing that value by small increments until it reaches a final value determined by the program. The analog output is 100 cycles of a triangular waveform (actually, a stepped triangu-

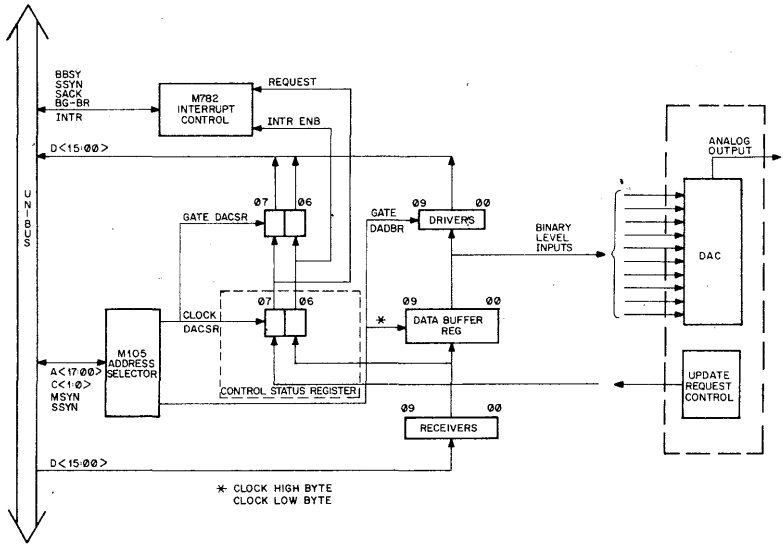


Figure 3-9 Output Interface with Interrupt Control (block diagram)

lar waveform) with the slope of the ascending portion equal to half the slope of the descending portion. The period of the waveform is 150 times the period between update request pulses.

In the interface program, the DAC output is reset to a higher value by the ADD #10. DADBR instruction or reset to a lower value by the SUB #20, DADBR instruction. In either case, the value in the DADBR is read, modified by an arithmetic operation, and the new value is stored in the DADBR. All these operations are under processor control.

The ability of the UNIBUS to access device registers as though they were memory locations allows the processor to directly perform tests and modifications on the device register. This program compares the value in the DADBR with the test values. The program uses a minimum of stored data because it is not necessary to use memory locations for counters or storage of temporary values.

The processor initializes operation by executing the following sequence of instructions:

```
CLR     DADBR              ;CLEAR DATA BUFFER REGISTER
CLR     DASW               ;RESET UP/DOWN SWITCH
MOV     #144,DACNT         ;SET CYCLE COUNTER TO 100
MOV     #100,DACSR         ;SET INTERRUPT ENABLE
```

The interrupt service routine includes the following instructions:

```
DAVEC:  DASERV                          ;POINTER TO SERVICE ROUTINE
        240                             ;PROCESSOR PRIORITY = 5

DASERV: TST     DASW                    ;SWITCH SET?
        BPL     UP                      ;NO, GO UP
        SUB     #20,DADBR               ;YES GO DOWN
        BNE     CONT                    ;OUTPUT VALUE EQUALS 0?
        CLR     DASW                    ;YES, RESET SWITCH
        DEC     DACNT                   ;REDUCE COUNT BY ONE
        BNE     CONT                    ;COUNT EQUALS 0?
        CLR     DACSR                   ;YES, DISABLE INTERRUPT AND EXIT
        RTI

UP:     ADD     #10,DADBR               ;OUTPUT VALUE GOES UP
        CMP     DADBR,#1000             ;1000 IS TOP LIMIT ON VALUE
        BNE     CONT                    ;DOES VALUE EQUAL TOP LIMIT
        COM     DASW                    ;YES, SET SWITCH

CONT:   RTI                             ;EXIT FOR INTERMEDIATE VALUES
```

3.6 DAC-DMA INTERFACE

A direct memory access (DMA) interface designed for a digital-to-analog converter (DAC) allows a specified number of words from memory to be transferred directly to the interface without processor intervention.

The previous interface example (paragraph 3.5) described a digital-to-analog converter interface that was serviced (controlled) by the vectored interrupt structure. In a real-time system where the time to service repetitive interrupts demands too much processor time, it may become necessary to expand the control section of the interface, so that the interface is less dependent on processor control, thereby reducing processor overhead.

This interface example uses the same DAC as the one discussed in the previous example. However, the interface to the UNIBUS differs. Added to the interface control section are direct bus access logic circuits, a word count register, and a bus address register. These additions allow a specified number of words from a particular group of memory addresses to be transferred directly to the interface, independent of processor control. This interface may be used, for example, to drive the X-Y deflection circuits of a CRT display scope in a refresh direct from memory mode.

3.6.1 Interface Description

A block diagram of the DAC-DMA interface is shown in Figure 3-10. The interface contains four registers: a DAC control and status register (DACSR) which contains control and status information; a DAC word count register (DAWC) which holds the 2's complement of the number of words to be transferred; a DAC bus address register (DABA) which indicates where the block of information is held in memory; and a DAC data buffer register (DADB) which buffers information during bus cycles and which can also be loaded under program control.

A typical method of programming this interface is to first initialize the control by loading the DAWC and DABA registers. The next step is to set the GO bit in the DACSR. Words of data are then sequentially taken from memory and loaded into the DADB register at a rate set by the DAC or by an external clock. After each transfer (which is under the control of the interface rather than the processor), the DAWC and DABA registers are incremented. Data transfers continue until the DAWC register overflows (goes to all 0s). At this point, a READY bit in the DACSR

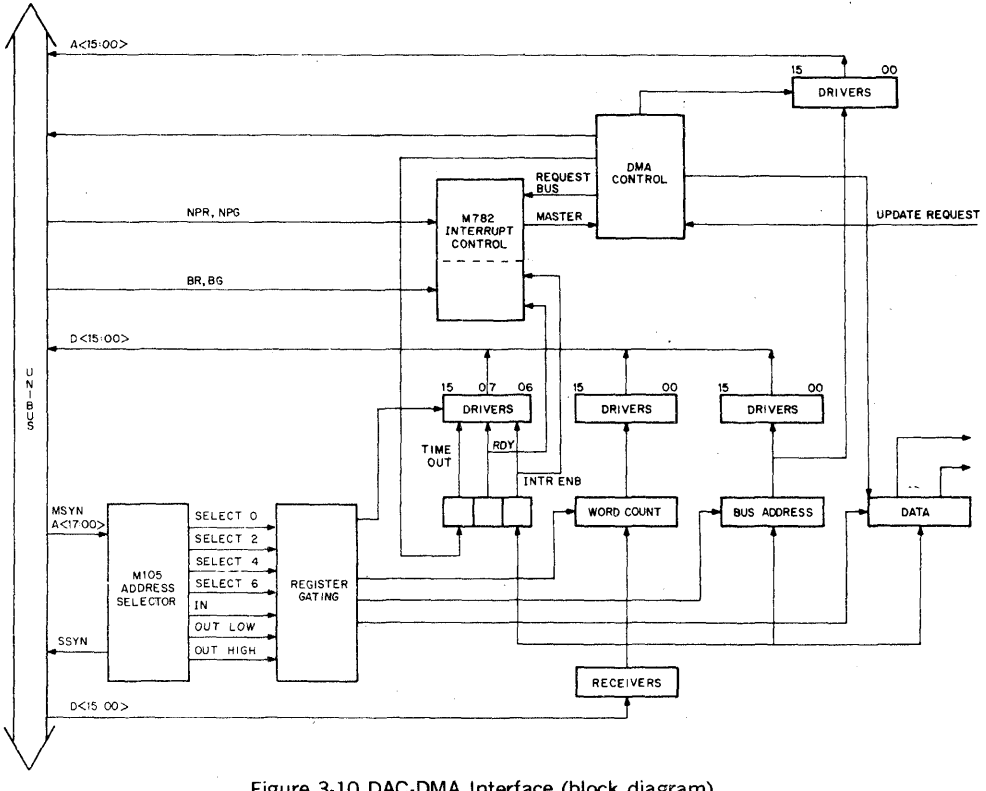


Figure 3-10 DAC-DMA Interface (block diagram)

is set. The READY bit can cause an interrupt to occur (provided INTR ENB is set), thereby notifying the processor that the block transfer is now complete, and another block transfer can be started.

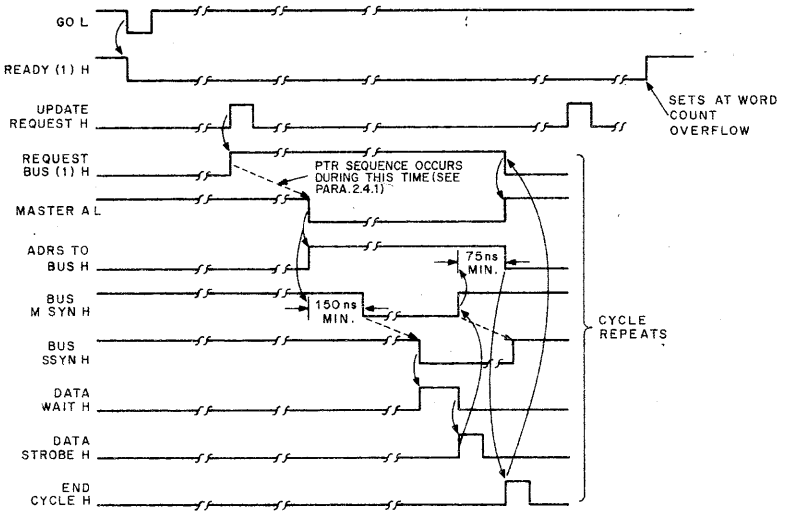


Figure 3-11 DAC-DMA Interface (timing diagram)

3.7 PDP-11 TO DATA CHANNEL INTERFACE

This paragraph presents a block diagram level descriptive of an interface between the PDP-11 UNIBUS and a data channel of another computer. Asynchronous timing permits the PDP-11 to operate successfully with the timing of other sytems through the implementation of a proper timing interface. Actual design depends on the characteristics of the other computer; therefore, this example is only a representative design.

3.7.1 Data Channel Description

Information on the data channel of the secondary computer includes an address, control and timing signals, and the data being transferred. The address is transmitted to a memory address (MA) register and is stored when the data channel begins operation. Data is supplied to a memory buffer (MB) register on one set of lines and is transmitted from the MB to the interface on a second set of lines. (These may be the same set of lines if the data channel uses bidirectional data lines.) Control and timing signals include: a break request (BRK REQ) signal; a data direction (DATA DIR) signal, which is high (+3V) for a transfer to the chan-

nel and low (0V) for a transfer from the channel; a break state (BRK STATE) signal, which is low when the secondary computer is in the break state; and three timing signals transmitted by the channel control to indicate break and address accepted (BRK ACPT), data accepted (DATA ACPT), and data available (DATA AVAIL).

3.7.2 Interface Description

The interface in Figure 3-12 operates as a cycle stealing device on a data channel of another computer and responds as a slave device on the PDP-11 UNIBUS. The primary purpose of this interface is to transfer data between two processors. Therefore, no provision is made to directly control operation of the secondary computer.

The interface structure includes the data paths between the two processors; the address paths from the UNIBUS to the secondary processor; a block (BLK) register (expandable to match the memory space of the secondary processor), which modifies the address transmitted on the data channel in order for it to access one of eight 4K word blocks; and the interface control logic, which determines the timing and gating of the data and control signal flow.

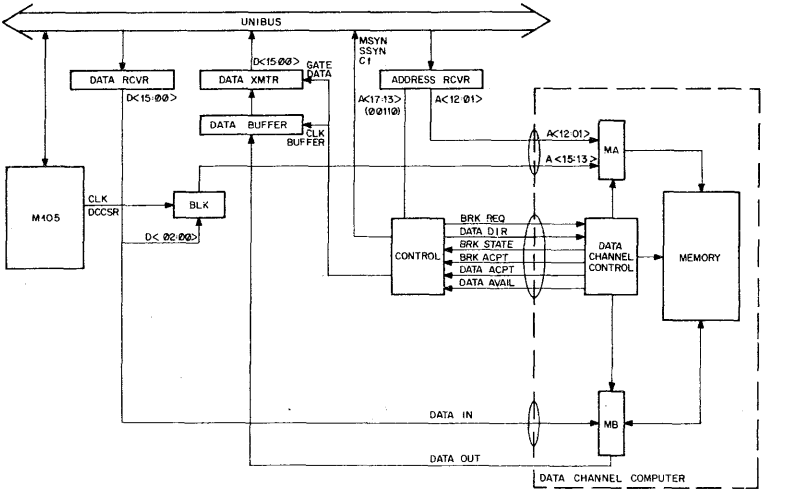


Figure 3-12 PDP-11-to-Data Channel Interface (block diagram)

When the PDP-11 addresses a bus location in the seventh block of 4K words (A<17:13> = 00110), the interface generates a BRK REQ signal. The address used by the data channel is a 15-bit number assembled by transmitting the information on lines A<12:01> as the 12 least significant bits, and transmitting the

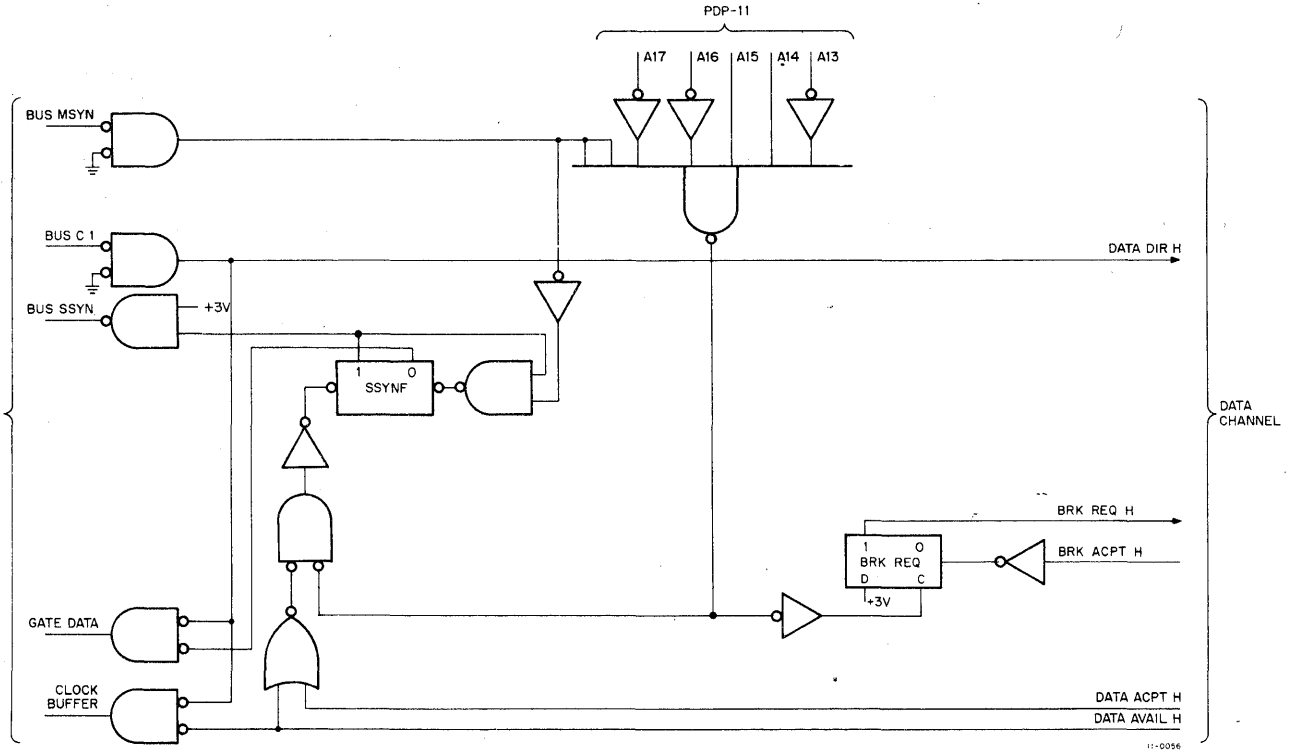


Figure 3-13 PDP-11-to-Data Channel Interface (control circuit schematic)

contents of the BLK register as the 3 most significant bits. The interface responds to 4K word (8K byte) addresses on the UNIBUS, but can access 32K words in the data channel. Only 4K words are accessible for any particular setting of the BLK register.

3.7.3 Interface Operation

When performing transfers with the data channel computer, the PDP-11 first loads the desired block number into the BLK register, which is addressed as a device register (A<17:13> = 11111 and A<12:00> equal to its assigned bus address). The PDP-11 then addresses a location in the 4K block of UNIBUS addresses which have A<17:13> = 00110. The corresponding location in the 4K block selected by the BLK register is selected by the data channel. A data transfer is accomplished by issuing a BRK REQ signal, an address, and setting the DATA DIR level; receiving a BRK ACPT pulse; gating data through the interface; and receiving either a DATA ACPT or a DATA AVAIL pulse to generate SSYN.

3.7.4 Interface Implementation

Figure 3-13 illustrates details of a possible control circuit for implementing the PDP-11 to data channel interface. The BRK REQ flip-flop is set when the bus address is in the specified 4K block and cleared by the BRK ACPT H pulse from the data channel. The SSYNF flip-flop is set by either a DATA ACPT H or a DATA AVAIL H pulse, depending on the direction of the data transfer. The SSYNF flip-flop is cleared when MSYN is cleared. The DATA AVAIL H pulse also clocks data into a buffer register, which is gated to the bus when the SSYNF flip-flop is set. This provides a data transfer to the bus. This implementation assumes that the data channel computer operates with logic levels similar to the PDP-11. Thus, a high (+3V), level is a logic 1 and a low (0V) level is a logic 0.

3.8 PDP-11 TO PDP-11 INTERFACE

The PDP-11 to PDP-11 interface permits devices on one PDP-11 UNIBUS to address locations on a second PDP-11 UNIBUS. Two possible applications of this interface are:

a. Connecting two PDP-11 processors so that one processor executes its own program and also controls execution of programs by a second slave processor.

b. Monitoring operation of a UNIBUS system by a processor that is not in the same system.

3.8.1 Interface Description and Operation

The PDP-11 to PDP-11 interface (Figure 3-14) consists of one M7820 Interrupt Control, one M105 Address Selector Module, several sets of bus receivers and bus drivers, and some control circuits. The M105 Module is connected to the Primary UNIBUS and the M7820 Module is connected to the secondary UNIBUS. The major flow of data within the interface is from one UNIBUS, through bus receivers and gated bus drivers, to the other UNIBUS. Data also flows from the primary UNIBUS to the control circuit.

When the primary UNIBUS requests interface operation, the interface requests control of the secondary UNIBUS, and the primary UNIBUS is connected to allow data transfers with the secondary UNIBUS. The interface is designed to recognize addresses in the seventh 8K (byte) field of primary UNIBUS addresses, and convert them to addresses in any selected 8K (byte) field of addresses on the secondary UNIBUS. This is equivalent to replacing one 8K field of bus addresses on the primary UNIBUS with an 8K field of addresses from the secondary UNIBUS. The field on the secondary UNIBUS is selected by loading a field select register in bits

5 through 1 of the UNIBUS-to-UNIBUS control status register (UUCSR) in the interface. The contents of this 5-bit register are used for the five most significant bits of the secondary bus address. This may be loaded by a MOV BLOCK, UUCSR instruction.

The interface can be operated in one of two modes. In the first mode, a single bus operation may access the secondary UNIBUS by addressing the seventh 4K field on the primary UNIBUS. The interface recognizes the address, requests control of the secondary bus, and interconnects the two sets of bus lines when it receives control. The interface releases control of the secondary UNIBUS when the transfer is complete.

In the second mode of operation, if the hold bit is set in the UUCSR, the interface requests control of the secondary bus and maintains bus mastership until the hold bit is cleared. This mode of operation permits the primary bus to conduct a series of data transfers with the secondary bus at the full bus transfer speed. The only additional time required for a transfer is the signal transmission time within the interface. The time delays caused by waiting for the secondary bus to grant bus mastership to the interface are eliminated; therefore, a disk on the primary bus can transfer data to locations on the secondary bus with the lowest possible latency delays.

3.8.2 Interface Implementation

In Figure 3-14 UNIBUS 1 (the primary UNIBUS) controls the interface and conducts data transfers through the interface to UNIBUS 2 (the secondary UNIBUS). The interface control circuit is shown in greater detail in Figure 3-15. This figure illustrates the UUCSR device register, an address recognition circuit, a MSYN delay circuit, and several gating circuits.

When the address asserted on the primary UNIBUS is in the seventh 8K field (A<17:13> = 00110), the STEAL signal is asserted in the interface. The STEAL L signal causes an NPR request on the secondary UNIBUS. (If the hold flip-flop is set, the interface is already bus master and no further bus requests are initiated.) When the interface becomes a bus master, the MASTER A L signal is asserted. The combination of STEAL L and MASTER A L produces gating signals to interconnect the two sets of bus lines as shown in Table 3-1. The MSYN delay circuit regenerates the 150-ns deskewing period between the assertion of the A and C lines and the assertion of MSYN on the secondary UNIBUS. This prevents delays in signal transmission within the interface from affecting the timing on either UNIBUS.

Table 3-1 Bus Line Gating

Signal	From	To	Gated by	Remarks
A<17:13>	Block Reg	UNIBUS 2	GATE ADDR/CTRL	
A<12:00>	UNIBUS 1	UNIBUS 2	GATE ADDR/CTRL	
C<1:0>	UNIBUS 1	UNIBUS 2	GATE ADDR/CTRL	
D<15:00>	UNIBUS 2	UNIBUS 1	GATE IN	C1 = 0 (DATI or DATIP)
D<15:00>	UNIBUS 1	UNIBUS 2	GATE OUT	C1 = 1 (DATO or DATOB)
MSYN	UNIBUS 1	UNIBUS 2	GATE MSYN	
SSYN	UNIBUS 2	UNIBUS 1	GATE ADDR/CTRL	

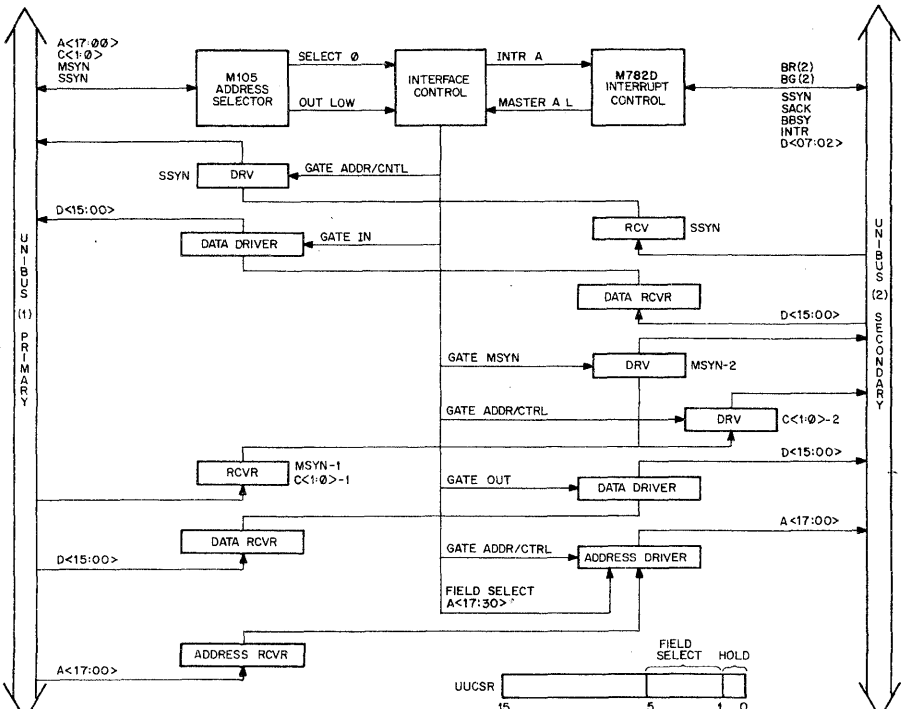


Figure 3-14 PDP-11-to-PDP-11 Interface (block diagram)

3.8.3 Interface Programming

To type a character on the secondary UNIBUS system Teletype, the processor on the primary UNIBUS executes the following sequence of instructions:

```
MOV    #75,UUCSR    WHERE: UUCSR IS THE CONTROL REGISTER IN THE INTERFACE
MOV    CHAR,XPB            CHAR IS THE LOCATION CONTAINING THE CHARACTER
                           XPB HAS THE VALUE 157566
```

The address transmitted on the secondary UNIBUS is the 13 least significant bits of XPB (17566) with the contents of the field select register appended as the 5 most significant bits. The address is therefore 777566, which is the address of the system Teletype TPB.

A block of data is transferred to locations on the secondary UNIBUS by setting the hold bit when the field register is set:

```
MOV    FIELD,UUCSR    WHERE: FIELD IS THE NUMBER OF THE 4K FIELD
                             OF WORD ADDRESSES TO BE ACCESSED ON
                             THE SECONDARY UNIBUS (WITH A 1 APPENDED
                             TO SET THE HOLD BIT)
```

Data transfers then access locations in that address field when the address on the primary UNIBUS has A<17:13> equal to 00110 and A<12:00> equal to the desired value of A<12:00> on the secondary UNIBUS. If FIELD has the value 11_8, the address 140020_8 is translated to the address 100020_8.

3.9 MEMORY INCREMENT INTERFACE

An Increment Memory interface is used to increment a device-selected memory location without requiring processor intervention. The interface operates by performing a DATIP, DATO sequence with the selected memory location. This sequence is the same as processor operation with a destination operand. Data read from the memory location by the DATIP transfer is loaded into a counter register. A count cycle is initiated, and the count is allowed to ripple through the register. The new value is written back into the memory during the DATO cycle.

A more flexible implementation uses an adder instead of a counter. The contents of the memory location are brought into a latch, which forms one input to the adder. The other input can be under device or program control, or a simple increment operation can be executed by providing a carry into the least significant bit. The adder permits arbitrary values to be added to the selected location. This expanded interface is not described in subsequent discussions.

This interface differs from previous interface examples because the device output is used as a bus address rather than as data. The operations performed on the data in these locations effectively generate a time-interval histogram directly in core memory.

3.9.1 Interface Description and Operation

In Figure 3-16, the analog-to digital converter (ADC), which is an external device that supplies the digital value used as an address, is not part of the interface. One device register is used in the interface. The device register contains the enable bit which controls access of the interface to the UNIBUS, and contains the five field select bits used to select a 4K word block of bus addresses that the interface uses for conducting transfers. The counter and transmitters are under interface control. The interface provides all timing and control signals for one cycle of oper-

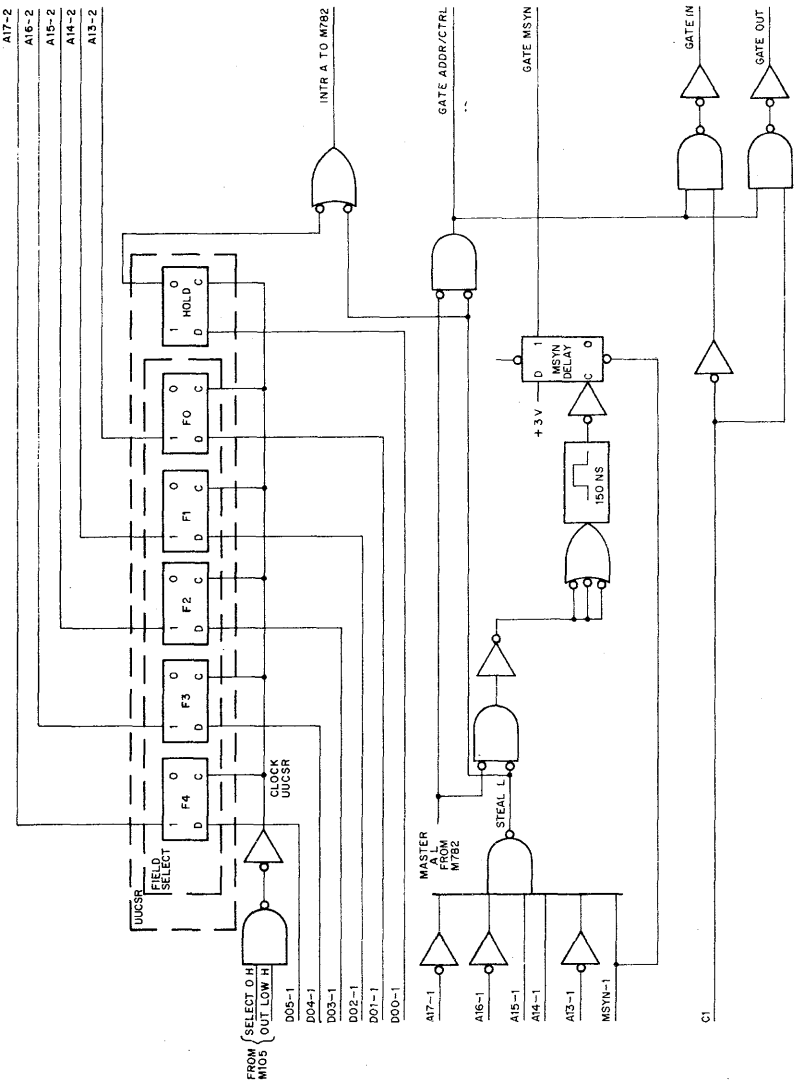


Figure 3-15 PDP-11-to-PDP-11 Interface Control (circuit schematic)

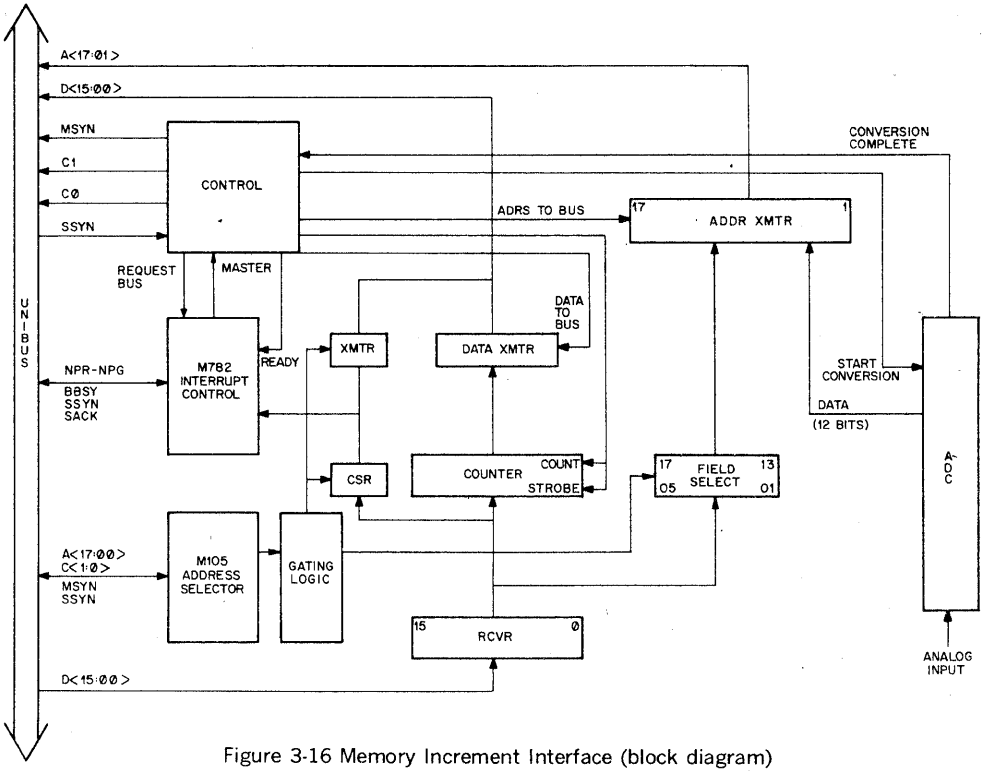


Figure 3-16 Memory Increment Interface (block diagram)

ation and each successive cycle of operation is initiated by a signal from the device. In this example, the device is an ADC similar to the ADC described in Paragraph 3.3. The rate at which successive conversion cycles are performed is not defined in this example. However, the rate can be controled by an external clock, so that the clock frequency determines the sampling rate.

A timing diagram is shown in Figure 3-17. The signal that starts a cycle of interface operation is CONVERSION COMPLETE H. This signal is generated by the ADC after it has completed conversion of the analog input to a digital value, and that value is available as a data output from the ADC. The CONVERSION COMPLETE signal sets the REQUEST BUS flip-flop which causes the M7820 Master Control A module to gain control of the UNIBUS by means of an NPR request. The MASTER A L signal triggers START on the M796 module and, since CYCLE CONTROL is clear, a DATIP bus cycle is performed. The ADRS TO BUS H signal is used to gate an address on to the address bus. This address is formed by data from the ADC (least significant portion of the address) and the field select bits (most significant portion of the address). After a delay, BUS MSYN L is asserted.

When the slave (usually memory) responds with data and a BUS SSYN L signal, DATA WAIT L is triggered to allow for deskewing of the data. The trailing edge of DATA WAIT triggers the DATA STROBE one-shot. The DATA STROBE signal loads the data present on BUS D<15:00> into the interface counter register. When DATA STROBE times out, DATA ACCEPTED is asserted, negating BUS MSYN, and firing the COUNT PULSE and COUNT DELAY one-shots. COUNT PULSE is set for the worst case ripple time of the counter.

When the COUNT DELAY is complete and BUS SSYN L is negated by the previous DATIP bus cycle, START is again asserted. Since CYCLE CONTROL is now set (set by END CYCLE of the previous DATIP), a DATO bus cycle is performed. The DATA TO BUS H signal is asserted and gates the contents of the incremented counter to the bus data lines.

When the DATO cycle is complete, END CYCLE and CYCLE CONTROL set are ANDed to clear the REQUEST BUS flip-flop, which causes the M7820 module to drop BUS BBSY L, thereby releasing control of the bus.

3.9.2 Optional Arrangements

The timing chain of DATA WAIT, DATA STROBE, COUNT PULSE, and COUNT DELAY is designed for the case where count time is significant and the counter is loaded and incremented by a level rather than a transition.

Other logic may be used dependent upon the type and speed of the counter employed in the interface.

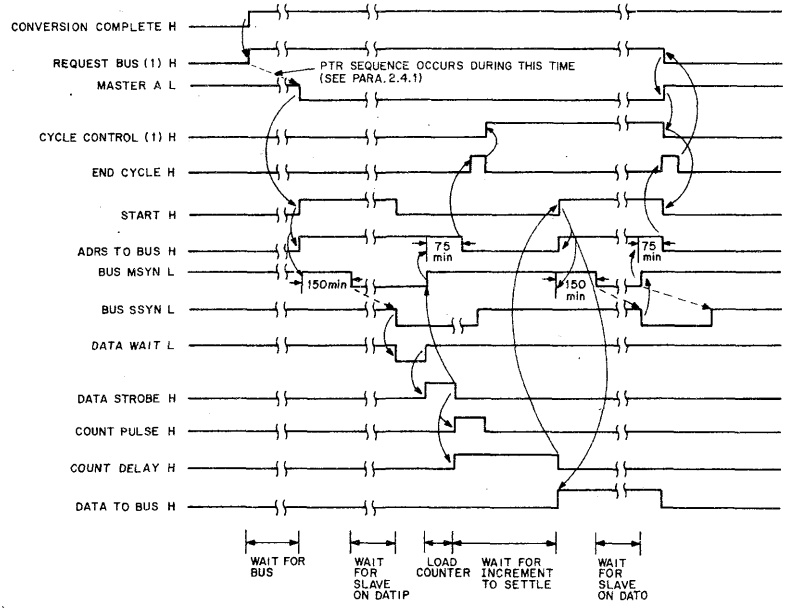


Figure 3-17 Memory Increment Interface (timing diagram)

3.10 DIRECT MEMORY ACCESS INTERFACE (DR11-B)

The DR11-B is a general purpose direct memory access (DMA) interface to the UNIBUS. The DR11-B, rather than using program controlled data transfers, operates directly to or from memory, moving data between the UNIBUS and the user device.

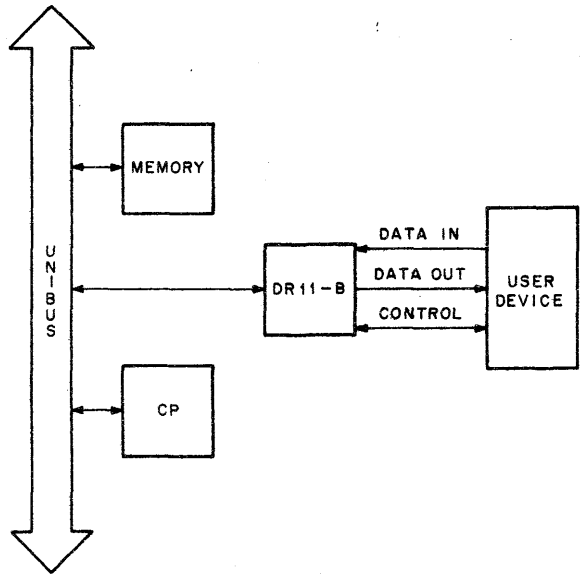


Figure 3-18 System Block Diagram

The interface consists of four registers: command and status, word count, bus address, and data. Operation is initialized under program control by loading word count with the 2's complement of the number of transfers, specifying the initial memory or bus address where the block transfer is to begin, and by loading the command/status register with function bits. The user device recognizes these function bits and responds by setting up the control inputs. If the user device requests data from memory or a UNIBUS device, the DR11-B performs a UNIBUS data transfer (DATI) and loads its data register with the information held at the referenced bus address. The outputs of this register are available to the user device. (This output data is buffered.) If the user device requests data to be written into memory, the DR11-B performs a UNIBUS data transfer (DATO), moving data from the user to the referenced bus address. (This input data from the user is not buffered.) Transfers normally continue at a user defined rate until the specified number of words are transferred.

The user is given a number of control lines allowing for flexible operation. Burst modes, read-modify-restore operations, and byte addressing are possible with the control structure.

3.10.1 Physical Description

The DR11-B is packaged in one standard system unit allowing convenient incorporation into a PDP-11 system. A UNIBUS jumper module (M920) is supplied with the unit. Power is applied to the logic through the power harness already provided in the BA11 mounting box. Current requirements are 3.3 amps at +5V, zero at -15V.

Connections to the user device are made through two M957 split lug cable boards, which are supplied with the unit. Alternatively, an M920 can be used to jumper all user signals to an adjacent BB11 blank mounting panel, which might package some or all of the device logic. (Neither the additional M920 nor the BB11 is supplied with the unit.)

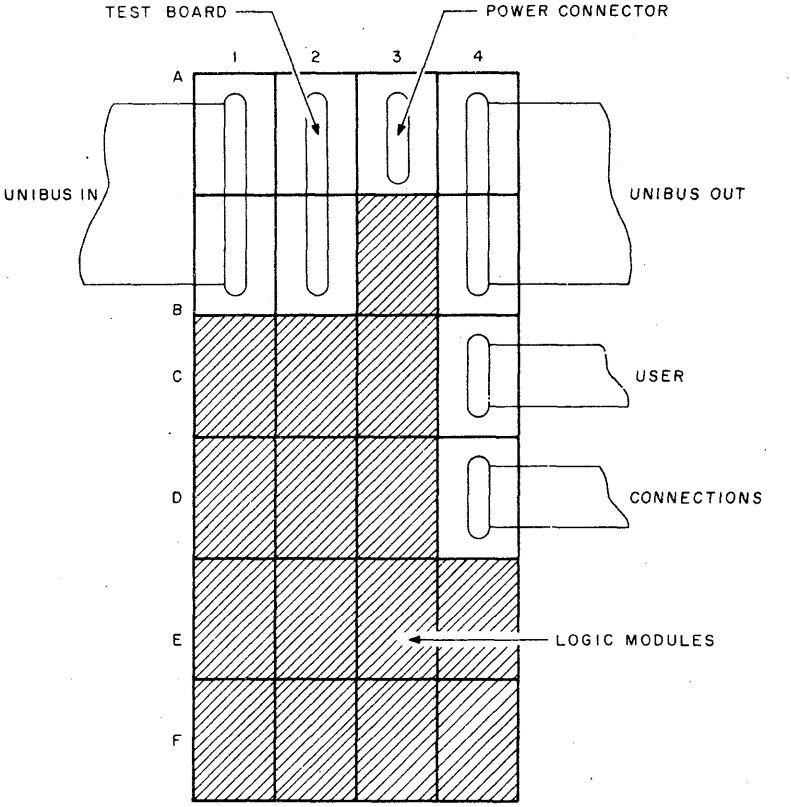


Figure 3-19 DR11-B System Unit

3.10.2 Software Interface

The following presents a detailed description of the four DR11-B registers. These registers are assigned bus addresses and can be read or loaded (with the exception noted) using any instruction that refers to their address. "INIT" refers to the initialization signal produced on power up, power down, by the RESET instruction, or by the start switch on the console. "R/W" stands for read/write. Note that the INIT signal is held asserted internal to the DR11-B whenever an interlock error occurs (M968 test board neither in slots AB02 for normal operation nor CD04 for maintenance mode).

Status and Command Register (DRST)

The DRST is used to give commands to the user device and to provide status indicators of the DR11-B control and the user device.

BIT	NAME	MEANING AND OPERATION
15	Error	Indicates an error condition: either NEX (BIT 14), ATTN (BIT 13), interlock error (test board is neither in slots AB02 nor CD04), or bus address overflow (BAOF:DRBA incremented from all 1's to all 0's). Sets READY (BIT 7) and causes interrupt if IE (BIT 6) is set. ERROR is cleared by removing all four possible error conditions: interlock error is removed by inserting test board in CD04 for diagnostic tests or in AB02 for normal operation; bus address overflow is cleared by loading DRBA; NEX is cleared by loading bit 14 with a zero; ATTN is cleared by user device. Read only.
14	Nonexistent Memory (NEX)	Non-existent memory indicates that as Unibus master, the DR11-B did not receive a SSYN response 20 usec after asserting MSYN. Cleared by INIT or loading with a 0; can not be loaded with a 1. Sets ERROR. Read/Write 0.
13	Attention (ATTN)	Attention bit that reads the state of the ATN user signal. Sets ERROR. (Used for device initiated interrupt.) Set and cleared by user control only. Read only.
12	Maintenance	Maintenance bit used with diagnostic programs. Cleared by INIT. Read/Write.
11-9	Device Status (DSTAT A,B,C)	Device status bits that read the state of the DSTAT A, B, and C user signals. (Not tied to interrupt.) Set and cleared by user control only. Read only.
8	Cycle	CYCLE is used to prime bus cycles; if set when GO is issued, an immediate bus cycle occurs. Cleared when bus cycle begins; cleared by INIT. Read/Write.

7	Ready	Indicates that the DR11-B is able to accept a new command. Set by INIT or ERROR; cleared by GO; set on word count overflow. Causes interrupt if bit 6 is set. Forces DR11-B to release control of the Unibus and prevents further DMA cycles. Read only.
6	Enable Interrupt IE	Enables interrupt to occur when either ERROR or READY is set. Cleared by INIT. Read/Write.
5-4	Extended Bus Address	Extended bus address bits 17 and 16 that in conjunction with DRBA specify A(17:01) in direct memory transfers. Cleared by INIT. XBA17 & 16 do not increment when DRBA overflows; instead ERROR is set. Read/Write.
3-1	Function 3,2,1	Three bits made available to the user device. User defined. Cleared by INIT. Read/Write.
0	Go	Causes a pulse to be sent to the user device indicating a command has been issued. Clears READY. Always reads as a zero. Write only.

Word Count Register (DRWC)
DRWC is a 16-bit R/W register. It is initially loaded with the two's complement of the number of transfers to be made and normally increments up towards zero after each bus cycle. Incrementation can be inhibited by the user device; refer to the WC INC ENB user signal. When overflow occurs (all 1's to all 0's), the READY bit of DRST is set and bus cycle stop. DRWC is a word register; do not use byte instructions when loading this register. Cleared by INIT.

Bus Address Register (DRBA)
DRBA is a 15-bit R/W register. Bit 0, corresponding to address line A00 is provided by the user device. Along with XBA16 and 17 in DRST, DRBA is used to specify BUS A8(17:01) in direct bus access. The register is normally incremented (+2) after each bus cycle, advancing the address to the next sequential word location on the bus. If DRBA (corresponding) to A(15:01)) overflows (all 1's to all 0's) the ERROR bit in DRST is set. This error condition (BAOF) is cleared by loading DRBA or INIT. Incrementation can be inhibited by the user device; refer to the BA INC ENB user signal. With this control signal and A00 provided externally, DRBA can be used to address sequential bytes. This is a word register; do not use byte instructions when loading this register. Cleared by INIT.

Data Buffer Register (DRDB)
The DRDB serves two functions: First, it is a 16-bit write only register. The outputs of this register are available to the user device (refer to the DATA OUT signals). The register can be loaded under program control, but is also used to buffer information when data is being transferred from the UNIBUS to the user device (when DR11-B does a DATI cycle). DRDB is a word register; do not use byte instructions when loading this register. Cleared by INIT.

Second, the DRDB functions as a 16-bit read only register. Information to be read is provided by the user device on the DATA IN signal lines. These lines are not buffered and must be held until either read under program control or transferred directly to memory (DATO bus cycle).

Address and Vector Assignments
Direct bus access level: NPR (hardwired)

Priority interrupt level: BR5 (hardwired)

APPENDIX A

PDP 11 DEVICE REGISTERS AND INTERRUPT VECTORS.
VECTORS

000	RESERVED	
004	TIME OUT, BUS ERROR	
010	RESERVED INSTRUCTION	
014	DEBUGGING TRAP VECTOR	
020	IOT TRAP VECTOR	
024	POWER FAIL TRAP VECTOR	
030	EMT TRAP VECTOR	
034	"TRAP" TRAP VECTOR	
040	SYSTEM SOFTWARE	
044	SYSTEM SOFTWARE	
050	SYSTEM SOFTWARE	COMMUNICATION WORDS
054	SYSTEM SOFTWARE	
057		
060	TTY IN-BR4	
064	TTY OUT-BR4	
070	PC11 HIGH SPEED READER-BR4	
074	PC11 HIGH SPEED PUNCH	
100	KW11L - LINE CLOCK BR6	
104	KW11P - PROGRAMMER REAL TIME CLOCK BR6	
110		
114		
120	XY PLOTTER	
124	DR11B-(BR5 HARDWIRED)	
130	ADO1 BR5-(BR7 HARDWIRED)	
134	AFC11 FLYING CAP MULTIPLEXER BR4	
140	AA11-A,B,C SCOPE BR4	
144	AA11 LIGHT PIN BR5	
150	.	
154	.	
160	.	
164	.	
170	USER RESERVED	
174	USER RESERVED	
200	LP11 LINE PRINTER CTRL-BR4	
204	RF11 DISK CTRL-BR5	
210	RC11 DISK CTRL-BR5	
214	TC11 DEC TAPE CTRL-BR6	
220	RK11 DISK CTRL-BR5	
224	TM11 COMPATIBLE MAG TAPE CTRL-BR5	
230	CR11/CM11 CARD READER CTRL-BR6	
234	UDC11 (BR4, BR6 HARDWIRED)	
240	11/45 PIRQ	
244	FPU ERROR	
250		
254	RP11 DISK PACK CTRL-BR5	

260
264
270 USER RESERVED
274 USER RESERVED

300 START OF FLOATING VECTORS--BR5
304 STARTING AT 300 ALL KL11'S (BR4), THEN ALL DC11'S (BR5), THEN DP11'S (BR5)
THEN DM11 (BR5), DN11 (BR5), AND DM11BB, DR11A, TYPE SET READERS, TYPE
SET PUNCHES, DT11 (BR7) (DS11 VECTOR IS AT 1000)

500 FACTORY BUS TESTERS

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546

DEVICE ADDRESS

NOTE: XX MEANS A RESERVED ADDRESS FOR THAT OPTION. OPTION MAY NOT USE IT BUT IT WILL RESPOND TO BUS ADDRESS.

777776 CPU STATUS
777774 11/45 STACK LIMIT REGISTER
777772 11/45 PIRQ REGISTER
777716 TO 777700 CPU REGISTERS
777676 TO 777600 11/45 SEGMENTATION REGISTER
777656 TO 777650 MX11 #6
777646 TO 777640 MX11 #5
777636 TO 777630 MX11 #4
777626 TO 777620 MX11 #3
777616 TO 777610 MX11 #2
777606 TO 777600 MX11 #1
777576 11/45SSR2
777574 11/45 SSR1

777572 11/45 SSR0
777570 CONSOLE SWITCH REGISTER
777566 KL11 TTY OUT DBR
777564 KL11 TTY IN CSR
777562 KL11 TTY IN DBR
777560 KL11 TTY OUT CSR
777556 PC11 HSP DBR
777554 PC11 HSP CSR
777552 PC11 HSR DBR
777550 PC11 HSR CSR
777546 LKS LINE CLOCK KW11-L

777526 DR11A-XX--
777524 SEE 767776
777522 DR11A DBR
777520 DR11A CSR
777516 LP11 DBR
777514 LP11 CSR
777512 LP11 XX
777510 LP11 XX
777506
777504
777502
777500

777476 RF11 DISK RFLA LOOK AHEAD
777474 RF11 DISK RFMR MAINTENANCE
777472 RF11 DISK RFDBR
777470 RF11 DISK RFDAE
777466 RF11 DISK RFDAR
777464 RF11 DISK RFCAR
777462 RF11 DISK RFWC
777460 RF11 DISK RFDSC

777456 RC11 DISK RCDBR
777454 RC11 REMAINTENANCE
777452 RC11 RCCAR
777450 RC11 RCWC
777446 RC11 RCCSR1
777444 RC11 RCCSR1
777442 RC11 RCDAR
777440 RC11 RCLA

777434 DT11 BUS SWITCH #7
777432 BUS SWITCH #6
777430 BUS SWITCH #5
777426 BUS SWITCH #4
777424 BUS SWITCH #3
777422 BUS SWITCH #2
777420 BUS SWITCH #1

777416 RKDB RK11 DISK
777414 RKMR
777412 RKDA

777410	RKBA	
777406	RKWC	
777404	RKCS	
777402	RKER	
777400	RKDS	
777356	TCXX	
777354	TCXX	
777352	TCXX	
777350	TCDT	DEC TAPE (TC11)
777346	TCBA	
777344	TCWC	
777342	TCCW	
777340	TCST	
777336	ASH	EAE (KE11-A) # 2
777334	LSH	
777332	NOR	
777330	SC	
777326	MUL	
777324	MQ	
777322	AC	
777300	DIV	
777316	ASH	EAE (KE11-A) # 1
777314	LSH	
777312	NOR	
777310	SC	
777306	MUL	
777304	MQ	
777302	AC	
777300	DIV	
777166	CR11 XX	
777164	CRDBR2	CR11/CM11 CARD READER
777162	CRDBR1	
777160	CRCSR	
776776	ADO1-D XX	
776774	ADO1-D XX	
776772	ADDBR	A/D CONVERTER ADO1-D
776770	ADCSR	
776766	DAC3	DAC AA11
776764	DAC2	
776762	DAC1	
776760	DAC0	
776756	SCOPE CONTROL - CSR	
776754	AA11 XX	
776752	AA11 XX	
776750	AA11 XX	

776740 RPBR3 RP11 DISK
776736 RPBR2
776734 RPBR1
776732 MAINTENANCE #3
776730 MAINTENANCE #2
776726 MAINTENANCE #1
776724 RPDA
776222 RPCA
776720 RPBA
776716 RPWC
776714 RPCS
776712 RPER
776710 RPDS

776676 TO 776500 MULTI TTY FIRST STARTS AT 776500

776476 TO 776406 MULTIPLE AA11'S SECOND STARTS @ 776760
776476 TO 776460 5TH AA11
776456 TO 776440 4TH AA11
776436 TO 776420 3RD AA11
776416 TO 776400 2ND AA11
NOTE 1ST AA11 IS AT 776750

776377 TO 776200 DX11
775600 DS11 AUXILIARY LOCATION
775577 TO 775540 DS11 MUX3
775537 TO 775500 DS11 MUX2
775477 TO 775440 DS11 MUX1
775436 TO 775400 DS11 MUX0
775377 TO 775200 DN11
775177 TO 775000 DM11
774777 TO 774400 DP11/DC11
774377 TO 774000 DC11/DP11

773777 TO 773000 DIODE MEMORY MATRIX

773000 BM792-YA PAPER TAPE BOOTSTRAP
773100 BM792-YB RC,RK,RP,RF AND TC11 - BOOTSTRAP
773200
773300
773400
773500
773600
773700 RESERVED FOR MAINTENANCE LOADER

772776 TO 772700 TYPESET PUNCH
772676 TO 772600 TYPESET READER

772576 AFC-MAINTENANCE
772574 AFC-MUX ADDRESS
772572 AFC-DBR
772570 AFC-CSR

772546 KW11P XX
772544 KW11P COUNTER
772542 KW11P COUNT SET BUFFER
772540 KW11P CSR
772536 TM11 XX
772534 TM11 XX
772532 TM11 LRC
772530 TM11 DBR
772526 TM11 BUS ADDRESS
772524 TM11 BYTE COUNT
772522 TM11 CONTROL
772520 TM11 STATUS
772512 OST CSR
772510 OST EADRS1,2
772506 OST ADRS2
772504 OST ADRS1
772502 OST MASK2
772500 OST MASK1
772476 DR11B DBR4
772474 DR11B CSR4
772472 DR11B BA4
772470 DR11B WC4
772466
772462
772460
772456 DR11B DBR3
772454 DR11B CSR3
772450 DR11B BA3
772450 DR11B WC3
772446
772444
772442
772440
772436 DR11B DBR2
772434 DR11B CSR2
772432 DR11B BA2
772430 DR11B WC2
772426
772424
772422
772420
772416 DR11B/DATA
772414 DR11B/STATUS
772412 DR11B/BA
772410 DR11B/WC
772146 TO 772110 MEMORY PARITY CSR
772146 15
772120 4
772116 3
772114 2
772112 1
772110 0
771776 UDCS - CONTROL AND STATUS REGISTER

771774 UDSR - SCAN REGISTER
771772 UDCM - MAINTENANCE REGISTER
771766 UDC FUNCTIONAL I/O MODULES
771000 UDC FUNCTIONAL I/O MODULES
770776 TO 770700 KG11 CRC OPTION
770776 KG11A KGNU7
770774 KGBCC7
770772 KGDBR7
770770 KGCSR7
770716 KGNU4
770714 KGBCC3
770712 KGDBR2
770710 KGCSR1
770706 KGNU0
770704 KGBCC0
770702 KGDBR0
770700 KG11A KGCSR0
770676 TO 770500 16 LINE FOR DM11BB
770676 DM11BB #16
770674
770672
770670
770666 DM11BB #15
770664
770662
770660
770656 DM11BB #14
770654
770652
770650
770646 DM11BB #13
770644
770642
770640
770636 DM11BB #12
770634
770632
770630
770626 DM11BB #11
770624
770622
770620
770616 DM11BB #10
770614
770612
770610
770606 DM11BB #9
770604
770602
770600 DM11BB #8
770076 LATENCY TESTER
770074 LATENCY TESTER
770072 LATENCY TESTER

770070 LATENCY TESTER
770056 TO 770000 SPECIAL FACTORY BUS TESTERS
767776 TO 764000 FOR USER and SPECIAL SYSTEMS---DR11A ASSIGNED IN USER
AREA-STARTING AT HIGHEST ADDRESS WORKING DOWN
767776 DR11A #0
767774
767772
767770
767766 DR11A #1
767764
767762
767760
767756 DR11A #2
767754
767752
767750

764000 START NORMAL USER ADDRESSES HERE AND ASSIGN UPWARD.
760004 TO 760000 RESERVED FOR DIAGNOSTIC - SHOULD NOT BE ASSIGNED

APPENDIX B

SLOTS A1 AND B1 (A4 AND B4) ARE WIRED AS SHOWN IN TABLES B-1 AND B-2.

TABLE B-1 UNIBUS PIN ASSIGNMENTS (BY PIN NUMBERS)

PIN	SIGNAL	PIN	SIGNAL
AA1	INIT L	BA1	BG 6 H
AA2	POWER(+5V)	BA2	POWER(+5V)
AB1	INTR L	BB1	BG 5 H
AB2	GROUND	BB2	GROUND
AC1	DOO L	BC1	BR 5 L
AC2	GROUND	BC2	GROUND
AD1	DO2 L	BD1	GROUND
AD2	DOI L	BD2	BR 4 L
AE1	DO4 L	BE1	GROUND
AE2	DO3 L	BE2	BG 4 H
AF1	DO6 L	BF1	ACLO L
AF2	DO5 L	BF2	DCLO L
AH1	DO8 L	BH1	AO1 L
AH2	DO7 L	BH2	AOO L
AJ1	D1O L	BJ1	AO3 L
AJ2	DO9 L	BJ2	AO2 L
AK1	D12 L	BK1	AO5 L
AK2	D11 L	BK2	AO4 L
AL1	D14 L	BL1	AO7 L
AL2	D13 L	BL2	AO6 L
AM1	PA L	BM1	AO9 L
AM2	D15 L	BM2	AO8 L
AN1	GROUND	BN1	A11 L
AN2	PB L	BN2	A1O L
AP1	GROUND	BP1	A13 L
AP2	BBSY L	BP2	A12 L
AR1	GROUND	BR1	A15 L
AR2	SACK L	BR2	A14 L
AS1	GROUND	BS1	A17 L
AS2	NPR L	BS2	A16 L
AT1	GROUND	BT1	GROUND
AT2	BR 7 L	BT2	C1 L
AU1	NPG H	BU1	SSYN L
AU2	BR 6 L	BU2	CO L
AV1	BG 7 H	BV1	MSYN L
AV2	GROUND	BV2	GROUND

TABLE B-2 UNIBUS PIN ASSIGNMENTS (BY SIGNAL NAME)

SIGNAL	PIN	SIGNAL	PIN
AO0 L	BH2	DO6 L	AF1
AO1 L	BH1	DO7 L	AH2
AO2 L	BJ2	DO8 L	AH1
AO3 L	BJ1	DO9 L	AJ2
AO4 L	BK2	D10 L	AJ1
AO5 L	BK1	D11 L	AK2
AO6 L	BL2	D12 L	AK1
AO7 L	BL1	D13 L	AL2
AO8 L	BM2	D14 L	AL1
AO9 L	BM1	D15 L	AM2
A10 L	BN2	GROUND	AB2
A11 L	BN1	GROUND	AC2
A12 L	BP2	GROUND	AN1
A13 L	BP1	GROUND	AP1
A14 L	BR2	GROUND	AR1
A15 L	BR1	GROUND	AS1
A16 L	BS2	GROUND	AT1
A17 L	BS1	GROUND	AV2
ACLO L	BF1	GROUND	BB2
BBSY L	AP2	GROUND	BC2
BG4 H	BE2	GROUND	BD1
BG5 H	BB1	GROUND	BE1
BG6 H	BA1	GROUND	BT1
BG7 H	AV1	GROUND	BV2
BR4 L	BD2	INIT L	AA1
BR5 L	BC1	INTR L	AB1
BR6 L	AU2	MSYN L	BV1
BR7 L	AT2	NPG H	AU1
CO L	BU2	NPR L	AS2
C1 L	BT2	PA L	AM1
DOO L	AC1	PB L	AN2
DO1 L	AD2	+ 5V*	AA2
DO2 L	AD1	+ 5V*	BA2
DO3 L	AE2	SACK L	AR2
DO4 L	AE1	DCLO L	BF2
DO5 L	AF2	SSYN L	BU1

* + 5V IS WIRED TO THESE PINS TO SUPPLY POWER TO THE BUS TERMINATOR ONLY.

+ 5V SHOULD NEVER BE CONNECTED VIA THE UNIBUS BETWEEN SYSTEM UNITS.

TABLE B-3 BB11 POWER PIN ASSIGNMENTS

PIN	POWER
A1	-15V
A2	+5V
B1	-15V
B2	-15V
C1	-15V
C2	GND
D1	-15V
D2	GND
E1	-15V
E2	GND
F1	-15V
F2	GND
H1	-15V
H2	+5V
J1	-15V
J2	+5V
K1	-15V
K2	+5V
L1	-15V
L2	+5V
M1	-15V
M2	+5V
N1	GND
N2	-25V
P1	GND
P2	LTC L
R1	GND
R2	ACLO L
S1	GND
S2	DCLO L
T1	GND
T2	+8V
U1	GND
U2	+8V
V1	GND
V2	+8V

NOTE

POWER IS IN MODULE SLOT A3 OF ALL SYSTEM UNITS MOUNTED IN BA11 MOUNTING BOXES EQUIPPED WITH H720 POWER SUPPLIES.

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Numerous individuals in the PDP-11 Marketing, PDP-11 Engineering, Programming, Tape Preparation, and Technical Documentation departments, contributed to the writing, editing and production of this Handbook. Particularly noteworthy contributions were made by Sandra Egan, Nanette Moffa, Lori Gorman, Bill Vales, and Elliott Hendrickson.

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Waldenmarthranesgate 84/B-86
Oslo 1, Norway
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1211 Geneva 26, Switzerland
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ZURICH
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Telephone: 01 60 35 66 Telex: 56059

ITALY

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