digital INTEROFFICE MEMORANDUM

NO: RC:69:27 DATE: March 4, 1969

SUBJECT: Proposed PDP-11 Re-Organization

TO: Design Review Committee FROM: R. Cady

Attached is the proposed PDP-11 re-organization.

jq

PROPOSED PDP-11 RE-ORGANIZATION

Machine Organization

Eight hardware registers:

Accumulator	A
Program Counter	P
Priority and condition codes	C
Stack pointer	XS
Index Registers	X1
	X2
	X3
	X4

Addressing Modes

	bytes	not deferred	deferred
Immediate	3	EFA = next location	EFA = (Next location)
Relative to P	2	EFA = (P) +OFFSET	EFA = ((P) +OFFSET)
Page Zero	2	EFA = ØØOFFSET$_{16}$	EFA = (ØØOFFSET$_{16}$)
Indexed	2	EFA = (XR) +OFFSET	EFA = ((XR) +OFFSET)

NOTES:

OFFSET is an 8 bit quantity (7 bits magnitude, 1 bit sign) and is the second byte of the two byte instruction.

For Page Zero references, OFFSET is considered an 8 bit quantity which forms the least significant byte of an address of which the most significant byte is all zeroes. Page zero is thus 256 bytes long.

XR refers to the index register which is desired to be used in the address computation. It may be X1, X2, X3, X4, or XS.

The internal registers of the processor may be explicitly addressed by external devices, but may not be explicitly addressed in a program execution of a memory reference instruction.

I - Memory Reference (2 or 3 byte)

LDB
LDW
STB
STW
ADB
ADW
CPB
CPW
AND
INC
JMP (JMP immediate (1 byte) = NOP)
JSR (JSR immediate (1 byte) = TRAP to LOC #?) for debug

II - Operate group (1 byte)

IAC
CMA
NEG
CLA
CML
CCC
RAR
RAL

+1 → AC
-1 → AC
} lost.

III - Add to register (2 byte) (second byte is signed byte which is added to the register specified)

ATX1
ATX2
ATX3
ATX4
ATXS
~~ATA~~ Will not implement (ADB immediate)
ATC

IV - External transfer (2 byte) (second byte is the device select)

XTR

V - Transfer to/from register (using accumulator) (1 byte)

TTX1	TFX1
TTX2	TFX2
TTX3	TFX3
TTX4	TFX4
TTXS	TFXS
TTP	TFP
TTC	TFC
TTA	TFA - Use to swap bytes in accumulator.

Typical execution:

TTX1 = A → X1

TFX1 = X1 → A

at expense of inclusive or.

VI - Push/Pop group (1 byte)

PUX1	POX1
PUX2	POX2
PUX3	POX3
PUX4	POX4
PUXS	POXS
PUP	POP
PUC	POC
PUA	POA

Typical Execution:

PUX1 = (X1) (S), (S) +2 S

POX1 = (S) -2 S, ((S)) X1

VII - Conditional Jump (2 byte) (second byte is signed byte which is added to P if test is true)

JCT	Z,N,L (logical or)	may be micro-programmed
JCF	Z,N,L (logical and)	may be micro-programmed
JFS	I/O Flag set	
JFR	I/O Flag reset	