ADVANCE COPY
THIS DESCRIPTION IS PRELIMINARY AND
SUBJECT TO CHANGE WITHOUT NOTICE.

IDENTIFICATION

PRODUCT CODE:	MAINDEC-12-D8CA-D-(D)
PRODUCT NAME:	KW12-REAL TIME CLOCK DIAGNOSTIC
DATE CREATED:	OCTOBER 1, 1969
AUTHOR:	JAMES KELLY STEVE TEICHER

Mnemonic : KW12TST

ADVANCE COPY
THIS DESCRIPTION IS PRELIMINARY AND
SUBJECT TO CHANGE WITHOUT NOTICE.

ABSTRACT

The KW-12 diagnostic program verifies the correct operation of the buffer preset register, the clock counter register, the clock control register, the clock enable register, the IO bus interfare, and the clock input channels. The test once started halts, only in case of an error or operator intervention.

REQUIREMENTS

Storage

Locations 0--3200 in bank 0 are utilized.

Equipment

PDP-12--with KW-12 option

Program Loading

a) If the Binary Loader is in memory, proceed to step b. Otherwise, load the binary loader into memory.

b) Set Left Switches=7777_8

c) Set: Right Switches=4000_8

d) Press IO preset and start Left Switches

e) Turn Reader on

General Description

The ability to transfer all numbers between the AC and the clock registers is thoroughly tested. All modes of the KW-12 operation are tested. The clock counter is operated at the five crystal controlled rates and at the rate of input channel 1. External KW-12 inputs are tested with the selector switch turned to line frequency. There are four test options of which one is to eliminate testing of the AD-12 fast SAM instruction which is affected by mode bit Ø of the KW-12.

Operation Procedure

a) Load programs with binary loader

b) Select option by setting right switches as follows:

1) Bit Ø (1) suppress test completion alarm
2) Bit 5 (1) suppress print pass completion printing
3) Bit 8 (1) suppress test of AD-12 fast SAM instruction

Normal operation on a PDP-12C is with right switches=ØØØØ

c) Set Selector switches on KW-12 panels to line frequency.

d) Set Left Switches=Ø2ØØ

e) If AD-12 fast SAM instructions is to be tested, set KNOB Ø to extreme counterclockwise and KNOB 1 to extreme clockwise.

f) Set mode key on PDP-8 mode, press ID preset, and start Left Switches.

Test Operation

After start; at location Ø2ØØ the program performs 39 tests per, pass, halting only in the case of an error. At the end of each pass, which requires approximately 30 seconds, the letter K is typed on the teletype unless suppressed by the right switch setting. If after 30 seconds the program fails to complete a pass the operator should stop the computer and check the location counter against the program listing as the program is in a counting loop which indicates a failure of the counter, the time house, or an external input channel.

After 16 complete passes of the test program, the program will cease testing and sound a distinctive whistle on the PDP-12 speaker, unless this mode is suppressed by the right switch setting.

Options:

There are 4 options available selected by the right switches.

Right Switch Setting	Description of Option
ØØØØ	Tests AD-12 fast SAM prints letter K after every pass of program after 16 passes of program quits test and sounds completion alarm on speaker
1ØØØ	Supresses test of AD-12 fast SAM
2ØØØ	Supresses typing of K after every pass of program
4ØØØ	Allows program to repeat indefinitely

All combinations of options are legal.

Errors

a) Error Halts--If the computer halts check the listing for explanation of the halt.

b) Failure of the counter time base or an external input channel can cause the program to loop indefinitely through a 2 or 3 instruction loop. If the program fails to complete a pass in approximately 30 seconds, the operator should stop the machine and check the location counter against the listing to determine if the program is waiting for a counter overflow or external input channel.

Manual Test

When the computer is halted, the run light is out, it is possible to check the advancement of the clock counter manually as follows:

a) Set mode Switch to PDP-8 mode

b) Set Left Switches equal to 6137

c) Press IO preset and DO alternately

After every press of the DO Switch, the clock counter will be read into the AD? Each press of IO preset will clear the AC and advance the clock counter one or two counts. Therefore, by noting the reading of the AC after each DO, the fact that the clock counter advanced may be ascertained.

TESTS

The following--tests are performed in the order listed below:

Test #	Description
TST 2Ø	Does AC change after a transfer to the Buffer Preset Register?
TST 21	Does the Buffer Preset Register Jam into the AC?
TST 22	Can the Buffer Preset Register be cleared to ØØØØ?
TST 23	Do all numbers transfer between the AC and the Buffer Preset Register?
TST 24	Do random numbers transfer between the AC and the Buffer Preset Register?
TST 25	Does reading the Buffer Preset Register change its content?
TST 26	Can the Buffer Preset Register gate perform at maximum speed?
TST 27	Can the Buffer Preset Register survive checkerboard patterns?
TST 28	Can the Buffer Preset Register handle random complement patterns?
TST 29	Does executing the CLEN instruction affect the AC?
TST 3Ø	Does the Buffer Preset Register change after a transfer to the clock counter register?
TST 31	Can the clock counter be read using the 6137 instruction?
TST 32	Can the clock counter be cleared?
TST 33	Do all numbers transfer between the Buffer Preset Register and the clock counter register?
TST 34	Do random numbers transfer between the Buffer Preset Register and the clock counter register?
TST 35	Does reading the clock counter register change its CONTENTS?

TST 37	Can the Buffer Preset Register be ORED into the clock counter register?
TST 38	Can the clock counter register be loaded with mode 2(Ø) in error?
TST 39	Can the clock counter be loaded with mode 1 (1) in error?
TEST 3Ø	Does rapid actuating of the mode gates affect counter?
TEST 31	This is a general gate shaking test of the mode flip flops.
TEST 32	Does mode bit 2 changing from 1 Ø clear the clock counter register?
TST 4Ø	Does the overflow of the clock counter register set the overflow flip flop?
TST 41A	This is a general test of the overflow flip flop.
TEST 4	This is a series of tests. Labeled TST 41 through TST 49B that check each bit of the counter.
TEST 5	Does the clock counter register count at all rates?
ITSTØ1	Does input channel 1 cause a proper interrupt?
INPTØ1	This is a simulated input test for channel 3.
ITSTØ2	Does input channel 2 cause a proper interrupt?
ITSTØ3	Does input channel 3 cause a proper interrupt?
INPTØ2	This is a simulated input test for channel 2.
INPTØ3	This is a simulated input test for channel 3.
INPTØ4	This is a test of the external inputs for channels 1, 2, 3 which includes a test of the M503 schmitt triggers.
TSM	This is a test of the affect of mode bit Ø(1) on the FAST sample instruction.
TSM1	Is the fast SAM instruction affected by mode bit Ø(Ø)?
TCNT1	Does IO preset clear the rate bits?

TCNT2	Does IO preset clear the overflow flip flop, the enable flip flops, and the mode flip flop?
TMOD1	Does Mode bit 1(1) work properly?
TMOD3	Does mode bit 1(1) and mode bit 2 (1) work properly?

clv

```
                        /MAINDEC 12-D0CA-D-(D)
                        /SUPER KILLER FOR CLOCKS

                6131    CLBS=6131
                6132    CLLR=6132
                6133    CLAB=6133                       /AC TO BUFFER PRESET REGISTER
                6134    CLEN=6134
                6135    CLSA=6135
                6136    CLBA=6136                       /BUFFER PRESET REGISTER TO AC
                6137    CLCA=6137
                        *1
02 1    5223            JMP I   RETURN

                0020    *20
0020    0022    SEND,   0
0021    0000    RXED,   0
0022    0010    REGA,   10
0023    0100    K0100,  0100
0024    0200    K0200,  0200

0025    7777    M0001,  -1
0026    0001    K0001,  1
0027    7776    M0002,  -2

0030    0003    K0003,  0003
0031    7774    M0004,  -4
0032    0007    K0007,  0007
0033    0017    K0017,  0017
0034    0037    K0037,  0037
0035    0077    K0077,  0077

0036    0177    K0177,  0177
0037    0377    K0377,  0377
0040    0777    K0777,  0777
0041    1777    K1777,  1777
0042    3777    K3777,  3777
0043    7777    K7777,  7777

0044    7770    M0010,  -10
0045    7760    M0020,  -20
0046    7740    M0040,  -40
0047    7700    M0100,  -100
0050    7600    M0200,  -200
0051    7400    M0400,  -0400

0052    7000    M1000,  -1000
0053    6000    M2000,  -2000
0054    4000    M4000,  -4000
0055    4000    K4000,  4000
```

ADVANCE COPY

THIS DESCRIPTION IS PRELIMINARY AND SUBJECT TO CHANGE WITHOUT NOTICE.

```
                RANDOM,
                        TAD     RNA
                        TAD     RNB
                        TAD     RNC
                        DCA     RNA
                        RAL
                        TAD     RNA
                        TAD     RNB
                        TAD     RNC
                        DCA     RNB
                        RAL
                        TAD     RNA
                        TAD     RNB
                        TAD     RNC
                        DCA     RNC
                        RAL
                        TAD     RNA
                        DCA     RNA
                        TAD     RNA
                        JMP I   RANDOM
```

```
                    RM4,    2003
                    RM5,    7150
                    RM6,    2465
                    KZZZZ,  0200
                    KZZZZ,  0302
                    KZZZZ,  0702
0113  1674          PNT4,   LOC4
0114  1636          PNT3,   LOC3
0115  1634          PNT2,   LOC2
0116  0000          RETURN, 0
0117  0000          K1111,  1111
0120  5252          K5252,  5252
0121  2002          K2002,  2002
0122  3003          K3333,  3333
0123  7777          K7777,  7777
0124  4100          K4111,  4111
0125  5000          K5555,  5555
0126  0200          K0202,  0202
0127  0020          K0020,  0020
0130  0353          TST27A, TST27
0131  0700          TST35A, TST35
0132  0033          TST32A, TST32
0133  1011          TST38A, TST38
0134  0014          K0013,  0013
0135  0004          K0004,  0004
0136  2075          PNT0,   LOC0
0137  2105          PNT1,   LOC1
0140  2121          PNT5,   LOC5
0141  2461          PNT6,   LOC6
0142  2172          PNT7,   LOC7
0143  2202          PNT8,   LOC8
0144  1750          TST49X, TST49A
0145  1717          TST49Y, TST49+13
0146  0010          K0010,  0010
0147  0040          K0040,  0040
0150  0400          K0400,  0400
0151  0500          K0500,  0500
0152  6000          K6000,  6000
0153  5555          K5555,  5555
0154  2015          IPT04,  INPT04
0155  2400          TSMA,   TSM
0156  2473          TSM1A,  TSM1
0157  2044          TCNT2A, TCNT2
0160  1410          TST41B, TST41A
0161  0600          K0600,  0600
0162  2106          INT01,  INPT01
0163  0002          K0002,  0002
0164  3527          COUNTX, COUNT
0165  1062          TST31X, TST31
      0177          .177
0177  7414                  SKP
```

```
                *2??
                /MAJOR START B ??DE, ACR?
                /TEST 2:  TEST BUFFER AND PRESET REGISTER DATA INTERCHANGE
                /CLAB=6133  AC TO CLOCK PRESET REGISTER
                /CLBA=6136  CLOCK PRESET REGISTER TO AC
                /DOES AC CHANGE AFTER A TRANSFER TO BUFFER REG?
????  ????      DCA I DCNTX
???1  7???    TST2?,  CLA CLA
????  1???            TAD     REGA            /GET A NUMBER-BINARY UPCOUNT SEQUENCE 0 THRU 7777
????  6133            CLAB                    /LOAD BUFFER
????  3???            DCA     RXED            /STORE WHAT WAS LEFT IN AC
????  1???            TAD     RXED            /FETCH IT
????  7041            CIA                     /INVERT CONTENTS OF AC
????  1???            TAD     REGA            /SUBTRACT SEND
????  7???            SZA CLA                 /EQUAL?
????  7???            HLT                     /NO HALT CLAB CHANGED AC, EXAMINE CELL 22 FOR TEST NUMBER
????  2???            ISZ     REGA            /CHANGE TEST NUMBER
????  5???            JMP     TST2?+1         /DO TEST 4096 TIMES

                /DOES BUFFER DATA JAM INTO THE AC

????  7???    TST21,  CLA CLL
????  3???            DCA     SEND            /0 SEND REG
????  6???            CLAB                    /SET BUFFER AND PRESET REGISTER TO 0000
????  7???            CLA CMA                 /SET AC TO 7777
????  6???            CLBA                    /JAM BUFFER PRESET (0000) OVER AC (7777
????  3???            DCA     RXED            /SAVE AC
????  1???            TAD     RXED            /RESTORE AC
????  7???            SZA CLA                 /DID AC BECOME (0000)?
????  7???            HLT                     /CLBA FAILED TO CLEAR THE AC
????  2???            ISZ     REGA
????  5???            JMP     TST21           /DO TEST 4096 TIMES

                /DOES SIGNAL CLR BUF FUNCTION

????  7???    TST22,  CLA CMA
????  6???            CLAB                    /SET BUFF=7777
????  7???            CLA CLL                 /CLEAR AC
????  6???            CLAB                    /LOAD BUFFER TO ALL ZEROS
????  3???            DCA     SEND            /SAVE AC
????  6???            CLBA                    /READ BUFFER AND PRESET REGISTER
????  3???            DCA     RXED            /SAVE TEST VALUE
????  1???            TAD     RXED            /RESTORE IT
????  7???            SZA CLA                 /DID BUFFER AND PRESET REGISTER GET CLEARED BY CLR CNT?
????  7???            HLT                     /CLR BUF FAILED TO CLEAR THE BUFFER
????  2???            ISZ     REGA            /
????  5???            JMP     TST22           /DO TEST 4096 TIMES
```

```
                        /DO ALL NUMBERS TRANSFER BETWEEN AC AND BUFFER PROPERLY

2243  7300      TST23,  CLA CLL
2244  3022              DCA     SEND            /0 SEND REG
2245  1022              TAD     SEND            /GET TEST NUMBER
2246  6133              CLAB                    /SEND IT
2247  7200              CLA
2250  6136              CLBA                    /RETRIEVE IT
2251  3021              DCA     RXED            /SAVE IT
2252  1021              TAD     RXED            /RESTORE IT
2253  7041              CIA                     /COMPLEMENT
2254  1022              TAD     SEND            /ADD TEST NUMBER
2255  7540              SZA CLA                 /WERE THEY EQUAL?
2256  7402              HLT                     /AC = BUFFER TO AC DATA TRANSFER FAILED
2257  2022              ISZ     SEND            /INCREMENT TEST NUMBER
2260  5245              JMP     TST23+2         /DO TEST 4096 TIMES

                        /DO RANDOM NUMBERS TRANSFER BETWEEN AC AND BUFFER PROPERLY

2261  4256      TST24,  JMS     RANDOM          /LOAD BUFFER AND PRESET REGISTER WITH A RANDOM NUMBER
2262  3022              DCA     SEND            /SAVE IT
2263  1022              TAD     SEND            /RESTORE IT
2264  6133              CLAB                    /SEND IT
2265  4256              JMS     RANDOM          /LOAD THE AC WITH A RANDOM NUMBER
2266  6136              CLBA                    /READ BACK RANDOM NUMBER FROM BUFFER PRESET REGISTER
2267  3021              DCA     RXED            /SAVE TEST RETURN
2270  1021              TAD     RXED            /RESTORE IT
2271  7041              CIA                     /COMPLEMENT
2272  1022              TAD     SEND            /SUBTRACT TEST NUMBER
2273  7540              SZA CLA                 /EQUAL?
2274  7402              HLT                     /AC = BUFFER - AC DATA INTERCHANGE FAILED
2275  2022              ISZ     REGA
2276  5261              JMP     TST24           /DO TEST 4096 TIMES
```

```
                        /DOES READING THE BUFFER CHANGE ITS CONTENTS

                TST25,  JMS     RANDOM          /GET RANDOM NUMBER
                        DCA     SEND            /SAVE IT
                        TAD     SEND            /RESTORE IT
                        CLAB                    /SEND IT
                        JMS     RANDOM          /LOAD AC WITH A RANDOM NUMBER
                        CLBA                    /BRING BACK TEST NUMBER
                        JMS     RANDOM          /LOAD AC WITH A RANDOM NUMBER
                        CLBA                    /READ BUFFER AGAIN
                        DCA     RXED            /SAVE TEST VALUE
                        TAD     RXED            /RESTORE IT
                        CIA                     /COMPLEMENT
                        TAD     SEND            /SUBTRACT TEST NUMBER
                        SZA CLA                 /EQUAL
                        HLT                     /CLBA CHANGED THE CONTENTS OF THE BUFFER
                        ISZ     REGA
                        JMP     TST25           /DO TEST 4096 TIMES

                        /CAN THE GATES FUNCTION AT HIGH SPEED

                TST26,  CLA CLL
                        DCA     SEND
                        TAD     SEND
                        CLAB
                        CLBA
                        CLAB
                        CLBA
                        CLAB
                        CLBA
                        CLAB
                        CLBA
                        CLAB
                        CLBA
                        CLAB
                        CLBA
                        CLAB
                        CLBA
                        CLAB
                        CLBA
                        CLAB

                        CLBA
                        CLAB
                        CLBA
                        CLAB
                        CLBA
                        DCA     RXED
                        TAD     RXED
                        CIA
                        TAD     SEND
                        SZA CLA
                        HLT                     /BUF FAILED TO TOGGLE AT HIGH SPEED
                        ISZ     SEND            /DO TEST 4096 TIMES
                        JMP     TST26+2
```

D8CA - D-(D)

/CAN THE BUFFER SURVIVE CHECKERBOARD

```
[illegible] 7540    TST27,  CLA CLL
[illegible] 3[illegible]            TAD     KDEDE
[illegible] 3[illegible]            DCA     SEND            /SAVE TEST PATTERN
[illegible] 1[illegible]            TAD     SEND            /RESTORE IT
[illegible] 6133                    CLAB
[illegible] 6135                    CLBA
[illegible] 7[illegible]            CMA
[illegible] 6133                    CLAB
[illegible] 6135                    CLBA
[illegible] 7[illegible]            CMA
2372 6133                           CLAB
2373 6135                           CLBA
2374 7040                           CMA
2375 6133                           CLAB
2376 6135                           CLBA
2377 7040                           CMA
2400 6133                           CLAB
2401 6135                           CLBA
2402 7040                           CMA
2403 6133                           CLAB
2404 6135                           CLBA
2405 7040                           CMA
2406 6133                           CLAB
2407 6135                           CLBA
2410 7040                           CMA
2411 6133                           CLAB
2412 6135                           CLBA
2413 7040                           CMA
2414 6133                           CLAB
2415 6135                           CLBA
2416 7040                           CMA
2417 6133                           CLAB
2420 6135                           CLBA
2421 7040                           CMA
2422 6133                           CLAB
2423 6135                           CLBA
2424 7040                           CMA
2425 6133                           CLAB
2426 6135                           CLBA
2427 7040                           CMA
2430 3021           RXED            /SAVE FINAL PATTERN
2431 1421           RXED            /RESTORE IT
2432 7041                           CIA                     /COMPLEMENT
2433 1020           SEND            TAD                     /SUBTRACT TEST PATTERN
2434 7040                           SZA CLA                 /EQUAL?
2435 7402                           HLT                     /BUFFER FAILED CHECKBOARD TEST
2436 2022                           ISZ     REGA            /DO TEST 4096 TIMES
2437 5325                           JMP I   TST27A          /CROSS PAGE REF TO TST27
```

```
                    /
                    /CAN THE BUFFER SURVIVE RANDOM COMPLEMENT PATTERNS
                    /
                    TS128,  CLA          RANDOM          /GENERATE A RANDOM NUMBER
                            DCA          SEND            /SAVE IT
                            TAD          SEND            /RESTORE IT
                            CLAB
                            CLBA
                            CMA
                            CLAB
                            CLBA
                            CMA
                            CLAB
                            CLBA
                            CMA
                            CLAB
                            CLBA
                            CMA
                            CLAB
                            CLBA
                            CMA
                            CLAB
                            CLBA
                            CMA
                            CLAB
                            CLBA
                            CMA
                            CLAB
                            CLBA
                            CMA
                            CLAB
                            CLBA
                            CMA
                            CLAB
                            CLBA
                            CMA
                            CLAB
                            CLBA
                            CMA
                            DCA          RXED            /SAVE FINAL PATTERN
                            TAD          RXED            /RESTORE IT
                            CIA                          /COMPLEMENT
                            TAD          SEND            /SUBTRACT TEST PATTERN
                            SZA CLA                      /EQUAL?
                            HLT                          /BUFFER FAILED RANDOM COMPLEMENT PATTERN
                            ISZ          NEGA
                            JMP          TS128           /DO TEST 4096 TIMES
```

```
                    /
                    /CLEN=6134 AC TO CLOCK ENABLE REGISTER
                    / DOES CLEN AFFECT THE AC
                    /
0520 7300   TST29,  CLL CLA
0521 3420           DCA     SEND            /CLEAR SEND REG
0522 1420           TAD     SEND            /RESTORE TEST NUMBER
0523 6134           CLEN                    /DOES CLEN AFFECT AC
0524 3461           DCA     RXED            /SAVE AC
0525 1461           TAD     RXED            /RESTORE IT
0526 7041           CIA                     /COMPLEMENT
0527 1420           TAD     SEND            /SUBTRACT TEST NUMBER
0530 7040           SZA CLA                 /EQUAL?
0531 7402           HLT                     /AC TO CLOCK ENABLE REG CHANGED AC
0532 2420           ISZ     SEND            /INCREMENT TEST NUMBER
0533 5322           JMP     TST29+2
                    /
                    /TEST33: PRESET REGISTER AND COUNTER DATA INTERCHANGE
                    /CLSA=6135 STATUS REGISTER TO AC
                    /CLLR=6132 AC TO CLOCK CONTROL REGISTER


                    /DOES BUFFER CHANGE AFTER A TRANSFER TO THE COUNTER

0534 7300   TST30,  CLL CLA
0535 3420           DCA     SEND            /CLEAR SEND REG
0536 6135           CLSA                    /CLEAR STATUS
0537 7300           CLA CLL
0540 1420           TAD     SEND            /RESTORE TEST NUMBER
0541 6133           CLAB                    /LOAD BUFFER PRESET REGISTER WITH A BINARY UPCOUNT NUMBER
0542 7300           CLA CLL
0543 6132           CLLR                    /STOP CLOCK, SET ALL MODES=0
0544 1423           TAD     K2100           /MODE CONTROL REG BIT 2=1
0545 6132           CLLR                    /SET MODE 2, ENABLING CLR LOAD CNT
0546 7300           CLA
0547 1425           TAD     K2200           /AC BIT 4=1, SIMULATE CLR OFLOW ON 6134
0550 6134           CLEN                    /TRANSER PRESET COUNT TO CLOCK COUNTER
0551 6136           CLBA                    /READ THE BUFFER
0552 3461           DCA     RXED            /SAVE IT
0553 1461           TAD     RXED            /RESTORE IT
0554 7041           CIA                     /COMPLEMENT
0555 1420           TAD     SEND            /SUBTRACT TEST NUMBER
0556 7040           SZA CLA                 /EQUAL?
0557 7402           HLT                     /TRANSFER FROM BUFFER TO COUNTER CHANGES BUFFER
0560 2420           ISZ     SEND            /INCREMENT TEST NUMBER
0561 5330           JMP     TST30+2
```

```
                /DOES OR ENTER DATA JAM THE BUFFER AND AC
                /CLOCK=6137 CLOCK COUNTER TO PRESET REGISTER, THEN PRESET REG TO AC

0012  6133     TST31,  CLSA                    /CLEAR STATUS
0013  7200             CLA CLL
0014  6136             CLAB                    /LOAD BUFFER TO 0000
0015  6132             CLLR                    /STOP CLOCK, SET ALL MODES=0
0016  1265             TAD     K0100           /SET AC 05=1
0017  6132             CLLR                    /SET MODE 2=1, THEREBY CLEARING CLOCK COUNTER
0020  6134             CLEN                    /ENABLE INTERRUPT ON OVERFLOW
0021  7240             CLA CMA                 /SET AC 7777
0022  6136             CLAB                    /SET BUFFER 7777 AND AC
0023  6137             CLCA                    /READ COUNTER
0024  3261             DCA     RXED            /SAVE COUNT
0025  1261             TAD     RXED            /RESTORE IT
0026  7440             SZA CLA                 /ZERO?
0027  7402             HLT                     /COUNTER FAILED TO JAM 0000 INTO 7777
0030  2262             ISZ     REGA            /DO TEST 4096 TIMES
0031  5232             JMP I   TST31X          /CROSS PAGE REFERENCE TO TST31
0032  3264             DCA     SEND            /ZERO SEND FOR NEXT TEST
                /DOES SIGNAL CLR CNT WORK
0033  6133     TST32,  CLSA                    /CLEAR STATUS
0034  7053             CLA CMA CLL RAR         /SET AC=3777
0035  6136             CLAB                    /SET BUFFER TO 3777 (USE 3777 SO WE DON'T SET OVERFLOW FLOP)
0036  7200             CLA CLL
0037  1265             TAD     K0200           /ENABLE LOAD COUNT GATES
0040  6134             CLEN                    /LOAD COUNTER TO 3777 (GENERATE LOAD CNT)
0041  7200             CLA CLL
0042  6132             CLLR                    /ZERO MODE 2
0043  1265             TAD     K0100           /SET AC 05=1
0044  6132             CLLR                    /SET MODE 2, THEREBY GENERATING "CLC CLR CNT"
0045  7200             CLA CLL
0046  6137             CLCA                    /READ THE COUNTER
0047  3261             DCA     RXED            /SAVE IT
0050  1261             TAD     RXED            /RESTORE IT
0051  7440             SZA CLA                 /ZERO?
0052  7402             HLT                     /CLR CNT FAILED TO CLEAR THE COUNTER FROM 3777 TO 0000
0053  2262             ISZ     REGA            /DO TEST 4096 TIMES
0054  5233             JMP I   TST32A          /INDIRECT REFERENCE TO TST32
```

D8CA-D-(D)


```
                        /ALL NUMBERS TRANSFER BETWEEN THE BUFFER AND COUNTER

2365  6225  TST33,  CLSA                    /CLEAR STATUS
2366  7300          CLA CLL
2367  1247          TAD     SEND            /LOAD AC WITH TEST NUMBER
2370  6233          CLAB                    /SET BUFFER TO TEST NUMBER
2371  7300          CLA CLL
2372  6132          CLLR                    /STOP CLOCK, SET ALL MODES=0
2373  1223          TAD     K2100           /SET AC 05=1
2374  6132          CLLR                    /GENERATE "CLR CNT"
2375  7200          CLA
2376  1224          TAD     K0200           /SET AC 04=1
2377  6134          CLEN                    /GENERATE "LOAD CNT"
2400  6137          CLCA                    /COUNTER TO AC
2401  3021          DCA     RXED            /SAVE IT
2402  1021          TAD     RXED            /RESTORE IT
2403  7041          CIA                     /COMPLEMENT
2404  1247          TAD     SEND            /SUBTRACT TEST NUMBER
2405  7040          SZA CLA                 /EQUAL?
2406  7402          HLT                     /BUFFER TO COUNTER DATA INTERCHANGE FAILED
2407  2246          ISZ     SEND            /INCREMENT TEST NUMBER
2410  5225          JMP     TST33

                        /DO RANDOM NUMBERS TRANSFER BETWEEN BUFFER AND COUNTER

2411  4036  TST34,  JMS     RANDOM          /GET RANDOM NUMBER
2412  6133          CLAB                    /LOAD BUFFER RANDOM
2413  3022          DCA     SEND            /SAVE TEST NUMBER
2414  6135          CLSA                    /CLEAR CLOCK STATUS
2415  7200          CLA                     /CLEAR AC
2416  6132          CLLR                    /STOP CLOCK, SET ALL MODES=0
2417  1223          TAD     K0100           /SET AC 05=1
2420  6132          CLLR                    /GENERATE "CLR CNT"
2421  7200          CLA
2422  1224          TAD     K0200           /SET AC 04=1
2423  6134          CLEN                    /GENERATE "LOAD CNT"
2424  4036          JMS     RANDOM          /GET RANDOM NUMBER
2425  6133          CLAB                    /LOAD BUFFER RANDOM
2426  4036          JMS     RANDOM          /LOAD AC RANDOM
2427  6137          CLCA                    /READ COUNTER
2430  3021          DCA     RXED            /SAVE TEST VALUE
2431  1021          TAD     RXED            /RESTORE IT
2432  7041          CIA                     /COMPLEMENT
2433  1222          TAD     SEND            /SUBTRACT TEST NUMBER
2434  7040          SZA CLA                 /EQUAL?
2435  7402          HLT                     /BUFFER TO COUNTER RANDOM DATA INTERCHANGE FAILED
2436  2222          ISZ     REGA            /DO TEST 4096 TIMES
2437  5211          JMP     TST34
```

12-08CA-D-(D)


```
                    /DOES READING THE COUNTER CHANGE ITS STATE,

0711  4035  TST35,  JMS     RANDOM          /GET RANDOM TEST NUMBER
0712  6133          CLAB                    /SEND IT TO BUFFER
0713  3021          DCA     SEND            /SAVE IT
0714  6132          CLLR                    /STOP CLOCK, SET ALL MODES=0
0715  1023          TAD     K0200           /SET AC 05=1
0716  6132          CLLR                    /GENERATE "CLR CNT"
0717  6135          CLSA                    /CLEAR CLOCK STATUS
0720  7200          CLA
0721  1025          TAD     K0200           /SET AC 04=1
0722  6134          CLEN                    /GENERATE "LOAD CNT"
0723  4035          JMS     RANDOM          /GET RANDOM NUMBER
0724  6133          CLAB                    /SEND IT TO BUFFER
0725  4035          JMS     RANDOM          /GET RANDOM NUMBER
0726  6137          CLCA                    /READ CLOCK COUNTER
0727  4035          JMS     RANDOM          /GET RANDOM NUMBER
0730  6133          CLAB                    /SEND IT TO BUFFER
0731  4035          JMS     RANDOM          /GET RANDOM NUMBER
0732  6137          CLCA                    /READ CLOCK COUNTER
0733  3021          DCA     RXED            /SAVE IT
0734  1021          TAD     RXED            /RESTORE IT
0735  7041          CIA                     /COMPLEMENT
0736  1020          TAD     SEND            /SUBTRACT TEST NUMBER
0737  7040          SZA CLA                 /EQUAL?
0740  7402          HLT                     /(CLCA) READ THE COUNTER CHANGES THE COUNTERS STATE
0741  2022          ISZ     REGA            /DO TEST 4095 TIMES
0742  5335          JMP I   TST35A          /CROSS PAGE REF TO TST35

                    /CAN THE BUF TO COUNTER AND COUNTER TO BUF FUNCTION AT HIGH SPEED

0743  4035  TST36,  JMS     RANDOM          /GET RANDOM NUMBER
0744  6133          CLAB                    /SEND IT TO BUFFER
0745  3020          DCA     SEND            /SAVE IT
0746  7200          CLA
0747  6132          CLLR                    /STOP CLOCK
0750  1023          TAD     K0100           /SET AC 05=1
0751  6132          CLLR                    /GENERATE "CLR CNT"
0752  6135          CLSA                    /CLEAR CLOCK STATUS
0753  7200          CLA
0754  1025          TAD     K0200           /SET AC 04=1

0755  6134          CLEN                    /GENERATE "LOAD CNT"
0756  6137          CLCA                    /READ COUNTER
0757  2022          ISZ     REGA            /DO THIS 4096 TIMES
0760  5343          JMP     TST36+3
0761  3021          DCA     RXED            /SAVE FINAL NUMBER
0762  1021          TAD     RXED            /RESTORE IT
0763  7041          CIA                     /COMPLEMENT
0764  1020          TAD     SEND            /SUBTRACT TEST NUMBER
0765  7040          SZA CLA                 /EQUAL?
0766  7402          HLT                     /THE BUFFER COUNTER BUFFER DATA INTERCHANGE FAILED AT HIGHSPEED
```

```
                        /DOES (LOAD CNT) PERFORM LOGIC OR

                TST37,  CLA CLL
                        CLLR
                        TAD     K0100           /SET AC 05=1
                        CLLR                    /GENERATE "CLR CNT"
                        CLSA                    /CLEAR CLOCK STATUS
                        JMS     RANDOM          /GET RANDOM TEST NUMBER
                        CLAB                    /LOAD BUFFER WITH A RANDOM NUMBER
                        DCA     SEND            /SAVE IT
                        TAD     K0200           /SET AC 04=1
                        CLEN                    /LOAD COUNTER FROM THE BUFFER REGISTER: GENERATE "LOAD CNT"
                        CLA CLL
                        TAD     SEND            /GET TEST NUMBER
                        CMA                     /COMPLEMENT
                        CLAB                    /LOAD BUFFER WITH THE COMPLEMENT OF THE PREVIOUS NUMBER
                        CLA CLL
                        TAD     K0200           /SET AC 04=1
                        CLEN                    /LOAD COUNTER (OR) IN COMPLEMENT OF THE FIRST NUMBER
                        CLCA                    /READ COUNTER.
                        DCA     RXED            /SAVE IT
                        TAD     RXED            /RESTORE IT
                        CMA                     /CONVERT TO ALL ZEROS FOR TESTING
                        SZA CLA                 /ZERO?
                        HLT                     /THE (LOAD CNT) SIGNAL FAILED TO "OR" DATA INTO COUNTER
                        ISZ     REGA            /DO TEST 4096 TIMES
                        JMP I   TST37X          /INDIRECT REF TO TST37
                        SKP
                TST37X, TST37                   /DEF, OF TST37X

                        /TEST LOAD CNT GENERATION GATES (CLR CLOCK RATE) MODE 2 (0)

                TST38,  CLA
                        CLAB                    /CLEAR BUFFER
                        CLLR                    /CLEAR ALL MODES
                        TAD     K0130           /SET AC 05=1
                        CLLR                    /GEN. "CLR CNT"
                        CLSA                    /CLEAR STATUS
                        JMS     RANDOM          /GET RANDOM NUMBER
                        CLAB                    /SEND IT TO BUFFER
                        DCA     SEND            /SAVE IT
                        CLLR                    /STOP CLOCK, SET ALL MODES=0
                        TAD     K0130           /SET AC 05=1
                        CLLR                    /GENERATE "CLR CNT"
                        CLA
                        CLLR                    /SET ALL MODES=0
                        TAD     K0200           /SET AC 04=1
                        CLEN                    /TRY TO GENERATE "LOAD CNT"
                        CLCA                    /GET COUNTER
                        DCA     RXED            /SAVE IT
                        TAD     RXED            /RESTORE IT
                        SZA CLA                 /WAS IT ZERO?
                        HLT                     /LOAD CNT GATES FUNCTIONED WITH MODE 2=0 IN ERROR
                        ISZ     REGA            /DO TEST 4096 TIMES
```

```
                        /TEST LOAD CNT GENERATION GATES (CLR CLOCK RATE) MODE 1(1)

1[illegible]  [illegible]  TST59,  JMS     RANDOM          /GET RANDOM NUMBER
1[illegible]  [illegible]          CLAB                    /SEND IT TO BUFFER
1[illegible]  [illegible]          DCA     SEND            /SAVE IT
1[illegible]  1[illegible]          TAD     K0000           /SET AC 04,05=1
1[illegible]  6[illegible]          CLLR                    /GENERATE "CLR CNT", SET MODE 1 AND 2 =1
1[illegible]  6[illegible]          CLSA                    /CLEAR CLOCK STATUS
1[illegible]  7[illegible]          CLA                     /CLEAR AC
1[illegible]  1[illegible]          TAD     K0200           /SET AC 04=1
1[illegible]  6[illegible]          CLEA                    /TRY TO GENERATE "LOAD CNT"
1[illegible]  6[illegible]          CLCA                    /READ COUNTER
1[illegible]  3[illegible]          DCA     RXED            /SAVE TEST VALUE
1[illegible]  1[illegible]          TAD     RXED            /RESTORE IT
1[illegible]  7040                  SZA CLA                 /ZERO?
1[illegible]  7402                  HLT                     /LOAD CNT GATES FUNCTIONED WITH MODE 1=1 IN ERROR
1[illegible]  2[illegible]          ISZ     REGA            /DO TEST 4096 TIMES
1[illegible]  5[illegible]          JMP     TST59

                        /GLITCH TEST OF LOAD CNT GATES

1200  4026  TEST60,  JMS     RANDOM          /GET RANDOM NUMBER
1201  6153           CLAB                    /SEND IT TO BUFFER
1202  3020           DCA     SEND            /SAVE IT
1203  1205           TAD     K0200           /SET AC 04=1
1204  6152           CLLR                    /SET MODE 1=1
1205  7200           CLA                     /CLEAR AC
1206  1206           TAD     K0300           /SET AC 04,05=1
1207  6152           CLLR                    /SET MODE 2=1
1210  7200           CLA
1211  2022           ISZ     REGA            /DO THIS 4096 TIMES
1212  5203           JMP     .-7
1213  6157           CLCA                    /READ COUNTER
1214  3021           DCA     RXED            /SAVE IT
1215  1021           TAD     RXED            /RESTORE IT
1216  7040           SZA CLA                 /ZERO?
1217  7402           HLT                     /THE MODE REGISTER CAUSES ILLEGAL LOAD COUNTER
```

```
                        /GENERAL GATE SHAKING TEST OF THE MODE FLIP FLOPS

1100  7300    TEST31, CLA CLL             /GET RANDOM NUMBER
1101  6133            CLSB                /SEND IT TO BUFFER
1102  3422            DCA     SEND        /SAVE IT
1103  1422            TAD     SEND        /GET TEST COUNTER
1104  7006            RTL                 /ROTATE TWO LEFT
1105  7006            RTL                 /ROTATE TWO LEFT
1106  7006            RTL                 /ROTATE TWO LEFT
1107  0207            AND     K7700       /INSURE THAT MODE 0,1,2=1
1110  6132            CLLR                /SEND RANDOM NUMBER TO CONTROL REGISTER
1111  7040            CMA                 /COMPLEMENT
1112  0207            AND     K7700       /INSURE THAT MODE 0,1,2=1
1113  6132            CLLR                /SET TO COMPLEMENT OF THE NUMBER
1114  2022            ISZ     SEND        /DO THIS 4096 TIMES
1115  5100            JMP     TEST31+3
1116  6136            CLSA                /GET TEST VALUE FROM BUFFER
1117  3421            DCA     SAVE        /SAVE IT
1120  1421            TAD     SAVE        /RESTORE IT
1121  7041            CIA                 /COMPLEMENT
1122  1420            TAD     SEND        /SUBTRACT TEST NUMBER
1123  7240            SZA CLA             /EQUAL?
1124  7402            HLT                 /BUFF CHANGED IN ERROR
1125  6137            CLSA                /READ COUNTER
1126  3421            DCA     SAVE        /SAVE IT
1127  1421            TAD     SAVE        /RESTORE IT
1130  7240            SZA CLA             /STILL ZERO?
1131  7402            HLT                 /COUNTER CHANGED IN ERROR
```

```
                        /DOES MODE 2 1-0 CLR CNT?

1132  4055              TEST32, JMS     RANDOM          /GET RANDOM NUMBER
1133  6133                      CLAB                    /SEND IT TO BUFFER
1134  3220                      DCA     SEND            /SAVE IT
1135  6132                      CLLR                    /ZERO MODE 2
1136  1223                      TAD     K0100           /AC 05=1
1137  6132                      CLLR                    /GENERATE "CLR CNT"
1140  7200                      CLA                     /CLEAR AC
1141  1225                      TAD     K0200           /SET AC 04=1
1142  6134                      CLEN                    /GENERATE "LOAD CNT"
1143  7200                      CLA
1144  6132                      CLLR                    /0 MODE 2
1145  6137                      CLCA                    /READ COUNTER
1146  3221                      DCA     RXED            /SAVE IT
1147  6133                      CLAB                    /CLEAR BUF OR OVERFLOW WILL RELOAD CNT
1150  1221                      TAD     RXED            /RESTORE IT
1151  7041                      CIA                     /COMPLEMENT
1152  1220                      TAD     SEND            /SUBTRACT TEST NUMBER
1153  7640                      SZA CLA                 /EQUAL?
1154  7402                      HLT                     /MODE 2 1-0 DID IT

1155  1223                      TAD     K0100           /SET AC 05=1
1156  6132                      CLLR                    /GENERATE "CLR CNT"
1157  6137                      CLCA                    /READ COUNTER
1160  3221                      DCA     RXED            /SAVE IT
1161  1221                      TAD     RXED            /RESTORE IT
1162  7640                      SZA CLA                 /ZERO?
1163  7402                      HLT                     /MODE 2 0-1 FAILED
                        /TEST 41 TEST OF SKIP OVERFLOW AND INTERRUPT
                        /
                        /DOES COUNTER OVERFLOW SET OVERFLOW FLOP
                        /
1164  7200                      NOP
1165  7200                      NOP
1166  7200                      NOP
1167  7200              TST41,  CLA CLL
1170  6132                      CLLR                    /CLEAR STATUS
1171  1223                      TAD     K0100           /SET AC 05=1
1172  6132                      CLLR                    /0 TO COUNTER
1173  6135                      CLSA                    /CLEAR CLOCK STATUS
1174  7360                      CLA CLL CML RAR         /SET AC=4000
1175  6133                      CLAB                    /SET BUFFER TO 4000
1176  7200                      CLA CLL
1177  1225                      TAD     K0200           /SET AC 04=1
1200  6134                      CLEN                    /LOAD CNT (00)=1; 1 TO OVERFLOW
1201  7200                      CLA CLL
1202  6133                      CLAB
1203  6132                      CLLR                    /CLEAR ALL MODES
1204  1223                      TAD     K0100           /SET AC 05=1
1205  6132                      CLLR                    /GEN "CLR CNT"
1206  6135                      CLSA                    /GET STATUS OF CLOCK
1207  7500                      SMA CLA
1210  7402                      HLT                     /OVERFLOW NOT SET
```

12-D8CA-D-(D)


```
1211  2422            ISZ     REG4        /DO TEST 4096 TIMES
1212  5614            JMP I   TST40X      /INDIRECT REF. TO TST40
1213  7410            SKP
1214  1407  TST40X,   TST40               /DEF. OF TST40x
```

```
1215  7000      NOP
                /DOES CLSA (6135) CLEAR OVERFLOW FLOP
                /
1216  7300      TST41A, CLA CLL
1217  6132              CLLR                    /CLEAR ALL MODES
1220  1023              TAD     K0100
1221  6132              CLLR                    /GEN "CLR CNT"
1222  6135              CLSA                    /CLEAR CLOCK STATUS
1223  7330              CLA CLL CML RAR
1224  6133              CLAB                    /SET BUF=4000 OCTAL
1225  7300              CLA CLL
1226  1025              TAD     K0200
1227  6134              CLEN                    /GEN LOAD CNT
1230  7300              CLA CLL
1231  6133              CLAB                    /ZERO BUF.
1232  6132              CLLR                    /CLEAR ALL MODES
1233  1023              TAD     K0100           /SET AC 05=1
1234  6132              CLLR                    /GEN "CLR CNT"
1235  7300              CLA CLL
1236  6135              CLSA                    /GET STATUS BIT 0=1
1237  7300              CLA CLL
1240  6135              CLSA                    /GET STATUS BIT 0=0
1241  7710              SPA CLA
1242  7402              HLT                     /CLSA FAILED TO CLEAR OVERFLOW FLOP

                /
                /TEST OVERFLOW SKIP
                /
1243  7300              CLA CLL
1244  6132              CLLR                    /CLEAR ALL MODES
1245  1023              TAD     K0100           /SET AC 05=1
1246  6132              CLLR                    /GEN "CLR CNT"
1247  6135              CLSA                    /CLEAR CLOCK STATUS
1250  7330              CLA CLL CML RAR
1251  6133              CLAB                    /SET BUF=4000 OCTAL
1252  7300              CLA CLL
1253  1025              TAD     K0200
1254  6134              CLEN                    /GEN LOAD CNT
1255  7300              CLA CLL
1256  6133              CLAB                    /CLR BUF.
1257  6132              CLLR                    /CLEAR ALL MODES
1260  1023              TAD     K0100           /AC 05=1
1261  6132              CLLR                    /GEN "CLR CNT"
1262  7300              CLA CLL
1263  6131              CLSK
1264  7417              SKP
1265  7402              HLT                     /CLOCK PRESET DIDN'T 0 OVERFLOW ENABLE
```

```
                    /TEST FOR NO INTERRUPT

1256  1210          TAD     PNTA
1257  3213          DCA     RETURN
1260  6001          ION
1261  7000          NOP
1262  6002          IOF
1263  7410          SKP
1264  7402    LOCA, HLT                     /ILLEGAL INTERRUPT OVERFLOW=1 OVERFLOW ENABLE=0

                    /SET INT ENABLE

1265  1223          TAD     K0100
1266  6134          CLEN                  /TURN ON CLOCK OVERFLOW INT
1267  7300          CLA CLL
1270  6131          CLSK
1271  7402          HLT                   /CLSK FAILED TO SKIP OVERFLOW=1 EN OVF INT=1

                    /
                    /TEST FOR CLOCK INTERRUPT
                    /
1272  1211          TAD     PNTB
1273  3213          DCA     RETURN
1274  6001          ION
1275  7000          NOP
1276  6002          IOF
1277  7402          HLT                   /CLOCK INT FAILED TO INTERRUPT
```

12-D8CA-D-(D)

#19-055-47
7.50

```
                        /TEST WITH FLAG UP ZERO OVERFLOW INT ENABLE

1310  7600      LOCB,   CLA CLL
1311  6134              CLEN
1312  6101              CLSK
1313  7410              SKP
1314  7402              HLT                     /OVERFLOW ENABLE WON'T ZERO

                        /TEST WITH FLAG ZERO OVERFLOW SET

1315  1426              TAD     K00100
1316  6134              CLEN
1317  7600              CLA CLL
1320  6132              CLLR                    /STOP THE CLOCK
1321  6135              CLSA                    /READ AND ZERO FLAG
1322  7600              CLA CLL
1323  6131              CLSK
1324  7410              SKP
1325  7402              HLT                     /BAD INTERRUPT CONDITION STILL EXIST'S

                        /TEST INT OVERFLOW=0

1326  1412              TAD     PNTC
1327  3413              DCA     RETURN
1330  6001              ION
1331  7000              NOP
1332  6002              IOF
1333  7410              SKP
1334  7402      LOCC,   HLT                     /ILLEGAL CLOCK INTERRUPT
1335  2422              ISZ     REGA            /DO INTERRUPT TEST 4096 TIMES
1336  5555              JMP I   TST41B          /CROSS PAGE REF TO TST41A
```

```
                /
                /TEST4: COUNTER CARRY TESTING
                /COUNTER PRESET SUCH THAT CLOCK CNT RAISES BIT IN QUESTION

                /DOES BIT 11 SET UP

1337  7200      CLA
1340  6132      CLLR                    /CLEAR ALL MODES
1341  6133      CLAB                    /CLEAR BUF
1342  1223      TAD     K0100           /SET AC 05=1
1343  6132      CLLR                    /GEN "CLR CNT"
1344  6135      CLSA                    /CLEAR STATUS
1345  7223      CLA
1346  3022      DCA     REGA
1347  3023      DCA     SEND
1350  6133      CLAB
1351  1225      TAD     K0200           /MODE 1 100 H2 RATE
1352  6134      CLEN
1353  7302      CLA CLL
1354  1224      TAD     K5100
1355  6132      CLLR
1356  6137      CLCA                    /READ COUNTER
1357  3021      DCA     RXED
1360  1021      TAD     RXED
1361  1225      TAD     M0001
1362  7650      SNA CLA
1363  5367      JMP     .+4
1364  2022      ISZ     REGA
1365  5356      JMP     .-7             /WAIT SOME MORE
1366  7402      HLT                     /BIT 11 FAILED TO GET SET BY A CLOCK PULSE

                /DOES BIT 10 SET UP

1367  7200      CLA
1370  6132      CLLR
1371  6133      CLAB
1372  1223      TAD     K0100
1373  6132      CLLR
1374  6135  TST41, CLSA
1375  7200      CLA
1376  3022      DCA     REGA
1377  1226      TAD     K0001
1400  6133      CLAB
1401  3023      DCA     SEND
1402  1225      TAD     K0200
1403  6134      CLEN
1404  7300      CLA CLL
1405  1224      TAD     K5100
1406  6132      CLLR
1407  6137      CLCA
1410  3021      DCA     RXED
1411  1021      TAD     RXED
1412  1027      TAD     M0002
1413  7650      SNA CLA
1414  5220      JMP     .+4
```

```
14:5  2022          ISZ     .+1
14:6  5C /          JMP     .-/
```

```
1447  7402            HLT             /BIT 10 FAILED TO GET SET BY COUNTING

                /DOES BIT 9 SET UP

1450  7200            CLA
1451  6032            CLLR
1452  6033            CLAB
1453  1225            TAD     K7100
1454  6132            CLLR
1455  6135    TST42,  CLSA
1456  7440            CLA
1457  3422            DCA     REGA
1460  1432            TAD     K0003
1461  6133            CLAB
1462  6023            DCA     SEND
1463  1423            TAD     K2200
1464  6134            CLEN
1465  7350            CLA CLL
1466  1224            TAD     K5100
1467  6132            CLLR
1470  6137            CLCA
1471  3421            DCA     RXED
1472  1421            TAD     RXED
1473  1431            TAD     M0004
1474  7650            SNA CLA
1475  5271            JMP     .+4
1476  2022            ISZ     REGA
1477  5242            JMP     .-7
1500  7402            HLT             /BIT 9 FAILED TO GET SET BY COUNTING

                /DOES BIT 8 SET UP

1501  7200            CLA
1502  6032            CLLR
1503  6033            CLAB
1504  1225            TAD     K0100
1505  6132            CLLR
1506  6135    TST43,  CLSA
1507  7440            CLA
1510  3422            DCA     REGA
1511  1432            TAD     K0007
1512  6133            CLAB
1513  3423            DCA     SEND*
1514  1423            TAD     K2200
1515  6134            CLEN
1516  7350            CLA CLL
1517  1224            TAD     K5100
1520  6032            CLLR
1521  6137            CLCA
1522  3421            DCA     RXED
1523  1421            TAD     RXED
1524  1434            TAD     M0010
1525  7650            SNA CLA
1526  5242            JMP     .+4
```

```
[illegible]  ISZ   REGA
[illegible]  JMP   .-1
[illegible]  HLT
```

/BIT 6 FAILED TO GET SET BY COUNTING

```
                        /DOES BIT 7 SET UP

1510  7200              CLA
1511  6132              CLLR
1512  6133              CLAB
1513  1425              TAD     K7777
1514  6132              CLLR
1515  6135    TST44,    CLSA
1516  7200              CLA
1517  3422              DCA     REGA
1520  1433              TAD     K2217
1521  6133              CLAB
1522  3420              DCA     SEND
1523  1425              TAD     K0200
1524  6134              CLEN
1525  7240              CLA CLL
1526  1424              TAD     K5100
1527  6132              CLLR
1530  6137              CLCA
1531  3421              DCA     RXED
1532  1421              TAD     RXED
1533  1445              TAD     K0020
1534  7650              SNA CLA
1535  5343              JMP     .+4
1536  2422              ISZ     REGA
1537  5322              JMP     .-7
1540  7402              HLT                     /BIT 7 FAILED TO GET SET BY COUNTING

                        /DOES BIT 6 SET UP

1541  7200              CLA
1542  6132              CLLR
1543  6133              CLAB
1544  1425              TAD     K0100
1545  6132              CLLR
1546  6135    TST45,    CLSA
1547  7200              CLA
1550  3422              DCA     REGA
1551  1434              TAD     K0037
1552  6133              CLAB
1553  3420              DCA     SEND
1554  1105              TAD     K0220
1555  6134              CLEN
1556  7240              CLA CLL
1557  1424              TAD     K5100
1560  6132              CLLR
1561  6137              CLCA
1562  3421              DCA     RXED
1563  1421              TAD     RXED
1564  1446              TAD     K0040
1565  7650              SNA CLA
1566  5344              JMP     .+4
1567  2422              ISZ     REGA
1570  5353              JMP     .-7
```

/MAINDEC [illegible] PAL13 V141 18-OCT-69 10:55 PAGE 22-1

[illegible] HLT /BIT 6 FAILED TO GET SET BY COUNTING

12 - DCA - D - (D)


```
                        /DOES BIT 5 SET UP

1634  7200              CLA
1635  6132              CLLR
1636  6133              CLAB
1637  1263              TAD     K7100
1640  6132              CLLR
1641  6135    TST46,    CLSA
1642  7200              CLA
1643  3422              DCA     REGA
1644  1255              TAD     K2277
1645  6133              CLAB
1646  3420              DCA     SEND
1647  1263              TAD     K0277
1650  6134              CLEN
1651  7300              CLA CLL
1652  1024              TAD     K5200
1653  6132              CLLR
1654  6137              CLCA
1655  3421              DCA     AXED
1656  1021              TAD     AXED
1657  1047              TAD     M0200
1660  7038              SNA CLA
1661  5215              JMP     .+4
1662  2422              ISZ     REGA
1663  5204              JMP     .-7
1664  7402              HLT                     /BIT 5 FAILED TO GET SET BY COUNTING

                        /DOES BIT 4 SET UP

1665  7200              CLA
1666  6132              CLLR
1667  6133              CLAB
1670  1263              TAD     K0100
1671  6132              CLLR
1672  6135    TST47,    CLSA
1673  7200              CLA
1674  3422              DCA     REGA
1675  1256              TAD     K0177
1676  6133              CLAB
1677  3420              DCA     SEND
1700  1263              TAD     K0200
1701  6134              CLEN
1702  7300              CLA CLL
1703  1024              TAD     K5200
1704  6132              CLLR
1705  6137              CLCA
1706  3421              DCA     AXED
1707  1021              TAD     AXED
1710  1047              TAD     M0200
1711  7038              SNA CLA
1712  5246              JMP     .+4
1713  2422              ISZ     REGA
1714  5235              JMP     .-7
```

11 - DEC(8) - D - (D)

/MAI DEC 12-B?? PAL10 V141 12-OCT-69 10:55 PAGE 23-1

16:3 7 2 HLT /BIT 4 FAILED TO GET SET BY COUNTING

```
                    /DOES BIT 3 SET UP

1680  7200          CLA
1681  6036          CLLR
1682  6033          CLAB
1683  1423          TAD     K0100
1684  6036          CLLR
1685  6035    TST48,CLSA
1686  7200          CLA
1687  3422          DCA     REGA
1688  1437          TAD     K3777
1689  6033          CLAB
1690  3420          DCA     SEND
1691  1403          TAD     K0200
1692  6034          CLEN
1693  7300          CLA CLL
1694  1424          TAD     K5100
1695  6036          CLLR
1696  6037          CLCA
1697  3421          DCA     RXED
1700  1421          TAD     RXED
1701  1452          TAD     M0900
1702  7650          SNA CLA
1703  5707          JMP     .+4
1704  2022          ISZ     REGA
1705  5665          JMP     .-7
1706  7402          HLT                     /BIT 3 FAILED TO GET SET BY COUNTING

                    /DOES BIT 2 SET UP

1707  7200          CLA
1710  6036          CLLR
1711  6033          CLAB
1712  1423          TAD     K0100
1713  6036          CLLR
1714  6035    TST49,CLSA
1715  7200          CLA
1716  3422          DCA     REGA
1717  1437          TAD     K3777
1720  6033          CLAB
1721  3020          DCA     SEND
1722  1403          TAD     K0200
1723  6034          CLEN
1724  7300          CLA CLL
1725  1424          TAD     K5100
1726  6036          CLLR
1727  6037          CLCA
1730  3421          DCA     RXED
1731  1421          TAD     RXED
1732  1452          TAD     M1000
1733  7650          SNA CLA
1734  5741          JMP I   TST49X          /CROSS TO TST49A
1735  2022          ISZ     REGA            /BACK TO TST49+13
```

```
        17[illegible] 5[illegible]   JMP I   TST49Y
        17[illegible] 7412           HLT

                                     /BIT 2 FAILED TO GET SET BY COUNTING
```

```
                        /DOES BIT 1 SET UP

1760  7400              CLA
1761  6132              CLLR
1762  6135              CLSA
1763  1776              TAD     K7776
1764  6132              CLLR
1765  6135    TST49A,   CLSA
1766  7200              CLA
1767  3642              DCA     REGA
1770  1641              TAD     K1777
1771  6135              CLSA
1772  3643              DCA     SEND
1773  1640              TAD     K0200
1774  6204              CLEN
1775  7342              CLA CLL
1776  1624              TAD     K5100
1777  6132              CLLR
2000  6137              CLSA
2001  3621              DCA     RXED
2002  1621              TAD     RXED
2003  1633              TAD     M2000
2004  7550              SNA CLA
2005  5201              JMP     .+4
2006  2242              ISZ     REGA
2007  5203              JMP     .-7
2010  7402              HLT                     /BIT 1 FAILED TO GET SET BY COUNTING

                        /DOES BIT 0 SET UP

2011  7400              CLA
2012  6132              CLLR
2013  6135              CLSA
2014  1775              TAD     K0177
2015  6132              CLLR
2016  6135    TST49B,   CLSA
2017  7200              CLA
2020  3642              DCA     REGA
2021  1642              TAD     K3777
2022  6135              CLSA
2023  3643              DCA     SEND
2024  1640              TAD     K0200
2025  6204              CLEN
2026  7342              CLA CLL
2027  1624              TAD     K5100
2030  6132              CLLR
2031  6137              CLSA
2032  3621              DCA     RXED
2033  1621              TAD     RXED
2034  1634              TAD     K4000
2035  7550              SNA CLA
2036  5212              JMP     .+4
2037  2242              ISZ     REGA
2040  5201              JMP     .-7
```

DEC(1) - D- (D)

/MAINDEC-12-D7? PAL10 V141 17-OCT-69 10:55 PAGE 25-1

HLT

/BIT 0 FAILED TO GET SET BY COUNTING

```
                        /TEST9: DOES COUNTER COUNT NORMALLY AND AT ALL RATES
                        /
                        /RUN ALL COUNT RATES FUNCTIONS

2012  1224              TAD     K1400
2013  6252              CLLR                        /SET 400KC RATE
2014  7300              CLA CLL
2015  6135              CLSA                        /READ STATUS
2016  7710              SMA CLA
2017  5215              JMP     .-2                 /WAIT FOR OVERFLOW

2020  1216              TAD     K2000
2021  6252              CLLR
2022  7300              CLA CLL                     /SET 100KC RATE
2023  6135              CLSA
2024  7710              SMA CLA
2025  5223              JMP     .-2                 /WAIT FOR OVERFLOW

2026  1217              TAD     K3000
2027  6252              CLLR                        /SET 10KC RATE
2030  7300              CLA CLL
2031  6135              CLSA
2032  7710              SMA CLA
2033  5231              JMP     .-2

2034  1220              TAD     K7700               /PRESET THE CLOCK
2035  6203              CLAB                        /FOR 100 CPS TEST
2036  7200              CLA
2037  1221              TAD     K4100               /SET 1KC RATE
2040  6252              CLLR
2041  7300              CLA CLL
2042  6135              CLSA
2043  7710              SMA CLA
2044  5242              JMP     .-2

2045  1224              TAD     K5100               /SET 100 CPS RATES
2046  6252              CLLR
2047  7300              CLA CLL
2050  6135              CLSA
2051  7710              SMA CLA
2052  5250              JMP     .-2

2053  7300              CLA CLL
2054  1224              TAD     K0020               /SET AC 07=1
2055  6134              CLEN                        /ENABLE INPUT CHAN1
2056  7200              CLA
2057  1247              TAD     K6000               /SET INPUT RATE CHAN1=60HZ
2060  6252              CLLR
2061  7300              CLA CLL
2062  6135              CLSA
2063  7710              SMA CLA
2064  5262              JMP     .-2
```

```
                    /
                    / TEST INPUT CHANNEL INTERRUPT CHAN 1
                    /
2254  1436  ITST1,  TAD     PNTO
2255  3425          DCA     RETURN          /SET UP INTERRUPT RETURN
2256  1225          TAD     K0050           /ENABLE INPUT AND INTERRUPT
2257  6264          CLEV
2260  6232          CLLR                    /SIMULATE INPUT CHANNEL ONE
2261  6001          IOF
2262  7402          HLT                     /WAIT
2263  7402          HLT                     /NO INTERRUPT ERROR

2264  6264  LOCD,   AND     K0020           /CLEAR INTERRUPT ENABLE SET SIMULATE INPUT
2265  6264          CLEV
2266  7002          CLA CLL
2267  1264          TAD     PNTE
2270  3413          DCA     RETURN
2271  6001          IOF
2272  6235          CLSA                    /CLEAR CLOCK STATUS
2273  7610          SKP CLA
2274  7402  LOCE,   HLT                     /INTERRUPT IN ERROR
```

```
                    /
                    /SIMULATED INPUT TESTS CHANNEL 3
                    /
2140  0000  INT01,  TAD      K0001
2141  6234          CLEN
2142  6232          CLLR                    /SET ERCNT FLOP
2143  7000          NOP
2144  7000          NOP
2145  7000          NOP
2146  7000          NOP
2147  6232          CLLR                    /SET PREVENT FLOP
2150  7000          CLA
2151  7410          CLL
2152  7000          NOP
2153  6234          CLEN                    /CLEAR ENABLES
2154  6235          CLSA
2155  3220          DCA      SEND
2156  6235          CLSA
2157  4000          AND      K0003
2160  3132          DCA      RXED
2161  1941          TAD      RXED
2162  7540          SPA CLA
2163  7402          HLT                     /CLSA DOESN'T Ø INPUT CHANNEL

2164  1220          TAD      SEND
2165  7041          CIA
2166  1200          TAD      K0003          /SUBTRACT SET
2167  7540          SZA CLA
2170  7402          HLT                     /BOTH PRE-EVENT  AND EVENT NOT SET
2171  2222          ISZ      REGA
2172  5740          JMP I    INT01          /INDIRECT REF TO INPT01

                    /
                    /TEST INPUT CHANNEL INTERRUPT CHAN 2
                    /
2173  1335  INTST2, TAD      PNTF
2174  3213          DCA      RETURN         /SET UP INTERRUPT RETURN
2175  1201          TAD      K3214
2176  6234          CLEN
2177  6232          CLLR
2200  6001          ION
2201  7000          NOP                     /WAIT
2202  7402          HLT                     /NO INTERRUPT

2203  4202  LOOP,   AND      K0004          /CLEAR INTERRUPT ENABLE
2204  6234          CLEN
2205  7500          CLA CLL
2206  1335          TAD      PNTG
2207  3213          DCA      RETURN
2210  6001          ION
2211  6235          CLSA                    /CLEAR CLOCK STATUS
2212  7610          SKP CLA
2213  7402  LOOP,   HLT                     /INTERRUPT IN ERROR
                                            /CLEA EN EV 2 INT BAD
```

```
                        /
                        /TEST INPUT CHANNEL INTERRUPT CHAN 3
                        /
2[illegible] [illegible] ITST3, TAD     PNTI
2[illegible] 3123       DCA     RETURN          /SET UP INTERRUPT RETURN
2[illegible] 1430       TAD     K0003
2[illegible] 6[illegible] CLEN
2[illegible] 6[illegible] CLLR
2[illegible] 6[illegible] ION
2[illegible] 7[illegible] NOP                   /WAIT
2[illegible] 7402       HLT                     /NO INTERRUPT

2[illegible] [illegible] LOCH,  AND     K0001           /CLEAR INTERRUPT ENABLE
2[illegible] 6[illegible] CLEN
2[illegible] 7[illegible] CLA CLL
2[illegible] 1[illegible] TAD     PNTI
2[illegible] 3[illegible] DCA     RETURN
2[illegible] [illegible] ION
2[illegible] [illegible] CLSA                   /CLEAR CLOCK STATUS

2[illegible] 7[illegible] SKP CLA
2[illegible] 7[illegible] LOCI, HLT             /INTERRUPT IN ERROR
```

```
                    /
                    /SIN INPUT TESTS CHAN 2
                    /
2200  7000          NOP
2201  7000          NOP
2202  7000          NOP
2203  6004          IOF                     /INT OFF
2204  7000          NOP
2205  7000          NOP
2206  7000          NOP
2207  7000          NOP
2210  7000          NOP
2211  7000          NOP
2212  7000          NOP
2213  7000          NOP
2214  7000          NOP
2215  7000          NOP
2216  7000          NOP
2217  7000          NOP
2220  7000          NOP
2221  7000          NOP
2222  1032  INPT02, TAD     K0004
2223  6131          CLEN                    /ENABLE CHAN 2
2224  6132          CLLR                    /SET EVENT FLOP
2225  7000          NOP
2226  7000          NOP
2227  7000          NOP
2230  7000          NOP
2231  6132          CLLR                    /SET PREVENT FLOP
2232  7200          CLA
2233  7100          CLL
2234  7000          NOP
2235  6131          CLEN
2236  6135          CLSA
2237  3024          DCA     SEND
2240  6135          CLSA
2241  0031          AND     K0014
2242  3021          DCA     RXED
2243  1021          TAD     RXED
2244  7640          SZA CLA
2245  7402          HLT                     /CLSA DOESN'T 0 INPUT CHANNEL

2246  1024          TAD     SEND
2247  7041          CIA
2250  1031          TAD     K0014           /SUBTRACT SET
2251  7542          SZA CLA
2252  7402          HLT                     /BOTH PRE-EVENT AND EVENT NOT SET
2253  2022          ISZ     REGA
2254  5222          JMP     INPT02
```

```
                    /
                    /SIX INPUT TESTS CHAN 1
                    /
2250  1124  INPT03, TAD     K0020
2251  6134          CLEN
2252  6132          CLLR                    /SET EVENT FLOP
2253  7000          NOP
2254  7000          NOP
2255  7000          NOP
2256  7000          NOP
2257  6132          CLLR                    /SET PREVENT FLOP
2260  7200          CLA
2261  7100          CLL
2262  7000          NOP
2263  6134          CLEN
2264  6135          CLSA
2265  3020          DCA     SEND
2266  6135          CLSA
2267  0123          AND     K0060
2270  3021          DCA     RXED
2271  1021          TAD     RXED
2272  7040          SZA CLA
2273  7402          HLT                     /CLSA DOESN'T 0 INPUT CHANNEL

2274  1020          TAD     SEND
2275  7041          CIA
2276  1123          TAD     K0060           /SUBTRACT SET
2277  7640          SZA CLA
2300  7402          HLT                     /BOTH PRE-EVENT AND EVENT NOT SET
2301  7000          NOP
2302  7000          NOP
2303  7000          NOP
2304  2022          ISZ     REGA            /DO TEST 4096 TIMES
2305  5714          JMP I   .+2             /INDIRECT REF. TO INPT03
2306  7410          SKP
2307  2255          INPT03
```

```
                    /TEST OF INPUT CHANNEL #3
                    /KNOBS OF CHAN1,CHAN2,CHAN3 SET TO LINEFREQ

2320  6135          INPT04, CLSA                    /CLEAR STATUS
2321  7200                  CLA CLL
2322  6132                  CLLR                    /CLEAR ALL MODES
2323  1203                  TAD     K0003
2324  6134                  CLEN                    /ENABLE CHAN3 INPUT AND INTER.
2325  7200                  CLA
2326  6131                  CLSK                    /SKIP ON CLOCK INTER.
2327  5327                  JMP     .-2             /WAIT
2330  6135                  CLSA                    /GET CLOCK STATUS
2331  3421                  DCA     RXED            /SAVE IT
2332  1421                  TAD     RXED            /RESTORE IT
2333  7041                  CIA
2334  1204                  TAD     K0002
2335  7540                  SZA CLA
2336  7402                  HLT                     /INTERRUPT BUT CHAN 1
                                                    /EVENT HOP NOT SET
                    /TEST OF INPUT CHANNEL 2

2337  6135                  CLSA                    /CLEAR STATUS
2340  7200                  CLA CLL
2341  6132                  CLLR                    /ZERO ALL MODES
2342  1231                  TAD     K0014           /ENAB. CHAN. 2 INPUT AND
                                                    /INTERRUPT FLOPS
2343  6134                  CLEN
2344  7200                  CLA
2345  6131                  CLSK                    /CHECK FOR CLOCK INTER.
2346  5346                  JMP     .-2             /WAIT
2347  6135                  CLSA                    /GET STATUS
2350  3421                  DCA     RXED            /SAVE IT
2351  1421                  TAD     RXED            /RESTORE IT
2352  7041                  CIA
2353  1243                  TAD     K0010
2354  7540                  SZA CLA
2355  7402                  HLT                     /INTERRUPT BUT CHAN 2
                                                    /EVENT FLOP NOT SET

                    /TEST OF INPUT CHAN 1

2356  6135                  CLSA                    /CLEAR STATUS
2357  7200                  CLA CLL
2360  6132                  CLLR                    /CLEAR ALL MODES
2361  1223                  TAD     K0050           /ENAB. CHAN1 INPUT
2362  6134                  CLEN                    /AND INTER.
2363  7200                  CLA
2364  6131                  CLSK                    /CHECK FOR CLOCK INTER.
2365  5365                  JMP     .-2             /WAIT
2366  6135                  CLSA                    /GET CLOCK STATUS
2367  3421                  DCA     RXED            /SAVE IT
2370  1421                  TAD     RXED            /RESTORE IT
2371  7041                  CIA
2372  1244                  TAD     K0040
2373  7540                  SZA CLA
```

```
                HLT                     /INTER. BUT CHAN 1 EVENT
                                        /FLOP NOT SET

                TAD     [illegible]
                TAD     REGA
                DCA     REGA
                TAD     REGA
                SZA CLA                 /DO TEST 128 TIMES
                JMP I   IPT04           /INDIRECT REF. TO IPT04
```

```
                    /TEST OF SAMPLE MODE
                    LINC=6141                       /START LINC MODE
                    CLA=7211                        /CLEAR AC AND LINC
                    ESF=7224                        /ENAB SPEC. IN REG.
                    SAM0=6210                       /READ KNOB 0
                    SAM1=6121                       /READ KNOB 1
                    STA=1240                        /STORE AC
                    LOAI=1020                       /LOAD AC
                    PDP=6202                        /ENTER PDP-8 MODE
2400  7104          CSR                             /IF RIGHT SW BIT 2(1)
2401  7440          SZL                             /SKIP FAST SAM TEST
2402  7510          SPA
2403  5005          JMP I   .+2                     /INDIRECT REF TO TCNT1
2404  7410          SKP
2405  2355          TCNT1
2406  6141  TSM,    LINC                            /ENTER LINC MODE
2407  7211          CLA
2410  7224          ESF                             /CLEAR SPEC. IN REG.
2411  6210          SAM0                            /READ KNOB ZERO
2412  6202          PDP
2413  3020          DCA     SEND
2414  6141          LINC
2415  6121          SAM1                            /READ KNOB 1
2416  7211          CLA                             /CLEAR AC
2417  1020          LOAI
2420  0123          0123
2421  7224          ESF                             /ENABLE FAST SAM
2422  6202          PDP                             /ENTER PDP-8 MODE
2423  6133          CLSA                            /CLEAR CLOCK STATUS
2424  7300          CLA CLL
2425  1245          TAD     K0400                   /SET MODE BIT0=1
2426  6132          CLLR
2427  7300          CLA CLL
2430  6141          LINC                            /ENTER LINC MODE
2431  6210          SAM0                            /FAST SAM SET THEREFORE
                                                    /READ IN VALUE OF KNOB1
                                                    /AS THIS WAS LAST CONVER
                                                    /SION
2432  6210          SAM0                            /SHOULD STILL READ KNOB1
2433  6202          PDP                             /ENTER PDP-8 MODE
2434  3021          DCA     RXED                    /SAVE VALUE
2435  1021          TAD     RXED                    /RESTORE IT
2436  7041          CIA
2437  1020          TAD     SEND                    /COMPARE IT
2440  7640          SZA CLA
2441  7410          SKP
2442  7402          HLT                             /READING FAST SAM
                                                    /INITIATED CONVERSION
                                                    /IN ERROR
2443  1245          TAD     K0400
2444  6132          CLLR                            /MODE 2(1),0(1)
```

```
2445  7000    CLA     CLL CML RAR
2446  6205            CLAB                    /SET BUFF=4000
2447  7200            CLA
2450  1150            TAD     K7600
2451  6204            CLEN                    /LOAD CTR FROM BUF
2452  7200            CLA
2453  6203            CLAB                    /CLR BUF
2454  7200            CLA
2455  6232            CLLR                    /CLEAR ALL MODES
2456  1140            TAD     K4000
2457  6132            CLLR                    /SET OVERFLOW MODE 0(1)
2460  6141            LINC                    /ENTER LINC MODE
2461  6206            SAM2                    /SAMPLE KNOB 0
2462  6032            PDP                     /ENTER PDP-8 MODE
2463  3021            DCA     RXED            /STORE
2464  1021            TAD     RXED            /RESTORE
2465  7041            CIA
2466  1020            TAD     SEND
2467  7040            SZA CLA
2470  7402            HLT                     /CONVERSION NOT INITIATED BY OVFLO
2471  2022            ISZ     REGA            /DO TEST 4096 TIMES
2472  5652            JMP I   TSMA            /CROSS PAGE REF TO TSM
                /CHECK THAT MODE 2(2),1(1),2(1) DO NOT AFFECT
                /SAM

2473  7200    TSM1,   CLA
2474  6132            CLLR                    /ZERO ALL MODES
2475  1136            TAD     K3600
2476  6132            CLLR                    /MODE 1(1),2(1),0(0)
2477  6141            LINC                    /ENTER LINC MODE
2500  6211            CLR
2501  6004            ESF                     /ZERO SPEC. IN. REG.
2502  6206            SAM2                    /SAMPLE KNOB 0
2503  6002            PDP
2504  3020            DCA     SEND
2505  6141            LINC
2506  6201            SAM1                    /SAMPLE KNOB 1
2507  1020            LOAI
2510  0100            0100
2511  0004            ESF                     /SET FAST SAM FLOP
2512  6100            SAM0                    /GET KNOB 1 SETTING
2513  0002            PDP                     /ENTER PDP MODE
2514  3021            DCA     RXED            /STORE
2515  1021            TAD     RXED            /RECEIVE
2516  7041            CIA
2517  1020            TAD     SEND            /COMPARE
2520  7042            SZA CLA
2521  7410            SKP
2522  7402            HLT                     /FAST SAM NOT SET
2523  6141            LINC                    /ENTER LINC MODE
2524  6206            SAM2                    /READ KNOB 0
2525  6002            PDP                     /ENTER PDP MODE
2526  3021            DCA     RXED            /STORE
2527  1021            TAD     RXED            /RESTORE
```

```
[illegible]  7[illegible]      CLA
[illegible]  1[illegible]      TAD     SEND                    /COMPARE
[illegible]  7[illegible]      SPA CLA
[illegible]  7[illegible]      HLT                             /MODE 2(1),1(1) INHIBIT FAST SAM
[illegible]  2[illegible]      ISZ     .MLOP                   /DO TEST 4096 TIMES
[illegible]  5[illegible]      JMP I   TSM1A                   /INDIRECT REF TO TSM1
```

```
                    /DOES TO PRESET CLEAR OVFLO, ENABLES, RATES AND MODES
                    /PROGRAMED IO PRESET USED
                    /IS COUNTER WORKING
2542  7200  TCNTI,  CLA                          /CLEAR AC
2543  6132          CLLR                         /CLEAR ALL MODES
2544  6102          CLEN                         /CLEAR ALL ENABLES
2545  1147          TAD     K6200                /SET RATE=10KHZ
2546  6142          CLCA                         /READ COUNTER
2547  6131          CLCA
2550  3020          DCA     SEND                 /STORE
2551  1147          TAD     K6200
2552  7041          IAC
2553  7442          SZA
2554  5346          JMP     .-2                  /WAIT LOOP 4,92 MSEC
2555  6137          CLCA                         /READ COUNTER AGAIN
2556  7041          CIA
2557  1020          TAD     SEND                 /COMPARE
2560  7042          SZA CLA
2561  7412          SKP
2562  7402          HLT                          /COUNTER NOT WORKING
                                                 /WITH RATE BITS 1+2 SET
                    /NOW DO IO PRESET CHECK IF RATE BITS 1,2 CLEAR
2563  6141          LINC                         /ENTER LINC MODE
2564  1022          LDAI
2565  0020          0020
2566  0004          ESF                          /DO IO PRESET
2567  0002          PDP                          /ENTER PDP MODE
2570  6137          CLCA                         /GET COUNTER
2571  3020          DCA     SEND                 /STORE
2572  1147          TAD     K6200
2573  7002          NOP
2574  7000          NOP
2575  7000          NOP
2576  7041          IAC
2577  7442          SZA
2600  5372          JMP     .-2                  /WAIT LOOP 4,92 MSEC
2601  6137          CLCA                         /READ COUNTER AGAIN
2602  7041          CIA
2603  1020          TAD     SEND                 /COMPARE
2604  7040          SZA CLA
2605  7402          HLT                          /IO PRESET FAILED TO
                                                 /CLEAR RATE BITS 1,2
2606  6132          CLLR                         /CLEAR ALL MODES
```

```
                /NOW CHECK RATE BIT 0
                /FIRST SEE IF COUNTER WORKS AT 1KHZ RATE
2613  7200      CLA                             /CLEAR AC
2614  6132      CLLR                            /CLEAR ALL MODES
2615  6130      CLEN                            /CLEAR ENABLES
2616  1023      TAD     K4000
2617  6134      CLLR                            /SET RATE=1KHZ
2620  6137      CLSA                            /READ COUNTER
2621  3022      DCA     SEND
2622  7000      NOP
2623  7041      IAC
2624  7440      SZA
2625  5215      JMP     .-2                     /WAIT LOOP 16 MSEC
2626  6137      CLSA                            /READ COUNTER
2627  7041      CIA
2630  1022      TAD     SEND                    /COMPARE
2631  7440      SZA
2632  7410      SKP
2633  7402      HLT                             /COUNTER NOT WORKING
                                                /WITH RATE BIT 0 SET
                /NOW DO IO PRESET AND SEE IF BIT 1 CLEARED
2634  6141      LINC                            /ENTER LINC MODE
2635  1220      LDAI
2636  0000      0200
2637  0034      ESP                             /DO IO PRESET
2640  0033      PDP                             /ENTER PDP MODE
2641  6137      CLSA                            /READ COUNTER
2642  3022      DCA     SEND                    /STORE
2643  7000      NOP
2644  7041      IAC
2645  7440      SZA
2646  5244      JMP     .-2                     /WAIT 16 MSEC
2647  6137      CLSA                            /READ COUNTER AGAIN
2650  7041      CIA
2651  1022      TAD     SEND                    /COMPARE
2652  7540      SZA CLA
2653  7402      HLT                             /RATE BIT 0 SET AFTER IO
                                                /PRESET
                /DOES OVERFLOW AND OVFLO INT. FLOP
                /CLEAR WITH IO PRESET
2654  7200  TCNT2, CLA                           /CLEAR AC
2655  6132      CLLR                            /CLEAR ALL MODES
2656  1023      TAD     K2100
2657  6132      CLLR                            /SET MODE 2(1)
2660  6135      CLSA                            /CLEAR STATUS
2661  7200      CLA
2662  1025      TAD     K4000
2663  6143      CLAB                            /SET BUF TO 4000
2664  7200      CLA
2665  1022      TAD     K4200
2666  6134      CLEN                            /LOAD COUNTER
2667  7200      CLA
2670  6133      CLAB                            /ZERO BUF
2671  6132      CLLR                            /CLEAR ALL MODES
```

```
2552  1728          TAD     K0100
2553  6402          CLLR                    /GEN "CLR CNT"
2554  6401          LINC                    /ENTER LINC MODE
2555  7404          LDAI
2556  0020          0020
2557  6414          ESF                     /SO IO PRESET
2570  6402          PDP                     /ENTER PDP MODE
2571  6435          CLSA                    /GET STATUS
```

```
2672  7440          SNA CLA
2673  7510          SKP
2674  7402          HLT                             /OVFLO STILL SET AFTER IO
                                                    /PRESET
                    /TEST OVFLO INT ENABLE
2675  7600          CLA                             /CLEAR AC
2676  1423          TAD     K0100
2677  6132          CLLR                            /SET MODE 2(1)
2700  6135          CLSA                            /CLEAR STATUS
2701  7600          CLA
2702  1425          TAD     K0200
2703  6133          CLAB                            /SET BUF PRESET REG.
2704  7600          CLA
2705  1425          TAD     K0200
2706  6134          CLEN                            /LOAD CNT WITH 4000
2707  7600          CLA
2710  1423          TAD     K0100
2711  6134          CLEN                            /SET INT.
2712  6141          LINC                            /ENTER LINE MODE
2713  1020          LDAI
2714  0220          0220
2715  6004          ESF                             /DO IO PRESET
2716  6002          PDP                             /ENTER PDP MODE
2717  7600          CLA
2720  6132          CLLR                            /CLEAR ALL MODES
2721  1423          TAD     K0100
2722  6132          CLLR                            /GEN.
2723  6131          CLSK
2724  7410          SKP
2725  7402          HLT                             /OVFLO INTER.
                                                    /SET AFTER IO PRESET
                    /DOES IO PRESET CLEAR INPUT ENABLE FLOPS
2726  7600          CLA
2727  6132          CLLR                            /CLEAR ALL MODES
2730  1425          TAD     K0077
2731  6134          CLEN                            /ENABLE INPUTS TO ALL CHAN
2732  6135          CLSA                            /CLEAR STATUS
2733  6141          LINC                            /ENTER LINE MODE
2734  1020          LDAI
2735  0220          0220
2736  6004          ESF                             /DO IO PRESET
2737  6002          PDP                             /ENTER PDP MODE
2740  7600          CLA
2741  1425          TAD     K0077
2742  6132          CLLR                            /SIMULATE INPUTS ON ALL CHAN
```

```
2743  7000          NOP
2744  7000          NOP
2745  7000          NOP
2746  7000          NOP
2747  7000          NOP
2750  7000          NOP
2751  6132          CLLR                    /SIM INPUTS ON ALL CHAN
2752  7000          NOP
2753  7000          NOP
2754  7000          NOP
2755  7000          NOP
2756  7000          NOP
2757  7000          NOP
2760  7200          CLA
2761  6135          CLSA                    /GET STATUS
2762  7440          SZA
2763  7402          HLT                     /STATUS NOT ZERO
                                            /IO PRESET FAILED TO CLEAR
                                            /ENABLES=AC CONTAINS STATUS
2764  7200          CLA                     /CLEAR AC
                    /DOES IO PRESET CLEAR MODE 2
2765  6133          CLAB
2766  6132          CLLR                    /CLEAR MODES
2767  1023          TAD     K0100
2770  6132          CLLR                    /SET MODE 2(1) - CLR CNT
2771  6141          LINC                    /ENTER LINC MODE
2772  1020          LDAI
2773  0020          0020
2774  6004          ESF                     /DO IO PRESET
2775  0002          PDP                     /ENTER PDP MODE
2776  7200          CLA
2777  1150          TAD     K5555
3000  6133          CLAB                    /LOAD BUF WITH 5555
3001  7200          CLA
3002  1165          TAD     K0200
3003  6134          CLEN                    /GEN LOAD CNT
3004  6137          CLCA                    /LOAD CNT TO AC
3005  7710          SPA CLA
3006  7402          HLT                     /MODE 2 NOT CLEARED
                                            /BY IO PRESET
                    /DOES IO PRESET CLEAR MODE 0
3007  7424          OSR                     /IF RIGHT SW BIT 2(1)
3010  7006          RTL                     /SKIP FAST SAM TEST
3011  7510          SPA
3012  5254          JMP     INDEX
3013  7200          CLA
3014  6132          CLLR                    /CLEAR ALL MODES
3015  6141          LINC                    /ENTER LINC MODE
3016  0100          SAM0                    /READ KNOB 0
3017  0002          PDP
3020  3020          DCA     SEND
3021  6141          LINC
3022  0101          SAM1                    /READ KNOB 1
3023  0002          PDP                     /ENTER PDP MODE
```

```
3024  7200        CLA
3025  1145        TAD     .+0400
3026  6132        CLLR                    /SET MODE B(1)
3027  6141        LINC                    /ENTER LINC MODE
```

```
3240  1220          LDAI
3241  0020          0020
3242  6004          ESF                     /DO IO PRESET
3243  1220          LDAI
3244  0100          0100                    /ENABLE FAST SAM
3245  6004          ESF
3246  6144          SAM0                    /READ KNOB 1=FAST S. MODE
3247  6002          PDP                     /ENTER PDP MODE
3250  7041          CIA
3251  1020          TAD     SEND
3252  7640          SZA CLA
3253  7410          SKP
3254  7402          HLT                     /FAST SAM NOT SET
3255  6141          LINC                    /ENTER LINC MODE
3256  0100          SAM0                    /READ KNOB 0
3257  0002          PDP                     /ENTER PDP MODE
3260  7041          CIA
3261  1022          TAD     SEND
3262  7640          SZA CLA
3263  7402          HLT                     /MODE 0 NOT CLEARED
3264  2022  INDEX,  ISZ     REGA            /DO TEST 4096 TIMES
3265  5264          JMP I   TCNT2A          /CROSS PAGE BER TO TCNT2
3266  6141          LINC
3267  1020          LDAI
3270  0020          0020
3271  6004          ESF                     /DO IO PRESET
3272  0002          PDP
```

```
3263  7240            CLA
                /DOES MODE 1(1) WORK
3264  7240    TM001,  CLA
3265  6132            CLLR                    /CLEAR ALL MODES
3266  6133            CLAB                    /CLEAR BUF
3267  4456            JMS     RANDOM          /GET RANDOM NUM
3270  3220            DCA     SEND
3271  1020            TAD     SEND
3272  6133            CLAB                    /SEND RANDOM NUM TO BUF
3273  7200            CLA
3274  1025            TAD     K0100
3275  6132            CLLR                    /GEN "CLR CNT"
3276  6135            CLSA                    /CLEAR CLOCK STATUS
3277  7240            CLA
3300  1025            TAD     K0200
3301  6134            CLEN                    /GEN LOAD CNT
3302  6132            CLLR                    /SET MODE BIT 1(1)
3303  7200            CLA
3304  6133            CLAB                    /CLEAR BUF
3305  1023            TAD     K0060
3306  6134            CLEN                    /ENABLE INPT 1 AND INT CHAN1
3307  6131            CLSK                    /SKP ON CLOCK INT
3310  5307            JMP     .-1
3311  6135            CLSA                    /CLEAR STATUS
3312  7200            CLA
3313  7240            NOP
3314  6136            CLBA                    /GET BUF
3315  7041            CIA
3316  1020            TAD     SEND            /COMPARE
3317  7040            SZA CLA
3320  7402            HLT                     /CHAN 1 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
3321  6134            CLEN                    /CLEAR ENABLES
3322  6135            CLSA                    /CLEAR CLOCK STATUS
3323  7200            CLA
3324  6133            CLAB                    /CLEAR BUF
3325  1021            TAD     K0014
3326  6134            CLEN                    /ENABLE CHAN 2 INPUT AND INT
3327  6131            CLSK                    /SKP ON CLOCK INT
3330  5327            JMP     .-1
3331  6135            CLSA                    /CLEAR STATUS
3332  7240            CLA
3333  7240            NOP
3334  7240            NOP
3335  6136            CLBA                    /GET BUF
3336  7041            CIA
3337  1020            TAD     SEND            /COMPARE
3340  7040            SZA CLA
3341  7402            HLT                     /CHAN2 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
3342  6134            CLEN                    /CLEARS ENABLE
3343  6135            CLSA                    /CLEAR STATUS
3344  7200            CLA
3345  6133            CLAB                    /CLEAR BUF
3346  1022            TAD     K0003
```

```
3147  6134          CLEN                    /ENABLES CHAN 3 INPUT AND INT
3150  6131          CLSK                    /SKIP ON CK INT
3151  5352          JMP     .-1
3152  6135          CLSA                    /CLEAR CLOCK STATUS
3153  7200          CLA
3154  7200          NOP
3155  7200          NOP
3156  6136          CLBA                    /GET BUF
3157  7041          CIA
3160  1022          TAD     SEND            /COMPARE
3161  7040          SZA CLA
3162  7402          HLT                     /CHAN 3 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
                    /TEST MODE 1(1) AND MODE 2(1)
3163  6134  TMOD3,  CLEN                    /CLEARS ENABLES
3164  1106          TAD     K0300
3165  1114          TAD     K1000
3166  6132          CLLR                    /START CNT RATE=400KHZ - MODE 1(1) AND 2(1)
3167  7000          NOP                     /WAIT
3170  7000          NOP
3171  7000          NOP
3172  7000          NOP
3173  7000          CLA
3174  1100          TAD     K0300
3175  6132          CLLR                    /STOP CNT - MODE 1(1) AND 2(1)
3176  6137          CLCA                    /GET CNT
3177  3022          DCA     SEND            /STORE
3200  6135          CLSA
3201  7200          CLA
3202  6133          CLAB                    /CLEAR BUF
3203  1123          TAD     K0060
3204  6134          CLEN                    /ENABLE CHAN1 INPUT AND INT
3205  6131          CLSK                    /SKP ON CLOCK INT
3206  5205          JMP     .-1
3207  6135          CLSA                    /CLEAR CLOCK STATUS
3210  7200          CLA
3211  6136          CLBA                    /GET BUF
3212  7041          CIA
3213  1022          TAD     SEND            /COMAPRE
3214  7040          SZA CLA
3215  7402          HLT                     /CHAN1 FAILED TO CAUSE CNT TO BUF TRANSFER
3216  6134          CLEN                    /CLEARS ENABLES
3217  6135          CLSA                    /CLEAR STATUS
3220  7200          CLA
3221  6133          CLAB                    /CLEAR BUF
3222  1131          TAD     K0014
3223  6134          CLEN                    /ENABLE CHAN 2 INPUT AND INT
3224  6131          CLSK                    /SKP ON CLOCK INT
3225  5224          JMP     .-1
3226  6135          CLSA                    /CLEAR STATUS
3227  7200          CLA
3230  7200          NOP
3231  7200          NOP
3232  6136          CLBA                    /GET BUF
3233  7041          CIA
```

```
                TAD     SEND            /COMPARE
                SZA CLA
                HLT                     /CHAN 2 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
                CLEN                    /CLEAR ENABLES
```

```
                            CLSA
                            CLA
                            CLAB                    /CLEAR BUF
                            TAD     K2003
                            CLEN                    /ENABLES CHAN3 INPUT AND INT
                            CLSK                    /SKP ON CLOCK INT
                            JMP     .-1
                            CLSA                    /CLEAR CLOCK STATUS
                            CLA
                            NOP
                            NOP
                            CLBA                    /GET BUF
                            CIA
                            TAD     SEND            /COMPARE
                            SZA CLA
                            HLT                     /CHAN 3 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
                            CLCA                    /GET CNT
                            SZA CLA
                            HLT                     /CHAN3 INPUT FAILED TO CLEAR CNT
                            NOP
                            NOP
                            OSR
                            RAL
                            SPA CLA                 /IF RIGHT SWITCHES BIT 1(1) SUPPRESS PRINTING OF K
                            JMP     .+10
                            LINC
                            LDAI
                            0313
                            PDP
                            TLS                     /TYPE LETTER K
                            TSF
                            JMP     .-1
                            CLA
                            TAD     COUNT
                            IAC
                            DCA     COUNT
                            TAD     COUNT
                            CIA
                            TAD     K0020
                            SZA CLA CLL
                            JMP     IOPRE
                            DCA     COUNT
                    /WHISTLE ROUTINE
                            OSR
                            SPA CLA                 /IF BIT 0(1) SUPPRESS END OF TEST WHISTLE
                            JMP     IOPRE
                    WHISTLE,TAD     K0040
                            SNL
                            JMP     .-2
                            CLL
                            TAD     K0001
                            TAD     K2400
                            SNL
                            JMP     .-2
```

```
[illegible]  1,<2>          TA,     <2*01
[illegible]  5[illegible]   [illegible]  <-1STLE
[illegible]  [illegible]    CC[illegible] TA,  -1
[illegible]  6[illegible]   IOP-E,  LI  2
```

```
                        LDAI
                        0220
                        ESF             /DJ IO PRESET
                        POP
                        JMP     177
                $
```

```
02[illegible]  [illegible]  [illegible]  [illegible]  [illegible]  11111111  11111111  11111111  11111111
014  [illegible]  [illegible]  [illegible]  [illegible]  11111111  11111111  11100000  00000001

020  [illegible]  [illegible]  [illegible]  [illegible]  11111111  11111111  11111111  11111111
03[illegible]  [illegible]  [illegible]  [illegible]  11111111  11111111  11111111  11111111

042  [illegible]  [illegible]  [illegible]  [illegible]  11111111  11111111  11111111  11111111
050  [illegible]  [illegible]  [illegible]  [illegible]  11111111  11111111  11111111  11111111

060  [illegible]  [illegible]  [illegible]  [illegible]  11111111  11111111  11111111  11111111
070  [illegible]  [illegible]  [illegible]  [illegible]  11111111  11111111  11111111  11111111

100  [illegible]  [illegible]  [illegible]  [illegible]  11111111  11111111  11111111  11111111
110  [illegible]  [illegible]  [illegible]  [illegible]  11111111  11111111  11111111  11111111

120  [illegible]  [illegible]  [illegible]  [illegible]  11111111  11111111  11111111  11111111
130  [illegible]  [illegible]  [illegible]  [illegible]  11111111  11111111  11111111  11111111

140  [illegible]  [illegible]  [illegible]  [illegible]  11111111  11111111  11111111  11111111
150  [illegible]  [illegible]  [illegible]  [illegible]  11111111  11111111  11111111  11111111

160  [illegible]  [illegible]  [illegible]  [illegible]  11111111  11111111  11111111  11111111
170  [illegible]  [illegible]  [illegible]  [illegible]  11111111  11111111  11111111  11111111

200  [illegible]  [illegible]  [illegible]  [illegible]  11111111  11111111  11111111  11111111
210  [illegible]  [illegible]  [illegible]  [illegible]  11111111  11111111  11111111  11111111

220  [illegible]  [illegible]  [illegible]  [illegible]  11111111  11111111  11111111  11111111
230  [illegible]  [illegible]  [illegible]  [illegible]  11111111  11111111  11111111  11111111

240  [illegible]  [illegible]  [illegible]  [illegible]  11111111  11111111  11111111  11111111
250  [illegible]  [illegible]  [illegible]  [illegible]  11111111  11111111  11111111  11111111

260  [illegible]  [illegible]  [illegible]  [illegible]  11111111  11111111  11111111  11111111
270  [illegible]  [illegible]  [illegible]  [illegible]  11111111  11111111  11111111  11111111

300  [illegible]  [illegible]  [illegible]  [illegible]  11111111  11111111  11111111  11111111
312  [illegible]  [illegible]  [illegible]  [illegible]  11111111  11111111  11111111  11111111

324  [illegible]  [illegible]  [illegible]  [illegible]  11111111  11111111  11111111  11111111
330  [illegible]  [illegible]  [illegible]  11111100  00000000  00000000  00000000  00000000

340
350

360
370
```

12-08(A-D-(D)

[illegible]	[illegible]	[illegible]	0142	TCNT2	2044	TST49X	0141
[illegible]	[illegible]	[illegible]	[illegible]	TCNT2A	0154	TST49Y	0142
[illegible]	[illegible]	[illegible]	[illegible]	TEST30	1064	WHISTL	3315
[illegible]	[illegible]	[illegible]	[illegible]	TEST31	1100		
[illegible]	[illegible]	[illegible]	[illegible]	TEST32	1132		
[illegible]	[illegible]	[illegible]	[illegible]	TMOD1	3064		
[illegible]	[illegible]	[illegible]	[illegible]	TMOD3	3103		
[illegible]	[illegible]	[illegible]	[illegible]	TSM	2406		
[illegible]	[illegible]	[illegible]	[illegible]	TSM1	2473		
[illegible]	[illegible]	[illegible]	[illegible]	TSM1A	0153		
[illegible]	[illegible]	[illegible]	[illegible]	TSMA	0152		
[illegible]	[illegible]	[illegible]	[illegible]	TST2X	2201		
[illegible]	[illegible]	[illegible]	[illegible]	TST21	0214		
[illegible]	[illegible]	[illegible]	[illegible]	TST22	0227		
[illegible]	[illegible]	[illegible]	[illegible]	TST23	0243		
[illegible]	[illegible]	[illegible]	[illegible]	TST24	2261		
[illegible]	[illegible]	[illegible]	[illegible]	TST25	0277		
[illegible]	[illegible]	[illegible]	[illegible]	TST26	0317		
[illegible]	[illegible]	[illegible]	[illegible]	TST27	0360		
[illegible]	[illegible]	[illegible]	[illegible]	TST27A	0125		
[illegible]	[illegible]	[illegible]	[illegible]	TST28	0440		
[illegible]	[illegible]	[illegible]	[illegible]	TST29	0520		
[illegible]	[illegible]	[illegible]	[illegible]	TST30	0534		
[illegible]	[illegible]	[illegible]	[illegible]	TST31	0562		
[illegible]	[illegible]	[illegible]	[illegible]	TST31X	0162		
[illegible]	[illegible]	[illegible]	[illegible]	TST32	0603		
[illegible]	[illegible]	[illegible]	[illegible]	TST32A	0127		
[illegible]	[illegible]	[illegible]	[illegible]	TST33	0625		
[illegible]	[illegible]	[illegible]	[illegible]	TST34	0651		
[illegible]	[illegible]	[illegible]	[illegible]	TST35	0700		
[illegible]	[illegible]	[illegible]	[illegible]	TST35A	0126		
[illegible]	[illegible]	[illegible]	[illegible]	TST36	0732		
[illegible]	[illegible]	[illegible]	[illegible]	TST37	0756		
[illegible]	[illegible]	[illegible]	[illegible]	TST37X	1010		
[illegible]	[illegible]	[illegible]	[illegible]	TST38	1011		
[illegible]	[illegible]	[illegible]	[illegible]	TST38A	0130		
[illegible]	[illegible]	[illegible]	[illegible]	TST39	1040		
[illegible]	[illegible]	[illegible]	[illegible]	TST40	1167		
[illegible]	[illegible]	[illegible]	[illegible]	TST4DX	1214		
[illegible]	[illegible]	[illegible]	[illegible]	TST41	1374		
[illegible]	[illegible]	[illegible]	[illegible]	TST41A	1216		
[illegible]	[illegible]	[illegible]	[illegible]	TST41B	0155		
[illegible]	[illegible]	[illegible]	[illegible]	TST42	1425		
[illegible]	[illegible]	[illegible]	[illegible]	TST43	1456		
[illegible]	[illegible]	[illegible]	[illegible]	TST44	1507		
[illegible]	[illegible]	[illegible]	[illegible]	TST45	1540		
[illegible]	[illegible]	[illegible]	[illegible]	TST46	1571		
[illegible]	[illegible]	[illegible]	[illegible]	TST47	1622		
[illegible]	[illegible]	[illegible]	[illegible]	TST48	1653		
[illegible]	[illegible]	[illegible]	[illegible]	TST49	1704		
[illegible]	[illegible]	[illegible]	[illegible]	TST49A	1735		
[illegible]	[illegible]	TCNT1	2536	TST49B	1766		

ERRORS DETECTED: 0

LINKS GENERATED: 0

RUN-TIME: 17 SECONDS

3K CORE USED