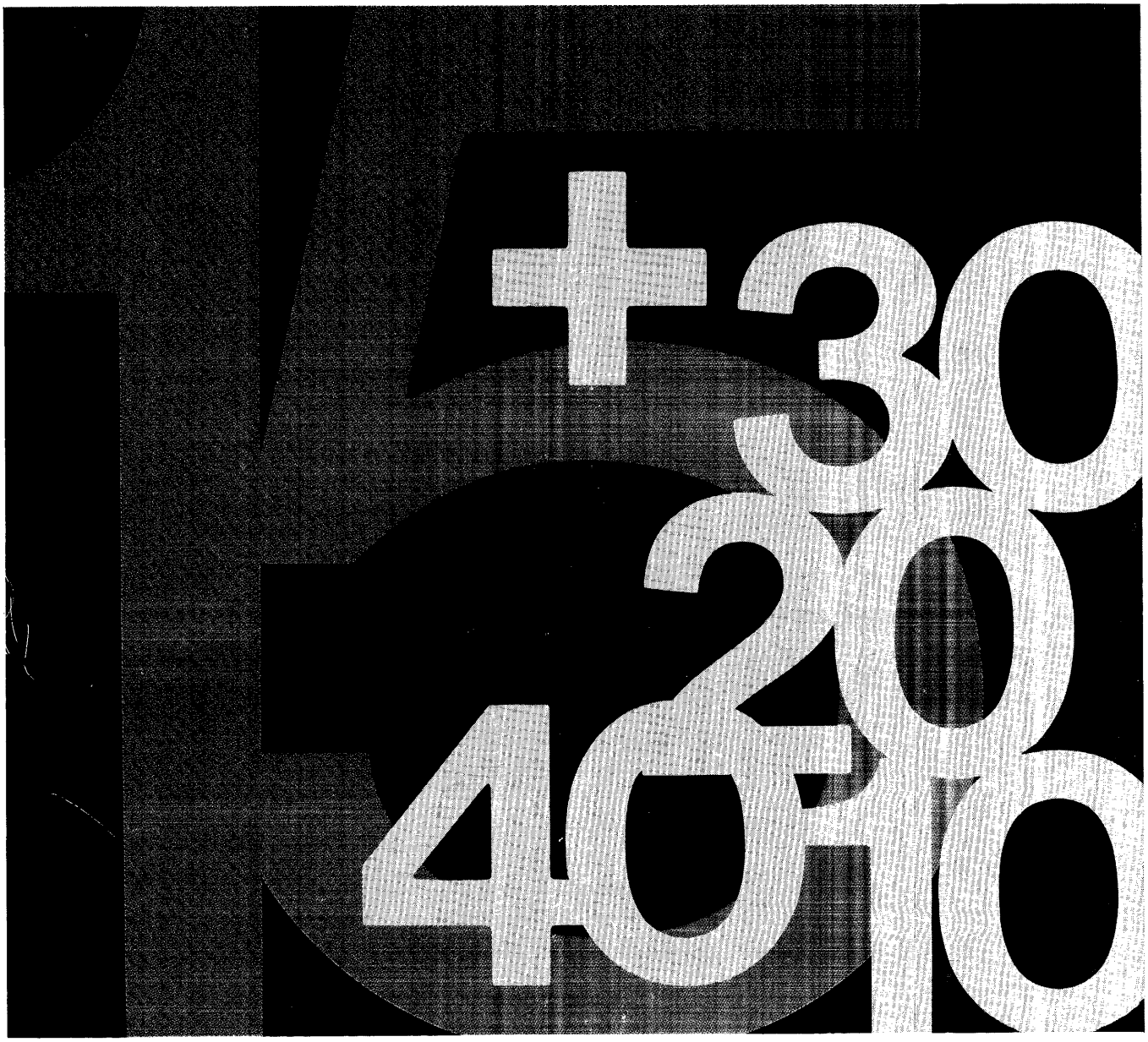
Digital Equipment Corporation
Maynard, Massachusetts

digital

PDP-15 Systems
Maintenance Manual

AD15 Analog Subsystem



DEC-15-H3AA-D

AD15
ANALOG SUBSYSTEM MAINTENANCE MANUAL

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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CONTENTS

CONTENTS (Cont)

CONTENTS (Cont)

ILLUSTRATIONS

TABLES

TABLES (Cont)

FOREWORD

The AD15 Analog Subsystem Maintenance Manual consists of six chapters that cover the following general topics:

Chapter 1 contains a functional and physical description of the AD15 Analog Subsystem. It also describes system expansion capabilities, options, and accessories. A list of pertinent system parameters and specifications is included at the end of the chapter.

Chapter 2 contains a detailed block diagram description of the AD15 Analog Subsystem. Logic descriptions of complicated circuitry are also provided at the end of the chapter.

Chapter 3 describes the AD15 IOT instructions, input status word and output status word formats. Several programming examples are provided to illustrate the capabilities of the AD15 Analog Subsystem.

Chapter 4 contains the installation and adjustment procedures for the AD15.

Chapter 5 provides a description of the procedures required to maintain and troubleshoot the AD15 Analog Subsystem.

Chapter 6 contains the engineering drawing set and complete signal glossary for the AD15.

The reader should be familiar with and have access to the following documentation:

PDP-15/10 Software System	DEC-15-GR1A-D
PDP-15/20/30/40 Advanced Monitor Software System	DEC-15-MR2A-D
PDP-15 Maintenance Manual	DEC-15-H2BB-D
PDP-15 Module Manual	DEC-15-H2EA-D
PDP-15 Interface Manual	DEC-15-H0AB-D
DEC Logic Handbook	042D 00370 AKO
AD15 Engineering Specification	A-SP-AD15-0-14
AD15 Acceptance and Calibration Procedure	A-SP-AD15-0-15
AD15 MAINDEC Diagnostics	DEC-15-D6GA-D(D)

CHAPTER 1
BASIC DESCRIPTION

1.1 PURPOSE OF EQUIPMENT

The AD15 Analog Subsystem is a computer-controlled device capable of multiplexing a maximum of 128 analog channels onto a common bus for analog-to-digital conversion. A maximum of 25,000 conversions per second can be handled by the system. The analog input voltage range is ±10V. Typical sources of analog input are: biomedical research, data accumulation on patients, and psychological and scientific investigation. The system can detect analog inputs as low as ±300 μV increments. The AD15 is designed to operate with the 18-bit PDP-15 computer. Both analog channel and gain selection are under control of the PDP-15. Figure 1-1 illustrates all interface signals between the PDP-15 and the AD15.

1.2 SYSTEM FUNCTIONAL DESCRIPTION

The AD15 Analog Subsystem consists of an interface, a single-ended multiplexer, and an analog-to-digital converter. Figure 1-2 shows the functional relationship of these units.

To initiate an analog-to-digital conversion, the accumulator in the PDP-15 is initially loaded with a status word containing gain selection, analog channel selection, and certain designated control functions (refer to Chapter 3). This status word is transferred to the AD15, using the input-output transfer (IOT) instructions. Other IOT instructions allow the analog inputs, which have been converted to digital data, to be transferred to the PDP-15 accumulator, or allow status information such as channel and flag selection to be transferred to the accumulator. The IOT instructions consist of an operation code (70_8), a device and subdevice select code, and IOP pulses used for determining program skips and direction of transfer. The IOT instruction uniquely addresses the AD15 with a device select code of 13_8.

There are two basic operating modes in the AD15 subsystem: program-controlled transfers and data channel (DCH) transfers. When operating in program control mode, data transfers occur between the PDP-15 accumulator and the AD15 under IOT control. When operating in the DCH mode, data transfers are made directly to and from memory under control of the PDP-15 I/O processor. Both sequential

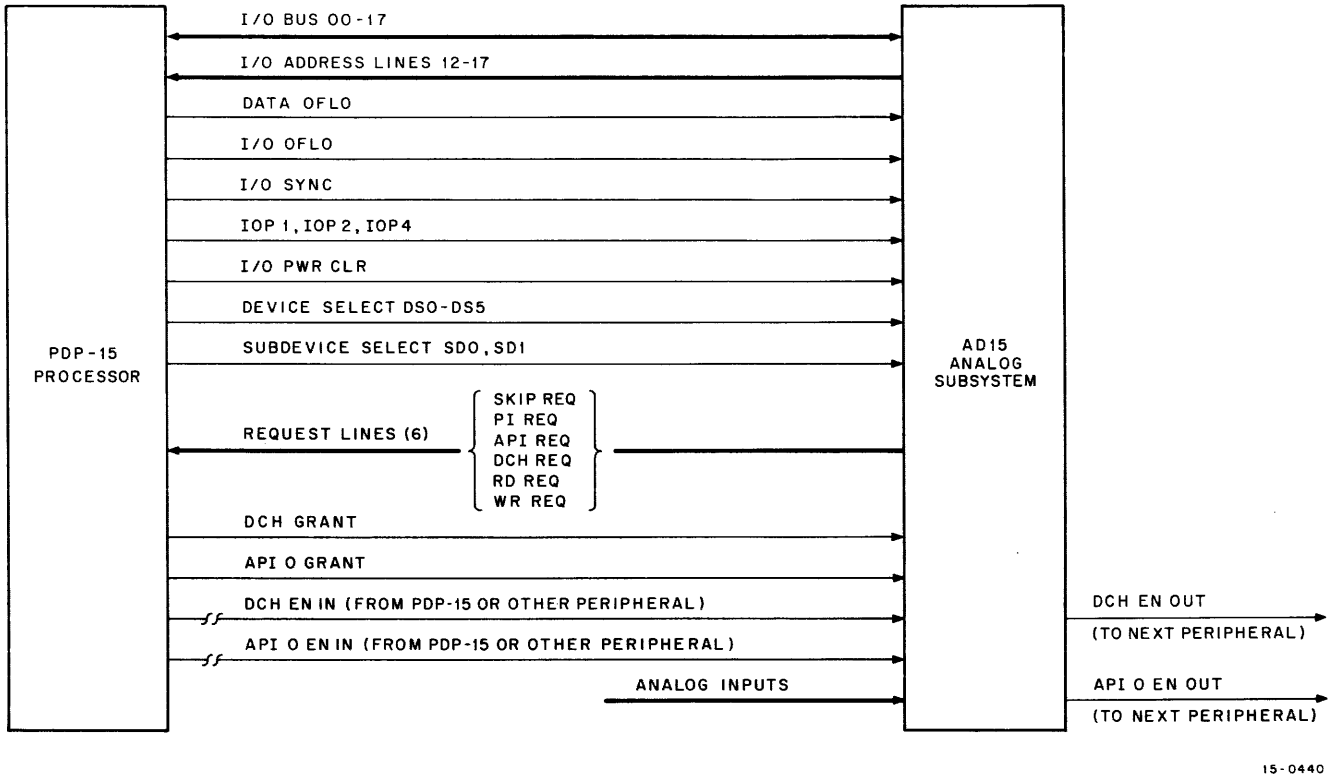


Figure 1-1 AD15 Signal Interface Diagram

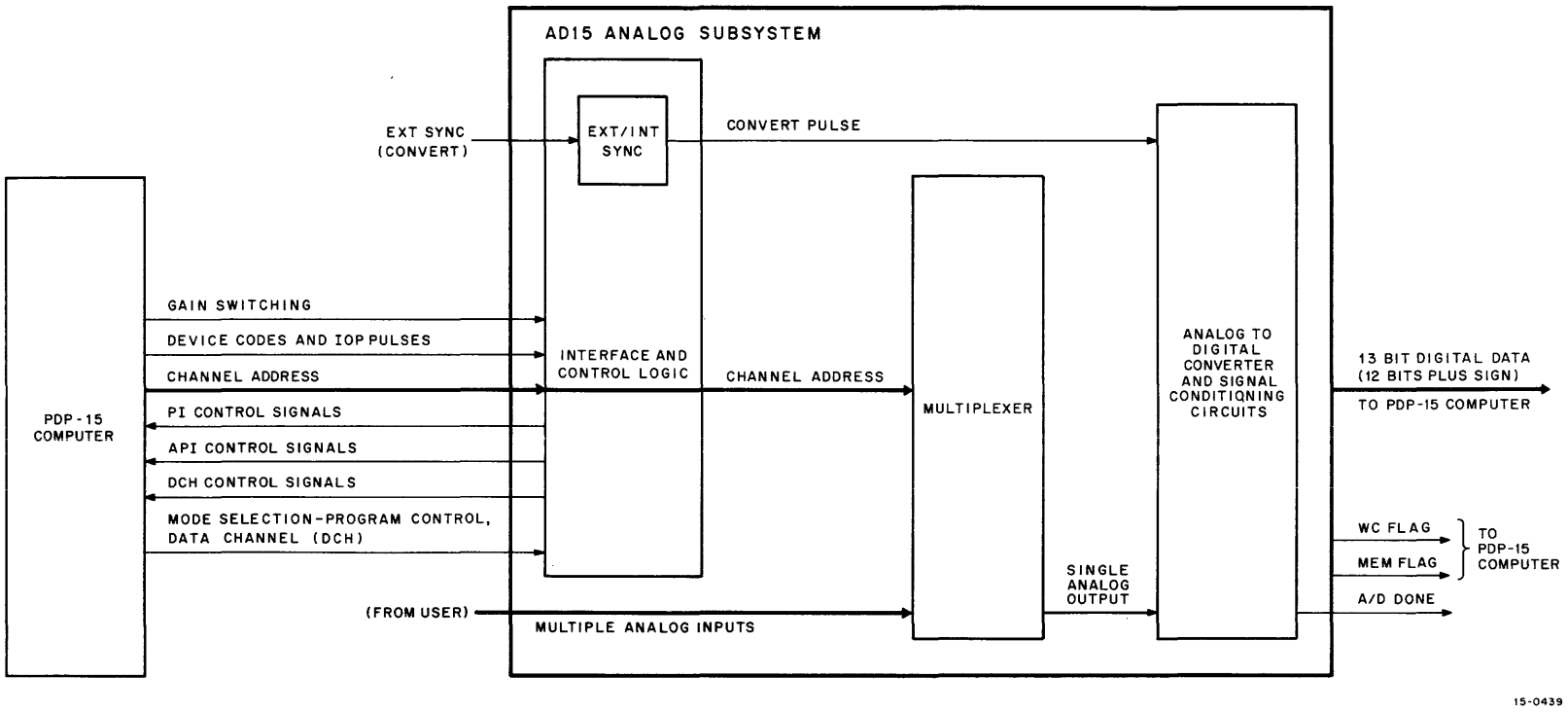


Figure 1-2 AD15 System Block Diagram

and random operations are possible in DCH mode. In sequential operation, analog channels are converted successively; while, in random operation, preselected analog channels can be converted without regard for any specific sequence.

An add-to-memory feature is employed in the AD15 whereby a converted value can be added to the contents of an existing memory location. The add-to-memory feature is desirable for signal averaging techniques.

1.2.1 Interface

The AD15 interface provides an address and data interface between the PDP-15 and the AD15; the interface also contains additional control logic, which includes selection of external or internal sync. When internal sync is selected, a convert pulse that initiates the conversion is internally generated within the AD15. When external sync is selected, the convert pulse is supplied from an external source.

The AD15 interface also provides additional logic to initiate program interrupts (PI), automatic priority interrupts (API), or data channel activity (DCH). The PI and API logic give the AD15 the capability to interrupt the PDP-15 computer to request servicing. The data channel logic interrupts the PDP-15 on a cycle-stealing basis and allows direct data transfers between the AD15 and the PDP-15 memory. For a detailed description of PI, API, or DCH, refer to the PDP-15 Maintenance Manual (DEC-15-H2BB-D).

Moreover, the interface logic decodes the IOT device code of 13_8 (which is used to uniquely address the AD15), decodes the IOP pulses to determine if a skip is to be made, or determines the direction of data transfer (to or from the AD15). The status word is also decoded by the interface logic to determine the gain selected, the analog input channel selected, and the operating mode.

1.2.2 Multiplexer

The analog channel address supplied to the AD15 from the PDP-15 is a 7-bit code capable of addressing a maximum of 128 analog channels. The analog input signal, uniquely addressed by this 7-bit code from the computer, is multiplexed onto a common output line. This signal is subsequently amplified by a single-ended operational amplifier. A gain factor of 1, 2, 4 or 8 can be selected for increased dynamic range with unchanged accuracy. For example, if signals are in the range of ±1.25V, a gain of 8 is selected to provide a full-scale deflection of ±10V, as seen by the A/D converter. A sample and hold circuit is provided in the multiplexer to allow sufficient time for analog-to-digital conversion when sampling rapidly fluctuating voltages.

1.2.3 Analog-to-Digital Converter

The amplified analog input is applied to an analog-to-digital converter module along with a start pulse. The module produces 13 output bits corresponding to a 2's complement, right-justified digital value of the input voltage. When the digital value of the 13 output bits has been determined, an A/D DONE pulse is generated, indicating completion of the conversion. The digital data from the output of the analog-to-digital converter is then transferred to the PDP-15 where it is used for further processing (such as signal analysis).

The input voltage range of the analog-to-digital converter is ±10V with an input resistance of 28 kΩ. Greater accuracy of small signals can be obtained by increasing the gain; consequently, these signals approximate the maximum input voltage to the converter, i.e., the gain should be selected to maximize the reading as a percentage of full-scale.

1.3 PHYSICAL DESCRIPTION

A physical description of the AD15 Analog Subsystem is provided in the following paragraphs. A minimum system 32-channel configuration is described first, followed by a description of increased system capability in increments of 32 channels. The user can purchase any number of channels in increments of four; however, based on the modular design, the most economical configurations are in increments of 32 channels.

1.3.1 AD15 Minimum System Configuration

When an AD15 subsystem is ordered, the user receives the items listed in Table 1-1. The frame and wired assembly include all the modules necessary for operation, including one A124 Multiplexer Module for the switch gain amplifier. Multiplexer modules intended for use with the analog channels must be ordered separately. Each multiplexer module handles four channels; thus, if a user desires a 32-channel subsystem, he must order an AD15 and eight BA124 Multiplexer Modules. He will receive the items listed in Table 1-1, and also the eight BA124 Multiplexer Modules specified. The following paragraphs describe each of the items shipped with the AD15.

1.3.1.1 Frame and Wired Assembly - The frame and wired assembly is the mounting frame used to house all the modules and connector boards. The assembly includes all the modules listed in Table 1-1. The modules are housed on H803 Connector Blocks (see DEC Logic Handbook for pin assignments); each connector block has receptacles for eight single-height, single-width modules.

NOTE

Certain modules are double or quadruple height and correspondingly take up two or four module slots.

Table 1-1
AD15 Equipment and Module Complement

Quantity	Nomenclature	Part Number/Module	Module Locations
1	Frame and Wired Assembly	D-AD-7007029-0-0	-
2	Amphenol Connector Cable Assemblies	BC01P-4	-
1	Mounting Plate	H929A	-
6	Filler Plates	H929B	-
1	Analog Power Supply and Chassis	H728	-
1	I/O Bus Cable Assembly	BC09B	-
9†	Multiplexer	BA124	C13, C14, D12, D13, D14, E12, E13, F12, F13
1	Switch Gain Amplifier	A222	C12
1	Sample and Hold Amplifier	A405	A12
1	Voltage Regulator	A708	A10
1	Analog-to-Digital Converter	A877	C10
1	Bus Data Interface	M101	C9
1	Device Selector	M103	B6
2	I/O Bus Multiplexer	M104	A6, A7
2	Inverter	M111	C7, E9
5	2-Input NAND Gates	M113	B8, B9, B13, E1, E2
2	3-Input NAND Gates	M115	E3, E4
2	4-Input NAND Gates	M117	B7, E8
1	Binary-Octal Decimal Decoder	M161	F9
1	Binary Counter	M211	C8
5	Six D-Type Flip-Flops	M216	D7, D8, D9, E6, E7
3	Dual Delay Multivibrator	M302	A8, A9, F8
4	I/O Bus Receiver	M510	C1, C2, D3, C4
5	Data Bus Driver	M621	D1, D2, D3, D4, D6
1	8-Bit Positive Input/Output Driver	M622	C6
2	Ribbon Connector	M908	E14, F14
4	I/O Bus Connector	M912	A1, A2, A3, A4
1	Bus Connector Module	M935	A14

†One A124 Module is supplied with the AD15 and is used by the Switch Gain Amplifier. For 32-channel operation, eight additional BA124 Modules must be ordered.

Three connector blocks strapped together constitute a system unit (see Figure 1-3). The 32-channel minimum configuration AD15 contains three system units as shown.

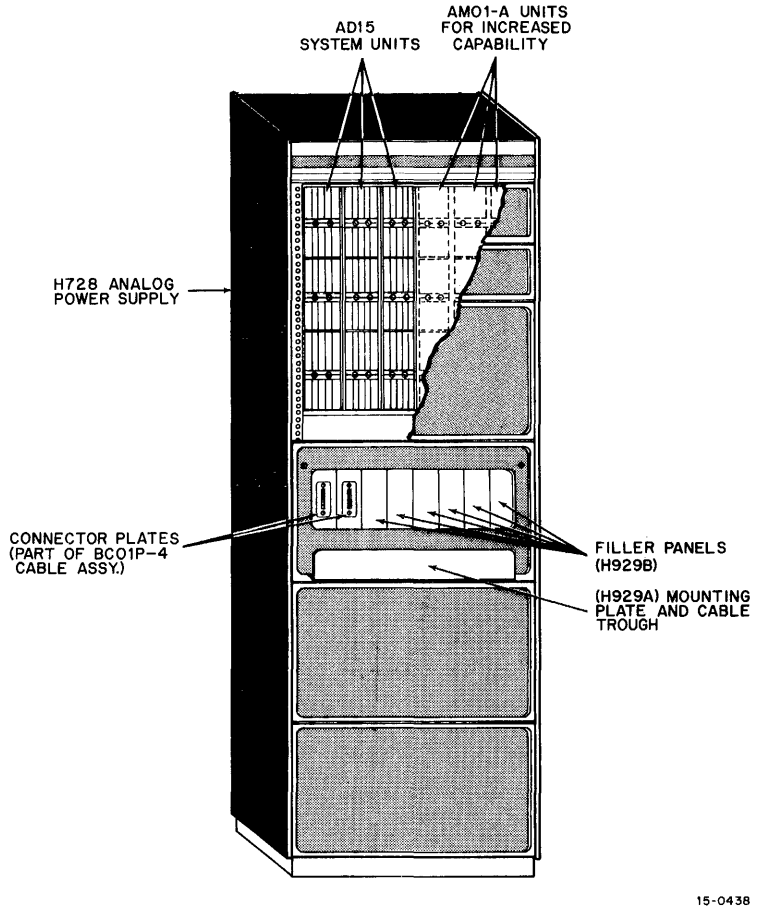


Figure 1-3 Analog Cabinet H963-P

1.3.1.2 Amphenol Connector Assembly - Two BC01P-4 Amphenol Connector Assemblies are supplied with the AD15 subsystem. Each cable assembly handles 16 channels. The cable assembly consists of a user receptacle (Amphenol Series 26), a connector plate that is mounted in a 10-1/2 in. high connector panel, a woven twisted-pair cable, and an M908 Connector Board (see Figure 1-4). User inputs are soldered to the user receptacle and are routed to the AD15 via the M908 Connector Board, which plugs into module slots E14 and F14 (see Drawing D-AD-7007029-0-0).

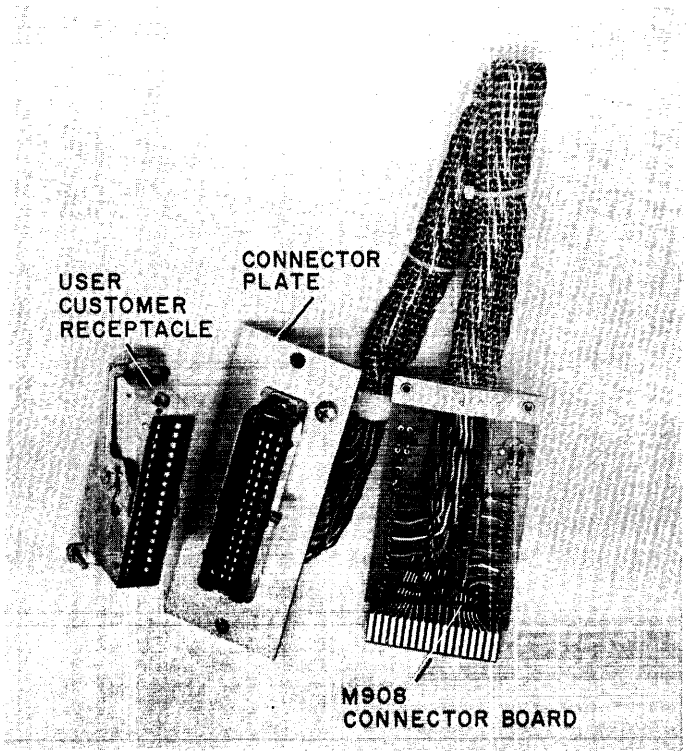


Figure 1-4 BC01P-4 Cable Assembly

NOTE

If the user installation employs BNC connectors, two BC01N-4 Cable Assemblies (see Figure 1-5) must be ordered, because they are not supplied with the basic system. The BC01N-4 assembly is similar to the BC01P-4; it differs in that the panel houses the BNC connectors rather than the 32-pin ribbon-type connectors. Customer inputs are routed to the AD15 via the BNC connector panel and the M908 Connector Card, which also plugs into slots E14 and F14. The BNC connector panel is clearly marked by channel number for wiring of customer inputs.

The user analog inputs can be wired to the AD15, using the Amphenol Series 26 connectors (see Figure 1-6). Each connector contains 32 pins (one analog signal pin and one ground for each channel).

1.3.1.3 H929B Filler Plates - For the 32-channel minimum configuration AD15, six H929B Filler Plates are included on the connector panel adjacent to the BC01P-4 Cable Assembly Connector Plates. As the system configuration is expanded, the required H929B Filler Plates are removed to allow the added BC01P-4 Cable Assembly Connector Plates to be installed.

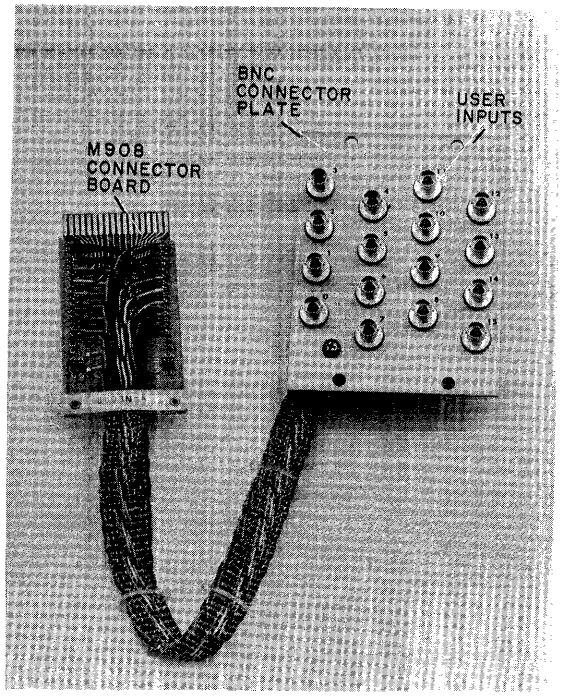


Figure 1-5 BC01N-4 Cable Assembly

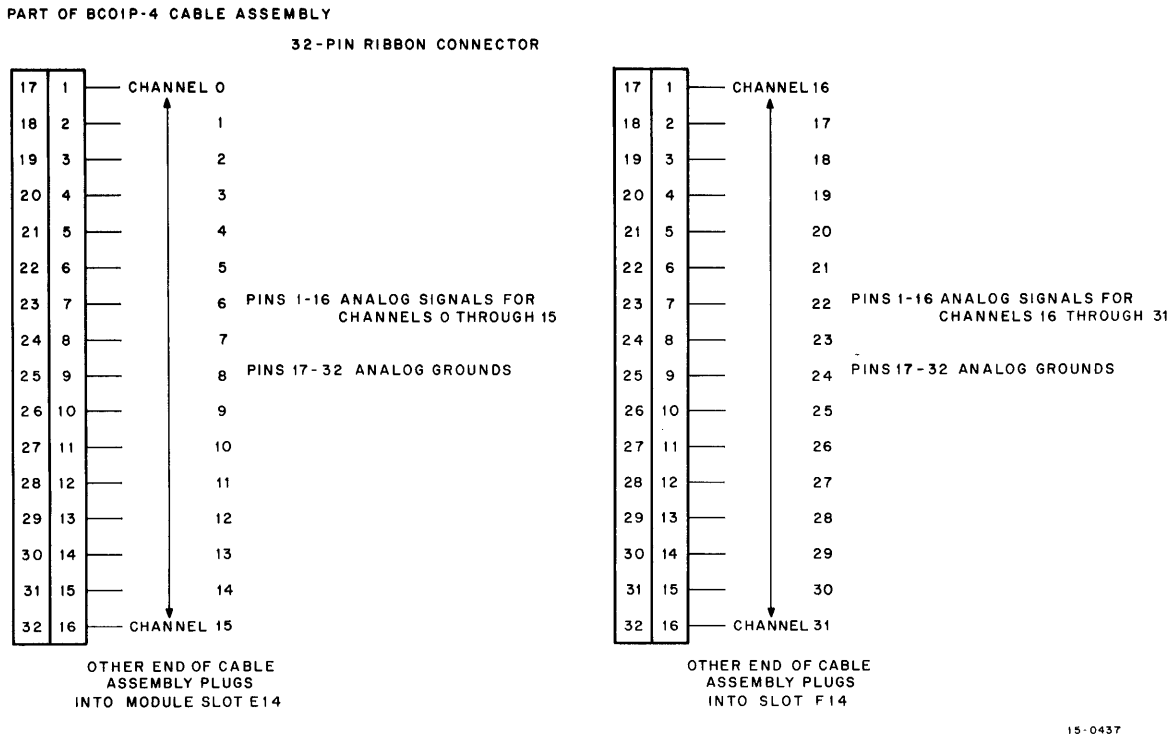


Figure 1-6 Wiring of User Inputs

1.3.1.4 Analog Power Supply - The AD15 subsystem contains an H728 Analog Power Supply. This power supply operates with 110V input and provides regulated outputs of 15 Vdc at 2A and 20 Vdc at 1.2A.

1.3.1.5 I/O Bus Cable Assembly - A BC09B I/O Bus Cable is supplied with the AD15 to interface the AD15 to the PDP-15 computer. The BC09B Cable Assembly comprises two multiconductor cables with two M912 Connectors at each end and associated hardware. The M912 is a double-height board and connects to module slots A1, A2 and B1, B2. Module slot A3 is jumpered to A1, A4 is jumpered to A2, B3 is jumpered to B1, and B4 is jumpered to B2 to provide a receptacle for another BC09B cable that is daisy-chained to the next device. For a more detailed description of the BC09B Cable Assembly, refer to the PDP-15 Interface Manual.

1.3.2 System Expansion

The addition of an AM01-A system unit is required to expand the AD15 from 32 to 64 channels. The AM01-A comprises two BC01P-4 Cable Assemblies and the modules listed in Table 1-2. The required number of BA124 Multiplexer Modules must be ordered, as with the AD15 subsystem. Thus, to expand a system from 32 to 64 channels, an AM01-A system unit and eight additional BA124 Multiplexer Modules must be ordered. The BC01P-4 Cable Assemblies connect the user's 32 analog channels to the AD15. Two of the H929B Filler Plates are removed, and the 32-pin Amphenol Connector Plates (part of the BC01P-4) are mounted in place. If the user employs BNC connectors at his site, he must procure two BC01N-4 Cable Assemblies for each 32 channels; they are not supplied with the system.

Table 1-2
AM01-A Equipment and Module Complement

Quantity	Nomenclature	Part Number/Module	Module Locations
2	Amphenol Connector Cable Assemblies	BC01P-4	-
8†	Multiplexer	BA124	C1 - C4, D1 - D4
1	Jumper Card	G729	B3
1	Octal Decoder	M161	B2
1	Bus Receiver	M510	E1
2	Bus Connector Card	M935	A1, A4

†BA124 Multiplexer Modules are not supplied with the AM01-A and must be ordered separately. For an additional 32 channels beyond the 32 channels in the AD15, eight modules must be ordered.

Table 1-3 lists different system configurations and the equipment provided with each. The user can tailor the system to his own individual needs using the examples provided.

Table 1-3
System Expansions

Channel	AD15	BA124 Modules†	AM01-A
28	1	7	0
32	1	8	0
36	1	9	1
60	1	15	1
64	1	16	1
68	1	17	2
92	1	23	2
96	1	24	2
100	1	25	3
124	1	31	3
128	1	32	3

†Excluding the A124 Multiplexer Module used with the Switch Gain Amplifier and supplied with the System.

1.4 SPECIFICATIONS

Table 1-4 lists the specifications of the AD15 Analog Subsystem.

Table 1-4
General Specifications

Specification	Description
PHYSICAL SPECIFICATIONS	
Frame Dimensions	Height - 17 in. Depth - 1.5 in. Width - 19 in.
ENVIRONMENTAL SPECIFICATIONS	
Cooling	Ambient air (forced)
Temperature range - operating	0° to 50°C
- storage	-25° to +85°C
Humidity	To 90% without condensation

Table 1-4 (Cont)
General Specifications

Specification	Description
POWER REQUIREMENTS	
Input voltage and frequency	105 - 125 Vac 47 to 420 Hz single-phase
AC current	Less than 1A
Power dissipation	Less than 100W
ACCURACY	
System	±0.04%
Temperature coefficient	±30 PPM/°C
Sample and Hold	±0.02%
Multiplexer and Switch Gain Amplifier	±0.02%
Analog-to-Digital Converter	±0.015% ±1/2 LSB
30 day long term stability Temperature coefficient	±20 PPM/°C
RANGE OF INPUT SIGNALS	
±10V full-scale ± 5V full-scale ±2.5V full-scale ±1.25V full-scale	(gain = 1) (gain = 2) (gain = 4) (gain = 8)
SAMPLING RATE	
Sample and Hold	25 kHz
SYSTEM SPEED	
ADC conversion	<35 µs
ADC conversion, multiplexer, sample and hold and amplifier settling	<40 µs
Switch Gain Amplifier setting time including 100% overload recovery (x8 gain with 10V input)	<3 µs
NUMBER OF CHANNELS	
Expandable in groups of 4 Basic system is 32 channels	To a maximum of 128

Table 1-4 (Cont)
General Specifications

Specification	Description
INPUT SPECIFICATION	
Single-ended input	---
Impedance	Greater than 100 MΩ in parallel with 20 pf
NOISE	
Less than ±4 mV peak-to-peak RTO	±3 sigma confidence level
CROSSTALK	78 db (32 channels, 180 Hz)
RESOLUTION	One part in 4096 full-scale

CHAPTER 2
DETAILED THEORY OF OPERATION

2.1 MODES OF OPERATION

The AD15 has two basic modes of operation: program control and data channel. All transfers made in program control mode occur through the PDP-15 accumulator, while all transfers made using the data channel are made directly to memory.

2.1.1 Program Control

In program control mode, each analog input to be converted and stored requires a new set of instructions. Consequently, this method is not advantageous in the case of many conversions.

2.1.2 PDP-15 Data Channel

Two types of operation are possible using the PDP-15 data channel facility: sequential or random. In sequential operation, only one set of instructions is required to convert successive analog channels and store the results in sequential memory locations. To accomplish this, the programmer must load two memory locations (26 and 27) in the PDP-15. Location 26 is loaded in 2's complement notation with the desired number of words to be converted (word count). Location 27 is loaded with the starting address minus one, where the first converted analog input is stored (current address). After each analog input is converted, the word count is incremented. The incremented word count, in turn, causes the current address to be incremented. This ensures that the next analog input to be converted will be stored in the next sequential memory location. When the desired number of conversions have been completed, a word count overflow flag is raised, because sensing all 0s in word count location 26 causes I/O OFLO to be generated and supplied to the AD15. I/O OFLO causes the word count flag to be raised. This flag causes an interrupt, indicating completion of the required number of conversions. Bit 10 of the input status word must be a logic 1 for sequential operation.

NOTE

When employing sequential operation, only one status word is employed, and the data words are converted one after the other automatically. Therefore, it is necessary to use the same fixed-gain for all channels in this mode.

Random operation is similar to sequential operation except that a separate status word (channel address, gain, etc.) is associated with each analog channel. The status words are retrieved from one memory table and the converted data words are stored in a second memory table. Memory locations 24 and 25 are reserved for the status words, and memory locations 26 and 27 are reserved for the data words. Location 24 is loaded with one less than the 2's complement of the number of words to be converted, and location 25 is loaded with the starting address minus one where the first status word is stored. Location 26 is loaded with the 2's complement of the word count value; location 27 is loaded with the memory location minus one where the first converted data word is to be stored. Although random channels may be converted in this manner, note that the status words are sequentially stored in memory, and the data words are also stored in successive memory locations. In this way, the word count and current address cycles of the three-cycle data channel facility are utilized (refer to the PDP-15 Maintenance Manual for a more detailed description of the three-cycle data channel). Bit 10 of the input status word must be a logic 0 for random operation.

NOTE

In sequential operation, one three-cycle data break is required for each data word to be transferred into PDP-15 memory. In random operation, however, two three-cycle data breaks are required for each data word. The first three-cycle break transfers the status word to the AD15, and the second three-cycle break transfers the converted data word to PDP-15 memory. When word count overflow occurs, it is a result of location 26 overflowing indicating that all data words have been transferred.

2.1.3 Add-to-Memory

The add-to-memory feature of the PDP-15 computer allows an analog input (after it is converted to digital) to be added to the contents of a memory location. If the value added to memory is sufficient to cause a sign change in the result, a data overflow pulse is generated. If the programmer desires to cause an interrupt when a change of sign occurs, it is necessary for him to set the add-to-memory bit (bit 9) of the input status word to a logic 1 and to also set bit 6 of the status word to a logic 1. Bit 6, when set, enables the memory flag to cause a program interrupt. The add-to-memory feature is discussed in greater detail in the PDP-15 Maintenance Manual.

2.2 PROGRAM INTERRUPT

There are three sources of program interrupts: A/D DONE, data overflow (DATA OFLO), or word count overflow (WC OFLO). A/D DONE causes an interrupt under program control operation, data overflow causes an interrupt during add-to-memory, if enabled, and word count overflow causes an

interrupt during the data channel mode. When the desired number of conversions have been accomplished, the PDP-15 senses word count overflow (all 0s in location 26) and issues an OFLO signal that raises the word count flag in the AD15. This flag raises the API flag, which is fed to the M104 API Multiplexer Control Module. An output, designated API, is supplied to the PDP-15 via two I/O bus drivers. One bus driver yields PROG INT RQ and the other yields API 0 RQ. If the PDP-15 does not have the API option installed, only the PROG INT RQ is recognized. The main program traps to location 000000_8 as a result of the program interrupt, and the current contents of certain PDP-15 registers is stored in this location. The instruction in location 000001_8 is fetched and executed. This instruction is an entry to a skip chain that determines the peripheral device causing the interrupt. When this is ascertained, the program enters a service routine to service the device. On completion of servicing, control is returned to the main program.

2.3 AUTOMATIC PRIORITY INTERRUPT

If the AD15 is connected to the Automatic Priority Interrupt (API) System, it is assigned the trap address of 57_8. Conversions are done on a cycle stealing basis, similar to that described in the program interrupt section (see Paragraph 2.2). When the required number of conversions have been accomplished, the PDP-15 senses word count overflow in location 26 and generates an OFLO signal, causing the word count flag to be raised in the AD15. This signal causes the API flag to be raised which, in turn, causes API to be generated at the output of the M104 API Multiplexer Control Module. This signal is applied to two bus drivers to yield PROG INT RQ and API 0 RQ. With the API option installed and enabled in the PDP-15, the API 0 RQ overrides PROG INT RQ and the main program in the PDP-15 traps to location 57 (AD15 trap address). Location 57 contains a JMS to a service routine. The first location of the service routine stores the contents of certain PDP-15 registers. Each device associated with API has its own unique trap address; thus, it is not necessary to enter a skip chain to determine the device that caused the interrupt. A small skip chain is necessary to determine the internal source (A/D DONE, WC OFLO or MEM OFLO) of the interrupt. On completion of the servicing, a JMP * instruction returns control to the main program.

2.4 LATENCY

If there are many devices of higher priority than the AD15 operating on the data channel, the programmer should be concerned with I/O Latency Time. The I/O Latency Time must be considered because a data word that has been converted to digital is available in the AD15 buffer register for a maximum of approximately 40 μs. If this data word is not transferred to the PDP-15 memory within this time, the initial data word is lost as a result of the next data word being strobed into the buffer register.

2.5 DETAILED BLOCK DIAGRAM DESCRIPTION

The following paragraphs describe the AD15 power supplies, modes and types of AD15 operation, and a detailed block diagram description.

2.5.1 Power Supplies

The AD15 operates at 110V, 60 cycle input, and includes an analog power supply (designated H728) operating with input power of 110V at 60 cycles. The power supply provides outputs of +15V and -20V for the A877 Analog-to-Digital Converter, the A405 Sample and Hold Amplifier, the A222 Gain-Switching Amplifier, and the A124 Multiplexer Modules. In addition to the H728 Power Supply, the H721 Power Supply, housed in the H963-P Analog Equipment Cabinet, provides +5 Vdc for all the digital modules.

2.5.2 Sync Logic

In either program control or data channel mode, a convert pulse is generated (see Figure 2-1). This pulse is coupled with a sync enable signal to generate internal sync. Internal sync initiates the timing for the analog-to-digital conversion. This timing can also be initiated externally by an external sync signal that serves as the convert pulse. With internal or external sync, a delay of 3.0 μs is timed out before allowing the analog-to-digital conversion to take place. This delay provides sufficient time for amplifier settling and for stabilizing of circuit elements. At the end of the delay, a start pulse is developed and applied to the analog-to-digital converter.

2.5.3 Analog Multiplexing

The computer-specified 7-bit address of the analog input to be converted is loaded in the AD15 channel address register via I/O bus lines 11 through17. The 7-bit address is then converted to octal format as shown in Figure 2-2. The octal addresses range from 000 to 177 in the maximum system configuration.

The channel address is then supplied to a 32-channel multiplexer (minimum system configuration) along with the external analog inputs. The multiplexer logic selects the analog input specified by the channel address. The selected analog input is then multiplexed onto a common output line.

2.5.4 Gain Selection

The selected analog signal, after being multiplexed, is supplied to a single-ended gain switching amplifier with selectable gain of 1, 2, 4 or 8. The gain is selected on the basis of the voltage range of the analog inputs. For voltages in the range of 10V, unity gain is selected, whereas voltages in the range of 1.25V require a gain of 8 for full-scale deflection.

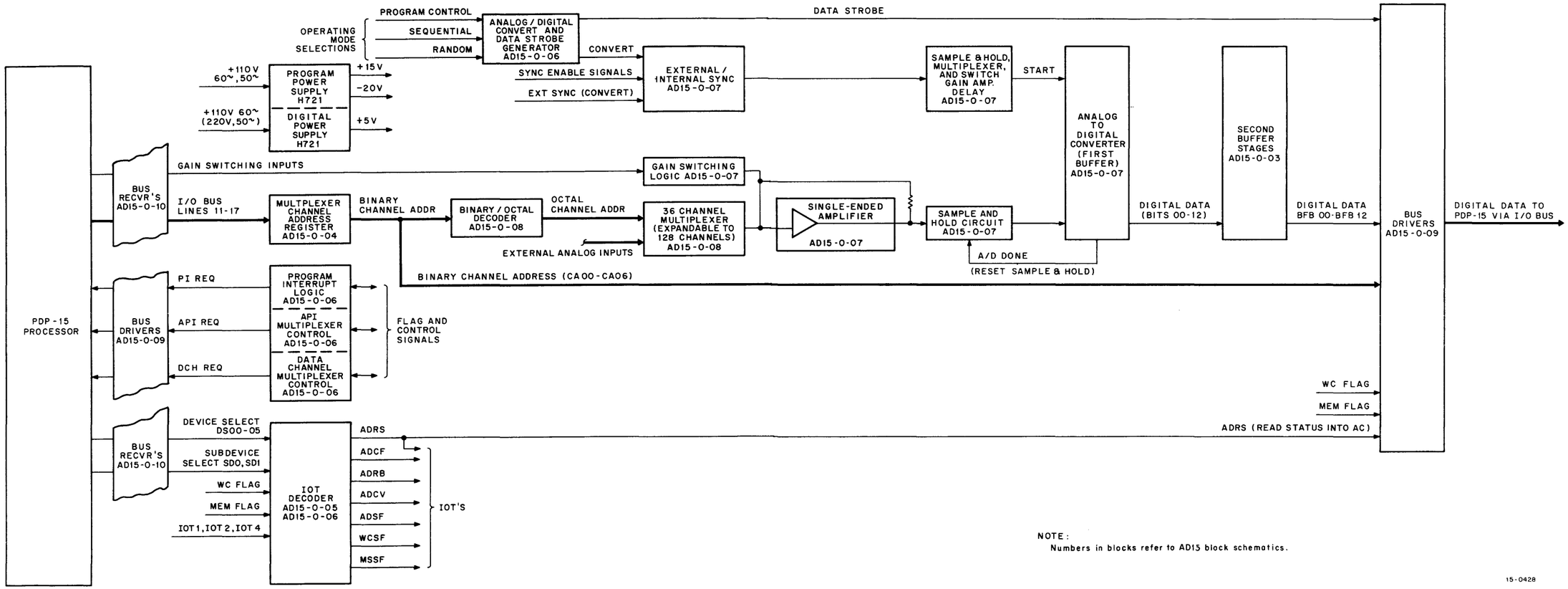


Figure 2-1 AD15 Analog Subsystem Functional Block Diagram

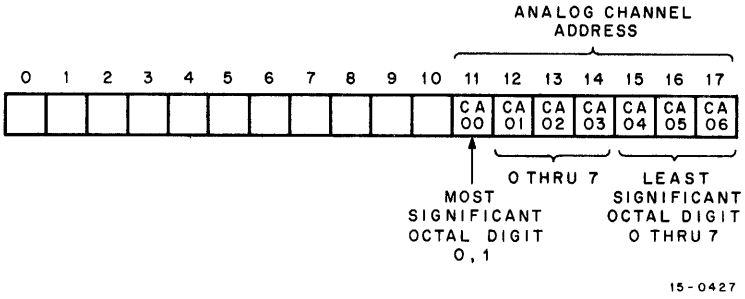


Figure 2-2 Analog Addressing

2.5.5 Sample and Hold Amplifier

From the gain-switching amplifier, the amplified analog signal is supplied to a sample and hold amplifier that stores rapidly fluctuating analog signals to allow sufficient time for analog-to-digital conversion. The input is continually tracked in the sample mode and is stored in the hold mode for the length of time needed to convert the signal from analog to digital. This time is approximately 35 μs. The sample and hold amplifier is common to all analog channels and can sample any desired input.

2.5.6 Analog-to-Digital Conversion

The analog-to-digital converter provides a 12-bit digital equivalent of the analog input with a 13th sign bit used to distinguish between positive and negative voltages. After conversion, the digital word is supplied to a series of bus drivers. On coincidence of the digital word and a data strobe, the data is strobed onto the I/O bus and transferred into the PDP-15 computer.

2.5.7 Flag Status and IOT Decoding

The PDP-15 computer can monitor the analog channel address and the status of word count overflow and memory overflow flags by issuing an ADRS instruction, one of the seven IOT instructions used in the AD15. This instruction is normally used for diagnostic purposes. The IOT instructions are decoded from the I/O bus device and subdevice select lines, the IOP pulses, and word count and memory flag status.

2.6 DETAILED LOGIC ANALYSIS

The following paragraphs provide additional detailed descriptions concerning the applicable logic schematics. These paragraphs, with the system description, functional description, and signal glossary, provide the user with adequate knowledge of system orientation and detailed theory of operation.

2.6.1 Status Register and Buffered Data Register

The upper half of block schematic AD15-0-03 represents the 13-bit buffer register (12 bits plus sign bit) that receives the 13-bit digital data from the output of the analog-to-digital converter (see block schematic AD15-0-07). This second stage of buffering stores the converted data word while waiting for the PDP-15 to accept it and allows a second conversion to be started without destroying the contents of the first conversion. The buffer register is strobed by A/D DONE at the end of each conversion. If a memory overflow flag is raised (add-to-memory), the buffer register cannot be loaded because MEM FLAG (1) H inhibits A/D DONE from strobing the register. This allows the programmer the capability of preserving the contents of the buffer register. By preserving the contents of the buffer register, the original value in memory before add-to-memory can be reconstructed. For example, assume the memory location contained the value X and the value Y was added to it, resulting in the sum of Z with a sign change. When overflow occurred, the original value (X) in memory is lost but by preserving Y in the buffer register and knowing the value of Z it is possible to reconstruct the value X.

The lower portion of block schematic AD15-0-03 shows the various control flip-flops that are set or reset by the control bits of the input status word. The flip-flops include sequential/random, add-to-memory, external/internal sync, data channel/program control, memory enable/disable, and the two gain switching flip-flops (GS01 and GS02). The control flip-flops are strobed by SELECT CLOCK, which is generated during data channel, when no word count overflow occurs or when an ADCV IOT instruction is issued under program control.

2.6.2 Multiplexer Channel Address Register

Block schematic AD15-0-04 shows the seven-stage channel address register employed. The register is preset with the starting address and is incremented on completion of each conversion in sequential mode. Note that the register uses jam transfer. Either the true (set) or complement (reset) version of each address bit is present at the input to the register. Consequently, the input address can be properly loaded into the register regardless of the previous contents.

NOTE

The input bits are inverted on the I/O bus and inverted a second time through the channel address register, restoring the bits to their original value.

The SEQ input to the register enables the register during sequential operation, and the COUNT signal causes the register to increment after each conversion. The COUNT signal is generated on block schematic AD15-0-05 as a result of A/D DONE, the DCH/PRG CTRL flip-flop in DCH mode, and WC FLAG (1) H.

The input address to the channel address register is strobed by SELECT CLOCK, which occurs as a result of an ADCV instruction or a LOAD signal. LOAD occurs during direct memory access if no word count flag is present and if IOP4 (PDP-15 to AD15 transfer) is present. During add-to-memory, it is necessary to inhibit IOP4 from affecting certain logic in the AD15. This is accomplished when both write (WR) and read (RD) signals are present; these signals occur only during add-to-memory.

2.6.3 Flag Logic

Block schematic AD15-0-05 shows the logic necessary to implement the following flags:

a. Word count flag
b. API flag
c. Memory flag
d. DCH flag
e. Done flag

In addition, the block schematic contains the read and write logic necessary to implement transfers to and from the PDP-15.

2.6.3.1 Word Count Flag - The word count flag is employed during sequential and random operation. In sequential mode, a word count location in PDP-15 memory (location 26) is preset with the 2's complement of the number of data words to be transferred. This location is incremented each time a word is converted to digital. In random mode, memory location 24 is also preset with the 2's complement of the number of data words to be transferred. In addition, however, memory location 24 is preset with one less than the 2's complement of the number of data words to be transferred. Each time a data word is transferred, location 26 is incremented; each time a status word is transferred to the AD15, location 24 is incremented. When location 26 increments from all 7s to all 0s, an overflow signal is generated indicating that the desired number of words have been converted. In addition to the overflow signal, a data channel enable signal (DCH ENB) is required to raise the word count flag indicated by WORD COUNT FLAG (0) H. The flag flip-flop can be reset by a power clear or ADCF IOT instruction, which clears all flags. The word count flag, when raised, is supplied to the PDP-15 and to the IOT decoding logic to enable a program skip, when executed. It is also supplied as an inhibit to the API, DCH, and select clock logic.

NOTE

The word count flip-flop is delayed by 2 μs due to the delay multivibrators shown on block schematic AD15-0-04 (see DEL OFLO). The flip-flop is delayed by 2 μs to enable IOP2 to allow the last data word in a series of conversions to be transferred.

2.6.3.2 API Flag - The API flag is designed to cause an API interrupt if the API option is installed in the PDP-15. When the interrupt occurs, the program traps to location 57_8. This location normally contains a jump-to-subroutine (JMS), which stores the contents of the PDP-15 program counter in the first address of the subroutine. The next instruction is the start of the AD15 service routine. On completion of the routine, a JMP * (jump indirect) returns control to the main program at the point where the interrupt occurred. The API flag can be raised under any of the following three conditions:

a. Word count overflow indicated by WORD COUNT FLAG (1) L.
b. Under program controlled transfers, when a data word has been converted (A/D DONE), and
c. Under add-to-memory operation, when overflow occurs (MEM FLAG (0) H).

The API flag, when raised, is indicated as API FLAG (0) H and can be cleared by power clear, ADCF, or clear API flag signals. The API flag is supplied to the M104 API Multiplexer Control Module to initiate an API request (API RQ 00), which is supplied to the PDP-15 via the I/O bus.

2.6.3.3 Memory Flag - The memory flag is raised when data overflow occurs during add-to-memory operation only. Data overflow occurs when the contents of an existing memory location is added to a data word in the PDP-15 adder and the sum results in a change of sign. To raise the memory flag, bit 6 (memory enable overflow) must be set, and bit 9 (add-to-memory) of the input status word must be set. These bits set the memory enable and add-memory flip-flops, respectively (see block schematic AD15-0-03). The add-memory flip-flop must be set to initiate a write request during add-to-memory operation. The write request sent to the PDP-15 causes the contents of the specified memory location to be strobed into the PDP-15 adder, where it is added with the converted data word. If overflow (change of sign) occurs, a DATA OFLO signal is generated in the PDP-15 and transferred to the AD15.

This signal and the memory enable (MEM EN) signal, generated by bit 6 of the input status word, cause the memory flag to be raised. The flag can be lowered by power clear or the ADCF IOT instruction. The memory flag is supplied to the PDP-15 computer via the I/O bus and is also applied to the IOT decoding logic to enable a program skip if memory overflow occurs.

2.6.3.4 Read/Write Logic - The read/write logic on block schematic AD15-0-05 is used to request a read (transfer to memory) or write (transfer from memory) cycle from the PDP-15. A read request is generated under any of the following condition:

a. Issuance of ADRS or ADRB IOT instructions,
b. Operating in sequential mode, or
c. Operating in random mode for a read operation.

A write request is generated under any of the following conditions:

a. In add-to-memory mode, under sequential operation or when doing a read operation.
b. In random mode, when doing a write operation.

The WRITE flip-flop (M216-E05) is wired with a toggle input and is enabled when in random mode. When the flip-flop is in the write state (reset) a status word is transferred to the AD15. When the flip-flop toggles to the read state (set) on the next DCH ENA pulse, a data word is transferred to the PDP-15.

2.6.3.5 DONE Flag - The DONE flag is raised by A/D DONE, which occurs at the end of a conversion. It is used in conjunction with the skip logic on block schematic AD15-0-06. The flag can be cleared by ADRB, ADCV, or ADCF IOT instructions or by the PWR CLR signal.

2.6.3.6 DCH Flag - The data channel (DCH) flag can be raised as a result of A/D DONE during data channel activity, providing word count overflow has not occurred. This flag is raised to allow the data word to be transferred to PDP-15 memory. A second method of raising the DCH flag occurs during data channel random operation. In this operation, it is necessary to transfer the first status word to the AD15 by means of the ADC instruction. Subsequent status word transfers occur as a result of IOP2 of the preceding data word transfer. The DCH flag can be lowered by PWR CLR or CLEAR DCH FLAG signals or by the ADCF IOT instruction. The DCH flag is first applied to the M104 Data Channel Multiplexer Control Module and then to the PDP-15 via the I/O bus as DCH REQ to initiate a data channel request to the PDP-15.

2.6.3.7 Flag Testing - The following flags generated in the AD15 can be tested by the programmer:

Flag	Raised by	Lowered by
WC Flag	I/O OFLO	ADCF or PWR CLR
API Flag	WC Flag or A/D DONE (under program control) or MEM Flag	PWR CLR or ADCF or CLEAR API FLAG
MEM Flag	DATA OFLO (MEM EN Bit must be set)	PWR CLR or ADCF
DONE Flag	A/D DONE	ADRB or ADCV or PWR CLR or ADCF

2.6.4 Device Decoders, API and Data Channel Logic

Block schematic AD15-0-06 contains the logic used to decode the various IOT instructions. Three of the IOTs (ADSF, WCSF, and MSSF) cause a SKIP signal to be generated. This signal is supplied to the PDP-15 to cause a skip of the next sequential instruction in the main PDP-15 program.

NOTE

The IOT instructions associated with transferring status to the AD15 are enabled by an IOT 04 signal (bit 15 of status word), and the IOT instructions associated with transferring data to the PDP-15 are enabled by the IOT 02 signal (bit 16 of the status word).

A complete description of the M104 API and data channel multiplexer control modules can be found in the PDP-15 Interface Manual or the PDP-15 Module Manual.

The convert (CNVT) pulse is applied to the analog-to-digital converter when internal sync is employed. The convert pulse logic, shown on block schematic AD15-0-06, permits the convert pulse to be generated under any of the conditions below:

a. In sequential mode, the first convert pulse is generated as a result of SEQ (1) H and DEL ADCV H. All other convert pulses in this mode are generated as a result of A/D DONE, the DCH flip-flop being set, absence of the word count flag, and absence of the memory flag.

b. In random mode, the convert pulse is generated as a result of the LOAD signal (see block schematic AD15-0-06).

c. In program control mode, DEL ADCV (delayed from ADCV by 1.0 μs) causes the convert pulses to be generated.

A signal, designated DCH STROBE, is generated on AD15-0-06 and is used to raise the DCH flag (see AD15-0-05) in random mode. This signal allows input status words to be transferred to the AD15.

2.6.5 Analog Subsection

Block schematic AD15-0-07 contains the internal/external sync logic, gain switching logic, sample and hold amplifier, and analog-to-digital converter. Either internal or external sync is required to initiate the timing for the analog-to-digital conversion. If internal sync is used, the convert pulse, internally generated on AD15-0-06, initiates the timing. A delay of 4.5 μs is necessary, before the conversion is started, to allow for amplifier, multiplexer switch, and sample and hold settling. Two M302 Dual Delay Multivibrators provide this function. If external sync is employed, the conversion is not started until an external sync pulse is received (see Figure 2-3).

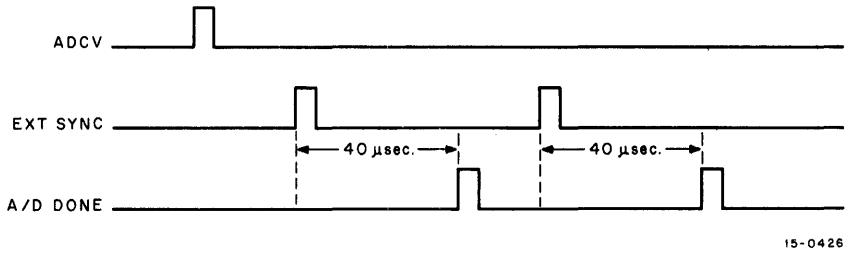


Figure 2-3 External Sync Timing Diagram

2.6.5.1 Gain Switching - Gain switching is accomplished by the A124 Multiplexer, which selects one of four possible gains (1, 2, 4 or 8) for the A222 Operational Amplifier. The gain switching bits (GS00 and GS01 of the input status word) specify the selected gain, as shown.

Gain	GS00	GS01
1	0	0
2	0	1
4	1	0
8	1	1

NOTE

When an interrupt is issued, the EXT SYNC/INT SYNC flip-flop is forced to INT SYNC to prevent undesired conversions from occurring without the programmer's knowledge. External sync pulses will cause conversions as long as the EXT/INT SYNC flip-flop is on EXT SYNC. Therefore, it is necessary to have this flip-flop on INT SYNC for the last conversion. This is accomplished by the EXT/INT SET L signal generated on drawing AD15-0-05.

2.6.5.2 Sample and Hold Amplifier - The amplified analog signal is then applied to sample and hold amplifier A405, which samples and stores the input at 25 kHz, minimum. The sample and hold amplifier provides the capability of sampling and storing extremely rapid analog fluctuations, which could not otherwise be accurately measured.

2.6.5.3 Analog-to-Digital Converter - The output from the sample and hold amplifier is applied to the A877 Analog-to-Digital Converter, where the analog signal is converted to a 13-bit digital word (12 bits plus sign bit). Conversion time is approximately 35 µs, and at the completion of this period, an A/D DONE signal is generated indicating the conversion is complete. In sequential mode, while the first conversion is waiting to be transferred to the PDP-15 memory, the second analog signal is being converted as a result of A/D DONE, which enables the next convert pulse to initiate a

conversion. After the conversion, which takes approximately 35 μs, A/D DONE is issued which, in turn, enables another convert pulse to be issued. The timing relationships for this interaction are shown on Figure 2-4.

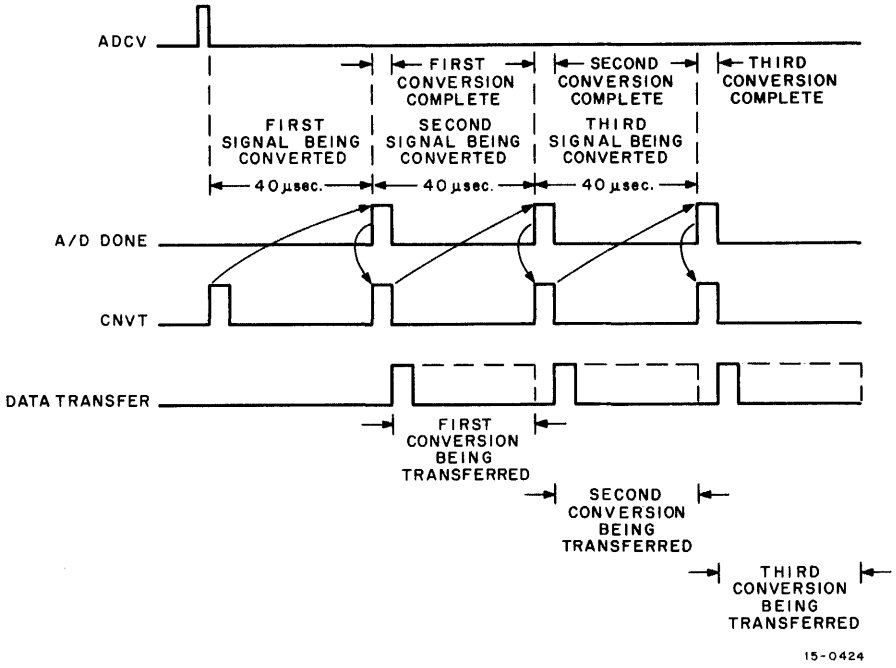


Figure 2-4 Sequential Mode Timing Relationships

In random or program controlled mode, a new status word must be loaded prior to another conversion. The timing relationships for this mode of operation are shown in Figure 2-5. The A/D DONE signal, in addition to being supplied to the circuits previously described, is also applied to the sample and hold amplifier as a reset to allow new analog inputs to be sampled and stored.

2.6.6 Binary-Octal Decoder and Analog Multiplexer

Block schematic AD15-0-08 shows the binary-to-octal decoder and a 32-channel multiplexer designated A124. This logic is necessary for a 32-channel system. For each additional 32 channels added to the system, an additional multiplexer is required; thus, 128 channels (maximum system configuration) requires four multiplexers. The multiplexers are specified by bits 0 and 1 of the analog channel address, as follows.

0-31 channels	CA00=0, CA01=0
32-63 channels	CA00=0, CA01=1
64-95 channels	CA00=1, CA01=0
96-127 channels	CA00=1, CA01=1

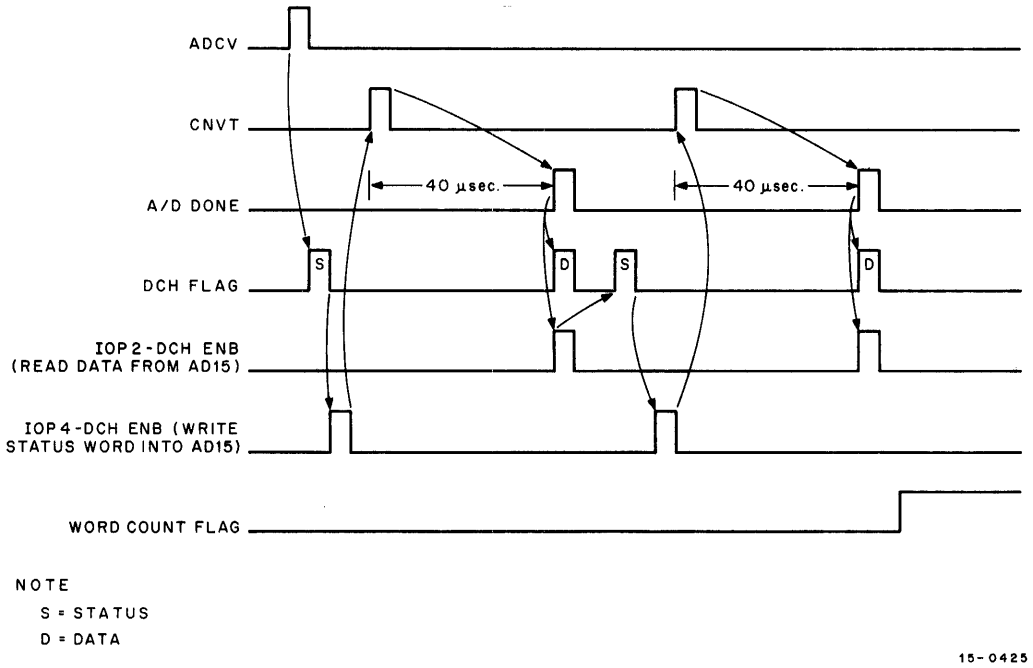


Figure 2-5 Random Mode Timing Relationships

Bits 2 through 6 of the analog channel address specify one of 32 channels within the multiplexer designated by CA00 and CA01. For example, in the minimum 0- to 32-channel system, channel 19 is addressed when bits 2, 5, and 6 are logic 1s, and bits 3 and 4 are logic 0s.

NOTE

The channel numbers shown by 32, with each new AM01-A multiplexer added.

2.6.7 I/O Bus Drivers

Block schematic AD15-0-09 (sheets 1 and 2) contain the I/O bus drivers that provide the drive necessary to transmit signals down the I/O bus to the PDP-15 computer. The contents of the 13-stage buffer register is strobed on the I/O bus when DATA STROBE occurs, while the analog channel address is strobed on the I/O bus when the ADRS IOT instruction is issued. The ADRS also enables the PDP-15 to monitor the status of the word count and memory flags.

Sheet 2 of block schematic AD15-0-09 contains the drivers for the API Trap address, the word count addresses (status and data words), and the various request signals. The API Trap address causes lines 12 and 14 through 17 to go low, and 13 to remain high. This represents the complement of the trap address, which is inverted by the I/O bus receivers in the PDP-15 to yield the true address.

The data word count address (26) is enabled by a READ signal indicating a request to transfer information to the PDP-15. The information in this case is the data word count address. I/O address lines 13, 15, and 16 are driven low and 12, 14, and 17 remain high, representing the complement of the word count address of 26. This complement is again inverted in the I/O bus receivers to yield the true version of the address. The status word count address (24) is enabled during a write operation if the AD15 is in random mode. I/O address lines 13 and 15 are driven low and 12, 14, 16, and 17 remain high, representing the complement of the word count address of 24. The complement is inverted by the I/O bus receivers to yield the true version of the address.

2.6.8 Bus Receivers, Analog Inputs, and I/O Bus Interface

Block schematic AD15-0-10 shows the I/O bus receivers that receive signals from the PDP-15 I/O bus drivers. Both the true and complement versions of the signals are available at the receiver outputs.

Block schematic AD15-0-11 shows the connections from the external analog inputs to the AD15 subsystem. A more detailed description of these connections can be found in the physical description in Chapter 1 of this manual.

Block schematic AD15-0-12 shows the I/O bus interface containing all the signals between the PDP-15 computer and the AD15 subsystem. Some of the signals shown are not used with the AD15. Figure 1-1 of this manual depicts the signals that are used and do interface between the PDP-15 and the AD15.

2.6.9 Expansion Unit AM01

Each AM01 (a maximum of three) provides the AD15 with 32 additional channels for increasing the system configuration. Block schematics AM01-A-03 through AM01-A-05 show the AM01 circuitry. Block schematic AM01-A-03 shows the M908 Card that provides connections for 32 additional channels. Thus, each AM01 contains a M908 Connector to interface the PDP-15 to the external analog sources. Block schematic AM01-A-04 contains an A124 Multiplexer that provides multiplexer capability for an additional 32 channels. Block schematic AM01-A-05 shows the M935 Bus Extender Card, which is provided to jumper the operating voltages and the appropriate channel address bits to the AM01. The right-hand section of the drawing shows the M510 I/O Bus Receivers used to increase the fan-out capability for channel address bits CA05 and CA06.

CHAPTER 3
IOT INSTRUCTION FORMAT

3.1 EQUIPMENT TURN-ON/TURN-OFF PROCEDURES

There are no special turn-on or turn-off procedures associated with the AD15 subsystem. The normal PDP-15 turn-on procedure is all that is required to initiate AD15 operation.

3.2 INSTRUCTION AND DATA FORMATS

The AD15 Analog Subsystem uses a total of seven IOT instructions for system operation. These instructions provide transfer of status information and data between the PDP-15 computer and the AD15 subsystem. The IOTs also provide clearing of flags and force program skips when certain flags are raised. The IOTs are described in the following paragraphs and are followed by a description of the input status word (from the PDP-15 to the AD15), output status word (from the AD15 to the PDP-15), and the converted data word (from the AD15 to the PDP-15).

3.2.1 IOT TIMING

For a description of IOT Timing, refer to the PDP-15 Maintenance Manual.

3.2.2 IOT INSTRUCTION FORMAT

The format for the IOT instruction is shown in Figure 3-1. Bits 0 through 5 specify the IOT operation code of 70_8; bits 6 through 11 are device select bits, and bits 12 and 13 are subdevice select bits. The device select bits specify an octal code of 13_8 to uniquely address the AD15. These bits are also used in conjunction with the subdevice select bits to decode the various IOT instructions. Bit 14 is a microprogrammable bit that is used to clear the PDP-15 accumulator. Bits 15, 16, and 17 are the IOP4, IOP2, and IOP1 pulses, respectively. These bits are also microprogrammable. IOP4 is employed in the transfer of information from the PDP-15 to the AD15. IOP2 is employed in the transfer of information from the AD15 to the PDP-15. IOP1 is used for I/O skip instructions to test a device flag. For transfers between the PDP-15 and the AD15, the first 12 bits (operation code and device select code) are fixed ($7013--_8$). Bits 12 through 17 can be altered depending on the type and direction of transfer.

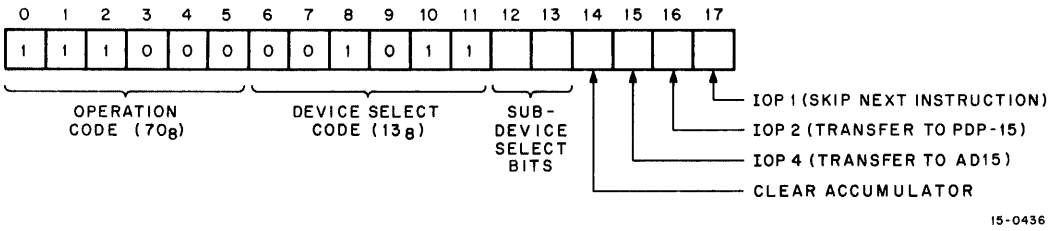


Figure 3-1 IOT Instruction Format

3.2.2.1 ADCV (convert) Octal Code 701304 - This IOT instruction transfers the contents of the PDP-15 accumulator (containing the input status word) to the AD15 Analog Subsystem, clears the A/D DONE flag, and initiates timing for the analog-to-digital conversion.

3.2.2.2 ADRB (read data buffer) Octal Code 701302 - This IOT instruction transfers the converted data from the AD15 data buffer to the PDP-15 accumulator and clears the A/D DONE flag.

3.2.2.3 ADRS (read status register) Octal Code 701342 - This IOT instruction transfer certain contents of the AD15 status register to the PDP-15 accumulator (see Paragraph 3.2.3). The status register contains selected gain data, analog channel address, and designated control functions, such as mode, type of operation, sync selection, memory overflow, etc.

3.2.2.4 ADCF (clear all AD15 flags) Octal Code 701362 - This IOT instruction clears all AD15 flags. These flags include word count overflow, memory, A/D DONE and DCH flags.

3.2.2.5 ADSF (skip on A/D DONE flag) Octal Code 701301 - This IOT instruction is a skip instruction that causes a program skip of the next sequential instruction if the A/D DONE flag is raised.

3.2.3 Output Status Word Format

The output status word is a word in the AD15 containing information regarding analog channel selection, and word count and memory sign overflow (see Figure 3-2). The AD15 status can be monitored by transferring the output status word to the PDP-15 accumulator via an ADRS IOT instruction. Bits 0 through 3 of the output status word are not used. A logic 1 in bit 4 indicates a word count overflow, and a logic 1 in bit 5 indicates a memory sign overflow. Bits 6 through 10 are not used, and bits 11 through 17 represent the analog channel address.

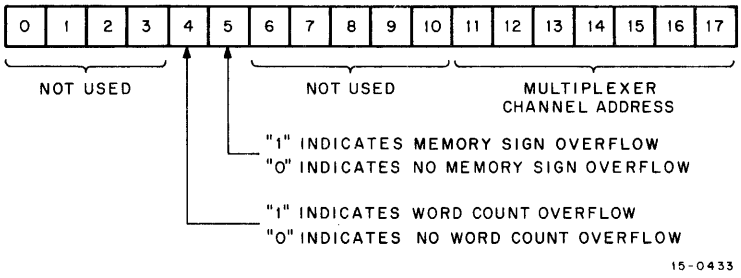


Figure 3-2 Output Status Word Format

3.2.4 Data Word Format

The format of the converted data word is shown in Figure 3-3. The converted word is a 12-bit, right-justified, 2's complement, data word with extended sign bit (bits 0 through 5). This data word represents the digital value of the analog word after conversion.

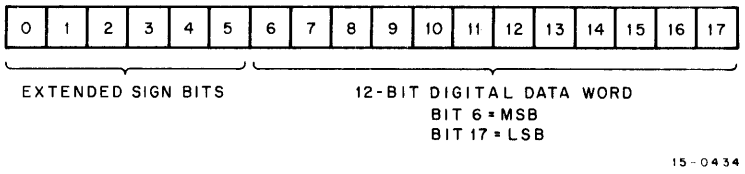


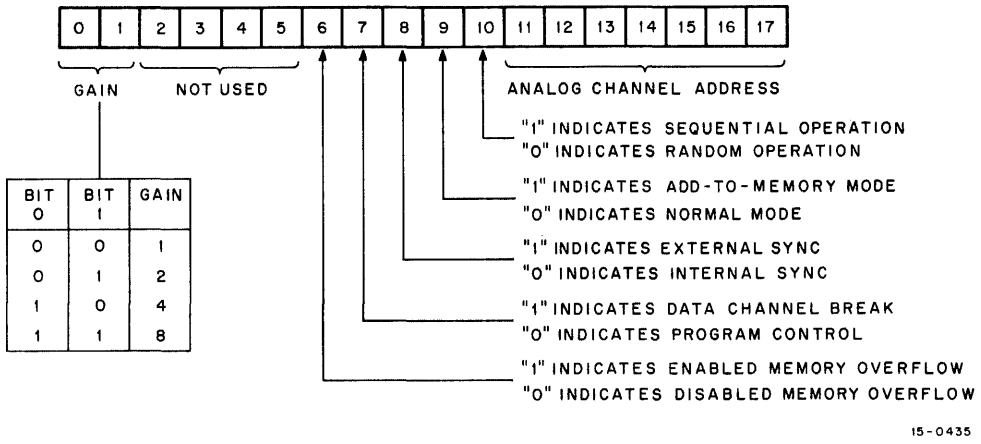
Figure 3-3 Data Word Format

3.2.4.1 WCSF (skip on word count overflow flag) Octal Code 701341 - This IOT skip instruction causes a program skip of the next sequential instruction, if the word count overflow flag is raised. The raising of the word count overflow flag signifies that the desired number of words have been transferred.

3.2.4.2 MSSF (skip on memory overflow flag) Octal Code 701321 - This IOT skip instruction causes a program skip of the next sequential instruction, if the memory overflow flag is raised. This flag is raised during an add-to-memory operation where the value added to memory was of sufficient magnitude to cause a sign change.

3.2.5 Input Status Word

The input status word is the word that is initially loaded in the PDP-15 accumulator prior to the IOT instruction. The IOT instruction causes the contents of the accumulator containing this word to be transferred to the AD15 subsystem. The format of the input status word is shown in Figure 3-4. Bits 0 and 1 determine the gain selected. Bits 2 through 5 are not used. Bits 6 through 10 are control bits and the function of each is defined in Figure 3-4. Bits 11 through 17 comprise the seven-bit analog channel address which specifies one of 128 possible addresses.



BIT 0	BIT 1	GAIN
0	0	1
0	1	2
1	0	4
1	1	8

Figure 3-4 Input Status Word Format

3.3 PROGRAMMING EXAMPLES

The following paragraphs describe several programming examples that illustrate the capabilities of the AD15 in the various modes and types of operation. These examples are described for illustrative purposes and are not intended to replace existing software.

3.3.1 Program Control Mode

The following program is an example of a program controlled transfer, where channel 74_8 is to be converted from analog-to-digital, a gain of 4 is to be selected, and external sync is to be employed. The results of the conversion are read into the accumulator.

```
000200/200210        LAC 210
000201/701304        ADCV
000202/701301        ADSF
000203/600202        JMP. -1
000204/701312        CLAI ADRB
000205/740040        HLT

000210/401074        INPUT STATUS WORD
```

The first instruction (LAC 210) loads the accumulator with the contents of location 210, which is the input status word. The format of the input status word for this example (401074) is shown in Figure 3-5. For those bits which are not used or are "don't cares", logic 0s have been assumed. The results are the same if logic 1s are assumed; the only difference is the octal value of the status word.

The computer has set up the status word specifying the various parameters for the conversion (see Figure 3-5). The ADCV instruction then transfers the status word in the accumulator to the AD15, clears the A/D DONE flag, and initiates timing for the conversion. The ADSF (skip on A/D flag) and

JMP. -1 instructions form a waiting loop that allows time for the conversion to be completed. On completion of the conversion, the A/D flag is raised and the ADSF instruction causes a program skip of the JMP. -1 instruction. The CLA! ADRB instruction clears the accumulator and transfers the converted data word of channel 74_8 to the PDP-15 accumulator. The next sequential instruction (HLT) halts the program. Thus, the analog signal in channel 74_8 has been converted to digital and transferred to the PDP-15 accumulator.

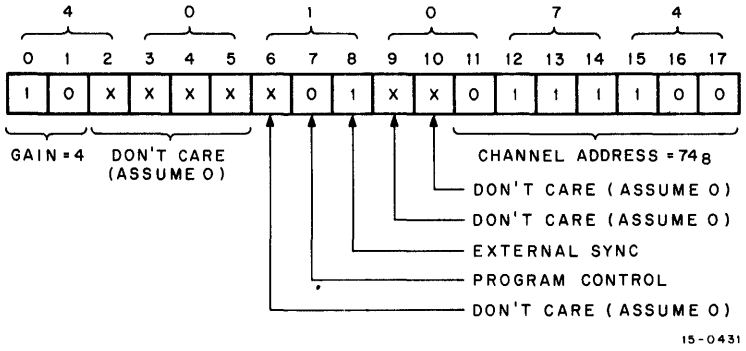


Figure 3-5 Example of Program Control Input Status Word

3.3.2 Data Channel Mode - Sequential Operation

The following program uses the sequential feature of the data channel mode of operation. The analog inputs from 16_8 successive channels starting at location 37_8 are to be converted to digital data. The converted data is to be stored in successive locations, starting at location 400. The following parameters are to be selected:

Gain = 1
Add-to-memory feature
Enable memory sign overflow
Internal sync

Initially, it is necessary to preload the word count and current address locations (26, and 27, respectively). The word count location is loaded with 777762_8 (2's complement of 16_8). The current address location is loaded with one less than the starting address or 000377_8, because the current address is incremented before the first conversion takes place. Consequently, the first converted word is transferred to location 400, the second to location 401, etc.

Figure 3-6 shows the format of the status word associated with this example; this status word is initially stored in location 000170.

The following sample program, starting at location 100, accomplishes the successive conversions previously stated.

```
000100/200170        LAC 170
000101/701304        ADCV
000102/701341        WCSF
000103/600102        JMP. -1
000104/600350        JMP 350

000170/006637        Input Status Word
```

The first instruction loads the status word stored in location 000170 (006637) into the accumulator. The ADCV instruction transfers the status word to the AD15, clears the A/D DONE flag, and initiates the timing for the conversion.

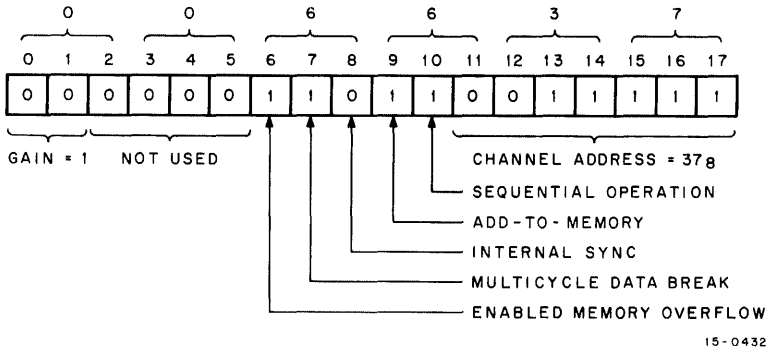


Figure 3-6 Example of Sequential Mode Status Word

The next two instructions (WCSF and JMP. -1) form a waiting loop for the conversion to be completed. The PDP-15 can be programmed to execute normal program sequences during this time. At the conclusion of the conversion, the AD15 issues an A/D DONE signal and requests a data channel break. When the PDP-15 grants this request, the word count is incremented to 777763, the current address is incremented to 400, and the converted data word is transferred to the PDP-15 and stored in location 400. While the AD15 is converting the next data word, the PDP-15 is free to operate normal program sequences. After the data word is converted, another A/D DONE signal is generated and a second data channel request is initiated. When the request is granted, word count is incremented to 777764, current address is incremented to 401, and the data word is then transferred to memory location 401. The process continues until the word count transitions change from all 7s to all 0s. The PDP-15 senses this as word count overflow and generates an overflow signal. This signal is then sent to the AD15 to raise the word count flag. This flag causes a program interrupt, or automatic priority interrupt to occur if these systems are enabled. The interrupt, when acknowledged, indicates that the required number of data words have been converted and stored in the PDP-15 memory. In the preceding example, when the word count flag is raised, the WCSF instruction causes a program skip of the JMP. -1 instruction and allows execution of the JMP 350 instruction to occur.

3.3.3 Data Channel Mode - Random Operation

The following program illustrates random operation in the data channel mode. Convert the following three channels using the control functions indicated:

a. Channel 114 (octal) - gain of 1, add-to-memory mode, enabled memory overflow, internal sync

b. Channel 002 (octal) - gain of 4, normal mode, disabled memory overflow, external sync

c. Channel 021 (octal) - gain of 8, normal mode, disabled memory overflow, internal sync.

The first status word is stored at location 600, and the first data word is to be stored at location 700. The format of each of the status words is shown in Figure 3-7.

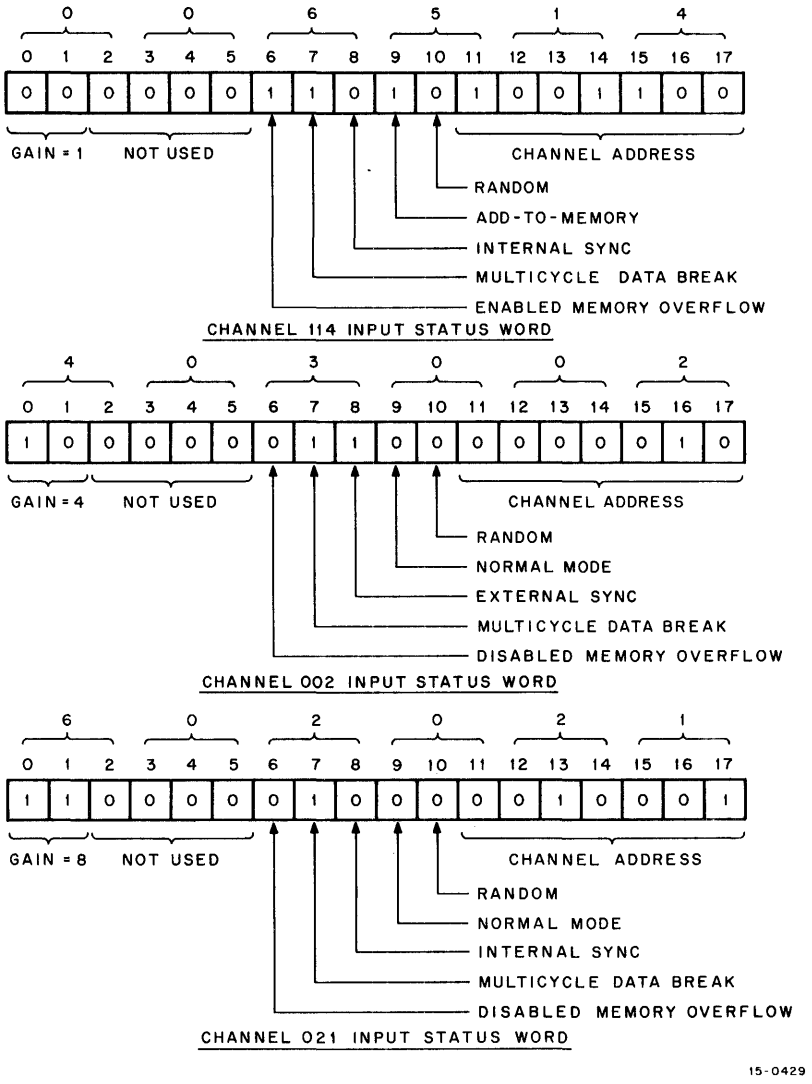


Figure 3-7 Examples of Status Words - Random Operation

The status words and data words are stored as follows:

000600/006514	
000601/403002	Status Words
000602/602021	
000700/XXXXXX	
000701/XXXXXX	Data Words
000702/XXXXXX	

In addition to formatting the status words, word count and current address for both the status word table and data word table must be preloaded as shown below:

000024/777774	Word count (2's complement) status words plus one
000025/000577	Current address of first status word minus one
000026/777775	Word count (2's complement) data words
000027/000677	Current address of first data word minus one

The program, starting at location 100, is shown below:

000100/700042	ION
000101/200600	LAC 600
000102/701304	ADCV
000103/701341	WCSF
000104/600103	JMP. -1
000105/700002	IOF
000106/600350	JMP 350

The ION instruction turns the program interrupt facility on, so that interrupts can be acknowledged by the PDP-15. The LAC 600 instruction loads the first status word (006514) into the accumulator.

NOTE

The LAC 600 instruction is a convenient means of establishing DCH and RANDOM mode operating bits. The other information in the status word is ignored. The status word will be retrieved during a data channel break, at which time the whole word will be utilized.

The next instruction, ADCV, specifies the mode of operation to the AD15, clears the flags, and initiates the first DCH request. When the request is granted by the PDP-15, the DCH request causes the word count and current address of the first status word to be incremented. LOC 24 is incremented to 777775, and LOC 25 is incremented to 000600. The first status word is then transferred to the AD15 from location 600, and the conversion on channel 114 is started. When the data is converted, the AD15 issues an A/D DONE signal that causes a second DCH request. When the second request is granted locations 26 and 27 are incremented to 777776 and 000700, respectively. The first data word is then transferred to the PDP-15 and stored in memory location 700. The transfer of this data word

causes another DCH request to be raised and again, when granted, status word locations 24 and 25 are incremented to 777776 and 000601, respectively. The second status word is now transferred to the AD15 from location 601, and the second conversion is started. When the data is converted the AD15 again issues an A/D DONE signal that raises another DCH request. When this request is granted the data word locations (26 and 27) are incremented to 777777 and 000701, respectively. The second data word is transferred to the PDP-15 and stored in location 701. The transfer of this data word causes another DCH request to be raised; when granted, locations 24 and 25 are incremented to 777777 and 602, respectively. The third status word from location 602 is now sent to the AD15, and a conversion on channel 21 is started. When the conversion is complete, the AD15 issues another A/D DONE signal that raises another DCH request. This request, when granted, causes locations 26 and 27 to be incremented to 000000 and 702, respectively. The third data word is now transferred to the PDP-15 and stored in LOC 702.

Because LOC 26 has incremented from all 1s to all 0s, the PDP-15 senses word count overflow and generates an I/O OFLO signal that causes the AD15 logic to generate a program interrupt or automatic priority interrupt. When word count overflow has been sensed, the process is complete and no further DCH requests are raised.

CHAPTER 4
INSTALLATION AND ADJUSTMENTS

4.1 INSTALLATION PLANNING

The AD15 is installed in the upper portion of the H963-P Analog Equipment Cabinet (see D-AR-PDP15-0-2). The AD15 Wired Frame Assembly has the following dimensions:

Width	19 in.
Depth	1.5 in.
Height	17 in.

The associated H728 Analog Power Supply mounts on the left side of the cabinet.

4.2 ENVIRONMENTAL REQUIREMENTS

The AD15 and PDP-15 operate in identical environments; the operating environmental limitations are listed in Chapter 1 of this manual.

4.3 INSTALLATION PROCEDURE

The following steps outline the recommended installation procedure for the AD15 Analog Subsystem:

Step	Procedure
1	Unpack the AD15 from the shipping container and inspect the unit for damage. Any damage claims should be made to the DEC district supervisor.

NOTE

DEC field service personnel should be available for consultation on potential problems.

Step	Procedure
2	Remove the tape holding the modules and cables in place and verify that the modules and connectors are seated in the proper connector slots (refer to Drawing D-AD-7007029-0-0).
	NOTE If this is the first AD15 purchased by user, it will be shipped in the Analog Equipment cabinet.
3	Mount the AD15 Wired Frame Assembly in the assigned location (H963-P Analog Equipment Cabinet), using the appropriate hardware.
4	Install the analog power supply and chassis subassembly in the assigned location (refer to Drawing E-UA-AD15-0-0).
5	Connect the H728 Analog Power Supply cable from the power supply to AD15 subsystem.
6	Determine where I/O bus is terminated; remove four M909 Terminator Cards and install the BC09B I/O Bus Cable between this point and the AD15. If the AD15 is the last device on the bus, install the M909 Terminator Cards in the AD15.
7	Perform the acceptance checkout of the AD15 logic and analog circuits using the MAINDEC 15-D6GA-D(D) Diagnostic Program and Acceptance and Calibration Procedure A-SP-AD15-0-15.
8	Perform calibration procedure in accordance with A-SP-AD15-0-15.
	NOTE When the acceptance test and calibration procedure has been successfully performed, the system is considered operational, and the user can connect his inputs to the system.
9	If user is not planning to use external sync, the external sync pin connection (refer to logic diagram AD15-0-07) should be grounded.
	NOTE Be certain to disconnect from ground the external sync connection, if it is desired to use external sync at some future date.
10	If the user's system is greater than the 32-channel configuration, involving the addition of one or more AM01-A system units, jumper wires must be connected for the various AM01-A units (see Figure 4-1).
11	If the AD15 subsystem is larger than the basic 32-channel configuration, install the M935 Bus Connector Cards in slots A1 and A4 of appropriate AM01-A system unit expansion (refer to Drawing D-AD-7007029-0-0).

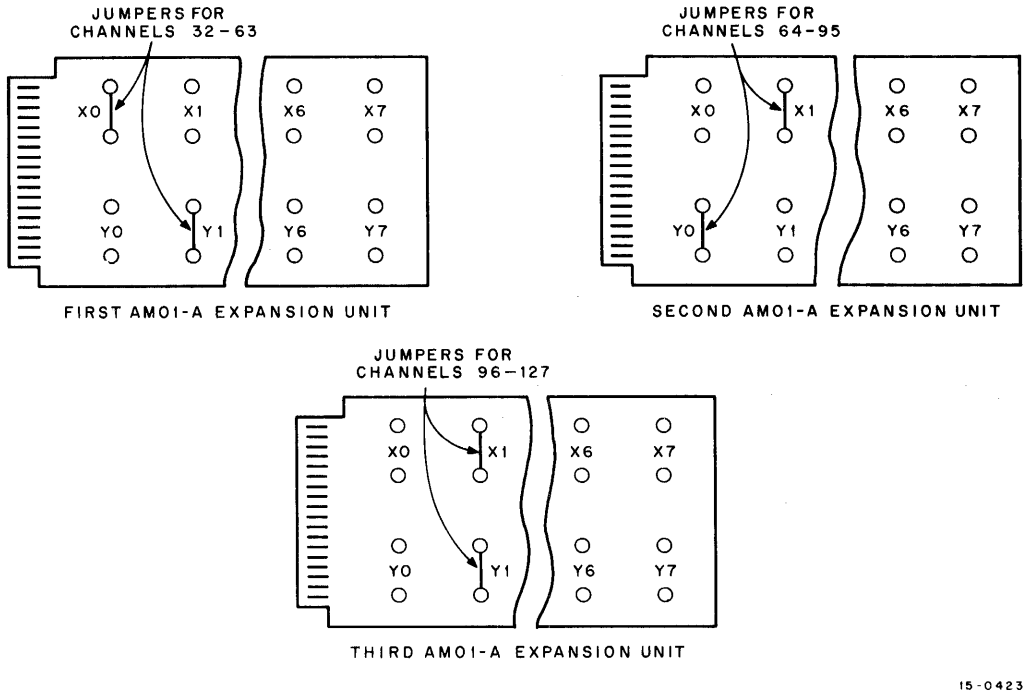


Figure 4-1 Jumper Connections for G729 Card

4.4 ADJUSTMENTS

AD15 adjustment should never be undertaken until it is confirmed that a failure is due to circuit aging or misalignment, rather than component failure. Replacement of certain components or correction of an unsatisfactory environment may eliminate the need for adjustment.

If adjustments are necessary, Table 4-1 lists the items that are adjustable, their adjustments, and their location.

Table 4-1
Adjustments

Item	Nomenclature	Adjustment	Location
1	H728 Analog Power Supply	+15 Vdc, -20 Vdc	Left side of analog cabinet
2	A708 Voltage Regulator Card	+5 Vdc regulated	A11, B11
3	M302 Dual Delay Multivibrator (DEL ADCV) (AD15-0-06)	Both potentiometers adjusted for 500 ns	F08

Table 4-1 (Cont)
Adjustments

Item	Nomenclature	Adjustment	Location
4	M302 Dual Delay Multivibrator (DEL OFLO) (AD15-0-04)	Upper potentiometer adjusted for 1.5 μs	A08
		Lower potentiometer adjusted for 500 ns	A08
5	M302 Dual Delay Multivibrator (CONVERT) (AD15-0-07)	Upper potentiometer adjusted for 4.5 μs	A09
		Lower potentiometer adjusted for 500 ns	A09

CHAPTER 5
MAINTENANCE

When operated under normal conditions, the AD15 Analog Subsystem requires little maintenance (periodic performance of diagnostic programs, cleaning, and inspection). If preventive maintenance is required, follow the procedures outlined in this Chapter to return the equipment to optimum operating efficiency.

If a module requires replacement, refer to the spare parts list outlined in this Chapter. Do not replace a faulty component without first determining the cause of the failure. Refer to the block schematics associated with each module to determine the location of the components in question.

5.1 AD15 MAINDEC-15-D6GA-D(D) DIAGNOSTIC PROGRAM

The AD15 diagnostic program is used to test the unique hardware features of the system that cannot be tested with existing MAINDECs. The program is designed to facilitate troubleshooting by selectively exercising circuits in the AD15. Instructions and procedures for loading, operating, and interpreting the results of diagnostic tests are written in clear, concise language for beginning maintenance personnel.

The program tests are divided into the following six separate tests:

a. Logic Test - This test consists of 60 subtests that completely check out the AD15 logic. Each test is looped 2048 times for reliability.

b. Noise Test - In this test, a count spread of approximately the average of ± 1-4 is requested. A total of 1024 conversions are taken on all available A/D channels at a gain of 8. Any channel with a count spread greater than that requested is considered in error.

c. Gain Test - This test is used to determine the accuracy of the AD15 at different gain settings. Eight positive and eight negative voltages are applied to channel 0. A total of 1024 conversions are taken for every voltage and gain setting, and the average is compared against the true value for that specific setting. If the average is more than ± two counts from the true value, it is considered in error.

d. Calibration Test - This test is designed to accept a channel and gain input from the Teletype and to take continuous conversions, displaying the conversion results in the accumulator.

e. Was-Is Test - This test is used to determine the long-term stability of the AD15. The test requests a channel and gain input via the Teletype and prints out the conversion result. Then, continuous conversions are taken, and when the conversion value changes more than ± one count from the previous conversion value, the value is printed out.

f. Recovery Test - This test is used to determine the settling times of the system. With this test, both channel and gain can be changed simultaneously. A channel and gain is first selected, with eight conversions being taken followed by selection of a second channel and second gain with eight additional conversions.

5.2 PREVENTIVE MAINTENANCE

A systematic preventive maintenance program is a useful tool for averting system failures. Proper application of a preventive maintenance program is an aid to both serviceman and user, because detection and prevention of probable failures can substantially reduce maintenance and downtime.

Scheduling of computer usage should always include time for maintenance. Careful diagnostic testing can indicate problems that may only occur intermittently during on-line operation.

Weekly program checks and thorough preventive maintenance should be followed, based on the following criteria:

electrical - 1000 hours
mechanical - 500 hours

or at least quarterly.

5.2.1 Preventive Maintenance Tasks

The following tasks should be performed quarterly:

Step	Procedure
1	Clean the exterior and interior of the equipment cabinet using a vacuum cleaner, air blower, or a brush with long soft bristles, and/or cloths moistened in nonflammable solvent. If an air hose is used for cleaning, do not disturb components or wiring.
2	Lubricate hinges, slide mechanisms, and casters, with a light machine oil. Wipe off excess oil.
3	Visually inspect equipment for general condition. Repaint any scratched area with DEC black paint or Krylon glossy white No. 1501.

Step	Procedure
4	Inspect all wiring and cables for cuts, breaks, fraying, wear, deterioration, kinks, strains, and mechanical security. Tape, solder, or replace any defective wiring or cable covering.
5	Inspect the following for mechanical security: keys, switches, control knobs, lamps, connectors, transformers, fans, capacitors, etc. Tighten or replace as required.
6	Inspect all module mounting panels to ensure that each module is securely seated in its connector. Remove and clean any module that may have collected dirt or dust due to improper air filter service.
7	Inspect power supply components for leaky capacitors, overheated resistors, etc. Replace any defective components.
8	Check the output voltages (+15V and -20V) and ripple content of the H728 Analog Power Supply as specified in Engineering Specification A-SP-AD15-0-14. Use a multimeter to make these measurements without disconnecting the load. Use an oscilloscope to measure p-p ripple on all dc outputs of the supply. The outputs of the supplies are adjustable; therefore, if any output voltages are not within the specified tolerance, readjust the output voltages. If the desired output voltages are not attainable, initiate power supply maintenance. Refer to the block schematic associated with the power supply in question. If ripple content is not within specifications, the power supply is considered defective, and corrective maintenance should be performed.
9	Run AD15 programs to verify proper equipment operation.
10	Enter preventive maintenance results in a log book.
11	While running the diagnostics, vibrate the modules and wiring panels.
12	While running the diagnostics, check all analog adjustments.

5.3 CORRECTIVE MAINTENANCE

The AD15 Analog Subsystem is constructed of highly reliable modules. The reliability of these circuits, in conjunction with performance of the preventive maintenance tasks, ensures relatively little equipment downtime due to failure. If a malfunction occurs, maintenance personnel should analyze the condition and correct is as indicated in the following paragraphs.

The best corrective maintenance tool is a thorough understanding of the physical and electrical characteristics of the equipment. Persons responsible for maintenance should become thoroughiy familiar with the system concept, the block schematics, the operation of specific module circuits, and the location of mechanical and electrical components. Diagnosis and remedial action for a faulty condition can be undertaken logically and systematically in the following phases:

a. Preliminary Investigation
b. System Troubleshooting
c. Logic Troubleshooting

d. Circuit Troubleshooting

e. Repair/Replacement

f. Validation Tests

g. Recording

5.3.1 Preliminary Investigation

Before commencing troubleshooting procedures, explore every possible source of information. Analyze the problem before attempting to troubleshoot the system. Gather all available information from users who have encountered the problem, and check the system log book for any previous references to the problem.

Do not attempt to troubleshoot using complex system programs alone. Run the AD15 MAINDEC 15-D6GA-D(D) Diagnostic program and select the shortest, simplest program available that exhibits the error conditions.

5.3.2 System Troubleshooting

When the problem is understood and the proper program has been selected, the logic section of the system at fault should be determined. Obviously, the program that has been selected gives a reasonable idea of what section of the system is failing. However, faults in equipment that transmit or receive information, or improper connection of the system, frequently give fault indications similar to those caused by computer malfunctions.

5.3.3 Logic Troubleshooting

Before attempting to troubleshoot the logic, make certain that proper and calibrated test equipment is available. Always calibrate the vertical preamp and probes of an oscilloscope before using. Make certain the oscilloscope has a good ac ground and keep the dc ground from the probe as short as possible.

Use the oscilloscope to trace signal flow through the suspected logic element. Oscilloscope sweep can be synchronized by control pulses or by level transitions that are available on individual module terminals at the wiring side of the logic.

CAUTION

When probing the logic, do not short between pins. Shorting of signal pins to power supply pins may result in damage to components.

5.3.4 Circuit Troubleshooting

Engineering schematic diagrams of each module used in the AD15 are available; refer to these diagrams for detailed circuit information.

Visually inspect the module on both the component side and the printed wiring side to check for overheated or broken components or etch. If this inspection fails to reveal the cause of trouble or to confirm a fault condition observed, use the multimeter to measure resistances.

CAUTION

To avoid damaging components, do not use the lowest or highest resistance ranges of the multimeter when checking semiconductor devices. The X10 range is suggested.

Measure the forward and reverse resistances of diodes; diodes should measure approximately 20Ω forward and more than 1000Ω reverse. If readings in each direction are the same and no parallel paths exist, replace the diode.

Measure the emitter-collector, collector-base, and emitter-base resistances of transistors in both directions. Short circuits between collector and emitter, or an open circuit in the base-emitter path, cause most failures. A good transistor indicates an open circuit in both directions between collector and emitter. Normally 50 to 100Ω resistance exists between the emitter and the base, or between the collector and the base in the forward direction, and an open circuit condition exists in the reverse direction. To determine forward and reverse directions, consider a transistor as two diodes connected back to back. In this analogy, PNP transistors would have both cathodes connected together to form the base, and both the emitter and collector assume the function of an anode. In NPN transistors, the base would be a common-anode connection, and both the emitter and collector, the cathode.

Multimeter polarity must be checked before measuring resistance, because many meters apply a positive voltage to the common lead when in the resistance mode.

Because ICs contain complex integrated circuits with only the input, output, and power terminals available, static multimeter testing is limited to continuity checks for shorts between terminals. IC checking is best accomplished under dynamic conditions using a module extender to make terminals readily accessible. Using AD15 block schematics and module schematics, proceed as follows to locate an IC on a circuit board:

Step	Procedure
1	Hold the module with the handle in your left hand; component side facing you.
2	ICs are numbered starting at the contact side of the board, upper right-hand corner.
3	The numbers increase toward the handle.
4	When a row is complete, the next IC is located in the next row at the contact end of the boards (see Figure 5-1).
5	The pins on each IC are located as illustrated in Figure 5-2.

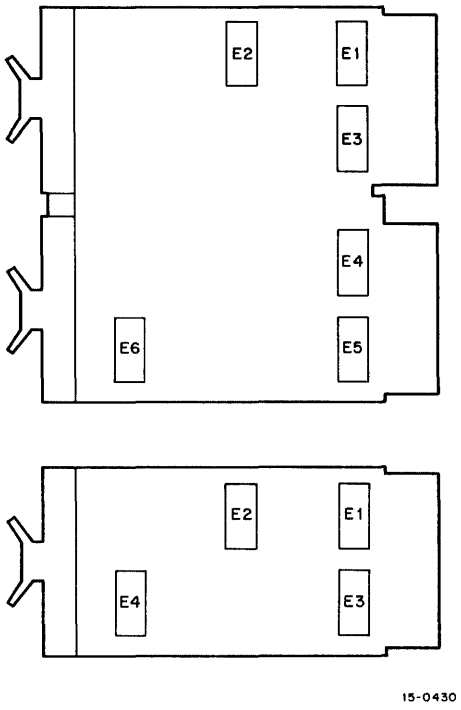


Figure 5-1 IC Location

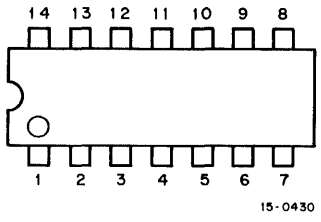


Figure 5-2 IC Pin Location

5.3.5 Validation Tests

Always return repaired modules to the location from which they were removed. If a defective module is replaced by a new module while repairs are being made, tag the defective module, and note the location from which it was taken and the nature of the failure. When repairs are completed, return the repaired module to its original location, and confirm that the repairs have resolved the problem by running all tests that originally exhibited the problem.

NOTE

If modules have been moved during the troubleshooting period, return all modules to their original positions before running the validation tests.

5.3.6 Recording

A log book (supplied) should be maintained regarding AD15 failures and corrective maintenance. All maintenance should be recorded in this book. Record all data indicating the symptoms of the fault, the method of fault detection, the component at fault, and any comments that would be helpful in maintaining the equipment in the future.

The log should be maintained on a daily basis, recording all operator usage and corrective maintenance results.

5.4 TEST EQUIPMENT

To service the AD15 Analog Subsystem, the equipment listed in Table 5-1 is recommended. If recommended equipment is not available, alternate equipment with the same performance specification should be used.

Table 5-1
Maintenance Equipment

Equipment	Specifications	Equivalent
Multimeter	10 kΩ/V - 20 kΩ/V	Triplett Model 310
Oscilloscope	dc to 50 mc with calibrated deflection factors from 5 mV to 10V/div. Maximum horizontal sweep rate of 0.1 μs/div. Delaying sweep is desirable and dual trace is a necessity.	Tektronix Type 453

Table 5-1 (Cont)
Maintenance Equipment

Equipment	Specifications	Equivalent
Probes	X10 with response characteristics matched to oscilloscope and a X1 probe.	Tektronix Type P6010 Probe Type P6011
Recessed Probe Tip		Tektronix
Unwrapping tool for 30 AWG		Gardner-Denver H812A-505-244-475
Wire-Wrap Tool		Gardner-Denver A-20557-29
30 AWG bit for wrap tool (H810)		Gardner-Denver 504221
Sleeve for 30 AWG bit		Gardner-Denver 500350
Flip-Chip Module Extender		DEC No. W980
Jumper Wires		Assorted lengths affixed with 30 AWG termipoint connectors
Null Meter Model MV100G (Precision Power Supply)	Measurement Mode Range: 0 to ± 11.1110 Vdc (resolution: 1V) Input Impedance: infinite at null; 2 kΩ off null. Max. Sensitivity: 25 μV/minor division. Zero Control: Front panel zero meter control calibration balances automatically. Output Mode Range: 0 to ± 11.1110 Vdc (resolution: 1 μV) Absolute Accuracy: ± .01% or 50 μV (of setting) High range and .01% or ± 2 μV (of setting) low range Output Current: 10 mA Power Requirements: 105 to 125 Vac; 50-65 Hz; 2W Protection: Short circuit and overload protected front panel overload indicator; recovery automatic. Vernier: ± .001V (W/Disable switch for zero) Output Impedance: <.03 Ω on high range and <20 Ω on low range.	Electronic Development Corp.
Pulse Generator	Data Pulse 101 or equivalent	

5.5 MODULE HANDLING AND REPAIR

To insert or extract modules, first turn off all power. To gain access to components on a module, remove the module by exerting a straight, even pull on the module handle to prevent twisting of the printed-wiring board. Insert a type W380 Flip-Chip Module Extender into the vacated module mounting panel, then insert the module into the extender.

For information on module repair, refer to Volume 1 of the PDP-15 Maintenance Manual. Do not attempt to repair, adjust, or calibrate the A877 Analog-to-Digital Converter board except as noted in the Acceptance and Calibration procedure (A-SP-AD15-0-15).

NOTE

Failure to follow this rule may violate the warranty.

5.6 SPARE PARTS

The customer should maintain a spare parts inventory of those modules listed in Table 5-2. For a list of recommended ICs refer to Drawing A-SB-PDP15-0-18.

Table 5-2
Spare Parts List

Quantity	Nomenclature	Module No.
1	Multiplexer	BA124
1	Switch Gain Amplifier	A222
1	Sample and Hold Amplifier	A405
1	Voltage Regulator	A708
1	Analog-to-Digital Converter	A877
1	Bus Data Interface	M101
1	Device Selector	M103
1	I/O Bus Multiplexer	M104
1	Inverter	M111
1	2-Input NAND Gates	M113
1	3-Input NAND Gates	M115
1	4-Input NAND Gates	M117
1	Binary-Octal Decimal Decoder	M161
1	Binary Counter	M211
1	Six D-Type Flip-Flops	M216
1	Dual Delay Multivibrator	M302
1	I/O Bus Receiver	M510
1	Data Bus Driver	M621
1	8-Bit Positive Input/Output Driver	M622
1	Ribbon Connector	M908
1	I/O Bus Connector	M912
1	Bus Connector Module	M935

CHAPTER 6
ENGINEERING DRAWINGS

A complete set of drawings is supplied with each AD15 Analog Subsystem. If any discrepancies exist between the drawings in this chapter and those supplied with the equipment, consider the drawing set supplied with the equipment as the most accurate.

6.1 DRAWING CODES

Digital Equipment Corporation's engineering drawings are coded to designate drawing type, major assembly, and series. A drawing number such as D-BS-AD15-0-01 contains the following information:

D	Size
BS	Type (Block Schematic)
AD15	Equipment designation
0	Manufacturing variation
01	The drawing number of a series

The drawing type codes are designated as follows:

AD	Assembly Drawing
BS	Block Schematic
DI	Drawing Index
IC	Interconnecting Cabling
MU	Module Utilization Drawing
FD	Flow Diagram
ML	Master Drawing List
SP	Specification
TD	Timing Diagram
UA	Unit Assembly
WL	Wire List

6.2 DRAWING NUMBER INDEX

Table 6-1 is an index to the engineering drawings contained in this manual.

Table 6-1
List of AD15 Drawings

Drawing Number	Title	Page
D-DI-AD15-0-01	Drawing Index List	6-7
D-BS-AD15-0-03	Status and Buffered Data Register	6-9
D-BS-AD15-0-04	Multiplexer Address Register	6-11
D-BS-AD15-0-05	Flags	6-13
D-BS-AD15-0-06	Device Decoder, API and DCH Logic	6-15
D-BS-AD15-0-07	Analog Subsection	6-17
S-BS-AD15-0-08	Multiplexer and Decoder	6-19
D-BS-AD15-0-09	Bus Drivers (two sheets)	6-21
D-BS-AD15-0-10	Bus Receivers	6-25
D-BS-AD15-0-11	Analog Inputs	6-27
D-IC-AD15-0-12	I/O Bus Interface	6-29
D-DI-AM01-A-01	Drawing Index	6-31
D-BS-AM01-A-03	Analog Inputs	6-33
D-BS-AM01-A-04	Multiplexer	6-35
D-BS-AM01-A-05	Multiplexer Address Decoder	6-37
D-AD-7007029-0-0	Wired Assembly (Includes Module Slot Locations)	6-39

6.3 SIGNAL GLOSSARY

A signal glossary is provided in Table 6-2 as a maintenance aid in detailed troubleshooting. The table lists the signals in mnemonic form, followed by a brief description of each signal.

Table 6-2
Signal Glossary

Signal Mnemonic	Description
ADCF	Clears all AD15 flags.
ADCV	Transfers contents of PDP-15 accumulator to the AD15 status register, clears A/D DONE flag, and initiates timing for the conversion.
ADD MEM (add-to-memory)	When bit 9 is a logic 1, the AD15 is in add-to-memory mode where the converted data is added to the value in an existing memory location.
ADRB	Transfers contents of AD15 data buffer to the PDP-15 accumulator. Also clears A/D DONE flag.
ADRS	Transfers contents of status register into the PDP-15 accumulator.
ADSF	Causes a program skip when an A/D flag is raised.
API ENA (Automatic Priority Interrupt Enable A)	Used to gate the API trap address onto the I/O bus.
API 0 EN IN, API 0 EN OUT	An enable signal daisy-chained from device to device. The API Multiplexer Control Module can interrupt this level, inhibiting it from all devices further down the bus. The device receives API 0 EN IN and transmits API 0 EN OUT.
API Flag	A flag raised indicating an API request to the API Multiplexer Control Module.
API 0 GR (API 0 GRANT)	A signal from the PDP-15 indicating that the API request from the AD15 has been granted.
API 0	A signal from the AD15 occurring at I/O sync time to request service from the PDP-15 on API priority level 0.
API 0 RQ	Bus driver output of API 0. (API level 0)
BFB 00 - BFB 12 (Buffered bits 00 through 12)	This is a second stage of buffering that permits a second analog-to-digital conversion to begin without destroying the results of a previous conversion.
A/D DONE (Analog-to-Digital Done)	A signal generated on completion of the analog-to-digital conversion.
CA 00 - CA 06 (Channel address 00 through 06)	Represents address of 1 of 128 possible analog input channels.
CNVT (Convert)	A pulse used with INT SYNC EN to start analog conversion during internal sync operation.
Count	A signal applied to the multiplexer address register to increment the register each time a conversion is completed in sequential mode.

Table 6-2 (Cont)
Signal Glossary

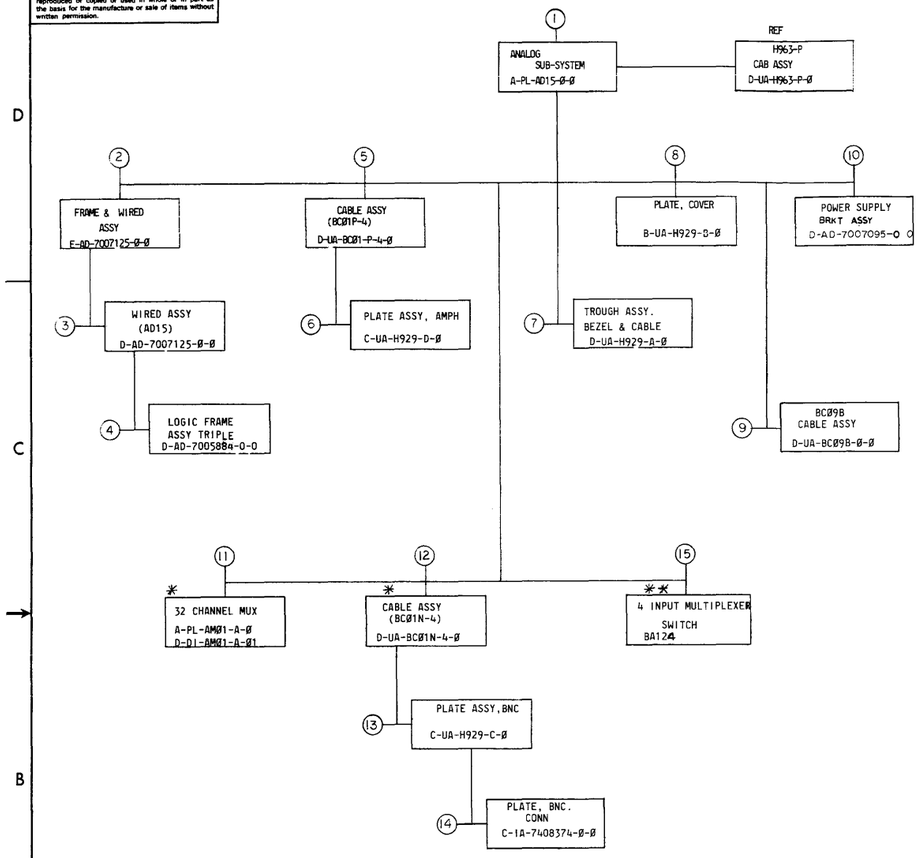
Signal Mnemonic	Description
DATA OFLO (Data Overflow)	Used by the PDP-15 to indicate that a sign change has occurred due to overflow during add-to-memory. The AD15 uses this signal to set the memory overflow flag and generates an interrupt when enabled.
DATA STROBE	An enable signal used to gate the converted data onto the I/O bus.
DCH EN A (Data Channel Enable A)	An enable signal used to gate the word count address onto the I/O bus during direct memory access mode.
DCH EN B	An enable signal used to request the PDP-15 to read, write, or add-to-memory.
DCH EN IN DCH EN OUT	An enable signal daisy-chained from device to device. The DCH Multiplexer Control Module can interrupt this level, inhibiting it from all devices further down the bus. The device receives DCH EN IN and transmits DCH EN OUT.
DCH FLAG	A flag raised to request direct memory access via data channel.
DCH GR	Issued by the I/O processor when it acknowledges a request from the AD15.
DCH	Generated in AD15, occurring at I/O sync time to request a direct memory access data transfer.
DCH RQ	Bus driver output of DCH.
DEL ADCV (Delayed ADCV)	Delayed from ADCV to permit settling of registers.
DEL OFLO	Delayed by 2.0 μs from I/O OFLO to enable IOP2; consequently, the last data word can be transferred.
DCH/PROG CTRL	This flip-flop, when set, denotes data channel operation in the AD15. When reset, it indicates program-controlled operation.
DCH STROBE	Used to initiate a data channel request during random operation.
DONE FLAG	A flag raised as a result of A/D DONE being generated.
DS0-DS5 (Device Select 0 through 5)	The six device select lines decoded from bits 6 through 11 of the IOT instruction.
EXT SYNC	Used when an external source of sync is desired with the AD15.

Table 6-2 (Cont)
Signal Glossary

Signal Mnemonic	Description
EXT SYNC EN/INT SYNC EN	Bit 8 of the I/O bus is used to load a control flip-flop with EXT SYNC EN (flip-flop set) or INT SYNC EN (flip-flop reset).
EXT/INT SET L	Used to force the EXT SYNC/INT SYNC flip-flop to internal sync on completion of conversions.
GS0, GS1 (Gain Switching)	Two bits decoded into one of four possible gain selections.
I/O ADDR 12-17 (Input/Output Address 12 through 17)	These lines constitute an input bus to the PDP-15 for delivering address data from the AD15. The address is either an API trap address or data channel word count address.
I/O Bus 00-17	A set of lines connected between PDP-15 and its peripherals for bidirectional data transfer.
I/O SYNC	A PDP-15 clock pulse issued every microsecond. The signal is used to synchronize API RQ or DCH RQ to the PDP-15.
I/O OFLO	Indicates to the AD15 that the desired number of words have been transferred on the completion of the transfer in progress. It is normally used to turn off the AD15 and to initiate an interrupt.
IOP1 (Input/Output pulse 1)	A microprogrammable control signal decoded from bit 17 of the IOT instruction. Used for I/O skip instructions to test a device flag.
IOP2	A microprogrammable control signal decoded from bit 16 of the IOT instruction, when in program control mode. This signal can also be generated during direct memory access mode when an AD15-to-PDP-15 data transfer (read request) is desired.
IOP4	A microprogrammable control signal decoded from bit 15 of the IOT instruction, when in program control mode. This signal can be generated during direct memory access mode when a PDP-15-to-AD15 data transfer (write request) is desired.
IOT1 (Input/Output Transfer 1)	Bus received version of IOP1.
IOT2	Bus received version of IOP2.
IOT4	Bus received version of IOP4.
LOAD	Used to generate CNVT pulse during random operation.
MEM EN (Memory Enable)	Enables DATA OFLO signal to raise memory flag when bit 6 is set to a logic 1.

Table 6-2 (Cont)
Signal Glossary

Signal Mnemonic	Description
MEM FLAG	This flag is raised during an add-to-memory operation when the quantity added to memory causes a change of sign.
MSSF	Causes a program skip when the memory overflow flag is raised.
PROG INT	A signal generated in the AD15 to request interruption of the program in progress so that the AD15 can be serviced. This signal causes the program to trap to location 000000 where no higher priority action is in progress. The instruction in location 000001 is then fetched and executed.
PROG INT RQ	Bus driver output of PROG INT.
PWR CLR (Power Clear)	System clear signal. Used as initializing signal for AD15 control flip-flops and registers.
RD (Read)	Used by the AD15 to specify that a data word is to be transferred from the AD15 to the PDP-15.
RD RQ	Bus driver output of RD.
SD 00, SD 01 (Subdevice code, 00, 01)	Two subdevice select lines decoded from bits 12 and 13 of the IOT instruction.
SELECT CLOCK	A control signal used to clock various control signals, gain switching and operating modes.
SEQ/RAND (Sequential/Random)	If bit 10 is a 1, the AD15 is in sequential mode where conversions are done in sequential multiplexer channels. If bit 10 is a 0, the AD15 is in random mode where conversions are taken in random multiplexer channels.
SKIP	A PDP-15 instruction generated in the AD15 to cause a program skip of the next sequential instruction.
SKIP RQ	Bus driver output of SKIP.
SYNC	Bus received version of I/O SYNC.
WCSF	Causes a program skip when the word count overflow flag is raised.
WC FLAG	A flag indicating word count overflow (desired number of words have been transferred).
WR (write)	A signal used by the AD15 to specify to the PDP-15 that a PDP-15-to-AD15 data transfer is to be made.
WR RQ	Bus driver output of WR.



NOTES:

*1. DENOTES OPTIONS TO AD15.

** SEE MODULE UTILIZATION (OPTION) 2. FOR MAX CONFIGURATION REFER TO D-AR-PDP15-Ø-2

FIND NO.	DESCRIPTION	PART NO.	DEPT USAGE PROD	CUST	F/C
1.	ANALOG SUB-SYSTEM (PL)	A-PL-AD15-Ø-Ø			
2.	FRAME & WIRED ASSY	E-AD-7007125-Ø-Ø			
	FRAME& WIRED ASSY (PL)	A-PL-7007125-Ø-Ø			
	FRAME, LOGIC MOUNTING	E-1A-7408379-Ø-Ø			
3.	WIRED ASSY (AD15)	D-AD-7007029-Ø-Ø			
	WIRED ASSY (AD15) (PL)	A-PL-7007029-Ø-Ø			
4.	LOGIC FRAME ASSY TRIPLE	D-AD-7005884-Ø-Ø			
	LOGIC FRAME ASSY TRIPLE (PL)	A-PL-7005884-Ø-Ø			
	STRAP TRIPLE FRAME	C-MD-7407513-Ø-Ø			
	CONN. BLOCK MTG FRAME	D-1A-7407507-Ø-Ø			
	288 PIN CONN BLOCK WRAP TYPE	E-SC-1205348-Ø-Ø			
5.	CABLE ASSY (BCØ1P-4)	D-UA-BCØ1P-4-Ø			
6.	PLATE ASSY, AMPH	C-UA-H929-D-Ø			
	PLATE ASSY, AMPH (PL)	A-PL-H929-D-Ø			
	PLATE, AMP	C-1A-7408376-Ø-Ø			
7.	TROUGH ASSY, BEZEL & CABLE	D-UA-H929-A-Ø			
	TROUGH ASSY, BEZEL & CABLE (PL)	A-PL-H929-A-Ø			
	TROUGH, CABLE	E-1A-7408458-O-O			
	SUPPORT, BEZEL	C-1A-7408482-O-O			
	10- 1/2 SNAP ON BEZEL	E-SC-1209225-O-O			
8.	PLATE, COVER	B-UA-H929-B-Ø			
9.	BCØ9 B CABLE ASSY	D-UA-BCØ9-B-Ø			
	BCØ9 B CABLE ASSY (PL)	A-PL-BCØ9-B-Ø			
10.	POWER SUPPLY BRKT ASSY	D-AD-7007095-O-O			
	POWER SUPPLY BRKT ASSY (PL)	A-PL-7007095-O-O			
	POWER SUPPLY DECAL, CHASSIS, POWER SUPPLY	A-DC-5309245-Ø-Ø E-1A-5309244-Ø-Ø			
11.	*32 CHANNEL MUX (PL)	A-PL-AMØ1-A-Ø			
	DRAWING INDEX LIST (AMØ1)	D-DI-AMØ1-A-Ø1			
12.	*CABLE ASSY (BCØ1N-4)	D-UA-BCØ1N-4-Ø			
13.	PLATE ASSY, BNC	C-UA-H929-C-Ø			
	PLATE ASSY, BNC (PL)	A-PL-H929-C-Ø			
14.	PLATE, BNC CONN	C-1A-7408374-Ø-Ø			
	BNC CONN PLATE	B-SS-7408374-Ø-1			
15.	**4 INPUT MULTIPLEXER SWITCH	BA124			

FIND NO.	DESCRIPTION	PART NO.	DEPT USAGE PROD	CUST	F/C
1.	ANALOG SUB-SYSTEM	A-ML-AD15-Ø			
	MODULE UTILIZATION LIST	K-MU/PL-AD15-Ø-Ø2			
	STATUS & BUFFERED DATA REG	D-BS-AD15-Ø-Ø3			
	MULTIPLEXER ADDRESS REG	D-BS-AD15-Ø-Ø4			
	FLAGS	D-BS-AD15-Ø-Ø5			
	DEVICE DECODERS API & DCH LOGIC	D-BS-AD15-Ø-Ø6			
	ANALOG SUB SECTION	D-BS-AD15-Ø-Ø7			
	MULTIPLEXER & DECODER	D-BS-AD15-Ø-Ø8			
	BUS DRIVERS	D-BS-AD15-Ø-Ø9			
	BUS RECEIVERS	D-BS-AD15-Ø-1Ø			
	ANALOG INPUTS	D-BS-AD15-Ø-11			
	I/O BUS INTERFACE	D-IC-AD15-Ø-12			
	ENGINEERING SPECIFICATION	A-SP-AD15-Ø-14			
	CALIBRATION & CHECKOUT PROCEDURE	A-SP-AD15-Ø-15			
	ACCEPTANCE PROCEDURE	A-SP-AD15-Ø-16			
3.	WIRED ASSY (AD15)	D-AD-7007029-Ø-Ø			
	WIRED ASSY (AD15) (PL)	A-PL-7007029-Ø-Ø			
	WIRE LIST	K-WL-AD15-Ø-13			
10.	SCHEMATIC	D-SC-1210040-O-O			

REVISIONS: REV. / CHANGE NO. / CHK

FIRST USED ON OPTION/MODEL: AD15

DRN.		DATE 10-7-70
CHK'D		DATE 11/3/70
ENG.		DATE 11/5/70
PROJ. ENG.		DATE 11/5/70
PROD.		DATE 11/6/70

NEXT HIGHER ASSY: A-ML-AD15-Ø

SCALE: —

SHEET 1 OF 1

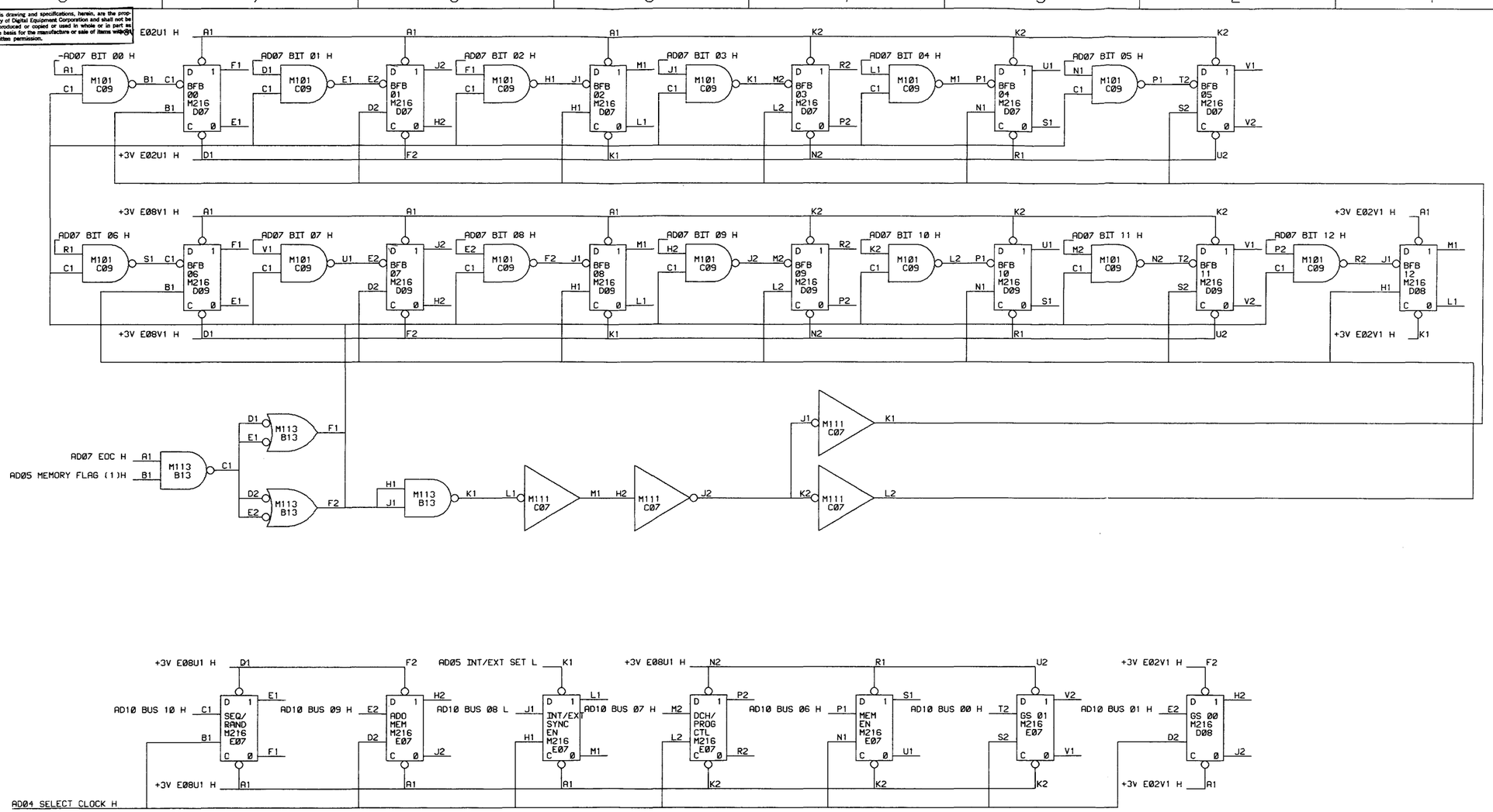
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: DRAWING INDEX LIST

SIZE D | CODE DI | NUMBER AD15-Ø-Ø1 | REV

DIST.

DEC FORM NO DRG 1119



REVISIONS		
CHK	CHANGE NO.	REV.

-PRODUCED BY THE AUTOMATED DRAFTING SYSTEM-

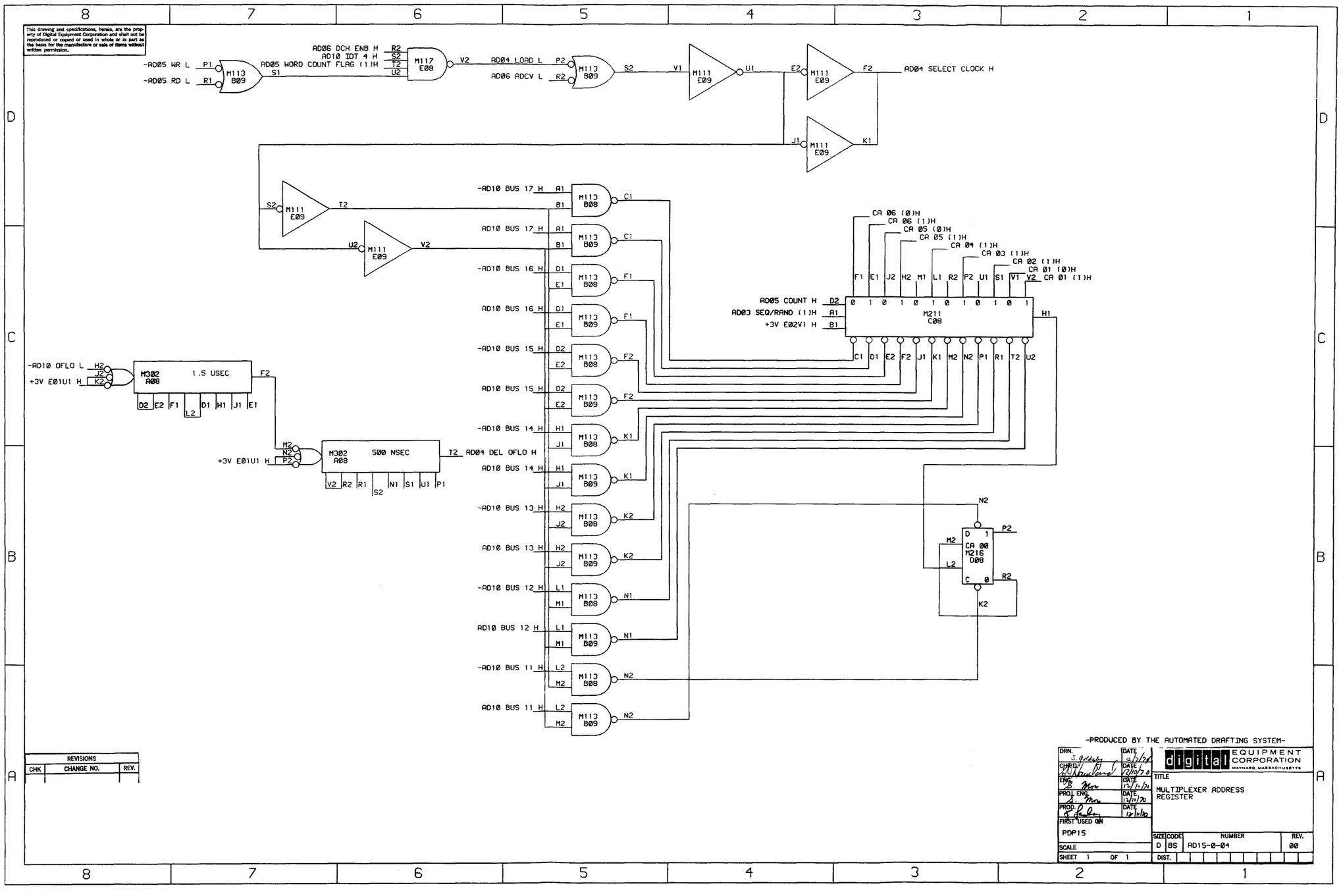
DRN. S. Goldsky	DATE 12/2/70
CHK'D [illegible]	DATE 12/10/70
ENG. [illegible]	DATE 12/10/70
PROJ. ENG. [illegible]	DATE 12/11/70
PROD. [illegible]	DATE 12/11/70
FIRST USED ON: PDP15	
SCALE	
SHEET 1 OF 1	

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: STATUS + BUFFERED DATA REGISTER

SIZE	CODE	NUMBER	REV.
D	BS	AD15-0-03	00

DIST.



-PRODUCED BY THE AUTOMATED DRAFTING SYSTEM-

REVISIONS		
CHK	CHANGE NO.	REV.

DRN. S. Goldsby	DATE 12/2/70	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHKD. D. Knowlton	DATE 12/10/70	TITLE MULTIPLEXER ADDRESS REGISTER
ENG. S. Mon	DATE 12/11/70	
PROJ ENG. S. Mon	DATE 12/11/70	
PROD. [illegible]	DATE 12/11/70	
FIRST USED ON PDP15		SIZE D · CODE BS · NUMBER AD15-0-04 · REV. 00
SCALE		DIST.
SHEET 1 OF 1		

AD10 PWR CLR L
AD06 ADCF L
M113 E02
M111 C07
AD06 DCH ENB H
AD04 DEL OFLO H
M113 E02
M111 C07
WORD COUNT FLAG M216 E06
+3V E01U1 H
AD06 CLEAR API FLAG L
M113 E02
M111 C07
AD05 WORD COUNT FLAG (1)L
AD07 A/D DONE H
AD03 DCH/PROG CTL (0)H
M113 E02
M115 E04
API FLAG M216 E06
+3V E01U1 H
AD10 B DATA OFLO H
AD03 MEM EN (1)H
M115 E04
M111 C07
MEM FLAG M216 E06
+3V E01U1 H
AD06 ADCV L
AD03 SEQ/RAND (1)H
M113 E02
M113 E02
M111 E09
WRITE M216 E06
AD06 DCH ENA H
AD03 SEQ/RAND (0)H
M113 B08
M111 E09
+3V E01U1 H
AD06 CLEAR DCH FLAG L
M113 E02
M111 C07
AD03 SEQ/RAND (0)H
AD06 DEL ADCV H
AD03 DCH/PROG CTL (1)H
M115 E03
AD05 WORD COUNT FLAG (1)H
AD05 MEMORY FLAG (1)H
M117 E08
M115 E03
DCH FLAG M216 E06
+3V E01U1 H
AD06 DCH STROBE L
M111 E09
AD03 SEQ/RAND (0)H
M113 E01
AD06 ADRB L
AD06 ADCV L
M115 E04
M111 C07
AD07 A/D DONE H
DONE FLAG M216 E06
+3V E01U1 H
AD10 PWR CLR L
M113 B08
M111 E09
AD03 INT/EXT SET L
M111 E09
AD05 COUNT H
AD06 ADRS L
AD06 ADRB L
M113 E02
M111 E09
AD03 SEQ/RAND (1)H
M113 E02
AD03 SEQ/RAND (0)H
M115 E04
M115 E04
AD05 RD H
M111 C07
AD05 RD L
AD03 DCH/PROG CTL (1)H
AD06 DCH ENB H
AD03 ADD MEM (1)H
M117 E08
M115 E04
M113 E02
AD05 WR H
M111 C07
AD05 WR L

REVISIONS		
CHK	CHANGE NO.	REV.

-PRODUCED BY THE AUTOMATED DRAFTING SYSTEM-

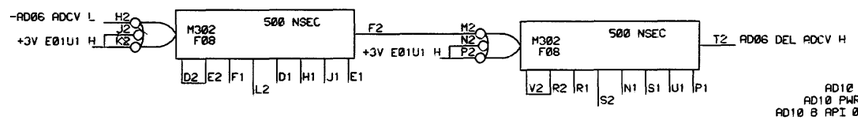
DRN. S. Goldsby	DATE 12/10/74
CHK'D. R. Chandler	DATE 12/10/74
ENG. D. Mars	DATE 12/10/74
PROJ. ENG. D. Mars	DATE 12/10/74
PROD. R. Foster	DATE 12/10/74
FIRST USED ON: PDP15	
SCALE	
SHEET 1 OF 1	

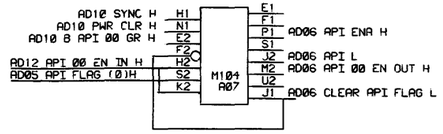
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

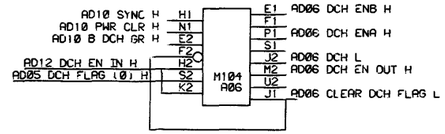
TITLE: FLAGS

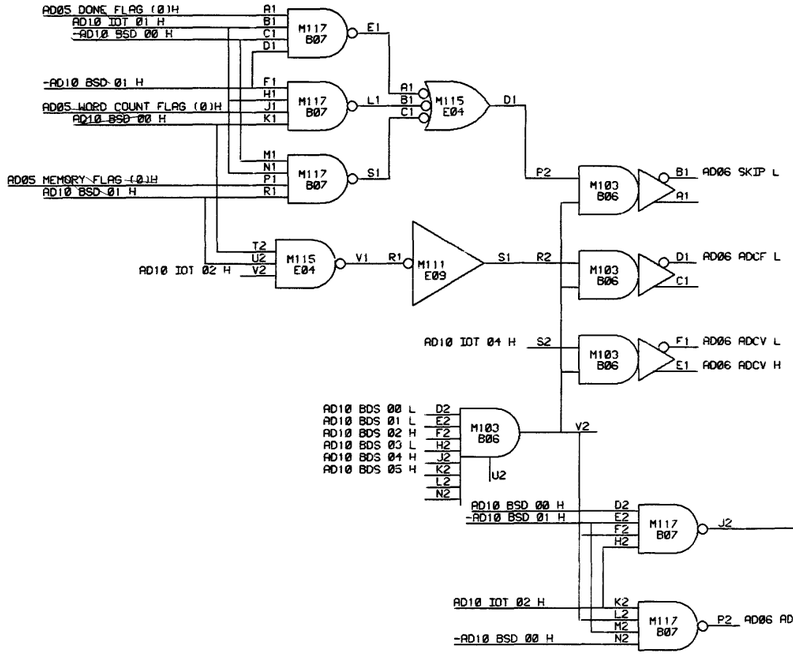
SIZE	CODE	NUMBER	REV.
D	BS	AD15-0-05	00

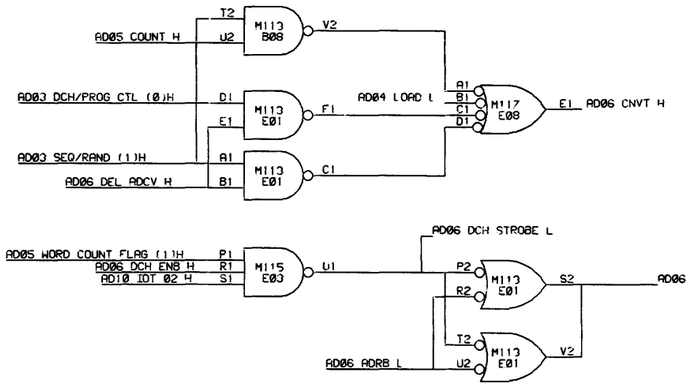
DIST.











REVISIONS		
CHK	CHANGE NO.	REV.

-PRODUCED BY THE AUTOMATED DRAFTING SYSTEM-

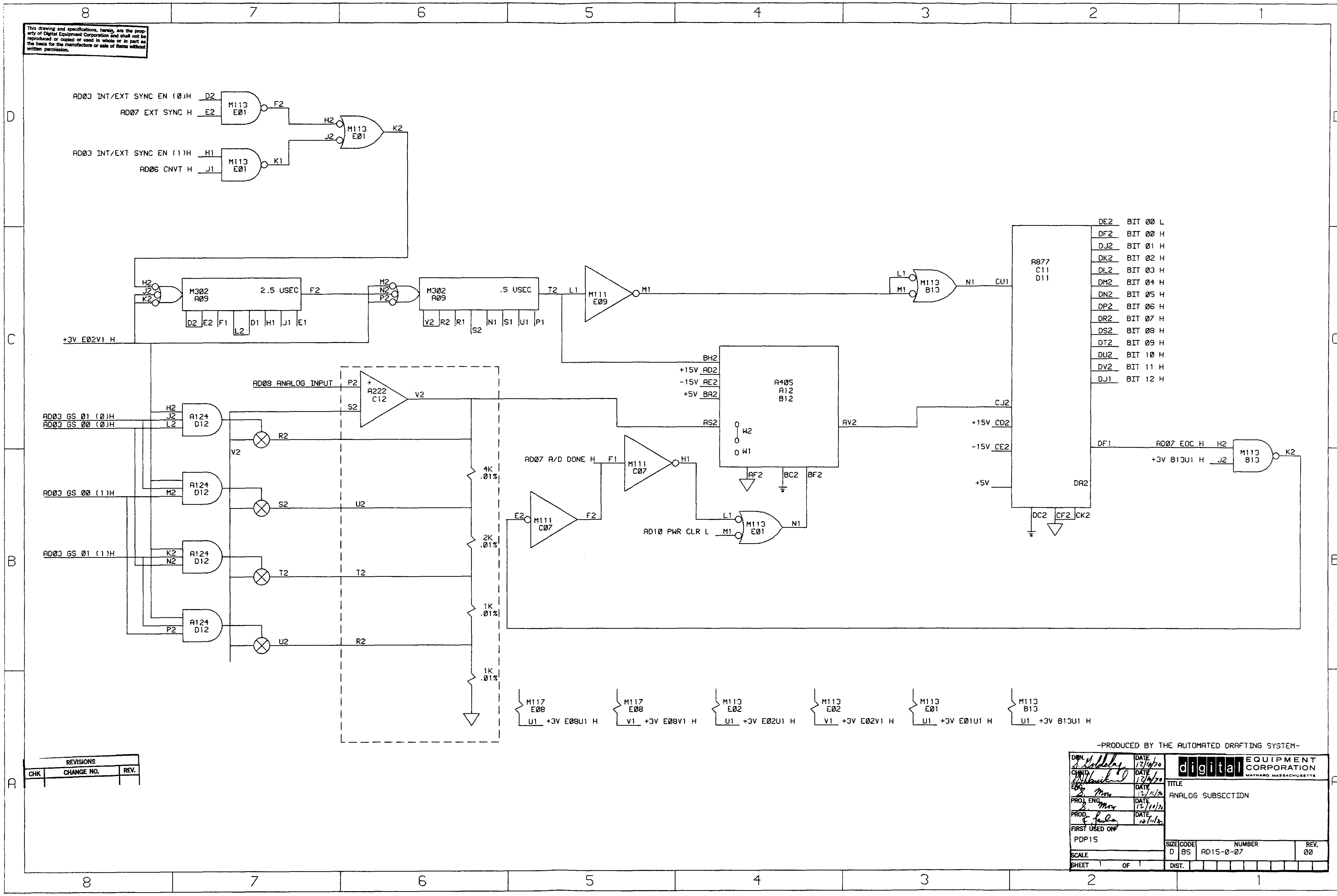
DRN.	DATE 12/17/74
CHKD.	DATE 12/20/74
ENG.	DATE 12/23/74
PROJ. ENG.	DATE 12/23/74
PROD.	DATE 12/31/74
FIRST USED ON: PDP15	
SCALE	
SHEET 1 OF 1	

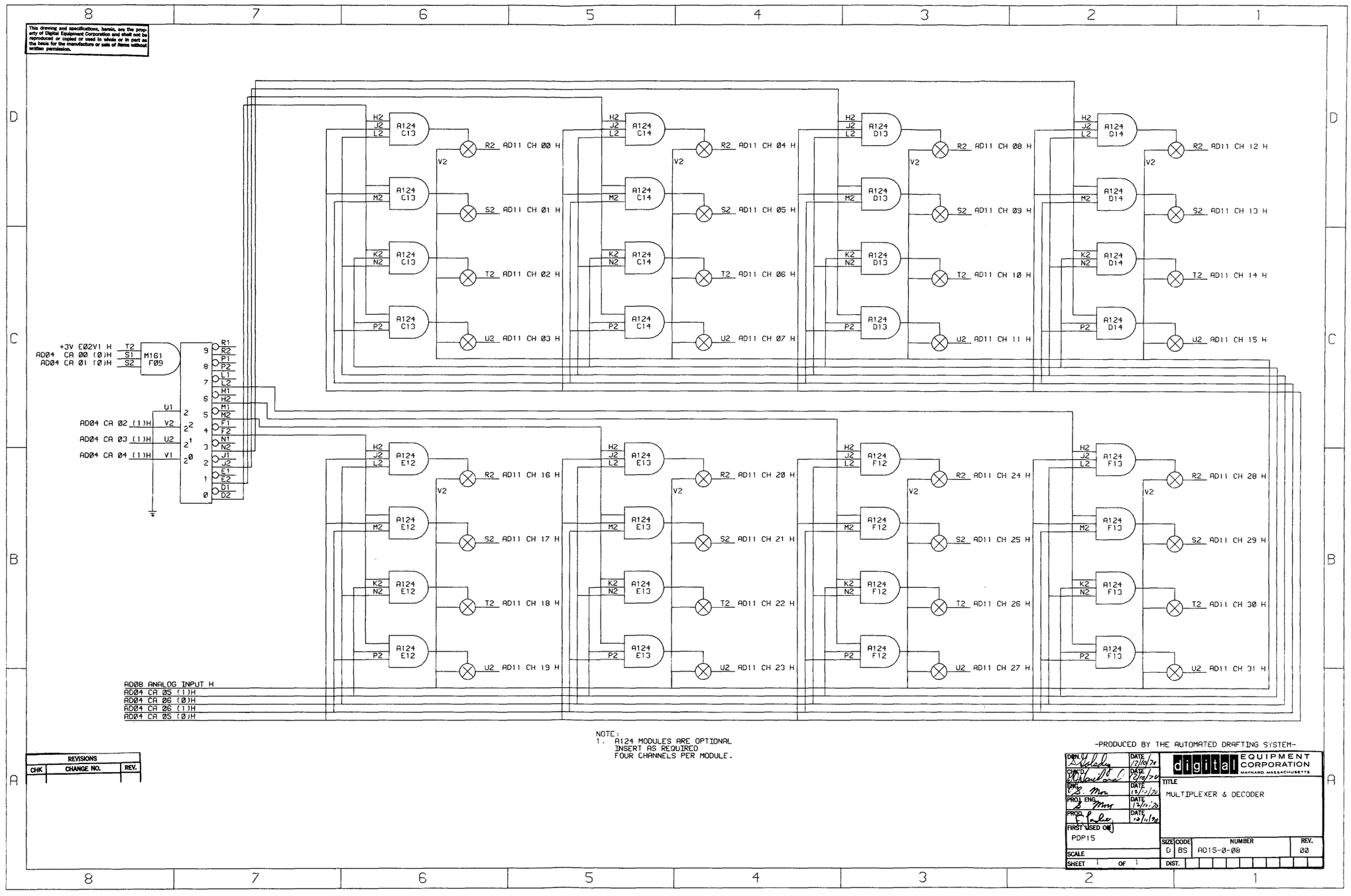
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: DEVICE DECODERS API + DCH LOG

SIZE	CODE	NUMBER	REV.
D	BS	AD15-0-06	00

DIST.


This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission.
AD03 INT/EXT SYNC EN (0)H
AD07 EXT SYNC H
AD03 INT/EXT SYNC EN (1)H
AD06 CNVT H
M113 E01
M302 A09
2.5 USEC
.5 USEC
M111 E09
M113 B13
A877 C11 D11
BIT 00 L
BIT 00 H
BIT 01 H
BIT 02 H
BIT 03 H
BIT 04 H
BIT 05 H
BIT 06 H
BIT 07 H
BIT 08 H
BIT 09 H
BIT 10 H
BIT 11 H
BIT 12 H
+3V E02V1 H
AD08 ANALOG INPUT
A222 C12
A405 A12 B12
AD03 GS 01 (0)H
AD03 GS 00 (0)H
AD03 GS 00 (1)H
AD03 GS 01 (1)H
A124 D12
4K .01%
2K .01%
1K .01%
AD07 A/D DONE H
M111 C07
AD10 PWR CLR L
AD07 EOC H
+3V B13U1 H
M117 E08
+3V E08U1 H
+3V E08V1 H
M113 E02
+3V E02U1 H
+3V E02V1 H
+3V E01U1 H
-PRODUCED BY THE AUTOMATED DRAFTING SYSTEM-
REVISIONS
CHK
CHANGE NO.
REV.
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE
ANALOG SUBSECTION
FIRST USED ON
PDP15
SIZE D
CODE BS
NUMBER AD15-0-07
REV. 00
SHEET 1 OF 1



NOTE:
1. A124 MODULES ARE OPTIONAL INSERT AS REQUIRED FOUR CHANNELS PER MODULE.

REVISIONS		
CHK	CHANGE NO.	REV.

-PRODUCED BY THE AUTOMATED DRAFTING SYSTEM-

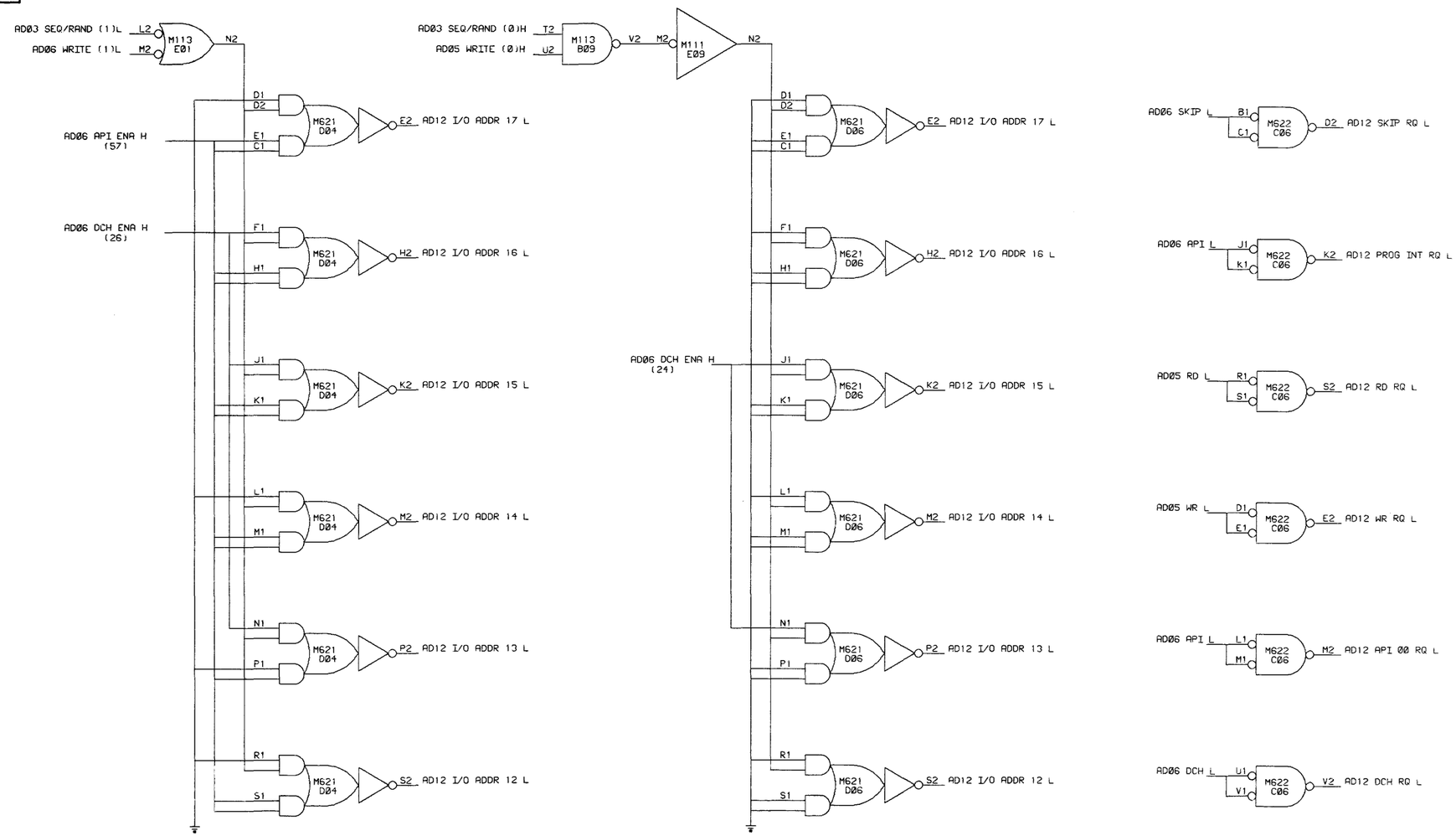
DRN BY	DATE 12/10/70
CHK'D	DATE 12/10/70
ENG.	DATE 12/10/70
PROJ. ENG.	DATE 12/10/70
PROD.	DATE 12/11/70
FIRST USED ON	PDP15
SCALE	
SHEET 1 OF 1	

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: MULTIPLEXER & DECODER

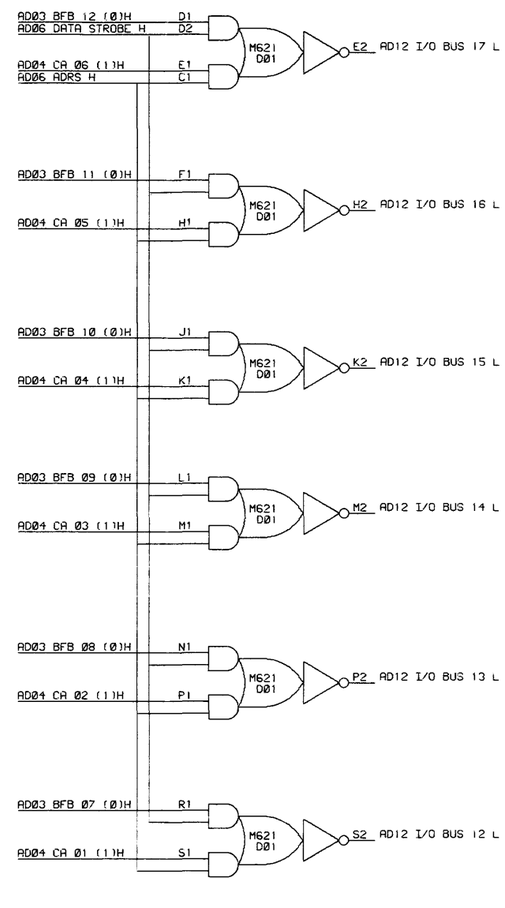
SIZE	CODE	NUMBER	REV.
D	BS	AD15-0-00	00

DIST.



REVISIONS		
CHK	CHANGE NO.	REV.

DES.	DATE 12/10/70	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHNG	DATE 12/10/70	
ENG.	DATE 12/11/70	TITLE: BUS DRIVERS
PROJ. ENG.	DATE 12/11/70	
PROD.	DATE 12/11/70	
FIRST USED ON: PDP15		SIZE D · CODE BS · NUMBER AD15-0-09 · REV. 00
SCALE		DIST.
SHEET 2 OF 2		



REVISIONS		
CHK	CHANGE NO.	REV.

-PRODUCED BY THE AUTOMATED DRAFTING SYSTEM-

DRN	DATE 12/6/78
CHK'D	DATE 12/7/78
ENG.	DATE 12/8/78
PROJ. ENG.	DATE 12/11/78
PROD.	DATE 12/11/78
FIRST USED ON: PDP15	
SCALE	
SHEET 1 OF 2	

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: BUS DRIVERS

SIZE	CODE	NUMBER	REV.
D	BS	AD15-0-09	00

DIST.

AD12 SD 00 H — H2 — M510 C01 — H1 AD10 BSD 00 L / F1 AD10 BSD 00 H

AD12 SD 01 H — K2 — M510 C01 — K1 AD10 BSD 01 L / J1 AD10 BSD 01 H

AD12 DCH GR H — M2 — M510 C01 — M1 AD10 B DCH GR L / L1 AD10 B DCH GR H

AD12 I/O BUS 00 L — P2 — M510 C01 — N1 AD10 BUS 00 L / P1 AD10 BUS 00 H

AD12 I/O BUS 01 L — R2 — M510 C01 — U2 AD10 BUS 01 L / T2 AD10 BUS 01 H

AD12 I/O BUS 06 L — S2 — M510 C01 — R1 AD10 BUS 06 L / S1 AD10 BUS 06 H

AD12 I/O BUS 07 L — U1 — M510 C01 — V1 AD10 BUS 07 L / V2 AD10 BUS 07 H

AD12 I/O BUS 08 L — D2 — M510 C02 — C1 AD10 BUS 08 L / D1 AD10 BUS 08 H

AD12 I/O BUS 09 L — H2 — M510 C02 — F1 AD10 BUS 09 L / H1 AD10 BUS 09 H

AD12 I/O BUS 10 L — K2 — M510 C02 — J1 AD10 BUS 10 L / K1 AD10 BUS 10 H

AD12 I/O BUS 11 L — M2 — M510 C02 — L1 AD10 BUS 11 L / M1 AD10 BUS 11 H

AD12 I/O BUS 12 L — P2 — M510 C02 — N1 AD10 BUS 12 L / P1 AD10 BUS 12 H

AD12 I/O BUS 13 L — R2 — M510 C02 — U2 AD10 BUS 13 L / T2 AD10 BUS 13 H

AD12 I/O BUS 14 L — S2 — M510 C02 — R1 AD10 BUS 14 L / S1 AD10 BUS 14 H

AD12 I/O BUS 15 L — U1 — M510 C02 — V1 AD10 BUS 15 L / V2 AD10 BUS 15 H

AD12 I/O BUS 16 L — D2 — M510 C03 — C1 AD10 BUS 16 L / D1 AD10 BUS 16 H

AD12 I/O BUS 17 L — H2 — M510 C03 — F1 AD10 BUS 17 L / H1 AD10 BUS 17 H

AD12 DATA OFLO H — K2 — M510 C03 — K1 AD10 B DATA OFLO L / J1 AD10 B DATA OFLO H

AD12 I/O OFLO H — M2 — M510 C03 — M1 AD10 OFLO L / L1 AD10 OFLO H

AD12 I/O SYNC H — P2 — M510 C03 — P1 AD10 SYNC L / N1 AD10 SYNC H

AD12 IOP 01 H — R2 — M510 C03 — T2 AD10 IOT 01 L / U2 AD10 IOT 01 H

AD12 IOP 02 H — S2 — M510 C03 — S1 AD10 IOT 02 L / R1 AD10 IOT 02 H

AD12 IOP 04 H — U1 — M510 C03 — V2 AD10 IOT 04 L / V1 AD10 IOT 04 H

AD12 I/O PWR CLR H — D2 — M510 C04 — D1 AD10 PWR CLR L / C1 AD10 PWR CLR H

AD12 API 00 GR H — H2 — M510 C04 — H1 AD10 B API 00 GR L / F1 AD10 B API 00 GR H

AD12 DS 00 H — K2 — M510 C04 — J1 AD10 BDS 00 L / K1 AD10 BDS 00 H

AD12 DS 01 H — M2 — M510 C04 — M1 AD10 BDS 01 L / L1 AD10 BDS 01 H

AD12 DS 02 H — P2 — M510 C04 — P1 AD10 BDS 02 L / N1 AD10 BDS 02 H

AD12 DS 03 H — R2 — M510 C04 — T2 AD10 BDS 03 L / U2 AD10 BDS 03 H

AD12 DS 04 H — S2 — M510 C04 — S1 AD10 BDS 04 L / R1 AD10 BDS 04 H

AD12 DS 05 H — U1 — M510 C04 — V2 AD10 BDS 05 L / V1 AD10 BDS 05 H

REVISIONS		
CHK	CHANGE NO.	REV.

-PRODUCED BY THE AUTOMATED DRAFTING SYSTEM-

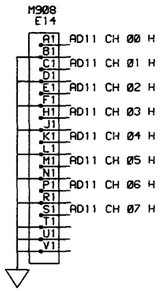
DSN	DATE 12/9/74
CHKD	DATE 12/9/74
ENG	DATE 12/6/74
PROJ. ENG.	DATE 12/9/74
PROD	DATE 12/6/74
FIRST USED ON	PDP15
SCALE	
SHEET	1 OF 1

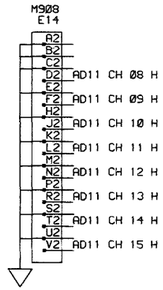
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

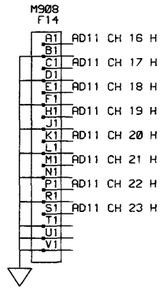
TITLE: BUS RECEIVERS

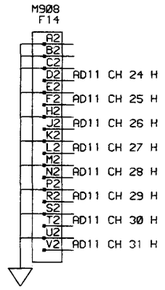
SIZE	CODE	NUMBER	REV.
D	BS	AD15-0-10	00

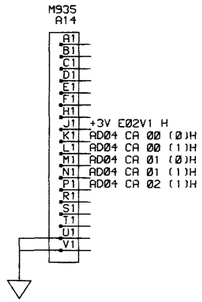
DIST.

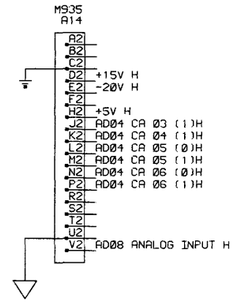


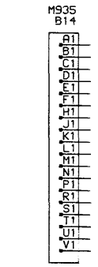


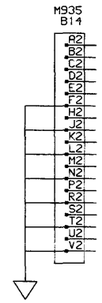


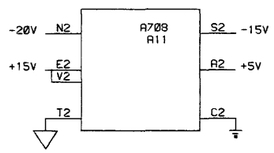








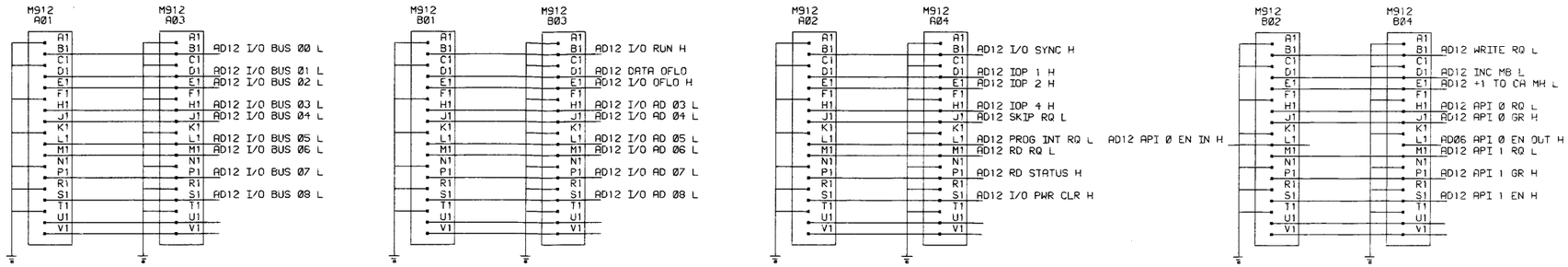


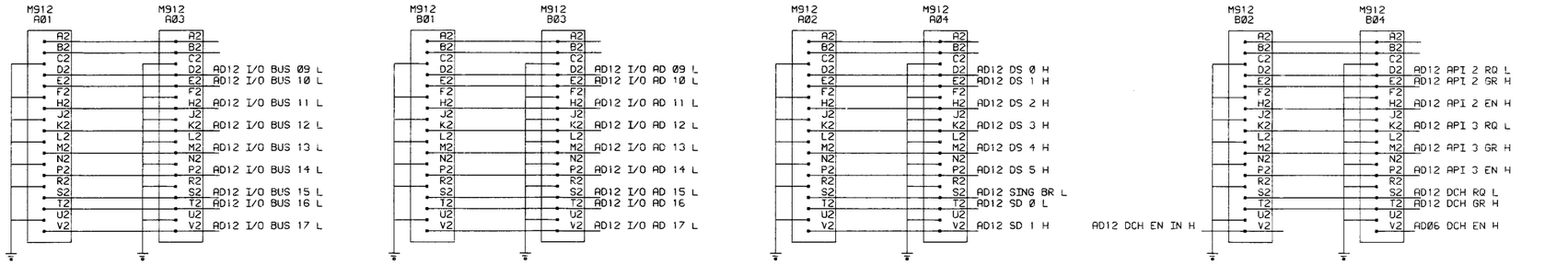


REVISIONS		
CHK	CHANGE NO.	REV.

-PRODUCED BY THE AUTOMATED DRAFTING SYSTEM-

DRN.	DATE 12/10/71	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D.	DATE 12/9/71	
ENG.	DATE 12/10/71	TITLE ANALOG INPUTS
PROJ. ENG.	DATE 12/10/71	
PROD.	DATE 12/16/71	
FIRST USED ON PDP15		SIZE D / CODE BS / NUMBER AD15-0-11 / REV. 00
SCALE		
SHEET 1 OF 1		DIST.





REVISIONS		
CHK	CHANGE NO.	REV.

-PRODUCED BY THE AUTOMATED DRAFTING SYSTEM-

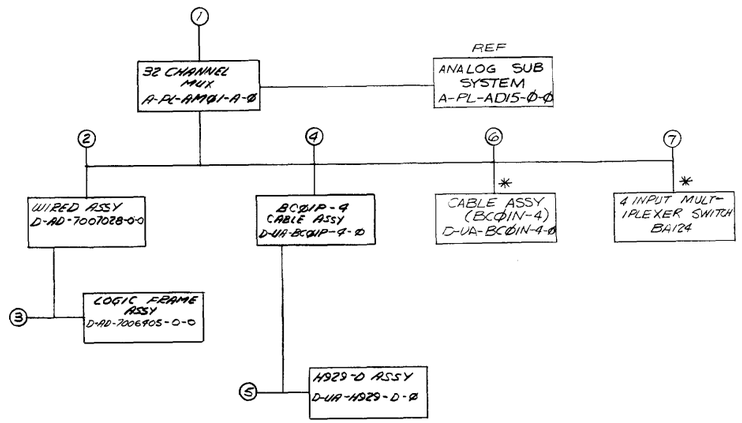
DRN.	DATE 12/19/72
CHK'D	DATE 12/19/72
ENG.	DATE 12/19/72
PROJ. ENG.	DATE 12/20/72
PROD.	DATE 12/21/72
FIRST USED ON: PDP15	
SCALE	
SHEET 1 OF 1	

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE
I/O BUS INTERFACE

SIZE	CODE	NUMBER	REV.
D	IC	AD15-Ø-12	Ø0

DIST.



* OPTIONS

FIND NO.	MECHANICAL DESCRIPTION	PART NO.	DEPT USAGE PROD	CUST	F/C
1.	32 CHANNEL MUX	A-PL-AM01-A-0			
2.	WIRED ASSY WIRED ASSY (P.L) LOGIC SERIAL DECAL	D-AD-7007028-0-0 A-PL-7007028-0-0 A-SS-7407896-0-0			
3.	LOGIC FRAME ASSY (SINGLE) LOGIC FRAME ASSY (P.L) CONN BLOCK MTG FRAME	D-AD-7006905-0-0 A-PL-7006905-0-0 D-IA-7407501-0-0			
4.	BC01P-9 CABLE ASSY BC01P-9 CABLE ASSY (P.L)	D-UA-BC01P-9-0 A-PL-BC01P-9-0			
5.	H929-D ASSY H929-D ASSY (P.L) PLATE AMP	D-UA-H929-D-0 A-PL-H929-D-0 C-IA-7408376-0-0			
6.	CABLE ASSY (BC01N-9)	D-UA-BC01N-9-0			
7.	9 INPUT MULTIPLEXER SWITCH	BA124			

FIND NO.	ELECTRICAL DESCRIPTION	PART NO.	DEPT USAGE PROD	CUST	F/C
1.	32 CHANNEL MUX MULTIPLEXER ADDRESS DECODER MULTIPLEXER ANALOG INPUTS MODULE UTILIZATION (AM01)	A-PL-AM01-A D-BS-AM01-A-03 D-BS-AM01-A-04 D-BS-AM01-A-05 K-W/P-AM01-A-02			
2.	WIRED ASSY WIRED ASSY (P.L) WIRE LIST	D-AD-7007028-0-0 A-PL-7007028-0-0 K-WL-AM01-A-06			

REV NUMBER AM01-A-01 SIZE CODE D DI

* OPTIONS

REVISIONS

REV.	CHANGE NO.	CHK

DEC FORM NO DRG 119

FIRST USED ON OPTION/MODEL
PDP 15

		DATE
DRN	Robert Frank	8-20-70
CHK'D	J. F. Comia	8-23-70
ENG.	[illegible]	10-7-70
PROJ. ENG.	[illegible]	10-7-70
PROD.	[illegible]	/ /

NEXT HIGHER ASSY
A-ML-AM01-A

SCALE —"

SHEET 1 OF 1

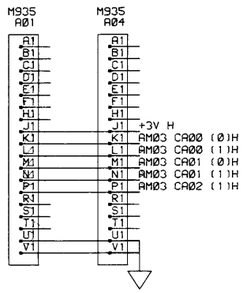
digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS

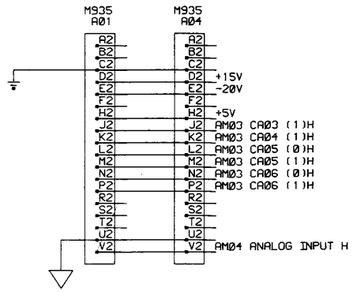
TITLE
DRAWING
INDEX LIST (AM01-A)

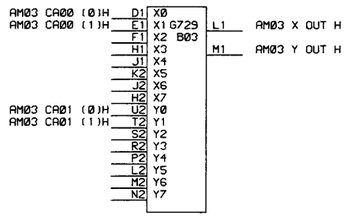
SIZE	CODE	NUMBER	REV.
D	DI	AM01-A-01	

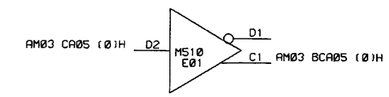
DIST.

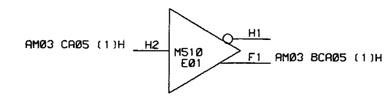
G729 JUMPER LIST	
CHANNELS	ADD JUMPERS
32-63	X0 X1
64-95	X1 Y0
96-127	X1 Y1

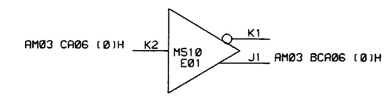


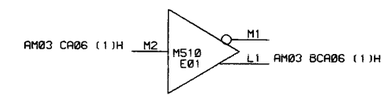


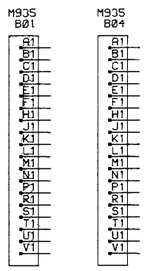


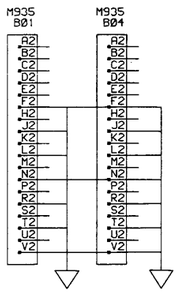








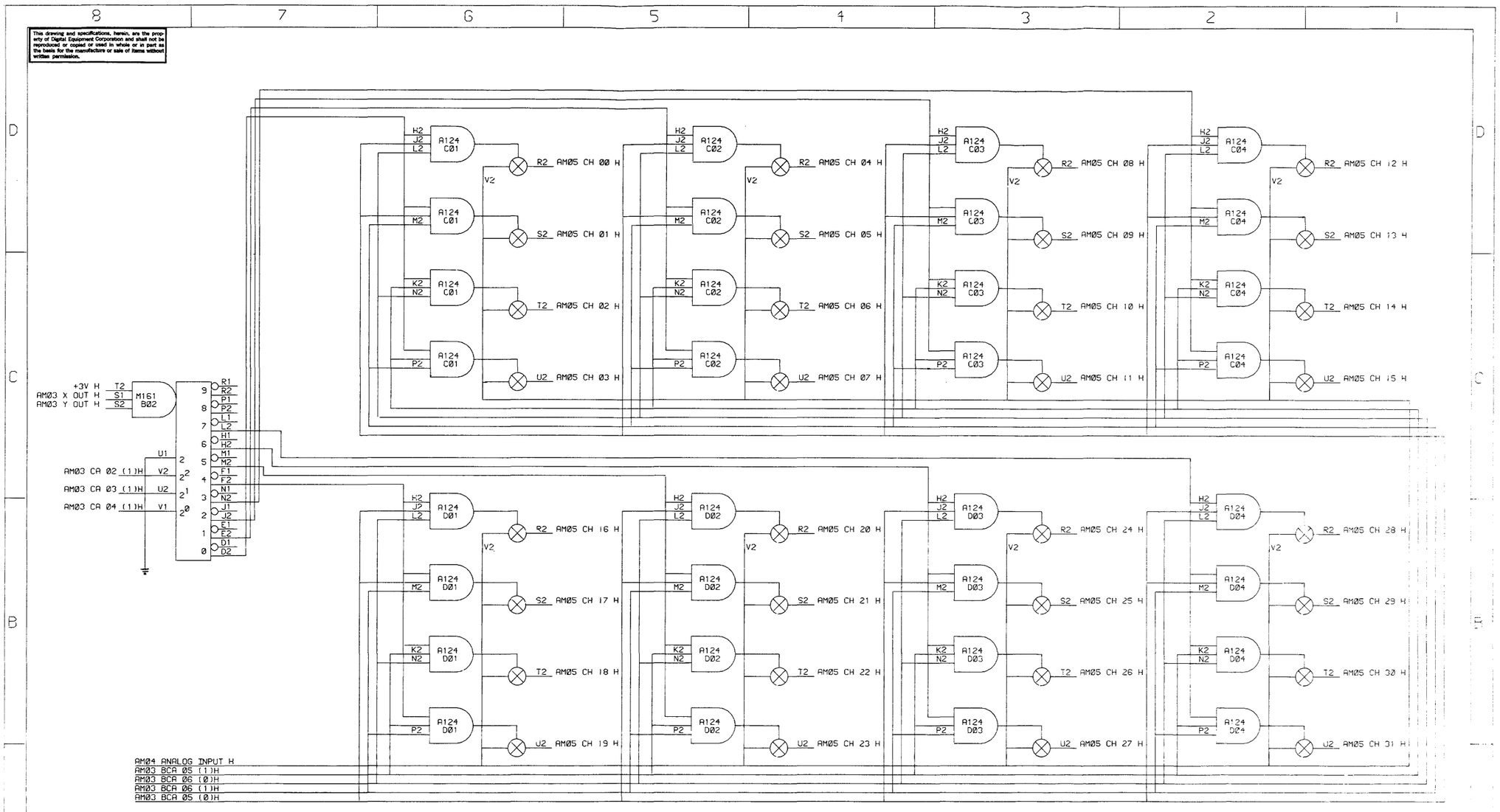




REVISIONS		
CHK	CHANGE NO.	REV.

-PRODUCED BY THE AUTOMATED DRAFTING SYSTEM-

DRN. Y. Leung	DATE 12/4/78	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D	DATE 12/10/78	
ENG. S. Moss	DATE 12/11/78	TITLE: MULTIPLEXER ADDRESS DECODER
PROJ. ENG. S. Moss	DATE 12/11/78	
PROD. Foley	DATE 9/14/79	
FIRST USED ON: PDP15		SIZE D · CODE BS · NUMBER AM01-A-03 · REV. 00
SCALE		DIST.
SHEET 1 OF 1		



REVISIONS		
CHK	CHANGE NO.	REV.

NOTE:
1. A124 MODULES ARE OPTIONAL INSERT AS REQUIRED FOUR CHANNELS PER MODULE.

-PRODUCED BY THE AUTOMATED DRAFTING SYSTEM-

DRN.	DATE
CHK'D.	DATE
ENG.	DATE 5/11/72
PROJ. ENG.	DATE 11/15/72
PROD.	DATE 12/15/72
FIRST USED ON: PDP15	
SCALE	
SHEET 1 OF 1	

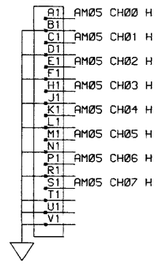
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: MULTIPLEXER

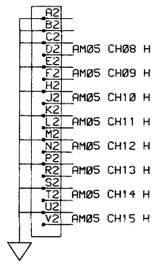
SIZE	CODE	NUMBER	REV.
D	BS	AM01-A-04	02

DIST.

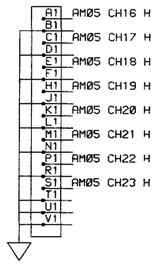
M908
E04



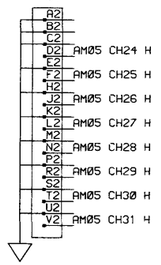
M908
E04



M908
F04



M908
F04



REVISIONS		
CHK	CHANGE NO.	REV.

-PRODUCED BY THE AUTOMATED DRAFTING SYSTEM-

DRN.	DATE 2 [illegible]
CHKD. [signature]	DATE 12/16/70
ENG. [signature]	DATE 12/10/71
PROJ. ENG. [signature]	DATE 11/2/72
PROD. [signature]	DATE 10/11/74
FIRST USED ON	PDP15
SCALE	
SHEET 1 OF 1	

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

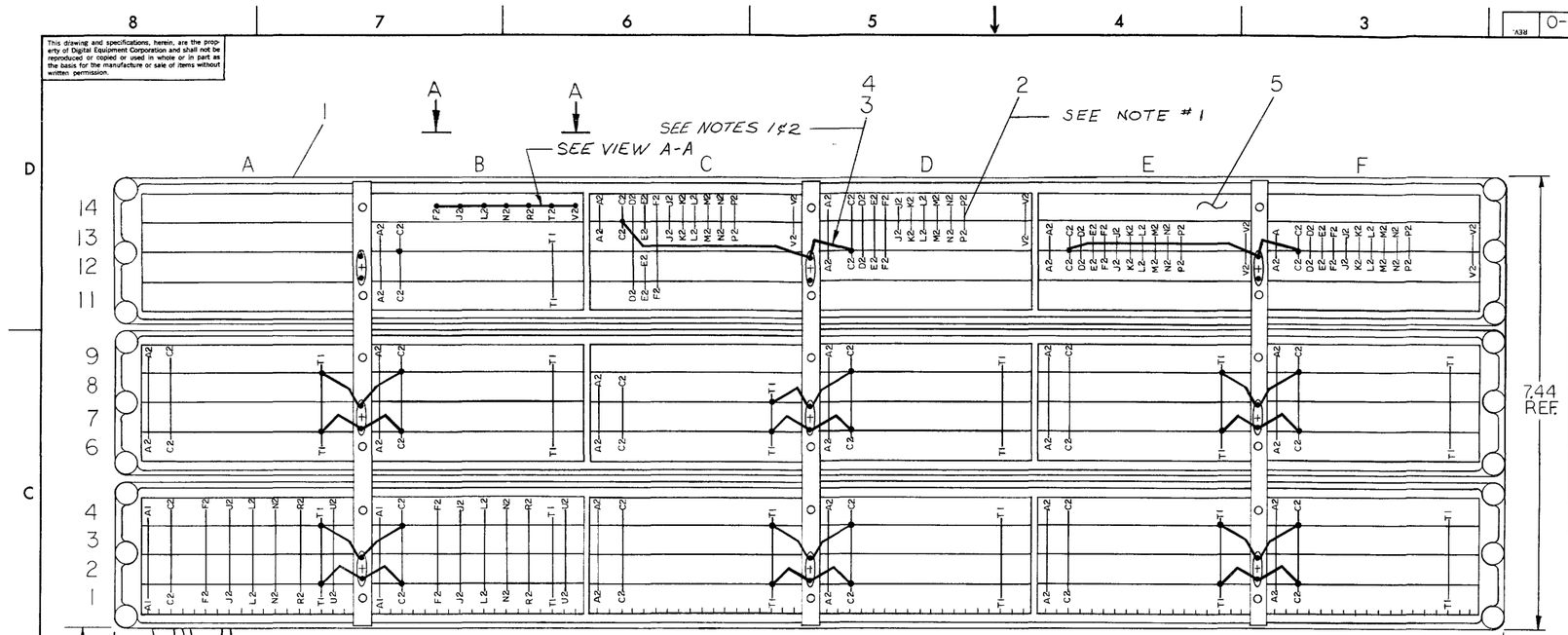
TITLE
ANALOG INPUTS

SIZE	CODE	NUMBER	REV.
D	BS	AM01-A-05	00

DIST.

REV. 0-0 | SIZE D | CODE | NUMBER 7007029

NOTES:
1. CONNECTIONS ON ITEMS 2 & 3 TO BE SOLDERED AND LOCATED AT MINIMUM PRACTICAL HEIGHT ABOVE BLOCKS.
2. CONNECTOR BLOCKS TO BE GROUNDED TO GROUND LUG AS SHOWN.
3. ALL VERTICAL HAND WIRING TO RUN OUTSIDE OF CONNECTOR BLOCKS.



VIEW A-A

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

FIRST USED ON OPTION/MODEL: AD15

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 | FRACTIONS ± 1/64 | ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN.		DATE 3-4-70
CHK'D		DATE 12/14/70
ENG.		DATE 12/15/70
PROJ. ENG.		DATE 12/17/70
PROD.		DATE 12/18/70

NEXT HIGHER ASSY: E-AD-7007125-0-0

SCALE: NONE

SHEET 1 OF 2

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: WIRED ASSY. (AD15)

SIZE D | CODE | NUMBER AD7007029-0-0 | REV.

DIST.

REVISIONS | REV. | CHANGE NO. | CHK

DEC FORM NO. DRD 100

WIRE TABLE

ITEM NO.	DESCRIPTION AWG	DESCRIPTION COLOR	FROM CONNECTION	FROM WITH	TO CONNECTION	TO WITH	SIGNAL
16	#18	GRN	P1-1	12	AØ9 A2	SOLDER	+5V
15		BLK	P1-3		AØ9 C2		GND
15		BLK	P1-4		A11 T2		GND
15		BLK	P1-5		A11 T2		GND
17		RED	P1-7		A11 V2		+15 V
14		BLU	P1-8		A11 N2		-20 V
9	#24	GRN	CØ4 A2	*	CØ6 A2	*	+5V
9			DØ4 A2		DØ6 A2		
9			EØ4 A2		EØ6 A2		
9			FØ4 A2		FØ6 A2		
9			CØ8 A2		C13 A2		
9			DØ9 A2		D12 A2		
9			EØ9 A2		E12 A2		
9			FØ9 A2		F12 A2		
9			AØ6 A2		BØ6 A2		
9			BØ6 A2		CØ6 A2		
9			CØ4 A2		DØ4 A2		
9			DØ6 A2		EØ6 A2		
9			EØ4 A2		FØ4 A2		
9			AØ9 A2		A14 H2		
11		BLU	A11 N2		A14 E2		-20V
11		BLU	A14 E2		C14 E2		-20V
11		BLU	C13 E2		D13 E2		-20V
11		BLU	D12 E2		E12 E2		-20V
11		BLU	E13 E2		F13 E2		-20V
6		BLK	A11 T2		B14 F2		ANALOG GND
6			B14 J2		A12 F2		
6			B14 N2		C14 F2		
6			B14 R2		D14 F2		
6			B14 T2		E13 F2		
6			C11 F2		D11 C2		
6			B14 V2		F12 F2		
6		BLK	A11 C2		AØBC2		GND
6		BLK	AØ9 C2		A14 C2		GND
9		GRN	A11 A2		B11 A2		+5 VA
9			CØ9 A2		D11 A2		
9			CØ9 A2		B11 A2		
6		BLK	A11 C2		B11 C2		GND A
6			CØ9 C2		D11 C2		
6			CØ9 C2		B12 C2		
7		RED	A11 V2		A11 E2		+15V
7			A12 D2		A14 D2		
7			A11 E2		A12 D2		
7			A14 D2		C14 D2		
7			C13 D2		D13 D2		
7			D12 D2		E12 D2		
7			E13 D2		F13 D2		
10		YEL	A11 S2		A12 E2		-15V
10		YEL	A12 E2		C12 E2		-15V

* TO BE HAND WIRE WRAPPED AFTER MACHINE WIRE WRAP.

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		

FIRST USED ON OPTION/MODEL: AD15

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 | FRACTIONS ± 1/64 | ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN. Tom Davis	DATE 10-8-70	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. R. Cook	DATE 10/14/70	
ENG. E. Mew	DATE 12/1/70	
PROJ. ENG. E. Mew	DATE 12/1/70	TITLE: WIRED ASSY. (AD15)
PROD. R. Cook	DATE 12/14/70	
NEXT HIGHER ASSY: E-AD-7007125-0-0		SIZE CODE: D; NUMBER: AD7007029-0-0; REV.
SCALE		
SHEET 2 OF 2		DIST.

REVISIONS: REV. | CHANGE NO. | CHK

DEC FORM NO. DRD 100

SIZE CODE: D AD7007029-0-0 REV.

Digital Equipment Corporation
Maynard, Massachusetts

printed in U.S.A.