DATA CONTROL
TYPE
136

DATA CONTROL
TYPE 136
INSTRUCTION MANUAL

CONTENTS

CONTENTS (continued)

CONTENTS (continued)

ILLUSTRATIONS

TABLES

ENGINEERING DRAWINGS

ENGINEERING DRAWINGS (continued)

SECTION 1

INTRODUCTION AND DESCRIPTION

INTRODUCTION

The purpose of this instruction manual is to aid personnel in the installation, operation, and maintenance of the DEC Data Control Type 136.

Anyone who wishes to learn the details of the system logic can save considerable time by first noting the conventions used on the engineering drawings. These conventions are explained in Appendix 2. It is recommended that this section of the manual be scanned before reading Section 2.

Abbreviations

The following abbreviations are used throughout this manual.

CCT	Character Counter
C(DA)	Contents of Data Accumulator
CHAR	Character
CLBD	Clobbered
CLR	Clear
CONI	Condition In
CONO	Condition Out
CP0, CP1	Command Pulse 0, 1
DA	Data Accumulator
DASH	Data Accumulator Shift
DATAI	Data In
DATAO	Data Out
DB	Data Buffer
DC	Data Control
DEC	Digital Equipment Corporation
DEV	Device

GV	Give
IC	Control Status Register (IC is mnemonic for Initial Conditions)
I/O	Input/Output
IOB	Input/Output Bus
IOS	Input/Output Selection
IOT	Input/Output Transfer
IR	Instruction Register
LT	Left
MCV	Marginal Check Voltage
PA	Pulse Amplifier
PI	Priority Interrupt
PIA	Priority Assignment
PDP	Programmed Data Processor
RQ	Request
RT	Right
SCT	Shift Counter
STRB	Strobe
TK	Take

Pertinent Documents

The following publications serve as source material and complement the information in this manual.

Programmed Data Processor-6 Handbook, F-65 – contains programming information for the Data Control Type 136.

System Modules Catalog, C-100 – describes the functional operation of the elements of the various logical modules comprising the data control. It is suggested that this handbook be referenced when reviewing the data control logic diagrams in Appendix 2 of this manual.

PDP-6 Installation Manual, F-68 – gives environmental, power, and cabling requirements as well as other information for installation of the 136 Data Control in a PDP-6 system.

PDP-6 Maintenance Manual, F-67 - covers topics not repeated in this manual which are essential to efficient maintenance of the data control when used with the PDP-6.

GENERAL DESCRIPTION

The Data Control Type 136 is a programmable buffer unit through which the PDP-6 Processor can control up to six input-output devices (Figure 1-1). Of the six I/O devices, two are uni-directional 6-bit devices, two are bidirectional 6-bit devices, and two are variable character-length devices. The variable character-length devices can handle data words composed of three 12-bit characters, two 18-bit characters, or one n-bit character where n can be any integer from 1 to 36.

Purpose of Data Control System

Besides saving processor time by matching the format and timing requirements of the various asynchronous I/O devices to the PDP-6 processor, the data control also frees the processor from the necessity of exercising detailed program control over the micro-operations required for the various in-out transfers. Because most of the required sub-operations are built into the data control logic, the programmer need not be concerned with the detailed byte manipulations required by the various I/O devices. The CONO DATA CONTROL instruction need only specify the device to be used, the number of bits per character, and whether an output or input operation is to be performed.

Programmed Operations

The details of data control programming are described in Section 4; the present paragraph briefly lists the primary variables of data control operations which are controlled by a CONO DATA CONTROL instruction in the processor program.

Device Selection

A 3-bit field of the CONO-instruction effective address specifies to which of the six possible I/O devices a given output or input sequence is to apply.

PDP-6 ARITHMETIC
PROCESSOR 166

IN-OUT BUS (36 BITS)

DATA CONTROL
TYPE 136

VARIABLE
CHARACTER-LENGTH DEVICES
(12,18, OR N* BITS)

BIDIRECTIONAL
6-BIT DEVICES

UNIDIRECTIONAL
6-BIT DEVICES

IO
DEVICE
NO.1

IO
DEVICE
NO. 3

IO
DEVICE
NO. 5

(6)

12,18, OR N

IO
DEVICE
NO. 2

IO
DEVICE
NO.4

IO
DEVICE
NO. 6

$*1 \leq N \leq 36$
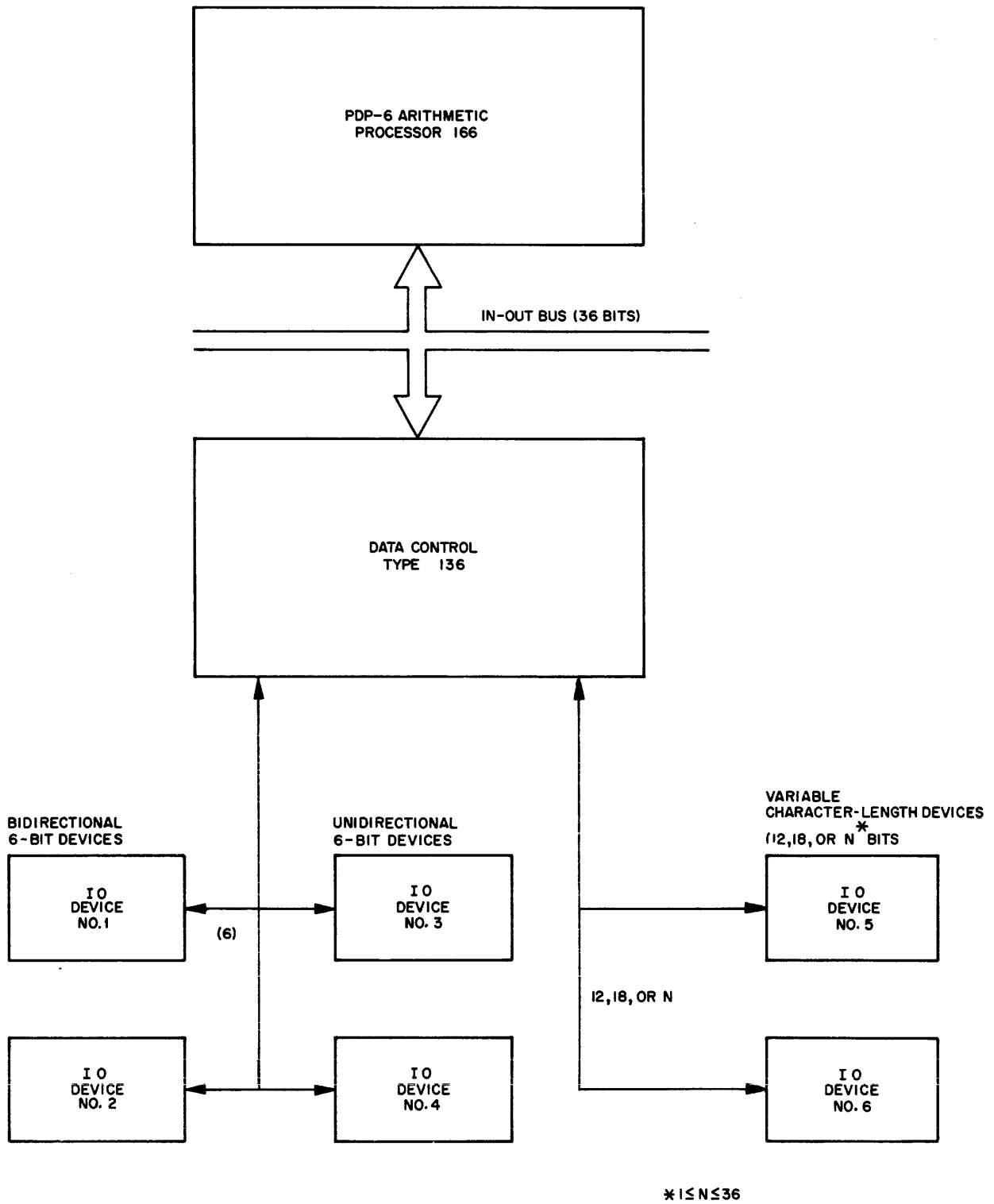
Figure 1-1   System Application

1-4

Input/Output

A single bit of the CONO-instruction effective address determines whether the data control is to treat the operations that follow as an output or input sequence.

Character Mode

A 2-bit field of the CONO-instruction effective address determines whether the data control is to transfer out (or read in) characters of 6, 12, 18, or n bits. Once the character mode has been specified, the built-in logic of the data control internally programs the requisite number of data shifts.

Priority Interrupt Assignment

A 3-bit field of the CONO-instruction effective address can assign a priority interrupt request channel to the data control. If such assignment is made, a PI channel can be chosen at any of seven ranked priority levels. This permits the data control to request a priority interrupt break with the Arithmetic Processor Type 166.

Logical Organization of Data Control

The data control contains a 16-bit control-status register called IC (Initial Conditions) and two 36-bit data registers, the data accumulator DA, and the data buffer DB (Figure 1-2). The internal logic of the data control governs the transfer of data through these registers and between them, the processor, and the I/O devices.

The data control internal logic is controlled by signals from two sources: the processor, and the IC register of the data control itself. Eight control inputs are sent to the data control from the processor (See Input Signals from Processor in Section 2). During CONI DATA CONTROL instructions, the processor can sample the contents of all 16 IC bits (see Figure 1-2).

Bidirectional Output and Input

The capability for both left and right data shifts is built into the data accumulator, DA. This enables the data control to operate with bidirectional input-output devices for example, DECtape (formerly Microtape) Control 551 and DECtape Transport 555. Because the direction of tape

PDP-6 ARITHMETIC
PROCESSOR 166

7 PRIORITY - INTER-
RUPT REQUEST LINES

7 IN-OUT
SELECTION LINES

IN-OUT BUS (36 BITS)

(36)

(13 OUT, 16 IN)

DATA CONTROL 136

DATA BUFFER DCDB
(36 BITS)

CONTROL
DCIC (16 BITS)

(8)   (7)   (7)

8 CONTROL LINES

(36)

ACCUMULATOR DCDA
(36 BITS)

INTERNAL LOGIC
OF DATA CONTROL

(6,12,18, OR N)

TRANSFERS TO OR FROM
IO DEVICES 1-6
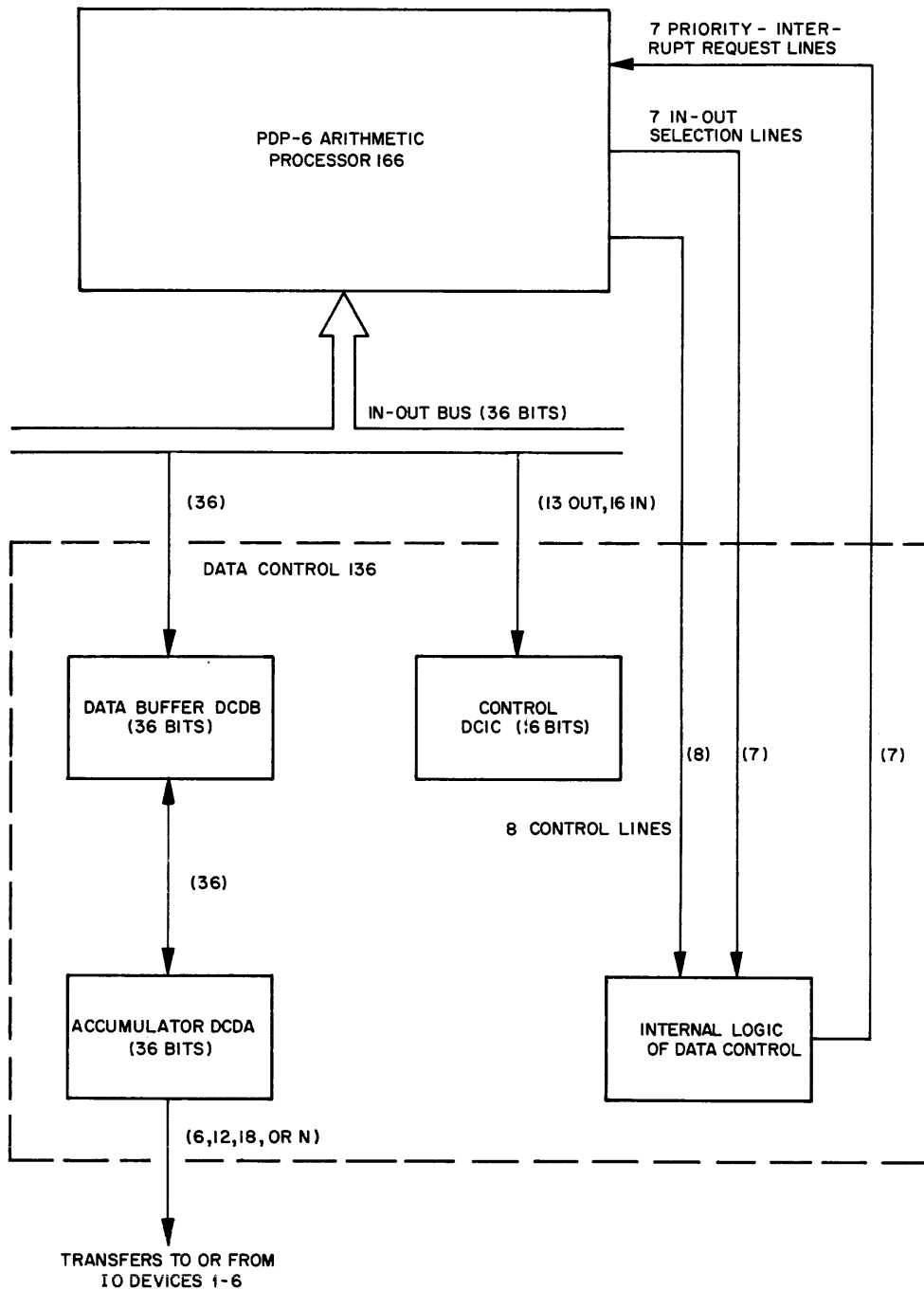
Figure 1-2   Logical Organization of Type 136 Data Control

1-6

motion determines the sequence of data bytes within a data word, the data control's bidirectional accumulator is a particularly useful feature. Depending on the current direction of tape motion, bytes can be shifted in or out from either end of the DA. The bidirectional accumulator permits correctly ordered data words to be read or written immediately while the DECtape moves in either direction. This frees the processor program from the necessity of reshuffling the bytes within a data word to remedy an inversion.

System Operating Specifications

APPLICATION	PDP-6 Input-Output Buffer
TIMING	Asynchronous
INPUT-OUTPUT DEVICES	
Number of Devices Controlled	1-6
Unidirectional 6-Bit Devices	0-2
Bidirectional 6-Bit Devices	0-2
Variable Character Length Devices	0-2
Character Modes Available (Variable Character Length Devices Only)	Three 12-bit characters per word
Character Modes Available (cont'd)	Two 18-bit characters per word One n-bit character per word $1 \le n \le 36$
BUFFER STORAGE	
Media	500 kc flip-flops
Quantity	Two 36-bit registers (one a bidirectional shift register)
STATUS-CONTROL REGISTER	16 bits, 13 programmable

MAXIMUM DATA RATE OF
DATA CONTROL LOGIC

	Character Mode	Minimum Interval Between Characters	Characters per Second
(Ordinarily not relevant.	6-bit	3 μsec	333K
System speed normally	12-bit	4 μsec	250K
limited by I/O device data	18-bit	5 μsec	200K
rate.)	36-bit (n-bit)	3 μsec	333K

PROGRAMMABLE FUNCTIONS	Selection of I/O device from up to six devices Selection of character mode from four available modes Selection of input or output mode Selection of priority interrupt request channel

ERROR BIT	One lost-data flag (described in Section 2)
PRIORITY INTERRUPT CHANNELS	7 ranked channels available. Any one, or none, may be used

Physical Characteristics

CONSTRUCTION	One standard all steel construction DEC cabinet, containing four logic racks
MODULES	Standard DEC system plug-in units, series 1000, 4000, and 6000
POWER EQUIPMENT	Power Supply unit 728; Power Control unit 811
LOGIC	Solid-state. Transistors and crystal diodes utilizing static logic levels (0 vdc and -3 vdc)
DIMENSIONS	
Height	69-1/2 inches
Width	22-1/4 inches
Depth	27-1/8 inches
CLEARANCE	
Front Doors	8-3/4 inches
Rear Door	14-7/8 inches
WEIGHT	73 pounds

Power Requirements

LINE VOLTAGE INPUT	105 to 125 volts, 60 cycle, single phase Power plug - Hubble Twist-Loc 3-prong, 30-ampere, 250-volt
CURRENT CONSUMPTION	5 amperes surge, 30 amperes normal
POWER CONSUMPTION	345 Watts
HEAT DISSIPATION	1175 BTU per hour

SECTION 2

THEORY OF OPERATION

Tables A1-1 through A1-6 are referenced throughout this and subsequent sections. These tables are contained in Appendix 1 on foldout pages.

Engineering drawings pertinent to the 136 Data Control are also referred to in this chapter. They are included in Appendix 2 and listed in the table of contents. The entire engineering drawing number is given with each reference so that either the reduced drawings in Appendix 2 of this manual or those that were supplied with the equipment may be consulted. Each block schematic number is followed by a comma and letters and/or numbers which refer to zones on the drawing. See Appendix 2 for an explanation on DEC logic symbols and codes.

PROCESSOR INTERFACE

These paragraphs describe the interchange of data and control information between the PDP-6 and the data control.

Cabling - Processor to Data Control

There are four 18-conductor cables from the PDP-6 processor to the I/O control units. Each cable is wired to two 22-terminal Methode plugs connected in parallel. The remaining four terminals, A, J, S, and Z, are used for grounding the shielding of the 18 conductors. Two of the four 18-conductor cables from the processor comprise the 36-bit I/O bus. These two cables are connected to Methode plugs 1A1-1B1 and 1A2-1B2 respectively. The 18 more significant data bits IOB0-17 enter the data control through Methode plugs 1A1-1B1. Methode plugs 1A2-1B2 receive the remaining 18 data bits IOB18-35 and also (via bus lines IOB20-35) the 16 IC control register bits IC20-35.

The remaining two 18-conductor cables between the processor and the data control are used for control information. One of these two cables is connected to Methode plugs 1A4-1B4. This cable carries the 14 IOS selection lines (described below under Device Selection Decoding) as well as the two ungated input signals, POWER ON and IOB RESET.

The second 18-conductor control cable enters through Methode plugs 1A3-1B3. This cable carries the six gated command signal inputs from the processor to the data control (IOB CONO SET, IOB CONO CLEAR, IOB DATAO SET, IOB DATAO CLEAR, IOB STATUS, and IOB DATAI; all described under Input Signals from Processor). The same cable also includes the seven priority interrupt request lines from the data control to the processor.

The specific terminal assignments of all four of the 18-conductor cables connected to Methode plugs 1A1-1A4 are listed in engineering drawing CD-D-166-0-IOMB in Appendix 2.

IC Register as Control Interface

The 16-bit control-status register, IC, is the principal interface for the exchange of control information between the processor and the data control. Most of the processor control information that governs the data control operation is transferred through the I/O bus and stored in the IC register. During the CONO instruction the processor determines the state of 13 of the 16 IC bits. The resulting state of IC determines the operations carried out by the data control logic during subsequent output or input instructions.

The IC register also serves to store control information moving in the opposite direction - from the data control to the processor. Since the processor samples the contents of all 16 IC bits with a CONI instruction, the state of DB RQ, status bit number 26, can readily be used to synchronize processor operations to appropriate phases of the data control output or input sequence. In a similar manner DA RQ, status bit number 25, synchronizes the operations of the I/O devices to the data control output or input sequence (see Table A1-1).

Device Selection Decoding

The device selection code portion of the IOT instructions determines which I/O device is to be utilized by a given instruction. The command levels produced by the IOT instruction must actuate only the selected I/O device, and must not be allowed to affect other non-selected devices. The gating function is performed by the device selection levels. These levels are applied to the data control and other I/O devices through the I/O selection lines.

The 14 I/O selection lines IOS3-9 represent both states of the seven bits of the device code contained in bits 3-9 of the processor instruction register, IR. (Assertion is at ground.) Seven

of the 14 IOS lines, one from each bit in IR3-9, are applied to an IOS decoder in the data control. The specific input connections made determine the selection code for a given data control unit. The decoder is shown in Appendix 2 in system block diagram SD-D-136-0-DCSD, D1, and in drawing BS-D-136-0-DC1, C-D1. The first data control incorporated in the PDP-6 installation is assigned the device selection code 200 octal.

Input Signals from Processor

Various input levels and pulses are applied to the data control by the processor. These include two ungated signals (not associated with any IOT instruction and applied to all I/O devices and control units), and six gated command signals applied only to the specific unit specified by the device selection code of the current IOT instruction.

Ungated Signals

There are two ungated input signals, the POWER ON level, and the IOB RESET pulse (see column 1, BS-D-136-0-DC1.

POWER ON – The POWER ON line drops to -15 vdc whenever computer power is turned on. This line is connected to the remote terminal of the LOCAL/REMOTE switch on the power control for each device. Normally, the LOCAL/REMOTE switches are left in the REMOTE position, so that the -15 vdc POWER ON level causes all peripheral equipment to be turned on when computer power is turned on.

IOB RESET – This line supplies negative pulses to clear the control registers and data buffers of all equipment attached to the I/O bus. The IOB RESET pulse is generated when computer power goes on or when the operator presses the I/O RESET key on the computer console.

Gated Command Signals

The six command lines are applied to the data control through Methode plugs 1A3-1B3 (drawing BS-D-136-0-DC1, column 1). These lines are connected to all control units, but are gated by the selection level from the IOS decoder so that they can affect only the control unit for the addressed device. The six command lines carry four output command pulses and two input command levels.

<u>Output Command Pulses</u> - There are two pairs of negative command pulses which implement the basic output instructions. Each of these two pairs includes a clear pulse followed by a set pulse.

The CONO instruction (see Section 4) produces an IOB CONO CLEAR pulse followed 1 µsec later by an IOB CONO SET pulse. The principal function of the CONO CLEAR is to clear the data control IC register and shift counter. The CONO SET then loads the 13 low order IC register bits from the I/O bus. The processor places information on the bus for 2.5 µsec. The clear occurs at the 1 µsec point; the set occurs at the 2 µsec point.

Similarly, the DATAO instruction (see Section 4) produces an IOB DATAO CLEAR pulse followed 1 µsec later by an IOB DATAO SET pulse. These pulses clear the data control data buffer, and then load it from the I/O bus. The processor again places information on the bus for 2.5 µsec, and again the clear is at the 1 µsec point and the set at the 2 µsec point.

<u>Input Command Levels</u> - There are two negative command levels which implement the basic input instructions. These command levels gate the input information that is held by the data control onto the I/O bus for 2.5 µsec. The processor reads the information from the bus onto its I/O register at the 2 µsec point. The IOB STATUS level gates the contents of the entire IC register onto the I/O bus during the execution of each CONI instruction. Similarly, IOB DATAI gates the contents of the data buffer onto the bus during DATAI instructions.

Priority Interrupt Request Lines

There are seven priority interrupt request lines running from data control to processor. The data control requests a priority interrupt by placing a ground on one of these seven PI request lines. To assign a priority to the data control, a CONO instruction loads a 3-bit number into the PIA (priority assignment) field of the IC register, IC33-35. (Refer to Priority Interrupt Assignment Bits IC33-35).

DATA BUFFER AND DATA ACCUMULATOR

The data control contains two 36-bit data registers, the data buffer register DB, and the data accumulator DA. Both the data buffer and the data accumulator are shown in engineering

drawing BS-D-136-0-DAB1. Each of the 12 4230 flip-flop modules shown in simplified block form is composed of logical elements identical to those illustrated in the detailed block schematic at column 8 of the figure. Each of the 12 4230 modules contains 3 bits of the data buffer DB, and 3 bits of the data accumulator DA. The 12 modules are arranged in 6 pairs of 2 modules each; each pair contains 6 bits of DB and 6 bits of DA. The 6 DA bits are connected to form a bidirectional 6-bit shift register.

Note that the bits contained in each module pair do not represent adjacent bit positions. Rather, each bit in a given module pair represents a bit position six bits less significant than the next bit to the left. Therefore, when the accumulator is operated as a conventional bidirectional shift register, each shift of one bit position to the left or to the right on the six module pairs causes the entire contents of the accumulator to be shifted six bits to the left or the right.

Data Buffer (DCDB)

The data buffer DB is a 36-bit storage register with no shift requirement. The various operations it performs in response to applied input signals are described below.

I/O Bus Transfers

Processor output data can be parallel transferred from the 36-bit I/O bus into DB. This transfer is produced by the application of a negative-going pulse, DC DB $\longleftarrow$ IOB, to the terminal Y ("LOAD BUFFER") inputs of the 12 4230 modules. For input, the 36-bit data word in the buffer can be read into the processor via the I/O bus. The data is placed on the bus by applying a negative level, DC DB $\longrightarrow$ IOB, to the terminal K ("BUFFER BUS") emitter-follower inputs.

Buffer-Accumulator Transfers

When the DC DB $\longrightarrow$ DA pulse is applied to the W terminals, it jam transfers the contents of DB into the data accumulator. Note that the apparently converse pulse DC DA $\longrightarrow$ DB (applied to the X and T terminals) not only jam transfers the contents of the accumulator into the buffer, but also clears the accumulator.

Buffer Clear

The buffer is cleared by DC CLR DB at terminal E.

Data Accumulator (DCDA)

The data accumulator DA is a 36-bit bidirectional shift register capable of successive 6-bit shifts in either direction. The various operations it performs in response to applied input signals are described below.

Accumulator Output

The accumulator contents are always available at output terminals J, N, and R of each module. Ground levels at these terminals correspond to ones in the corresponding bits of the accumulator. These accumulator output levels are applied to the output inverter buffers shown in engineering drawing BS-D-136-0-DAB2, A-B. During output operations, the I/O devices sample the inverter outputs at appropriate phases of the device operating cycles (negative levels at the inverter outputs correspond to accumulator bits containing ones).

Devices 3 and 4 receive only the six high order bits DA0-5. The bidirectional devices, I/O devices 1 and 2, receive the six high order bits during normal tape motion, but during reverse tape motion these devices receive instead the six low order bits DA30-35. The variable character-length devices, I/O devices 5 and 6, receive data in bytes of 12, 18, or n bits $(1 \leq n \leq 36)$ (refer to Data Control Outputs to I/O Devices).

Accumulator-Buffer Transfers

The application of DC DA $\dashrightarrow$ DB to the X and T terminals of the 12 4230 modules causes the jam transfer of C(DA)* into DB and clears DA.

Accumulator Dash Data Inputs

Data can be read in from I/O devices 1-4 to the six low order (right-end) bits of the accumulator, DA30-35. In addition to this right-end readin, the bidirectional I/O devices, devices 1 and 2, can also read data into the six high order (left-end) bits of the accumulator, DA0-5.

*C(DA) means contents of data accumulator.

Data transfer from I/O devices 1-4 into the low order bits is carried out as follows. Data is presented to the six terminal S inputs shown in engineering drawing BS-D-136-0-DAB1, B. The data inputs are designated DASH DATA IN 30 RT through DASH DATA IN 35 RT. A ground DASH DATA IN level corresponds to a 1 input from the corresponding bit position of the selected I/O device. The detailed block schematic in column 8 of BS-D-136-0-DAB1 shows how the data is read into the accumulator applying a DASH LT pulse to the U terminals of all 12 4230 modules. This pulse strobes the input data from the I/O device into the six low order bits of the accumulator, and simultaneously shifts the previous contents of the entire accumulator six bit-positions left. (See page 2-5, second paragraph).

During reverse tape motion, the bidirectional devices, I/O devices 1 and 2, read data into the six high order bits of the accumulator, DA0-5. This operation is exactly similar to the low-order-bits transfer described above. The terminal H data inputs (BS-D-136-0-DAB1, C) are designated DASH DATA IN 0 LT through DASH DATA IN 5 LT. The data is strobed in by presenting a DASH RT pulse to the Z terminals of all 12 4230 modules. This pulse reads the input data from the I/O device into the six high order bits and shifts the accumulator right six bit-positions.

Accumulator Dash Strobe Inputs

The two variable-character-length devices, I/O devices 5 and 6, can read data into the accumulator in bytes of 12, 18, or n bits $(1 \leq n \leq 36)$. These devices always send each input byte of less than 36 bits into the low order end of the accumulator.

The data transferred in from devices 5 and 6 does not enter the accumulator in the same way as the data from I/O devices 1 through 4. If the IC30-32 bits select I/O device 5 for a read-in sequence, that device sends the data control a TK CHAR 5 pulse (take a character from device 5) when it is ready to send data into the data control. This pulse (BS-D-136-0-DASH,C1) generates DASH STRB LT and DASH STRB RT pulses. Similarly, if IC30-32 select I/O device 6 for a readin sequence, the TK CHAR 6 pulse generates DASH STRB LT and DASH STRB RT pulses.

Input data levels from device 5 are applied to the negative capacitor-diode gates shown in drawing BS-D-136-0-DAB2, 7C; negative levels correspond to 1 bits. The number of input

terminals used, 12, 18 or n, depends on the size of the input bytes that device 5 sends to the data control. For bytes of less than 36 bits the active input terminals are always those at the low order end of the accumulator.

The input data levels are strobed into the accumulator by device 5 DASH STRB pulses. If a negative input level is applied to a given capacitor-diode gate, the pulse inverter output of that gate generates a positive pulse at DASH STRB time, thereby setting the flip-flop to the 1 state. Input levels from device 6 are strobed into the accumulator by the same process.

Accumulator Shifts

The entire contents of the accumulator are shifted left six bit-positions by applying a DASH LT pulse to the U terminals of all 12 4230 modules. Application of a DASH RT pulse to the Z terminals produces a 6-bit right shift.

For I/O devices 1-4 the contents of the accumulator are always shifted left six bit-positions whenever a character is read into the six low order bits of the accumulator. This is necessary to prevent the destruction of the data previously read in. When reading in data from the bi-directional devices in reverse tape motion, C(DA) (the contents of DA) are shifted right six bit-positions as each new character is read in.

Devices 5 and 6, the variable character-length devices, are read in at the DASH STRB pulse but do not start to shift C(DA) until 1 μsec after DASH STRB. The accumulator is then shifted left six bit-positions every microsecond until there is room for the next byte of input data to be read in. For 12-bit bytes, two shifts are required; 18-bit bytes take three shifts; n-bit bytes are not shifted at all. For operations involving devices 5 or 6, no shifts ever follow the final character of the data word.

For output operations of all six I/O devices, the direction and number of accumulator shifts is the same as for input. Data is normally transferred out to the I/O devices from the high order (left-end) accumulator bits, and C(DA) are shifted left for each character that is trans-ferred out. In reverse tape motion, the bidirectional devices 1 and 2 transfer out data from the low order (right-end) accumulator bits, and shift right as each new character is transferred out.

CONTROL STATUS REGISTER (DCIC)

The internal logical operations of the data control are controlled largely by the 16-bit control-status register IC (mnemonic for Initial Conditions) and the 2-bit shift counter SCT. The IC register is composed of 16 identical 500-kc flip-flops. However, the conditions controlling these flip-flops and the uses to which they are applied are so diverse that each of the nine data fields (which together comprise the 16 IC bits) may be regarded as an essentially separate register. Thirteen of the 16 IC bits, IC23-35, are shown on engineering drawing BS-D-136-0-DC2, A-B. The remaining three IC bits, IC20-22, make up the 3-bit character counter shown in drawing BS-D-136-0-DC1, B6-7. The nine data fields making up the IC register are listed in Table A1-1, a foldout sheet in Appendix 1.

The 2-bit shift counter SCT0-1 is a separate auxiliary register, entirely internal to the data control. Because it can neither be controlled nor sampled by the processor, it is not considered to be part of the IC register. However, because the logical conditions governing the shift counter operations are closely interrelated with the conditions governing the operation of the character counter, the two counters are described together below. The shift counter is shown in BS-D-136-0-DC1, B5.

Character Counter IC20-22 and Shift Counter

The character counter (CCT 0-2) and the shift counter (SCT 0-1) are shown in drawing BS-D-136-0-DC1, B. Decoder nets which determine when the counters have reached the assigned count (DC CCT DONE and DC SCT DONE) are shown immediately above the counters. The control nets which govern the counting and clearing of the counters are also shown in the same drawing at zone C7-8.

Function

The character counter keeps track of the number of characters of a given data word which have been read in or transferred out. It completes its count at a number one less than the number of characters in the data word. The resulting DC CCT DONE (Character Counter Done) level serves two functions. First, during operations by I/O devices 5 or 6, it prevents the final

character from being shifted left. Second, and even more important, it is the character counter done level which enables the final command pulse of the readin or transfer out sequence to terminate the sequence by setting the DA RQ flip-flop.

The shift counter is only used by the variable character-length devices. When devices 5 or 6 are operating in the 12 or 18-bit mode, the shift counter keeps track of the number of 6-bit left shifts which have been made after the readin or transfer out of a given character. The DC SCT CONT level (which is asserted until the shift counter completes its assigned count) controls the generation of the repetitive DASH LT pulses that shift all non-final 12 or 18-bit characters left to make room for the next character.

CP1 Pulses

The CP1 pulse strobes all stepping and clearing of both counters. The generation of this pulse is described later in this section. A CP1 pulse is generated whenever any I/O device sends a command pulse to the data control. A CP1 pulse is also generated by the DASH LT pulse whenever the accumulator contents are shifted left.

Counter Done Levels

The character mode in which the data control operates (see Character Mode Bits IC28-29) determines the correct final count for both the shift counter and the character counter. The final count of the shift counter corresponds to the number of shifts required per character (after the command pulse that reads the character in or transfers it out). The final count of the character counter is always one less than the number of characters in the data word. The shift counter done level DC SCT DONE is generated by the decoders in BS-D-136-0-DC1, A-B5; the decoders in zone A-B7 of this drawing generate the character counter done level DC CCT DONE. Operation of these two sets of decoders is summarized in Table A1-2.

Shift Counter Continue

The shift counter is stepped and a DASH LT pulse is generated at each CP1 pulse which occurs while the DC SCT CONT (Shift Counter Continue) level is asserted negative. The level rises to ground if either the shift counter or character counter finishes its assigned count, that is, at the assertion of either SCT DONE or CCT DONE (see BS-D-136-0-DC1, C8).

2-10

Character Counter Continue

The character counter is stepped at each CP1 pulse which occurs while the DC CCT CONT (Character Counter Continue) level is asserted negative. The level is asserted only when the shift counter is done (BS-D-136-0-DC1, C8). This insures that the character counter is stepped only by those CP1 pulses corresponding to actual command pulses from the I/O devices, and not by the CP1 pulses resulting from repetitive DASH LT pulses in 12 or 18-bit operation. The latter class of CP1 pulses are counted by the shift register only; they represent merely shifts within a given character and not new characters. When the DC CCT DONE level is asserted, the DC CCT CONT level ends.

Clear Counter Levels

The circuits which clear the shift counter and character counter are also shown in BS-D-136-0-DC1, C7. Both shift counter and character counter are cleared by the initial data control clear pulse, DC IC CLR. The character counter is also cleared by the first CP1 pulse which occurs after the character counter completes its count. There is one further possibility of clearing the character counter. Under certain circumstances it may be desirable to clear the character counter by an externally generated clear pulse from one of the I/O devices. The negative capacitor-diode gate permits the option of connecting any of I/O devices 1-4 for an external character counter clear.

The shift counter is always cleared at the first CP1 pulse occurring after either the shift counter or the character counter is done.

Error Bit IC23

The DATA CLBD (Data Clobbered) error bit is set to 1 by any CP0 pulse generated when DA RQ contains 1. This error condition indicates either that an output command pulse has been sent to the data control while DA is empty, or else that an input command pulse has been sent to the data control while DA is still loaded with the previous data word.

The latter condition is the more serious one; its detection is the primary purpose of the data CLBD error bit. If an I/O device should attempt to read in data before the previous data word

were advanced from the accumulator to the data buffer, data would be lost. This error condition could arise only through an equipment malfunction or a programming error at the I/O device.

<center>Data Control Status Bits IC24-26</center>

The three status bit flip-flops DBDA MOVE, DA RQ, and DB RQ synchronize the processor and I/O device operations to the data control as well as governing the internal operations of the data control itself.

DBDA MOVE IC24

The DBDA MOVE (data buffer data accumulator move) flip-flop is shown in BS-D-136-0-DC2, A2. Its output is applied to input terminal M of diode gate 1B7 (BS-D-136-0-DC1, C3); a negative-to-ground transition at the output of that gate initiates all transfers (in either direction) between the data buffer and the data accumulator. A transfer can be initiated in either of two ways. When the DA RQ flip-flop is in the 1 state, the 0 to 1 transition of DBDA MOVE causes a rising edge at the output of gate 1B7, thus triggering pulse amplifier 1A9 and producing a DA —J> DB or DB —J> DA transfer. Similarly, when the DBDA MOVE flip-flop is in the 1 state, the 0 to 1 transition of the DA RQ flip-flop causes the transfer.

DA RQ Flip-flop IC25

The data accumulator request flip-flop DA RQ (BS-D-136-0-DC1, A2) indicates the status of the accumulator both to the I/O devices and to the internal logic of the data control. At most phases of the data control operating cycle, the state of DA RQ indicates whether or not the data accumulator is fully loaded with data. During output operations, a 0 in the DA RQ indicates that the accumulator is loaded. During input operations, however, a 1 in DA RQ indicates that the accumulator is loaded, and a 0 indicates that the accumulator is empty and free to receive data.

For either output or input operations, a 0 in DA RQ indicates that the data control is ready to act on commands from the I/O devices (to transfer out the data word in DA during

<center>2-12</center>

output, or to read in a new data word to the empty DA during input). Conversely, during both output and input operations, a 1 in DA RQ indicates that the accumulator is not ready to execute a transfer.out or readin sequence (refer to Table A1-3).

DB RQ Flip-flop IC26

The data buffer request flip-flop DB RQ (BS-D-136-0-DC1, A3) indicates the status of the data buffer both to the I/O devices and to the internal logic of the data control. At most phases of the data control operating cycle, the state of DB RQ indicates whether or not the data buffer DB is loaded with data. The immediate meaning of the state of DB RQ is the same as that of DA RQ described above. Either flip-flop in the 0 state during output, or in the 1 state during input, signifies that the corresponding register is loaded with data. When DB RQ contains a 1 during output (indicating that the buffer is empty), the data control is ready to accept output data from the processor. Moreover, when DB RQ contains a 1 during input (indicating that the buffer is loaded) the data control is ready to read data into the processor.

Status-Bit Configuration Tables (Tables A1-4 and A1-5)

The configurations of the three status-bit flip-flops after each phase of the data control output operations are summarized in Table A1-4. Input configurations are similarly summarized in Table A1-5. These two tables are frequently referred to in the paragraphs below describing the data control output and input cycles. Once the data control logic has been learned, these two tables and the system flow diagram, FD-D-136-0-FD1, can serve as a ready-reference summary of the data control operating cycle.

Input/Output Flip-flop IC27

The input/output flip-flop, DC IN/OUT, is shown in engineering drawing BS-D-136-0-DC2, A5. It indicates to the data control logic whether the current operation is an input operation or an output operation. The outputs of the in/out flip-flop are applied to input terminals Z and T of pulse amplifiers 1A10 (BS-D-136-0-DC1, C5). The state of the flip-flop determines whether the dual purpose transfer pulse DC DB $\longleftrightarrow$ DA produces a DC DA $\longrightarrow$ DB pulse which jam transfers C(DA) into DB during input cycles, or a DC DB $\longrightarrow$ DA pulse, which jam transfers C(DB) into DA during output cycles.

Character Mode Bits IC28-29

The two character-mode flip-flops CH MODE 0 and CH MODE 1 are shown in BS-D-136-0-DC2, B4. The states of these flip-flops determine the character mode in which the data control operates (refer to Table A1-2). The outputs from the character mode flip-flops are applied to the decoder nets shown in BS-D-136-0-DC1. Thus they determine the final contents of the shift counter that produce the DC SCT DONE level, and the final contents of the character counter that produce the DC CCT DONE level.

Internal Device Address IC30-32

The three internal device address flip-flops, DC DEVICE 0, DC DEVICE 1, and DC DEVICE 2, are shown in BS-D-136-0-DC2, 5-6. The 3-bit binary number contained in these three flip-flops indicates to the data control logic which of the six subsidiary devices is to be used for a given input or output operation.

The contents of the three internal device address flip-flops correspond directly to the I/O device numbers. When the flip-flops contain 010 (2 octal) I/O device 2 is selected; 100 (4 octal) selects I/O device 4, and so on. This 3-bit internal device address addresses an I/O device only from the selected data control. It should not be confused with the 7-bit device selection code used by the processor to address the selected I/O device directly, nor with the second 7-bit device selection code used by the processor to address the selected data control; levels 1-4 are first sent through the buffer-inverter circuits shown in BS-D-136-0-DC2, A5-6.

Priority Interrupt Assignment Bits IC33-35

The three priority interrupt assignment flip-flops, PIA-0, PIA-1, and PIA-2, are shown in BS-D-136-0-DC2, B7-8. The processor can assign a priority-interrupt request channel to the data control by means of a CONO instruction which sets these three bits to some number from 1 to 7. If all three PIA bits are left 0, no priority interrupt channel is assigned (see Section 4).

Until the contents of PIA0-2 are changed by another CONO from the processor, the data control can request a break on the assigned channel. The data control requests a break on the assigned channel when the DB RQ flip-flop is set to the 1 state. If this occurs during

an output sequence, it indicates that the DB register is empty and is therefore ready to receive more data from the processor. If it occurs during an input sequence, it indicates that the DB register is loaded with data and is therefore ready to read data into the processor. Both output levels from each of the three PIA flip-flops are applied to the binary-to-octal decoder 1B8 (BS-D-136-0-DC2, B7-8). When inactive, the seven PIA outputs from this decoder are negative levels. When the DB RQ flip-flop is set to 1, the PIA line corresponding to the assigned channel is grounded.

DEVICE INTERFACE

This section describes the interchange of data and control information between the data control and its subsidiary I/O devices.

Cabling - Data Control to I/O Devices

There are 16 22-conductor coaxial cables from the data control to the six I/O devices. Devices 1 and 2, the bidirectional devices, require two cables each. Unidirectional devices 3 and 4 have only one cable apiece. Devices 5 and 6, the variable character-length devices, are each assigned five cables. The 16 cables are wired to 22-pin Methode plugs in rack positions 1D10 through 1D25. The specific terminal assignments of all 16 cables are shown in engineering drawing ID-D-136-0-EDC.

Data Control Outputs to I/O Devices

The data control sends the I/O devices both control information and data levels.

Control Information

Output control information is sent to I/O Devices 1 through 6 through the six Methode plugs shown in BS-D-136-0-DASH, D. All six devices receive the state of the DA RQ flip-flop; furthermore each device receives its own device select signal. The negative 1 output of the DA RQ flip-flop is amplified by the 6684 Bus Driver 1B21 (BS-D-136-0-DC2, A3). The amplified output is then sent to the six I/O devices through the W terminals of the six Methode plugs (BS-D-136-0-DASH, D). When DA RQ contains a 1, the output is quiescent in the assertion state shown (W terminals negative). This indicates to the selected I/O device that

the data control is not ready. When the DA RQ output is active, the W terminals are at ground. This indicates to the I/O devices that the DA RQ flip-flop contains 0 and that the data control is ready.

The data control sends DC DEVICE SEL levels to the six I/O devices so that a given device responds to data control operations only when the internal device address in IC30-32 selects that device; refer to Internal Device Address IC30-32. The negatively asserted DC DEVICE SELECT level for each device is applied to the X terminal of the corresponding Methode plug (BS-D-136-0-DASH, D).

Data-Level Outputs

The ground assertion 1 outputs of the 36 accumulator flip-flop are applied to the output buffer-inverters shown in BS-D-136-0-DAB2, A-B. During output operations, the I/O devices sample the inverter outputs at appropriate phases of the device operating cycles. Negative levels at the inverter outputs correspond to accumulator bits containing ones. The outputs from the six high order accumulator bits, DA0-5, are applied to all six I/O devices. The output data levels are sampled only by the selected device. If bidirectional I/O device 1 or 2 is selected, the high order (left-end) accumulator bits are sampled only during normal tape motion. During reverse tape motion output cycles, the bidirectional devices 1 and 2 receive the six low order bits CA30-35. All 36 outputs are available for connection to the variable character-length devices 5 and 6. Data may be transferred out to these two devices in bytes of 12, 18, or n bits. For 12 or 18-bit characters I/O devices 5 and 6 always sample data from the high order end of the accumulator. For n-bit (n < 36) single-character data words, devices 5 and 6 sample from the low order end of the DA.

Inputs to Data Control from I/O Devices

Besides providing input levels that read data into the data control, the I/O devices also send command pulses to the data control. During output cycles, these pulses indicate to the data control when the selected I/O device is ready to accept another data character. During input cycles, command pulses from the I/O device let the data control know when a new data

character is ready to be read in. The command pulse inputs from the I/O devices govern the generation by the data control of internal command pulses, which in turn cause the data control to sample and shift at appropriate intervals.

Command Pulses from I/O Devices

Command pulse control information to the data control is not the same for all six I/O devices; the specific command pulses sent to the data control depend upon which I/O device is selected.

Bidirectional Devices 1 and 2 - The bidirectional devices send the same command pulses to the data control during both the output cycle and the input cycle. However, the command pulses from these devices do vary depending upon whether the device is functioning in normal tape motion. For both output and input cycles in normal tape motion, a TK/GV CHAR LT (Take or Give a Character Left) command pulse is sent to the data control.

During an output cycle, this pulse indicates to the data control that the I/O device has sampled the output levels from the six high order accumulator bits, DA0-5, and that the data control may shift the accumulator contents left six bits, thus bringing the next character of the data word into position to be sampled by the device. During an input cycle, the TK/GV CHAR LT command pulse indicates that the I/O device has applied a 6-bit input character to the low order accumulator DASH DATA IN RT inputs (described under Data-Level Inputs from I/O Devices below) and that the data control may shift the contents of the accumulator left six bit-positions, and at the same time strobe the input character into the six low-order bit-positions which are made available by the shift.

For both output and input cycles in reverse tape motion, the bidirectional devices send a TK/GV CHAR RT (Take or Give a Character Right) command pulse to the data control.

Unidirectional Devices 3 and 4 - For both output and input cycles, devices 3 and 4 send a TK/GV CHAR LT command pulse to the data control. This pulse serves exactly the same function for unidirectional devices 3 and 4 as it does the bidirectional devices 1 and 2 during normal tape motion.

Variable Character-Length Devices 5 and 6 - The variable character-length devices send the data control a GV CHAR command pulse during the output cycle, but send a TK CHAR command pulse during the input cycle. The GV CHAR command pulse indicates to the data control that the device has accepted the character, and that unless that character was the last in the output data word, the data control must shift the accumulator left by one character length in order to bring the next character into the high order bit positions.

During input operations, devices 5 and 6 send the data control a TK CHAR command pulse when they have presented an input character to the low order strobe data inputs of the accumulator (refer to the following paragraph). This indicates to the data control that it may strobe the character into the low order accumulator bits and then begin to shift the accumulator contents left to make room for the next character that will be read in (unless the character was the last one in the input data word).

Data-Level Inputs from I/O Devices

The paths by which the I/O devices transmit data into the data control also vary depending upon which device is selected for input and (for the bidirectional devices 1 and 2) depending upon which direction of tape motion the device is using.

Dash Data In Right - Devices 1 through 4 read information into the low order (right-end accumulator bits through the DASH DATA IN RT networks shown in BS-D-136-0-DASH, B4-8. These input networks are used by bidirectional devices 1 and 2 only during normal tape motion. The I/O devices apply six input data levels (called DATA IN RT levels) to the Methode plugs shown in BS-D-136-0-DASH, C4-8. Negative levels correspond to 1 bits.

If one of the DC DEVICE SELECT levels 1-4 is asserted negative, data from the corresponding device is gated into the six diode gates 1D2-1D4, and appears at the output terminals of these gates as the six data levels DASH DATA IN 30 RT through DASH DATA IN 35 RT. Since the gates invert the data levels, ground DASH DATA IN RT levels correspond to 1 bits from the devices. The DASH DATA IN RT outputs from the diode gates are strobed into the six low order (right-end) accumulator bits DA30-35 by the same DASH LT pulse that shifts the accumulator contents left. The accumulator readin is described earlier in this section under Accumulator Dash Data Inputs.

Dash Data In Left - During reverse tape motion, bidirectional devices 1 and 2 read information into the high order (left-end) accumulator bits through the DASH DATA IN LT networks shown in BS-D-136-0-DASH, A5-8. The I/O devices apply six DATA IN LT input levels to the Methode plugs 1D10 and 1D12. Negative levels at the gate inputs correspond to 1 bits read in from the I/O devices; the gate outputs are inverted and thus generate ground DASH DATA IN LT levels to represent 1 bits from the devices.

Variable Character-Length Data - The variable character-length devices 5 and 6 send data into the data control through the negative capacitor diode gates shown in BS-D-136-0-DAB2, C-D. The number of active inputs depends on the length of the input data byte; for bytes of less than 36 bits, the data is always sent into the low order bits of the accumulator. Negative inputs represent 1 bits; inactive inputs are not connected. Data from I/O device 5 is gated into the accumulator by the DASH STRB LT (DEV 5) and DASH STRB RT (DEV 5) pulses; data from I/O device 6 is gated into the accumulator by the (DEV 6) DASH STRB pulses.

Resulting Internal Command Pulses

Three sets of internally generated command pulses are produced by the data control in response to the incoming command pulses from the I/O devices. These pulses are: the dash strobe pulses; the dash left and dash right pulses; and the CP0 and CP1 pulses. These pulses strobe data into the accumulator, initiate the accumulator shifts, and control the shift and character counters that indicate to the data control when it has become to the end of a character or data word.

Dash Strobe Pulses

The dash strobe pulses, DASH STRB (DEV 5) and DASH STRB (DEV 6) gate in the variable character-length input data for I/O devices 5 and 6. The pulse amplifiers which generate the DASH STRB (DEV 5) pulse and those which generate the DASH STRB (DEV 6) pulse are shown in BS-D-136-0-DASH, D1. Each of these pulses is generated by two pulse amplifiers and applied to two independent lines, DASH STRB LT (which strobes data through capacitor-diode gates into the 18 high order accumulator bits) and DASH STRB RT (for the 18 low order bits of DA). For either device, the DASH STRB RT and DASH STRB LT lines are always pulsed together .

Dash Left and Dash Right Pulses

The DASH LT pulse always causes the accumulator contents to be shifted left six bit-positions. Furthermore, during input cycles of I/O devices 1-4, DASH LT strobes the input data carried by the six levels DASH DATA IN 30 RT through DASH DATA IN 35 RT into the six low order (right-end) bit-positions of the accumulator (the six bit-positions made available by the left shift).

The DASH RT pulse always causes the accumulator contents to be shifted right six bit-positions, and during input cycles strobes the DASH DATA IN 0 LT through DASH DATA IN 5 LT levels from bidirectional I/O device 1 or 2 into the six high order (left-end) accumulator bit-positions.

Conditions When Dash Right and Dash Left Are Generated (I/O Devices 1-4) - The pulse amplifiers that generate the DASH LT and DASH RT pulses are shown in BS-D-136-0-DASH, A2-3. Pulse amplifier 1A21 generates DASH RT whenever I/O device 1 or 2 is selected and takes or gives a character in reverse tape motion.

Pulse amplifier 1A18 generates the DASH LT pulse under two sets of conditions; one set of conditions applies to I/O devices 1-4, the other applies to I/O devices 5 and 6. The first set of DASH LT conditions, which is implemented by the negative capacitor diode gate at input terminal F of the pulse amplifier, is almost exactly similar to the DASH RT conditions. This set of conditions causes a DASH LT pulse to be generated when a character has been transferred out to or read in from selected I/O device 1-4. (If bidirectional device 1 or 2 is selected, the device must be in normal tape motion to produce a DASH LT.)

Condititons When Dash Left is Generated (I/O Devices 5 and 6) - The second set of input conditions which causes the generation of a DASH LT pulse is less self-evident. The variable character-length devices 5 and 6 can read in or accept data in bytes of 12, 18, or n bits. The n-bit bytes are single-character data words which are not shifted, and thus require no DASH LT pulses. However, each 12-bit character which is read in or transferred out (except the final character in the data word) must be followed by a 12-bit left shift of the accumulator contents. Each non-final 18-bit character is followed by an 18-bit left shift. To implement

these left accumulator shifts, it is necessary, when operating in 12-bit mode, to generate two DASH LT pulses for each character except the last. When operating in 18-bit mode, three DASH LT pulses are needed. Each DASH LT pulse produces a 6-bit left shift.

Circuits Used to Produce Dash Left Pulse - There are four sets of circuits involved in producing the correct dash left shift operations: 1) Pulse amplifier 1A18 is the final circuit which generates the required DASH LT output pulses; 2) the shift counter keeps track of the number of shifts executed; 3) the character counter indicates when the final character of the data word is being transferred out or read in; 4) finally the CP0-CP1 (Command Pulse 0 - Command Pulse 1) network produces the CP1 pulses which initiate the DASH LT pulses and step the shift counter.

The conditions for generating DASH LT during output and input cycles of I/O devices 1-4 are implemented by the capacitor-diode gate at input F of pulse amplifier 1A18 (BS-D-136-0-DASH, A2). Terminals K and L of this same pulse amplifier receive the inputs which govern the generation of DASH LT during output and input cycles by I/O devices 5 and 6. Pulse amplifier 1A18 generates a DASH LT pulse at the arrival of each CP1 pulse at terminal K so long as the DC SCT CONT (Shift Counter Continue) level is asserted at terminal L.

As soon as either the shift counter or the character counter completes its assigned count (indicating that the contents of the accumulator have been sufficiently shifted) the SCT CONT level rises to ground. This prevents any further CP1 pulses from generating a DASH LT, and also resets the shift counter. For a more detailed description of the shift counter operations and logic levels refer to Character Counter IC20-22 and Shift Counter.

DASH CP0 and CP1 Pulses

The DASH CP0 and CP1 pulses (Command Pulse 0 and Command Pulse 1) are generated by the network shown in BS-D-136-0-DASH, B2-3. The CP1 pulse is simply a CP0 pulse delayed 1 μsec by 1310 Delay Line 1A22. The CP1 pulse is the signal that steps the shift counter and character counter and that initiates the appropriate number of DASH LT signals during device 5 and 6 operations with 12- and 18-bit characters. The CP0 pulse is used only for the single purpose of setting the DATA CLBD error flip-flop.

Generated by Device Command Pulses - A CP0 pulse and a CP1 pulse are generated whenever any I/O device sends a command pulse to the data control. Any command pulse from I/O devices 1-4 must produce either a DASH LT or a DASH RT; either of these pulses triggers CP0 and CP1. The variable character-length device command pulses also initiate CP0 and CP1. When a character is transferred out to device 5 or 6, the GV CHAR 5 or GV CHAR 6 pulse directly produces CP0 and CP1. When a character is read in from I/O device 5 or 6, the TK CHAR 5 or TK CHAR 6 pulse first generates a corresponding DASH STRB (DEV 5) or DASH STRB (DEV6) pulse which then triggers pulse amplifier 1A18 to produce CP0 and CP1.

Repetitive Shifts - In addition to following every command pulse from the six I/O devices, CP0 and CP1 may also be produced by DASH LT pulses which are not themselves initiated by command pulses. As mentioned previously, each DASH LT pulse produces a CP1 1 μsec later. Note, however, that the DASH LT pulse itself can in turn be produced by CP1 so long as the DC SCT CONT level is asserted negative (BS-D-136-0-DASH, A2).

The result of this reciprocal causal relationship is a loop. The external command pulse from the I/O device which occurs when a character is first transferred out or read in (for example, GV CHAR 5) causes the generation of the first CP1 pulse for that character. This first CP1 pulse in turn produces a DASH LT pulse (the first DASH LT of the current character) and also constitutes the first shift counter step signal of the current character; CP1 steps the SCT to 01. The first DASH LT pulse initiates a second CP1 (after a delay of 1 μsec). This second CP1 pulse steps the shift counter to 10 (2 octal) and at the same time produces a second DASH LT pulse.

If 12-bit characters are being transferred out to the I/O device, the shift counter is done after being stepped by the second CP1. The second DASH LT can then produce a third CP1 (delayed 1 μsec), but that third CP1 cannot get through to trigger pulse amplifier 1A18. (It is no longer gated through by the DC SCT CONT level. That level ceased to be asserted when the shift counter reached its assigned count, 2 octal, at the second CP1 pulse.) Consequently, no third DASH LT pulse is ever generated. The third CP1 does not step the shift counter, but instead resets it. If 18-bit characters are being transferred out to the I/O device, or being read in from it, the process is similar, except that the shift counter is not done until it reaches a count of 11 (3 octal).

Final Characters Not Shifted for I/O Devices 5 and 6 - During input cycles involving devices 5 and 6, the last character of the data word (the first and only character in n-bit mode, the second character in 18-bit mode, or the third character in 12-bit mode) must not be shifted. If it were shifted, data would be lost out the left end of the accumulator (or for n-bit input cycles at least displaced). During output cycles involving devices 5 and 6, it would of course do no harm to shift the empty accumulator after the last character is transferred out, but this would be useless and is not done.

The logic which implements the data control shift operations prevents any shift pulses from being generated by the readin or transfer out of the final 12, 18, or n-bit character. The command pulse from I/O device 5 or 6 concurrent with the transfer out or readin of the final character does produce a CP0 and CP1 pulse. However, the CP1 is prevented from triggering a DASH LT by the removal of the DC SCT CONT level when the character counter reaches its final assigned count.

The final count of the character counter is always one less than the number of characters in the data word; refer to Table A1-2. The character counter is done at the count of zero for n-bit characters, at the count of one for 18-bit characters, and at the count of two for 12-bit characters. When it reaches its final count in 12- or 18-bit mode, it produces a DC CCT DONE (Character Counter Done) level, thereby terminating the negative DC SCT CONT level and preventing the generation of further DASH LT pulses. In n-bit mode, there is only one character to a data word. Both the character counter and the shift counter are done at the initial zero count. Consequently, no DASH LT pulses are generated.

During output or input cycles involving I/O devices 1-4, completion of the character counter count does not prevent generation of a DASH LT or DASH RT pulse. Such a shift pulse is generated concurrently with the final (sixth) character of the output or input data word. The sixth and final shift pulse is harmless for output cycles, and necessary during input cycles.

OUTPUT CYCLE

The simplified output cycle described in the present section consists of a CONO (Conditions Out) instruction followed by a series of DATAO instructions. Although for practical operations

other routines are employed (refer to Section 4 for a description of sample programs), the input signals to the data control, and the resulting internal cycle, are identical in both cases; the only difference lies in the intervening instructions executed by the processor.

CONO Out Instruction

The CONO Out (Conditions Out) instruction clears the IC register and the accumulator (preserving the contents of the accumulator in DB), and then sets the contents of the IC register to control codes such as those shown in Table A1-6. This prepares the data control for the following DATAO instructions, enabling it to dispatch the data out in appropriate bytes to a selected I/O device, and if required, enabling it to generate a priority interrupt request when more data is needed from the processor. Also see Table A1-7.

CONO Clear Pulse

The processor initiates the data control output sequence by sending the data control on IOB CONO CLR pulse (I/O Bus Conditions Out Clear). This pulse is represented by the initial operation (CONO CLR) of the output flow chart, engineering drawing FD-D-136-0-FD1. It occurs 1 μsec before time 0 of the output timing sequence shown in TD-D-136-0-TD1. The data control receives IOB CONO CLR over one of the I/O bus command lines (BS-D-136-0-DC1, A1); it clears all flip-flops in the IC and DA; the accumulator contents are preserved in the DB.

The IOB CONO CLR triggers pulse amplifiers 1A8 and 1A9, which generate negative and positive DC IC CLR pulses (Data Control Initial Conditions Clear). The positive DC IC CLR from PA 1A0 clears the shift counter and the entire IC register (drawings BS-D-136-0-DC1, B4-7 and BS-D-136-0-DC2, A-B). The negative DC IC CLR from 1A8 is applied to pulse amplifier 1A10 (BS-D-136-0-DC1, C5) which generates DC DA <J> DB. At the conclusion of DC IC CLR, the three status bits, DB DA MOVE, DA RQ, and DB RQ are all in the 0 state; refer to line 1 of Table A1-4.

IOB Reset Pulse

The clearing function described above can be initiated not only by IOB CONO CLR, but also by IOB RESET (BS-D-136-0-DC1, A1). The latter command line is pulsed whenever computer

power is turned on, and whenever the operator presses the I/O reset key on the computer console. The IOB reset triggers pulse amplifiers 1A8 and 1A9, generating negative and positive DC IC CLR pulses in the same manner as IOB CONO CLR. However, IOB RESET also triggers pulse amplifier 1A10 (BS-D0136-0-DC1, B2), generating an additional clear pulse, DC CLR DB, which clears the data buffer.

Device Selection Gating

Because IOB RESET is intended to clear all I/O control units, it causes an unconditional triggering of pulse amplifiers 1A8, 1A9, and 1A10. It is not gated by any device selection code. In contrast, IOB CONO CLR, and in fact all of the eight control line inputs to the data control except IOB RESET and POWER ON, are intended only for one specific addressed control unit, the unit selected by the device selection code in bits 3 through 9 of the CONO instruction. Consequently, these signals are all gated by the output of diode net 1A6 (BS-D-136-0-DC1, D1).

CONO Set Pulse

One μsec after IOB CONO CLR (at time 0 of the output sequence in TD-D-136-0-TD1) the processor sends an IOB CONO SET pulse (I/O Bus Conditions Out Set) to the data control (BS-D-136-0-DC1 B2). The CONO SET is gated by the data control device selection level and then triggers pulse amplifier 1A8 (BS-D-136-0-DC1, A2). The resulting DC IC SET output pulse causes the parallel transfer of the information on the I/O bus into bits 23 through 35 of the IC register. It is assumed for the present example that this sets the IC register flip-flops to the states indicated in Table A1-6. (See also line 2 of Table A1-4.)

First DATAO Instruction

At the completion of the CONO Out instruction, the data control is ready to respond to the next processor instruction, a DATAO (Data Out) instruction. The purpose of this instruction is to transfer a 36-bit data word from the processor into the data control data buffer, from there to transfer it to the data control accumulator, and then finally to shift it out into the selected I/O device.

DATAO Clear Pulse

The first processor signal to reach the data control during the DATAO instruction is the IOB DATAO CLR (I/O Bus Data Out Clear) pulse (BS-D-136-0-DC1, B1). This pulse is represented by the DATAO CLR operation on the output flow chart (FD-D-136-0-FD1). The DATAO CLR, is gated by the device selection level and then triggers pulse amplifier 1A10 (BS-D-136-0-DC1, B2). The resulting DC CLR DB output pulse from PA 1A10 produces two effects. First, it clears the data buffer register DB. Second, DC CLR DB clears the DB RQ flip-flop through diode gate 1B6 (BS-D-136-0-DC2, B3). The latter operation indicates that the DB register is in use, or at any rate is about to be used, and that succeeding instructions must not attempt to transfer data into it until the DB RQ is again set (indicating that DB is once more free to receive data). The state of the three status bits after the DATAO CLR and DC CLR DB pulses is indicated in line 3 of Table A1-4.

DATAO Set Pulse

One μsec after IOB DATAO CLR, the processor sends an IOB DATAO SET pulse (I/O Bus Data Out Set) to the data control (BS-D-136-0-DC1, C1). This pulse is represented by the DATAO SET operation in flow chart FD-D-136-0-FD1. After being gated by the device selection level, DATAO SET is applied to pulse amplifier 1A9.

I/O Bus Loads DB - Pulse amplifier 1A9 produces a 1-μsec negative output pulse, DC DB ←— IOB, which is applied to the Y inputs of the 4230 modules shown in BS-D-136-0-DAB1, D. The leading (negative-going) edge of the DC DB ←— IOB pulse loads the 36-bit output data word which the processor has applied to the I/O bus into bits 0 through 35 of the data buffer.

Set DB DA MOVE - Besides gating the Y inputs of DB, the DC DB ←— IOB pulse is also sent to input terminal S of inverter 1B9 (BS-D-136-0-DC2, B2), the output of which is in turn applied to input M of capacitor-diode 1B10. One μsec later, the positive-going trailing edge of the pulse sets the DB DA MOVE flip-flop momentarily to the 1 state.

FD-D-136-0-FD1, the output flow diagram, shows the 1-μsec width of the DC DB ←— IOB pulse as the delay between the transfers IOB —→ DB and DB DA MOVE ←— 1. Line 4 of Table A1-4 shows that the DATAO SET pulse and the leading edge of DC DB ←— IOB have

2-26

no immediate effect on the configuration of the three status bits. Line 5 shows the change in the state of these status bits 1 μsec later, immediately after the positive-going edge of DC DB ⟵— IOB sets the DB DA MOVE flip-flop.

Generation of DC DB ⟷ DA

The setting of the DB DA MOVE flip-flop causes the sudden appearance of a negative input at terminal M of negative diode 1B7 (BS-D-136-0-DC1, C3). Since the DA RQ flip-flop is already in the 1 state (see line 4 of Table A1-4), the 0 to 1 transition of DB DA MOVE (line 5 of Table A1-4) causes diode 1B7 to generate a positive output pulse, thereby triggering 4604 Pulse Amplifier 1A9 (BS-D-136-0-DC1, C4) which generates a 1-μsec negative output pulse, DC DB ⟷ DA. The double arrow indicates that the pulse occurs whenever there is any transfer (in either direction) between the data buffer and the accumulator (line 6 of Table A1-4).

During this first DATAO instruction, DA RQ is in the 1 state, and it is the transition of the DB DA MOVE flip-flop from 0 to 1 that produces the DC DB ⟷ DA pulse. This is represented by the left branch of the loop in the output flow diagram FD-D-136-0-FD1.

Transfer C(DB) Into DA - During the output sequence, the in/out flip-flop is in the out state (IC27 = 1). Consequently the negative-going leading edge of the 1-μsec pulse DC DB ⟷ DA is gated by DC OUT, and pulse amplifier 1A10 (BS-D-136-0-DC2, C5-6) generates DC DB ⟷ DA. Application of this pulse to the terminal W inputs of the 4230 modules shown in BS-D-136-0-DAB1, D causes the jam transfer of the contents of the data buffer into the accumulator. The 36-bit output data word from the processor is thus stored in the accumulator, ready to be shifted out in a series of bytes to be selected I/O device. The data buffer is free to receive another 36-bit output data word at the execution of the next DATAO instruction (line 6 of Table A1-4).

Other Effects of DC DB ⟷ DA (Leading Edge) - Besides transferring C(DB) into DA, the leading edge of the 1-μsec DC DB ⟷ DA pulse produces two other important results. The application of this negative-going leading edge to input terminals W and Y of inverter 1B19 (BS-D-136-0-DC2, A2-3), causes DB DA MOVE to be reset from 1 to 0, and DB RQ to be set from 0 to 1. The resulting configuration of the three status bits is shown in line 6 of Table A1-4.

Reset of DA RQ - Because the DB RQ flip-flop is again in the 1 state, indicating that the data buffer is free, the processor can immediately execute another DATAO instruction. There is, however, one more operation remaining to be executed in the current, first DATAO instruction. One μsec after DB RQ is set, the positive-going trailing edge of the DC DB ⟨-J-⟩ DA pulse resets the DA RQ flip-flop through terminal P of inverter 1B9 (BS-D-136-0-DC2, B2). The final configuration of the status bits at the end of the first DATAO instruction is reflected by line 7 of Table A1-4.

Further Operations

The reset of the DA RQ flip-flop is represented by the last output operation in the left column of the system flow diagram (FD-D-136-0-FD1). From that point on (any time after line 7 of Table A1-4) the actual transfer-out sequence to the external I/O device can begin. The transfer-out sequence is represented by the right-hand column of the system flow diagram; it is described in Output Transfer Sequence below.

Concurrently with the transfer-out sequence, the data control can, of course, start responding to a second DATAO instruction from the processor. The second DATAO instruction can be commenced any time after the setting of DB RQ to 1 (that is, at any time after line 6 of Table A1-4). However, before the processor executes a second DATAO, it must by some means be notified that DB RQ has in fact been set. The two customary programming methods that let the processor know that DB RQ = 1 (that is, data control is ready to accept more data) are described in Section 4. The second DATAO executed by the processor differs from the first in that the DA RQ flip-flop contained 1 at the commencement of the first DATAO (line 2 of Table A1-4), and in contrast contains 0 (line 7 of Table A1-4) at the beginning of the second DATAO.

Second DATAO Instruction

The data control responds to the second DATAO instruction executed by the processor in a slightly different manner than it responded to the first DATAO. In particular, the jam transfer of C(DB) into DA must wait for the I/O device to complete the first transfer-out sequence.

DATAO Clear and Set Pulses

As with the first DATAO instructions, the first processor signal to reach the data control during the second DATAO instruction is IOB DATAO CLEAR. In following the second DATAO instruction on drawing FD-D-136-0-FD1, jump from the bottom of the diagram (at the conclusion of the first DATAO) back to the point just above the DATAO CLR operation. The initial phase of the second DATAO instruction, down to the branch point, is identical with the first DATAO. Note, however, that the three status bits (shown in line 8 of Table A1-4) are not in the same configuration as they were at the same stage of the first DATAO (line 3 of Table A1-4). The DA RQ flip-flop contains 0, indicating that the accumulator is not yet available to receive data during the current instruction.

As in the first DATAO, 1 μsec after the IOB DATAO CLR the processor sends the data control an IOB DATAO SET. This pulse again produces a 1-μsec DC DB ⟵── IOB pulse, the leading edge of which loads the 36-bit output data word from the I/O bus into the data buffer. The leading edge of this pulse has no effect on the status bits (Table A1-4, line 9), but 1 μsec later, the trailing edge sets the DB DA MOVE flip-flop to the 1 state (line 10 of Table A1-4).

Generation of DC DB ⟨─┼─⟩ DA

During the first DATAO instruction, the 0 to 1 transition of DB DA MOVE triggered the generation of the pulse DC DB ⟨─┼─⟩ DA; this corresponded to the left FIRST PASS ONLY branch of the FD-D-136-0-FD1 output flow diagram. However, during the current second DATAO instruction, the 0 to 1 transition of DB DA MOVE has no immediate effect on the contents of DB. The DA RQ flip-flop does not contain 1, but 0 (see Table A1-4, line 9), when DB DA MOVE is set to 1. Consequently, the system halts with a 1 in the DB DA MOVE flip-flop (at line 10 of Table A1-4). No further operations can be carried out until the word in the accumulator is completely transferred out into the selected I/O device.

When the I/O device transfer-out sequence is complete, and the accumulator is again free to receive data, the final operations of the second output cycle can be carried out. As the last data byte is transferred out from the accumulator into the I/O device, the DC CCT DONE (Character Counter Done) level gates the final DASH CP1 pulse of the current data word through negative capacitor-diode 1B10 (BS-D-136-0-DC2, B2), thereby setting the DA RQ flip-flop to 1, and indicating the end of the transfer-out sequence.

Completion of Second DATAO Cycle

The setting of the DA RQ flip-flop to the 1 state causes the sudden appearance of a negative input at terminal N of negative diode 1B7 (BS-D-136-0-DC1, C3). Since DB DA MOVE = 1, (see line 10 of Table A1-4), the 0 to 1 transition of DA RQ (Table A1-4, line 11) causes diode 1B7 to generate a positive output pulse, thereby triggering pulse amplifier 1A9 (BS-D-136-0-DC1, C4). The pulse amplifier then generates a DC DB $\longleftrightarrow$ DA pulse (represented by the right-hand "A" branch of the output flow diagram at the left of FD-D-136-0-FD1).

The remaining operations of the second DATAO cycle exactly correspond to the final operations of the first DATAO cycle. The leading edge of DC DB $\longleftrightarrow$ DA resets DB DA MOVE to 0 and sets DB RQ to 1. The trailing edge resets the DA RQ flip-flop. The last three configurations of the status bits during the second DATAO (lines 11, 12, and 13 of Table A1-4) are identical to the final configurations of the first DATAO (lines 5, 6, and 7 of Table A1-4).

Additional DATAO Instructions

At the completion of the first DATAO instruction, DB is clear so that the processor can execute a second DATAO immediately. However, the accumulator is still loaded at the completion of the first DATAO instruction, and it remains loaded until the I/O device can receive its contents. This means that after the second DATAO instruction loads the data buffer, the processor must wait for the completion of the first transfer-out sequence to the I/O device. The data control cannot accept a third DATAO instruction until the accumulator is free and the contents of DB have been advanced into the accumulator. The interval between successive DATAO's is governed by the rate at which the I/O device can clear the data control accumulator.

When the last data word has been advanced into the accumulator and transferred out to the I/O device, the DA RQ flip-flop is once more set to 1, indicating that the accumulator is empty and ready to receive data.

Output Transfer Sequence

As soon as DA RQ is reset to 0 (line 7 of Table A1-4) the selected I/O device is free to initiate the output transfer sequence by sending a command pulse to the data control. The output transfer sequence is summarized in the right hand portion (headed by the "B" connector) of FD-D-136-0-FD1, the system flow diagram.

2-30

For I/O devices 1-4, the only branch point in the output sequence is that following the CP1 pulse. If the character counter is not done, the output transfer sequence loops back to point B and continues. If the character counter is done, the character counter is reset, and DA RQ is set. The setting of DA RQ terminates the transfer-out sequence, and the output cycle then proceeds to point A in column 3 of the system flow diagram.

Output cycles of I/O devices 5 and 6 are executed in exactly the same manner for n-bit mode (single-character) cycles. For 12-bit and 18-bit mode operations, there is a nested subordinate loop after the CP1 pulse (the left-hand loop). This loop executes the repetitive shifts described in Resulting Internal Command Pulses. Successive DASH LT pulses are produced until the shift counter is done. This requires one return through the left-hand loop for both the first and second character of the data word in 12-bit mode, and two returns through the left-hand loop for the first character in 18-bit mode.

When the character counter is done, the command pulse associated with the final character produces the final CP1 pulse, thereby resetting both the shift counter and the character counter and setting DA RQ. As in the case of output cycles of devices 1-4, the setting of DA RQ terminates the transfer-out sequence and the output cycle again proceeds to point A.

INPUT CYCLE

The operations making up the data control input cycle are listed in Table A1-5, and are shown in the center portion of the system flow diagram, FD-D-136-0-FD1.

Input Cycle CONO Instruction

The CONO instruction which sets up the data control for the input cycle is executed in the same manner as the output cycle CONO. There are, however, two differences in the coding of the effective address. First, for input operations, the in/out bit is 0. Second, the status bits are set to a different initial configuration. The DB DA MOVE flip-flop must be set to 1, and both DA RQ and DB RQ are 0. (See Table A1-2.)

First Readin Sequence

As soon as the IC register is set up, (line 2 of Table A1-5) the selected I/O device is free to initiate the readin sequence by sending an input command pulse to the data control. The readin sequence is summarized by the same portion of the FD-D-136-0-FD1 flow diagram (headed by the "B" connector) which illustrates the transfer-out sequence. The data control performs exactly the same shift operations during the readin sequence as during the transfer-out sequence. The only difference between the two sequences is that for I/O devices 5 and 6 the DASH STRB internal command pulses are generated only during the readin sequence, but not during the transfer-out sequence.

Completion of First Readin Sequence

At the completion of the first readin sequence, DA RQ is set to 1. This causes the input cycle to advance to point A in column 3 of the system flow diagram, FD-D-136-0-FD1. For the first input cycle, the data control follows the left branch of the loop, the branch immediately below the "A" connector. The contents of the accumulator are advanced to the data buffer (line 4 of Table A1-5), and DB RQ is set to 1, indicating to the processor that the data control is ready to read in data. The processor is then free to execute the first DATAI of the input cycle (from line 7 of Table A1-5). One μsec later DA RQ is reset to 0 (line 5 of Table A1-5). This permits the I/O device to initiate a second readin sequence.

Second Readin Sequence

This second sequence is exactly similar to the first. If the processor has not executed a DATAI instruction before the completion of the second readin sequence, the first data word read in will still be stored in the data buffer. Consequently, the second data word read in (stored in the accumulator) should not be advanced to the buffer until the processor reads in the first data word.

Completion of Second Readin Sequence

At the completion of the second readin sequence, the DB DA MOVE contains 0 rather than 1 as it did at the end of the first readin sequence. Consequently, the 0 to 1 transition of DA RQ cannot carry the input cycle to point A as it did after the first readin. Instead, the data

control must follow the left hand branch of the loop. This means that the DA —J→ DB transfer cannot be initiated by the setting of DA RQ, but must instead wait for the 0 to 1 transition of DB DA MOVE. This transition does not occur until the end of the first DATAI instruction executed by the processor.

First DATAI Instruction

During the DATAO instruction, the processor sends a 2.5-μsec negative level IOB DATAI into the data control (BS-D-136-0-DC1, A1). This level is gated by the data control device selection level, and then (as DC DB —→ IOB) the gated level is applied to the K terminals of the data buffer (BS-D-136-0-DAB1, D). The negative level at the K terminals places C(DB) on the I/O bus for sampling by the processor. The leading edge of this level (that is, the 0 to 1 transition; see the last line at the left-hand of TD-D-136-0-TD1, the system timing diagram) resets the DB RQ flip-flop to 0, thus indicating that the buffer is empty (or about to be empty) and that the processor should not send any further DATAI instructions until the buffer is reloaded (Table A1-5, line 7). The 1 to 0 transition at the trailing edge of the DC DB —→ IOB level sets the DB DA MOVE flip-flop to 1 (Table A1-5, line 8).

Subsequent Operations

When DB DA MOVE is set to 1, the input cycle advances through the left side of the loop below point A. The data word in the accumulator is advanced into the buffer and DB RQ is set to 1 (Table A1-5, line 9). The 1 in DB RQ indicates to the processor that the buffer is loaded, and that the data control is ready to read in a second data word. The processor is therefore free to execute a second DATAI instruction. One μsec later, DA RQ is reset to 0 (Table A1-5, line 10). The selected I/O device is then free to send the command pulse initiating the next readin sequence.

This process continues until the final data word has been read in from the selected I/O device. When that word has been advanced from the accumulator to the buffer, and then read into the processor by a final DATAI instruction (not followed by a DA —J→ DB transfer), the DB DA MOVE is left in the 1 state. The next readin, or series of readins, executed by the I/O device then encounters a completely cleared data control (both accumulator and buffer

empty). The first readin of the new series encounters the 1 in DB DA MOVE and therefore functions like the "first readin sequence" described above. The I/O device can then complete two readin sequences without any requirement to wait for the processor to execute a DATAI instruction.

SECTION 3

INSTALLATION

SITE SELECTION

Before installing the data control, select a suitable location near the PDP-6 arithmetic processor. The data control should be installed within 25 feet of the processor, and the I/O devices should be within 25 feet of the data control.

The data control cabinet is 69-1/2 inches high; width is 22-1/4 inches; depth is 27-1/8 inches. At least 3 feet of clearance should be allowed on all sides of the equipment for access during maintenance. A level floor is required because the equipment frames are mounted on casters. The floor should be capable of supporting 150 psf. The system is designed to operate efficiently from 50° to 100° F. The plug-in modules are cooled by blowing air out the front of the bay. Intake fans are factory-installed in the floor of the bay. No additional cooling equipment is required.

The data control runs on ordinary 115-volt, 60-cycle current. A 10-ampere line is sufficient. The data control power cable is equipped with a Hubble Twist-Loc 3-prong, 30-ampere, 250-volt plug. Although the data control draws only about 3 amperes in normal operation, turn-on surges may reach approximately 5 amperes.

UNPACKING

The data control is shipped on a skid, and may be crated or not, depending on the mode of transportation. For truck shipment it may be left uncrated. A crate is furnished for air shipment. The crate is approximately 74 inches high, 27 inches wide, and 32 inches deep.* The skid upon which it rests is about 6 inches high and 3 feet square. Interconnecting cables are specially made up for each installation, and are shipped with the equipment.

1. If the data control is crated, carefully remove all crating and strapping, and any packing material. If the unit is shipped uncrated, remove the skid and any protective padding.

* The skid upon which it rests is about 6 inches high and 3 feet square.

2. The plenum doors at the rear of the bay have spring catches. To reinforce these doors during shipment two bolts are used to hold each door shut. Remove these bolts and store them in the plastic loops provided.

3. Remove any packing material, shipping blocks, etc. from the inside of the data control.

4. The plug-in modules are taped into the logic panels to prevent damage in shipment. Remove the tape.

> NOTE: If the user plans to reship the equipment (or move it more than a short distance) in the near future, special containers and packing materials should be saved for reuse. These items are designed especially to accomodate the equipment and are the safest means of packing it for reshipment.

INSPECTION

The data control is thoroughly tested and checked before it leaves the factory. However, it should be inspected and checked again when installed to make sure that no damage has occurred during shipment. After the data control is unpacked, check the following:

1. Have all the shipping blocks, packing materials, tape, etc. been removed? If not, remove them.

2. Are all plug-in units inserted firmly in position? Secure any that are loose.

3. Are there any loose nuts or bolts? If so, tighten them.

4. Are there any loose or broken wires? If so, repair them.

CABLE CONNECTIONS

Before connecting cables, complete the inspection procedure given above.

1. Route the four cables from the PDP-6 processor in through the hole in the bottom of the bay. This hole is located directly in front of the fan.

2. Connect the four 22-pin Methode receptacles to the correct Methode plugs at the upper left of the data control logic racks. The four receptacles can be plugged in either to Methode Plugs 1A1-1A4 or to 1B1-1B4, depending on the layout of the specific installation. Each A plug is paralleled with the corresponding B plug; 1A1 is paralleled with 1B1, 1A2 with 1B2, and so on. It is essential that each of the four Methode receptacles at the ends of the processor cables should be connected to the correct pair of plugs. The receptacles should each be marked with the correct plug position. Consult CD-D-166-0-IOMB in Appendix 2 of this manual to make sure that the correct connections are made.

3. Route the 16 I/O device cables (fewer if less than six I/O devices are used) through the hole in the bottom of the bay, and connect the Methode receptacles at the cable ends to the correct plugs 1D10-1D25 at the lower right of the data control logic racks (ID-D-136-0-EDC).

4. A coiled ac power cable is taped to the fan at the bottom of the bay. Remove the tape, route the power cable out through the hole in the bottom of the bay, but do not plug it in.

PREOPERATIONAL CHECKOUT

Before using the data control, make sure that the system turns on and off properly, and that the correct voltages are present at all four logic racks. The checkout procedure makes use of the following switches:

The LOCAL/REMOTE switch at the left of the 811 Power Control. The power control is at the bottom rear of the data control.

The POWER circuit breaker slightly left of center on the 811 Power Control.

The three MCV switches (Marginal Check Voltage) at the front left of each of the four logic racks. In each of these four sets of MCV switches, the top switch is +10 vdc (A), the middle switch is +10 vdc (B), and the bottom switch is -15 vdc. All controls and indicators are described in detail in Section 4.

The following checkout procedure should be carried out after completing the cable connections described above. All voltages are measured from chassis ground with a Multimeter (Simpson Model 260A, Triplett Model 630NA, or equivalent).

1. Put the LOCAL/REMOTE switch in LOCAL position (up).

2. Turn POWER circuit breaker OFF (down).

3. Plug in power cable to 110-volt ac outlet.

4. Put all 12 MCV switches in FIXED position (down).

5. Turn POWER circuit breaker ON (up).

6. Check the fixed (internal) supply voltages at the terminals listed below.

Voltages:	+10 vdc (A)	+10 vdc (B)	-15 vdc
Terminals:	1A25A	1A25B	1A25C
	1B25A	1B25B	1B25C
	1C25A	1C25B	1C25C
	1D25A	1D25B	1D25C

The +10 vdc fixed supply voltages should be between +9.5 vdc and +11 vdc. The -15 vdc should be between -14.5 vdc and -16 vdc. If either voltage falls outside the specified range, the 728 Power Supply probably needs maintenance.

7. With the PDP-6 processor turned off, put the LOCAL/REMOTE switch in the REMOTE position (down). Check each of the fixed voltages at any terminal listed in step 6. No voltage should be present.

8. Turn on the PDP-6 processor. Again check each of the three fixed voltages. The same voltage recorded in step 6 should be present at each of the three terminals checked.

9. Put the LOCAL/REMOTE switch in the LOCAL position (up).

10. Put the four MCV switches which control the +10 vdc (A) lines (upper switch at the left of each logic rack) in the MARGINAL position (up).

11. Make the following settings at the MCV controls above the PDP-6 operator's control panel:

      a. Set polarity switch to +10 volt position (left).

      b. Adjust variac until marginal check voltage meter indicates +5 vdc.

12. Check the +10 vdc (A) voltage at the four terminals specified in step 6. It should coincide with the +5 vdc voltage shown on the marginal check voltage meter.

13. Return the MCV switches for +10 vdc (A) to the FIXED position (down) and set the MCV switches which control the +10 vdc (B) lines (middle switch at the left of each logic rack) to the MARGINAL position (up).

14. Check the +10 vdc (B) voltage at the four terminals specified in step 6. It should coincide with the +5 vdc voltage shown on the marginal check voltage meter.

15. Return the MCV switches for +10 vdc to the FIXED position (down).

16. At the PDP-6 MCV controls, set the MCV polarity switch to the -15 volt position (right) and adjust the variac until the marginal check voltage meter indicates -10 vdc.

17. Set the MCV switches which control the -15 vdc lines (bottom switch at the left of each logic rack) to the MARGINAL position (up).

18. Check the -15 vdc voltage at the four terminals specified in step 6. It should coincide with the -8 vdc voltage shown on the marginal check voltage meter.

19. Return the MCV switches for -15 vdc to the FIXED position (down).

20. Return the LOCAL/REMOTE switch to REMOTE.

21. Return the polarity switch at the PDP-6 to the center (off) position.

22. Turn off the PDP-6.

SECTION 4

OPERATING PROCEDURES AND PROGRAMMING

The purpose of this section is to provide the operator with the information needed to operate and program Data Control Type 136. A short section is devoted to descriptions of the few controls and indicators included in the data control. The remainder of the section describes the PDP-6 programming techniques used to govern the output and input cycles of the data control and its associated I/O devices. A thorough understanding of the relevant PDP-6 programming will not only facilitate operational use of the data control and its I/O devices, but also will be the best aid to efficient maintenance.

CONTROLS AND INDICATORS

Controls

811 Power Control

The 811 Power Control is mounted at the bottom of the data control cabinet. On its front panel (at the rear of the data control) are two controls, a circuit breaker, and a switch.

LOCAL/REMOVE Switch - This switch is located at the left of the 811 Power Control. In the LOCAL position (up), the processor has no effect on the data control power turn-on. The data control power can then be turned on or off by the POWER circuit breaker. The LOCAL position is used primarily for maintenance purposes. For normal operation it is usually more convenient to leave the circuit breaker on and the switch in the REMOTE position (down). The data control power is then turned on by the -15 vdc POWER ON level which is sent to all I/O units while the processor is turned on; refer to Ungated Signals in Section 2.

POWER Circuit Breaker - This circuit breaker is located to the right of the LOCAL/REMOTE switch. When the circuit breaker is in the OFF position (down) the data control power cannot be turned on. When it is in the ON position (up), and the LOCAL/REMOTE switch is

set to LOCAL, the data control power is on. When the circuit breaker is in the ON position, and the LOCAL/REMOTE switch is set to REMOTE, the data control power is on only when the processor power is on.

828 Power Distribution Panel

This convenience panel is located at the front of the data control just below the four logic racks. At the left of the panel is the DISTRIBUTION PANEL circuit breaker. When turned ON (up), this circuit breaker applies power from the hot side of the POWER circuit breaker to the four 110-volt ac 3-prong receptacles on the 828 Distribution Panel. This arrangement permits the application of power to the distribution panel whether or not the data control power is turned on. Power can be removed from all four receptacles by turning the DISTRIBU-TION PANEL circuit breaker off (down).

MCV Switches

There are 12 MCV (Marginal Check Voltage) switches on the front of the data control. One set of three MCV switches is located at the left of each of the four data control logic racks. The top switch in each set governs the +10 vdc (A) power lines, the middle switch governs the +10 vdc (B) lines, and the bottom switch governs the -15 vdc lines. There are two independent +10 vdc supply lines, A and B. The two lines are applied to different logical circuits in each module. This is an aid to trouble isolation because it permits selective application of marginal check voltages. In the FIXED position (down) each MCV switch connects the associated logic rack to the fixed supply voltage from the data control internal 728 Power Supply. In the MARGINAL position (up) each MCV switch connects the associated logic rack to the variable MCV voltage from the processor. This variable MCV voltage can be adjusted at the MCV controls over the operator's control panel of the PDP-6.

MCV Controls at Processor

The processor MCV controls include a 3-position polarity switch (+10 volts, OFF, -15 volts), a variac, and a marginal check voltage meter. When the polarity switch is in the +10 volts position, the variac can apply from 0 vdc to +20 vdc to the +10 vdc (A) and (B) lines. When the polarity switch is in the -15 volts position, the variac can apply from 0 vdc to -20 vdc to the -15 vdc lines.

4-2

Indicators

There are nine indicator lights on indicator card 1B22 (on the front of the data control) at the right of the second logic rack). These indicator lamps display the contents of nine bits of the data control IC register. When the lamps are on, the corresponding bits contain ones, when off, zeros. The nine bits represented by the nine front panel indicator lamps are shown in Table 4-1.

TABLE 4-1   FRONT PANEL INDICATOR LAMPS
(Listed from Top to Bottom)

Bit Designation	Location
DA RQ	IC25
DB RQ	IC26
DBDA MOVE	IC24
IN/OUT	IC27
CH MODE 0	IC28
CH MODE 1	IC29
CCT 0	IC20
CCT 1	IC21
CCT 2	IC22

PROCESSOR INSTRUCTION CODING

Input-output instructions executed by the processor initiate all data control operations. Every IOT instruction in the PDP-6 repertoire is coded with the format shown with PDP-6 Handbook, F-65, page 22. The CONO-DATA CONTROL address coding is summarized for the operator's convenience in Table A1-7 in Appendix 1.

SAMPLE PROGRAMS

There are two ways in which the processor can be notified that the data control is ready for another data word: by an active priority interrupt request, or by passively waiting for the processor to sample IC26, the DB RQ flip-flop.

The first method of notifying the processor, the passive sampling method, is illustrated by the output and input programs presented in Use of Data Control Without Priority Interrupt, below. This method has the disadvantage of keeping the processor tied up during the entire output or input cycle even though the operations required of it take only a small fraction of the time used by the I/O device. Nevertheless, this method might be used if the programmer wished to to have the processor complete an output or input sequence before proceeding to other operations.

The second method of notifying the processor that the data control is ready, the active priority interrupt request, is illustrated by the output and input programs presented in Use of Data Control with Priority Interrupt, below. This second method is often the more efficient, in that neither the processor nor the I/O device ever need be idle. The I/O device operates asynchronously at its own speed, and the processor takes part in the output or intput sequence only during the brief intervals needed to transfer a data word out to DB or to read a data word in from DB. The processor never has to wait for the comparatively slow output transfer sequence or readin sequence of the I/O device, but instead is used only for fast, parallel, full data-word transfers to and from the data control itself.

Use of Data Control Without Priority Interrupt

The following sample programs illustrate the use of the data control without the priority interrupt system.

SAMPLE OUTPUT PROGRAM $\overline{PI}$

```
100/CONO DC, (DARQ, DBRQ, OUT, MODE, DEVICE #)
101/CONSO DC, DBRQ
102/JRST, .-1
103/BLKO DC, STORE
104/JRST, DISMISS
105/JRST, .-4
```

SAMPLE INPUT PROGRAM $\overline{PI}$

100/CONO DC, (DBDA MOVE, IN, MODE, DEVICE #)
101/CONSO DC, DB RQ
102/JRST, .-1
103/BLKI DC, STORE
104/JRST, DISMISS
105/JRST, .-4

When using the Data Control out of the PI system, the IC register is set up by the instruction in 100. At the next instruction (101) the DB RQ flag is interrogated. If it is a 1, the next instruction (102) is skipped; if it is a 0, instruction 102 is executed. Instruction 102 says: jump from this location minus one instruction (to instruction 101). Therefore the program remains in this loop until DB RQ becomes a 1. The next instruction is BLKO or BLKI (depending on direction of word transfer). This instruction executes a data instruction (DATAO or DATAI) and skips the next instruction and jumps back to 101. This process is repeated until the entire block of information has been read in or transferred out. When the block is complete, the program executes 104 and jumps to a dismiss routine or another part of the main program.

Use of Data Control With Priority Interrupt

The following sample programs illustrate the use of the data control with the priority interrupt system.

SAMPLE OUTPUT PROGRAM PI

100/CONO DC, (DARQ, DBRQ, OUT, MODE, DEVICE #, PI # 1)
101/JRST, .
42/BLKO DC, STORE
43/JSR, DISMISS

SAMPLE INPUT PROGRAM PI

100/CONO DC, (DBDA MOVE, IN, MODE, DEVICE #, PI # 1)
101/JRST, .
42/BLKI DC, STORE
43/JSR, DISMISS

When using the data control with the PI system, the IC register is set up by the instruction in 100; note also that PI channel #1 is selected. The program then executes 101, which jumps to itself until an interrupt occurs. When an interrupt has occurred, the program executes the BLKO or BLKI instruction in location 42. After each data instruction (DATAO or DATAI) the program returns to 101, and iterates that one-instruction loop until the next interrupt. The instruction in 43 will be executed only when the entire block of information has been transferred. In these two sample programs, the JRST one-instruction loop in 101 takes the place of an actual operating routine. For actual working programs, the return would be to a more useful routine.

Further discussion of input-output programming is presented in the PDP-6 Handbook, F-65, on pages 51, 52, and 65 through 68.

SECTION 5

MAINTENANCE

The data control is ordinarily used as a peripheral system of the PDP-6 processor installation. The maintenance chapter of the processor manual covers a number of topics not repeated in the data control manual, but essential to efficient maintenance of all DEC systems used with the PDP-6, including the data control. These topics include Special Tools and Test Equipment, Log Entries, Maintenance Programs, Use of Marginal Check, Troubleshooting, and Module Removal and Repair.

CAUTION

The procedures described in the maintenance chapter of the PDP-6 processor manual should be thoroughly understood before undertaking the troubleshooting and repair of the data control.

USE OF DRAWINGS

The complete system logic is shown in the engineering logic drawings, in Appendix 2. BS-D-136-0-DC1 and DC2, BS-D-136-DAB1 and DAB2, and BS-D-136-0-DASH. Because these five drawings are the most frequently used source of troubleshooting information, it is important to be familiar with the symbols and conventions which they employ. The symbols used on these drawings are explained in Figure A2-1, DEC Logic Symbols, which precedes the engineering drawings in Appendix 2. A more detailed explanation of DEC logical design is presented in the Digital Logic Handbook.

Equipment Layout

The data control logic is contained in four DEC logic racks designated from top to bottom 1A-1D. The modules located in each rack position, and the function of each module, are shown in UML-D-136-0-DCML, Sheets 1 and 2, the logic-rack layout diagrams in Appendix 2. Power wiring is shown in PW-D-136-0-DCPW. The power supply is shown in RS-728. The power control is in RS-811. Circuit schematics of all data control modules are also presented in Appendix 2.

PREVENTIVE MAINTENANCE

Preventive maintenance procedures should be performed on a regular basis. By appropriate use of scheduled preventive maintenance techniques (described in the Arithmetic Processor portion of the PDP-6 Maintenance Manual) most potential malfunctions can be detected before they occur.

The cooling fan in the bottom of the bay should be checked daily for proper operation and free flow of air. Under normal operating conditions the air filter at the bottom of the bay should be changed and cleaned monthly. The correct procedure for changing and cleaning filters is described in the maintenance chapter of F-67(166).

RECOMMENDED SPARE PARTS

The most economical quantity of spare parts to be maintained depends on the requirements of the individual user, but the following listing is suitable for most installations.

Module Spares

Module	Quantity
1310	1
1669	1
4102	1
4112	1
4113	1
4118	1
4127	1
4129	1
4143	1
4150	1
4151	1
4215	1
4217	1
4230	2

Module	Quantity
4604	1
4606	1
4657	1
6102	1
6115	1
6117	1
6684	1

Component Spares

	Type		Quantity
Transistors:	2N456A	RCA	2
	2N485	Sprague	2
	2N489	Sprague	3
	2N599	GE	5
	2N711A	GE	3
	2N1184	RCA	3
	2N1184B	RCA	2
	2N1204	Motorola	3
	2N1304	GE	2
	2N1305	GE	5
	2N527	GE	5
	2N2451	Sprague	8
	2N1754*	General Instruments	3
	2N1754	General Instruments	5
	2N393	General Instruments	2

*BVCES 40V at 100 μa

	Type		Quantity
Diodes:	1N270	Transitron	1
	1N276	Transitron	20
	1N645	Transitron	15
	1N994	Transitron	4

	Type		Quantity
	1N1217	GE	2
	1N1220	GE	1
	1N429 (Zener) Motorola		1
	1N3316 (Zener) Motorola		1
	GRS20SP4B4	GE	1
Pulse Transformers:	T2003	DEC	3
	T2006	DEC	1.
	T2010	DEC	2
	T2012	DEC	1
	T2017	DEC	1
	T2018	DEC	1
	T2019	DEC	1
	T2020	DEC	1
	T2021	DEC	1
	T2023	DEC	1
	T2024	DEC	2
	T2029	DEC	2
	T2033	DEC	1

Mechanical Spares

Part Number and Description	Quantity
53E168, Type CFG: Rotron fan with #2R blade	1
X-1431, 10" x 10" x 2" EZ Kleen Filter	1
Type 418 Super Filter Kote, pints	1

Table A1-1   IC Register Bit Assignment

APPENDIX 1

FOLDOUT TABLES

TABLE A1-1 IC REGISTER BIT ASSIGNMENT

Field	Bit No.	Flip-flop Designation	Meaning of Designation
Character Counter	20	CCT 0	Character Counter Bits 0-2
	21	CCT 1	
	22	CCT 2	
Error Bit	23	DATA CLBD	Data lost; error condition (clobbered)
Status Bits	24	DBDA MOVE	Buffer-Accumulator Transfer Synchronization Flip-flop
	25	DA RQ	Data Accumulator Request Flip-flop
	26	DB RQ	Data Buffer Request Flip-flop
Input/Output	27	IN/OUT	Input/Output Flip-flop
Character Mode	28	CH MODE 0	Character Mode Bits 0-1
	29	CH MODE 1	
Internal Device Address	30	DEVICE 0	Internal Device Address Bits 0-2
	31	DEVICE 1	
	32	DEVICE 2	
Priority Interrupt Assignment	33	PIA 0	Priority Interrupt Assignment Bits 0-2
	34	PIA 1	
	35	PIA 2	

Table A1-2   Shift-Counter and Character Counter Done

TABLE A1-2   SHIFT-COUNTER AND CHARACTER COUNTER DONE

Char Mode IC28-29	No. of Bits in Char	No. of Shifts per Char	C(SCT) When DC SCT DONE	Asserted Output	No. of Char per Word	No. of Char per Word-1	C(CCT) When DC CCT DONE	Asserted Output
				I/O Devices 1-4				
0 0	6	1 *	0 0	1A13V	6	5	101	1A15Z
				I/O Devices 5 and 6				
0 1	n**	0	0 0	1A13V	1	0	000	1A15T
1 0	12	2	1 0	1A13R	3	2	010	1A15L
1 1	18	3	1 1	1A13K	2	1	001	1A14L

* Occurs at read in or transfer out command. Not governed by SCT.

** $1 \leq n \leq 36$

Table A1-3   Significance of DA RQ and DB RQ States

TABLE A1-3 SIGNIFICANCE OF DA RQ AND DB RQ STATES

DA RQ			
State	In/Out	Data Accumulator is:	Data Control is:
DA RQ = 0	Out	Loaded	READY to transfer out to I/O device
DA RQ = 0	In	Empty	READY to read in from I/O device
DA RQ = 1	Out	Empty	NOT READY to transfer out
DA RQ = 1	In	Loaded	NOT READY to read in

DB RQ			
State	In/Out	Data Accumulator is:	Data Control is:
DB RQ = 0	Out	Loaded	NOT READY for transfer out from processor
DB RQ = 0	In	Empty	NOT READY to read in to processor
DB RQ = 1	Out	Empty	READY for transfer out
DB RQ = 1	In	Loaded	READY to read in

Table A1-4   Configurations of Status Bits During Output Cycle

TABLE A1-4 CONFIGURATIONS OF STATUS BITS DURING OUTPUT CYCLE

Line	Preceding Event	Configuration of Status Bits			Loaded Registers
		DBDA MOVE (IC 24)	DA RQ (IC 25)	DB RQ (IC 26)	
CONO (Out) Instruction:					
1	CONO CLR, DC IC CLR	0	0	0	None
2	CONO SET, DC IC SET	0	1	1	None
First DATAO Instruction:					
3	DATAO CLR, DC CLR DB	0	1	0	None
4	DATAO SET, DC DB ←—IOB	0	1	0	DB
5	1 μsec delay: DC DB ←—IOB (t.e.)*	1	1	0	DB
6	DC DB ←↓→ DA (l.e.)	0	1	1	DB-DA (same word)
7	1 μsec delay: DC DB ←↓→ DA (t.e.)	0	0	1	DB-DA (same word)
Second DATAO Instruction: (can begin any time after line 6)					
8	DATAO CLR, DC CLR DB	0	0	0	DA
9	DATAO SET, DC DB ←—IOB	0	0	0	DB, DA
10	1 μsec delay: DC DB ←—IOB (t.e.)	1	0	0	DB, DA
Transfer-out Sequence: (can begin any time after line 7; duration depends on I/O device data rate)					
11	Transfer-out completed (CCT DONE and CP1)	1	1	0	DB
12	DC DB ←↓→ DA (l.e.)	0	1	1	DA
13	1 μsec delay: DC DB ←↓→ DA (t.e.) (at any time hereafter a second transfer-out sequence can begin)	0	0	1	DA
Third and Succeeding DATAO Instructions: (Same as second DATAO. Can begin any time after line 12.)					

* Note: l.e. = leading edge of pulse; t.e. = trailing edge.

Table A1-5   Configurations of Status Bits During Input Cycle

TABLE A1-5 CONFIGURATIONS OF STATUS BITS DURING INPUT CYCLE

Line	Preceding Event	Configuration of Status Bits			Loaded Registers
		DBDA MOVE (IC 24)	DA RQ (IC 25)	DB RQ (IC 26)	
CONO (In) Instruction:					
1	CONO CLR, DC IC CLR	0	0	0	None
2	CONO SET, DC IC SET	1	0	0	None
First Read-in Sequence: (Note that read-in duration depends on I/O device data rate.)					
3	Read-in completed. (CCT DONE and CP1)	1	1	0	DA
4	DC DB ⟷ DA (l.e.)*	0	1	1	DB
5	1 μsec delay: DC DB ⟷ DA (t.e.)	0	0	1	DB
Second Read-in Sequence: (can begin any time after line 5)					
6	Read-in completed (CCT DONE and CP1)	0	1	1	DA, DB
First DATAI Instruction: (can occur any time after line 4)					
7	IOB DATAI 0 ⟶ 1, DB ⟶ IOB	0	1	0	DA
8	2.5 μsec delay: IOB DATAI 1 ⟶ 0	1	1	0	DA
9	DC DB ⟷ DA (l.e.) (at any time hereafter a second DATAI can begin.)	0	1	1	DB
10	1 μsec delay: DC DB ⟷ DA (t.e.) (at any time hereafter another read-in can begin.)	0	0	1	DB

* Note: l.e. = leading edge of pulse; t.e. = trailing edge.

A1-9

Table A1-6   CONO Bit Assignments - Output Cycle

TABLE A1-6 CONO BIT ASSIGNMENTS - OUTPUT CYCLE

Bit No.	Contents	Meaning
23	0	No DATA CLBD error condition present.
24	0	Initial state of DADB MOVE synchronizing flip-flop.
25	1	DA RQ = 1; indicates that accumulator is initially empty.
26	1	DB RQ = 1; indicates that data buffer is initially empty.
27	1	An output cycle follows.
28-29	00	Data to be sent out in 6-bit character mode.
30-32	001	Data to be sent to I/O device No. 1.
33-35	011	Priority Interrupt Channel No. 3 assigned to data control.

Table A1-7   Effective Address Coding for CONO Data Control Instructions

TABLE A1-7 EFFECTIVE ADDRESS CODING FOR CONO DATA CONTROL INSTRUCTIONS

Bit Nos.	Field	Configuration	When Applicable
23	Error Bit	0	All Cycles
24-26	Status Bits	X 1 1	Output Cycles
		1 0 0	Input Cycles
27	In/Out	1	Output Cycles
		0	Input Cycles
28-29	Character Mode	0 0	All 6-bit Cycles
		0 1	All n-bit Cycles ($1 \leq n \leq 36$)
		1 0	All 12-bit Cycles
		1 1	All 18-bit Cycles
30-32	Internal Device Address	0 0 1	I/O Device No. 1
		0 1 0	I/O Device No. 2
		. . .	. . . .
		1 1 0	I/O Device No. 6
33-33-35	Priority Interrupt Assignment	0 0 0	No PI Assignment
		0 0 1	PI Request Channel 1 Assigned
		. . .	. . . .
		1 1 1	PI Request Channel 7 Assigned

APPENDIX 2

ENGINEERING DRAWINGS

Reduced engineering drawings are produced in this appendix as an aid to understanding and maintaining the system. A complete set of formal engineering drawings is supplied separately with each system. Should any discrepancy exist between the drawings in this manual and those supplied with the equipment, assume the formal drawings to be correct.

Refer to the Table of Contents for a complete list of engineering drawings for this system and the pages on which the drawings appear.

For all modules illustrated, circuit type is always shown as a 4-digit number. This number is the same type number used to identify the circuit in the DEC System Modules Catalog.

> Examples: 1310 – – – Delay Line (5-mc series)
>
> 4112 – – – Six 2-Input Negative Diode Gates (500-kc series)

On all circuit modules the circuit location code is lettered directly below the circuit type number. Circuit location code is shown as a single letter preceded by one digit and followed by one or two digits.

> Example: 1 A 1 2 E – – Pin E of
>
> | | | ___ ___ the module located in position 12
>
> | |___ ___ ___ of logic rack A
>
> |___ ___ ___ ___ in bay 1

As indicated on certain block schematics, the normal 4-digit module identification number is followed by the letter "R." This letter indicates that these modules contain internal jumpers which connect output terminals to clamped load resistors located on the module. Such modules are shipped from Digital with all jumpers connected. Before these modules can be installed in a particular Digital component, the module user must consult the block schematic for that component to determine which jumpers are to be removed and which jumpers are to remain connected.

Each engineering logic drawing is divided into 32 zones (4 horizontal, and 8 vertical) by marginal map coordinates. Figure references in the text are usually followed by a letter and a digit specifying the zone in which the referenced circuit is located.

SYMBOLS AND TERMINOLOGY

Engineering drawing numbers for this equipment contain five pieces of information, separated by hyphens. Read from left to right these bits of information are a 2-letter code specifying the type of drawing, a 1-letter code specifying the size of the drawing, the type number of the equipment, the manufacturing series of the equipment, and a 2-digit number specifying the number of a drawing within a particular series. The drawing type codes are:

     a. BS, block schematic or logic diagram

     b. CD, cable diagram

     c. CS, circuit schematic

     d. FD, flow diagram

     e. ID, interconnection drawing

     f. PW, power wiring

     g. RS, replacement schematic

     h. SD, system diagram

     i. TD, timing diagram

     j. TFD, timing and flow diagram

     k. UML, utilization module list

     l. WD, wiring diagram

Logic Signals

All logic signals are either standard Digital logic levels or standard Digital pulses. A standard Digital logic level is either a ground (0 to -0.3 volts) or -3 volts (-2.5 to -3.5 volts). Logic signals are generally given mnemonic names which indicate the condition represented by assertion of the signal. An open diamond (——◇) indicates that the signal is a level and that ground represents assertion; a solid diamond (——◆) indicates that the signal is a level and that -3 volts represents assertion. All logic levels applied to the conditioning-level inputs of capacitor-diode gates must be present either 1 or 3 microseconds (depending on the module used) before an input triggering pulse is applied to the gate.

A2-2

The standard Digital negative pulse is indicated by a solid triangle (——▶) and goes from ground to – 2.5 or – 3 volts (– 2.3 to – 3.5 volt tolerances). The standard Digital positive pulse, indicated by an open triangle (——▷), goes either from – 3 volts to ground or from ground to + 2.5 volts (+ 2.3 to + 3.0 volts). The width of the standard pulses used in this equipment is either 1.0, 0.4, or 0.07 microseconds, depending on the module and application.

Occasionally, the transition of a level is used at an input where a standard pulse is otherwise expected and a composite symbol (——◇▷) is drawn to indicate this fact. The triangle is drawn open or solid depending respectively on whether the positive (– 3 volt to ground) or the negative (ground to – 3 volt) transition triggers circuit action. The shading of the diamond either is the same as that of the triangle to indicate triggering on the leading edge of a level, or is opposite that of the triangle to indicate triggering on the trailing edge.

Any other signal is non-standard and is indicated by an arrowhead (——▷) pointing in the direction of signal flow. Figure A2-1 shows the standard symbols used in all Digital logic drawings.

NON-STANDARD SIGNAL

POSITIVE PULSE

NEGATIVE PULSE

POSITIVE LEVEL

NEGATIVE LEVEL

LEVEL TRANSITION USED AS A PULSE

TRIGGERING ON THE TRAILING EDGE
OF A PULSE

CLAMPED LOAD

PNP TRANSISTOR INVERTER
1. BASE
2. COLLECTOR
3. EMITTER

POSITIVE NAND, NEGATIVE NOR DIODE GATE
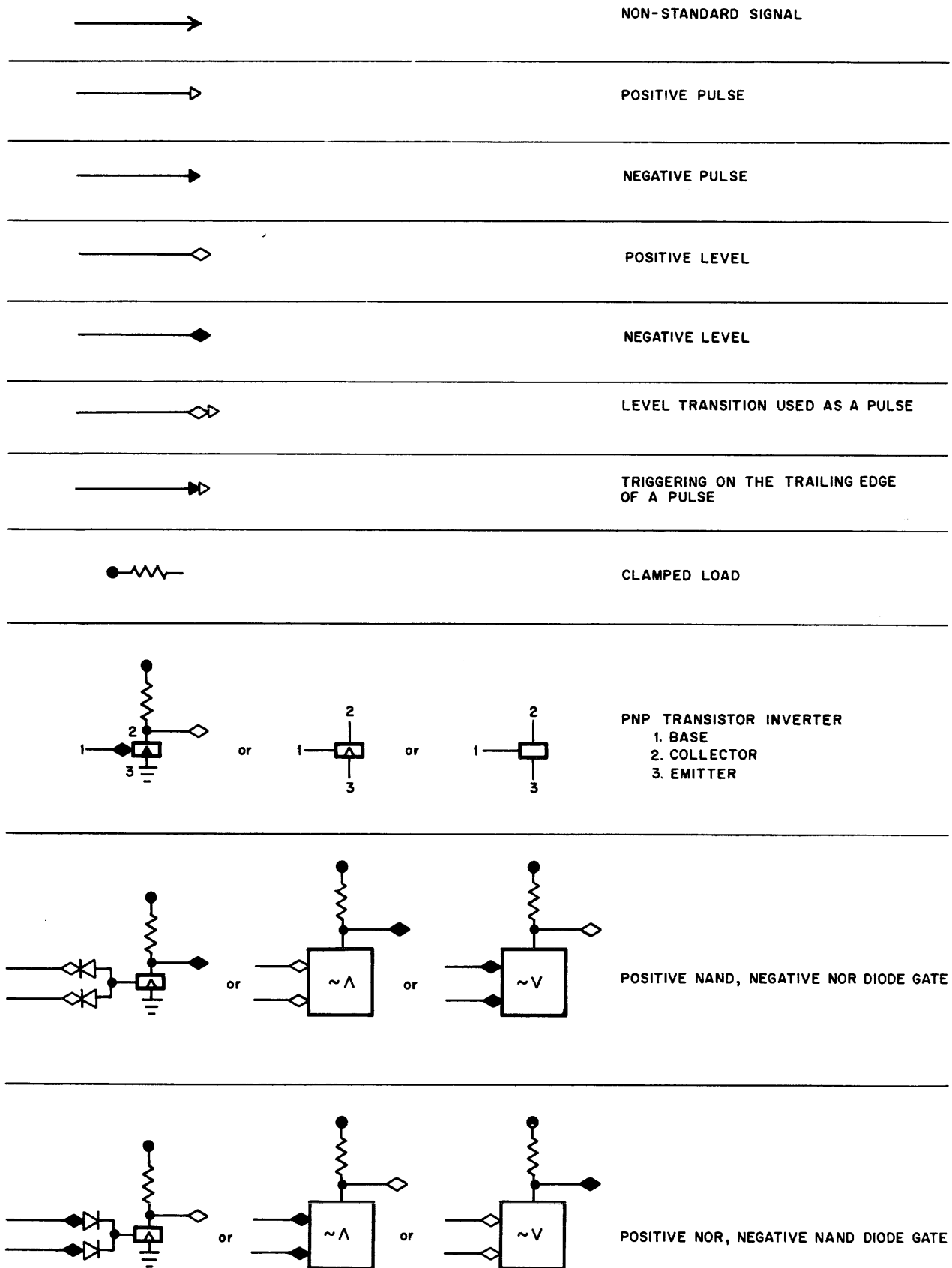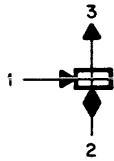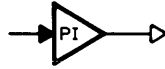
POSITIVE NOR, NEGATIVE NAND DIODE GATE

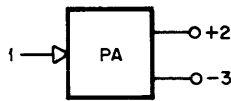Figure A2-1   DEC Logic Symbols

CAPACITOR-DIODE GATE, POSITIVE OR NEGATIVE
INDICATED BY POLARITY OF THE INPUTS.
    1. PULSE INPUT
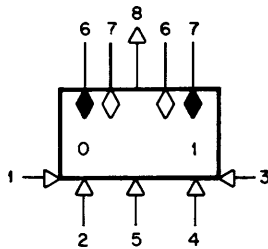   2. CONDITIONING LEVEL INPUT
    3. PULSE OUTPUT

PULSE INVERTER

PULSE AMPLIFIER
    1. PULSE INPUT, POLARITY INDICATED
       BY INPUT SIGNAL
    2,3. TRANSFORMER-COUPLED PULSE
        OUTPUT

FLIP-FLOP (MOST FLIP-FLOPS HAVE ONLY SOME
OF THE FOLLOWING):
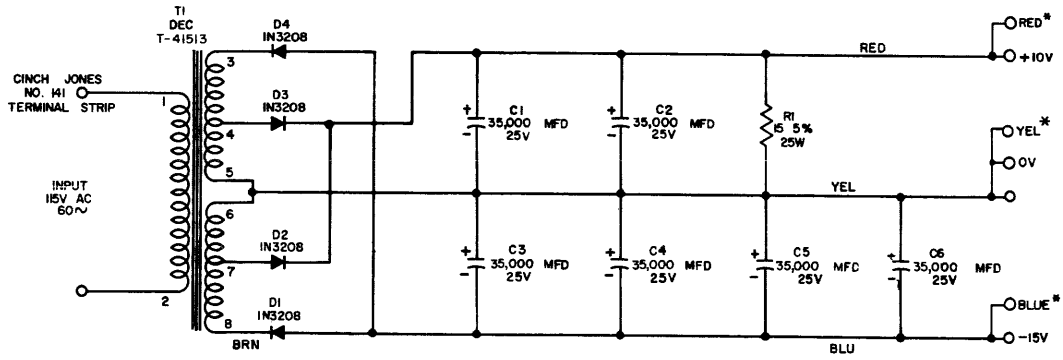   1. DIRECT-CLEAR INPUT
    2. GATED-CLEAR INPUT
    3. DIRECT-SET INPUT
    4. GATED-SET INPUT
    5. COMPLEMENT INPUT
    6. OUTPUT LEVEL, -3 V IF 0, 0 V IF 1
    7. OUTPUT LEVEL, 0 V IF 0, -3 V IF 1
    8. CARRY PULSE OUTPUT
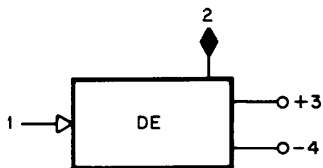
DELAY (ONE-SHOT MULTIVIBRATOR)
    1. INPUT PULSE
    2. OUTPUT LEVEL, -3V DURING DELAY
    3,4. TRANSFORMER-COUPLED PULSE
        OUTPUT

Figure A2-1   DEC Logic Symbols (continued)

Power Supply RS-728

T1
DEC
T-41513

CINCH JONES
NO. 141
TERMINAL STRIP

INPUT
115V AC
60 ~

D4 IN3208
D3 IN3208
D2 IN3208
D1 IN3208

BRN

C1 35,000 MFD 25V
C2 35,000 MFD 25V
R1 15 5% 25W

C3 35,000 MFD 25V
C4 35,000 MFD 25V
C5 35,000 MFD 25V
C6 35,000 MFD 25V
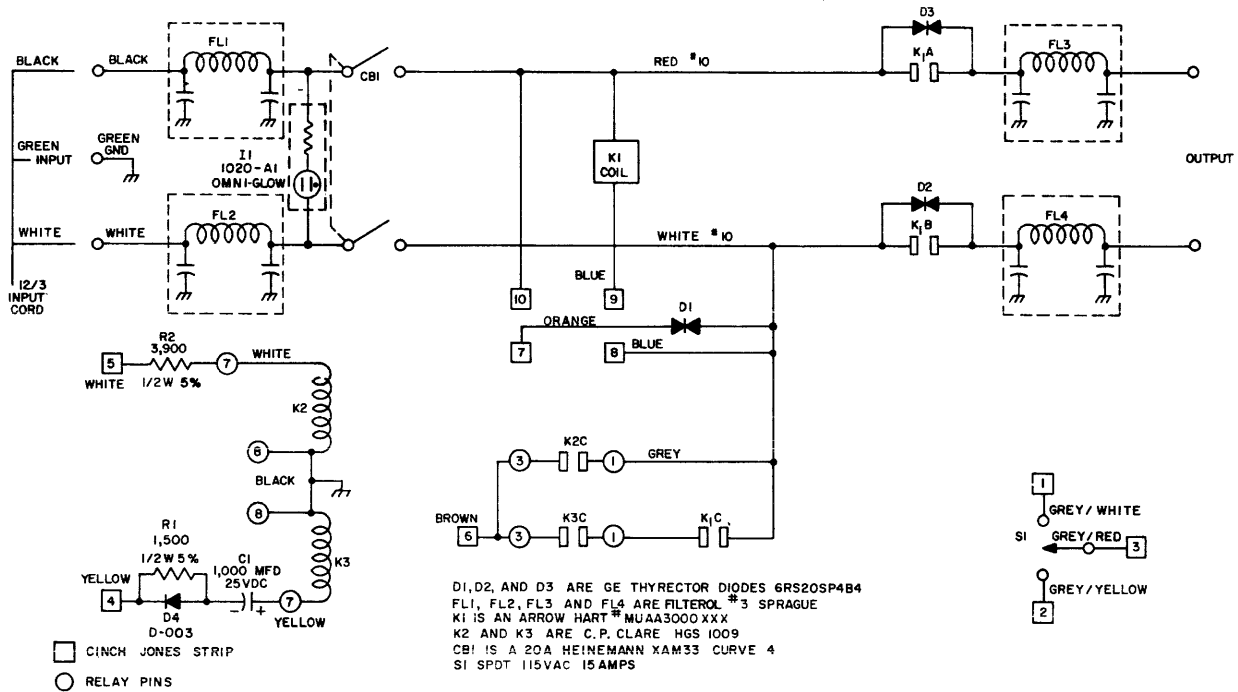
RED
YEL
BLU

RED* +10V
YEL* 0V
BLUE* -15V

* HEYMAN MFG. CO.
TAB TERMINALS

NOTE:
IN ORDER TO KEEP OUTPUT VOLTAGE WITHIN THE FOLLOWING LIMITS:
+10V: +9.5 TO +11V
-15V: -14.5 TO -16V
THE LOADING SHOULD BE WITHIN THE FOLLOWING LIMITS:
BOTH SIDES   +10V   0   TO   7.0   AMPS
LOADED   -15V 1.0 TO   8.0   AMPS
ONE SIDE   +10V   0   TO   7.5   AMPS
LOADED   -15V 1.0 TO   8.5   AMPS
SUM OF THE OUTPUT CURRENTS ARE LIMITED BY THE FOLLOWING
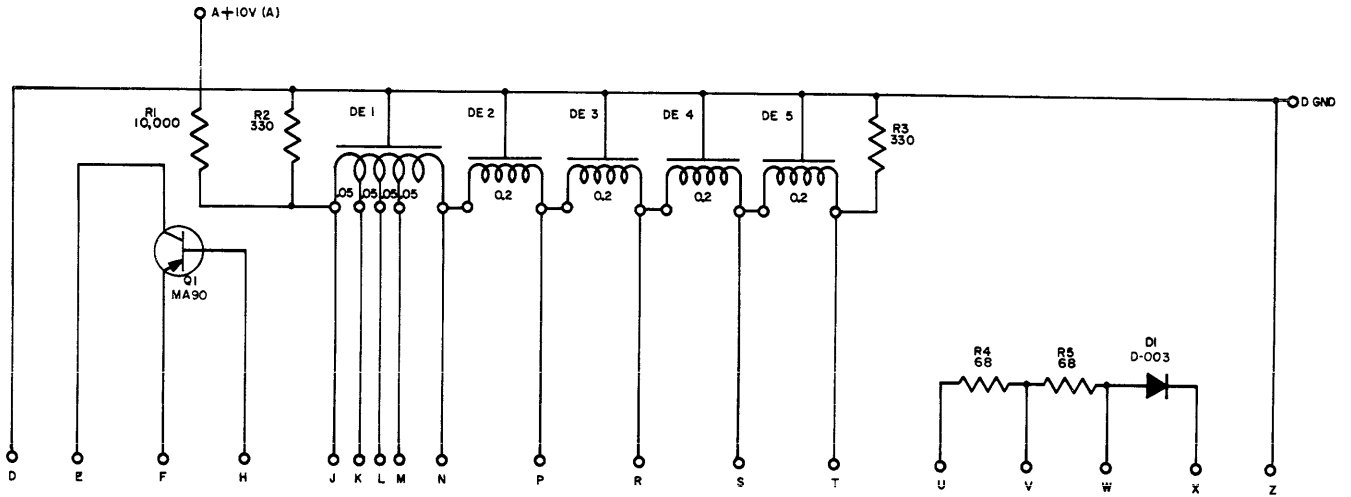EQUATION: $5 I_{10} + 6 I_{15} \leq 53$

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
IN3208	IN3208		

Power Control RS-811

BLACK
GREEN — INPUT
WHITE
12/3 INPUT CORD

BLACK
GREEN GND
WHITE

FL1
FL2
CB1

I1
1020-A1
OMNI-GLOW

RED #10
WHITE #10

K1 COIL

D3
K1A
FL3

D2
K1B
FL4

OUTPUT

R2 3,900
WHITE 1/2W 5%
K2
BLACK
R1 1,500 1/2W 5%
YELLOW
C1 1,000 MFD 25VDC
D4 D-003
K3
YELLOW

10
9
BLUE
ORANGE
D1
7
8 BLUE

K2C
3
GREY
BROWN
6
3
K3C
K1C

I
GREY/WHITE
S1 GREY/RED 3
GREY/YELLOW
2

D1, D2, AND D3 ARE GE THYRECTOR DIODES 6RS20SP4B4
FL1, FL2, FL3 AND FL4 ARE FILTEROL #3 SPRAGUE
K1 IS AN ARROW HART # MUAA3000 XXX
K2 AND K3 ARE C.P. CLARE HGS 1009
CB1 IS A 20A HEINEMANN XAM33 CURVE 4
S1 SPDT 115VAC 15 AMPS

☐ CINCH JONES STRIP
○ RELAY PINS

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D-003	IN994		

A2-6

A + IOV (A)

R1
10,000

R2
330

DE 1

DE 2

DE 3

DE 4

DE 5

R3
330

D GND

.05 .05 .05 .05

0.2

0.2

0.2

0.2

Q1
MA90

R4
68

R5
68

D1
D-003

D   E   F   H   J K L M   N   P   R   S   T   U   V   W   X   Z
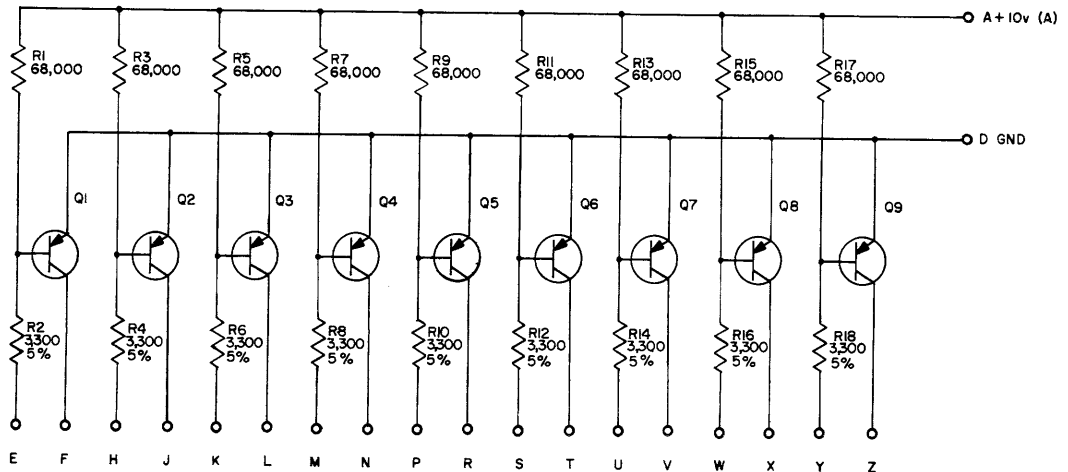
UNLESS OTHERWISE INDICATED:
   RESISTORS ARE 1/2W; 10%
   DE1= TECHNITROL 0.2 μ sec DELAY LINE 330 OHMS
         TAPPED AT 0.05 μ sec. INTERVAL
   DE2= DE5 TECHNTROL 0.2 μ sec. DELAY LINE

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
MA90	2N2481		
D-003	1N994		

Delay Line RS-1310

A + IOv (A)

R1
68,000

R3
68,000

R5
68,000

R7
68,000

R9
68,000

R11
68,000

R13
68,000

R15
68,000

R17
68,000

D GND

Q1   Q2   Q3   Q4   Q5   Q6   Q7   Q8   Q9

R2
3,300
5%

R4
3,300
5%

R6
3,300
5%

R8
3,300
5%

R10
3,300
5%

R12
3,300
5%

R14
3,300
5%

R16
3,300
5%

R18
3,300
5%

E   F   H   J   K   L   M   N   P   R   S   T   U   V   W   X   Y   Z

UNLESS OTHERWISE INDICATED:
   RESISTORS ARE 1/4W; 10%
   TRANSISTORS ARE 4JX1C741
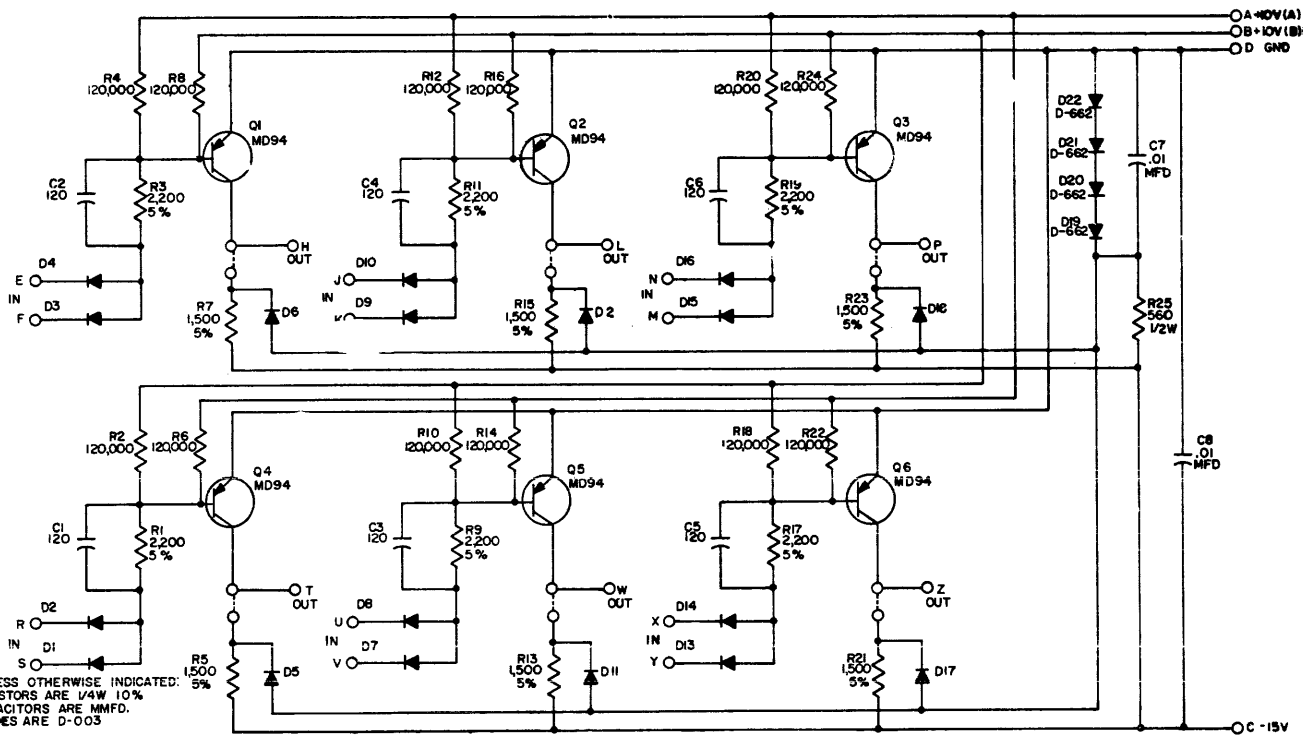
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
4JX1C741	2N527		

Indicator Driver RS-1669
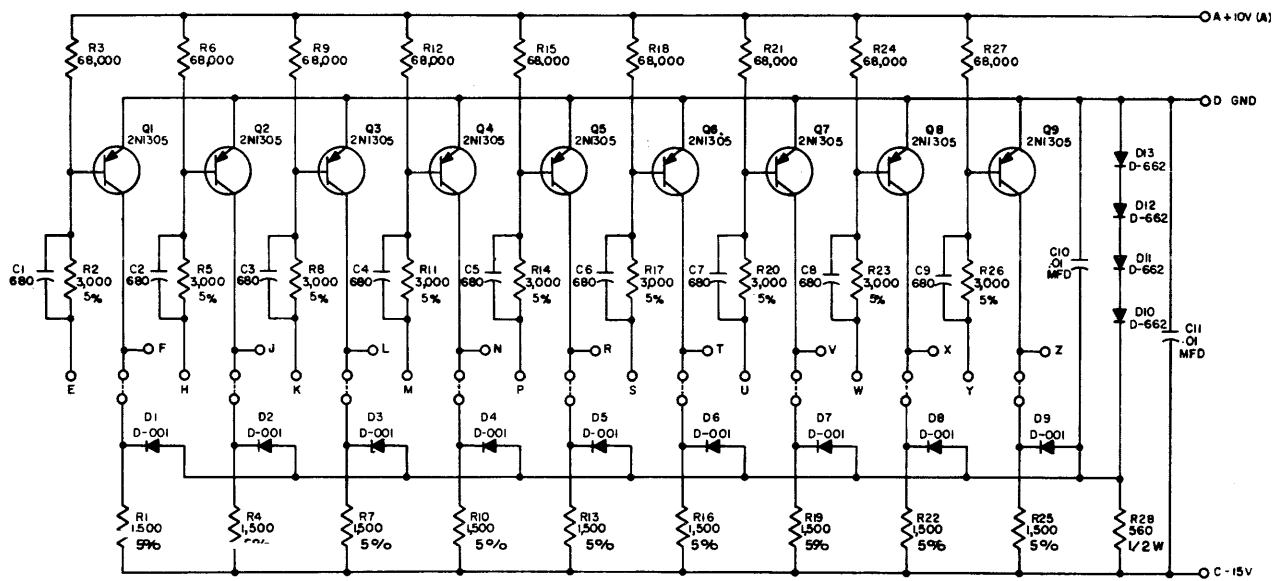
Inverter RS-4102

TRANSISTOR & DIODE CONVERSION CHART

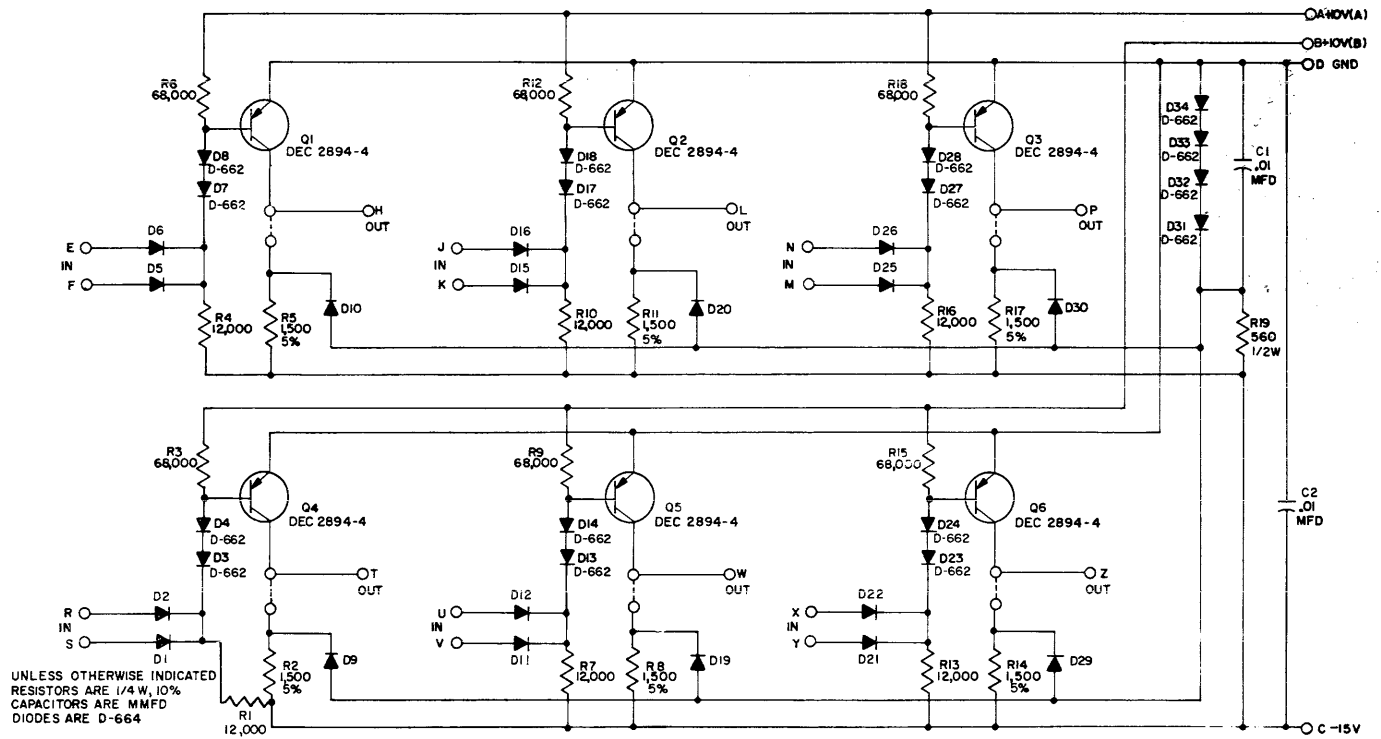| DEC	EIA	DEC	EIA
2N1305	2N1305		
D-001	1N276		
D-662	1N645		

UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4W, 10%
CAPACITORS ARE MMFD

Diode CS-4112

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
MD94	2N2488		
D-003	1N994		
D-662	1N645		

UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W 10%
CAPACITORS ARE MMFD.
DIODES ARE D-003

A2-8

Diode RS-4113

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC 2894-4	DEC 2894		
D-662	1N645		
D-664	1N3606		

UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD
DIODES ARE D-664
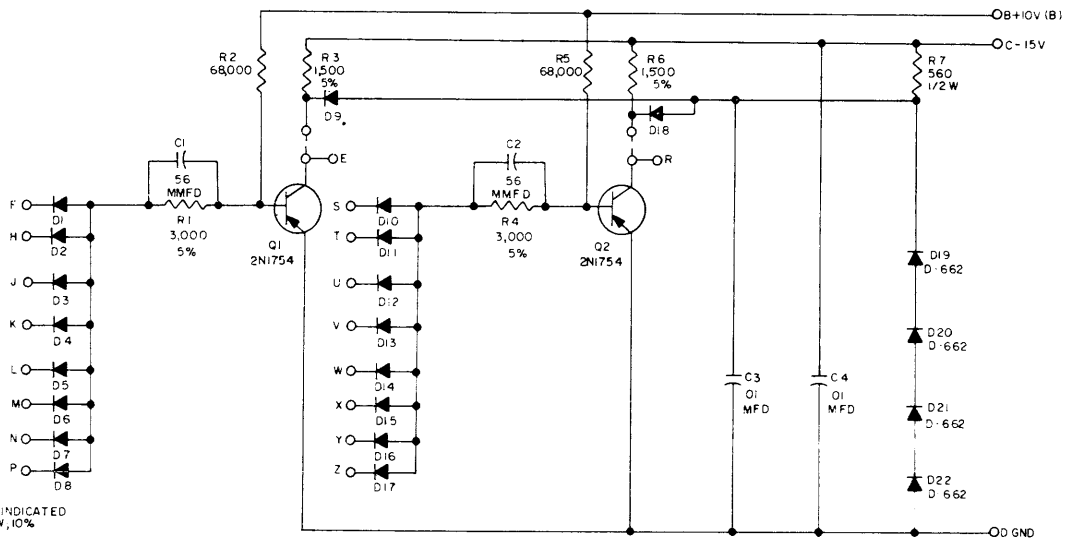
USE THE ETCHED BOARD OF THE 6118

Diode Gate RS-4118
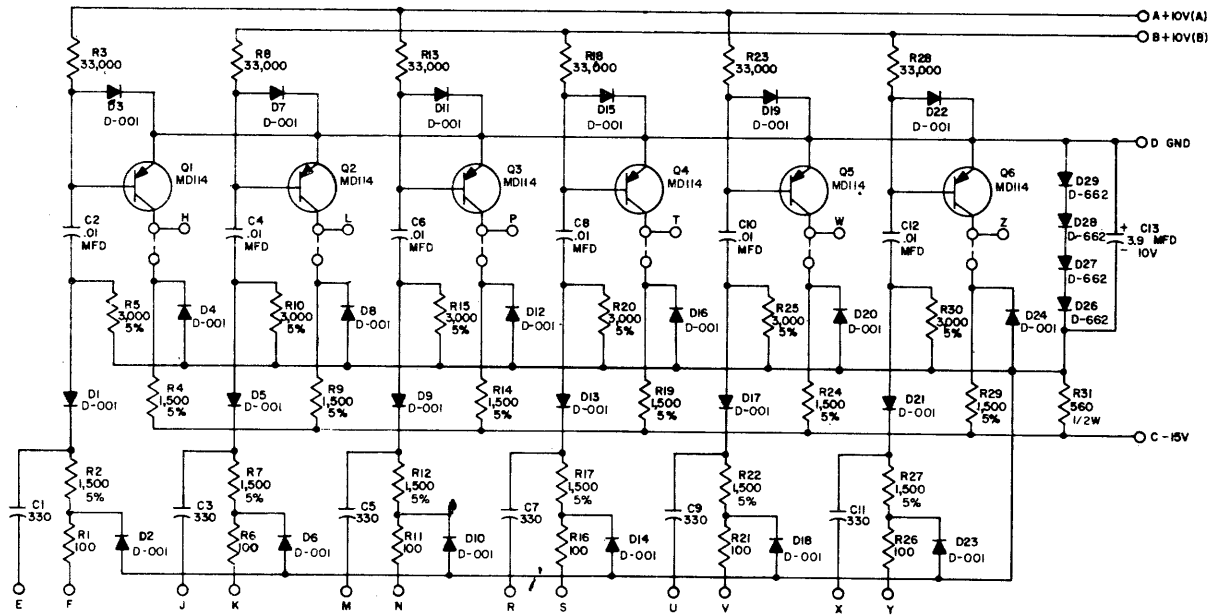
UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4 W, 10%
DIODES ARE D-003

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D-003	1N994		
D-662	1N645		
2N1754	2N1754		

A2-9

Capacitor Diode Inverter RS-4127

UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 10%
CAPACITORS ARE MMFD

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
MD114	2N1499A		
D-001	1N276		
D-662	1N645		

Capacitor Diode Inverter RS-4129
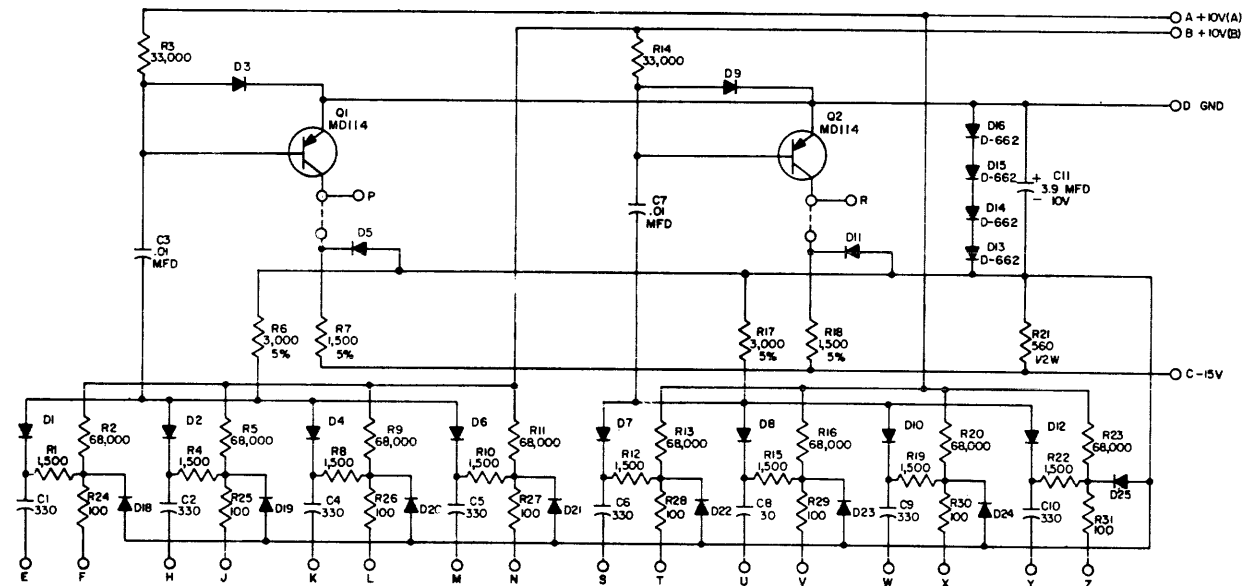
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W ; 10%
CAPACITORS ARE MMFD
DIODES ARE D-001

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
MD114	2N1499A		
D-001	1N276		
D-662	1N645		

A2-10
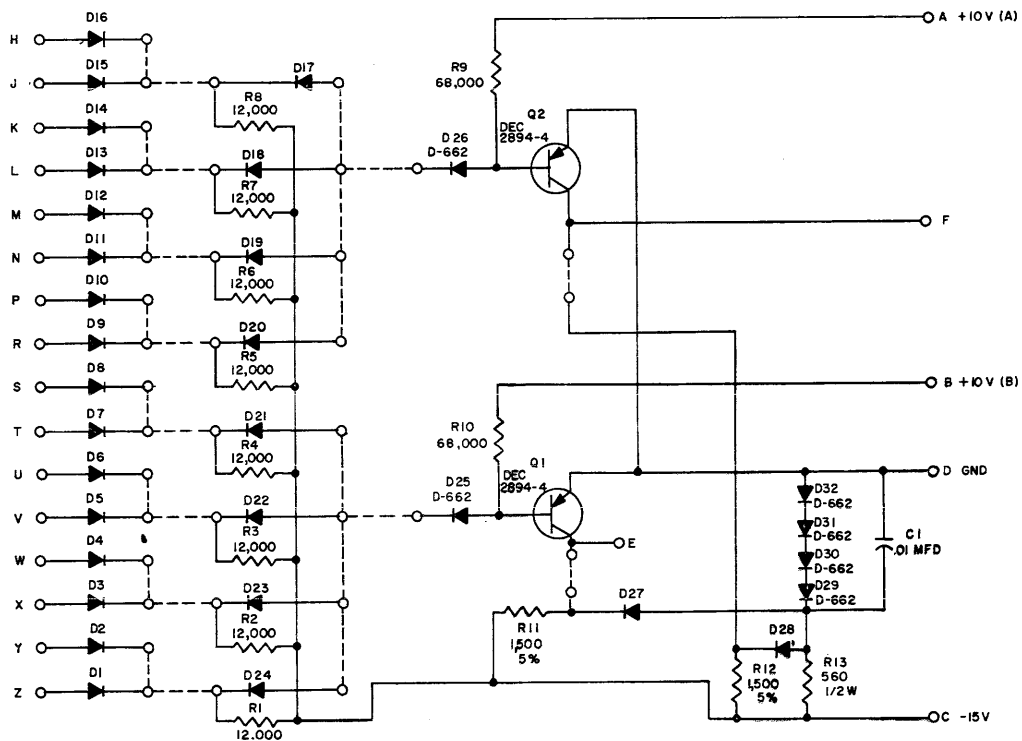
UNLESS OTHERWISE INDICATED
DIODES ARE D-664
RESISTORS ARE 1/4 W, 10%

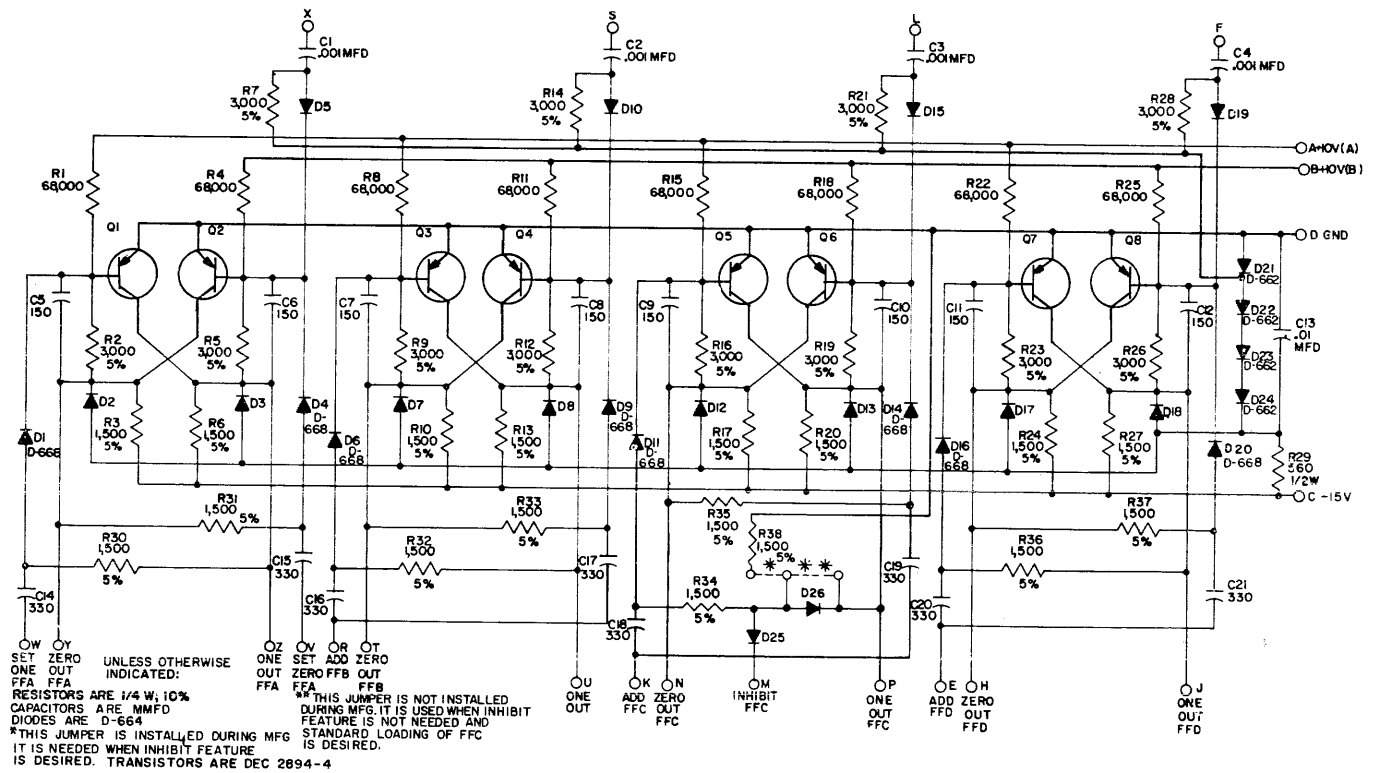| TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC 2894-4	DEC 2894		
D-664	1N3606		
D-662	1N645		

Diode Unit RS-4143
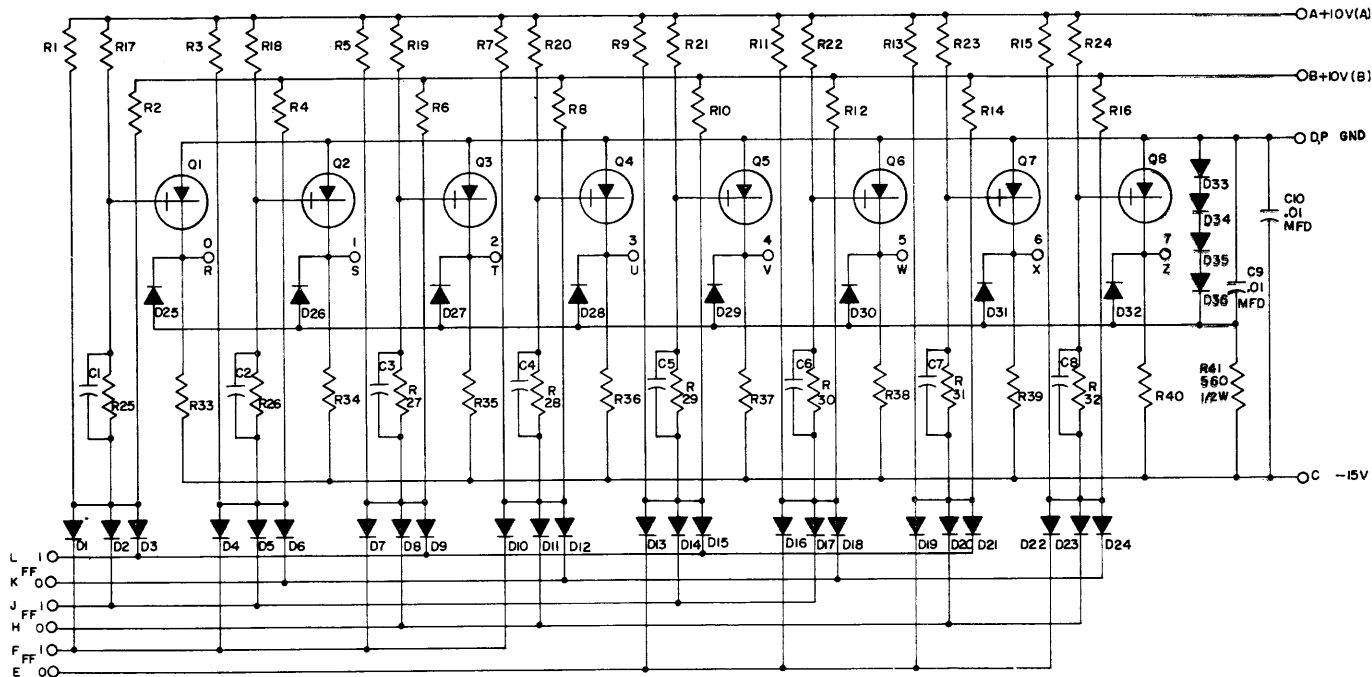
Q1-Q8 ARE 2N1305 : D1-D32 ARE 1N276
D33-D36 ARE 1N645 : R1-R16 ARE 27,000, 1/4W, 10%
R17-R24 ARE 56,000, 1/4W, 10% : R25-R32 ARE 2,200, 1/4W, 5 %
R33-R40 ARE 1,500, 1/4W, 5% : C1-C8 ARE .001 MFD

Binary-to-Octal Decoder RS-4150
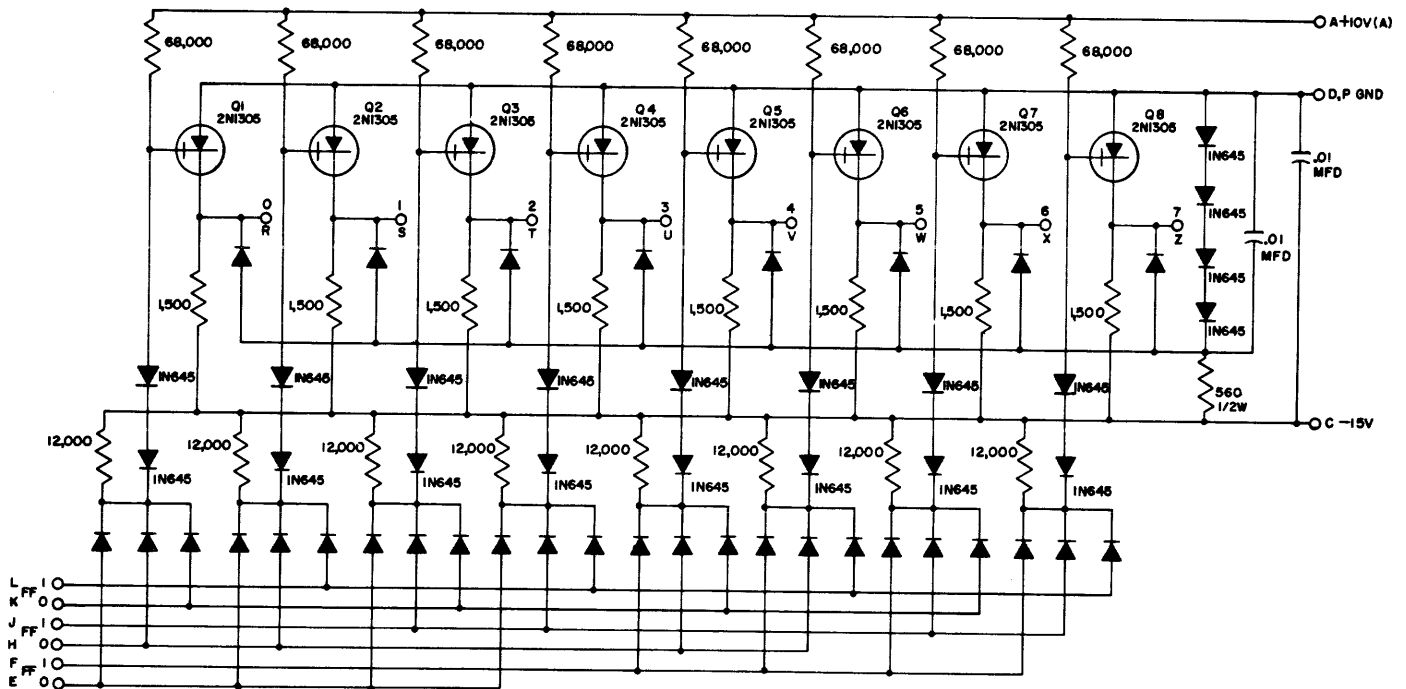
Binary-to-Octal Decoder RS-4151

UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 10%
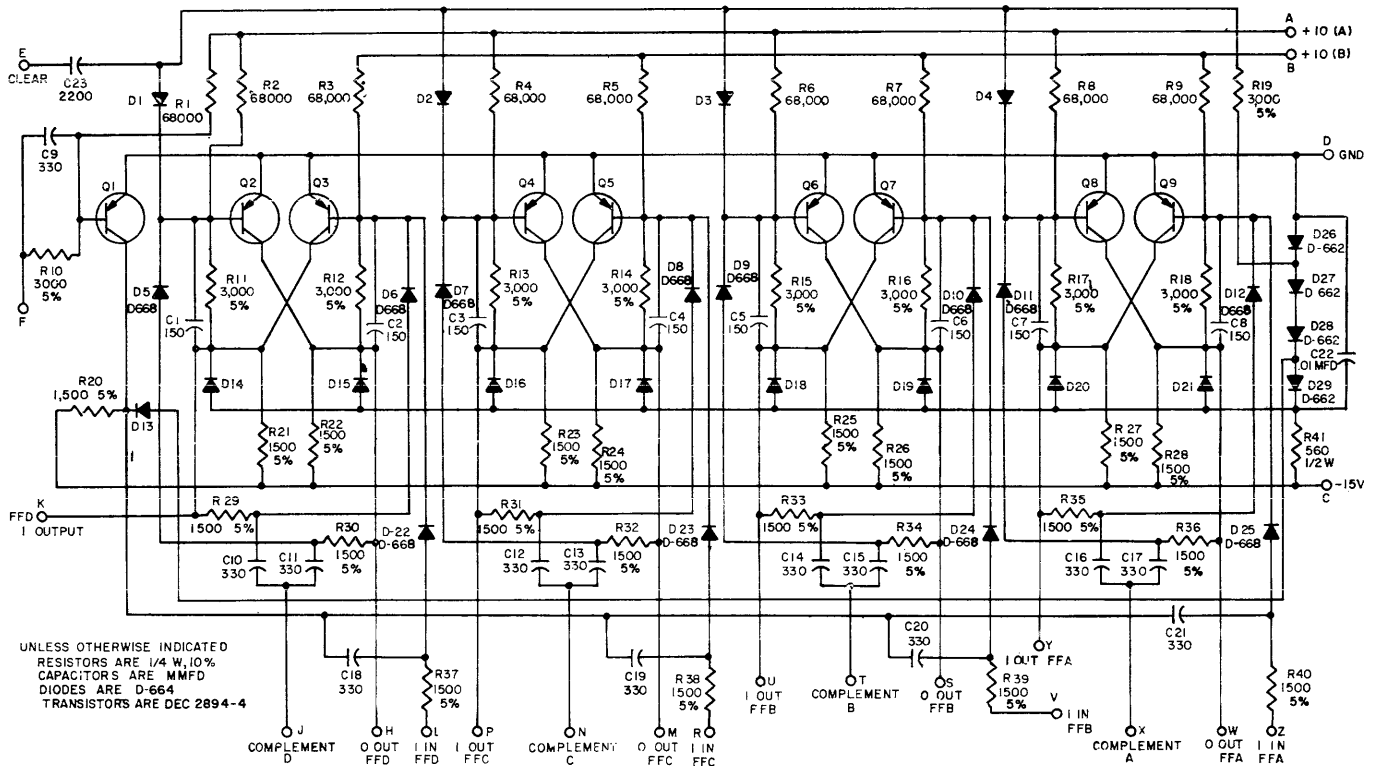DIODES ARE 1N276

UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD
DIODES ARE D-664
*THIS JUMPER IS INSTALLED DURING MFG
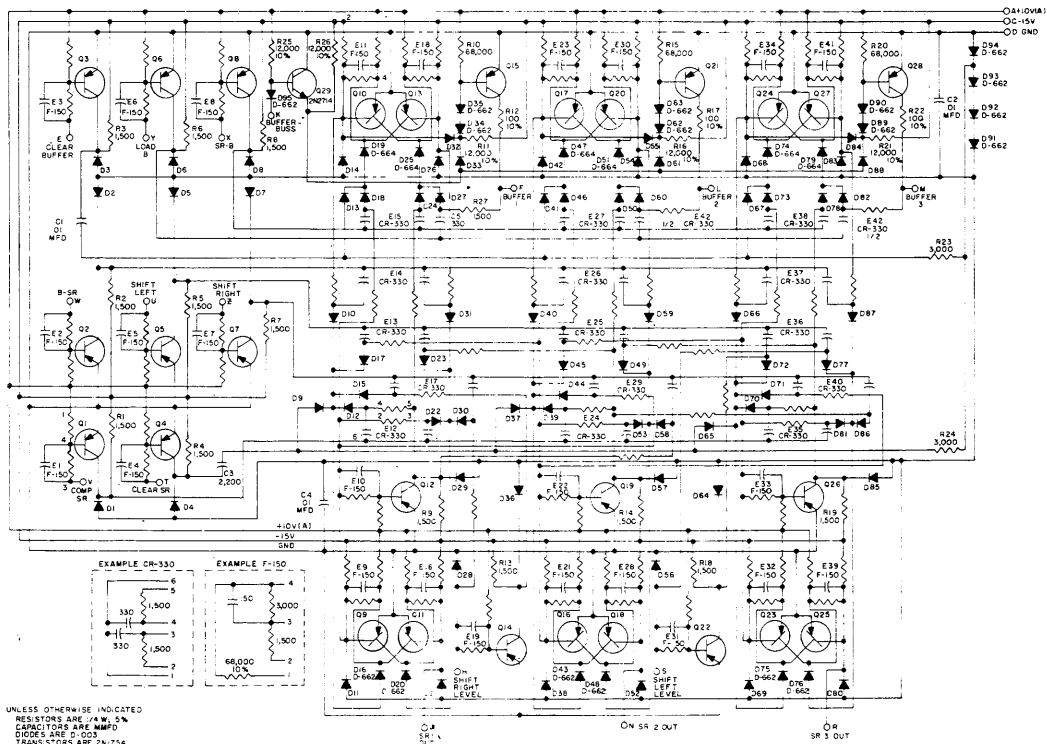IT IS NEEDED WHEN INHIBIT FEATURE
IS DESIRED. TRANSISTORS ARE DEC 2894-4

**THIS JUMPER IS NOT INSTALLED
DURING MFG. IT IS USED WHEN INHIBIT
FEATURE IS NOT NEEDED AND
STANDARD LOADING OF FFC
IS DESIRED.

TRANSISTOR & DIODE CONVERSION CHART				NOTES
DEC	EIA	DEC	EIA	***(TWO) 1N3606 IN SERIES
DEC 2894-4	DEC 2894			
D-668	D-668*			
D-662	1N645			
D-664	1N3606			

Four-Bit Counter RS-4215

A2-12

Four-Bit Counter RS-4217

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC 2894-4	DEC 2894		
D-668	D-668*		
D-662	IN645		
D-664	IN3606		

NOTES
*(TWO) IN3606 IN SERIES

UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD
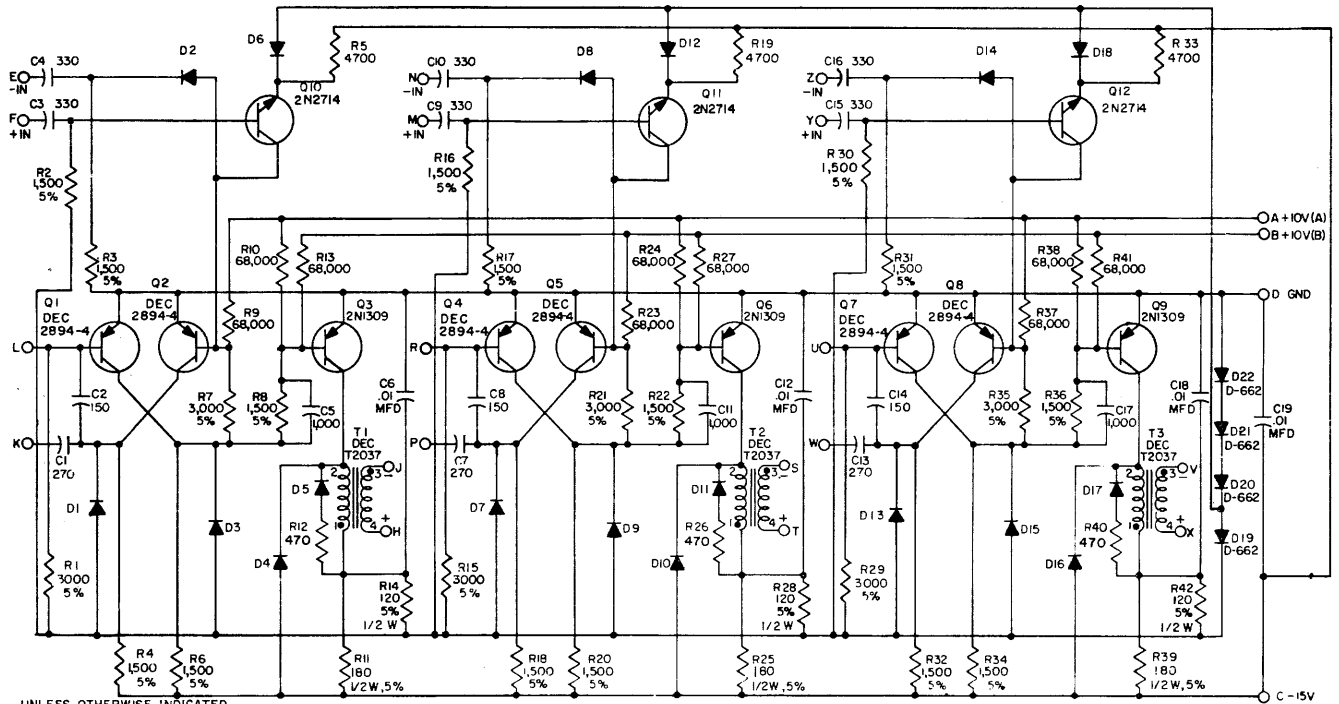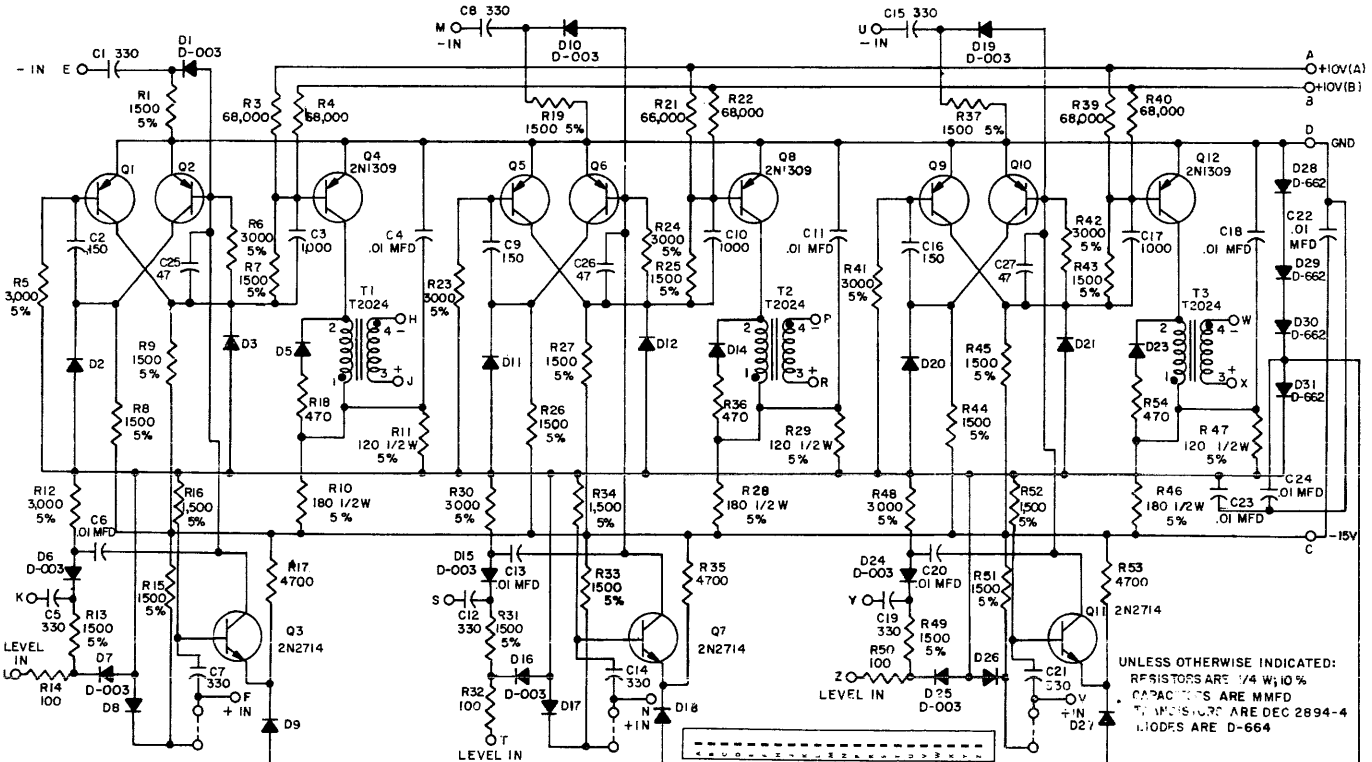DIODES ARE D-664
TRANSISTORS ARE DEC 2894-4

Three-Bit Shift Register with Buffer Register RS-4230

UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4 W, 5%
CAPACITORS ARE MMFD
DIODES ARE D-003
TRANSISTORS ARE 2N754

A2-13

Pulse Amplifier RS-4604

UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD
DIODES ARE D-664

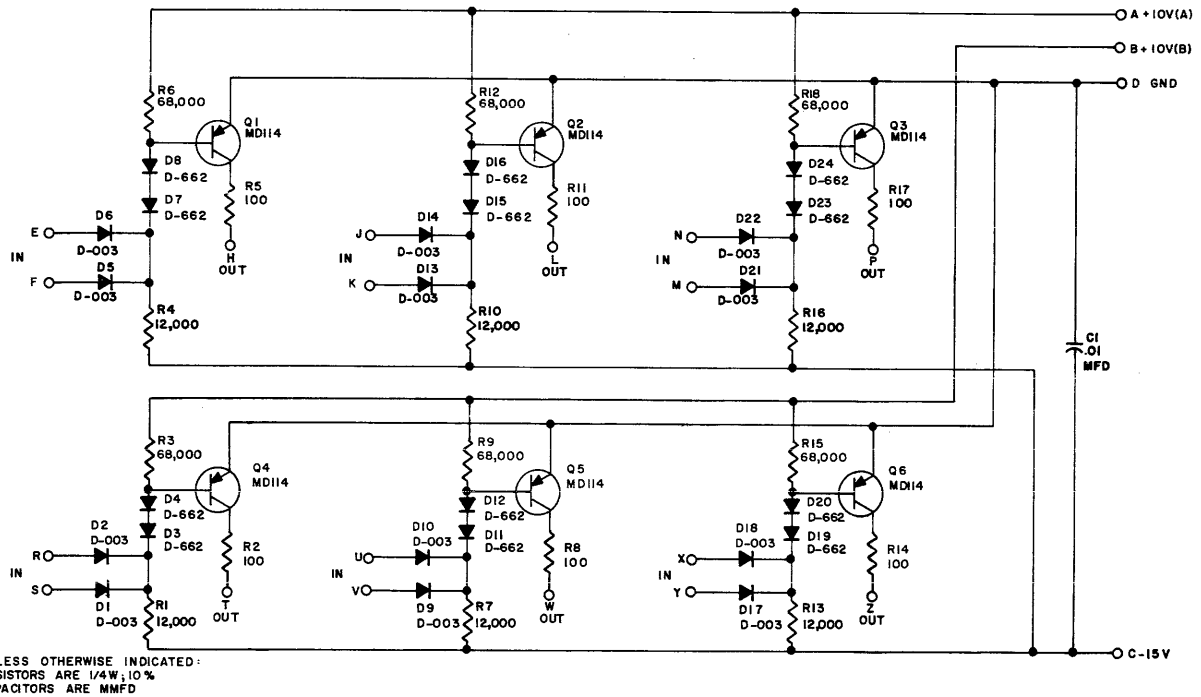| TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
2N2714	2N2714		
DEC 2894-4	DEC 2894		
2N1309	2N1309		
D-664	1N3606		
D-662	1N645		

Pulse Amplifier RS-4606

UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W; 10%
CAPACITORS ARE MMFD
TRANSISTORS ARE DEC 2894-4
DIODES ARE D-664

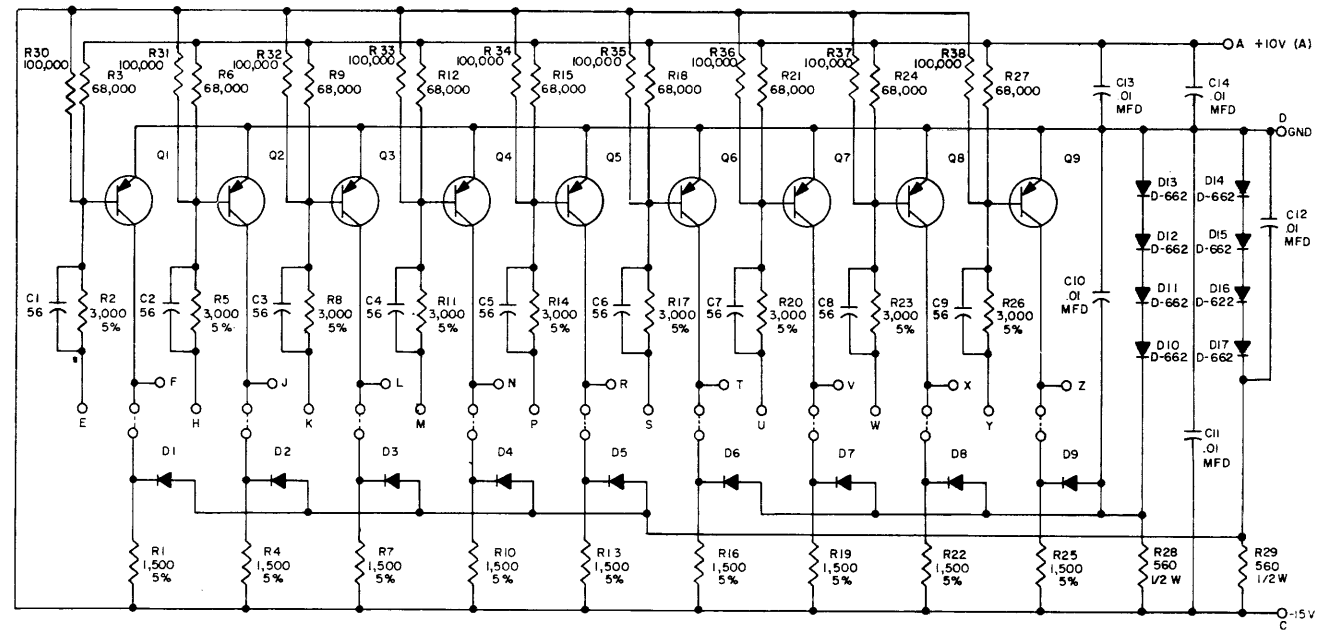| TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC 2894-4	DEC 2894	D-003	1N994
2N2714	2N2714		
2N1309	2N1309		
D-664	1N3606		
D-662	1N645		

A2-14

I/O Bus Driver RS-4657

UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD

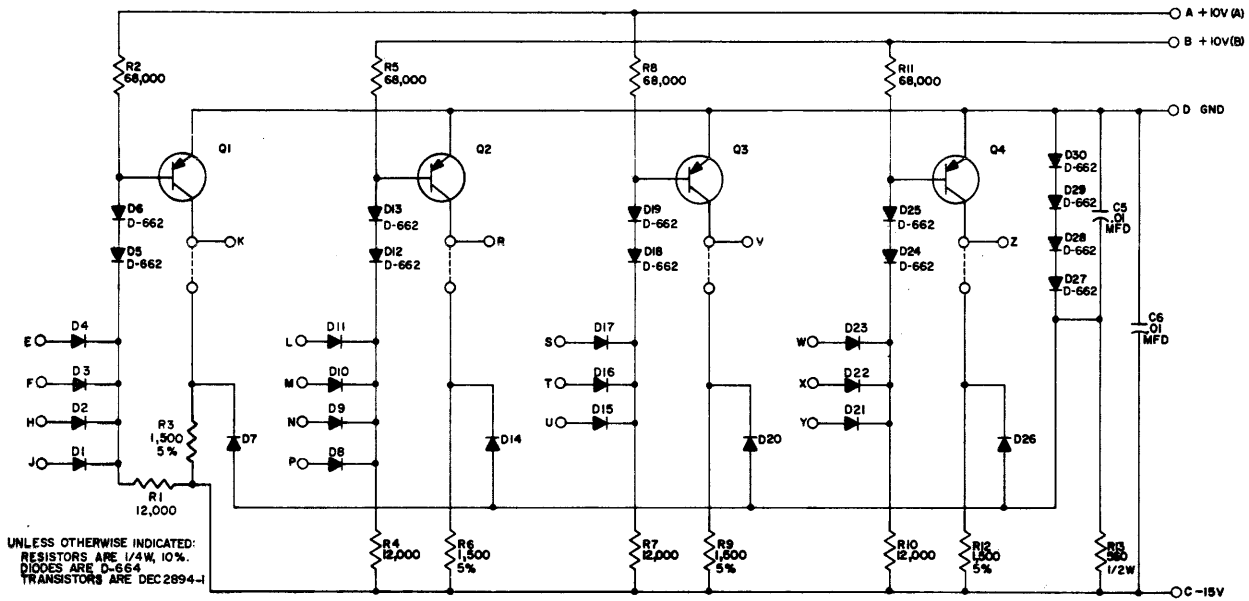| TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
MD114	2N1499A		
D-003	1N994		
D-662	1N645		

Inverter RS-6102

UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD
TRANSISTORS ARE DEC 2894-1
DIODES ARE D-664

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC 2894-1	2N2894		
D-664	1N914		
D-662	1N645		

A2-15

Diode RS-6115

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC 2894-1	DEC 2894		
D-664	IN914		
D-662	IN645		

UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 10%.
DIODES ARE D-664
TRANSISTORS ARE DEC 2894-1

Diode RS-6117

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC 2894-1	DEC 2894		
D-664	IN914		
D-662	IN645		

UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4W, 10%
DIODES ARE D-664
TRANSISTORS ARE DEC 2894-1

A2-16

Bus Driver RS-6684
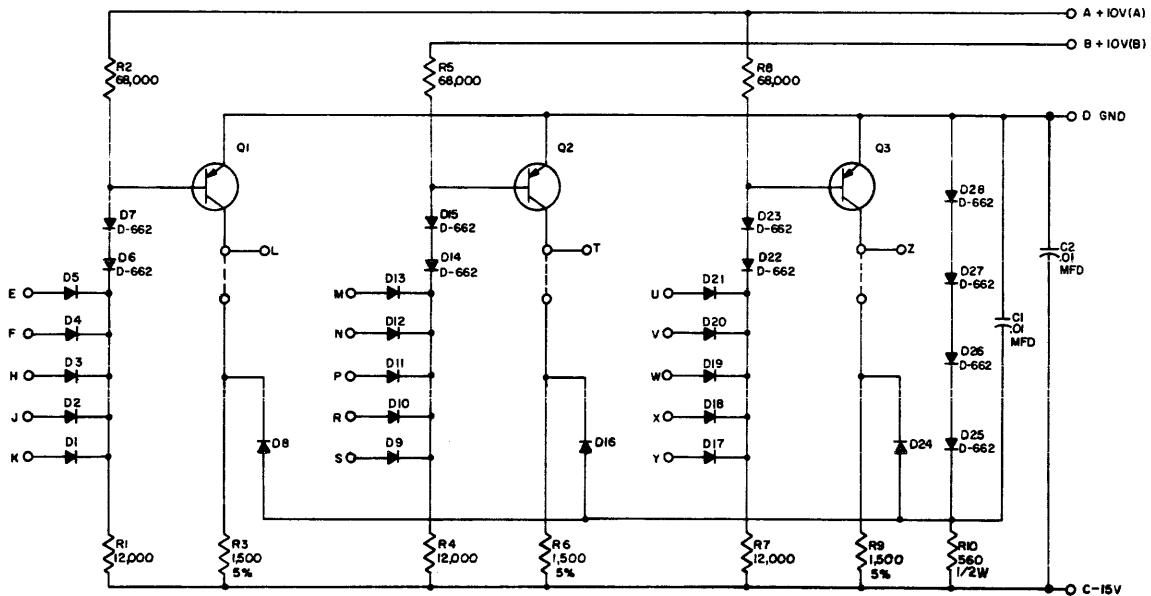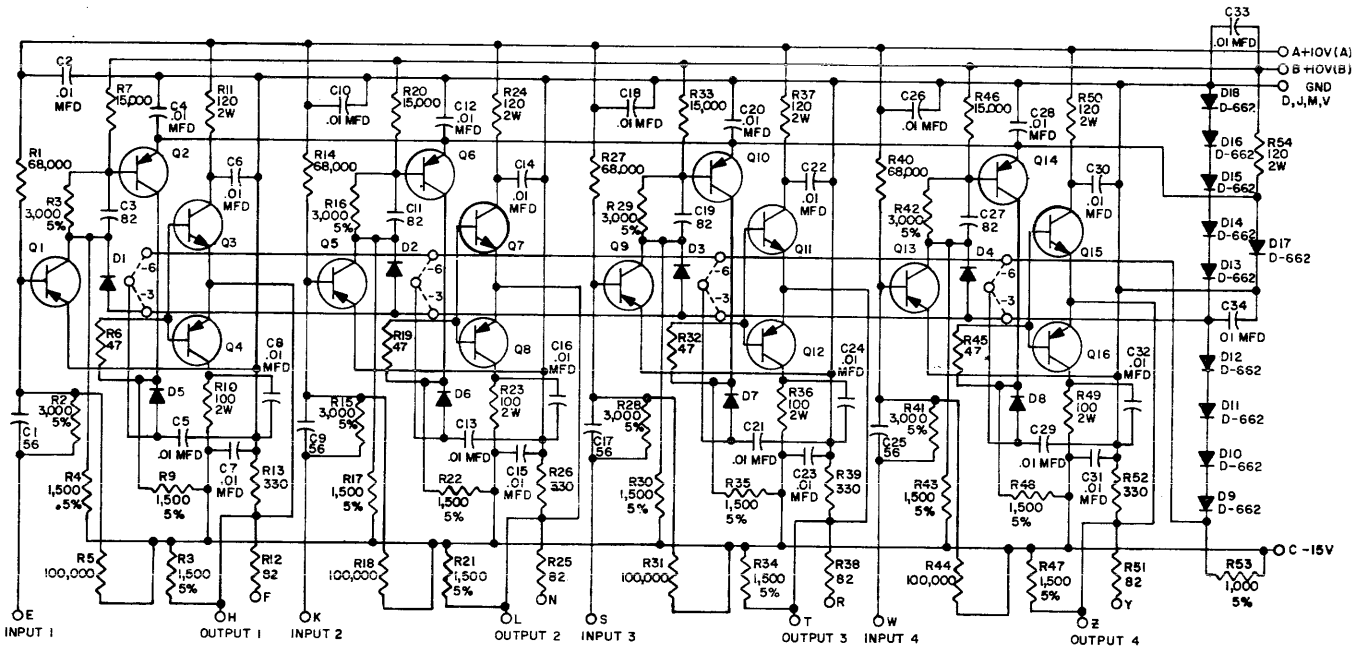
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD
DIODES ARE D-664
Q3,Q7,Q11,& Q15 ARE 2N3009
Q4,Q8,Q12,& Q16 ARE 2N2904
ALL OTHER TRANSISTORS ARE DEC2894-1

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC2894-1	DEC2894		
2N2904	2N2904		
2N3009	2N3C09		
D-664	1N3606		
D-662	1N645		

Data Buffer-Data Accumulator (sheet 1)
BS-D-136-0-DAB1

Data Buffer-Data Accumulator (sheet 1)
BS-D-136-0-DAB1

Data Buffer–Data Accumulator (sheet 2)
BS-D-136-0-DAB2
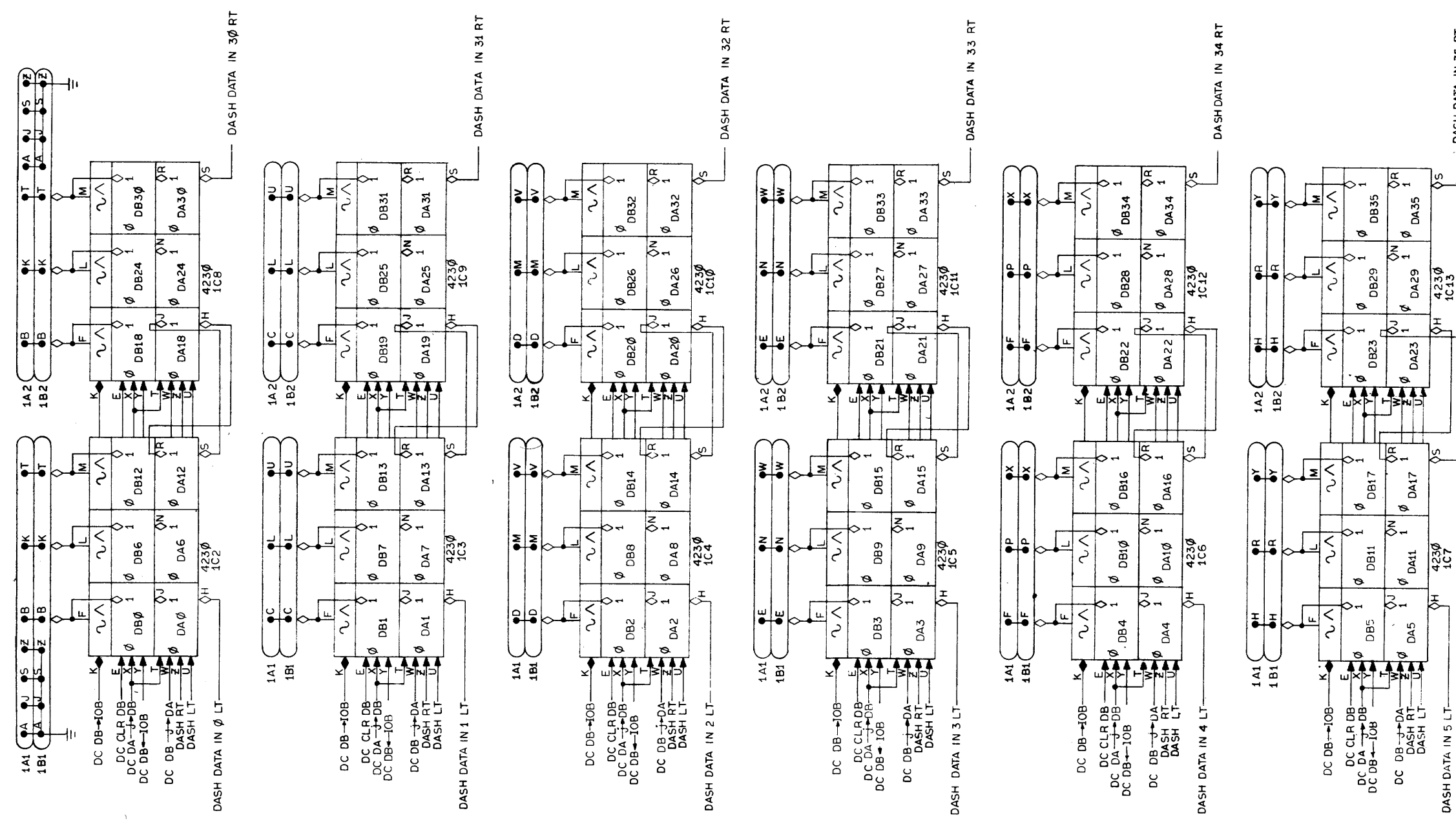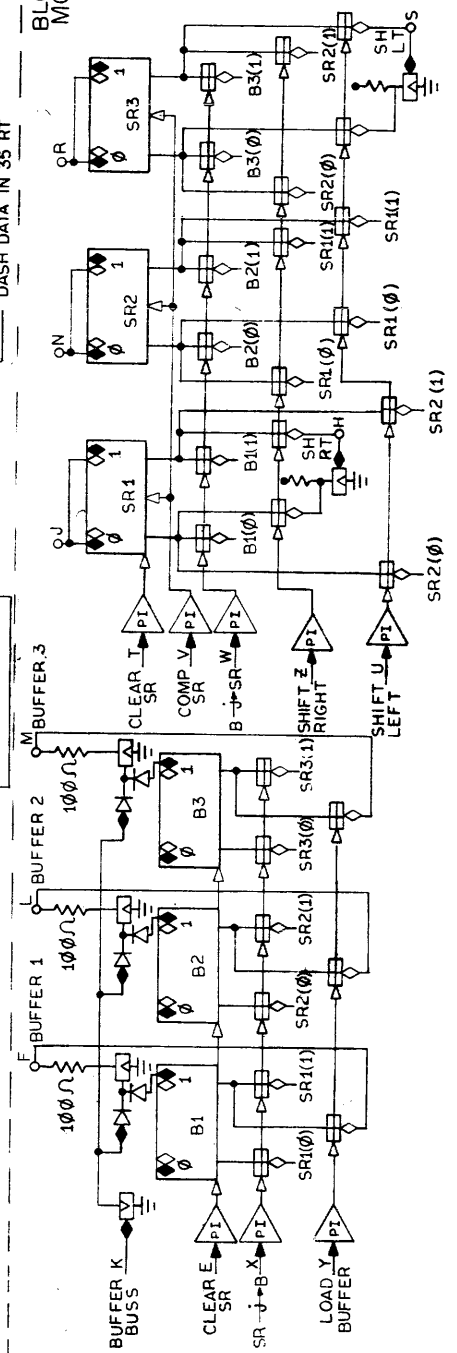
Data Buffer–Data Accumulator (sheet 2)
BS-D-136-0-DAB2
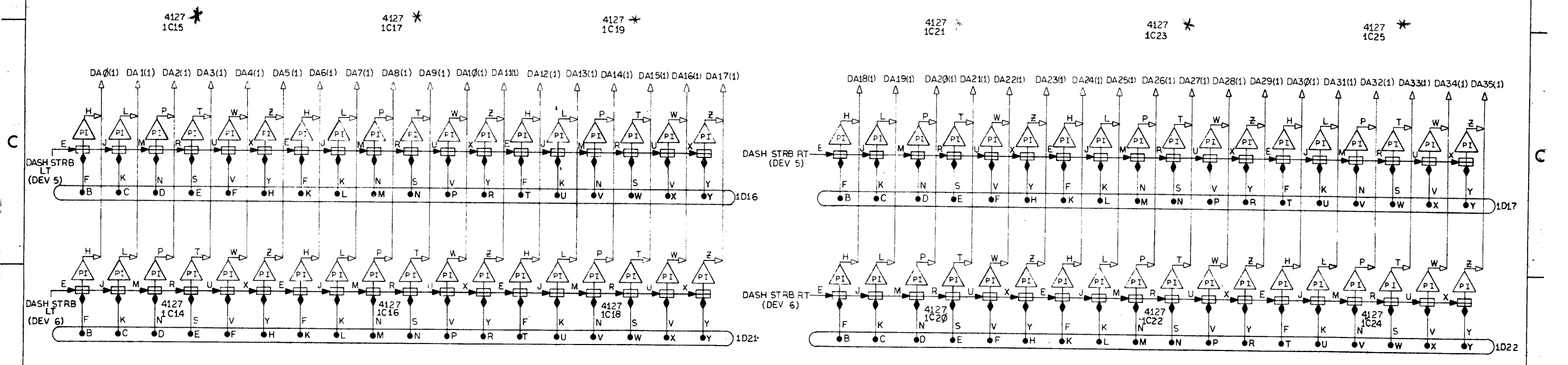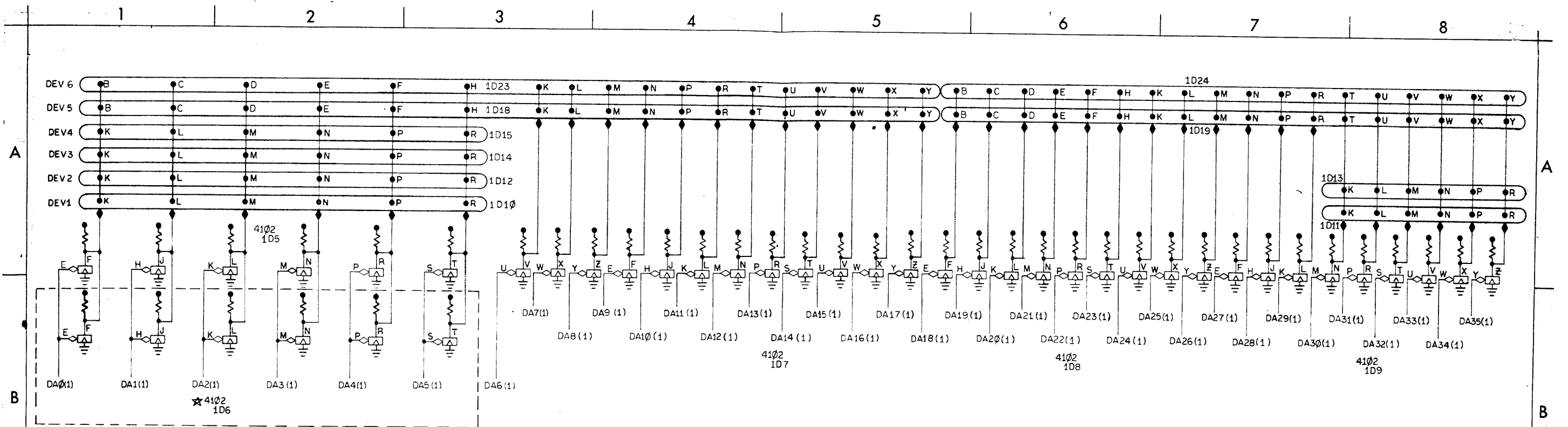
NOTES
1. ☆ PKG USED WITH FOUR OR MORE DEVICES CONNECTED
2. 1D10 THRU 1D25 GROUNDS ARE A,J,S, AND Z.
3. ✳ PKG must be connected to Gnd when connected to a die filter
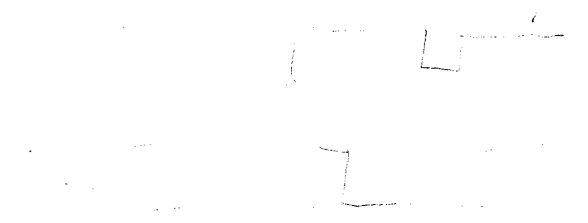
Data Accumulator Shift BS-D-136-0-DASH

A2-23
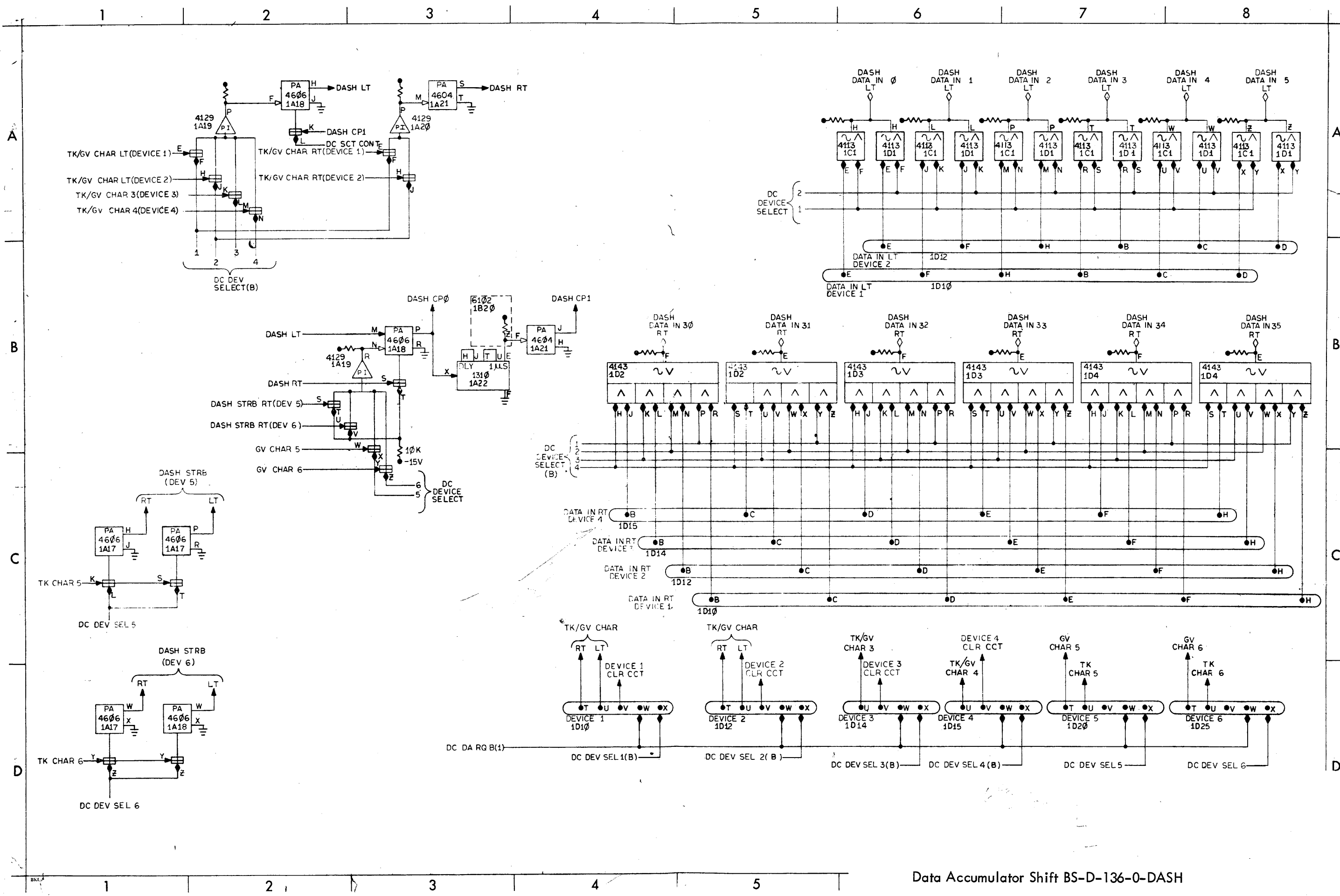
Data Accumulator Shift BS-D-136-0-DASH

Data Control (sheet 1) BS-D-136-0-DC1

A2-25

Data Control (sheet 1) BS-D-136-0-DC1
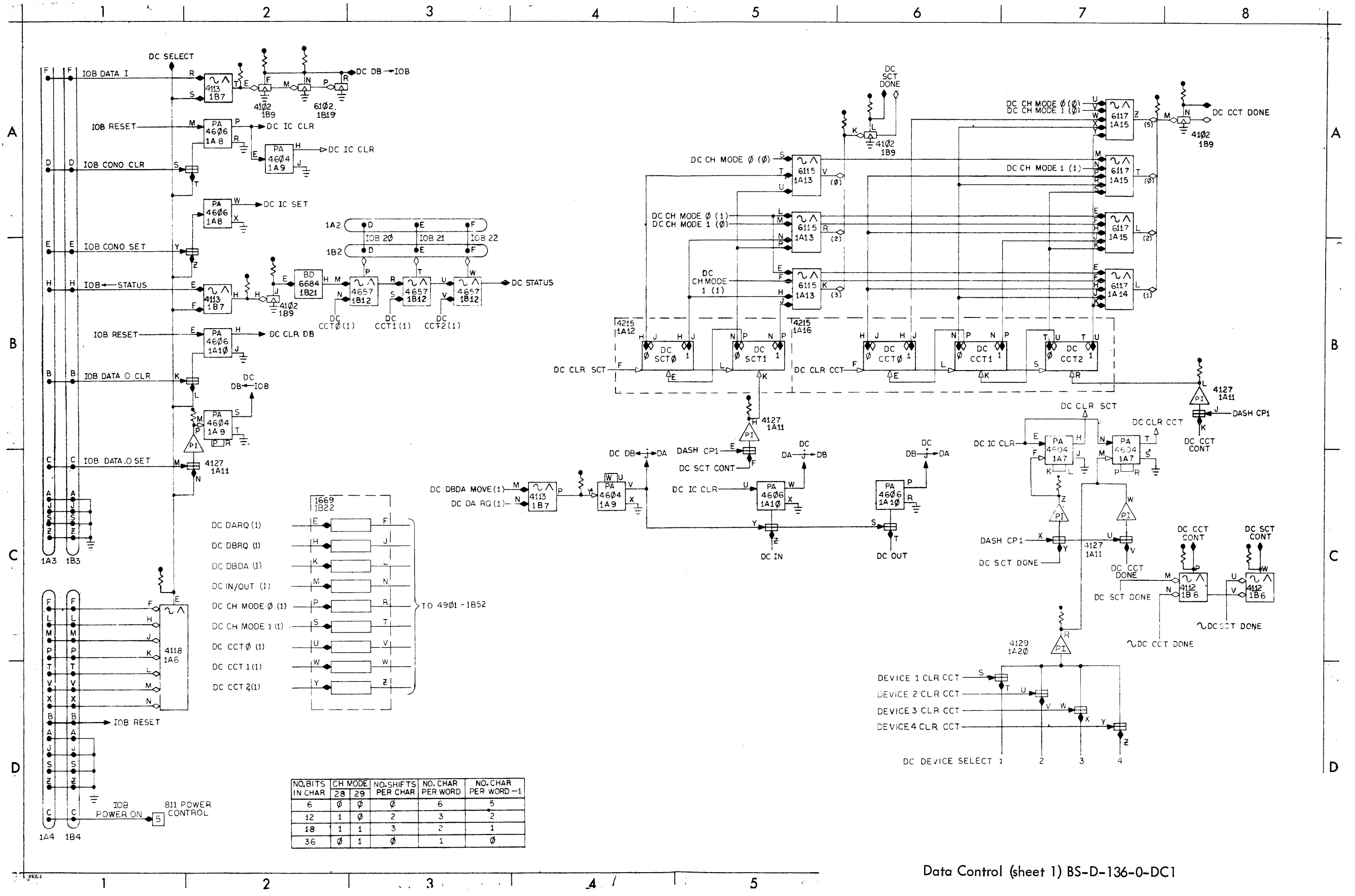
NO. BITS IN CHAR	CH MODE 28	CH MODE 29	NO. SHIFTS PER CHAR	NO. CHAR PER WORD	NO. CHAR PER WORD -1
6	Ø	Ø	Ø	6	5
12	1	Ø	2	3	2
18	1	1	3	2	1
36	Ø	1	Ø	1	Ø

Data Control (sheet 2) BS-D-136-0-DC2

Methode Plug Connections at
Processor Interface CD-D-166-0-IOMB

I.O. BUS

PIN	I.O. CABLE #1	I.O. CABLE #2	I.O. CABLE #3	I.O. CABLE #4
A	GND	GND	GND	GND
B	IOB Ø (1) —∘	IOB 18 (1) —∘	POWER RESET →	DATAO CLEAR →
C	IOB 1 (1) —∘	IOB 19 (1) —∘	POWER ON −15V	DATAO SET →
D	IOB 2 (1) —∘	IOB 20(1) —∘		CON O CLEAR →
E	IOB 3 (1) —∘	IOB 21(1) —∘		CON O SET →
F	IOB 4 (1) —∘	IOB 22(1) —∘	IOS 3 (Ø) —∘	IOB ← DATA I →
H	IOB 5 (1) —∘	IOB 23(1) —∘	IOS 3 (1) —∘	IOB ← STATUS →
J	GND	GND	GND	GND
K	IOB 6 (1) —∘	IOB 24(1) —∘	IOS 4 (Ø) —∘	
L	IOB 7 (1) —∘	IOB 25(1) —∘	IOS 4 (1) —∘	
M	IOB 8 (1) —∘	IOB 26(1) —∘	IOS 5 (Ø) —∘	
N	IOB 9 (1) —∘	IOB 27(1) —∘	IOS 5 (1) —∘	
P	IOB 10(1) —∘	IOB 28(1) —∘	IOS 6 (Ø) —∘	
R	IOB 11(1) —∘	IOB 29(1) —∘	IOS 6 (1) —∘	PI REQ 1 —∘
S	GND	GND	GND	GND
T	IOB 12(1) —∘	IOB 30(1) —∘	IOS 7 (Ø) —∘	PI REQ 2 —∘
U	IOB 13(1) —∘	IOB 31(1) —∘	IOS 7 (1) —∘	PI REQ 3 —∘
V	IOB 14(1) —∘	IOB 32(1) —∘	IOS 8 (Ø) —∘	PI REQ 4 —∘
W	IOB 15(1) —∘	IOB 33(1) —∘	IOS 8 (1) —∘	PI REQ 5 —∘
X	IOB 16(1) —∘	IOB 34(1) —∘	IOS 9 (Ø) —∘	PI REQ 6 —∘
Y	IOB 17(1) —∘	IOB 35(1) —∘	IOS 9 (1) —∘	PI REQ 7 —∘
Z	GND	GND	GND	GND
	(SOURCE 3L6)	(SOURCE 3L7)	(SOURCE 2L13)	(SOURCE 2N25)
PLUG NO.	1A1 — 1B1	1A2 — 1B2	1A4 — 1B4	1A3 — 1B3

1	2	3	4	4	3	2	1
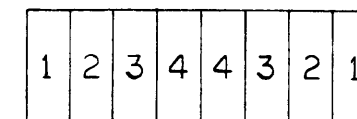
Methode Plug Connections at
Processor Interface CD-D-166-0-IOMB

Flow Diagram FD-D-136-0-FD1

OUT

CONO
CLR
→ CLR IC REG

1μS

CONO
SET
SET { DA RQ,DB RQ
OUT,MODE
DEV SEL

DATAO
CLR
CLR { DB
DB RQ

1μS

DATAO
SET
→ IOB → DB

1μS

→ DBDA MOVE ← 1   A

FIRST PASS ONLY
AFTER CONO(OUT) ------→

DBDA MOVE Ø → 1   DA RQ Ø → 1
∧ DA RQ (1)   ∧ DB DA MOVE(1)

DB↞j→DA
{ DB DA MOVE ← Ø
DB RQ ← 1

IN   1μS   OUT

DA↞j→DB   DA↞j→DB
(GO TO DATAI)   (GO TO DATAO)

DA RQ ← Ø
GO TO B

IN

CONO
CLR
→ CLR IC REG

1μS

CONO
SET
SET { DBDA MOVE
IN,MODE
DEV SEL

GO TO B

DATAI
(Ø → 1)   DB RQ ← Ø
DB → IOB
(1 → Ø)   DBDA MOVE → 1

GO TO B

B

DA RQ(Ø)
∧DEV SEL   EXTERNAL
DEVICE

DEVICE
TK/GV CHAR

TK/GV CHAR
∧DEV SEL   TK/GV CHAR
12,3,4   ∧DEV 5,6

DASH
← SHIFT DA

CPØ

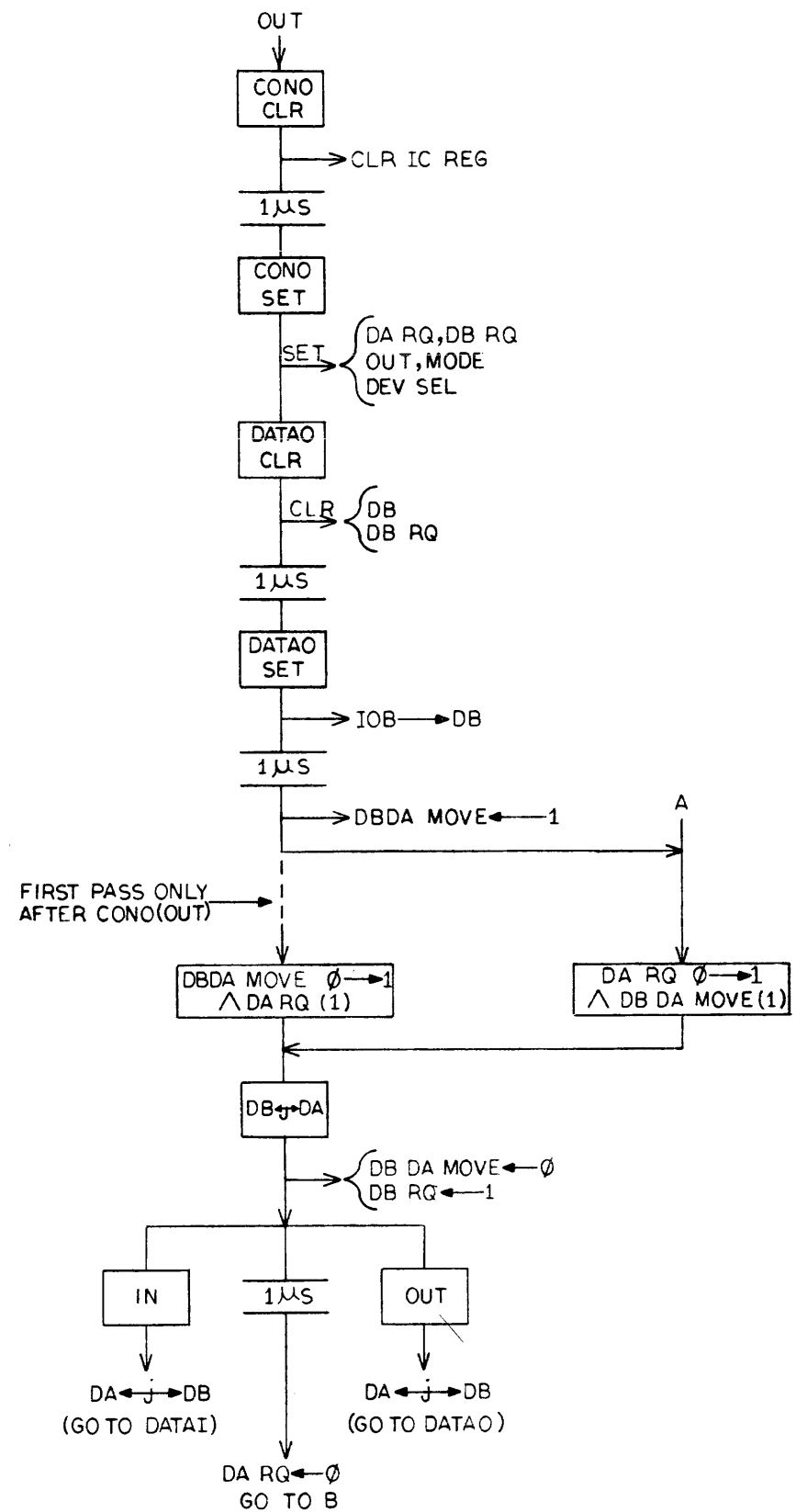1μS   DA RQ (1)
→ DATA CLBD ← 1

CP1
CCT DONE   DA RQ ← 1
CCT ← Ø } GO TO A

SCT DONE ∧ ᘺ CCT DONE

ᘺ SCT DONE
∧
ᘺ CCT DONE   IDX CCT
O ← SCT

→ IDX SCT

Flow Diagram FD-D-136-0-FD1

External Device Connections
ID-D-136-0-EDC

* PIN	DEVICE 1 JLT 551		DEVICE 2		DEVICE 3 MT 516	DEVICE 4	DEVICE 5 36 OR LESS BIT DEVICE					DEVICE 6 36 OR LESS BIT DEVICE				
	1E10	1E11	1E12	1E13	1E14	1E15	1E16	1E17	1E18	1E19	1E20	1E21	1E22	1E23	1E24	1E25
A	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
B	30 IN		30 IN		30 IN	30 IN	0 IN	18 IN	0 OUT	18 OUT		0 IN	18 IN	0 OUT	18 OUT	
C	31 IN		31 IN		31 IN	31 IN	1 IN	19 IN	1 OUT	19 OUT		1 IN	19 IN	1 OUT	19 OUT	
D	32 IN	SPARE	32 IN	SPARE	32 IN	32 IN	2 IN	20 IN	2 OUT	20 OUT	SPARE	2 IN	20 IN	2 OUT	20 OUT	SPARE
E	33 IN		33 IN		33 IN	33 IN	3 IN	21 IN	3 OUT	21 OUT		3 IN	21 IN	3 OUT	21 OUT	
F	34 IN		34 IN		34 IN	34 IN	4 IN	22 IN	4 OUT	22 OUT		4 IN	22 IN	4 OUT	22 OUT	
H	35 IN		35 IN		35 IN	35 IN	5 IN	23 IN	5 OUT	23 OUT		5 IN	23 IN	5 OUT	23 OUT	
J	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
K	0 OUT	30 OUT	0 OUT	30 OUT	0 OUT	0 OUT	6 IN	24 IN	6 OUT	24 OUT		6 IN	24 IN	6 OUT	24 OUT	
L	1 OUT	31 OUT	1 OUT	31 OUT	1 OUT	1 OUT	7 IN	25 IN	7 OUT	25 OUT		7 IN	25 IN	7 OUT	25 OUT	
M	2 OUT	32 OUT	2 OUT	32 OUT	2 OUT	2 OUT	8 IN	26 IN	8 OUT	26 OUT	SPARE	8 IN	26 IN	8 OUT	26 OUT	SPARE
N	3 OUT	33 OUT	3 OUT	33 OUT	3 OUT	3 OUT	9 IN	27 IN	9 OUT	27 OUT		9 IN	27 IN	9 OUT	27 OUT	
P	4 OUT	34 OUT	4 OUT	34 OUT	4 OUT	4 OUT	10 IN	28 IN	10 OUT	28 OUT		10 IN	28 IN	10 OUT	28 OUT	
R	5 OUT	35 OUT	5 OUT	35 OUT	5 OUT	5 OUT	11 IN	29 IN	11 OUT	29 OUT		11 IN	29 IN	11 OUT	29 OUT	
S	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
T	TK/GV RT		TK/GV RT		SPARE	SPARE	12 IN	30 IN	12 OUT	30 OUT	GV/CHAR	12 IN	30 IN	12 OUT	30 OUT	GV/CHAR
U	TK/GV LT		TK/GV LT		TK/GV 3	TK/GV 4	13 IN	31 IN	13 OUT	31 OUT	TK/CHAR	13 IN	31 IN	13 OUT	31 OUT	TK/CHAR
V	CLR CCT 1		CLR CCT 2		CLR CCT 3	CLR CCT 4	14 IN	32 IN	14 OUT	32 OUT		14 IN	32 IN	14 OUT	32 OUT	
W	DARQ(1)-	SPARE	DARQ(1)-	SPARE	DARQ(1)-	DARQ(1)-	15 IN	33 IN	15 OUT	33 OUT	DARQ(1)-	15 IN	33 IN	15 OUT	33 OUT	DARQ(1)-
X	SEL 1 -		SEL 2 -		SEL 3 -	SEL 4-	16 IN	34 IN	16 OUT	34 OUT	SEL 5-	16 IN	34 IN	16 OUT	34 OUT	SEL 6
Y	SPARE		SPARE		SPARE	SPARE	17 IN	35 IN	17 OUT	35 OUT	SPARE	17 IN	35 IN	17 OUT	35 OUT	SPARE
Z	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND

* NOTE
ALL CONNECTORS ARE 22 PIN METHODE PLUGS (MALE)
AND ALL MATING PLUGS SHOULD BE SAME.
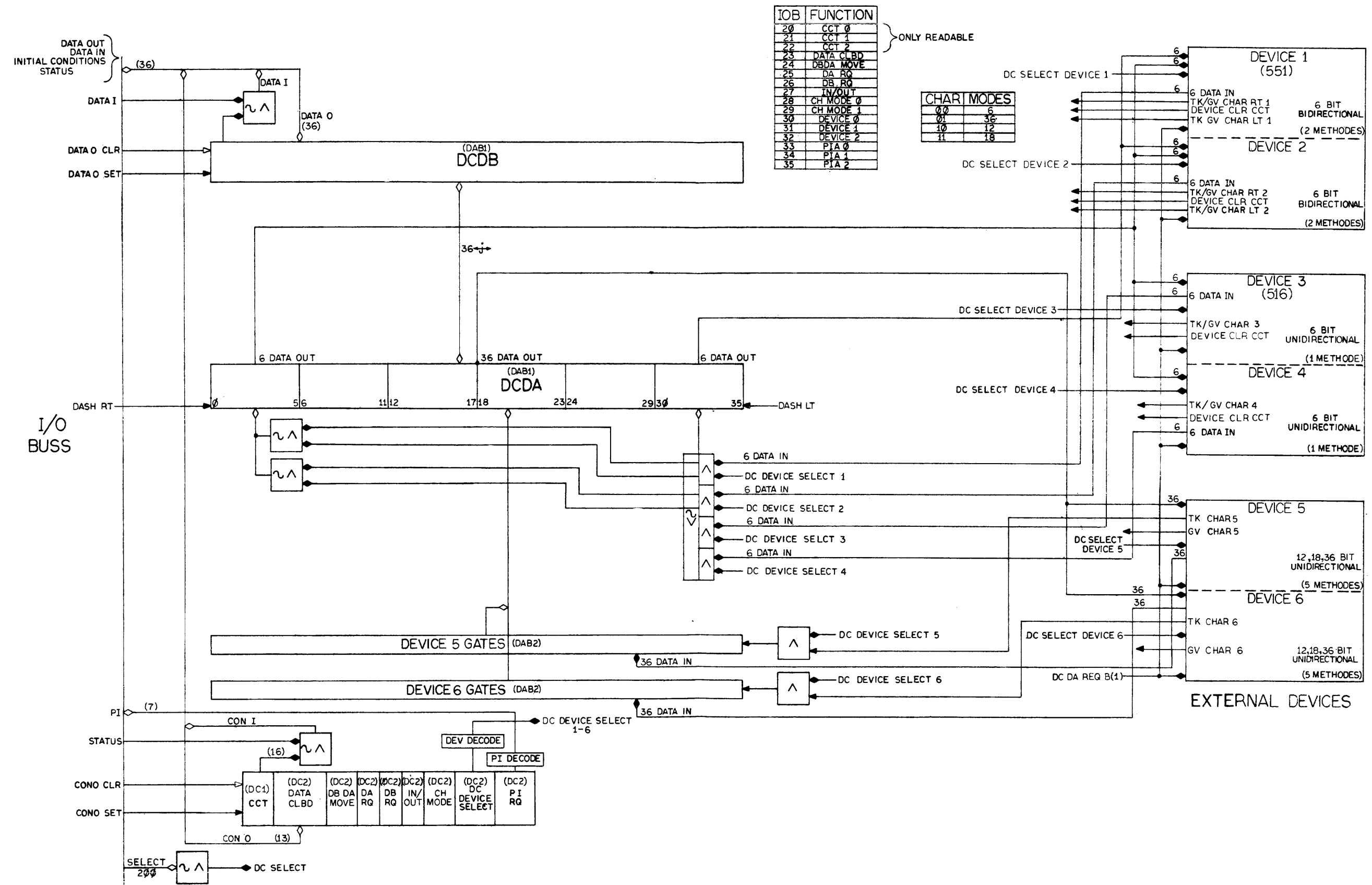
External Device Connections
ID-D-136-0-EDC

Data Control System Diagram
SD-D-136-0-DCSD
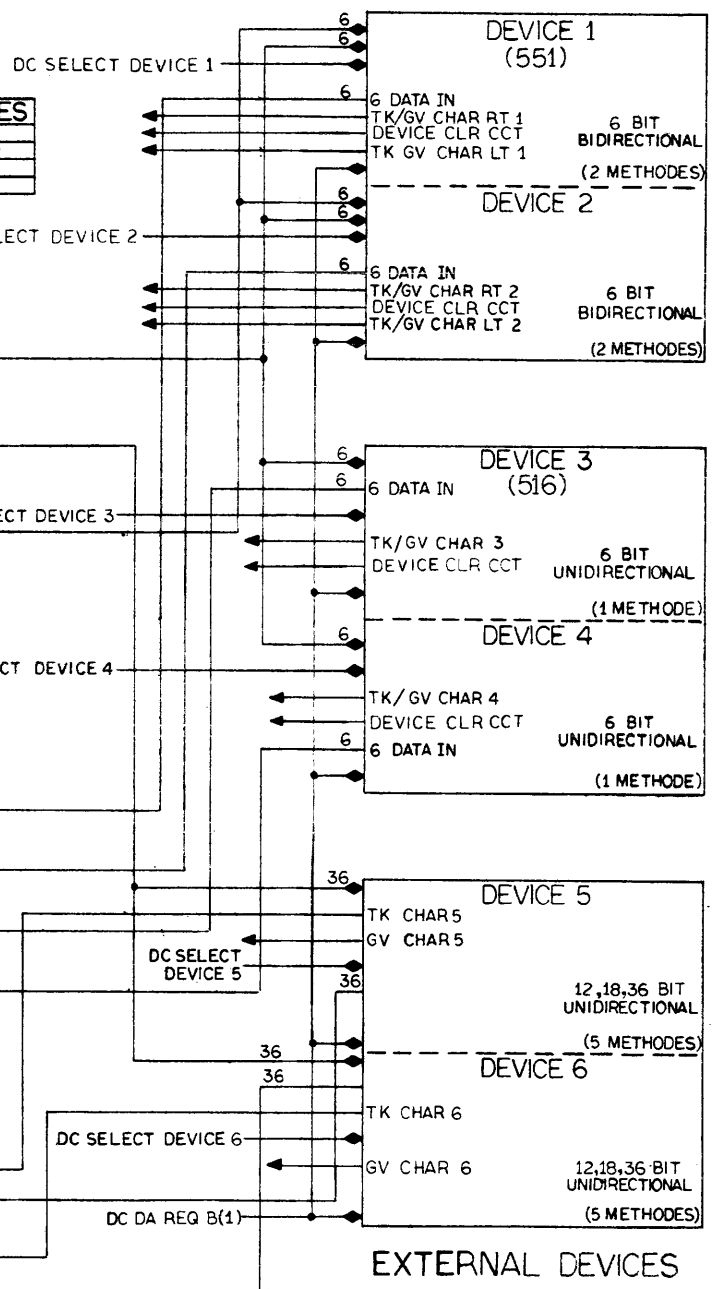
Data Control System Diagram
SD-D-136-0-DCSD

Timing Diagram TD-D-136-0-TD1
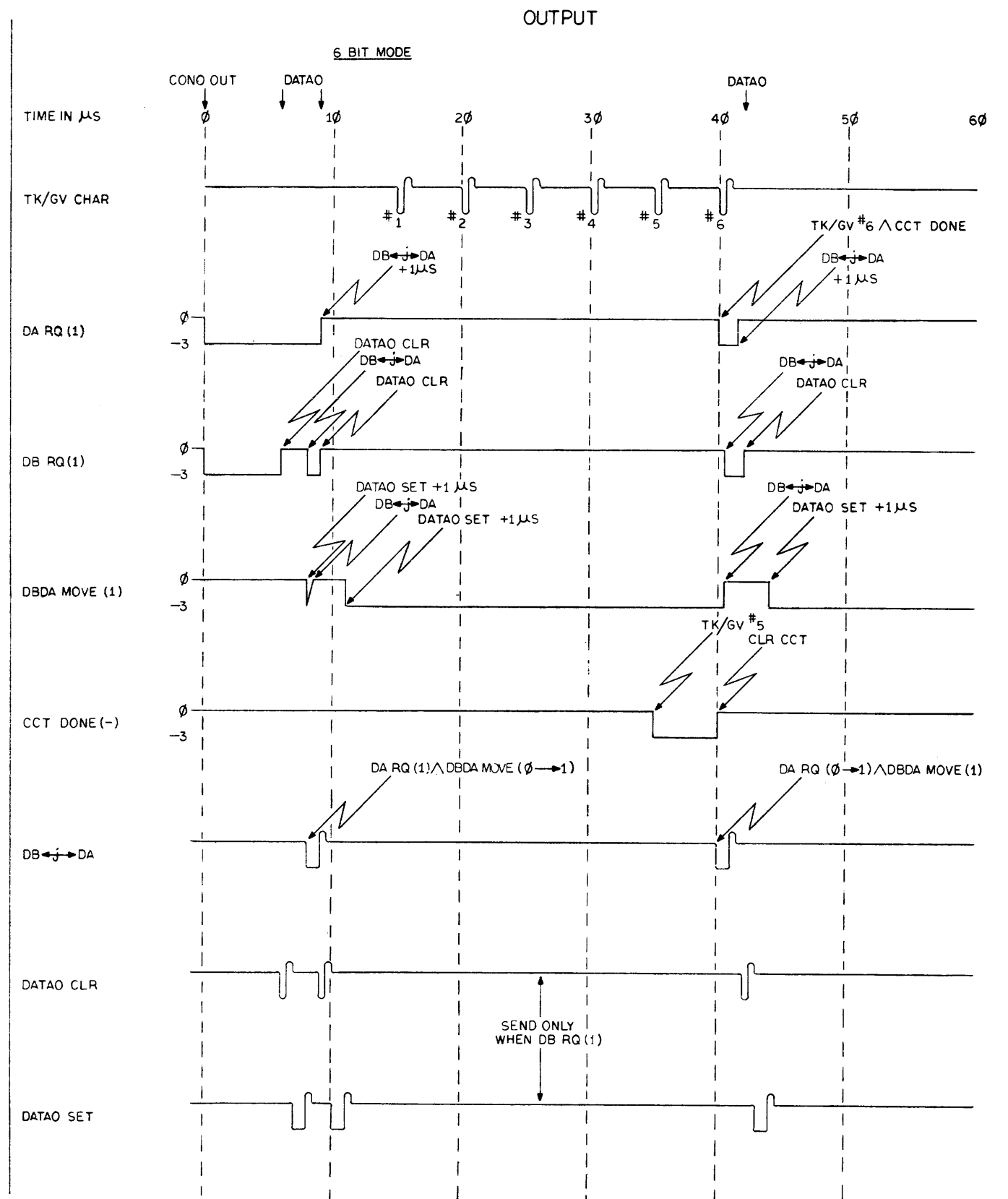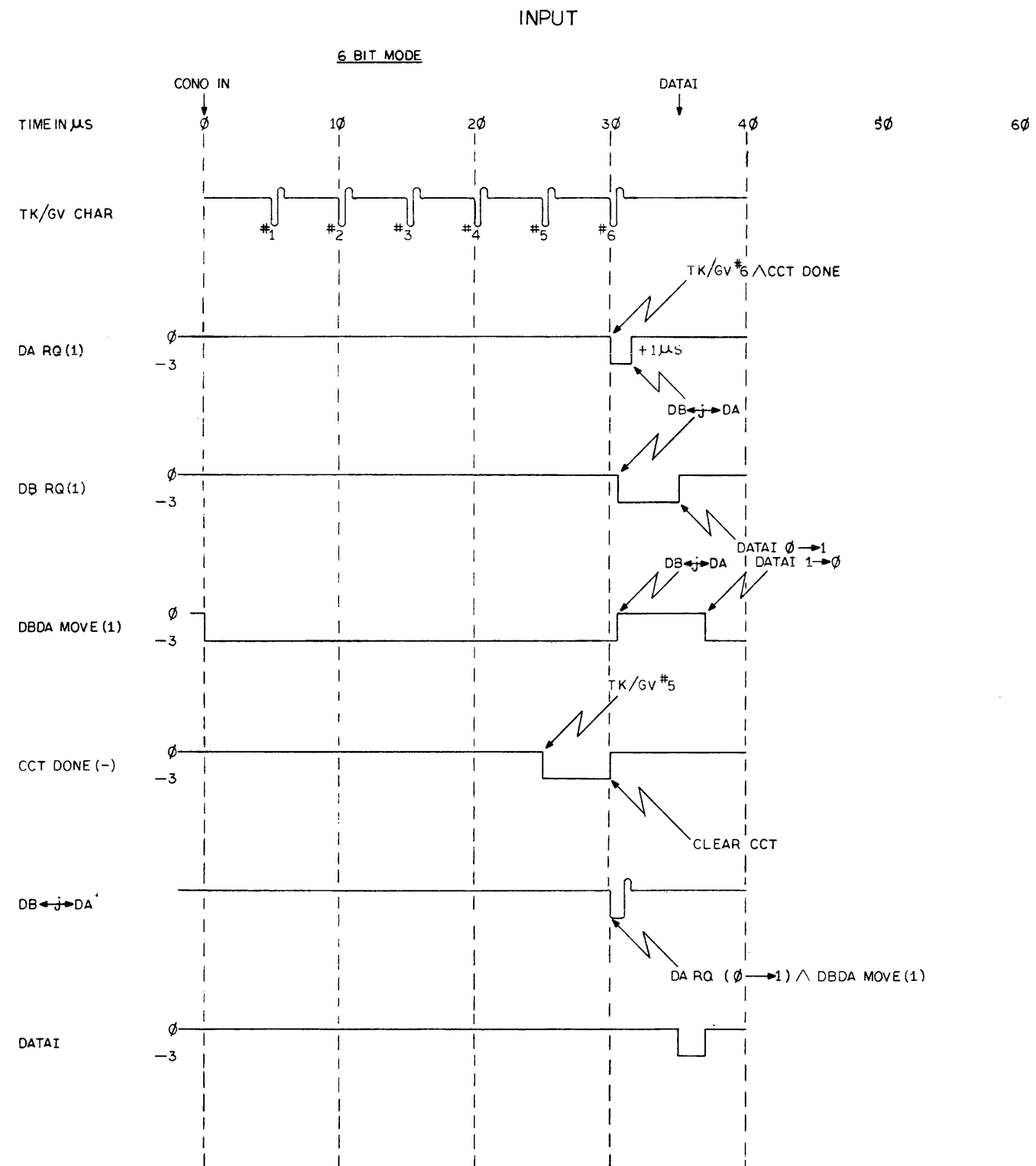
Timing Diagram TD-D-136-0-TD1

Data Control Power Wiring
PW-D-136-0-DCPW

A2-39

LOGIC PANELS

A

B

C

D

828 P.C.

FRONT

SEE DETAIL 'A'

723 P.S.
WHT
RED

BLK
BLU   RED
BLU

TWP
FL3
FL4
RED
WHT
FL1
FL2
811 P.C.
BLK

WHT   BLK   TWP
WHT

FAN

GRN

30 AMP HUBBLE "TWIST-LOCK"

INSIDE VIEW
OF PLENUM DOOR

BLK
RED
BLU

WHT

GRN

POWER SUPPLY
BUSS BRACKET

GRN
GRN   BLK   YEL
RED   BLU
YEL

TO MC BUSS

RED
BLK
BLU

828 P.C.

STANDARD D.E.C.
POWER CORD

FEMALE
PLUG

REAR VIEW
OF LOGIC PANELS

1A4C
(-15V)
#22 WHT
#22 WHT   #22 WHT   #22 WHT   #22 WHT

1 2 3 4 5 6 7 8 9 10

DETAIL A

Data Control Power Wiring
PW-D-136-0-DCPW

Utilization Module List (sheet 1)
UML-D-136-0-DCML

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
	1Ø32	1Ø32	1Ø32	1Ø32		4118-R	4604	4606	4604	4606	4127-75	4215	6115-02	6117-R	6117	4215-R	4606	4606	4129-R	4129-R	4604	1310			
1A		METHODE		PLUGS		DC SELECT	DC CLR SCT / DC CLR CCT	DC IC CLR / DC IC SET	DC IC CLR / DC DB←IOB / DC DB RQ←1	DC CLR DB / DB-J→DA / DA-J→DB	DC SCT 1 / DC CCT 2 / DC DB←IOB / DC CLR CCT / DC CLR SCT	DC SCT Ø / DC SCT 1	DC / SCT / DONE	DC CCT DONE	DC / CCT / DONE	DC CCT Ø / DC CCT 1 / DC CCT 2	DASH STRB RT DEV 5 / DASH STRB LT DEV 5 / DASH STRB RT DEV 6	DASH LT / DASH CP Ø / DASH STRB LT DEV 6	DASH LT / DASH CP Ø	DASH RT / DC CLR CCT	DASH CP 1 / DASH RT	DASH CP 1			
	1Ø32	1Ø32	1Ø32	1Ø32		4112-76	4113-R	4151	4102-R	4127	4217	4657	4217	4657	4217	4657	4217	4150	6102-150	6102-R	6684	1669			
1B		METHODE		PLUGS		DC CCT CONT / DC DB RQ / DC SCT CONT	DC STATUS / DC DB RQ←1 / DB→IOB	DC PI DECODE	DC DB IOB / DC STATUS / DC SCT DONE / DC CCT DONE / DC DA RQ / DC DB DA MOVE	DC DATA CLBD / DC DBDA MOVE / DC DA RQ / DC DATA CLBD	DC DATA CLBD	DC DB DA MOVE / IOB 2Ø / IOB 21 / IOB 22 / DC DATA CLBD	DC DB DA MOVE / DC DA RQ / DC IN/OUT / DC DB RQ / DC IN/OUT	DC DB DA MOVE / DC DA RQ / DC DB RQ / DC CH MODE Ø / DC CH MODE 1	DC CH MODE Ø / DC CH MODE 1 / DC DEV Ø' / DC DEV 1	DC DEVICE Ø / DC DEVICE 1 / DC DEVICE 2 / DC PIA Ø / DC PIA 1 / DC PIA 2	DC DEV 2 / DC PIA Ø / DC PIA 1 / DC PIA 2	DC DEVICE DECODE	DC DEVICE SELECT (B) / DC PI DECODE / DB→IOB / DC DB DA MOVE / DC DBDA MOVE / DC DB RQ	DC DEVICE SELECT (B) / DASH CP 1	DC STATUS / DC DA RQ B (1)	DC DARQ(1) / DC DBRQ(1) / DC DBDA(1) / DC IN/OUT(1) / DC CH MODE Ø(1) / DC CH MODE 1(1) / DC CCT Ø(1) / DC CCT 1(1) / DC CCT 2(1)			

Utilization Module List (sheet 2)
UML-D-136-0-DCML

1C

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
	4113-R	4230	4230	4230	4230	4230	4230	4230	4230	4230	4230	4230	4230	4127	4127	4127	4127	4127	4127	4127	4127	4127	4127	4127	4127
DASH DATA IN Ø LT																									
DASH DATA IN 1 LT														DA0(1)	DA0(1)	DA6(1)	DA6(1)	DA12(1)	DA12(1)	DA18(1)	DA18(1)	DA24(1)	DA24(1)	DA30(1)	DA30(1)
DASH DATA IN 2 LT		DB0,6,12	DB1,7,13	DB2,8,14	DB3,9,15	DB4,10,16	DB5,11,17	DB18,24,30	DB19,25,31	DB20,26,32	DB21,27,33	DB22,28,34	DB23,29,35	THRU	THRU	THRU	THRU	THRU	THRU	THRU	THRU	THRU	THRU	THRU	THRU
DASH DATA IN 3 LT		& DA0,6,12	& DA1,7,13	& DA2,8,14	& DA3,9,15	& DA4,10,16	& DA5,11,17	& DA18,24,30	& DA19,25,31	& DA20,26,32	& DA21,27,33	& DA22,28,34	& DA23,29,35	DA5(1)	DA5(1)	DA11(1)	DA11(1)	DA17(1)	DA17(1)	DA23(1)	DA23(1)	DA29(1)	DA29(1)	DA35(1)	DA35(1)
DASH DATA IN 4 LT																									
DASH DATA IN 4 LT																									

1D

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
	4113	4143-R	4143-R	4143-R	4102-R	4102-R	4102-R	4102-R	4102-R	1032	1032	1032	1032	1032	1032	1032	1032	1032	1032	1032	1032	1032	1032	1032	1032
DASH DATA IN Ø LT																									
DASH DATA IN 1 LT		DASH DATA IN 30 RT	DASH DATA IN 32 RT	DASH DATA IN 34 RT	DA Ø B(1)	DA Ø B(1)	DA 9 B(1)	DA 18 B(1)	DA 27 B(1)																
DASH DATA IN 2 LT																									
DASH DATA IN 3 LT						THRU	THRU	THRU	THRU		M	E	T	H	O	D	E		P	L	U	G	S		
DASH DATA IN 4 LT		DASH DATA IN 31 RT	DASH DATA IN 33 RT	DASH DATA IN 35 RT	DA 8 B(1)	DA 5 B(1)	DA 17 B(1)	DA 26 B(1)	DA 35 B(1)																
DASH DATA IN 5 LT																									

Data Buffer and Data Accumulator Racks C and D
WD-D-136-1-DAB1

Data Buffer and Data Accumulator Racks C and D
WD-D-136-1-DAB1