HARRIS

HD-6120

CMOS HIGH SPEED 12 BIT MICROPROCESSOR

Features

- LOW POWER, 50 MW OPERATING, 2 MW STATIC
- SINGLE SUPPLY – 5V
- OPERATION FROM DC TO 5.1 MHZ
- INDUSTRIAL AND MILITARY TEMPERATURE RANGES
- ON-CHIP CRYSTAL OSCILLATOR CIRCUITRY
- ON-CHIP EXTENDED MEMORY ADDRESSING–32K MAIN MEMORY, 32K CONTROL PANEL
- OPTIMIZED MICRO-CODE MINIMIZES THE NUMBER OF CLOCK CYCLES REQUIRED FOR ALL INSTRUCTIONS
- TWO ON-CHIP STACK POINTERS
- SIMPLIFIED MEMORY AND I/O CONTROL SIGNALS FOR EASY HARDWARE INTERFACING
- VECTORED INTERRUPT CAPABILITY
- SOFTWARE IS PAGE RELOCATABLE

Description

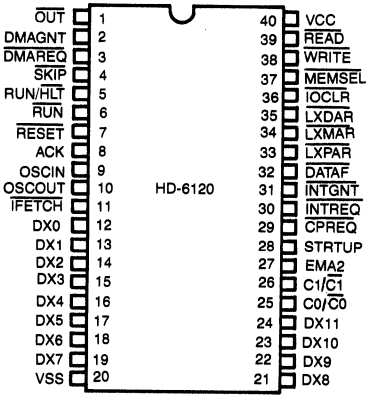
The HD-6120 is a general purpose high speed, CMOS 12 bit microprocessor. It is designed to recognize the instruction set of Digital Equipment Corporation's PDP-8/E* minicomputer.

Many architectural, functional and processing enhancements have been designed into the 6120 such that it can provide much higher system performance than its predecessor, the 6100.

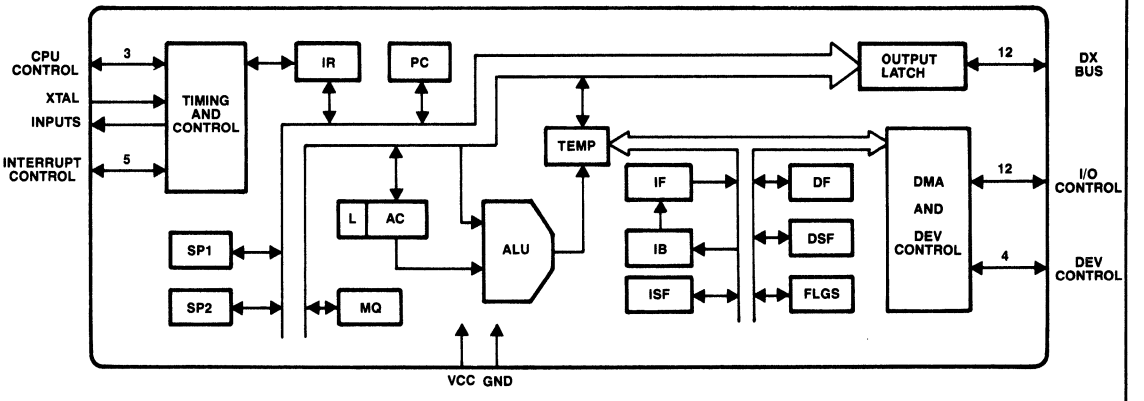
The 6120 is targeted toward the experienced PDP-8* or 6100 user. Twelve bit accuracy, rapid interrupt response, battery backup and low power (sealed enclosure) capability all equate to a processor ideally suited to real time control applications such as data acquisition, industrial control and harsh environment military systems.

* *TRADEMARK OF DIGITAL EQUIPMENT CORP.*

Pinout



Functional Diagrams



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0 VOLTS
Operating Voltage Range	+4V to +7V
Input/Output Voltage Applied	VSS−0.3V to VCC+0.3V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Industrial (−9, −9+)	−40°C to +85°C
Military (−2, −8)	−55°C to +125°C
Maximum Power Dissipation	1 Watt

CAUTION: Stresses above those listed in the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. ELECTRICAL CHARACTERISTICS; VCC=5.0V±5%; T_A = Industrial or Military

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	LOGICAL ONE INPUT VOLTAGE	70% VCC		V	
VIL	LOGICAL ZERO INPUT VOLTAGE		30% VCC	V	
VIH(CLK)	LOGICAL ONE CLOCK VOLTAGE	VCC−0.5		V	50% duty cycle $t_r, t_f \leq 20$ ns
VIL(CLK)	LOGICAL ZERO CLOCK VOLTAGE		VSS+0.5	V	50% duty cycle $t_r, t_f \leq 20$ ns
VTH+	SCHMITT TRIGGER POSITIVE THRESHOLD	50% VCC	VCC−0.5	V	$\overline{\text{RESET}}$, $\overline{\text{DMAREQ}}$, $\overline{\text{CPREQ}}$
VTH−	SCHMITT TRIGGER NEGATIVE THRESHOLD	0.5	30% VCC	V	$\overline{\text{RESET}}$, $\overline{\text{DMAREQ}}$, $\overline{\text{CPREQ}}$
VOH	LOGICAL ONE OUTPUT VOLTAGE	VCC−0.5		V	IOH = −1.6mA
VOL	LOGICAL ZERO OUTPUT VOLTAGE		0.5	V	IOL = 1.6mA
IIL	INPUT LEAKAGE CURRENT	−10	10	μA	OV≤VIN≤VCC
IO	OUTPUT LEAKAGE CURRENT	−10.0	10.0	μA	OV≤VO≤VCC
ICC	POWER SUPPLY STANDBY CURRENT		500	μA	VIN=VCC or GND VCC = 5.25 V RESET STATE OUTPUTS OPEN
ICC*	POWER SUPPLY OPERATING		10	ma	VIN=VCC or GND VCC = 5.25 V F = 5.1 Mhz OUTPUTS OPEN
IOSH	HOLD CURRENT DURING DMAGNT	−0.2	−0.6 −10.0	ma μa	Vout = VCC−1.0V Vout = OV $\overline{\text{LXMAR}}$, $\overline{\text{LXPAR}}$, $\overline{\text{READ}}$, $\overline{\text{WRITE}}$, $\overline{\text{OUT}}$ AND MEMSEL
IOSS	HOLD CURRENT DURING IOT SAMPLE TIMES	−1.6	−10.0	ma	Vout = OV C0, C1, AND $\overline{\text{SKIP}}$ OUTPUTS
IOSS	HOLD CURRENT DURING IOT SAMPLE TIMES	−50	−250	μa	Vout = OV $\overline{\text{INTREQ}}$ OUTPUT
CIN*	INPUT CAPACITANCE		5	pf	FREQ = 1 MHZ T_A=25°C VIN=VCC or GND
COUT*	OUTPUT CAPACITANCE		15	pf	FREQ = 1 MHZ T_A=25°C VIN=VCC or GND

** Guaranteed and sampled, but not 100% tested*

A.C. ELECTRICAL CHARACTERISTICS; VCC=5.0V±5%; T_A=Industrial or Military; C_L=50 pf, FREQ=5.1 MHZ

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
F	OPERATING FREQUENCY	0	5.1	Mhz	
T	MINOR CYCLE PERIOD	392		ns	T = 2/F
TL	LXMAR, LXPAR, LXDAR PULSE WIDTH	125		ns	F=5.1 Mhz
TAS	ADDRESS SET UP TIME	60		ns	
TAH	ADDRESS HOLD TIME	180		ns	
TREAD	READ ACCESS TIME	720		ns	
TRS	READ SET UP TIME	135		ns	
TRH	READ HOLD TIME	20		ns	MEMORY OPERATIONS
TRP	READ PULSE WIDTH	425		ns	
TRD	READ PULSE DELAY	40		ns	
TWPD	WRITE PULSE DELAY	200		ns	
TWS	WRITE SET UP TIME (ALL NON IOT)	375		ns	
TWP	WRITE PULSE WIDTH (ALL NON IOT)	425		ns	
TWH	WRITE HOLD TIME (ALL NON IOT)	200		ns	
TWSIO	WRITE SET UP TIME (IOT)	200		ns	
TWIO	WRITE PULSE WIDTH (IOT)	375		ns	
TWHIO	WRITE HOLD TIME (IOT)	125		ns	
TDA	READ ACK DELAY FOR NO WAIT		150	ns	
TXA	WRITE ACK DELAY FOR NO WAIT		150	ns	F=5.1 Mhz

NOTE: All measurements are taken with input rise and fall times ≤ 20 nsec.

DECOUPLING CAPACITORS

The transient current required to charge and discharge the 50 pF load capacitance specified in the 6120 data sheet is determined by

$$i = C_L\,(dv/dt)$$

Assuming that all DX outputs change state at the same time and that dv/dt is constant;

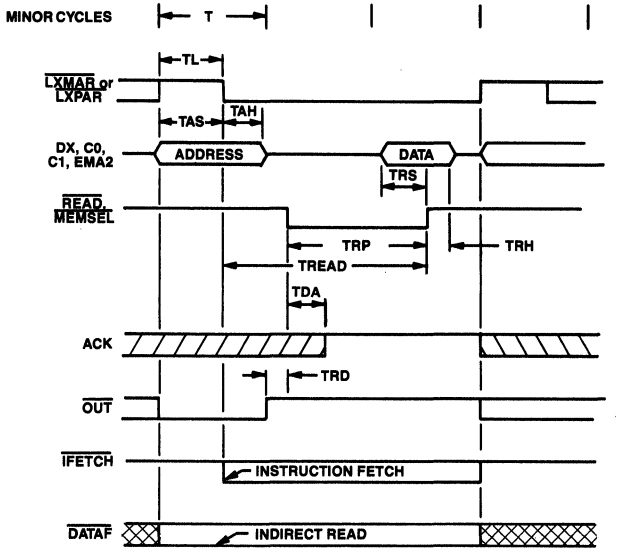
$$i \cong C_L \frac{(VCC \times 80\%)}{t_R/t_F}$$

where t_R=20 ns, VCC=5.0 volts, C_L=50 pF on each of twelve outputs.

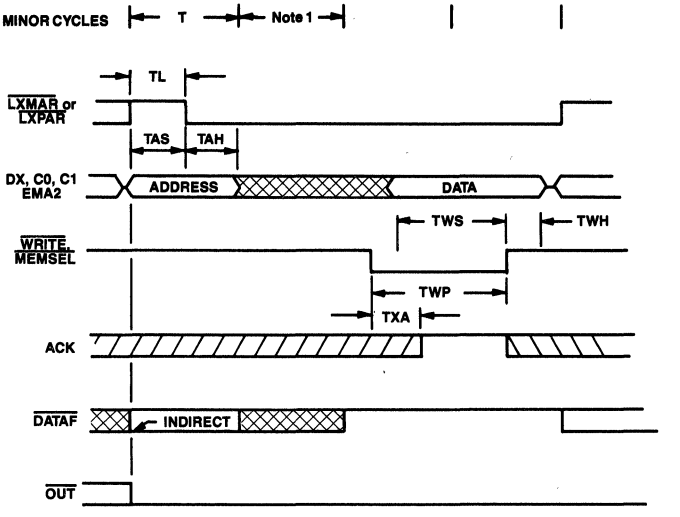
$$i \cong (12 \times 50 \times 10^{-12}) \times (5.0v \times 0.8)/(20 \times 10^{-9})$$
$$\cong 120\ mA$$

This current spike may cause a large negative voltage spike on VCC, which could cause improper operation of the device. To filter out this noise, it is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between VCC and GND at each device, with placement being as near to the device as possible.

It is recommended that for systems with greater than 50 pF loading on the DX outputs that Harris HD-6432 CMOS Hex Bi-directional bus drivers be used to buffer the 6120 from the rest of the system. The HD-6432 bus driver has guaranteed performance specifications up to a 300 pF load.

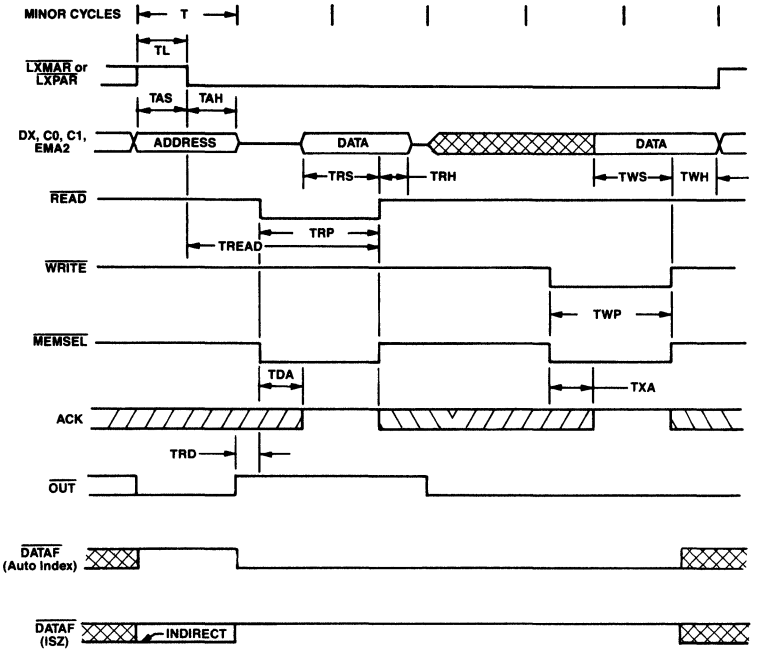


MEMORY READ OPERATION

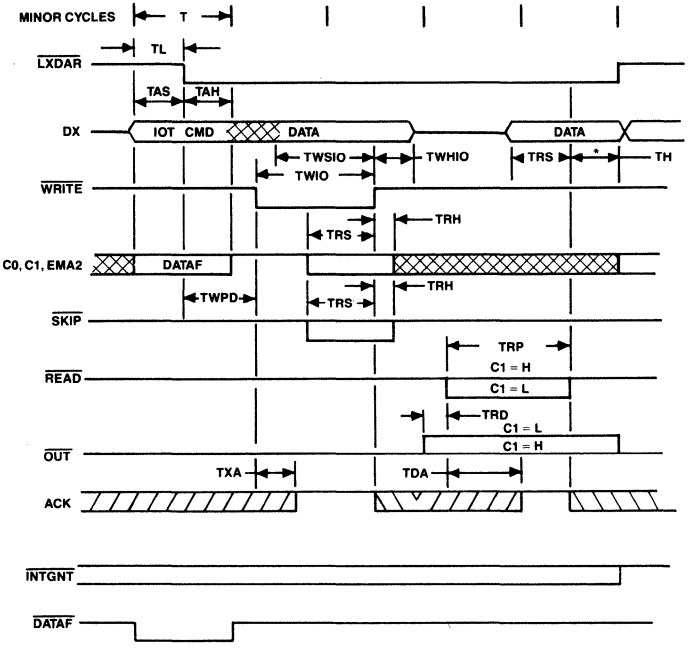


NOTE 1: This cycle is deleted on PAC1, PAC2, PPC1, PPC2 and control panel Interrupt writes.

MEMORY WRITE OPERATION



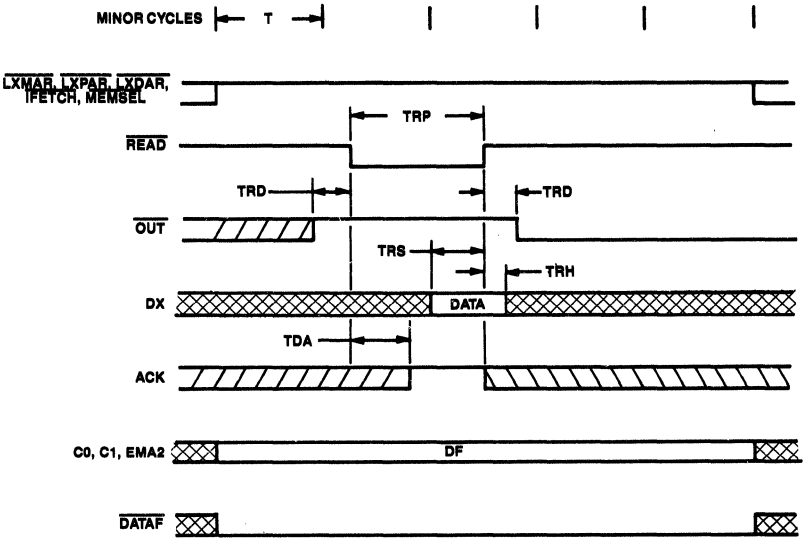
MEMORY READ-MODIFY-WRITE OPERATION



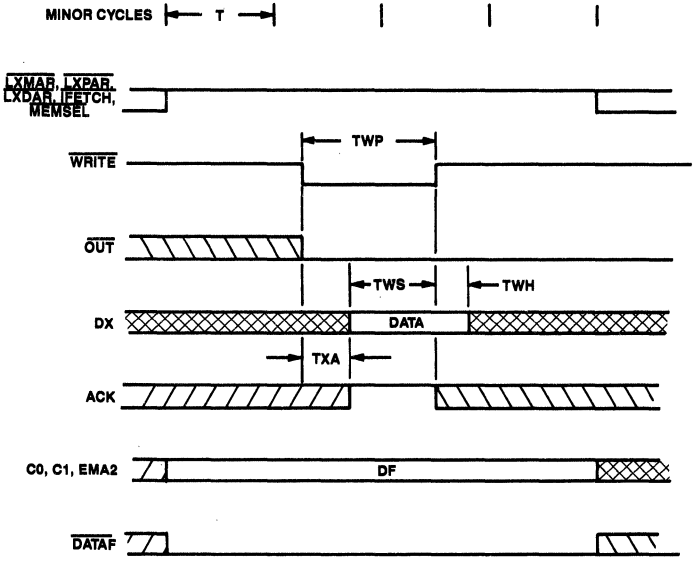
NOTES: Operation is shortened one Minor Cycle if READ is not executed.

* Read Data must be held until the rising edge of LXDAR for Read IOTs.

EXTERNAL IOT OPERATION



OR SWITCH REGISTER (OSR)



WRITE TO SWITCH REGISTER

Pin Assignments

I/O	Pin	Symbol	Active Level	Description
O	1	$\overline{OUT}$	Low	Bus timing control output which is low during all bus write or addressing operations. This signal is used to enable outbound bus drivers.
O	2	DMAGNT	High	Direct memory access grant output – DX, C0, C1, and EMA2 lines are high impedance.
I	3	$\overline{DMAREQ}$	Low	Schmitt trigger input. Direct memory access request – DMA is granted at the end of the current bus operation. Upon DMA grant, the 6120 suspends program execution until the $\overline{DMAREQ}$ line is pulled high.
I	4	$\overline{SKIP}$	Low	Input which causes the 6120 to skip the next instruction if low during an I/O instruction.
I	5	RUN/$\overline{HLT}$		Pulsing the RUN/$\overline{HLT}$ input causes the 6120 to alternately run and halt by changing the state of the internal RUNHLT flip flop on the positive transition of the RUN/$\overline{HLT}$ line.
O	6	$\overline{RUN}$	Low	This output indicates the operating state of the 6120. It is low at all times except during the reset and halt states.
I	7	$\overline{RESET}$	Low	Schmitt trigger input. Clears the AC and the memory extension registers and loads 7777 (octal) into the PC. RUNHLT is set. The STRTUP line controls whether execution starts in control panel or main memory. $\overline{RESET}$ must be held low at least 42 clock cycles after the clock starts running in order to initialize the timing generator. $\overline{LXDAR}$ is held low while $\overline{RESET}$ is low, and remains low until after the positive transition of $\overline{RESET}$ and $\overline{IOCLR}$.
I	8	ACK	High	This input indicates that peripheral or external memory is ready to transfer data. The 6120 read or write state gets extended as long as ACK is low. During this time the 6120 is in the lowest power state with clocks running.
I	9	OSCIN		Input to crystal oscillator amplifier. (Also external clock input.)
O	10	OSCOUT		Output of crystal oscillator amplifier.
O	11	$\overline{IFETCH}$	Low	Instruction fetch cycle output.
I/O	12-19, 21-24	DX0-DX11	High	Multiplexed bidirectional data in, data out and address lines. (DX0=MSB, DX11=LSB.)
	20	VSS		Most negative supply voltage.
I/O	25	C0/$\overline{C0}$		Multiplexed extended memory address (EMA) active high output MSB and peripheral device control line active low input from the peripheral device during an I/O transfer.
I/O	26	C1/$\overline{C1}$		Multiplexed EMA bit 1 and peripheral control line. See C0.
O	27	EMA2	High	Low order extended memory address output.
I	28	STRTUP		This input is tied to either VCC or VSS. If tied to VSS, the 6120 makes a panel request (caused by the PWRON flag) as soon as $\overline{RESET}$ goes to VCC. 7777 is stored in location 0000 of field O of panel memory. If STRTUP is tied to VCC, PWRON does not cause a panel request. Instead, the CPU starts running in location 7777 of field O of main memory. Location 0000 of main memory is not altered.
I	29	$\overline{CPREQ}$	Low	Schmitt trigger input. External control panel request – a dedicated interrupt which bypasses the normal device interrupt request structure. $\overline{CPREQ}$ causes a control panel interrupt request by setting the bootstrap flag with the negative going transition of $\overline{CPREQ}$. Therefore, this input is transition rather than level sensitive.
I	30	$\overline{INTREQ}$	Low	Peripheral device interrupt request input.
O	31	$\overline{INTGNT}$	Low	Peripheral device interrupt grant output.
O	32	$\overline{DATAF}$	Low	Output which is low whenever the Data Field is placed on the C0, C1 and EMA2 lines.
O	33	$\overline{LXPAR}$	Low	Output which causes control panel memory address register to be loaded. Same as $\overline{LXMAR}$, but for control panel memory operations.
O	34	$\overline{LXMAR}$	Low	Output which causes main memory address register to be loaded. Address is strobed into the main memory at the falling edge of $\overline{LXMAR}$.
O	35	$\overline{LXDAR}$	Low	Output which causes device address register to be loaded. Same as $\overline{LXMAR}$ or $\overline{LXPAR}$, except for IOT operations. Also used to distinguish between $\overline{IOCLR}$ signals. See $\overline{IOCLR}$ below.
O	36	$\overline{IOCLR}$	Low	Output which is low when $\overline{RESET}$ is low, or when CAF instruction is given. Used to clear I/O flags. If caused by $\overline{RESET}$, $\overline{LXDAR}$ is low during and after the trailing edge of $\overline{IOCLR}$.
O	37	$\overline{MEMSEL}$	Low	Memory select. During memory operations, this output pulses to VSS at bus read and write times.
O	38	$\overline{WRITE}$	Low	Write pulse. This output is low during all bus data write operations; memory, I/O, and write to switch register.
O	39	$\overline{READ}$	Low	Read pulse. This output is low during all bus read operations; memory, I/O and switch register. It also serves the function of enabling inbound bus drivers.
	40	VCC		Positive supply voltage.

Major Registers

ACCUMULATOR (AC)

The AC is a 12-bit register with which arithmetic and logical operations are performed. Data words may be fetched from memory to the AC or stored from the AC into memory. Arithmetic and logical operations involve two operands, one held in the AC and the other fetched from memory. The result of the operation is left in the AC. The AC may be cleared, complemented, tested, incremented or rotated under program control. The AC also serves as an input-output register. All programmed data transfers pass through the AC.

Link (L)

L is a 1-bit flip flop that serves as a high-order extension of the AC. It is used as a carry flip flop for 2's complement arithmetic. A carry out of the ALU complements L. L can be cleared, set, complemented and tested under program control and rotated as a part of the AC.

MQ REGISTER (MQ)

The MQ is a 12-bit temporary register which is program accessible. The contents of AC may be transferred to the MQ for temporary storage. MQ can be OR'ed with the AC and the result stored in the AC. The contents of the AC and the MQ may also be exchanged.

OUTPUT LATCH (OL)

While accessing memory or I/O, all data or addresses generated by the 6120 on the DX bus are held in the OL for the time required on the bus. This frees the 6120 internal bus for other uses during these operations. The output latch can also be read to the 6120 internal bus so that it can function as a temporary holding register for internal operations.

PROGRAM COUNTER (PC)

The 12-bit PC contains the address of the memory location from which the next instruction is fetched. During an instruction fetch, the PC is transferred to OL and the PC is then incremented by 1. When there is a branch to another address in memory, the branch address is set into the PC. Branching normally takes place under program control. A skip (SKP, SMA, SZA, SNL, etc.) instruction increments the PC by 1 (again), thus causing the next instruction to be skipped. The skip instruction may be unconditional or conditional on the state of the AC and/or LINK. During an input-output operation, a device can also cause the next instruction to be skipped.

TEMPORARY REGISTER (TEMP)

The 12-bit TEMP register latches the result of an ALU operation before it is sent to the destination register to avoid race conditions. The TEMP is also used as an internal register during instruction execution.

INSTRUCTION REGISTER (IR)

During an instruction fetch, the 12-bit IR contains the instruction that is to be executed by the 6120.

STACK POINTERS (SP1 and SP2)

The stack pointers are two twelve-bit registers which hold the address of the next stack storage location. PPCX or PACX instructions cause post-decrement of the contents of stack pointer SPX. RTNX or POPX cause a pre-increment of the contents of the stack pointer. Stack pointers are loaded from, and read into, the AC. They may also be used as program-controlled temporary registers.

Memory Extension Control Registers

INSTRUCTION FIELD (IF)

The 3-bit Instruction Field holds the memory field from which all instructions, all indirect address pointers and all directly addressed operands are obtained. It may be read into the AC, and loaded from the IB. It is cleared by $\overline{\text{RESET}}$.

INSTRUCTION BUFFER (IB)

The 3-bit Instruction Buffer serves as a holding register for instructions which change the IF. Instead of changing the IF directly, field bits are loaded into the IB, and transferred to the IF at the next JMP, JMS, RTN1 or RTN2. The IB may be loaded from instruction bits, from the AC or from the ISF. The IB is cleared by $\overline{\text{RESET}}$.

INSTRUCTION SAVE FIELD (ISF)

The 3-bit ISF is loaded with the contents of the IF upon granting of an interrupt. The ISF may be read into the AC. It is cleared by $\overline{\text{RESET}}$.

DATA FIELD (DF)

The 3-bit Data Field holds the memory field from which all indirectly addressed operands are obtained. The DF may be loaded from instruction bits, from the AC or from the DSF. It may be read into the AC. It is cleared by $\overline{\text{RESET}}$.

DATA SAVE FIELD (DSF)

The 3-bit DSF is loaded with the contents of the DF upon granting of an interrupt. The DSF may be read into the AC. It is cleared by $\overline{\text{RESET}}$.

Basic Timing and State Control

A 15-bit address is sent on the C0, C1, EMA2 and DX lines for memory reference instructions. The $\overline{\text{LXMAR}}$ or $\overline{\text{LXPAR}}$ signals cause an external register to store the address information if required. When executing an input-output instruction, $\overline{\text{LXDAR}}$ causes an external register to be loaded with device address and control information.

Memory data is read for an input transfer (READ). ACK controls the transfer duration. If ACK is low during input transfers, the 6120 waits with the $\overline{\text{READ}}$ line low. The high state of the ACK signal causes the 6120 to continue.

Output transfers are similar to input transfers. The address is defined as given above. ACK controls the length of time for which the $\overline{\text{WRITE}}$ signal is low, similar to the $\overline{\text{READ}}$ line control.

During an instruction fetch the instruction to be executed is retained internally and then executed. During the sequencing of the instruction the external request lines are sampled by the priority network. The state of this network decides whether the machine is going to fetch the next instruction in sequence or service one of the internal or external request lines.

Internal Priority Structure

GENERAL DESCRIPTION

The external request lines and the internal request flags are sampled in an internal priority network. The internal priority is RESET, DMAREQ, RUN/HLT, CPREQ, INTREQ, and IFETCH. The state of the priority network determines the next operation.

IFETCH

If no external or internal requests are pending, the 6120 fetches the next instruction pointed to by the contents of the PC. The IFETCH line is low during the cycle in which the instruction is fetched.

RESET

RESET initializes all internal flags and clears the AC, LINK and MQ. All memory extension bits (IF, IB, DF, ISF and DSF) are cleared. The interrupt enable and interrupt inhibit flip flops are cleared. RUNHLT is set to the run state. The RUN line is held high by RESET. The states of SP1 and SP2 are undefined at power up, and are unaffected by RESET.

Upon application of power, the internal timing generator is completely initialized within 42 clock pulses after power is within limits with RESET held low.

The 6120 remains in the reset state as long as the RESET line is low. LXMAR, LXPAR, READ, WRITE, MEMSEL, INTGNT and IFETCH are held high. IOCLR is held low. After RESET is changed from low to high, IOCLR is made high. LXDAR is held low for one minor cycle after IOCLR is high. DMAGNT and OUT are low. The first LXMAR or LXPAR occurs 5-1/2 minor cycles after IOCLR goes high. The PC is set to 7777 (octal) and execution commences in control panel or main memory, depending on whether the STRTUP input is low or high respectively. If execution commences in control panel memory, the FZ flag is set, the Panel Data flag is cleared, and 7777 is deposited in location 0000 of control panel memory before beginning instruction execution at location 7777. If execution commences in main memory, location 0000 of main memory is not modified.

RUN/HLT

The RUN/HLT line changes the state of the RUNHLT flip flop. This flip flop is initially placed in the run state by RESET. Pulsing RUN/HLT low causes the 6120 to alternately run and halt. This is true whether executing in main memory or control memory. The RUN/HLT line is normally high. The 6120 recognizes the positive transition of the RUN/HLT signal. The HLT instruction (7402 octal) does not cause the RUNHLT flip flop to be cleared, but causes entry into panel mode with the HLTFLG set.

Memory Organization

The 6120 has a basic addressing capacity of 4096 12-bit words. The addressing capacity is extended by the internal extended memory control hardware. The memory system is organized in 4096 word groups, called memory fields. The first 4096 words of memory are in field 0. If a full 32K block of memory is installed, the uppermost memory field will be numbered 7. Two 32K word blocks of memory may be connected to the 6120. One of these blocks is known as main memory and the other is known as panel memory.

In any given memory field, every location has a unique 4 digit octal (12 bit binary) address, 0000 to 7777 (0000 to 4095 decimal). Each memory field is subdivided into 32 pages of 128 words each. Memory pages are numbered sequentially from page 00, containing octal addresses 0000-0177, to page 37 (octal), containing octal addresses 7600-7777. The most significant 5 bits of a 12-bit memory address denote the page number and the 7 low order bits specify the address of the memory location within the given page.

During an instruction fetch cycle, the 6120 fetches the instruction pointed to by the IF, PC, and address strobes LXMAR or LXPAR. The contents of the PC are transferred to the OL. The PC is incremented by 1. The PC now contains the address of the 'next' sequential instruction. The OL now contains the address of the 'current' instruction which must be fetched from memory. Bits 0-4 of the OL identify the current page, that is, the page from which instructions are currently being fetched. Bits 5-11 of the OL identify the location within the current page. (Page zero, by definition, denotes the first 128 words of memory within a field, octal addresses 0000-0177.)

Memory Reference Instructions (MRI)

The memory reference instructions operate on the contents of a memory location or use the contents of a memory location to operate on the AC or the PC. Bits 0-2 of a memory reference instruction specify the operation code, or opcode, and the 9 low-order bits specify the operand address. Bits 5-11, the page address, identify the location of the operand on a given page, but they do not identify the page itself. The page is specified by bit 4, called the page bit. If bit 4 is a 0, the page address is interpreted as a location on page 0. If bit 4 is a 1, the page address is interpreted to be on the current page. The entire 12-bit address, consisting of the 7 low-order bits from the instruction and either 0 or the contents of the OL in the 5 high-order bits is known as the instruction address, or IA. The IF provides the 3 high-order bits of the complete 15-bit address, IA.

Other locations are addressed by utilizing bit 3. When bit 3 is a 0, the operand is directly addressed, and IA is the location of the operand. When bit 3 is a 1, the operand is indirectly addressed, and the contents of IA specify the location of the operand. To address a location that is not on page 0 or the current page, the absolute address of the desired location is stored in one of the 256 directly-addressable locations as a pointer address. The instruction addresses the operand indirectly through this pointer. Upon execution, the MRI operates on the contents of the location identified by the address contained in the pointer location. The pointer is obtained from the current Instruction Field; the data is in the current Data Field.

It should be noted that locations 0010-0017 (octal) in page 0 of any field are autoindexed. If these locations are addressed as indirect pointers, the contents are incremented by 1 and restored before they are used as the operand address. These locations may, therefore, be used for indexing applications. During the memory write operation, the DF appears on C0, C2, and EMA2. Indirect reference to auto index registers from page 0 work as defined whether the page bit is "1" or "0".

Data is represented in two's complement integer notation. In this system of notation, the negative of a number is formed by complementing each bit in the data word and adding "1" to the complemented number. The sign is indicated by the most-significant bit. In the 12-bit word used in the 6120, when bit 0 is a "0", it denotes a positive number and when bit 0 is a "1", it denotes a negative number. The number range for this system is +3777 to −4000 octal (+2047 to −2048 decimal).

Microprogramming

Group 1, 2 and 3 instructions are all microprogrammable. This means that as many as five discrete instructions can be combined into one instruction which can execute in the same amount of time required for a single discrete instruction. Instructions listed under Groups 1, 2 and 3 represent the most commonly used microcoded instructions for these groups and are not a complete listing of all possible instructions. The general rule of thumb is that if an instruction can be represented in machine code (using the "Microinstruction Format" templet), then it is a legal instruction. The logical sequence table which accompanies each "Microinstruction Format" templet shows the order in which the microcoded operations are performed. "Introduction to Programming" by Digital Equipment Corporation further explains the PDP-8* instruction set and the use of microprogramming. This handbook is also available from Harris Semiconductor.

* Trademark of Digital Equipment Corporation

HD-6120 Oscillator Requirements

The HD-6120 has been designed to work with either a parallel resonant, fundamental mode crystal or an external frequency source.

EXTERNAL CRYSTAL

When using an external crystal, two capacitors and a resistor are required to complete the oscillator circuit. Table 1 lists the required crystal characteristics and Figure 1 shows the correct circuit connections.

TABLE 1

Parameter	Typical Characteristic
Frequency	2.4 – 5.1 Mhz
Type of Operation	Parallel resonant, AT cut, Fundamental mode
Load Capacitance	C_L = 20pf or 32pf
R_{series} (Max.)	200 Ω at 5.1 Mhz

The load capacitors C1, C2 are chosen such that the total (including stray) capacitance seen by the crystal matches the specified load capacitance (C_L). For C_L = 20pf. a value of C1 = C2 = 20pf. is normally used. For C_L = 32pf. C1 and C2 would be approximately 47pf. The actual values are normally not critical unless an ultra precise frequency is desired.

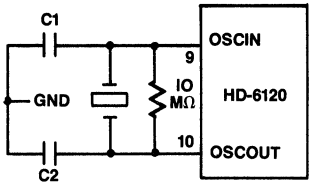


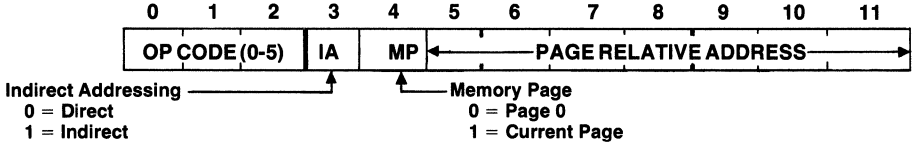
FIGURE 1

EXTERNAL FREQUENCY SOURCE

When using an external frequency source, the duty cycle should be 50/50 with rise and fall times less than 20ns. Input voltage levels should be $V_{IH} \geq VCC - 0.5V$ and $V_{IL} \leq 0.5V$. The OSCIN pin of the HD-6120 is used in this case with the OSCOUT pin left open. The Harris 82C84A CMOS Clock Generator is an excellent external frequency source which provides three outputs at different divide ratios (÷1, ÷3, ÷6).

Memory Reference Instructions

MICROINSTRUCTION FORMAT



Mnemonic	Opcode	Minor Cycles Dir	Ind	Auto	Operation
AND	0xxx	7	10	12	LOGICAL AND: Causes a bit-by-bit boolean AND between the contents of the Accumulator and the contents of the effective address (xxx) specified by the instruction. The result is left in the AC and the data word in the referenced location is not altered.
TAD	1xxx	7	10	12	TWO'S COMPLEMENT ADD: Performs a binary two's complement addition between the specified data word and the contents of the AC; the result is left in the AC. If a carry out occurs, the state of the Link is complemented. If the AC is initially cleared, this instruction acts as a load from memory.
ISZ	2xxx	9*	12*	14*	INCREMENT AND SKIP IF ZERO: The contents of the effective address is incremented by 1 and restored. If the result is zero, the next sequential instruction is skipped.
DCA	3xxx	7	10	12	DEPOSIT AND CLEAR THE ACCUMULATOR: The contents of the AC are stored in the effective address and the AC is cleared.
JMS	4xxx	7	10	12	JUMP TO SUBROUTINE: The contents of the PC is stored in the effective address and the effective address + 1 is stored in the PC. The Link, AC and MQ are unchanged.
JMP	5xxx	4	7	9	JUMP: The effective address is loaded into the PC thus causing program execution to branch to a new location.

* Add two Minor Cycles if a skip is taken.

Group 1 Operate Instructions

All group 1 instructions require 6 minor cycles, except those performing an RTR, RTL, or BSW instruction (8 minor cycles).

MICROINSTRUCTION FORMAT

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	0	CLA	CLL	CMA	CML	R1	R2	R3	IAC

Logical Sequence:
1 – CLA, CLL
2 – CMA, CML
3 – IAC
4 – RAR, RAL, RTR, RTL, BSW, R3L

Bit	R1	R2	R3	
	0	0	0	No Rotate
	0	0	1	BSW
	0	1	0	RAL
	0	1	1	RTL
	1	0	0	RAR
	1	0	1	RTR
	1	1	0	R3L
	1	1	1	Do Not Use

Mnemonic	Opcode	Logical Sequence	Operation
NOP	7000	1	No operation.
IAC	7001	3	Increment accumulator – the contents of the AC is incremented by 1. Carry out complements the LINK.
BSW	7002	4	Byte swap – AC0–5 are exchanged with AC6–11 respectively. The LINK is not changed.
RAL	7004	4	Rotate accumulator left – the contents of the AC and LINK are rotated one binary position to the left. AC0 is shifted to LINK and LINK is shifted to AC11.
RTL	7006	4	Rotate two left – equivalent to two RAL's.
RAR	7010	4	Rotate accumulator right – the contents of the AC and LINK are rotated one binary position to the right. AC11 is shifted into the LINK, and LINK is shifted to AC0.
RTR	7012	4	Rotate two right – equivalent to two RAR's.
R3L	7014	4	Rotate AC (but not LINK) left 3 places. AC0 is rotated into AC9, AC1 into AC10, etc.
CML	7020	2	Complement LINK – the contents of the LINK is complemented.
CMA	7040	2	Complement accumulator – the contents of the AC is replaced by its 1's complement.
CIA	7041	2, 3	Complement and increment accumulator – the contents of the AC is replaced by its 2's complement.
CLL	7100	1	Clear LINK – the LINK is made 0.
CLL RAL	7104	1, 4	Clear LINK, rotate left.
CLL RTL	7106	1, 4	Clear LINK, rotate two left.
CLL RAR	7110	1, 4	Clear LINK, rotate right.
CLL RTR	7112	1, 4	Clear LINK, rotate two right.
STL	7120	1, 2	Set the LINK – load binary 1 into LINK.
CLA	7200	1	Clear accumulator – load AC with 0000.
CLA IAC	7201	1, 3	Clear and increment accumulator – load AC with 0001.
GLK	7204	1, 4	Get LINK – place LINK in AC11; clear AC0-10 and LINK.
STA	7240	1, 2	Set accumulator – make AC=7777.
CLA CLL	7300	1	Clear AC and LINK.

Group 2 Operate Instructions

All group 2 instructions require 7 minor cycles, except OSR and LAS (8 minor cycles).

MICROINSTRUCTION FORMAT

0	1	2	3	4	5	6	7	8	9	10	11
					SMA	SZA	SNL	0			
1	1	1	1	CLA	SPA	SNA	SZL	1	OSR	HLT	0

Logical Sequence:
1 – (BIT 8=0) – SMA or SZA or SNL
– (BIT 8=1) – SPA and SNA and SZL
2 – CLA
3 – OSR, HLT

Mnemonic	Opcode	Logical Sequence	Operation
NOP	7400	1	No operation
HLT	7402	3	Set the HLTFLG. Causes entry into panel mode instead of executing the next instruction provided IIFF is not set. If IIFF is set, panel mode is entered after the JMP, JMS, RTN1 or RTN2 which clears IIFF. This instruction in panel mode does not cause a re-entry into panel mode, but does set HLTFLG.
OSR	7404	3	OR with switch register – the contents of an external device are "OR"ed with the contents of the AC, and the result stored in the AC. The contents of the DF are available for device selection.
SKP	7410	1	Skip – the content of the PC is incremented by 1, to skip the next instruction.
SNL	7420	1	Skip on non-zero LINK – skip if LINK one
SZL	7430	1	Skip if LINK zero
SZA	7440	1	Skip on zero accumulator – skip if AC=0000
SNA	7450	1	Skip on non-zero accumulator
SZA SNL	7460	1	Skip if AC=0000 or if LINK=1
SNA SZL	7470	1	Skip if AC not 0000 and if LINK is zero
SMA	7500	1	Skip on minus accumulator (ACO=1)
SPA	7510	1	Skip on positive accumulator (ACO=0)
SMA SNL	7520	1	Skip if AC is minus or if LINK is 1
SPA SZL	7530	1	Skip if AC is plus and if LINK is 0
SMA SZA	7540	1	Skip if AC is minus or zero
SPA SNA	7550	1	Skip if AC is positive and non-zero
SMA SZA SNL	7560	1	Skip if AC is minus or if AC is =0000 or if LINK is 1
SPA SNA SZL	7570	1	Skip if AC is positive, nonzero and if LINK is zero
CLA	7600	2	Clear accumulator
LAS	7604	2, 3	Load accumulator from switch register
SZA CLA	7640	1, 2	Skip if AC=0000, then clear AC
SNA CLA	7650	1, 2	Skip on non-zero accumulator, then clear AC
SMA CLA	7700	1, 2	Skip on minus AC, then clear AC
SPA CLA	7710	1, 2	Skip on positive AC, then clear AC

Group 3 Operate Instructions

If bits 6, 8, 9 or 10 are set to a one, instruction execution is not altered but the instruction becomes uninterruptable by either panel or normal interrupts. That is, the next instruction is guaranteed to be fetched barring a reset, $\overline{\text{DMAREQ}}$ or RUN/$\overline{\text{HLT}}$ flip flop in the HLT state.

Group 3 Operate Instructions

All group 3 instructions require 6 minor cycles.

MICROINSTRUCTION FORMAT

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	1	CLA	MQA	*	MQL	*	*	*	1

Logical Sequence:
1 – CLA
2 – MQA, MQL
3 – ALL OTHERS
* – CAUSES INSTRUCTION TO IGNORE INTERRUPTS IF A "1"

BIT 4	5	7	
0	0	0	NOP
0	0	1	AC→MQ, O→AC
0	1	0	(MQ + AC)→AC
0	1	1	MQ→AC
1	0	0	0→AC
1	0	1	0→AC: 0→MQ
1	1	0	MQ→AC
1	1	1	MQ→AC, 0→MQ

+ denotes logical OR

Mnemonic	Opcode	Logical Sequence	Operation
NOP	7401	3	No operation
MQL	7421	2	MQ register load – the MQ is loaded with the contents of the AC and the AC is cleared. The original contents of the MQ is lost.
MQA	7501	2	MQ "OR" with accumulator – the contents of the MQ is "OR"ed with the contents of the AC, and the result left in the AC. The MQ is not modified.
SWP	7521	3	Swap contents of AC and MQ – the contents of the AC and MQ are exchanged
CLA	7601	1	Clear accumulator
CAM	7621	3	Clear AC and MQ (actually a CLA MQL)
ACL	7701	3	Load AC with contents of MQ
CLA SWP	7721	3	Clear AC, then swap – the MQ is loaded into the AC; 0000 is loaded into the MQ

Stack Operation Instructions

The following IOT instructions are internally decoded to perform stack operations using internal stack pointers SP1 and SP2. These are internal IOT instructions; the $\overline{\text{LXDAR}}$ signal is not generated. If instructions are being fetched from main memory, the stacks are located in field 0 of main memory. If instructions are being fetched from panel memory, the stacks are located in field 0 of panel memory, except for the case of a ReTurN from control panel memory via a RTN1 or RTN2 instruction. In this case, the main memory stack is accessed by the instruction fetched from panel memory. Two separate stacks may be maintained – one for the PC, the second for the AC. An increment of the stack pointer is defined as a pop off the stack.

Mnemonic	Opcode	Operation
PPC1	6205	PUSH PC ON STACK. The contents of the PC are incremented by one and the result is loaded into the memory location pointed to by the contents of SP1. SP1 is then decremented by 1.
PPC2	6245	PUSH PC ON STACK. The same as PPC1 except that SP2 is used as the memory pointer.
PAC1	6215	PUSH AC ON STACK. The contents of the AC is loaded into the memory location pointed to by the contents of SP1. The contents of SP1 is then decremented by 1.
PAC2	6255	PUSH AC ON STACK. The same as PAC1 except that SP2 is used as the memory pointer.
RTN1	6225	RETURN. The contents of the stack pointer (SP1) is incremented by one. The contents of the Instruction Buffer (IB) is loaded into the Instruction Field (IF) register. If a prior PEX instruction was executed, the Control Panel Flip Flop (CTRLFF) is cleared. If the Interrupt Inhibit Flip Flop (IIFF) is set, then the Force Zero (FZ) flag is cleared. The contents of the memory location pointed to by SP1 is loaded into the PC. Prior PEX is cleared.
RTN2	6265	Same as RTN1 except that SP2 is used as the stack pointer.
POP1	6235	The contents of SP1 is incremented by 1. The contents of the memory location pointed to by SP1 is then loaded into the AC.
POP2	6275	Same as POP1 except that SP2 is used as the stack pointer.
RSP1	6207	The contents of SP1 is loaded into the AC.
RSP2	6227	The contents of SP2 is loaded into the AC.
LSP1	6217	The contents of the AC is loaded into SP1. The AC is cleared.
LSP2	6237	The contents of the AC is loaded into SP2. The AC is cleared.
CAUTION: When switching between main and control panel memory, the stack pointers must be saved and restored.		

Internal Control Instructions

Note that these instructions apply if the 6120 is executing instructions from main memory or control panel.

<table>
<tr><th>Mnemonic</th><th>Opcode</th><th>Operation</th></tr>
<tr><td>ION</td><td>6001</td><td>Turn on interrupt system. The Interrupt Enable Flip Flop is set. Neither $\overline{\text{INTREQ}}$ or any control panel request will be granted until after execution of the next instruction. (6 minor cycles.)</td></tr>
<tr><td>IOF</td><td>6002</td><td>Turn off interrupt. The interrupt enable flip flop is cleared immediately. If $\overline{\text{INTREQ}}$ is low while this instruction is being processed, the interrupt will not be recognized. (6 minor cycles.)</td></tr>
<tr><td>RTF</td><td>6005</td><td>Load the following from the AC:
<table>
<tr><th>AC bit</th><th>To</th></tr>
<tr><td>0</td><td>LINK</td></tr>
<tr><td>1</td><td>GT</td></tr>
<tr><td>4</td><td>IEFF</td></tr>
<tr><td>6-8</td><td>IB</td></tr>
<tr><td>9-11</td><td>DF</td></tr>
</table>
The IIFF is set. The AC is cleared following the load operation. (8 minor cycles.)</td></tr>
<tr><td>SGT</td><td>6006</td><td>Skip if the GT flag is set. (7 minor cycles.)</td></tr>
<tr><td>CAF</td><td>6007</td><td>The AC, LINK and GT flag are cleared. Interrupt enable flip flop is cleared. $\overline{\text{IOCLR}}$ is generated with $\overline{\text{LXDAR}}$ high, causing peripheral devices to clear their flags. (7 minor cycles.)</td></tr>
<tr><td>WSR</td><td>6246</td><td>Write to switch register. The contents of the AC are written to an external device using a special I/O transfer. The AC is then cleared. The contents of the DF are available for device selection. DATAF is asserted. (7 minor cycles.)</td></tr>
<tr><td>GCF</td><td>6256</td><td>Get current fields. The following bits are loaded into the AC:
<table>
<tr><th>AC bit</th><th>Function</th></tr>
<tr><td>0</td><td>LINK</td></tr>
<tr><td>1</td><td>GT flag</td></tr>
<tr><td>2</td><td>1 if $\overline{\text{INTREQ}}$ is low
0 if $\overline{\text{INTREQ}}$ is high</td></tr>
<tr><td>3</td><td>PWRON flag</td></tr>
<tr><td>4</td><td>IEFF</td></tr>
<tr><td>5</td><td>0</td></tr>
<tr><td>6-8</td><td>IF 0-2</td></tr>
<tr><td>9-11</td><td>DF 0-2</td></tr>
</table>
(9 minor cycles.)</td></tr>
</table>

Main Memory Control Instructions

Note that these instructions apply only if the 6120 is executing instructions from main memory.

Mnemonic	Opcode	Operation
SKON	6000	Skip if interrupt on, and turn off interrupt system. (7 minor cycles.)
SRQ	6003	Skip if the device interrupt line is low. Note that this skip does not depend on the state of the memory extension control's interrupt inhibit flip flop. The SRQ merely tests the state of the $\overline{\text{INTREQ}}$ pin. (7 minor cycles.)
GTF	6004	Get flags. The following bits are loaded into the AC:

AC bit	Function
0	LINK
1	GT flag
2	1 if $\overline{\text{INTREQ}}$ is low 0 if $\overline{\text{INTREQ}}$ is high
3	PWRON flag
4	1
5	0
6-8	ISF 0-2
9-11	DSF 0-2

(9 minor cycles.)

PR0 PR1 PR2 PR3	6206 6216 6226 6236	These four opcodes have the same effect. The PNLTRP is set, causing the 6120 to enter panel mode instead of executing the next instruction, provided the interrupt inhibit flip flop is not set. If the interrupt inhibit flip flop is set, the panel mode will be entered following the JMP, JMS, RTN1 or RTN2 which clears the interrupt inhibit flip flop. These instructions are a NOP in panel mode. (6 minor cycles.)

Panel Memory Control Instructions

The 6120's control panel is implemented in software. The software implementation of the control panel need not use any part of the main memory or change the processor state. This is an important feature, since the final version of the system may not have a control panel and the system designer would like to use the entire capacity of the main memory for the specific system application.

Panel mode is entered because of the occurrence of any of four events. Each of these events sets a status flag, as well as causing the entry into panel mode. It should be noted that more than one event might happen simultaneously.

Flag	Set by	Cleared by
PWRON	$\overline{\text{RESET}}$ low and STRTUP low	PRS and PEX
PNLTRP	PRQ (main memory)	PRS and PEX
HLTFLG	HLT instruction (or any OPR2 instruction with bit 10 a 1)	PGO
BTSTRP	High-to-low transition of $\overline{\text{CPREQ}}$	PRS if BTSTRP was set when status read

Panel mode entry is functionally similar to the granting of an interrupt with some important differences. Entry into panel mode for any reason is inhibited by the interrupt inhibit flip flop. Note that this means that a PRQ or HLT instruction executed when the interrupt inhibit flip flop is set will not be recognized until after the interrupt inhibit flip flop is cleared on the next JMP, JMS, RTN1 or RTN2. Entry into panel mode is also inhibited immediately following the ION instruction but will be recognized after the instruction following the ION is executed.

When a panel request is granted, the PC is stored in location 0000 of the control panel memory and the 6120 resumes operation at location 7777 (octal) of the panel memory. During PC write, 0 appears on C0, C1 and EMA2. The states of the IB, IF, DF, ISF and DSF registers are not disturbed by entry into the control panel mode but execution is forced to commence in field zero. The panel memory would be organized with RAM in the lower pages and ROM or PROM in the higher pages of field zero. The control panel service routine would be stored in the nonvolatile ROMs, starting at 7777 (octal).

A ConTRoL panel Flip Flop, CTRLFF, which is internal to the 6120, is set when the $\overline{\text{CPREQ}}$ is granted. The CTRLFF prevents further $\overline{\text{CPREQ}}$s from being granted, bypasses the interrupt enable system and redefines several of the internal control instructions.

As long as the CTRLFF is set, $\overline{\text{LXPAR}}$ is used for all instruction, direct data and indirect pointer references. Also, while CTRLFF is set, the $\overline{\text{INTGNT}}$ line is held high but the interrupt grant flip flop is not cleared. IOTs executed while CTRLFF is set do not clear the interrupt grant flip flop.

Indirectly addressed data references by control panel AND, TAD, ISZ or DCA instructions reference panel memory or main memory as controlled by a Panel Data Flag (PDF) internal to the 6120. If set, this flag causes indirect references from control panel memory to address control panel memory using $\overline{\text{LXPAR}}$. If cleared, this flag causes indirect references from control panel memory to address main memory using $\overline{\text{LXMAR}}$.

The PDF is cleared unconditionally whenever the panel mode is entered for any reason. It is also cleared by an instruction called CPD (Clear Panel Data). The PDF is set by an instruction called SPD (Set Panel Data). The state of the Panel Data flag is ignored when not operating in panel mode.

Extended memory operations are implemented for panel mode instructions by a 1-bit flag in the EMA logic (the Force Zero – FZ – flag). This flag is always set when panel mode is entered and before the first panel mode memory operation (the store of the PC at control panel memory location 0000). As long as the FZ flag is set, zero appears on C0, C1 and EMA2 in place of the IF except for special C0, C1, EMA2 contents defined during write intervals, which remain undisturbed by FZ being set. The IF remains unchanged, however, and may be read by the RIF instruction. The data field is unaffected by the FZ flag and functions as defined above, using the panel data flag to determine whether operands are in main or control panel memory. In particular if FZ=0:

Control panel instruction fetch is to control panel field 0.

Control panel indirect address fetch is to control panel field 0.

Control panel current page or page zero direct data operations are to control panel field 0.

Control panel indirect data operations are specified by DF. Main or control panel memory access is specified by the panel data flag.

The FZ flag is cleared in panel mode simultaneously with the (IF)←(IB) transfer following the first panel mode instruction which may change the IF. These instructions are CIF (62X2), CDF CIF (62X3), RTF (6005), and RMF (6244). The (IF)←(IB) transfer (and hence the FZ clear) takes place during the first JMP, JMS, RTN1, or RTN2 following the instruction. Once the FZ flag is cleared, the EMA logic operates in control panel memory as it does in main memory with the exception that the panel data flag controls whether indirect data operations are to control panel or main memory. In particular:

Control panel instruction fetch is specified by IF.

Control panel indirect address fetch is specified by IF.

Control panel current page or page zero data operations are specified by IF.

Control panel indirect data operations are specified by DF. Main or control panel memory access is specified by the panel data flag.

Once the FZ flag is cleared in panel mode, it is not set until panel mode is entered again. The state of the FZ flag when not in panel mode is a "don't care".

Exiting from the control panel routine is normally achieved by executing the following sequence:

```
PEX
JMP I 0000   /location 0000 in control panel memory
```

The second instruction in this sequence may be any JMP, JMS, RTN1 or RTN2 instruction. The use of JMS is not recommended, since the programmer has no means of preserving the FZ and panel data flags.

The PEX instruction will cause the next JMP, JMS, RTN1 or RTN2 instruction to reset the CTRLFF. Location 0000 in the control panel memory contains either the original return address deposited by the 6120 when the control panel routine was entered or it may be a new starting address defined by the control panel routine. The IF and DF registers may also contain their original field designations or may have been altered by the control panel routine. If an exit is made from the control panel routine with the HLTFLG set, one instruction is executed in main memory before control panel mode is reentered due to the HLTFLG being set. Note that this allows a software-controlled single step operation of programs in main memory. Caution: Single step operation will not occur for any uninterruptable instructions or any instructions which set the IIFF. Exiting from a control panel routine can also be achieved by activating the $\overline{\text{RESET}}$ line, since reset has a higher priority than control panel request. If the RUN/$\overline{\text{HLT}}$ line is pulsed while the 6120 is in the panel mode, the 6120 will halt at the completion of the current instruction.

Panel Mode Control Instructions

Note that these instructions apply only if the 6120 is executing instructions from Control Panel Memory

<table>
<tr><th>Mnemonic</th><th>Opcode</th><th>Description</th></tr>
<tr><td>PRS</td><td>6000</td><td>Read panel status bits into AC0-4, 0 into remainder of AC.
The bits are read as follows:
<table>
<tr><th>AC bit</th><th>Function</th></tr>
<tr><td>0</td><td>BTSTRP</td></tr>
<tr><td>1</td><td>PNLTRP</td></tr>
<tr><td>2</td><td>1 if $\overline{\text{INTREQ}}$ is low
0 if $\overline{\text{INTREQ}}$ is high</td></tr>
<tr><td>3</td><td>PWRON</td></tr>
<tr><td>4</td><td>HLTFLG</td></tr>
<tr><td>5-11</td><td>0</td></tr>
</table>
Following the reading of the flags into the AC, the flags are cleared, with the exception of HLTFLG. BTSTRP is cleared only if a 1 was read into AC0. (8 minor cycles).</td></tr>
<tr><td>PG0</td><td>6003</td><td>Reset the HLTFLG flip flop. (6 minor cycles).</td></tr>
<tr><td>PEX</td><td>6004</td><td>Exit from panel mode into main memory at the end of the next JMP, JMS, RTN1 or RTN2 instruction. Clear PWRON and PNLTRP. (6 minor cycles).</td></tr>
<tr><td>CPD</td><td>6266</td><td>Clear Panel Data Flag (PDF). Clears the panel data flag so that indirect data operands of panel mode instructions are obtained from main memory. The panel data flag is also cleared upon entry into panel memory. (5 minor cycles).</td></tr>
<tr><td>SPD</td><td>6276</td><td>Set panel data flag. Sets the panel data flag so that indirect data operands of panel mode instructions are obtained from panel memory. (5 minor cycles).</td></tr>
</table>

Memory Extension Instructions

Most memory extension instructions require 6 minor cycles, except for RIB which requires 9 minor cycles.

The internal memory extension control extends the basic 4K addressing structure of the 6120 to 32K. It does so by appending three high-order bits to the memory address. These bits, which appear on C0, C1 and EMA2 lines, apply to addresses within main memory or control panel memory. The changing of memory fields is accomplished via internal control instructions.

The Instruction Field (IF) serves as an extension to the PC, providing three high-order bits during instruction fetches. Note that there is no carry from the most-significant PC bit into the IF. The IF is also used for directly-addressed operands, and for indirect address pointers.

The Data Field (DF) serves to extend the address of indirectly addressed operands, external IOTs, OSR and WSR functions.

The Instruction Save Field and Data Save Field are used to retain the contents of the IF and the DF which existed prior to an interrupt.

Mnemonic	Opcode	Operation
CDF	62X1	Change Data Field to X. X is loaded into DF.
CIF	62X2	Change Instruction Field to X. X is loaded into IB, and the IIFF is set. (The set state IIFF causes the priority network to ignore interrupt requests). The contents of IB are loaded into the IF at the end of the next JMP, JMS, RTN1 or RTN2 instruction. At the same time the interrupt inhibit flip flop is cleared.
CDF CIF	62X3	A microprogrammed combination of CDF and CIF. Both fields are set to X.
RDF	6214	Load the contents of the Data Field register into bits 6-8 of the AC. DF0-2 goes to AC6-8 respectively. AC0-5 and 9-11 are unchanged.
RIF	6224	Load the contents of the Instruction Field register into bits 6-8 of the AC. IF0-2 goes to AC6-8 respectively. AC0-5 and 9-11 are unchanged.
RIB	6234	Load the contents of the ISF and DSF into bits 6-11 of the AC. ISF0-2 goes to AC6-8 and DSF0-2 goes to AC9-11 respectively. AC0-5 are unchanged.
RMF	6244	Load the contents of ISF into IB, DSF into DF, and set the interrupt inhibit flip flop. This instruction is used to restore the contents of the memory field registers to their values before an interrupt occurred.

Input/Output Instructions

Input/output transfer instructions, which have an opcode of 6, are used to initiate the operation of peripheral devices and to transfer data between peripherals and the 6120. Three types of data transfer may be used to receive or transmit information between the 6120 and one or more peripheral I/O devices. Programmed data transfer provides a straight-forward means of communicating with relatively slow I/O devices, such as teletypes, cassettes, card readers and CRT displays. Interrupt transfers use the interrupt system to service several peripheral devices simultaneously, on an intermittent basis, permitting computational operations to be performed concurrently with I/O operations. Both programmed data transfers and program interrupt transfers use the accumulator as a buffer, or storage area, for all data transfers.

IOT INSTRUCTION FORMAT

Bits 0-2 are always set to 6 (110) to specify an IOT instruction. The next six bits, 3-8, contain the device selection code that determines the specific I/O device for which the IOT instruction is intended. Device selection codes 00 and 2X specify internal operations, and may not be used by external devices. Up to 55 I/O devices can be specified. The last three bits, 9-11, contain the operation specification code that determines the specific operation to be performed. The nature of this operation for any given IOT instruction depends entirely upon the circuitry designed into the I/O device interface (see the 6121 specification).

Programmed data transfer begins when the 6120 fetches an instruction from the memory and recognizes that the current instruction is an external IOT. The 6120 sequences the IOT instruction through an execute phase. Bits 0-11 of the IOT instruction are placed on DX0-11; the data field is placed on C0, C1 and EMA2; and $\overline{\text{DATAF}}$ is asserted. $\overline{\text{LXDAR}}$ then falls, signalling the beginning of the IOT execute phase. These bits must be latched in an external register, since they are then removed to free the DX bus for I/O data exchanges. Following the fall of $\overline{\text{LXDAR}}$, the 6120 generates a write signal. During the $\overline{\text{WRITE}}$, the 6120 reads the $\overline{\text{SKIP}}$, C0 and C1 lines. $\overline{\text{SKIP}}$, C0, and C1 define the type of I/O operation. If C1 is pulled low during the write signal, then the 6120 adds one minor cycle and performs a read operation after the write.

The control line $\overline{\text{SKIP}}$, when low during the write portion of an IOT, causes the 6120 to skip the next instruction. This feature is used to sense the status of various signals in the device interface. The C0 and C1 lines are treated independently of the $\overline{\text{SKIP}}$ line.

Programmed I/O Control Lines

External programmed data transfers require 10 minor cycles if there is a read, 9 if not.

Control Lines C0	C1	Operation	Description
High	High	(Device)←(AC)	The contents of the AC is sent to the device.
Low	High	(Device)←(AC), CLA	The contents of the AC is sent to the device; then the AC is cleared.
High	Low	(AC)←(AC)V(Device)	Data is received from a device, "OR"ed with the data in the AC, and the result is stored in the AC.
Low	Low	(AC)←(Device)	Data is received from a device and loaded into the AC.

Interrupt Transfer

The program interrupt system may be used to initiate programmed data transfers in such a way that the time spent waiting for device status is greatly reduced. It also provides a means of performing programmed data transfers between the 6120 and peripheral devices while executing another program. This is accomplished by isolating the I/O handling routines from the mainline program and using the interrupt system to ensure that these routines are entered only when an I/O device is set, indicating that the device is actually ready to perform the next data transfer.

The interrupt system allows external conditions to interrupt the computer program (which must be in main memory) by driving $\overline{\text{INTREQ}}$ low. If no internal higher priority requests are outstanding and the interrupt system is enabled, the 6120 grants the device interrupt at the end of the current instruction. After an interrupt has been granted, the interrupt enable flip flop in the 6120 is reset so that no more interrupts are acknowledged until the interrupt system is re-enabled under program control.

The interrupt inhibit flip flop prevents interrupts (both device and control panel) from occurring when there is a possibility that the IF is not equal to the IB. More specifically, the interrupt inhibit flip flop is set whenever the IB is loaded (i.e., by the instructions CIF, CDF CIF, RMF or RTF), and cleared whenever the IF is loaded from the IB (i.e., at the proper phase of JMP, JMS, RTN1 or RTN2 instructions). Device interrupts are recognized only if the interrupt system is enabled, the interrupt inhibit flip flop is cleared and $\overline{\text{INTREQ}}$ is low.

Upon recognition of an interrupt, the 6120 stores the PC in location 0000 of field 0 and clears the interrupt enable flip flop. Zero appears on C0, C1 and EMA2 when the PC is stored. At the same time, $\overline{\text{INTGNT}}$ goes low. During the interrupt grant sequence, IF is loaded into ISF and DF is loaded into DSF. IF, IB and DF are then cleared. The next instruction is fetched from location 0001 of main memory field 0. $\overline{\text{INTGNT}}$ remains low until the trailing edge of the first $\overline{\text{LXDAR}}$ generated by a main memory IOT following the recognition of the interrupt. The granting of an interrupt requires 4 minor cycles. If a control panel interrupt is granted while $\overline{\text{INTGNT}}$ is low, $\overline{\text{INTGNT}}$ will be forced high as long as CTRLFF is set but will return to the low state when CTRLFF is cleared.

Direct Memory Access

Direct memory access, sometimes called data break, is the preferred form of data transfer to use with high-speed storage devices such as magnetic disk or tape units. The DMA mechanism transfers data directly between memory and peripheral devices. The 6120 is involved only in setting up the transfer; the transfers take place with no 6120 intervention on a "cycle stealing" basis. The DMA transfer rate is limited only by the bandwidth of the memory and the data transfer characteristics of the device.

The external device generates a DMA request when it is ready to transfer data. The 6120 grants the $\overline{\text{DMAREQ}}$ by pulling the DMAGNT signal high at any point in any of the instructions, or between instructions, when the 6120 is not using the DX bus in performing a bus read, write or read-modify-write operation. The 6120 suspends its internal timing until the $\overline{\text{DMAREQ}}$ line is high. The DX lines, EMA2, C0 and C1 lines are tristated. $\overline{\text{LXPAR}}$, $\overline{\text{LXMAR}}$, $\overline{\text{MEMSEL}}$, $\overline{\text{OUT}}$, $\overline{\text{READ}}$ and $\overline{\text{WRITE}}$ are all held high by a device on each of these lines which only has a very small pull-up drive. These lines can then be pulled down by an external device. In this way, these control lines are stable until the external device can gain control of them. $\overline{\text{IFETCH}}$ and $\overline{\text{LXDAR}}$ are both held high. $\overline{\text{RUN}}$ is held low. The states of $\overline{\text{DATAF}}$ and $\overline{\text{INTGNT}}$ are undisturbed.

The external DMA device must not drive the bus until DMAGNT is high. The DMA device must:

a. Drive all signals with three-state devices.
b. Provide all address, data, $\overline{\text{LXPAR}}$, $\overline{\text{LXMAR}}$, and other control signals with the proper timing.
c. Return all control lines to the high state before relinquishing the bus.
d. Three-state all drivers at or before $\overline{\text{DMAREQ}}$ is pulled high by the device.

After the $\overline{\text{DMAREQ}}$ line is pulled high, the 6120 negates DMAGNT and re-establishes proper timing before proceeding.

Internal Flags

Name	Set Conditions	Clear Conditions	Load Conditions	Comments
IEFF	ION inst.	1. $\overline{\text{RESET}}$=low 2. IOF inst. 3. During $\overline{\text{INTGNT}}$ sequence 4. SKON inst.	RTF inst.	INTERRUPT ENABLE FLIP FLOP: Tested by the SKON instruction. GCF inst. loads state of IEFF into AC4. $\overline{\text{INTREQ}}$ is honored only if IEFF is set (1).
IIFF	1. CIF inst. 2. CIF CDF 3. RMF 4. RTF	1. $\overline{\text{RESET}}$=low 2. JMP, JMS, RTN inst.	none	INTERRUPT INHIBIT FLIP FLOP: Suppresses any $\overline{\text{INTREQ}}$ or Control Panel mode request.
CTRLFF	Upon entry into panel mode	1. $\overline{\text{RESET}}$=low 2. Next JMP, JMS or RTN after PEX inst.	none	CONTROL PANEL FLIP FLOP: Indicates control panel operation. Interrupts are not honored when set.
FZ	Upon entry into panel mode	First JMP, JMS or RTN inst. executed with IIFF set.	none	FORCE ZERO FLAG: Forces control panel instruction field access to field zero. Indirect data accesses are not affected.
PDF	SPD inst.	1. Panel mode entry 2. CPD inst.	none	PANEL DATA FLAG: When set causes indirect data operations executed in control panel to access CP memory. Otherwise they are to main memory. PDF is ignored when executing in main memory.
RUNHLT	$\overline{\text{RESET}}$=low	none	On the low to high transition of the RUN/HLT line	RUN HALT FLIP FLOP: When cleared the 6120 will halt after the first instruction in which this state is detected. The 6120 will respond to $\overline{\text{DMAREQ}}$ in this state.
HLTFLG	HLT inst.	1. $\overline{\text{RESET}}$=low 2. PG0 inst.	none	HALT FLAG: When set, panel mode will be entered unless the IIFF is set or $\overline{\text{RESET}}$ is low. IIFF can be cleared on the next JMP, JMS or RTN instruction at which point panel mode will be entered.
PNLTRP	PR0, PR1, PR2, PR3 inst. (main only)	1. $\overline{\text{RESET}}$=low 2. PRS inst. 3. PEX inst.	none	PANEL TRAP FLAG: Same result as defined for HLTFLG.
BTSTRP	High to low transition of $\overline{\text{CPREQ}}$	1. $\overline{\text{RESET}}$=low 2. PRS inst.	none	BOOTSTRAP FLAG: Same result as defined for HLTFLG.
PWRON	$\overline{\text{RESET}}$ and STRTUP=low	1. $\overline{\text{RESET}}$ and STRTUP=high 2. PRS inst. 3. PEX inst.	none	POWER-ON FLAG: Causes entry into panel mode when $\overline{\text{RESET}}$ is released and this flag is set.
GT	none	$\overline{\text{RESET}}$=low	RTF inst.	GREATER THAN FLAG: General purpose flag which has no arithmetic significance.