PDP-9

Programmed Data Processor general purpose computer
Parallel, Binary with 18 Bit word fixed word length
8K - (8192) 18 Bit words 2½D type core
Single address
1.75 cycle time (complete memory cycle)

Standard peripherals
PTR - Paper Tape - PC02 300 lins/sec 8 level
can read alpha or Binary 1 line alph (8 Bits)
3 lines Binary (6 Bits)
Punch PC03 - 50 lines/sec also alpha or binary

Combined PC09

TTY Keyboard INPUT 10 CAR/sec
OUTPUT 10 CAR/sec

RTC - real time clock - 60 CPS counter

PI - Program Interupt facility can be turned on or off signal central processor when peripheral is ready (flag)

DMA - Direct Memory Access

switch to central processor or DMA to other computer

DCH - Data channel - entry port for peripheral to communicate med. speed - not built to know where to put, or how many or where from (Dec Tape)

Data channel break 3 or 4 cycles

2 memory locations are reserved DCH # 1 30 — # word ct
2. 31 CA CURRENT ADD.
CA + 1
3. STORE WORD

Dec Tape 200 ms to get ready

Registers

AC - Accumulator 18 Bit register main arithmetic register result end up here also contains 1 operand
I/O register program controlled
MB — Memory Buffer - 18 stage register

MA - Memory Address Location in core 13 bit register 15 bits with additional memory

PC - program counter 13 bit keeps track of address of next instruction sequencing

IR - instruction register 5 bits receive 1st 5 bits of 18 bit instruction

L. LINK 1 bit extension of AC ext. arithmetic capabilities

2 types of arithmetic Two's compliment or one's complement

LINC on ones is add overflow
2's is carry stage

Bit 0 is sign bit if 0 number is +
1 " is — in complimentary form

MR - arithmetic register 18 bit register to help accumulator on key operations is address indicator

Bus transfer system

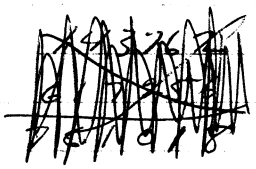
all transfers are transferred through MR to prevent runaway

Instructions SEE Pg 7-1 USERS MANUAL

1. Memory Ref
2. Augmented < Operate / IOT / EAE

I* says that the Referenced Location contains the Address for the operation specified

200 DAC I* 305



octal addition over 7 add 2

613562
046177
661761

AND

Data	001	010	011	000	001	010
∧	111	111	100	000	000	000
	001	010	000	000	000	000

204 LAC 300
205 AND 1000

~~20~~ - 123012
1000 774000

Masking or Extracting

XOR

202 XOR 517

01011 01010
⊕ 01000 10111
00011 11101

if both are same 0
different keep a 1

SAD

Skip next step if accumulator is different from 1000

203 SAD 1000
~~204~~
205

ISZ
303 ISZ 42 add a 1 and skip if Zero
does not affect AC or link

ISZ loop

```
200  XXX
201  XXX
202  XXX
203  XXX
204  ISZ 100 / -10
205  JMP 200
206  HLT
```

10 Decimal is 12 octal 000012

-10 is written 777766

000 000 000 000 001 010

111 111 111 111 110 101

+ 1

111 111 111 111 110 110

$$X = \sqrt{A+B} + \sqrt{C+D} - \sqrt{B+D}$$

C(100) - A
C(101) - B
C(102) - C
C(103) - D
C(104) - $\sqrt{A+B}$
C(105) - $\sqrt{C+D}$
C(106) $\sqrt{B+D}$

```
300  LAC  100 / GET VALUE of A
301  ADD  101 / Sum of A+B
302  JMS  1372 / Go Get √
     ↓ GET Sq Rt.
303  DAC  104  √A+B
304  LAC  102  Get C
305  ADD  103  Sum of C+D
306  JMS  1372 / Go Get √
307  DAC  105
```

√ Sub Routine

```
1372  PC #
  ≀
1422  ~~Go Back to~~
      JMP* 1372
```

JMS 1. must store in referenced location of PC
2. Ref location +1 → PC (+address)

CAL

302 CAL 606 allows extra bits to be fread
JMS 20

XCT

204 XCT 1000
205 ADD 100

1000 LAC 303

CAL $\angle$ PC → 20, "21" → PC

DAC AC → Y

JMS PC → Y, "Y"+1 → PC

DZM 0 → Y

LAC Y → AC

XOR Y ⊻ A → AC

ADD Y + AC → AC
LV OF/O : 1 → L

TAD Y + AC → AC
CO OF 00 : $\bar{L}$ - L

XCT - DO INS IN Y

ISZ Y + 1 → Y
IF Y+1 = 0 THEN PC+1 → PC

AND Y ∧ AC → AC

SAD IF Y ≠ AC : PC+1 → PC

JMP "Y" → PC

Y = CORE MEM LOCATION

Operate Instructions Pg 7-8

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
1	1	1	1	0	CLA	CLL	1 OR 2 PL	0	SNL	SZA	SMA	HLT	RAR	RAL	OAS	CML	CMA
							iF 1 moves 2 PL	1	SZL	SNA	SPA		RTR	RTL			1's comp

OP Code 74_8

Data or Accumulator Switches

AC V DATA Switches → AC (OAS)

EVENT TIMES

1. Sensing of skip conditions take place first
2. bits 5+6
3. bits 16+17
4. " 13+14
5. " 15
6. " 12

LAW 76 + "N" 00000 - 17777
Load AC with "N"

Auto Indexing

Mem Loc 10-17 when addressed indirectly contents will be incremented by 1 before it can be used

```
200 DZM * 13          want to zero 300-350
201 ISZ 04/777747     in 13/000277
202 JMP 200
203 HLT
```

ISZ Auto Indexing

200 ISZ*13

13 = 000 042
42 - 000 172
43 - 777 403

increment location + contents each I

Fetch cycle — at beginning MB contains address of instruction

- 100NS - MBO +1 PCI (Increment PC)
- 120 NS - MA JAM

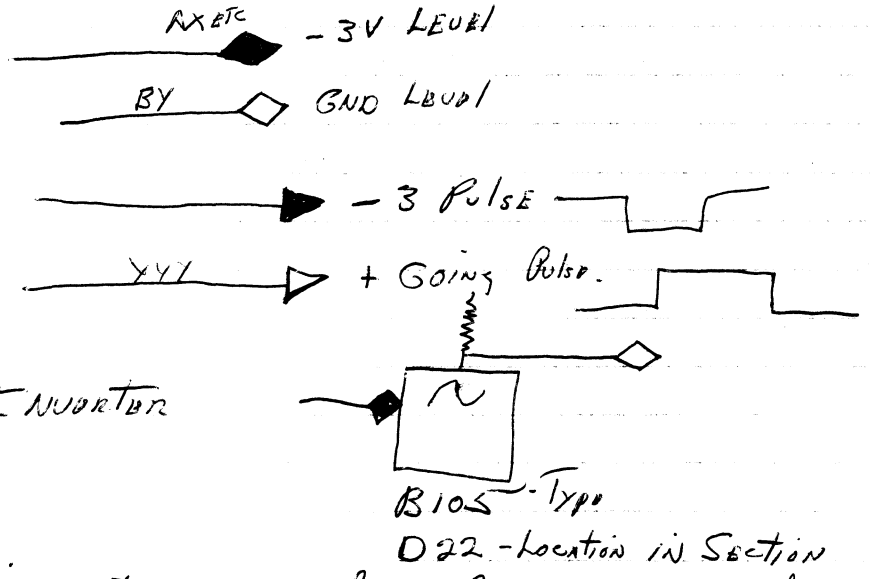
312 NS - AC OUT AR IN

500NS - Memory sends 18 Bit word SA to B Bus to Addr. nothing on A to MOSH to MB also code to IR

765NS - Memory write from MB back in memory

1 us

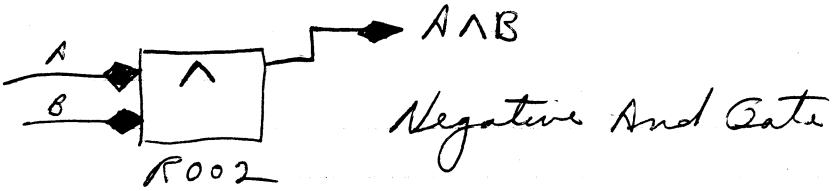
PDP 9 has −3 & ⏚ states

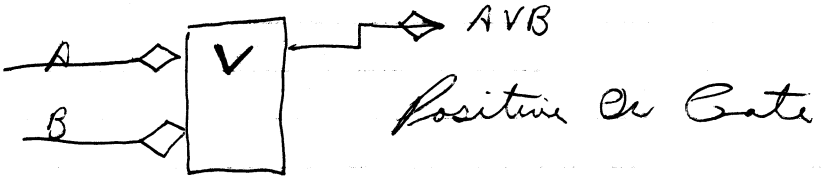


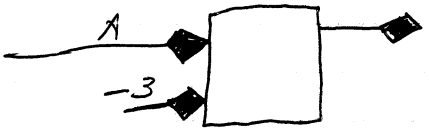
MEMORY MC-70
CENTRAL PROC. KC09-A #
I-O KO-09-A #

inputs can be levels or pulses

Diode Gate



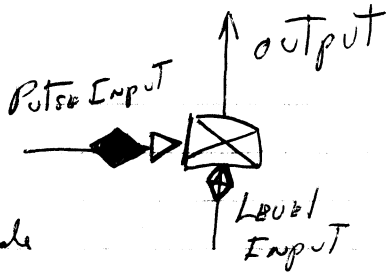




Term left floating = −3

Nand Gate R111 Pin on card mode terminal for expanding
Both inputs neg to get gnd. out

Nor Either input pos get neg −3 out



DCD gate

Diode capacitor Diode

SET { Set by pulse in at -3V
Level must be at + for 400 NS

FIRE — Pulse input goes + then output occurs
enable signal can be removed and output still
can be obtained for 200 NS

Pulse amp. ↑ Transformer coupled
B602
Pos or Neg out Pulse Width 40NS

S602-603 - 2 inputs DCD or strait input
100NS wide
400NS on 602 if D&M Jumper

W612 - Transformer coupled 120NS or 320NS J&K or T&V

Delay Network

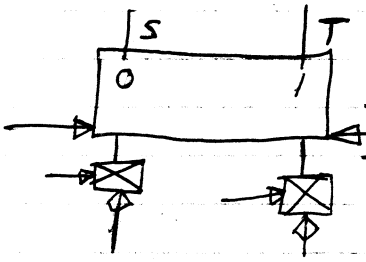
B310 Tapped Delay line inverter on output
12.5NS Taps 15NS delay thru transistor

B302 Single shot neg. out during delay time

B301 One shot, inversion on input neg pulse
level output & pulse output pulse occurs at
end of delay time

B360 - adjustable delay Pos or Neg out
variable delay 40NS pulse

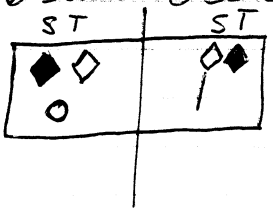
Mixer - B169 or B141 - Has 7 input and gates

Flip-Flop - 

if in zero state clear to -3

Gated Clear into zero state

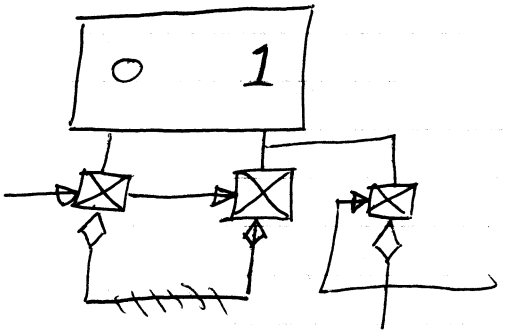
Direct set puts into 1 state
Direct clear puts into 0 state



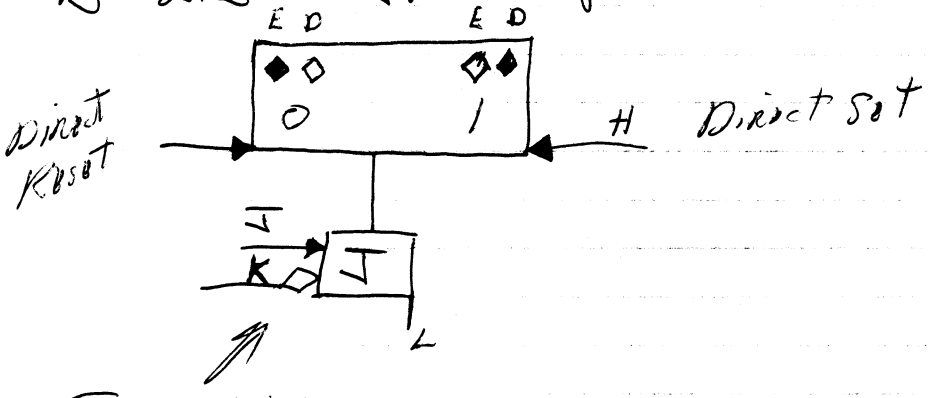
5202

5203 - Only Has DCD gate on 1 side only

5205 Has pulse input common to both sides



B-213 Jam FFlop



To put into 1 state Term J must be neg and if K is positive K is level input

0 state J is negative K negative

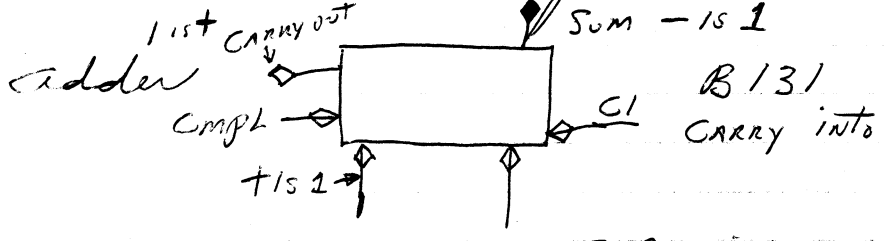
If put or gate on L expanded level input

Buffered means signal has come through inverter to ease loading

PU/KE AFTER JAM PU will end up at same KB same voltage

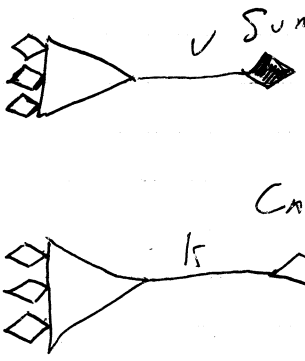
Jam network has 20NS time delay if level is there when Jam comes no delay

B 213 has emitter follower on outputs



true sum output (binary 1 out) an odd # of true inputs

To get carry out 2 or more true inputs



refer to module drawing

if CMPL is present make stage think CIN is present, is only used for logical functions other than ADD

Main Memory

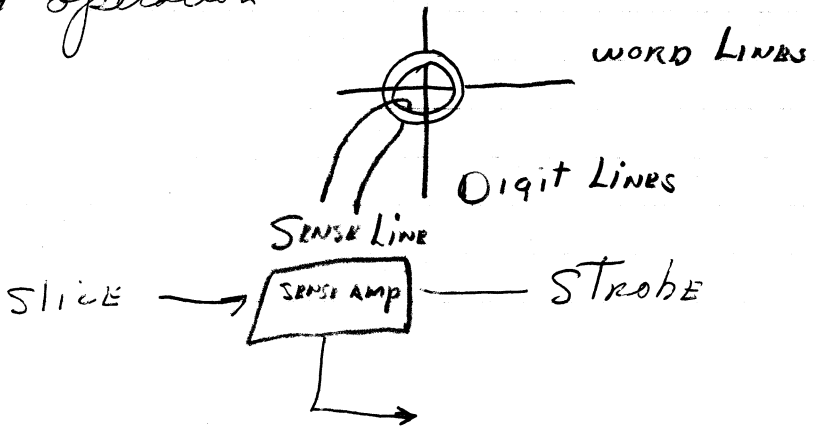
Dec Type MC 708

2½D organization

8K (8192) 18 Bit words

complete memory cycle 1 μs (read modify write)

3D Read operation



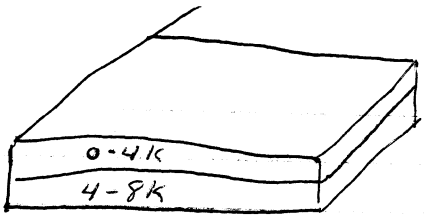
if switches, signal comes out

voltage applied to switch to zero

after reading all cores in 18 bit words are in zero state

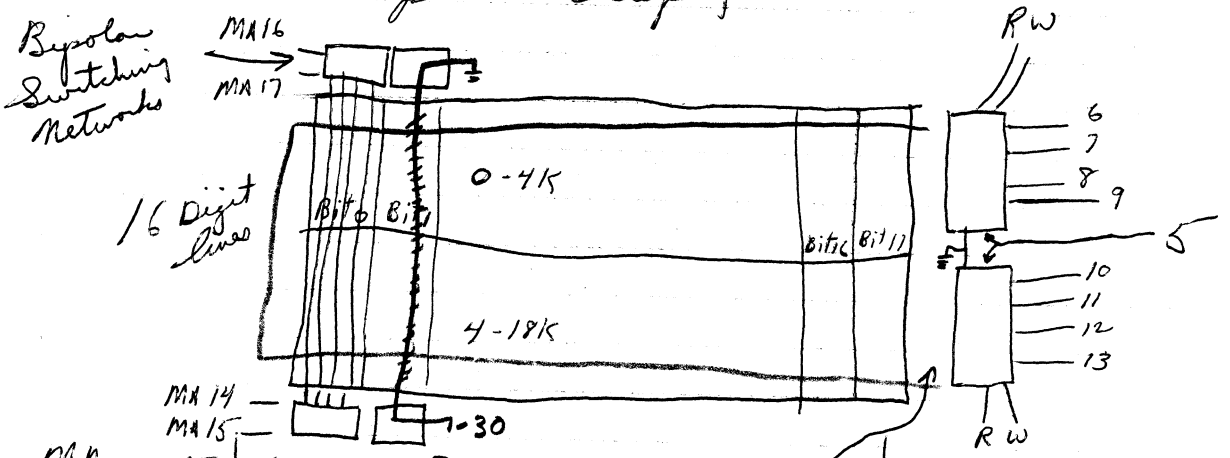
write operation - 2D write reversed current to switch state of core if bit coming out was 1 then switch ½ current is automatically reversed if bit is <u>one</u> ½ current is generated

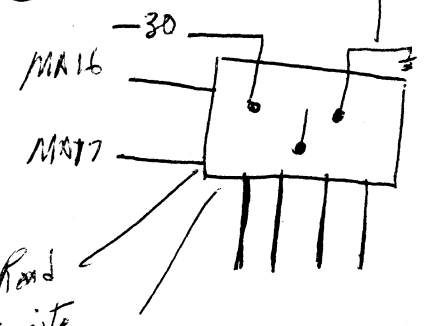
Main Memory Cycle 1 μs for read and write back



Field 0
Field 1

2 sided planer display

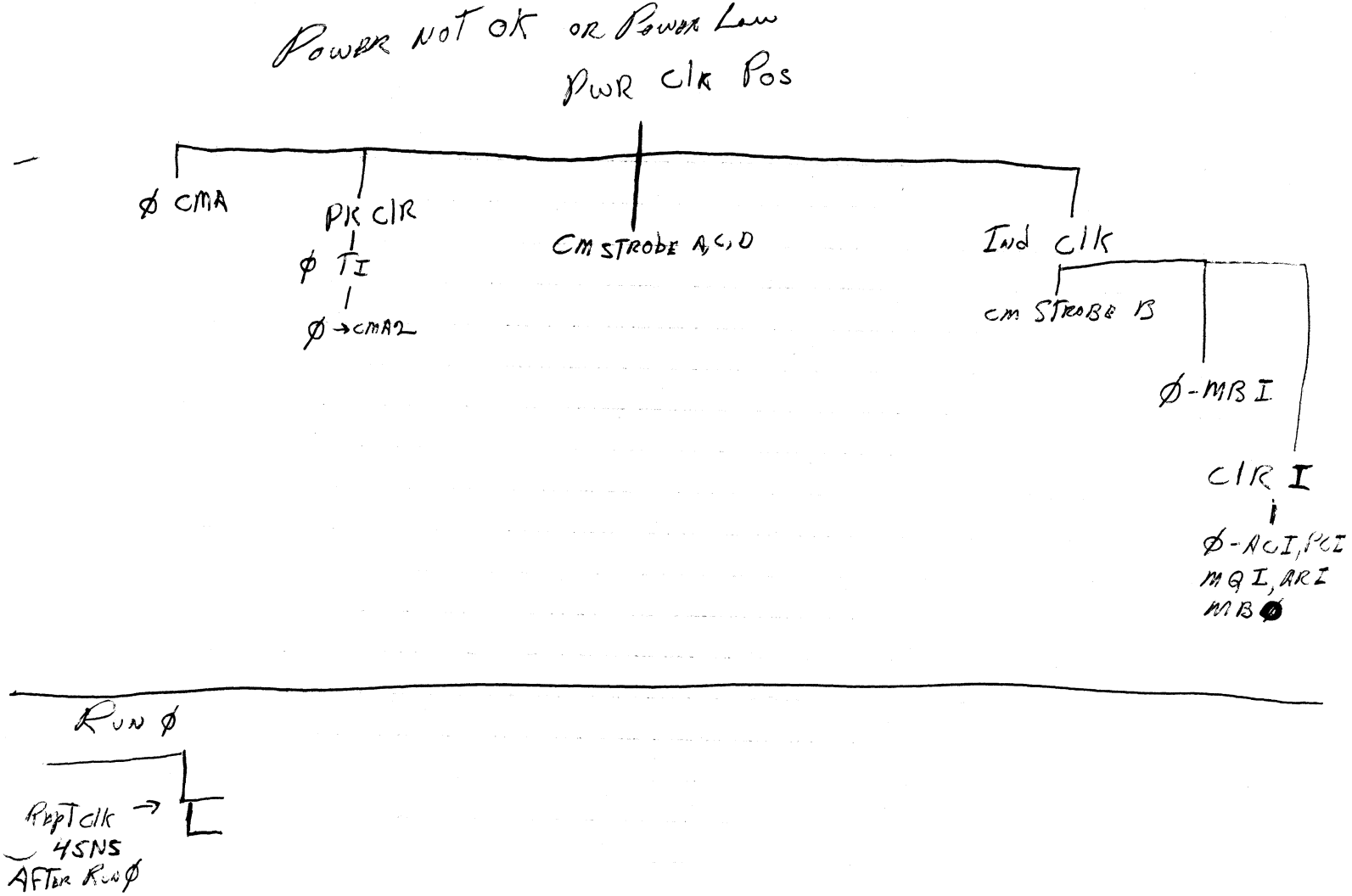




16 Lines out of each
256 Lines

4,096 upper or 4.096 lower

18 Sense amps
MA Bit 5 field selection


Power not OK or Power Low
PWR clk Pos
ø CMA
PK clk
ø TI
ø → CMA2
CM STROBE A, C, D
Ind clk
CM STROBE B
ø - MB I
clk I
ø - ACI, PCI
MQ I, ARI
MB ø
Run ø
RepT clk
45NS
After Run ø

Control Memory

sets up levels to perform operations

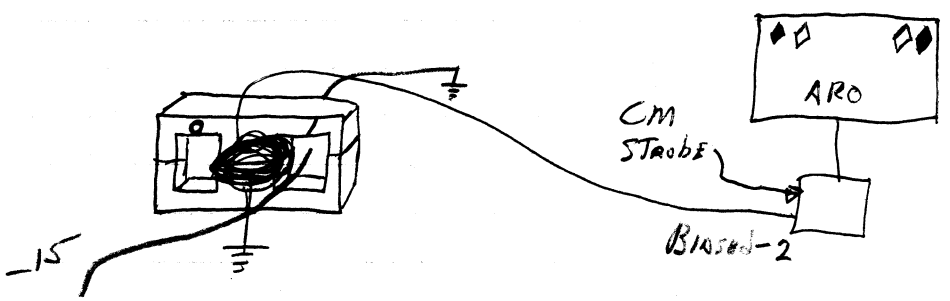
read only, prewired

Addressing locations it wants does not operate sequentially

64(10) addressable locations

each location contains 36 bit 30 Bits - command, 6 bits address bits. tell you where to go next

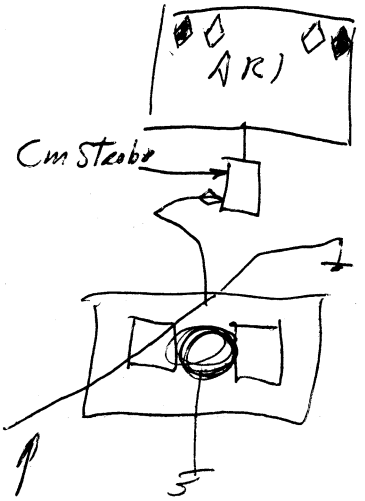
contains 36 cores..!!



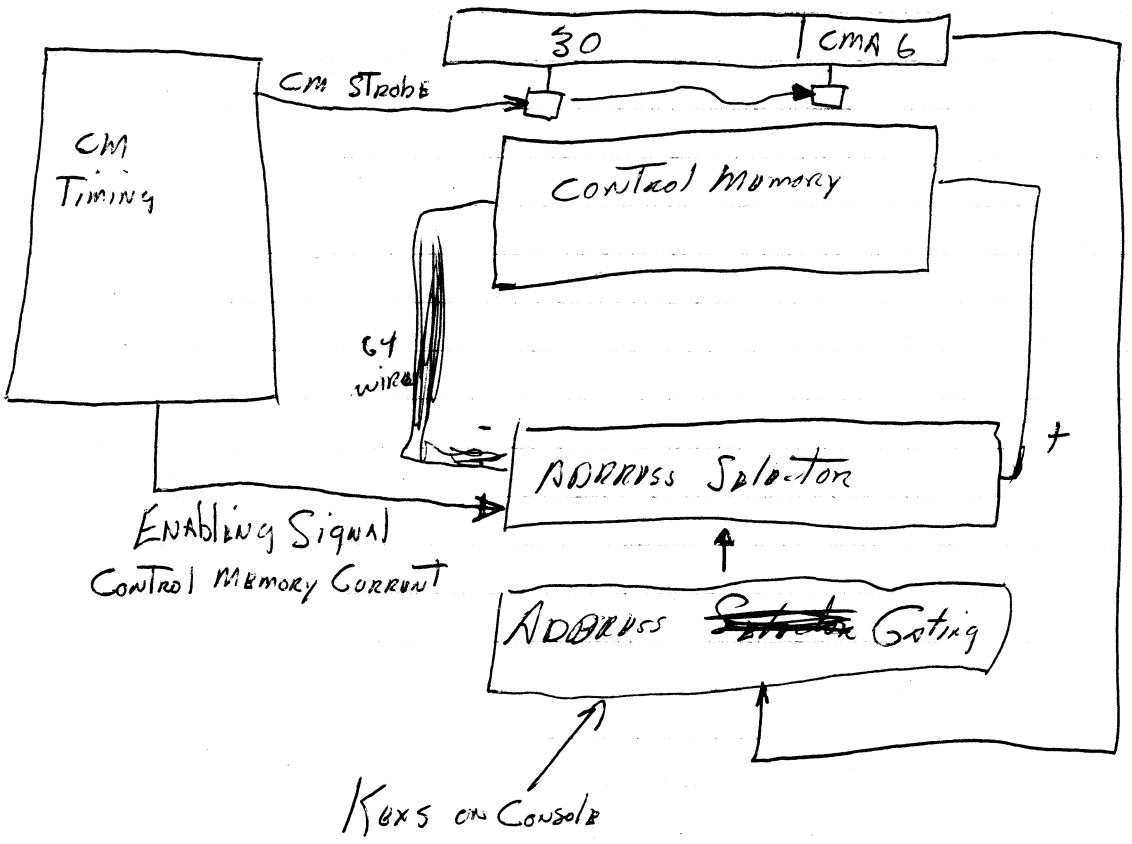
each long 1 each high

each 1 core feeds 1 flip-flop

each core will have 64 lines passing through it



output reversed



CMA

0	1	2	3	4	5
0	1	0	0	0	1

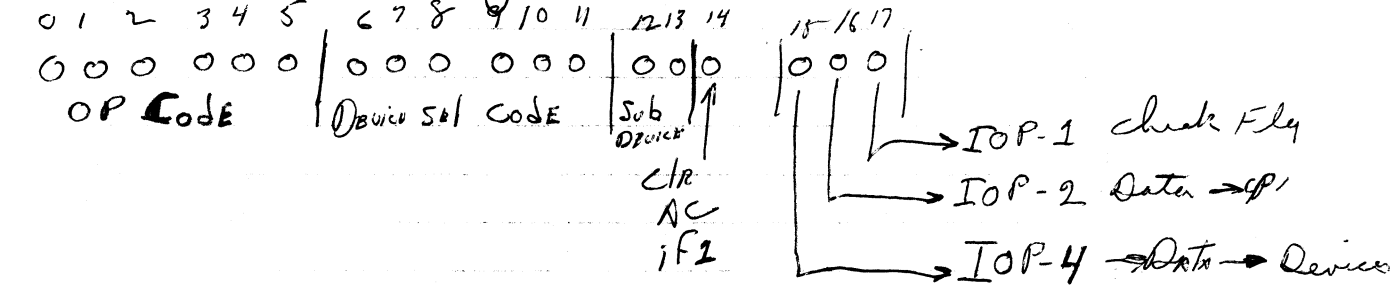
G-210 modules

IORS read flags 700314

0 0 0 0 0 0

Printer Scope

CAF clear all flags 703302
does not clear any controlling FF's



ION - Enables a peripheral to signal when it desires servicing interrupt facility on 700042

IOF 700002 - resets PIE

KSF - Skip on keyboard flag 700301

KRB - 700312 read keyboard buffer to AC 10-17

PCO2 - Reader
PCO3 - Paper tape punch

Punch either binary or alpha - usually ascii in binary & is always punched 7 never punched 1st 6 are bits

Reader - 300 line/sec optical reader completely under program control both alpha or binary mode
Alpha - 1 line of 8 bits
Binary - 3 lines of 6 bits

has 18 bit buffer in computer, must have hole -
8 punched in order to read.
Hardware read in format - Binary

RSB - Select reader in binary mode 700144

Real Time Clock

Main Mem loc 7 is real time clk counter. Increment is stolen with out any program cont. when clock count goes to 0 clock flag is set for program interrupt

ION 700044

Data Channel - provides fast transfer from M. Memory and medium speed peripheral. Flag on device will automatically pull program into break cycle (3 or 4) - Uses word count like real time clk
Reserved for data channels

Data ch 0 → 30 - word count location for determination of how many words
→ 31 - address of 1st word to be read in (current address)
Dec Tape are all tied to ch-0

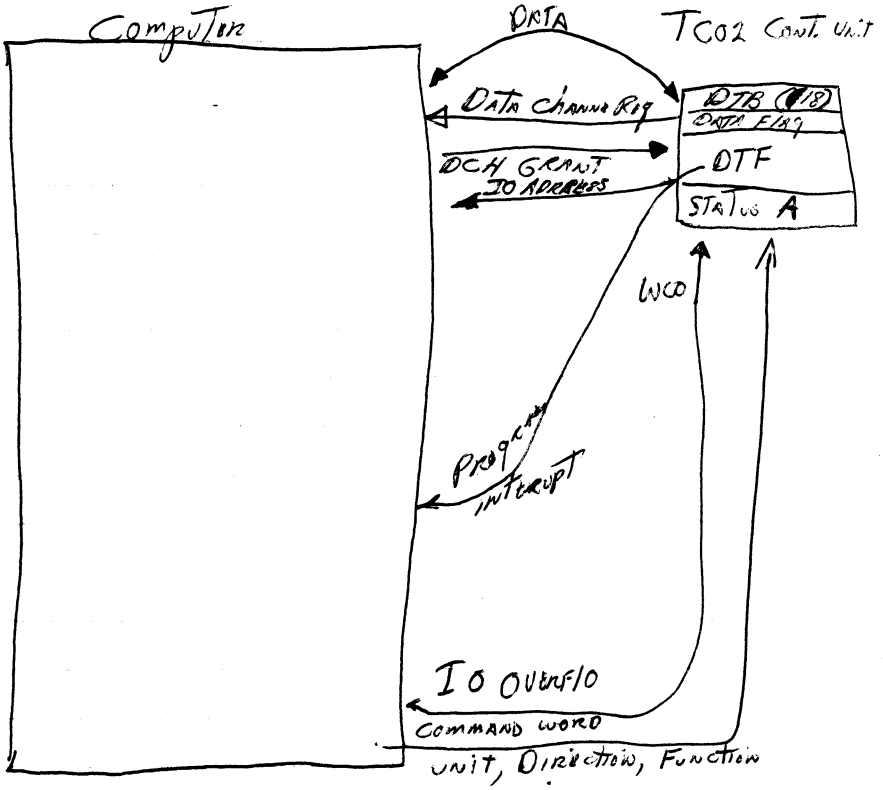
Data ch 1 → 32
→ 33

ch 2 → 34
→ 35

ch 3 → 36
→ 37

Dec Tape - 200 μs can assemble 18 bit word full speed

will handle up to 8 TU55



Add

AR
+MB
AC

carry out of adder 0
= end around carry

carry out of Add 1's compliment add end around carry
On 2's compliment add compliment line

IOT codes

0 1 2 3	4 5	6 7 8 9 10 11	12 13	14	15 16 17
OP Code 70(8)	NOT USED	DEVICE SEL CODE	Sub. Device Sel Mode of Operation	CLA	INPUT OUTputters 1 → IOP(1) Flag Clk → IOP 2 Data Trans To C.R. → IOP-4 DATA To A Device

IOT Pulses