EK-VT240-TM-001

VT240 Series

Technical Manual

digital

EK-VT240-TM-001

VT240 Series

Technical Manual

Prepared by Educational Services
of
Digital Equipment Corporation

1st Edition, August 1984

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This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference to radio and television reception. It has been type tested and found to comply with the limits for a Class B computing device in accordance with the specifications in Subpart J of part 15 of FCC Rules, which are designed to provide reasonable protection against such interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

reorient the receiving antenna
relocate the computer with respect to the receiver
move the computer away from the receiver
plug the computer into a different outlet so that computer and receiver are on different branch circuits.

If necessary, the user should consult the dealer or an experienced radio/television technician for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission helpful:

"How to Identify and Resolve Radio-TV Interference Problems".

This booklet is available from the US Government Printing Office, Washington, DC 20402, Stock No. 004-000-00345-4.

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INTRODUCTION

GENERAL

This manual provides information to help Field Service engineers, and other personnel trained by Digital Equipment Corporation, isolate VT240 Series Terminal malfunctions. This manual documents hardware functions to the major circuit level, identifying the major circuits within the VT240 Series terminal and providing functional descriptions of those circuits.

Summarized operating and programming information is provided where neccessary to understand the functionality of a hardware component or circuit.

MANUAL ORGANIZATION

The first three chapters of this manual introduce the VT240 Series terminal.

Chapter 1 System Introduction -- introduces the VT240 Series terminal.

Chapter 2, Controls, Indicators, and Connectors -- describes all VT240 Series terminal controls, indicators, and connectors.

Chapter 3, System Overview -- provides an overview of the VT240 Series terminal system interactions.

Chapters 4 through 10 identify the major logics that comprise the VT240 Series terminal, and identify and describe the major circuits within those logics.

Chapter 4, CPU Logic -- describes the logic responsible for overall control over VT240 Series terminal operation.

Chapter 5, System Communication Logic -- describes the logic responsible for communication with host and auxiliary devices.

Chapter 6, Video Logic -- describes the logic responsible for developing composite video output to a monitor device.

Chapter 7, LK201 Keyboard -- describes the module responsible for operator input.

Chapter 8, Monochrome Monitor -- describes the module responsible for visual output to the operator.

Chapter 9, -- Power Supply describes the system box power supply responsible for converting ac input to dc potentials needed to operate the terminal.

Chapter 10, Integral Modem -- describes the option responsible for modem communication with a remote host (when installed).

This manual does not provide a technical description of the VR241 color monitor (used with the VT241 terminal). This monitor is described in separate Digital Equipment Corporation publications (refer to Related Documentation).

The final part of this manual is made up of Appendices which provide specifications, differences between terminals, and programming reference data.

Appendix A, Specifications -- provides VT240 Series terminal specifications.

Appendix B, VT240/VT102 Differences -- descrbes the differences between the VT240 Series terminal and VT100 terminal.

Appendix C, VT240/VT125 Differences -- describes the differences between the VT240 Series terminal and VT125 terminal.

Appendix D, Register Bit Values -- provides a summary of bit values for register devices.

Appendix E, Video Logic Write Mode Programming Overview -- provides a summary of the video logic write modes.

RELATED DOCUMENTATION

The following related documents supplement the information in this manual.

VT240 Series Terminal Documentation

VT240 Series Pocket Service Guide	EK-VT240-PS
VT240 Series Programmer's Reference Manual	EK-VT240-RM
VT240 Series Programmer's Pocket Guide	EK-VT240-HR
VT240 Series Owner's Manual	EK-VT240-UG
VT240 Series Installation Guide	EK-VT240-IN
VT240 Series Integral Modem Installation Guide	EK-VT24X-IN
VT240 Series Video Terminal IPB	EK-VT240-IP

VR241-A Series Documentation

VT241-A Series Installation/Owner's Guide	EK-VR241-IN
VT241-A Series Installation Guide	EK-TILSW-IN
VT241-A Series Mini Maintenance Manual	EK-VR241E-PS
VT241-A Series Pocket Service Guide	EK-VR241-PS

Maintenance Print Sets

VT240 (VS240, VR201, LK201)	MP-01807
VS240 (System Box)	MP-01597
VR201 (Monochrome Monitor)	MP-01410
LK201 (Keyboard Module)	MP-01395
VR241 (Color Monitor)	MP-01893

CHAPTER 1
SYSTEM INTRODUCTION

1.1 GENERAL

The VT240 Series terminals are quarter page (up to 24 displayable lines of text) conversational terminals used to create, store, and edit text and graphic images.

The VT240 Series includes either the VT240 or VT241 terminal. These terminals are identical in function. The only difference is that the VT240 has a monochrome monitor (VR201), while the VT241 has a color monitor (VR241).

The VT240 Series terminal uses ANSI standard functions for text processing, and Remote Graphics Instruction Set (ReGIS) standard functions for graphic image processing. In addition, the terminal also has a 4010/4014 mode to support industry-standard Tektronix software packages.

1.2 PHYSICAL DESCRIPTION

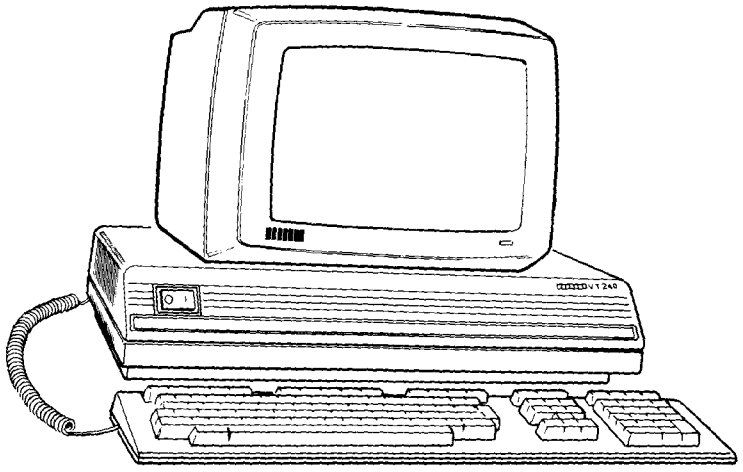
The terminal (Figure 1-1) consists of three units: a monitor, a keyboard, and a system box.

NOTE
Appendix A provides specifications for the VT240 Series terminal.

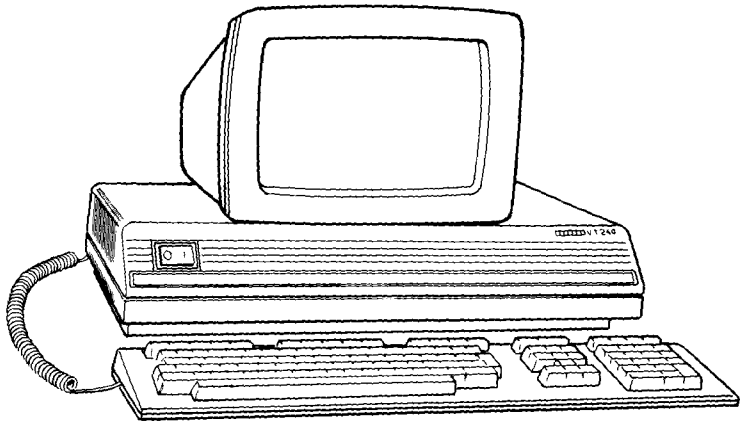
1.2.1 System Box (VS240)

The system box is the center of the terminal. Figure 1-2 shows the major system box components.

- Logic Board -- contains the components needed to control terminal operation.
- Power Supply (PS) Assembly -- converts ac input to the dc voltages required by the terminal.
- Integral Modem -- optional PCB which mounts inside the system box and provides modem functionality for the terminal.



VT241



VT240

MA-1178-83A

Figure 1-1 VT240 Series Video Terminals

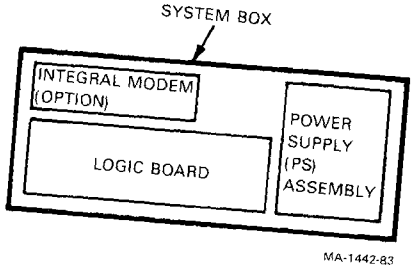


Figure 1-2 VT240 Series Terminal Block Diagram

1.2.2 Keyboard (LK201)

The terminal uses an LK201 keyboard with the following features.

- 4 LEDs -- provide visual indication of operational conditions.
- Typewriter-style Keypad -- contains 57 keys for text entry.
- Auxilliary Keypad -- contains 18 keys, including 4 programmable function keys.
- Editing Keypad -- contains 6 screen function keys, and 4 cursor movement keys.
- Top Row Function Keys -- 20 keys aligned across the top of the keyboard are provided for various functions.

Chapter 2 (Controls, Indicators, and Connectors) provides more detail concerning the functionality of the LK201 keyboard when used with the VT240 Series terminal.

1.2.3 Monitor

The VT240 uses the VR201, a 12-inch monochrome monitor; The VT241 uses the VR241, a 13-inch color monitor.

1.3 DISPLAY CAPABILITIES

Text and graphic image display is done by raster scan of an 800 X 240 picture element (pixel) matrix. The VT240 Series terminal display capabilities are upward compatable with VT102 text capabilities, and with VT125 graphics capabilities. In addition, VT240 Series terminals contain an operational mode that supports industry-standard Tektronix 4010/4014 software packages.

VT240 Series terminals use bit map technology so that each pixel in the 800 X 240 matrix is individually addressable. In addition, two bit maps are used so that each pixel is written and read as a two-bit code, with any given pixel having any one of four different values.

1.3.1 Display Characteristics

The terminal has two basic characteristics that affect both text and graphics modes.

- Screen Integration -- The terminal provides complete integration of text and graphic images within the display matrix
- Display Area -- The terminal's display area is defined by a 2-plane bit map, with an 800 X 240 pixel matrix comprising each plane.

1.3.2 Text Capabilities

The terminal has four text modes. Three modes execute standard ANSI functions (VT100 mode, VT200 mode with seven-bit controls, and VT200 mode with eight-bit controls), and one mode executes Digital private functions (VT52 mode). The following major text capabilities are available within these various modes.

- 24 rows of text with either 80 or 132 characters per row (characters formed within 7 X 9 dot matrix in 10 X 10 cell for 80 characters per row, and within 5 X 9 dot matrix in 6 X 10 cell for 132 characters per row)
- 5 character sets of 94 characters each, including DEC Multinational Character and Special Character Sets
- Down-line loadable character set
- Reverse video
- Underline
- Double-height/double-width characters on a line-to-line basis
- Bold/normal intensity
- Character blinking
- ANSI compatable control functions.

1.3.3 Graphics Capabilities

Graphic images are drawn at the terminal by turning on pixels in patterns that represent points, lines, circles, arcs, and curves, as well as alphanumeric characters (available for graphic images). The terminal's major graphics mode capabilities include:

- ReGIS mode
- 4010/4014 mode
- 95 character ASCII set and 3 programmable character sets (each with up to 95 characters) available for ReGIS text functions
- 64 colors available with any 4 displayable, on a pixel to pixel basis, at a given time (VT241)
- Four monochrome shades displayable, on a pixel to pixel basis, at a given time (VT240).

1.4 COMMUNICATION ENVIRONMENT

The terminal's major communications features include:

- Asynchronous communications at up to 19.2K bits per second
- EIA RS232C host port
- 20 mA host port
- EIA RS232C auxilliary port
- Seven-bit or eight-bit character formats
- Optional integral modem.

1.5 MAJOR OPERATING STATES

The VT240 Series terminal has three major operating states.

- Set-up
- On-line
- Local

Chapter 3 (System Overview) describes the operating states in more detail.

1.6 OPERATING MODES

The VT240 Series terminal has five major operating modes which can be selected either from the keyboard (in set-up), or by the host (via control codes).

- VT100
- VT200, seven-bit controls
- VT200, eight-bit controls
- VT52
- 4010/4014

In addition, you can access a sixth operating mode, ReGIS, by using escape sequences in VT100 or VT200 operating modes.

1.6.1 VT100 Mode

The VT100 mode executes standard ANSI functions. This mode is designed to emulate the text mode functionality of Digital's VT102 terminal (Appendix B describes differences between the VT240 and VT102), and Digital's VT125 terminal (Appendix C describes differences between the VT240 and VT125).

The VT100 mode provides strict backwards compatability with existing software written for the VT100 Series terminals (VT102 and VT125). This mode restricts keyboard use to keys that have a direct functional counterpart on the VT102 keyboard. All data is restricted to seven-bit format, and only ASCII, U.K., or special graphics characters are generated.

1.6.2 VT200 Mode, Seven-Bit Controls

The VT200 mode, with seven-bit controls, executes standard ANSI functions to provide the full range of VT240 Series terminal capabilities while using seven-bit controls in a seven-bit or eight-bit communications environment. This mode supports the DEC Multinational Character Set and provides some backward compatability with VT100 Series terminals.

1.6.3 VT200 Mode, Eight-Bit Controls

The VT200 mode, with eight-bit controls, executes standard ANSI functions to provide the full range of VT240 Series terminal capabilities while using eight-bit controls in an eight-bit communications environment. This mode supports the DEC Multinational Character Set and provides some backward compatability with the VT100 Series terminals.

1.6.4 VT52 Mode

The VT52 mode is a text mode that executes Digital private functions, and not ANSI. This mode has some compatability with a Digital VT102 operating in that terminal's VT52 mode.

The VT52 mode restricts keyboard use to those keys that have a direct functional counterpart on the VT102 keyboard when the VT102 is in VT52 mode. All data is restricted to seven-bit format, and only ASCII, U.K., or special graphics characters are generated.

1.6.5 ReGIS Mode

ReGIS mode is a graphics instruction set available when the terminal is in VT100 mode or either VT200 mode. ReGIS provides a full range of graphic image capabilities, and has a high degree of compatability with the ReGIS instruction set in Digital's VT125 (Appendix C describes the differences between a VT240 and VT125).

1.6.6 4010/4014 Mode

The 4010/4014 mode is designed to support industry-standard Tektronix 4010 and 4014 software packages.

CHAPTER 2
CONTROLS, INDICATORS, AND CONNECTORS

2.1 GENERAL

This chapter provides information about the terminal controls, indicators, and connectors. This chapter also includes information about various keypads and special function keys on the LK201 keyboard.

2.2 SYSTEM BOX (VS240)

The system box (Figure 2-1) includes the following controls, indicators and connectors.

- Power Switch -- turns the system box on or off.
- EIA Host Port Connector -- connects the system box to a host computer, either directly, or via an external modem.

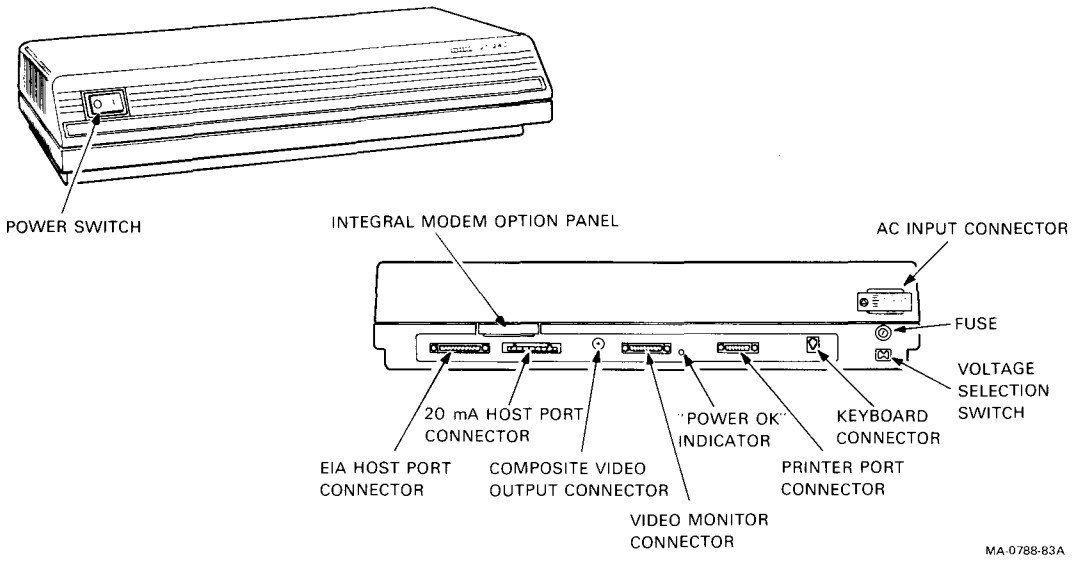


Figure 2-1 System Box Controls, Indicators, and Connectors

- 20 mA Connector -- connects the system box to a nearby host computer via a 20 mA loop.

- Composite Video Output Connector -- provides a complete composite video output signal for an additional slave monitor.

- Video Monitor Connector -- connects the monitor to the system box.

- Power Okay Indicator -- lights to indicate correct power is applied to the system box.

- Printer Port Connector -- connects a printer or an auxiliary input, output, or I/O device to the system box.

- Keyboard Connector -- connects the keyboard to the system box. (The keyboard can also connect directly to the VR201 monochrome monitor for the VT240, or to the connector at the VR241 color monitor end of the system box connection cable for the VT241.)

- AC Input Connector -- connects the power cord to the system box.

- Fuse -- protects the system box from electrical damage.

- Voltage Select Switch -- matches the input voltage selected for the system box to the voltage supplied at the wall outlet.

CAUTION

The wrong voltage select switch setting can cause damage to the system box.

2.3 MONOCHROME MONITOR (VR201)

The VR201 monochrome monitor (Figure 2-2) includes the following controls, indicators, and connectors.

- Contrast Control -- adjusts screen contrast.

- Brightness Control -- adjusts screen brightness.

- Video Monitor Connector -- connects the system box to the monitor.

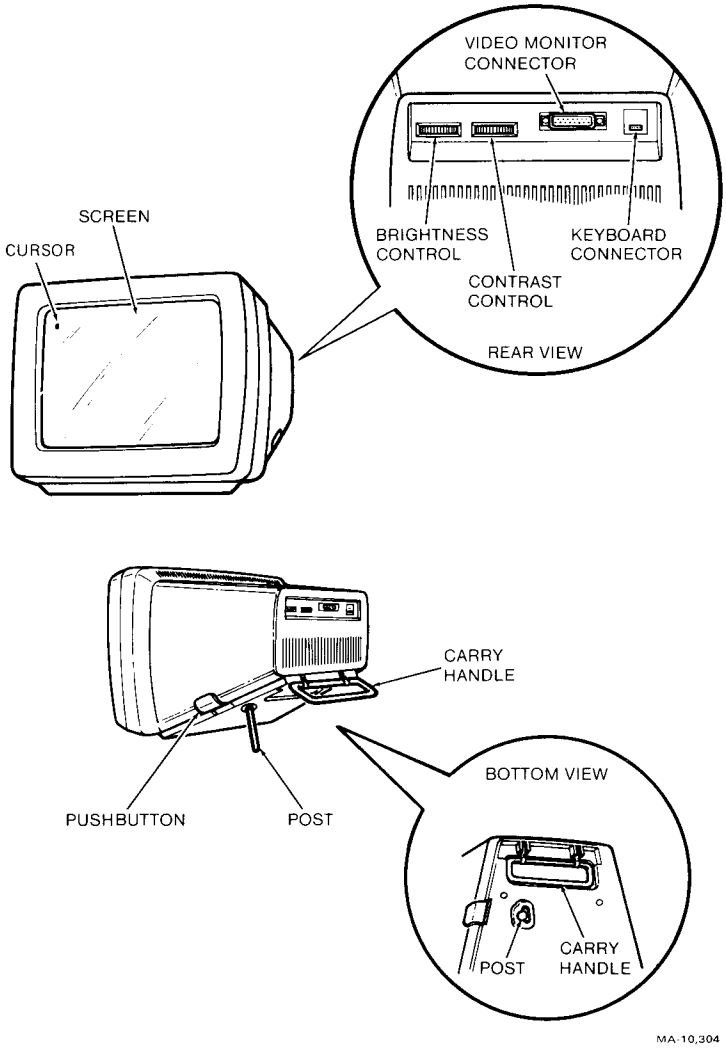


Figure 2-2 VR201 Monitor Controls, Indicators, and Connectors

- Keyboard Connector -- connects the keyboard to the monitor. (The keyboard can also connect to the system box.)
- Pushbutton -- releases a post that drops to provide a 30 degree tilt range for adjusting the monitor angle.
- Carry Handle -- provides an easy and safe way to carry the monitor.

2.4 COLOR MONITOR (VR241)

The VR241 color monitor (Figure 2-3) includes the following controls, indicators, and connectors.

- Power Switch -- turns the monitor on or off.
- Video Cable Connectors -- connect the system box to the monitor.

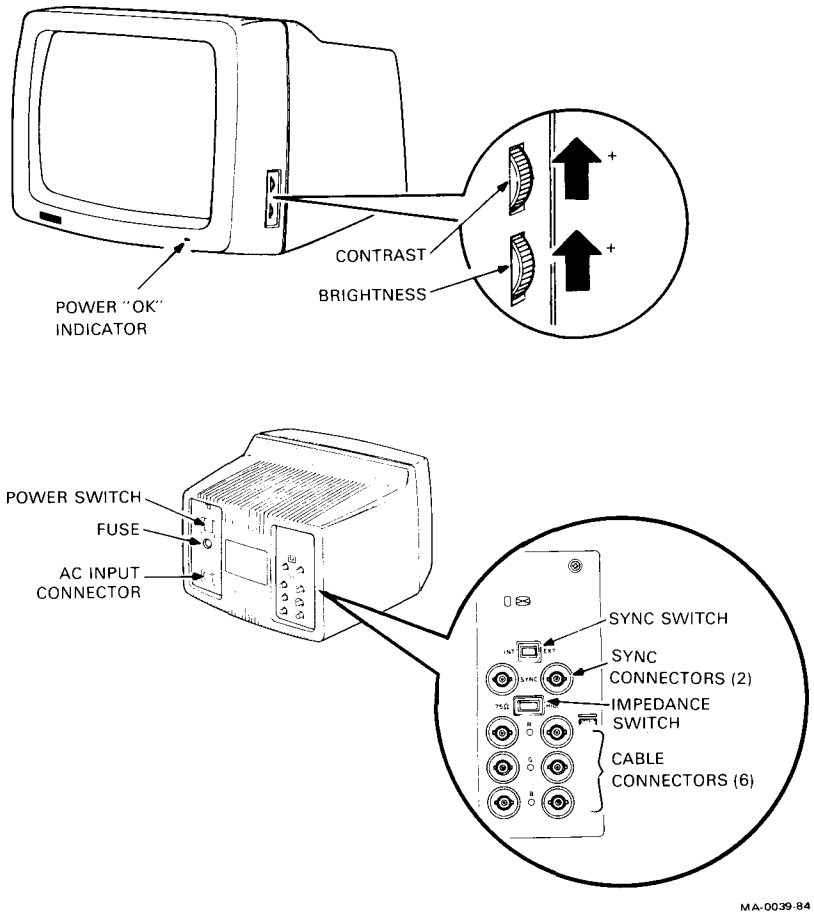


Figure 2-3 VR241 Monitor Controls, Indicators, and Connectors (Front and Rear)

- Power Okay Indicator -- lights to indicate correct power is applied to the monitor.
- Contrast Control -- adjusts screen contrast.
- Brightness Control -- adjusts screen brightness.
- AC Input Connector -- connects the power cord to the monitor.
- Fuse -- protects the monitor from electrical damage.
- Sync Switch -- selects internal or external synchronization.
- Sync Connectors -- connect external synchronization source to the monitor.
- Impedence Switch -- selects 75 ohm or high impedence.
- Voltage Select Switch -- matches the input voltage selected for the monitor to the voltage supplied at by the wall outlet.

CAUTION
The wrong voltage select switch setting can cause damage to the monitor.

2.5 KEYBOARD (LK2Ø1)

The LK2Ø1 keyboard (Figure 2-4) consists of the following parts.

- Main keypad
- Editing keypad
- Auxiliary keypad
- Top-row function keys
- Visual indicators
- Audible indicators
- Connector cable

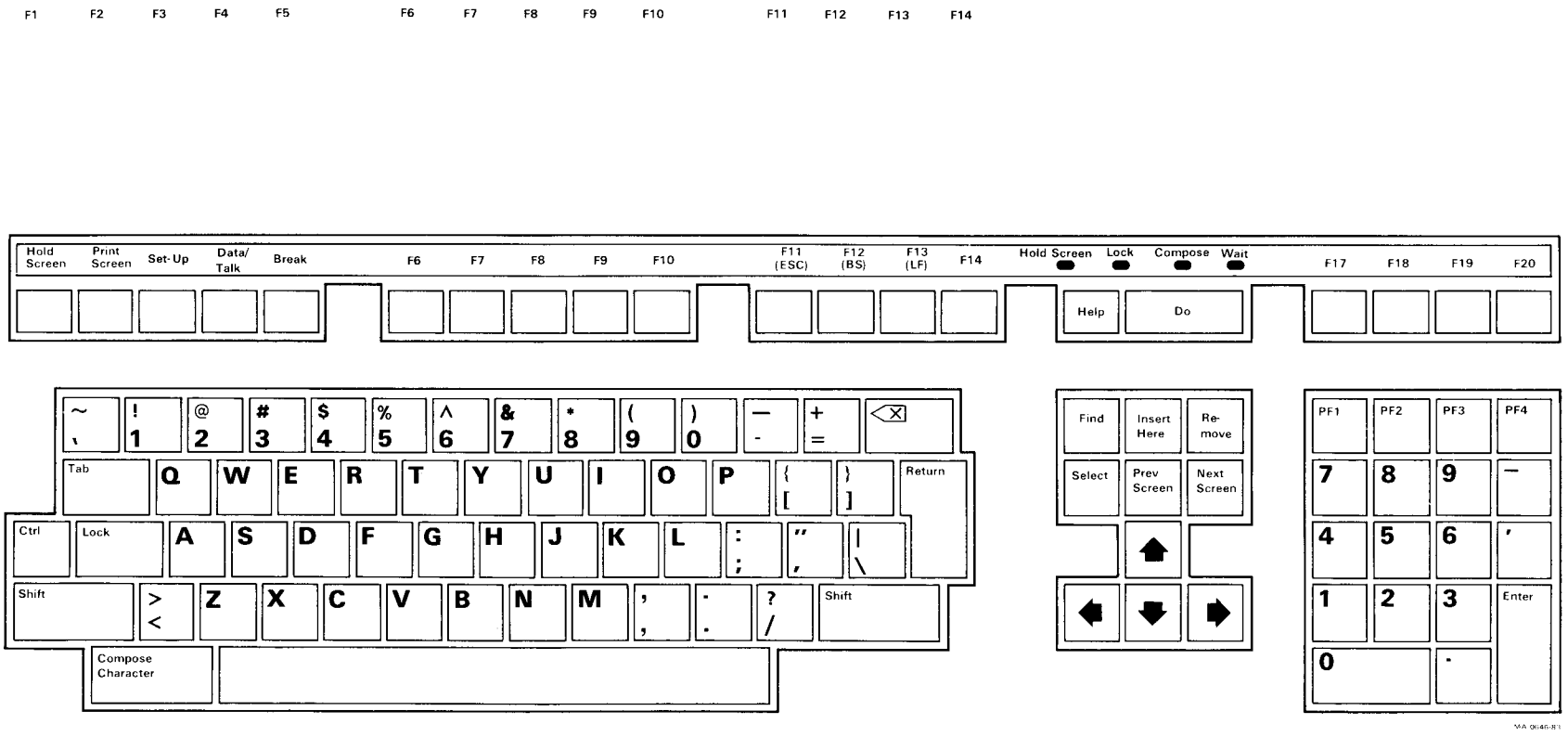


Figure 2-4 Keyboard (North American)

2.5.1 Main Keypad

The main keypad (Figure 2-5) operates like a standard typewriter keyboard and includes the following special function keys on the main keypad.

- **TAB** key -- generates a horizontal tab, which normally moves the cursor to the next tab stop.
- **CTRL** (Control) key -- when pressed with another key, generates a control code to tell the system to perform a defined function.
- **LOCK** Key -- when pressed, depending upon the set-up feature, serves as either a **SHIFT LOCK** (all keys generate shifted value), or a **CAPS LOCK** (alphabetic keys generate uppercase characters), until **LOCK** key is pressed again.
- **SHIFT** Key -- when pressed with another key, generates either the key's shifted value (for alphanumeric and two-symbol keys), or, as with some function keys, generates a predefined control function (such as **SHIFT** and <X which generates a CANCEL control character).
- **RETURN** Key -- generates a carriage return (or carriage return and linefeed as selected in set-up). In some cases, **RETURN** moves the cursor to the next line during text editing, or, in other cases, signals the system that a particular operation is finished.
- **<X (Delete)** Key -- generates a DEL character, normally moving cursor one character to the left and erasing character at the new cursor position.
- **COMPOSE CHARACTER** Key -- generates characters that do not exist as standard keys.

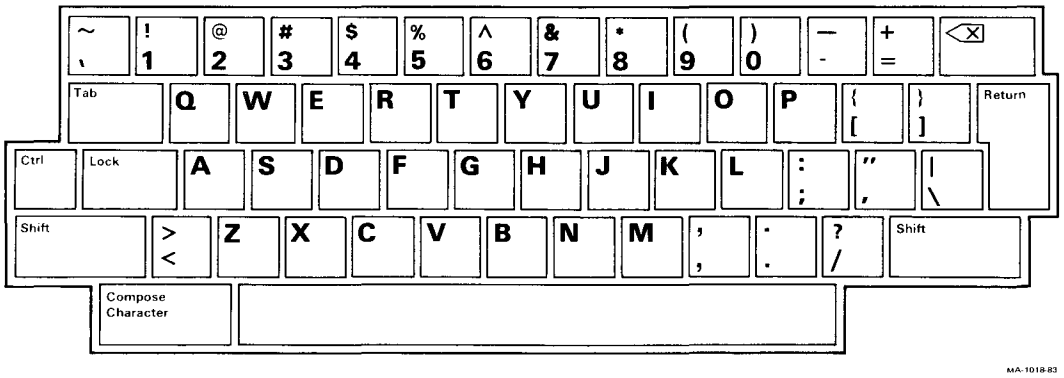


Figure 2-5 Main Keypad

2.5.2 Editing Keypad

The editing keypad (Figure 2-6) is normally used to control the cursor and edit data already entered. In a typical editing operation, the four arrow keys move the cursor in the direction of the arrow. The six editing keys can have functions that correspond to their legends, or can be defined for special functions, depending on the application program in effect.

2.5.3 Auxiliary Keypad

The auxiliary keypad (Figure 2-7) is used primarily to enter numeric data. However, some keys on this keypad (PF1, PF2, PF3, and PF4) can have different functions depending upon the application software. The ENTER key causes a carriage return (or a carriage return and linefeed, as selected in set-up), and is also used in set-up mode to activate selected features.

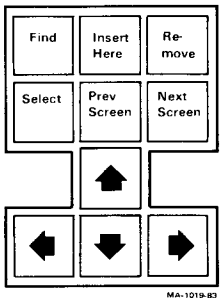


Figure 2-6 Editing Keypad

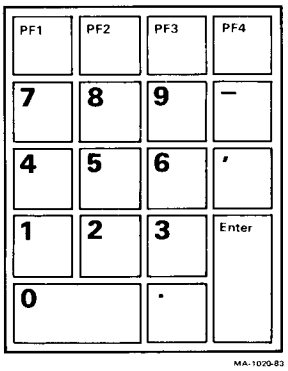


Figure 2-7 Auxiliary Keypad

2.5.4 Top-Row Function Keys

Most of the top-row function keys (Figure 2-8) have functions assigned to them by the application software in use. The following top-row function keys have predetermined values.

- **HOLD SCREEN** Key -- freezes the display and stops new characters from being displayed until you press **HOLD SCREEN** again to return the terminal to normal operation.

- **PRINT SCREEN** Key -- sends the text on the screen to the printer (**SHIFT** and **PRINT SCREEN** sends the entire screen image to the printer, while **CTRL** and **PRINT SCREEN** sets or resets the autoprint mode).

- **SET-UP** Key -- causes the terminal to enter or exit set-up.

- **DATA/TALK** Key -- controls use of a switched telephone line when the optional integral modem is installed in the system box.

- **BREAK** Key -- transmits a BREAK control character to the host if BREAK generation is enabled in set-up. (**SHIFT** and **BREAK** initiates a disconnect, while **CTRL** and **BREAK** sends the answerback message to the host).

- **F11** (ESC) -- generates an ESC character in either VT100 or VT52 mode (the function is determined by application programs in either VT200 mode).

- **F12** (BS) -- generates a BS character in either VT100 or VT52 mode (the function is determined by application programs in either VT200 mode).

- **F13** (LF) -- generates a LF character in either VT100 or VT52 mode (the function is determined by application programs in either VT200 mode).

2.5.5 Visual Indicators

The keyboard has the following four visual indicators that show the present status, or operation in progress.

- **HOLD SCREEN** Indicator -- lights when the display is frozen (refer to the **HOLD SCREEN** key description in section 2.5.4).

- **LOCK** Indicator -- lights when keyboard **LOCK** key is depressed (refer to the **LOCK** key description in section 2.5.1).

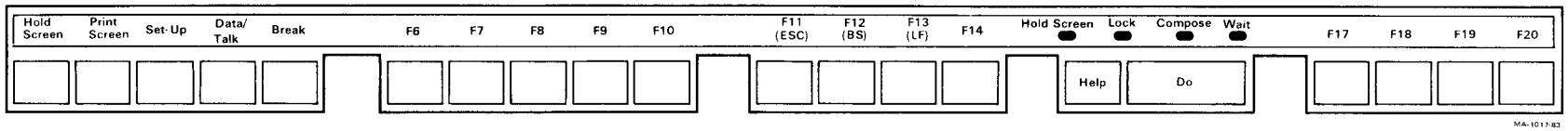


Figure 2-8 Top Row Function Keys and LEDs

- **COMPOSE** Indicator -- lights to indicate a compose sequence is in progress.

- **WAIT** Indicator -- lights when the keyboard is prevented from transmitting information (in effect, locked out of the system).

2.5.6 Audible Indicators

The keyboard generates the following two sounds which you can enable or disable in set-up.

- Keyclick
- Bell

2.5.6.1 Audible Keyclick -- The keyclick is generated each time you press a key, with the following exceptions.

- When the **SHIFT** or **CTRL** keys are depressed, because these keys do not generate characters, only modify characters generated by other keys.

- When the **WAIT** indicator is on (characters from the keyboard will be lost)

- When the keyclick is disabled in set-up

- When an inactive key is pressed

2.5.6.2 Bell -- The bell tone sounds in each of the following cases.

- As part of the power-up self-test

- When the terminal receives a BEL character from the host

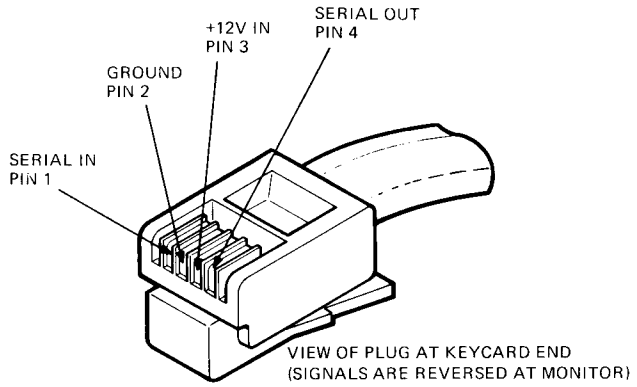
- When a compose error is made

- When the margin is approached (unless the bell tone is disabled in set-up).

2.5.7 Connector Cable

The keyboard module connects to the system via a BCCØ1 cable. Connection can be at the system box, the monochrome monitor (VR2Ø1), or at the cable that connects the system box to the color monitor (VR241).

Figure 2-9 shows the connector for the BCCØ1 cable.



CABLE CONNECTOR WIRING

KEYBOARD END		MONITOR END	
SIGNAL	PIN NO.	SIGNAL	PIN NO.
SERIAL IN	1	SERIAL OUT	4
GROUND	2	GND	3
+12 V IN	3	+12 V	2
SERIAL OUT	4	SERIAL IN	1

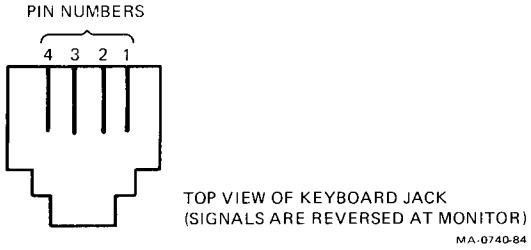


Figure 2-9 Connector for BCC01 Cable

CHAPTER 3
SYSTEM OVERVIEW

3.1 GENERAL

This chapter provides an overview of system interactions during each possible operating state of the VT240 Series terminal.

3.2 OPERATING STATES

The terminal functions in any one of the following three operating states.

Set-up mode
Local mode
On-line mode

3.2.1 Set-Up

You can select set-up from the keyboard (by pressing the SET-UP key) to:

- Examine or change terminal operating characteristics (such as transmit and receive speeds)
- Transfer from on-line mode to local mode, or from local mode to on-line mode.

While in set-up mode, the terminal is functionally disconnected from the host. Only the keyboard is enabled as an input device, and only the monitor is enabled for output. Any data received from the host is buffered until the terminal is placed in the on-line mode.

3.2.2 Local

You can select local while the terminal is in set-up mode. This operating state disables terminal-to-host communications. Any data received from the host while in local mode is buffered until the terminal is placed on-line.

In local, the keyboard serves as an input device; displayable data input from this device is sent to the screen. Also, you can configure the printer port as either an input or output port (selected in set-up mode). If you select the printer port as an input port, information can be input to the terminal from a device connected to the printer port. If you select the printer port as an output port, information can be output from the terminal (screen or keyboard data), to a device connected to the printer port.

3.2.3 On-Line

You can select on-line while the terminal is in set-up mode. This operating state lets the terminal communicate with a host. This communications link can be in any of the following forms.

- Null Modem -- Communication is through a direct line link with the host, either through the EIA host port, or the 20 mA port.
- External Modem -- Communication is with a remote host, using the external modem linked to the terminal through the EIA host port.
- Integral Modem -- Communication is with a remote host; the terminal is linked to the host through telephone connectors provided by the integral modem option.

When the terminal is on-line, data entered at the keyboard is transmitted to the host. A local-echo feature (selected in set-up mode) routes keyboard data to the monitor, as well as the host.

You can use the printer port to connect an input, output, or I/O device (selected in set-up mode). You can use both the keyboard and input device to generate data for transfer to the host (with local-echo at the monitor only for keyboard input if local-echo is enabled in set-up).

Both the monitor and the output device can receive information from the host, but not at the same time. However, data received for the monitor can be subsequently transferred to an output device.

If an I/O device is connected to the printer port, the terminal is effectively shut out of the communications and serves only as a buffer for communications between the I/O device and the host. No output is made to the monitor, and no keyboard input can be transfered to the host.

3.3 SYSTEM ARCHITECTURE

Figure 3-1 is a functional block diagram of the terminal. This diagram shows the following major components and or logics.

- CPU logic
- Video logic
- System communication logic
- Integral modem (option)
- Power supply
- Keyboard
- Monitor

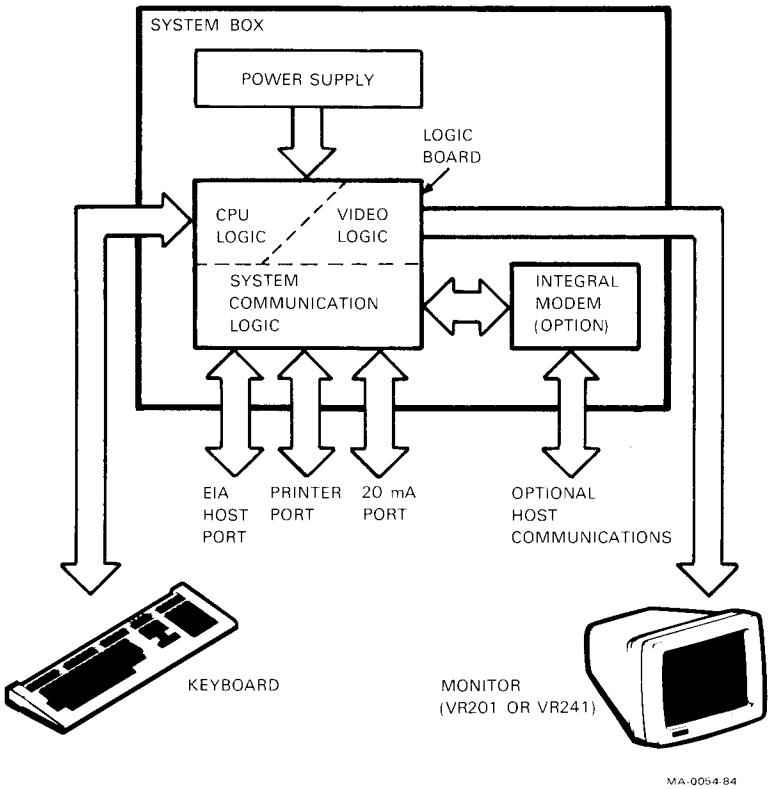


Figure 3-1 VT240 Series Terminal System Block Diagram

3.3.1 CPU Logic

The CPU logic controls overall terminal operation. It interprets host and operator input and directs terminal functions. The CPU logic contains the following major circuits/components.

- T11 microprocessor directly responsible for terminal operation
- Associated access logics such as I/O buffers, memory mappper, and address latch logics
- Keyboard interface circuitry
- 32K volatile random access memory (RAM) to provide data buffering and work space for terminal control operations
- 128 byte nonvolatile RAM to store terminal set-up information
- 96K byte read only memory (ROM) to contain firmware for all terminal control functions, including keyboard handling, screen data handling, set-up, self-test, ReGIS, 4010/4014 mode, VT52 mode, and serial I/O handling.

3.3.2 Video Logic

The video logic develops the video output signals necessary to drive the terminal monitor. The video logic consists of the following major circuits/components.

- 8085 microprocessor and associated circuits used as a character accelerator for high speed writing of text characters into the video logic
- Video controller to perform (DMA) direct memory access functions from character and screen RAM to video output, address buffering for CPU access to screen RAM, and video timing signal generation
- Two-plane bit map to allowing each addressable pixel to have any one of four values
- Output map to allow programmable interpretation of bit map values
- Digital to Analog (D/A) converter to change digital timing signals, and output map values into analog video signal output for the monitor

3.3.3 System Communication Logic

The system communication logic interfaces with the terminal external devices. The system communication logic consists of the following major circuits/components.

- Connectors for physical connection with the printer (or other auxiliary device), host (EIA host port or 20 mA port connectors), and integral modem option
- Interface logics responsible for data input and output from various connectors
- Registers for communication with CPU logic to control and report on interface activity

3.3.4 Integral Modem (Option)

When installed, the integral modem interfaces with the terminal through a switched or dedicated telephone line for communication with a remote host. The integral modem consists of the following major circuits/components.

- Two four-pin telephone jack connectors for interfacing with the telephone line
- Handshake circuits to control communication between the terminal and remote host

3.3.5 Power Supply

The power supply generates the operating voltages required by the system box, keyboard, and VR201 monochrome monitor (the VR241 color monitor has its own power supply). The power supply contains the following major circuits/components.

- AC input circuits
- +5 V development circuits
- +12 V development circuits
- -12 V development circuits

3.3.6 Keyboard

The keyboard enables operator input to the system. The keyboard consists of the following major circuits/components.

- 8051 microprocessor to control keyboard operation
- Serial interface for communication with the system box

- Key matrix scanning circuits to determine when a key is being pressed
- Beeper circuits to generate bell tones and key clicks
- LED drivers to enable the keyboard's visual indicators.

3.3.7 Monitor

The monitor converts a composite video input signal from the video logic, into visual output to the operator. The monitor can be either a VR2Ø1 monochrome monitor or a VR241 color monitor. In either case the monitor contains the following major circuits/components.

- CRT device to present the visual output
- Electronics to develope drive potentials for the CRT
- Brightness and contrast controls

The VR241 also contains its own power supply to convert ac input to the operating voltages required by this monitor. The VR2Ø1 develops its operating voltages from dc voltage provided by the power supply in the system box.

3.4 SYSTEM INTERACTION

Figures 3-2 through 3-15 provide an overview of the information flow within the terminal for various system configurations, during the different operating states (set-up, local, and on-line).

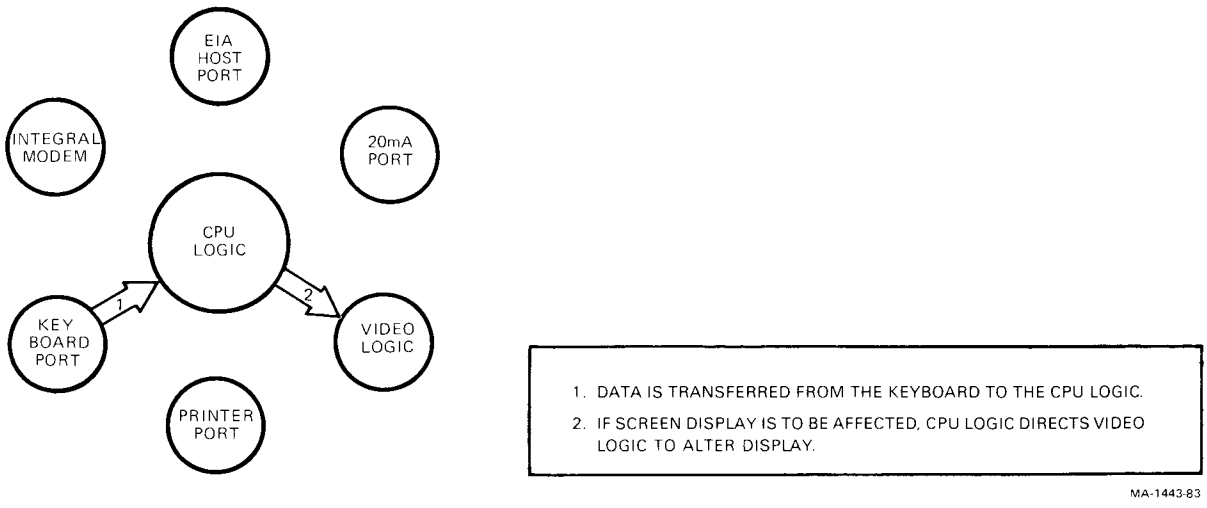
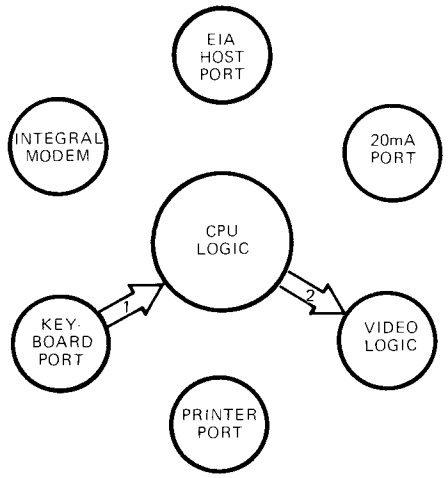


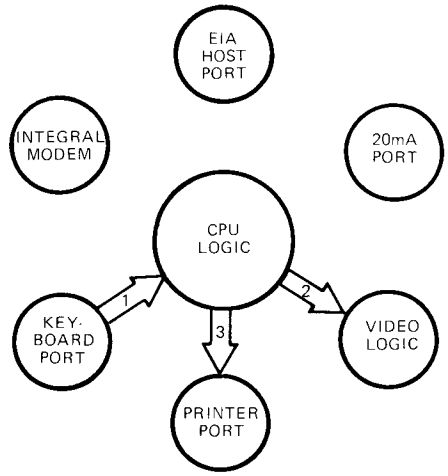
Figure 3-2 System Interaction in Set-Up



1. DATA IS TRANSFERRED FROM THE KEYBOARD TO THE CPU LOGIC.
2. IF SCREEN DISPLAY IS TO BE AFFECTED, CPU LOGIC DIRECTS VIDEO LOGIC TO ALTER DISPLAY.

MA-1444-83

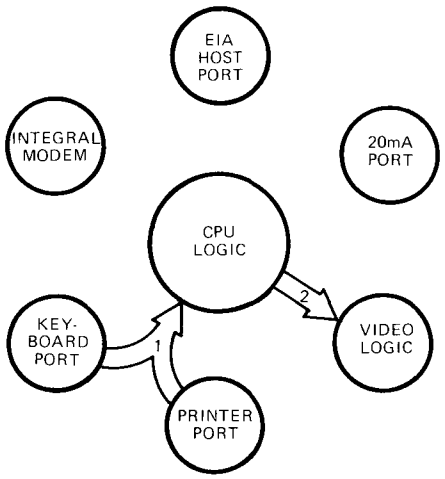
Figure 3-3 System Interaction in Local (Printer Port Inactive)



1. DATA IS TRANSFERRED FROM THE KEYBOARD TO THE CPU LOGIC.
2. IF SCREEN DISPLAY IS TO BE AFFECTED, CPU LOGIC DIRECTS VIDEO LOGIC TO ALTER DISPLAY.
3. IF DATA IS TO BE OUTPUT TO AN AUXILIARY DEVICE, CPU LOGIC DIRECTS TRANSFER OF DATA AND CONTROLS TO AUXILIARY DEVICE VIA PRINTER PORT PORTION OF SYSTEM INTERFACE LOGIC.

MA-1445-83

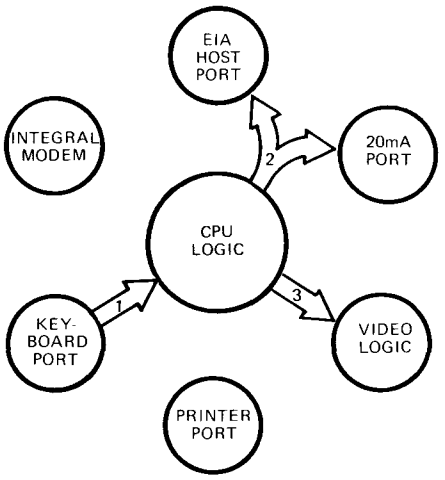
Figure 3-4 System Interaction in Local (Printer Port as Output Port)



1. DATA IS TRANSFERRED TO THE CPU LOGIC FROM AN ENABLED INPUT, EITHER THE KEYBOARD, OR THE AUXILIARY DEVICE (VIA PRINTER PORT PORTION OF THE SYSTEM INTERFACE LOGIC); IF DATA IS PRESENT FROM BOTH SOURCES, AND BOTH ARE ENABLED, CPU LOGIC WILL DETERMINE WHICH DATA TO PROCESS FIRST.
2. IF SCREEN DISPLAY IS TO BE AFFECTED, CPU LOGIC DIRECTS VIDEO LOGIC TO ALTER DISPLAY.

MA-1446-83

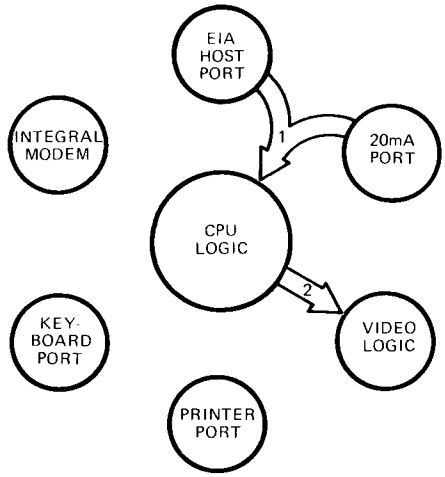
Figure 3-5 System Interaction in Local (Printer Port as Input Port)



1. DATA IS TRANSFERRED FROM THE KEYBOARD TO THE CPU LOGIC.
2. DATA IS TRANSFERRED FROM THE CPU LOGIC TO THE HOST, VIA EITHER EIA HOST PORT, OR 20 mA PORT PORTIONS OF THE SYSTEM COMMUNICATION LOGIC.
3. IF LOCAL-ECHO IS ENABLED, AND SCREEN DISPLAY IS TO BE AFFECTED, CPU LOGIC DIRECTS VIDEO LOGIC TO ALTER DISPLAY.

MA-1447-83

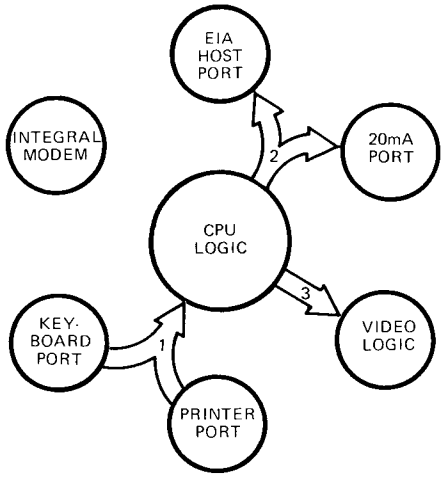
Figure 3-6 System Interaction in On-Line (Printer Port as Inactive or Output Port)



1. DATA IS TRANSFERRED TO THE CPU LOGIC FROM THE HOST, VIA EITHER EIA HOST PORT, OR 20 mA PORT PORTIONS OF THE SYSTEM COMMUNICATION LOGIC.
2. IF SCREEN DISPLAY IS TO BE AFFECTED, CPU LOGIC DIRECTS VIDEO LOGIC TO ALTER DISPLAY.

MA-1448-83

Figure 3-7 System Interaction in On-Line (Printer Port as Inactive or Input Port)



1. DATA IS TRANSFERRED TO THE CPU LOGIC FROM AN ENABLED INPUT, EITHER THE KEYBOARD, OR THE AUXILIARY DEVICE (VIA PRINTER PORT PORTION OF THE SYSTEM COMMUNICATION LOGIC); IF DATA IS PRESENT FROM BOTH SOURCES, AND BOTH ARE ENABLED, CPU LOGIC WILL DETERMINE WHICH DATA TO PROCESS FIRST.
2. DATA IS TRANSFERRED FROM THE CPU LOGIC TO THE HOST, VIA EITHER EIA HOST PORT, OR 20 mA PORT PORTIONS OF THE SYSTEM COMMUNICATION LOGIC.
3. IF LOCAL-ECHO IS ENABLED, AND SCREEN DISPLAY IS TO BE AFFECTED, CPU LOGIC DIRECTS VIDEO LOGIC TO ALTER DISPLAY.

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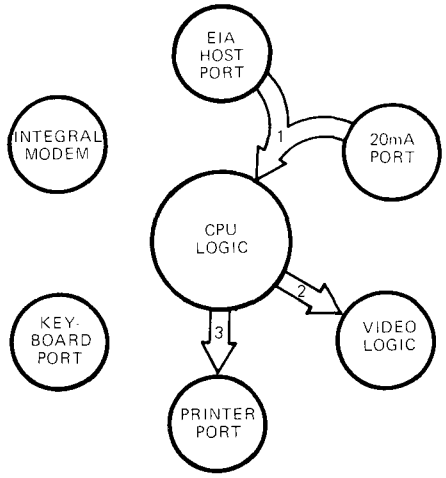
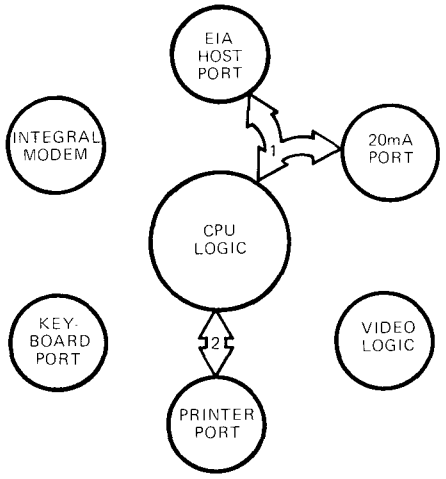
Figure 3-8 System Interaction in On-line (Printer Port as Input Port)



1. DATA IS TRANSFERRED TO THE CPU LOGIC FROM THE HOST, VIA EITHER EIA HOST PORT, OR 20 mA PORT PORTIONS OF THE SYSTEM COMMUNICATION LOGIC.
2. IF SCREEN DISPLAY IS TO BE AFFECTED, CPU LOGIC DIRECTS VIDEO LOGIC TO ALTER DISPLAY.
3. IF DATA IS TO BE OUTPUT TO AN AUXILIARY DEVICE, CPU LOGIC DIRECTS TRANSFER OF DATA AND CONTROLS TO AUXILIARY DEVICE VIA PRINTER PORT PORTION OF SYSTEM COMMUNICATION LOGIC.

MA-1450-83

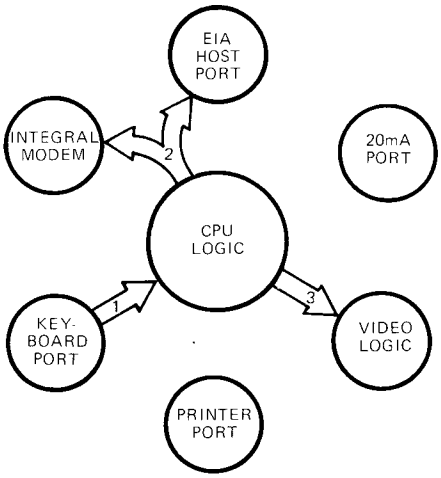
Figure 3-9 System Interaction in On-Line (Printer Port as Output Port)



1. DATA IS TRANSFERRED BETWEEN THE CPU LOGIC AND THE HOST, VIA EITHER EIA HOST PORT, OR 20 mA PORT PORTIONS OF THE SYSTEM COMMUNICATION LOGIC.
2. DATA IS TRANSFERRED BETWEEN THE CPU LOGIC AND THE AUXILIARY I/O DEVICE, VIA PRINTER PORT PORTION OF SYSTEM COMMUNICATION LOGIC.

MA-1451-83

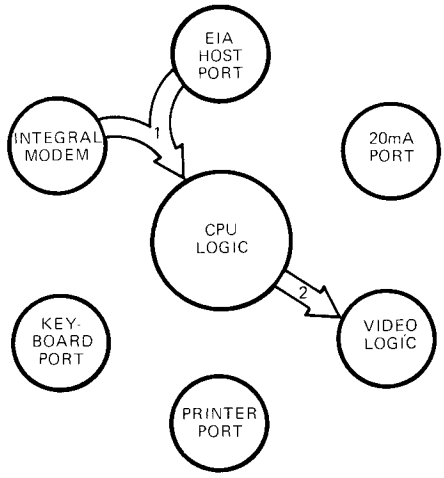
Figure 3-10 System Interaction in On-Line (Printer Port as I/O Port)



1. DATA IS TRANSFERRED FROM THE KEYBOARD TO THE CPU LOGIC.
2. DATA IS TRANSFERRED FROM THE CPU LOGIC TO THE HOST, VIA EITHER INTEGRAL MODEM OR EIA HOST PORT PORTIONS OF THE SYSTEM COMMUNICATION LOGIC.
3. IF LOCAL-ECHO IS ENABLED, AND SCREEN DISPLAY IS TO BE AFFECTED, CPU LOGIC DIRECTS VIDEO LOGIC TO ALTER DISPLAY.

MA-1452-83

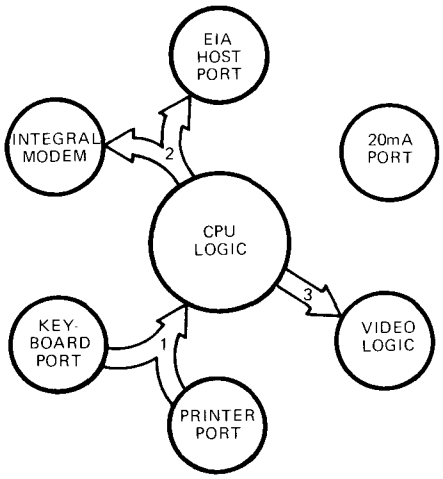
Figure 3-11 System Interaction in On-Line (Printer Port as Inactive or Output Port)



1. DATA IS TRANSFERRED TO THE CPU LOGIC FROM THE HOST, VIA EITHER INTEGRAL MODEM OR EIA HOST PORT PORTIONS OF THE SYSTEM COMMUNICATION LOGIC.
2. IF SCREEN DISPLAY IS TO BE AFFECTED, CPU LOGIC DIRECTS VIDEO LOGIC TO ALTER DISPLAY.

MA-1453-83

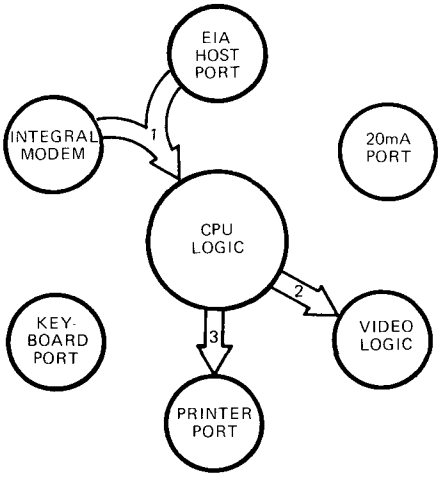
Figure 3-12 System Interaction in On-Line (Printer Port as Inactive or Input Port)



1. DATA IS TRANSFERRED TO THE CPU LOGIC FROM AN ENABLED INPUT, EITHER THE KEYBOARD, OR THE AUXILIARY DEVICE (VIA PRINTER PORT PORTION OF THE SYSTEM COMMUNICATION LOGIC); IF DATA IS PRESENT FROM BOTH SOURCES, AND BOTH ARE ENABLED, CPU LOGIC WILL DETERMINE WHICH DATA TO PROCESS FIRST.
2. DATA IS TRANSFERRED FROM THE CPU LOGIC TO THE HOST, VIA EITHER INTEGRAL MODEM, OR EIA HOST PORT PORTIONS OF THE SYSTEM COMMUNICATION LOGIC.
3. IF LOCAL-ECHO IS ENABLED, AND SCREEN DISPLAY IS TO BE AFFECTED, CPU LOGIC DIRECTS VIDEO LOGIC TO ALTER DISPLAY.

MA-1454-83

Figure 3-13 System Interaction in On-Line (Printer Port as Input Port)



1. DATA IS TRANSFERRED TO THE CPU LOGIC FROM THE HOST, VIA EITHER INTEGRAL MODEM, OR EIA HOST PORT PORTIONS OF THE SYSTEM COMMUNICATION LOGIC.
2. IF SCREEN DISPLAY IS TO BE AFFECTED, CPU LOGIC DIRECTS VIDEO LOGIC TO ALTER DISPLAY.
3. IF DATA IS TO BE OUTPUT TO AN AUXILIARY DEVICE, CPU LOGIC DIRECTS TRANSFER OF DATA AND CONTROLS TO AUXILIARY DEVICE VIA PRINTER PORT PORTION OF SYSTEM COMMUNICATION LOGIC.

MA-1455-83

Figure 3-14 System Interaction in On-Line (Printer Port as Output Port)

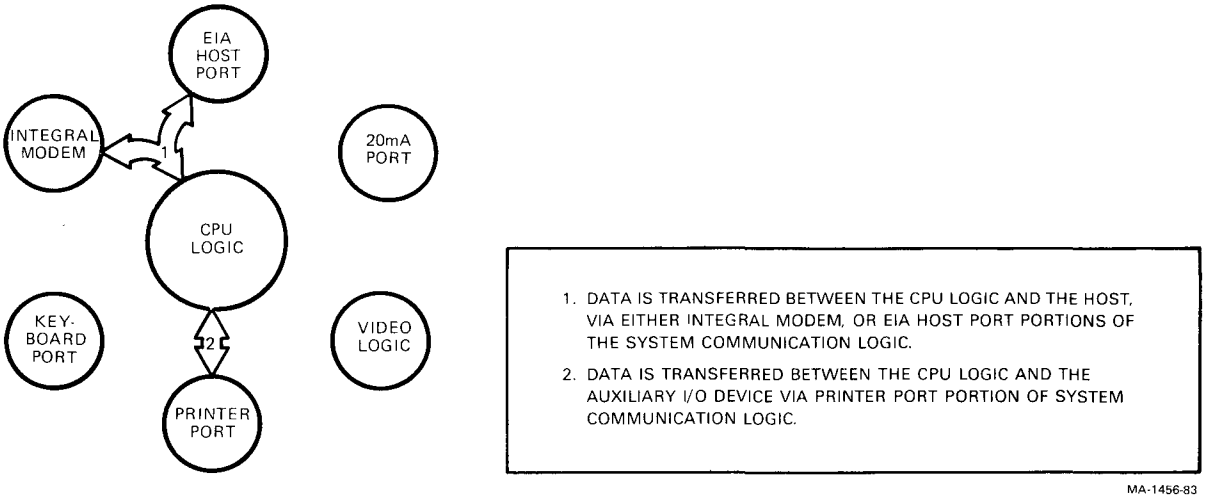


Figure 3-15 System Interaction in On-Line (Printer Port as I/O Port)

CHAPTER 4
CPU LOGIC

4.1 GENERAL

The CPU logic (shaded area in Figure 4-1) directs VT240 activity in response to either operator input (via keyboard), or host input (via system communication logic). In general, the CPU does the following task.

- Defines operating parameters for other logic components
- Directs system communication logic, video logic, and keyboard module operation
- Initializes system at power up, and executes self-test programs.

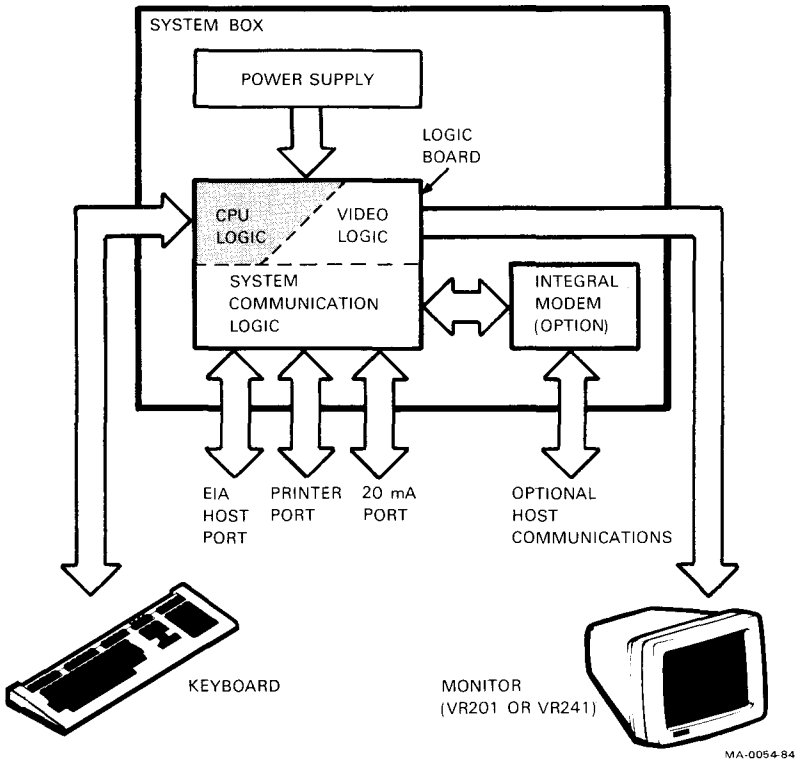


Figure 4-1 VT240-Series Terminal System Block Diagram

4.2 MAJOR CIRCUITS/COMPONENTS

Figure 4-2 is a block diagram that identifies the following major circuits/components that make up the CPU logic.

Central processor unit (CPU)
Mode register
Control gates
Address latch
Memory access decode
Read only memory (ROM)
Nonvolatile random access memory (NVR)
Volatile random access memory (RAM)
Memory map
Interrupt control
Command register
Clock generator
I/O buffer
I/O decode
Keyboard interface (I/F)

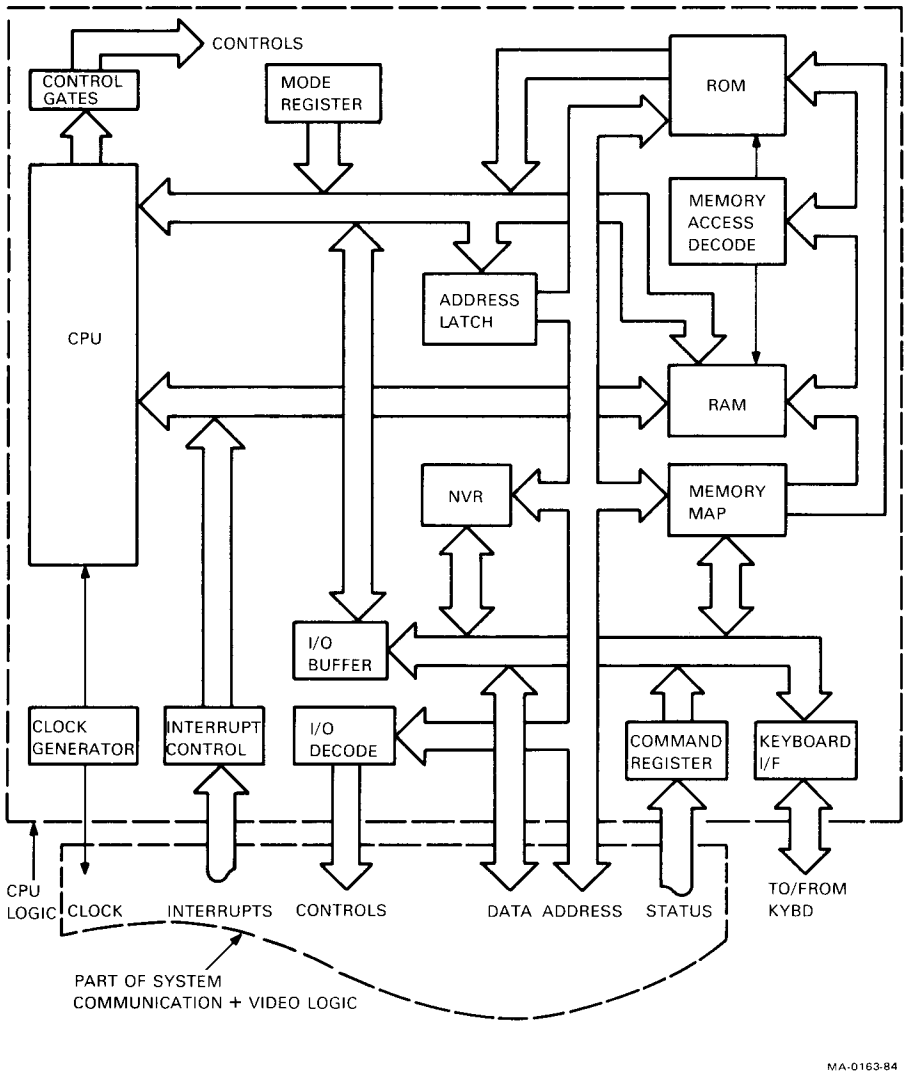


Figure 4-2 CPU Logic Block Diagram

4.2.1 Central Processor Unit

The CPU (Figure 4-3) is a DCT11-AA, commonly referred to as the T11. The T11 is responsible for the terminal's functionality and does the following tasks.

- Generates initial control signals.
- Compares data input to the VT240 against information stored in ROM memory to determine operations desired
- Initializes the system on power up, and executes test programming stored in ROM memory to determine the terminal's readiness

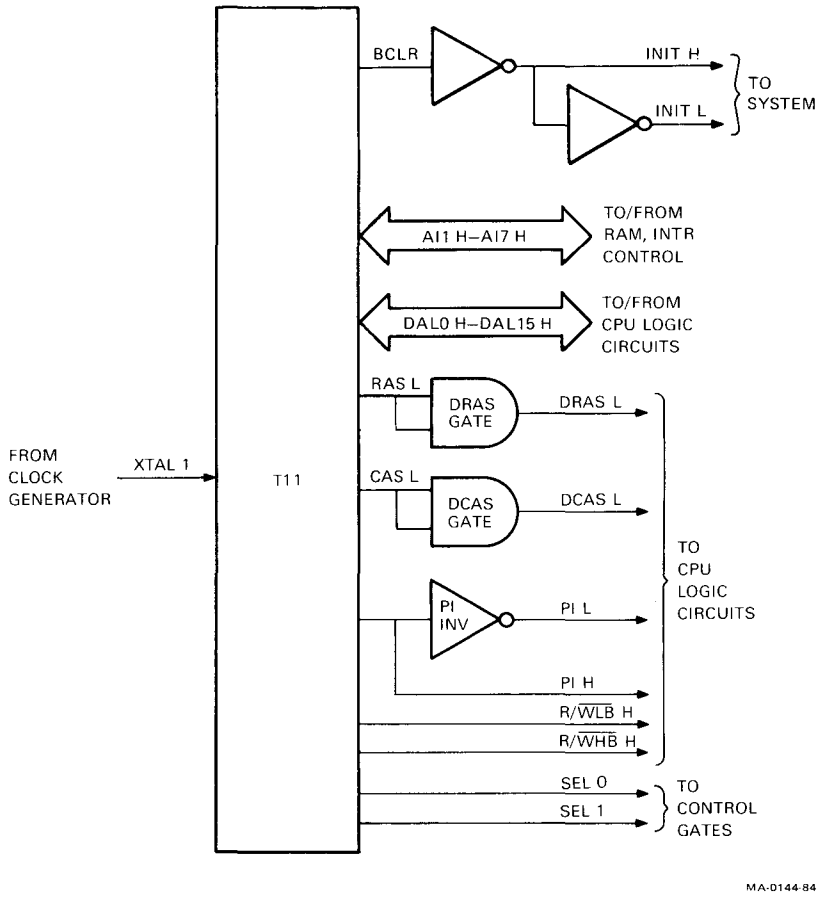


Figure 4-3 CPU Block Diagram

4.2.1.1 T11 Internal Circuits -- Figure 4-4 is a block diagram that shows the following major T11 internal circuits.

- General Purpose Registers (RØ--R5) -- are used for various functions, including accumulating, indexing, autoincrementing, autodecrementing, stack pointers for temporary data storage, and arithmetic operations.

- Stack Pointer (SP) Register (R6) -- contains the address of the last entry in the stack.

- Program Counter (PC) Register (R7) -- contains the address of the next instruction to be executed.

- Status Register -- contains information that defines the current processor status.

- Mode Register -- contains data that defines T11 operating parameters, with this data loaded from the external mode register during power-up sequence (refer to section 5.2.2 for a description of the values defined by the external mode register).

- Address Register -- contains the RAM address to be accessed by the next read or write operation.

- Clock Buffers -- buffers timing input from clock generator.

- Power Control -- monitors power conditions by generating a clear signal output for VT24Ø initialization when sensing a power on condition.

- Refresh Counter -- defines the RAM address to be accessed for a refresh operation.

- Address Multiplexer -- multiplexes inputs from the refresh counter and address register to generate an address output to the address/interrupt buffers for either a RAM refresh cycle (refresh counter input), or RAM read/write cycle (address register input).

- Address/Interrupt Buffers -- buffers RAM address output and interrupt control input.

- Control -- generates the control signals required for T11 to access VT24Ø components.

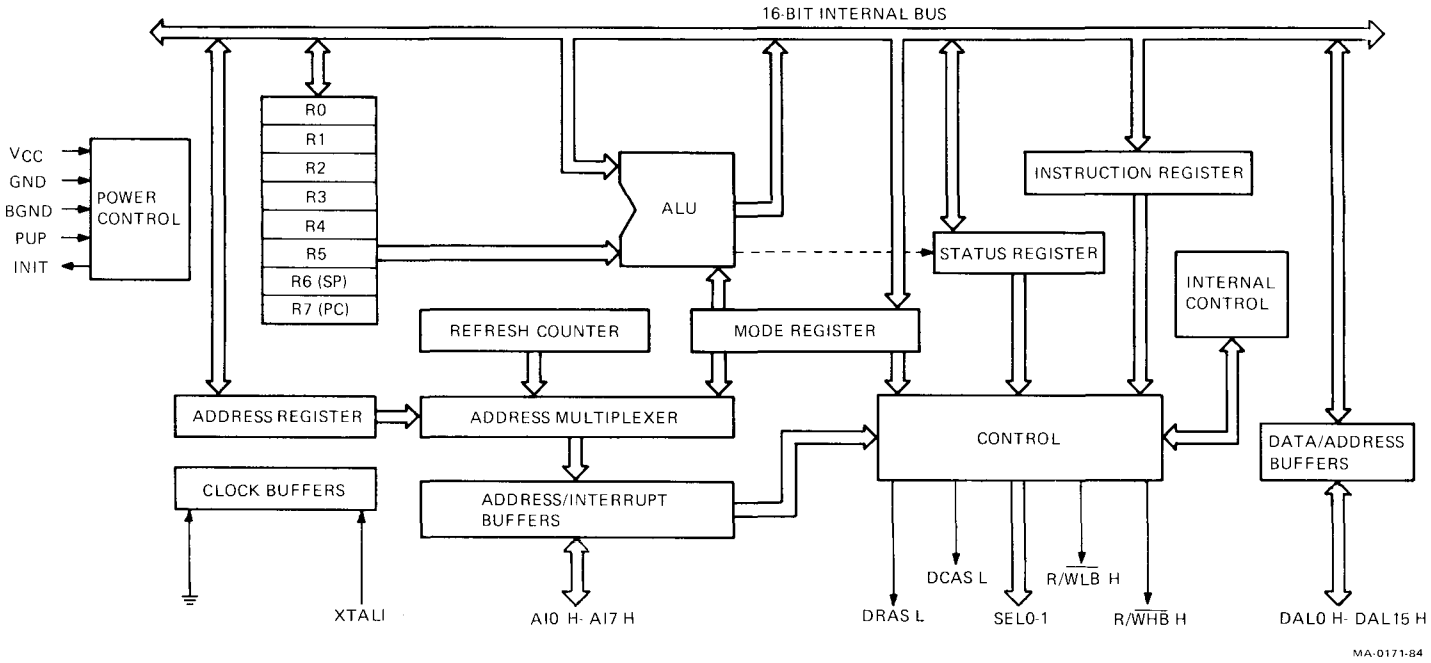


Figure 4-4 T11 Internal Block Diagram

- Internal Control -- generates the control signals required by the T11 internal circuits.

- Data/Address Buffers -- are two I/O devices that provide buffering between the DAL0 H--DAL15 H external bus and the T11 internal bus.

- Instruction Register -- contains data that defines the operation to be initiated by the control circuit outputs.

- ALU -- performs all arithmetic and logical instruction operations.

Later in this chapter, Table 4-6 describes the signals shown in Figures 4-3 and 4-4.

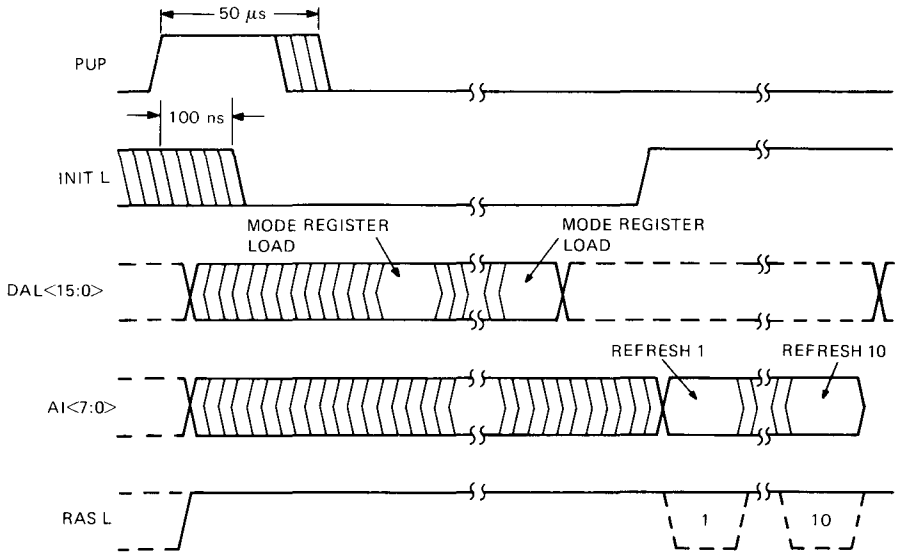
4.2.1.2 T11 Transactions -- A transaction is an activity that performs one of the following functions.

Read
Write
Refresh
Assert priority in (ASPI)
No operation (NOP)

Each transaction is made up of either one or two microcycles: two microcycles for read and write transactions or one microcycle for refresh, ASPI, or NOP. Each microcycle is the activity required to execute one micro-instruction. The microcycle performs all the functions necessary for transferring data internally and externally, and for calculating values.

Each read, write, refresh, and NOP microcycle is contains three clock phases: Ø1, Ø2, and ØW. ASPI transactions contain a fourth clock phase, phase D (ØD), which is added between Ø2 and ØW. All clock phases have the same duration between assertions, and are developed from the 7.3728 megahertz (MHz) input supplied by the clock generator. A three phase microcycle has a 813.6 nanoseconds (ns) duration; a four phase microcycle has a 1Ø84.6 ns duration.

Figure 4-5 is a timing diagram for the power-up sequence. Figure 4-6 is a timing diagram for T11 transactions. Figures 4-7 through 4-1Ø show ports of the T11 timing diagram (Figure 4-6) that identify specific conditions involved in each diagrammed bus transaction (no diagram is provided for NOP because no T11 external operation occurs).



NOTES
1. MODE REG RD 2.6 μs AFTER PUP L. 2. OUTPUTS SET 250 ns AFTER PUP H. 3. FIRST FETCH 89 μs AFTER PUP H AT ADDRESS: 000000. 4. INIT L 30 ns AFTER BCLR L: A. MAPPER OFF; B. 8085 RESETS; C. KYBD UART RESET & LPBK OFF; D. COMM SEL – EIA CONN; E. HOST/PRTR UART RESET. (DISABLES Tx & Rx, STOPS CTR/TIMER, ALL OUTPUTS H); F. MODEM OPTION (DESELECTED, BELL 212A, 1200 BAUD, DOMESTIC, 10 BITS, TEST OFF, ANSWER, AND OFF-D H). G. NVR RECALL

MA-0135-84

Figure 4-5 Power-Up Sequence

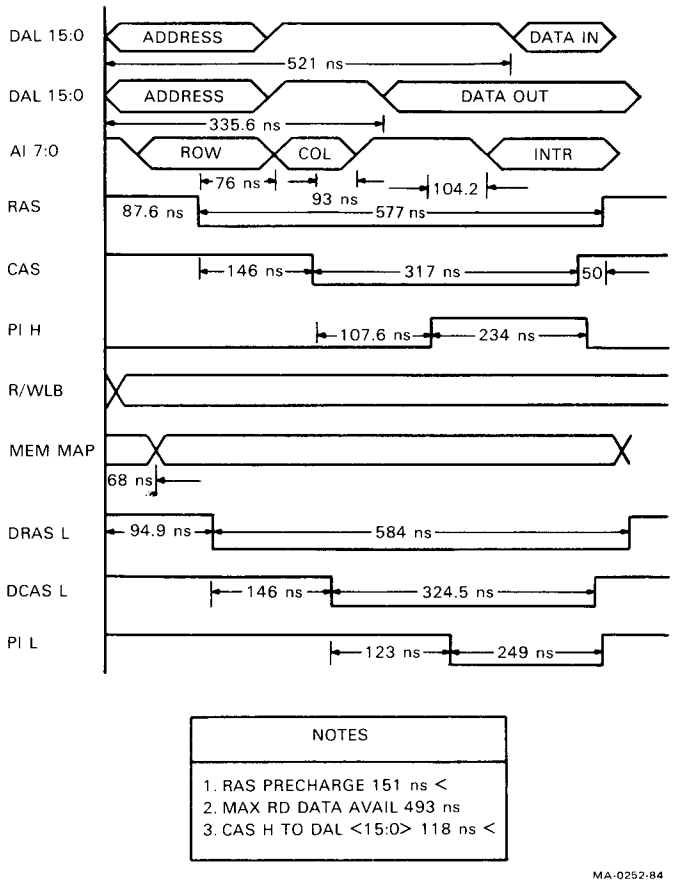


Figure 4-6 T11 Timing Diagram

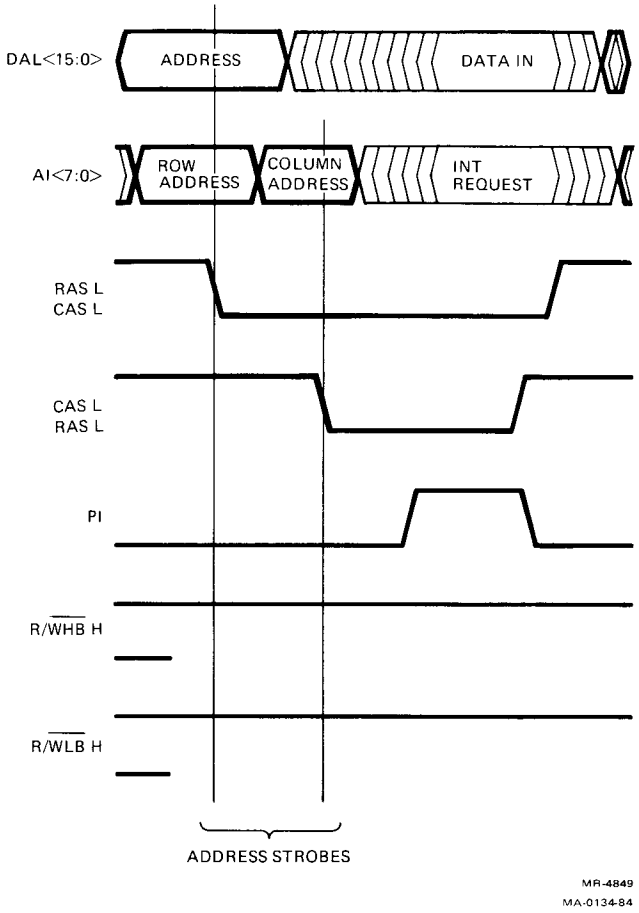


Figure 4-7 T11 16-Bit Dynamic Read Transaction Diagram

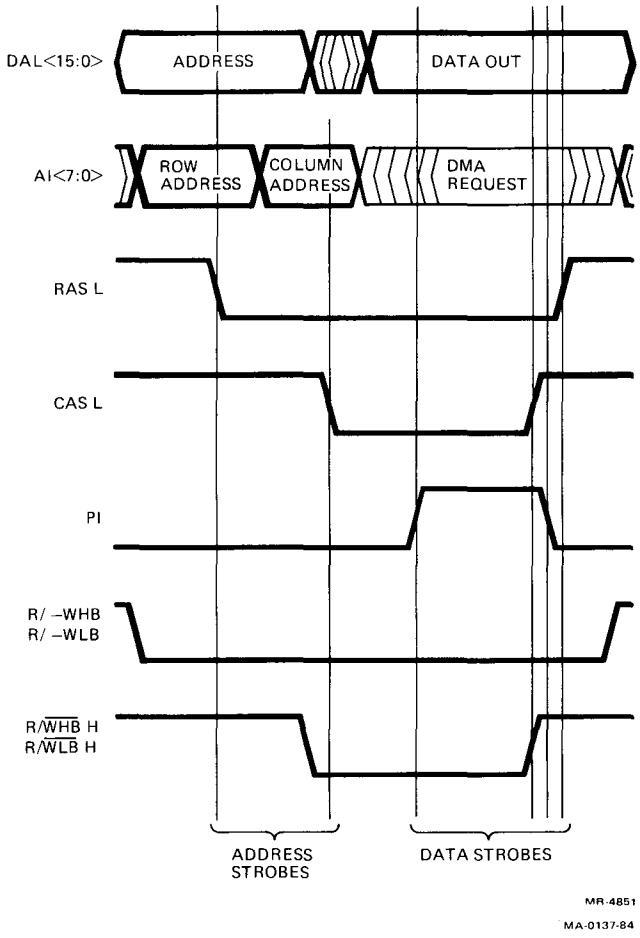


Figure 4-8 T11 16-Bit Dynamic Write Transaction Diagram

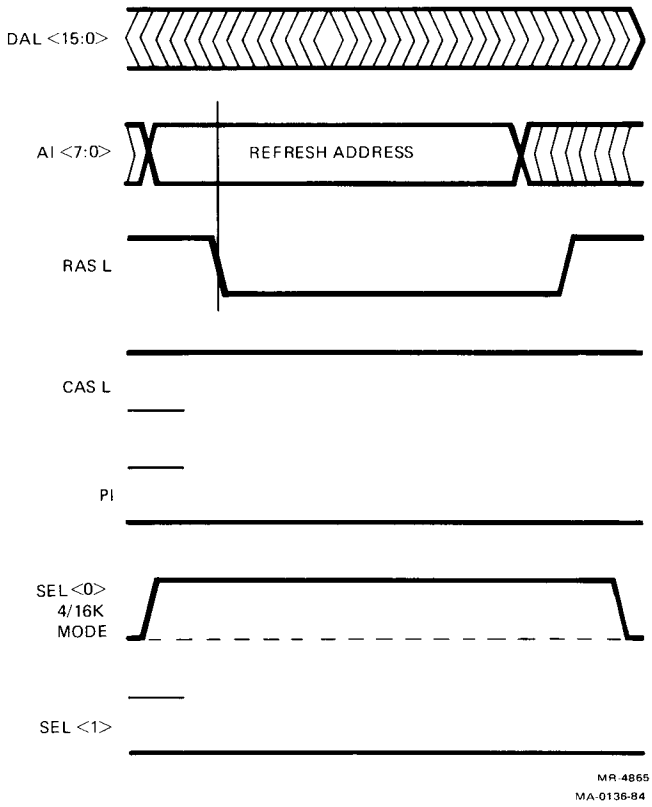


Figure 4-9 T11 Refresh Transaction Diagram

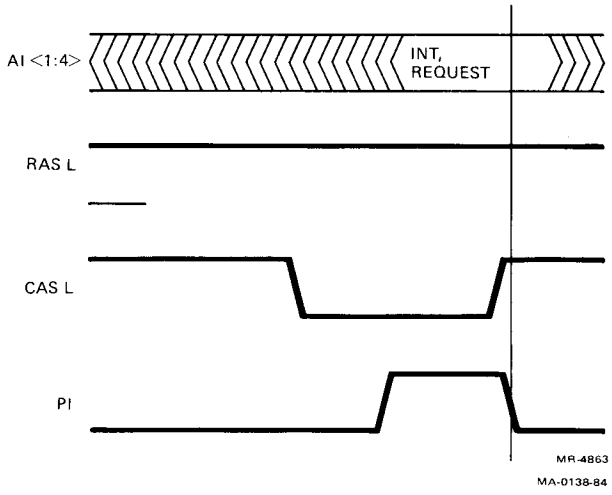


Figure 4-10 T11 ASPI Transaction Diagram

4.2.2 Mode Register

During power-up sequences, the T11 inputs the values of DALØ H -- DAL15 H and loads these values into its internal mode register. The loaded bits define operating parameters.

The mode register (Figure 4-11) drives five of the DAL lines low during power up sequences. INIT L goes low, enabling the mode register to pass ground values to the five DAL lines. All other DAL lines remain high, providing "1" states to the T11 for their values.

Table 4-1 lists the values associated with each of the 16 DAL lines during a power-up sequence, and defines the T11 operating modes selected by those DAL values.

Later in this chapter, Table 4-6 describes the signals shown in Figure 4-11.

4.2.3 Control Gates

The control gates generate control signal outputs in response to CPU control and flag signal signals. The control gates (Figure 4-12) consist of the following two decoding circuits.

- Output Flag Decode Gates -- decode SELØ -- SEL1 inputs to enable either refresh activity (REF H), or address strobe activity (RRAS L from DRAS L), with strobe activity occurring with or without I/O decode operation (BUSOP L).

- R/W Decode Gates -- decodes CPU read and write control signals (R/WHB H and R/WLB H), and asserts priority signals (PI H and PI L) into read and write control signal outputs.

Table 4-2 provides a truth table for the output flag decode gates. Table 4-3 provides a truth table for the read/write (R/W) decode gates. Later in this chapter, Table 4-6 describes the signals identified in Figure 4-12.

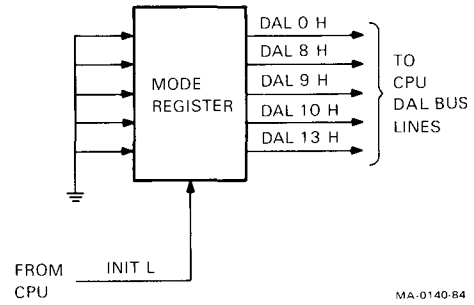


Figure 4-11 Mode Register

Table 4-1 DAL Signal Values During Power-Up Sequence

Bit	Value(s)	Mode Selection
DAL0 H	0	Constant clock timing input
DAL1 H	1	Standard microcycle (3 clock phases)
DAL2 H -- DAL7 H	All 1's	Reserved
DAL8 H	0	Normal read/write cycle
DAL9 H	0	Dynamic memory
DAL10 H	1	4K/16K memory
DAL11 H	0	16-bit bus
DAL12 H	1	User
DAL13 H -- DAL15 H	Octal 5	Start address of 000000/restart 000004

Table 4-2 Output Flag Decode Gates Truth Table

Input Values				Output Values	
SEL 0	SEL 1	DRAS L	REF H	RRAS L	BUSOP L
0	0	1	0	1	0
0	0	0	0	0	0
1	0	X	1	1	1
X	1	1	0	1	1
X	1	0	0	0	1

X = Don't care

Table 4-3 R/W Decode Gates Truth Table

Input Values				Output Values	
R/WHB H	R/WLB H	PI	RD H	DRD L	WLB L
1	1	1	1	Ø	1
1	1	Ø	1	1	1
Ø	1	X	Ø	1	1
X	Ø	1	Ø	1	Ø
X	Ø	Ø	Ø	1	1

X = Don't care

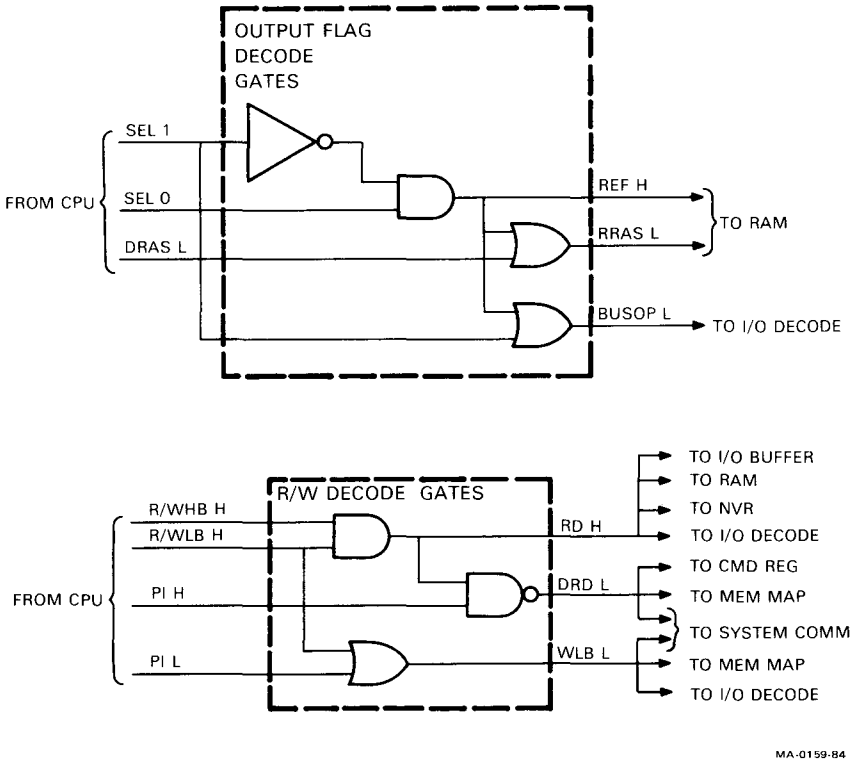


Figure 4-12 Control Gates Block Diagram

4.2.4 Address Latch

The T11 uses the DAL signal lines to define an address to be affected by read or write operations, and to transfer data to or from that address. The address latch (Figure 4-13) stores the address to be affected by a data transfer activity.

Later in this chapter, Table 4-6 describes the signals shown in Figure 4-13.

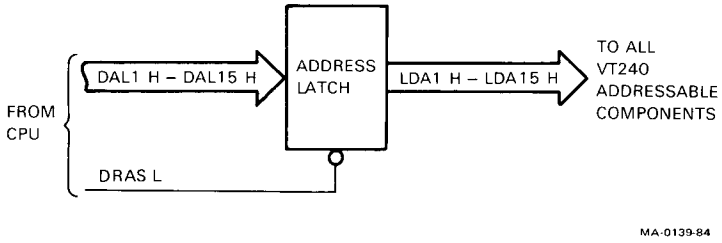


Figure 4-13 Address Latch Block Diagram

4.2.5 Memory Map

The memory map extends T11 addressing from 16 bits (32KW/64KB) to 20 bits (512KW/1MB), by adding address (from address latch) and data (from I/O buffer) inputs to develop values for the most significant 8 bits of the mapped 20-bit address.

The memory map (Figure 4-14) consists of the following circuits/conponents.

- Map Input Mux -- is enabled by MEM MAP CS L true (low) to pass values of LDA12 H -- LDA15 H to the inputs of the map adders. (When MEM MAP CS L is high, or false, LDA1 H through LDA4 H values are muxed through to the map adders. But, the map adders are disabled from using these signals by a high input from the map adders gate.)

- Map Adders Gate -- ORs MEM MAP CS L and WLB L to generate read/write control to the map adders, with a write control (low output) from the gate only when both inputs are true (low).

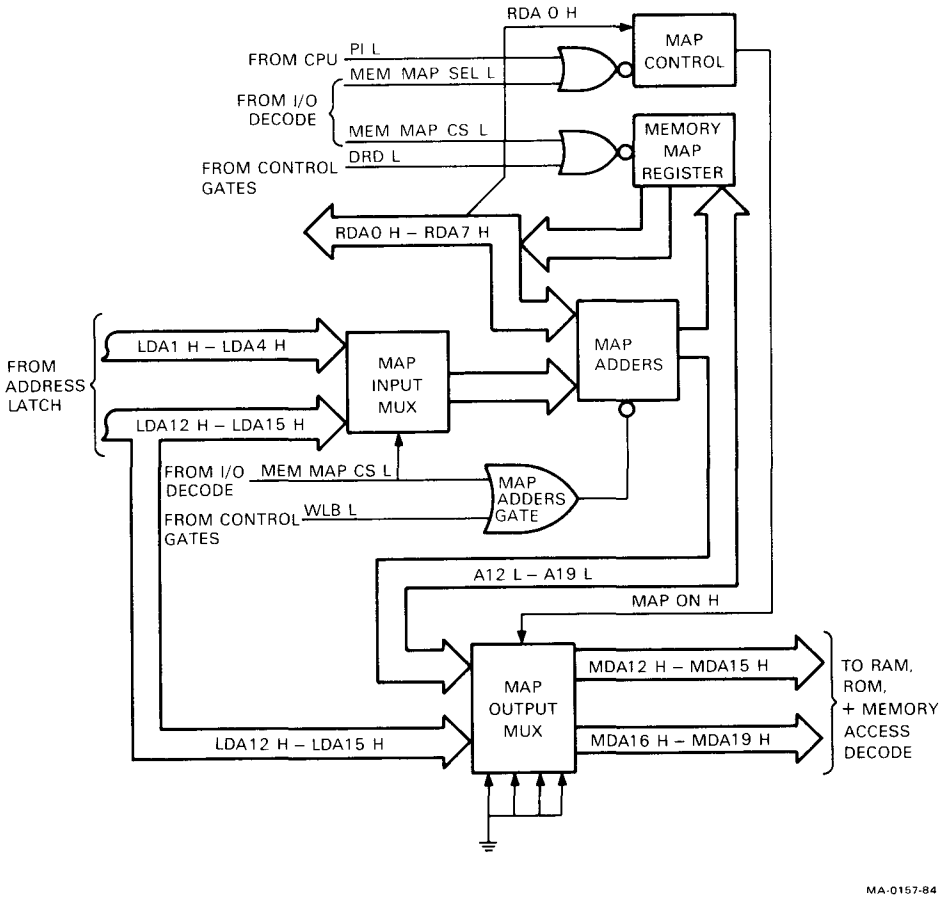


Figure 4-14 Memory Map Block Diagram

- Map Adders -- are two adder devices, each enabled by a low input from the map adders gate for write operation. One adds map input mux inputs to RDAØ H -- RDA3 H inputs from the I/O buffer, and the other adds map input mux signals against RDA4 H -- RDA7 H inputs from the I/O buffer. (When a high is present from the map adders gate, the adders are enabled to read out the value obtained during the last write operation.)

- Memory Map Register -- is enabled by ORed MEM MAP CS L and DRD L low inputs (both true) to output address values contained in the map adders. This gives T11 the means to verify value.

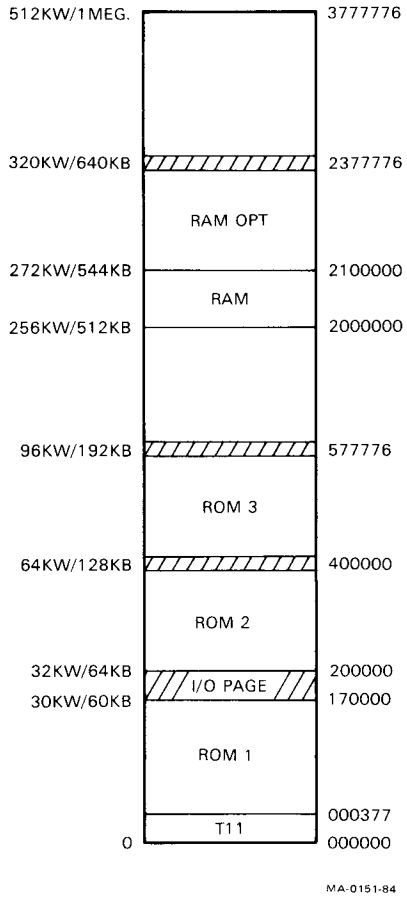


Figure 4-15 VT240-Series Terminal Address Map

- Map Control -- is set or reset, depending on the condition of RDAØ H, by ORed MEM MAP SEL L and PI L low inputs (both true), with the MAP ON H output acting as an input select signal for the map output mux.

- Map Output Mux -- consist of two mux devices, each enabled by MAP ON H high (true) to pass map adders inputs, or, when MAP ON H is low (false), to pass LDA12 H -- LDA15 H out as MDA12 H -- MDA 15 H, and all low conditions (from ground inputs) out as MDA16 H -- MDA19 H.

Figure 4-15 is an overall address map of the VT240. Later in this chapter, Table 4-6 describes the signals shown in Figure 4-14.

4.2.6 Memory Access Decode

Memory access decode generates the select signals for ROM and RAM access. Memory access decode is enabled by IO EN H low (false) and DRAS L low (true) to decode MDA inputs from the memory map into any of four possible signals. Three ROM select signals, or a select signal for RAM access (Figure 4-16).

Later in this chapter, Table 4-6 describes the signals shown in Figure 4-16.

4.2.7 Read Only Memory (ROM)

ROM stores the firmware required for terminal operation. A ROM can consist of up to six separate ROM devices, with a total ROM space of 96K bytes (Figure 4-17).

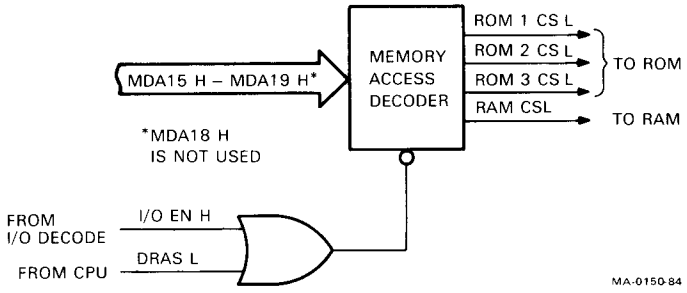


Figure 4-16 Memory Access Decode Block Diagram

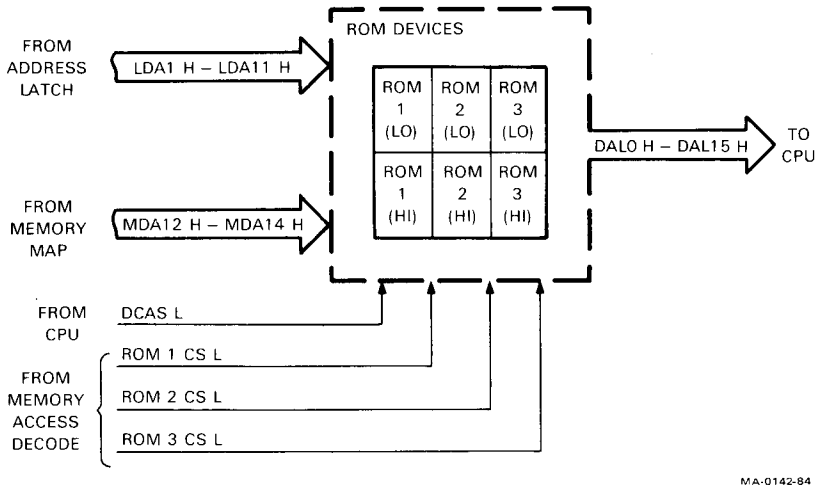


Figure 4-17 Read Only Memory (ROM) Block Diagram

Figure 4-17 shows how ROM is arrayed in the original version of the VT240 logic board. However, subsequent versions of the VT240 logic board have arrays that consist of four ROM devices: two 16K X 8 bit devices, and two 32K X 8 bit devices.

Regardless of the actual physical array, ROM select inputs (ROM1 CS L -- ROM3 CS L), in conjunction with address latch (LDA1 H -- LDA11 H) and memory map inputs (MDA12 H -- MDA14 H), define which location of ROM is to be read. The read occurs when DRAS L is low (true) at the same time as a low ROM Select input low (true).

Later in this chapter, Table 4-6 describes the signals shown in Figure 4-17.

4.2.8 Random Access Memory (RAM)

RAM provides the T11 with 32K byte/16K words of memory for various functions, such as buffer space, scratch pad operations, and data storage.

RAM is involved in three types of T11 transactions: read, write, and refresh.

During read and write transactions, addressing a specific memory location is done by first defining a row address (1 of 128), and then defining a column address (1 of 16) within that row. (Refer to Figure 4-6, the T11 timing diagram, and Figure 4-7 and Figure 4-8, the T11 read/write transaction diagrams.)

During refresh transactions, only row addressing is required. RAM is refreshed after 128 refresh cycles (one cycle for each of the 128 rows).

The RAM circuit (Figure 4-18) consists of the following circuits and components.

- RAM CAS Gates -- consists of nine gates that enable read (read word only) or write (write upper, lower, or both bytes). The gates generate CAS L outputs when RAM is selected and enabled, with one CAS signal for each byte of RAM to be accessed for a read/write transaction.

- RAM Address Buffer -- passes five least significant bits of row and column addresses. The buffer is transparent during row addressing, and latched during column addressing (DCAS L low, or true, is a latch enable that prevents buffer output values from being affected by new input values until DCAS L returns high.)

- RAM Address Input Mux -- is enabled by REF H to select either "B" or "A" inputs. The input mux selects "B" inputs (ground, AI7 H, and MUX H, which is tied to +5 V) when REF H is true (high). The input mux selects "A" inputs (MDA15 H, MDA13 H, and RRAS L), when REF H is low (false).

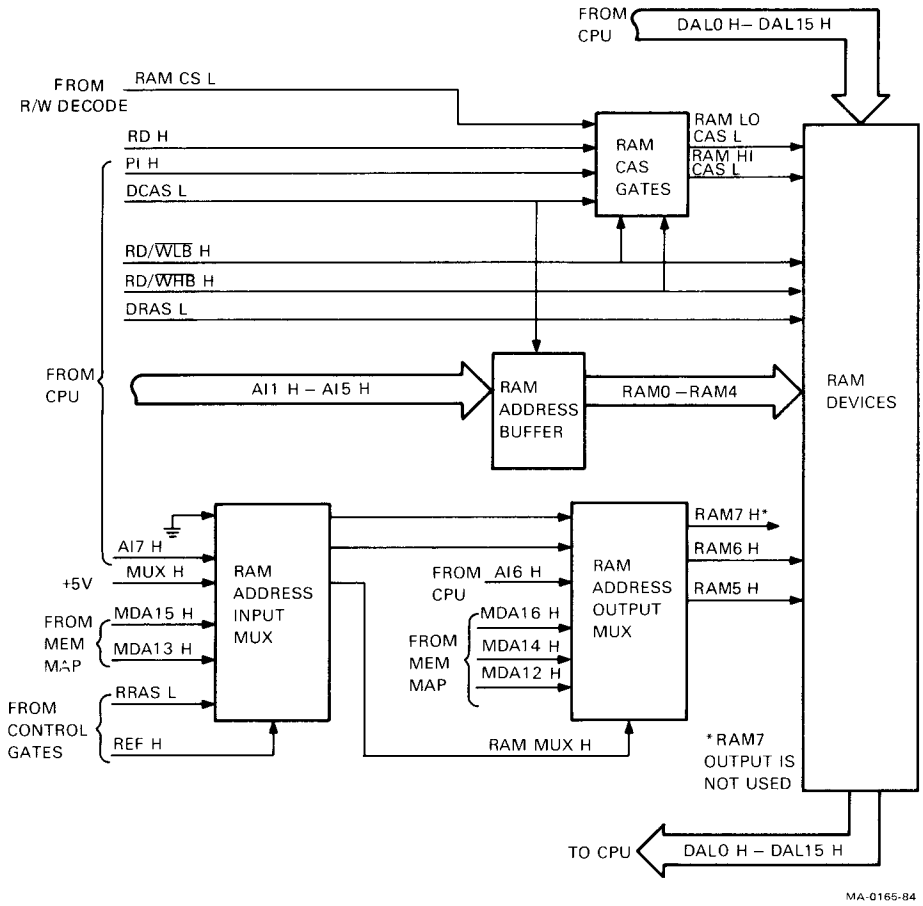


Figure 4-18 Random Access Memory (RAM) Block Diagram

- RAM Address Output Mux -- The output mux is enabled by RAM MUX H to select either "B" or "A" inputs. "B" inputs (ground, AI7 H passed by input mux, and AI6 H) when RAM MUX H is true (high developed from MUX H input to the input mux during refresh transactions). The output mux selects "A" inputs (MDA16 H, MDA14 H, and MDA12 H) when RAM MUX H is false (low developed from RRAS L input to the input mux during read/write transactions).

- RAM Devices -- consist of 16 MOS 16K bit X 1 RAM devices, arrayed in 2 banks of 8 bits. One bank is for the most significant byte of memory (enabled for read/write by DCAS L, DRAS L, and RD/WHB H inputs, and for refresh by RRAS L only). The other bank is for the least significant byte (enabled for read/write by DCAS L, DRAS L, and RD/WLB H inputs, and for refresh by RRAS L only).

Figure 4-19 is a diagram of the RAM CAS gates. Figure 4-20 is a diagram of the RAM device array. Later in this chapter, Table 4-6 describes the signals shown in Figures 4-18, 4-19, and 4-20.

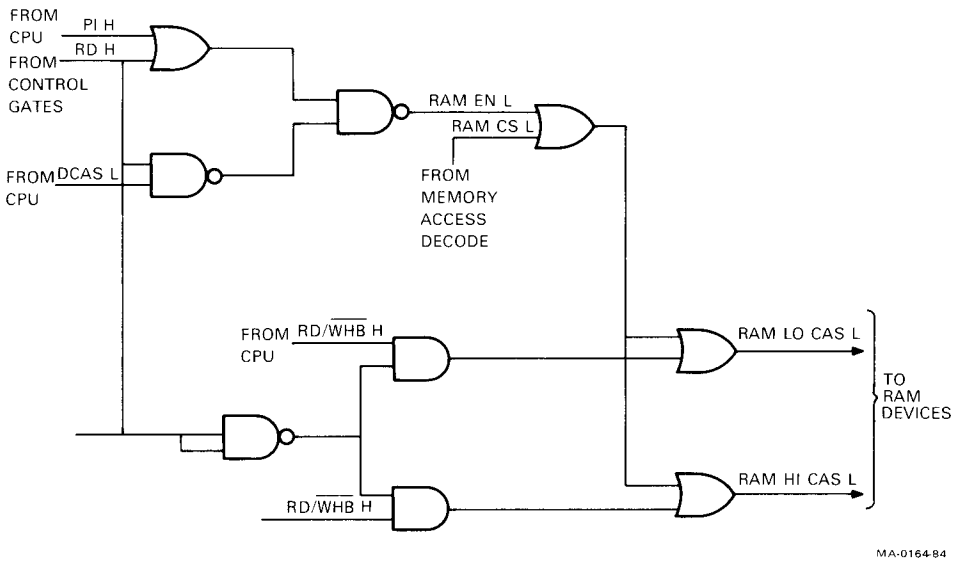


Figure 4-19 RAM CAS Gates

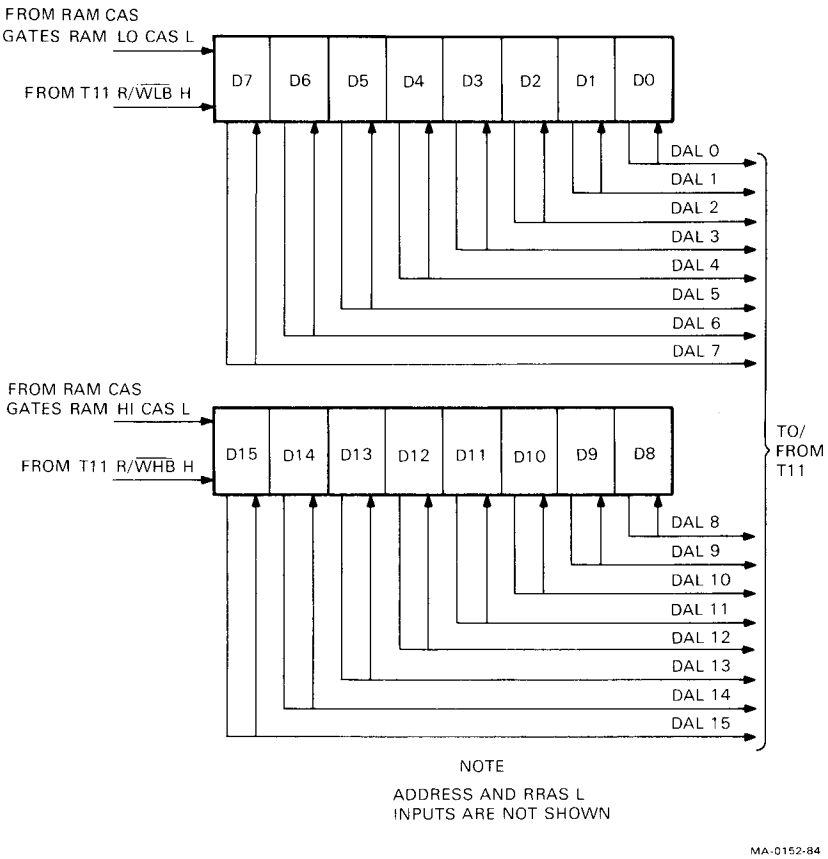


Figure 4-20 RAM Devices Array

4.2.9 I/O Buffer

The I/O buffer provides isolation between the DAL lines (16-bit bus, which the T11 uses for memory data transfers, and address data transfer to the address latch) and the RDA lines (eight-bit bus, which the T11 uses for data transfer to or from the various system I/O devices).

The I/O buffer (Figure 4-21) consists of the following components.

- I/O Buffer Device -- is a bidirection buffer enabled by DCAS L to pass data in direction determined by direction gate input.

- Direction Gate (DIR GATE) -- determines the direction of data transfer by the I/O buffer. Data is transferred from the RDA lines to the DAL lines only when both IO EN H and RD H are true (both high). Data is transferred from the DAL lines to the RDA lines for all other conditions (during T11 read/write of memory, data is transferred by the I/O buffer to the RDA lines, but has no effect, as no I/O device is enabled).

Later in this chapter, Table 4-6 describes the signals shown in Figure 4-21.

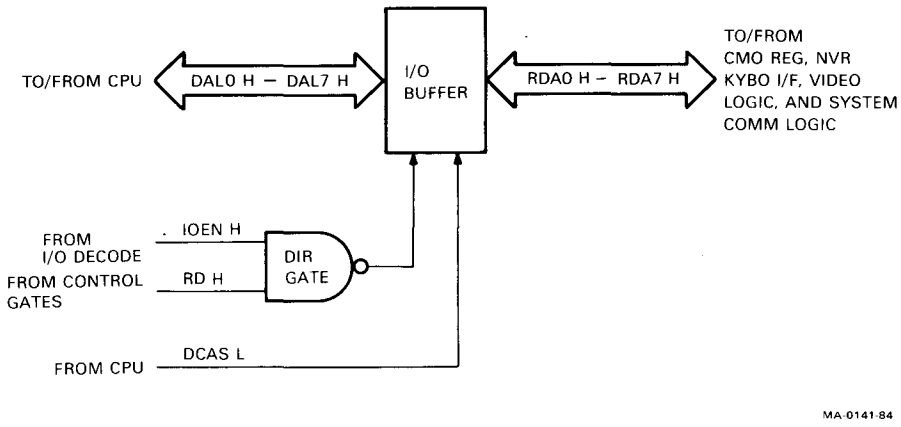


Figure 4-21 I/O Buffer Block Diagram

4.2.10 I/O Decode

The I/O decode circuitry decodes control and address inputs to determine when the T11 is attempting to access an I/O device, then generates the select signals needed for the access.

I/O decode (Figure 4-22) consists of the following circuits/components.

- I/O Enable Gates -- AND the most significant four bits of the address output from the address latch, providing partial enables to the I/O decoder and the I/O buffer, when all four bits are high (which occurs for octal code 17XXXX addresses).

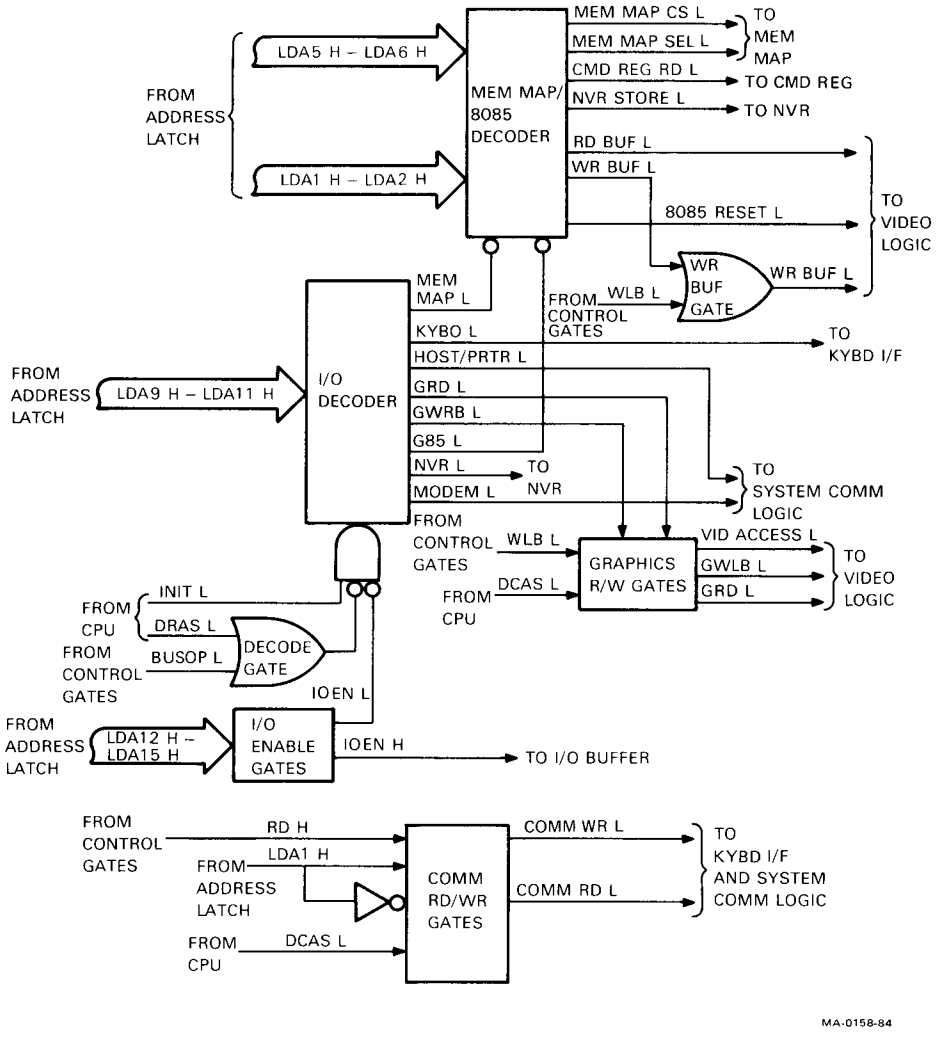


Figure 4-22 I/O Decode Block Diagram

- Decode Gate -- ORs DRAS L and BUSOP L, providing one enable to the I/O decoder when both are low (both true).

- I/O Decoder -- is enabled to decode LDA9 H -- LDA11 H into select outputs when INIT L is high (false), and when the decode gate and I/O enable gates are providing low inputs.

- Mem Map/8085 Decoder -- this dual decoder device is enabled to decode LDA5 H -- LDA6 H inputs into MEM MAP CS L, MEM MAP SEL L, CMD REG RD L, or NVR STORE L output, when MEM MAP L input from the I/O decoder is low (true). Or, the dual decoder device is enabled to decode LDA1 H -- LDA2 H inputs into RD BUF L, WR BUF L, or 8085 RESET L output, when G85 L input from the I/O decoder is low (true).

- WR BUF Gate -- ties the WR BUF L select signal to WLB L.

- Graphics R/W Gates -- consists of the AND gate and two OR gates. The AND gate generates a VID ACCESS L low output (true) whenever either GRD L or GWLB L is low (true). The OR gates tie GRD L to DCAS L, and GWLB L to WLB L.

- Communications (Comm) R/W Gates -- gates DCAS L with LDA1 signals to generate either COMM WR L (LDA1 signals true), or COMM RD L (LDA1 signals false). The RD H input is used to disable COMM WR L when RD H is true (high).

NOTE

The comm R/W gates operate independently of the remaining I/O decoder circuitry, but their outputs affect only an I/O device that is enabled by a specific I/O decoder select signal output.

Table 4-4 shows the address values for all the I/O decode select signal outputs.

Later in this chapter, Table 4-6 describes the signals shown in Figure 4-22.

Table 4-4 I/O Addresses

Signal	Octal Address	Destination
MEM MAP L	170XXX	MEM MAP/8085 decoder
MEM MAP CS L	1700XX	Memory map
MEM MAP SEL L	170040	Memory map
CMD REG RD L	170100	Command register
NVR STORE L	170140	NVR
KYBD L	17100X	Keyboard I/F
HOST/PRTR L	1720XX	System comm logic
GRD L	173000	Video logic
GWLB L	174000	Video logic
VID ACCESS L	173000/174000	Video logic
G8085 L	17500X	Video logic
RD BUF L	175000	Video logic
WR BUF L	175002	Video logic
8085 RESET L	175004	Video logic
NVR L	176XXX	NVR
MODEM L	17700X	System comm logic

X = Indicates that a specified select signal can be active for various addresses within the defined range, as different functions can be addressed while the specified select signal is active.

4.2.11 Keyboard Interface (I/F)

The keyboard I/F controls the data transfer between the T11 and the keyboard module. Parallel data for the keyboard (command or parameter information for the keyboard module) is written to the keyboard I/F, where it is converted to serial data, and transferred to the keyboard module. Serial data input from the keyboard module (key codes and status) is converted to parallel data, and read out of the keyboard I/F by the T11. The keyboard I/F uses interrupts to inform the T11 (via interrupt control) when the keyboard I/F is ready to transfer more data to the keyboard module, or when data from the keyboard module is ready for the T11.

The keyboard I/F (Figure 4-23) consists of the following circuits/components.

- 8251A USART Device -- is a programmable USART directly responsible for communications with the keyboard module.
- Loopback Gates -- are used for testing. The loopback gates are enabled by 8251A output (LPBK EN L developed from the DTR output of the 8251A) to route transmit (tx) data back to the 8251A as receive (rx) data.
- Keyboard Transmit Data (KYBD TxD) Buffers -- convert TTL level tx data signals from 8251A into +12 V/-12 V level outputs to the keyboard module.
- Keyboard Receive Data (KYBD RxD) Buffers -- convert +12 V/-12 V rx data signals from the keyboard module into TTL inputs to the 8251A.
- Keyboard Clock -- is a buffered output counter device which converts CLK2 H input from the clock generator (3.6864 MHz), into a clock input to the 8251A for general operation (1.8432 MHz) and an input for tx and rx timing (307.2 KHz).
- J6 -- is a four-pin telephone plug-type connector which provides a direct connection between the keyboard module and the system box (Figure 4-23 shows a pin-out of J6).

NOTE

The keyboard module can also connect to the monitor module, with keyboard data signals routed through J8 (shown in Figure 4-23).

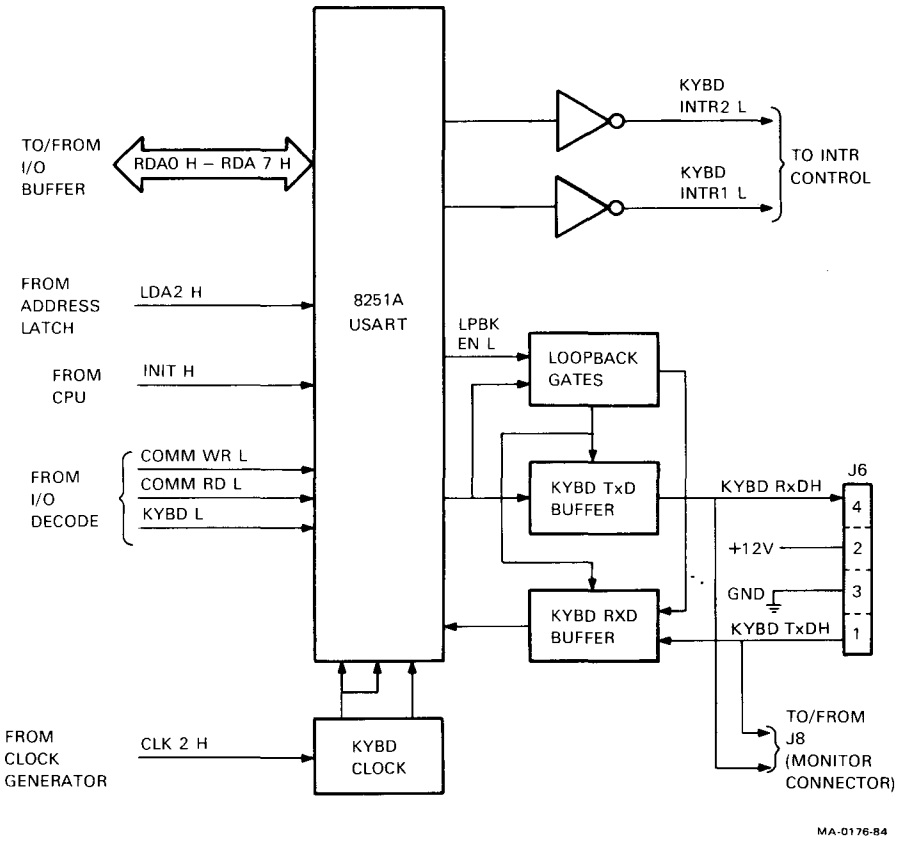


Figure 4-23 Keyboard Interface (I/F) Block Diagram

4.2.11.1 8251A USART Internal Circuits -- Figure 4-24 is a block diagram that shows the following major 8251A internal circuits.

- Data Bus Buffer -- buffers data transfer between the T11 (as RDAØ H -- RDA7 H) and registers within the 8251A (command, status, transmit data, and receive data register devices).

- Modem Control -- is used by the T11 to generate the loopback enable (LPBK EN L, generated by DTR output) for I/F testing.

- TxD Buffer -- converts parallel data input to a tx data register into serial output for the keyboard module.

- RxD Buffer -- converts serial data input to a rx data register into parallel data for transfer to the T11.

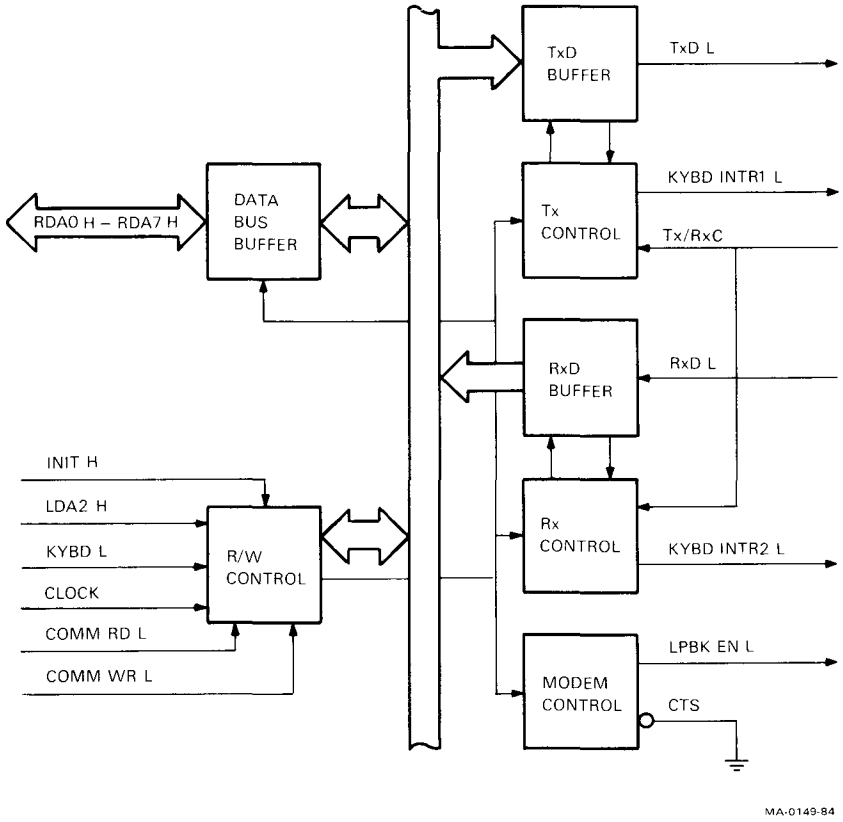


Figure 4-24 8251A USART Internal Circuits Block Diagram

- R/W Control -- contains command register programmed by the T11 to define 8251A operating parameters, as well as a status register to report operating conditions to the T11 and circuits required to determine what type of access is being attempted by the T11. The T11 can attempt the following types of access.
  - Data read (LDA2 H low, or false, with COMM RD L low, or true)
  - Data write (LDA2 H low, or false, with COMM WR L low, or true)
  - Command write (LDA2 H high and COMM WR L low, both true conditions)

- Status read (LDA2 H high and COMM RD L low, both true conditions)

NOTE

Used in VT240 Series terminal, T11 defines a baud rate of 4800 bits per second (bps), 10-bit characters (1 stop bit, 1 start bit, 8 data bits), and no parity check.

Later in this chapter, Table 4-6 describes the signals shown in Figures 4-23 and 4-24.

4.2.11.2 8251A USART Addresses -- The T11 accesses various 8251A internal registers to program control, read status, and transfer data to and from the 8251A. The T11 does this by addressing either control/status registers (KYBD L low, with LDA2 H high, both true conditions), or data registers (KYBD L low, or true, and LDA2 H low, or false), for either read (COMM RD L low, or true) or write activity (COMM WR L low, or true).

When programming 8251A operation, the T11 must write two separate bytes of programming. The first byte written defines the mode instruction format; the second byte written defines the command data for that mode format. Both bytes are written to the 8251A command register immediately following a power-up sequence, or following an 8251A internal reset.

Table 4-5 defines the 8251A internal registers that the T11 can address, the register's address, the type of operation that affects the register (read or write), and the 8251A circuit in which the register resides.

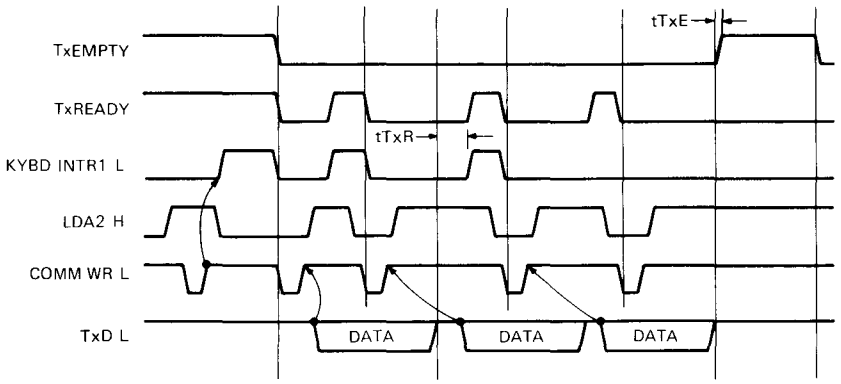
NOTE

Appendix D provides a complete description of the bit values for the command and status registers. This manual does not give any further description of the data registers.

Table 4-5 8251A USART Addresses

Address	RD/WR	Circuit	Register
171006	WR	R/W control	Command register
171004	RD	R/W control	Status register
171002	WR	TxD buffer	TxD register
171000	RD	RxD buffer	RxD register

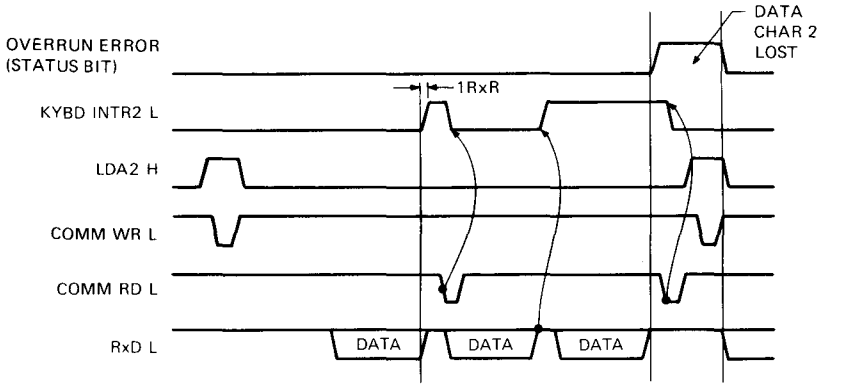
4.2.11.3 8251A USART Timing Diagrams -- Figure 4-25 is a timing diagram for transmit data transfer activity. Figure 4-26 is a timing diagram for receive data transfer activity.



NOTES
1. KYBD INTR1 L IS SHOWN ENABLED FOR rx READY CONDITION.
2. tTxR IS A MAXIMUM OF 8 CLOCK PERIODS.
3. tTxE IS A MAXIMUM OF 20 CLOCK PERIODS.

MA-0154-84

Figure 4-25 8251A USART Transmit Data (TxD) Timing Diagram



NOTES
1. KYBD INTR2 L IS SHOWN ENABLED FOR RX READY CONDITION.
2. TRxR IS A MAXIMUM OF 8 CLOCK PERIODS.
3. COMM RD L IS LOW (TRUE) FOR READING RX DATA, AND COMM WR L IS LOW (TRUE) FOR WRITING CONTROL FOR RX DATA INPUT.
4. LDA 2 H IS SHOWN HIGH (TRUE) FOR WRITING CONTROL FOR RX DATA INPUT, AND LOW (FALSE) FOR READING RX DATA.

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Figure 4-26 8251A USART Receive Data (RxD) Timing Diagram

4.2.12 Nonvolatile RAM (NVR)

The NVR combines a 256 X 4 bit static RAM with a 256 X 4 bit electically erasable ROM (EPROM) to provide memory for storing terminal operating parameters, and allow those parameters to be manipulated by the operator.

During a power-up sequence, data is transferred from the EPROM to the NVR RAM portion. While in the NVR RAM, the data stored can be altered. Operator keyboard input defines a new parameter, with the T11 directing a write to NVR to alter the stored value.

Operator keyboard input can direct the terminal to save the parameters currently stored in the NVR RAM as the new default values for the terminal. When this occurs, the T11 directs the transfer of values stored in the NVR RAM to be written into the EPROM, effectively reprogramming the EPROM. At the next power-up sequence, the new EPROM values are transferred back into the NVR RAM, and these values now determine the terminal's starting parameters.

The NVR (Figure 4-27) consists of the following circuits/components.

- NVR Strobe Gates -- are enabled by NVR STORE L low (true) and LDA8 H low (false) to generate a store input to the NVR device. The store input causes the NVR device to transfer the values stored in its RAM memory into its EPROM memory, reprogramming the EPROM.

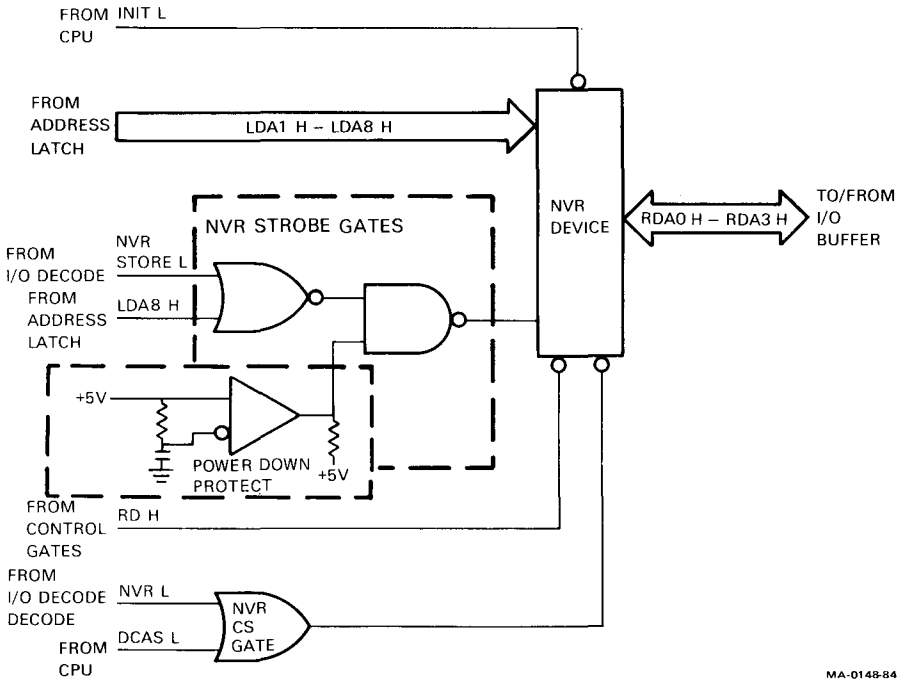


Figure 4-27 Nonvolatile RAM (NVR) Block Diagram

- Power Down Protect -- disables the NVR strobe output upon sensing power-down condition to prevent the T11 from accidently writing to NVR.

- NVR CS Gate -- generates a chip select (CS) to the NVR device when both NVR L and DCAS L are lows (both true). The CS input enables read or write transactions that affect the RAM memory portion of the NVR device.

- NVR Device -- contains the RAM and EPROM memories that perform the following NVR functionality.

    - Read Terminal Operating Parameters -- RD H is true (high), DCAS L and NVR L are both low (both true), and LDA1 H -- LDA8 H define the portion of the NVR device's RAM memory to be affected.

    - Write Terminal Operational Parameters -- This is the same as a read transaction, except RD H is low (false).

    - Store RAM Values in EPROM -- NVR STORE L is low (true), with LDA8 H low (false).

    - Transfer EPROM Values to RAM -- INIT L goes low (true) during the power-up sequence.

Later in this chapter, Table 4-6 describes the signals shown in Figure 4-27.

4.2.13 Interrupt Control

The interrupt control circuitry provides information about any pending interrupt requests to the T11. This information is sent to the T11 as a four-bit code (AI1 H -- AI4 H) whenever PI L goes low (true).

Interrupt control (Figure 4-28) consists of the following components.

- Interrupt (INTR) Buffer -- is a latched output buffer device. The value of its inputs are clocked into the output and latched (by grounded enable input) at each DCAS L low (true) condition.
- Interrupt (INTR) Memory -- is a 512 X 4 bit ROM enabled by PI L low (true) to output (as AI1 H -- AI4 H) the four-bit code at the memory location defined by inputs from the interrupt buffer (PROD TEST2 L input is always high, or false, as it is tied to +5 V) with this four-bit code defining the current interrupt status to the T11.

Later in this chapter, Table 4-6 describes the signals shown in Figure 4-28.

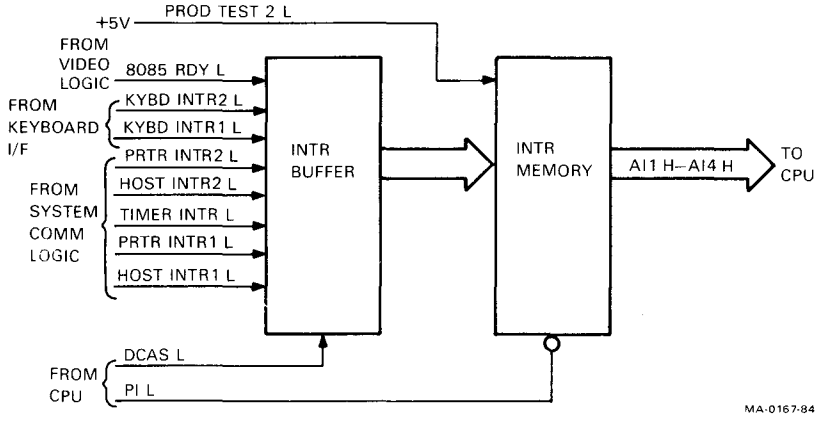


Figure 4-28 Interrupt Control Block Diagram

4.2.14 Command Register

The command register reports the status of various system conditions to the T11 when the T11 directs a read transaction that affects this register.

The command register (Figure 4-29) consists of the following components.

- Command Register (CMD REG) Gate -- enables output from the command register when CMD REG RD L and DRD L are both low (both true).
- Command Register -- is a latched output buffer device. The value of its inputs are clocked into the output on each DCAS L low (true) condition, and those values read out of the register (as RDAØ H -- RDA7 H) whenever a low is input from the command register gate.

Later in this chapter, Table 4-6 describes the signals shown in Figure 4-29.

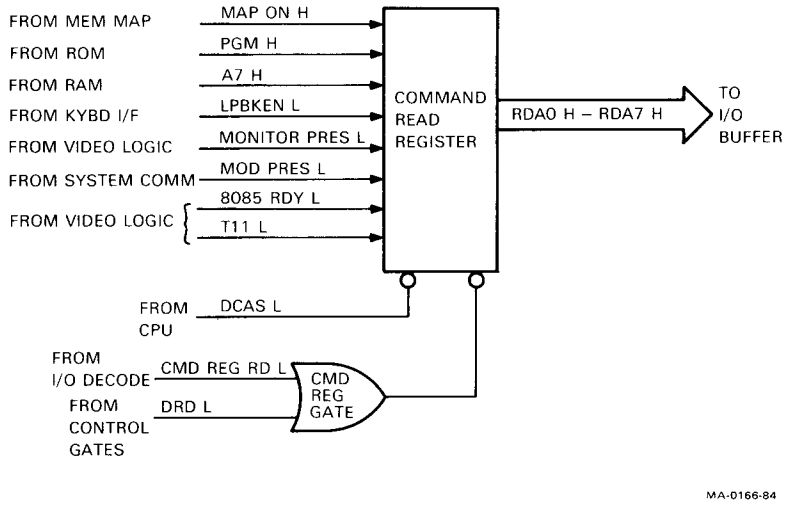


Figure 4-29 Command Register Block Diagram

4.2.15 Clock Generator

The clock generator generates the main clock signals required for the T11, keyboard controller, and system communication logic operations (separate clock signals are generated for video logic operations).

The clock generator (Figure 4-30) consists of the following components.

- Crystal (XTAL) -- generates a 7.3728 MHz output used at the CPU, and a 3.6864 output used by the keyboard interface and system communication logic circuits.
- Clock Buffer (CLK BUF) -- buffers the 7.3728 MHz output to the T11.

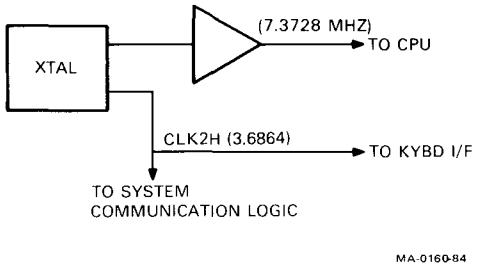


Figure 4-30 Clock Generator Block Diagram

4.3 SIGNAL DESCRIPTIONS

Table 4-6 gives descriptions of all the signals identified in this chapter. These descriptions are provided for reference, and are listed alphabetically by mnemonic (numeric mnemonics are listed last).

4.4 SCHEMATIC REFERENCE INFORMATION

Table 4-7 identifies the logic board component coordinate, and the schematic page and coordinates for each CPU logic circuit/component identified in this chapter.

NOTE
The reference listing is based on Rev. C of the schematics (CS5415495-0-1).

Table 4-6 CPU Logic Signal Descriptions

Signal Mnemonic	Signal Name	Description
A7	Address Bit 7	Status input from RAM reserved for use with 64K RAM (currently tied to +5 V).
A12 L -- A19 L	Address Data Lines 12 through 19 Low	Active output from map address used to develop mapped address when memory map is on.
AI1 H -- AI7 H	Address Interrupt Lines 1 through 7 High	Used by T11 to output RAM address values and to input interrupt data from the interrupt control.
BUSOP L	Bus Operation Low	Control output from control gates disabling I/O decode when T11 is in ASPI cycle.
CLK2 H	Clock 2 High	3.6864 MHz output from clock generator which provides general timing for CPU and system communication logics components.
CLOCK	Clock	1.8432 MHz input to 8251A from keyboard clock developed from CLK 2 H signal.
CMD REG RD L	Command Register Read Low	True (low) output from I/O decode enabling T11 access of command register for read transaction.
COMM RD L	Communication Read Low	Control signal output from I/O decode which, when true (low), partially enables a read transaction affecting a communication device (either the 8251A keyboard controller, or the DUART in the system communication logic).
COMM WR L	Communication Write Low	Same as COMM RD L, except enables write transaction.

Table 4-6 CPU Logic Signal Descriptions (Cont)

Signal Mnemonic	Signal Name	Description
CTS	Clear To Send	Input to 8251A which is tied to ground to be always true.
DALØ H -- DAL15 H	Data Address Lines Ø through 15 High	Used by T11 for output of data and address values, and for input of data.
DCAS L	Direct Column Address Strobe Low	Control signal output from T11 used to enable various circuits and components for operation.
DRAS L	Direct Row Address Strobe Low	Control signal output from T11 used to enable various circuits and components for operation.
DRD L	Delayed Read Low	Control signal output from the control gates whenever a read activity involving a fast I/O device is to occur.
G85 L	Graphics 8Ø85 Low	Enable to mem map/8Ø85 decoder to allow this device to decode inputs into video logic select signal.
GND	Ground	Operational potential output to keyboard module (J6, pin 3, or via J8).
GRD L	Graphics Read Low	Select signal from I/O decode enabling T11 access of graphics controller in video logic for a read transaction.
GWLB L	Graphics Write Low Byte Low	Select signal output from I/O decode enabling T11 access of graphics controller in video logic for a write transaction.

Table 4-6 CPU Logic Signal Descriptions (Cont)

Signal Mnemonic	Signal Name	Description
HOST INTR1 L	Host Interrupt 1 Low	Interrupt originating at DUART in system communication logic and indicating DUART has data received from the host that is ready for the T11.
HOST INTR2 L	Host Interrupt 2 Low	Interrupt originating at DUART in system communication logic and indicating DUART is ready to process data for a host device.
HOST/PRTR L	Host/Printer Low	Select signal output from I/O decode enabling T11 access of DUART in system communication logic for read/write transaction.
INIT H -- INIT L	Initialize High and Low	Initialize system during power-up sequence to known starting state.
IO EN H -- IO EN L	I/O Enable High and Low	Active outputs from I/O enable gates whenever any address within the 17XXXX octal range is being output from the address latch.
KYBD L	Keyboard Low	Select signal output from I/O decode enabling T11 access of the 8251A keyboard controller for read/write transaction.
KYBD INTR1 L	Keyboard Interrupt 1 Low	Interrupt output from 8251A when receive data is ready for processing.
KYBD INTR2 L	Keyboard Interrupt 2 Low	Interrupt output from 8251A when ready to process transmit data.
KYBD RxD H	Keyboard Receive Data High	Data input to keyboard module via J6, or J8.

Table 4-6 CPU Logic Signal Descriptions (Cont)

Signal Mnemonic	Signal Name	Description
KYBD TxD H	Keyboard Transmit Data High	Data input from keyboard module via J6, or J8.
LDA1 H -- LDA15 H	Latched Address Lines 1 through 15 High	Address outputs from the address used to access memory and I/O devices.
LPBK EN L	Loopback Enable Low	Test control signal enabling TxD L from 8215A to be looped back to the 8251A as RxD L. Also used as status input to command register to report loopback condition.
MAP ON H	Map On High	Enables memory map to select mapped address values for output when true (high), and regular address values when false (low). Also used as status input to command register to report memory map on or off condition.
MDA12 H -- MDA19 H	Mapped Address Lines 12 through 19 High	Most significant 8 bits of mapped 20-bit address output from the memory map.
MEM MAP L	Memory Map Low	Enables memory map/8085 decoder to decode inputs into a select output for memory map, command register, or NVR access by the T11.
MEM MAP CS L	Memory Map Chip Select Low	Selects signal output from I/O decode enabling memory map address to add data and address to achieve new mapped address value.
MEM MAP SEL L	Memory Map Select Low	Selects signal output from I/O decode enabling T11 to turn memory map on and off.

Table 4-6 CPU Logic Signal Descriptions (Cont)

Signal Mnemonic	Signal Name	Description
MOD PRES L	Modem Present Low	True (low) status input to the command register from the system communication logic whenever the integral modem is installed in the terminal.
MODEM L	Modem Low	Selects signal output from I/O decode enabling T11 access of various comm and modem control and status registers within the system communication logic.
MONITOR PRES L	Monitor Present Low	True (low) status input to command register from video logic whenever a monitor is hooked up to the system.
NVR L	NVR Low	Selects signal output from I/O decode enabling T11 access of NVR for read/ write transaction.
NVR STORE L	NVR Store Low	Selects signal output from I/O decode which enables transfer of data from NVR RAM to NVR EPROM.
PGM H	Program High	Status signal from ROM reserved for use with 32K ROM.
PI L -- PI H	Priority In Low and High	Control signal outputs for the T11 which are active signals during read, write, and ASPI transactions.
PRTR INTR1 L	Printer Interrupt 1 Low	Interrupt origianting at DUART in system communication logic and indicating receive data from a device on printer port is ready for the T11.

Table 4-6 CPU Logic Signal Descriptions (Cont)

Signal Mnemonic	Signal Name	Description
PRTR INTR2 L	Printer Interrupt 2 Low	Interrupt originating at DUART in system communication logic and indication DUART is ready to process data for a device on the printer port.
R/WLB H -- R/WHB H	Read/Write Low Byte and Read/Write High Byte Highs	Read/write control outputs from T11 defining type of read/write transaction to occur.
RAMØ -- RAM4	RAM Address Bits Ø through 4	Outputs from RAM address buffer which provide least significant four bits of column and row addresses to RAM for read/write transactions (or of row address for refresh transaction).
RAM5 H -- RAM6 H	RAM Address Bits 5 and 6 High	Outputs from RAM address output mux defining the most significant two bits of row address for refresh or read/write transactions.
RAM7 H	RAM Address Bit 7 High	Reserved for use with 64K RAM (currently tied to +5 V).
RAM CS L	RAM Chip Select Low	True (low) output from memory access decode whenever RAM is to be accessed for read/write transaction.
RAM HI CAS L	RAM High Byte Column Address Strobe Low	True (low) output from RAM CAS gates when active column address is being applied to the high byte array of RAM.

Table 4-6 CPU Logic Signal Descriptions (Cont)

Signal Mnemonic	Signal Name	Description
RAM LO CAS L	RAM Low Byte Column Address Strobe Low	True (low) output from RAM CAS gates when active column address is being applied to the low byte array of RAM.
RAM MUX H	RAM Mux High	True (High) output from RAM address input mux when RAM address output mux is to select address value for refresh activity, and false (low) output when address value is to be selected for RAM read/write transaction.
RD H	Read High	Control signal output from control gates true (high) for read transactions.
RD BUF L	Read Buffer Low	Select signal output from I/O decode enabling T11 access of data buffer in video logic for read transaction.
RDAØ H -- RDA7 H	Remote Data Lines Ø through 7 High	Used for transfer of data between the T11 (via I/O buffer) and the various system I/O devices.
REF H	Refresh High	Control signal output from the control gates during refresh transactions affecting RAM.
ROM1 CS L	ROM 1 Chip Select Low	True (low) output form memory access decode whenever ROM1 is to be accessed for a read transaction.
ROM2 CS L	ROM 2 Chip Select Low	True (low) output form memory access decode whenever ROM2 is to be accessed for a read transaction.

Table 4-6 CPU Logic Signal Descriptions (Cont)

Signal Mnemonic	Signal Name	Description
ROM3 CS L	ROM 3 Chip Select Low	True (low) output form memory access decode whenever ROM3 is to be accessed for a read transaction.
RRAS P	Remote Row Address Strobe Low	Control signal output from the control gates when T11 is to access RAM for read/write activity.
RxD L	Receive Data Low	Data input to 8251A originating at the keyboard module.
SELØ -- SEL1	Select Ø and 1	T11 output providing two-bit code to control gates with code value defining the type of transaction to occur.
T11 L	T11 Low	Status signal input to command register, low when T11 has written data to character processor (CP) in video logic, and high when last data written has been read by the CP.
TIMER INTR L	Timer Interrupt Low	Programmable interrupt condition orginating at DUART in system communication logic.
Tx/Rx C	Transmit/Receive Clock	3Ø7.2 kHz input to 8251A from keyboard clock used for transmit and receive timing and developed for CLK 2 H (3.6864 MHz).
TxD L	Transmit Data Low	Data output from 8251A for keyboard module.
VID ACCESS L	Video Access Low	Select Signal output from I/O decode whenever T11 is to access data buffer for read or write transaction.

Table 4-6 CPU Logic Signal Descriptions (Cont)

Signal Mnemonic	Signal Name	Description
WLB L	Write Low Byte Low	Control signal output for the control gates whenever a write transaction affecting an I/O device is to occur.
WR BUF L	Write Buffer Low	Select signal output from I/O decode enabling T11 access of data buffer in video logic for write transaction.
XTAL 1	Crystal 1	Clock input to T11 from clock generator (7.3728 MHz).
+12 V	+12 V dc	Operating output to keyboard module (via J6, pin 2, or via J8).
8Ø85 RDY L	8Ø85 Ready Low	Interrupt condition input to interrupt control from 8Ø85 at video logic whenever the 8Ø85 requires T11 access.
8Ø85 RESET L	8Ø85 Reset Low	Select signal output from I/O decode to reset 8Ø85 device in video logic whenever true (low).

Table 4-7 CPU Logic Schematic References

Circuit/Component	Logic Board Reference Numbers	Schematic Page	Coordinate
Address latch	E41,E43	1	C2--C3
Clock generator	E45,Y2	1	D8
CMD REG gate	E90	5	B3
COMM RD/WR gates	E48,E62	6	C7
Command read register	E91	5	C2
Decode gate	E69	5	C7
DIR gate	E47	1	D4
Graphics R/W gates	E72,E90	5	D4
INTR buffer	E75	1	B2
INTR memory	E74	1	B1
I/O buffer	E55	1	D3
I/O decoder	E68	5	D7
I/O enable gates	E47,E54	1	B1--B2
J6	J6	6	B2
KYBD clock	E27,E45	6	B5--B6
KYBD RxD buffers	E62,E66,E67	6	B2--B4
KYBD TxD buffers	E31,E69	6	C5--C6
LDA 1 INV	E44	1	D2
Loopback gates	E31,E61,E62,E67	6	B4,D3,D4
Map adders	E133,E134	2	D6,C6
Map adders gate	E71	2	B7
Map control	E73B	5	D2
Map input mux	E152	2	D7
Map output mux	E132,E151	2	D4,C4
MEM map/8085 decoder	E89	5	C7
MEM map register	E135	5	B2
Memory decode	E35,E53	3	A7,A8,B7
Mode register	E40	1	D5
NVR CS gate	E69	5	A5
NVR device	E56	5	B4
NVR store gates	E50,E70,E83	5	A5--A7
Output flag decode gates	E44,E47,E71,E72	1	B5--B6
Power down protect	E50	5	A7
RAM address buffer	E42	4	B7
RAM address input mux	E87	3	D2
RAM address output mux	E86	3	C2
RAM DAS gates	E28,E35,E48,E49	3	A6,A2,A3, B2,B3
RAM devices	E1--E16	4	D2-D5, B2-B5
ROM devices	E19--E22,E39,	3	D7,D4
T11	E85,E23,E28,E44	1	B7--07/ B6/06
WR BUF GATE	E62	5	C4
8251A UART	E44,E61	6	C6-D6/D4

CHAPTER 5
SYSTEM COMMUNICATION LOGIC

5.1 GENERAL

The system communication logic (shaded area in Figure 5-1) interfaces with the printer port, and either the integral modem option or the host (via the EIA host port or 20 mA port).

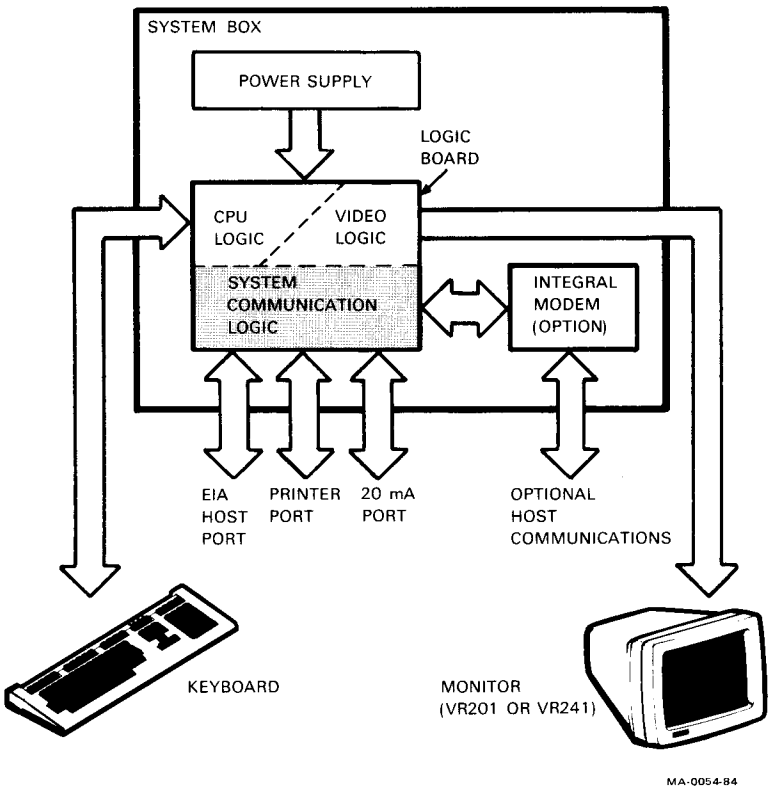


Figure 5-1 VT240-Series Terminal System Block Diagram

Printer interfacing is independent of host and integral modem interfacing. Host and integral modem interfacing, however, are not independent: when one interface is enabled (integral modem, EIA host port, or 20 mA port), the other two interfaces are disabled.

NOTE

Enabling and disabling the host and integral modem option interfaces is primarily a function of firmware response to system configuration data supplied by set-up features.

System communication logic operation is completely under CPU logic control. The CPU logic programs operating parameters, reads status, and directs data transfer to and from the system communication logic.

5.2 MAJOR CIRCUITS/COMPONENTS

Figure 5-2 is a block diagram that identifies the following major circuits/components that make up the system communication logic.

- Dual asycronous receiver/transmitter (DUART)
- Communications/modem control (COMM/MOD CONTROL)
- Communication multiplexer (COMM MUX)
- Printer interface (PRINTER I/F)
- EIA host interface (EIA HOST I/F)
- 20 mA interface (20 mA I/F)
- Integral modem option connector (J5)

5.2.1 Dual Asynchronous Receiver/Transmitter (DUART)

The DUART transfers host and printer data between the CPU logic and the following interfaces.

- EIA host interface
- 20 mA interface or integral modem for host data
- Printer interface for printer data

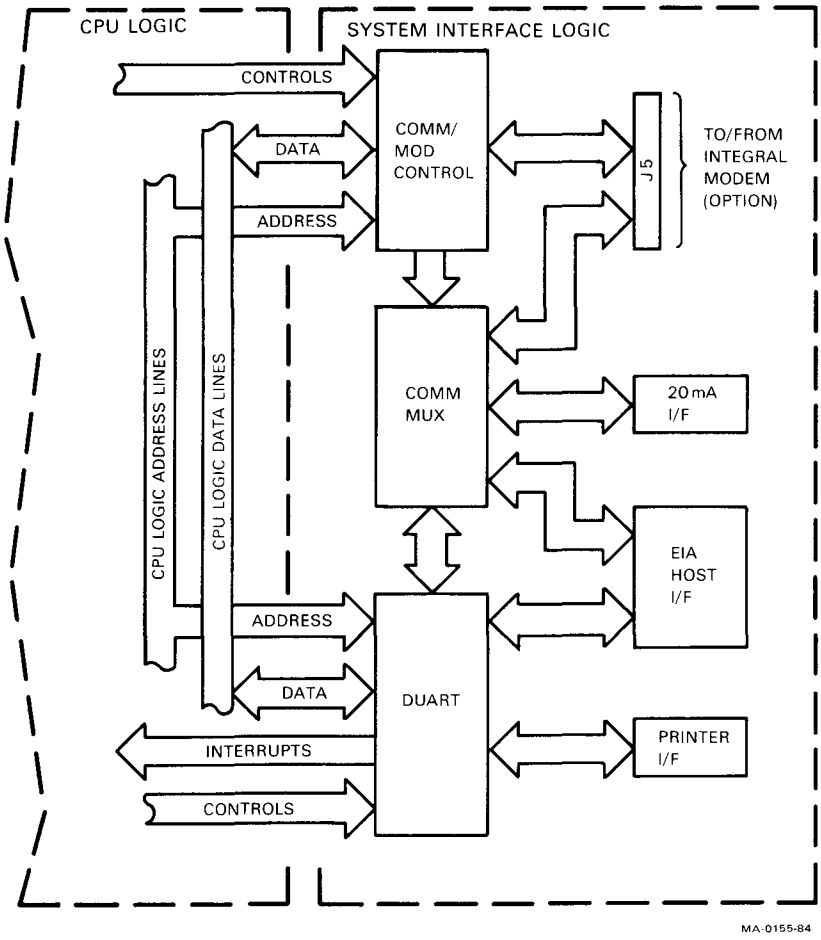


Figure 5-2 System Communications Logic Block Diagram

Figure 5-3 shows the following DUART components.

- 2681 DUART Device -- performs the data transfer functions.
- MOD CD GATE -- consists of two gates, an AND and an OR.

  OR -- disables MOD1 CD L from EIA HOST I/F during integral modem operation (CSL1 H high gated with MOD1 CD L).

  AND -- gates OR output with MOD2 CD L from integral modem to generate single MOD CD L input to DUART.

5.2.1.1 2681 DUART Internal Circuits -- Figure 5-4 is a block diagram that shows the following major 2681 DUART internal circuits.

- Data Bus Buffers -- transfer data between the 2681 DUART's internal circuits and the CPU logic data lines.

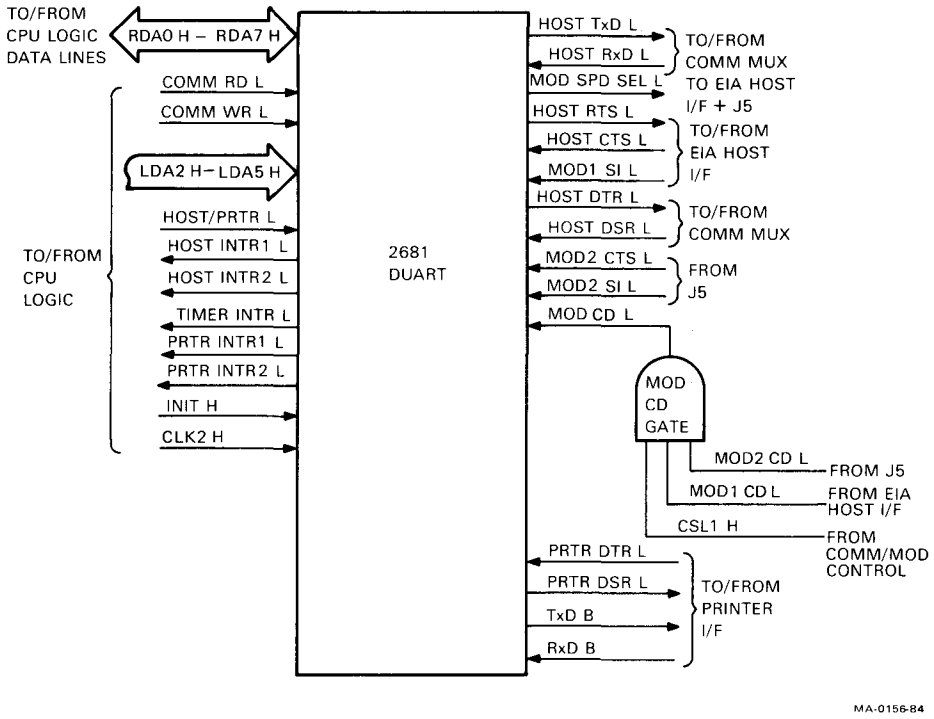


Figure 5-3 DUART Block Diagram

- Operation Control -- decodes read (COMM RD L), write (COMM WR L), address (LDA2 H -- LDA5 H), and chip enable (HOST/PRTR L) inputs to enable CPU logic access to control, status, and data registers within the various 2681 DUART circuits.

- Timing -- generates the clock and baud rate signals required for operation.

- Channel A (Host) -- converts host transmit data to serial data output (HOST TxD L), and serial host receive data input (HOST RxD L) to parallel data.

- Channel B (Printer) -- converts printer port transmit data to serial data output (TxD B), and serial printer port receive data (RxD B) to parallel data.

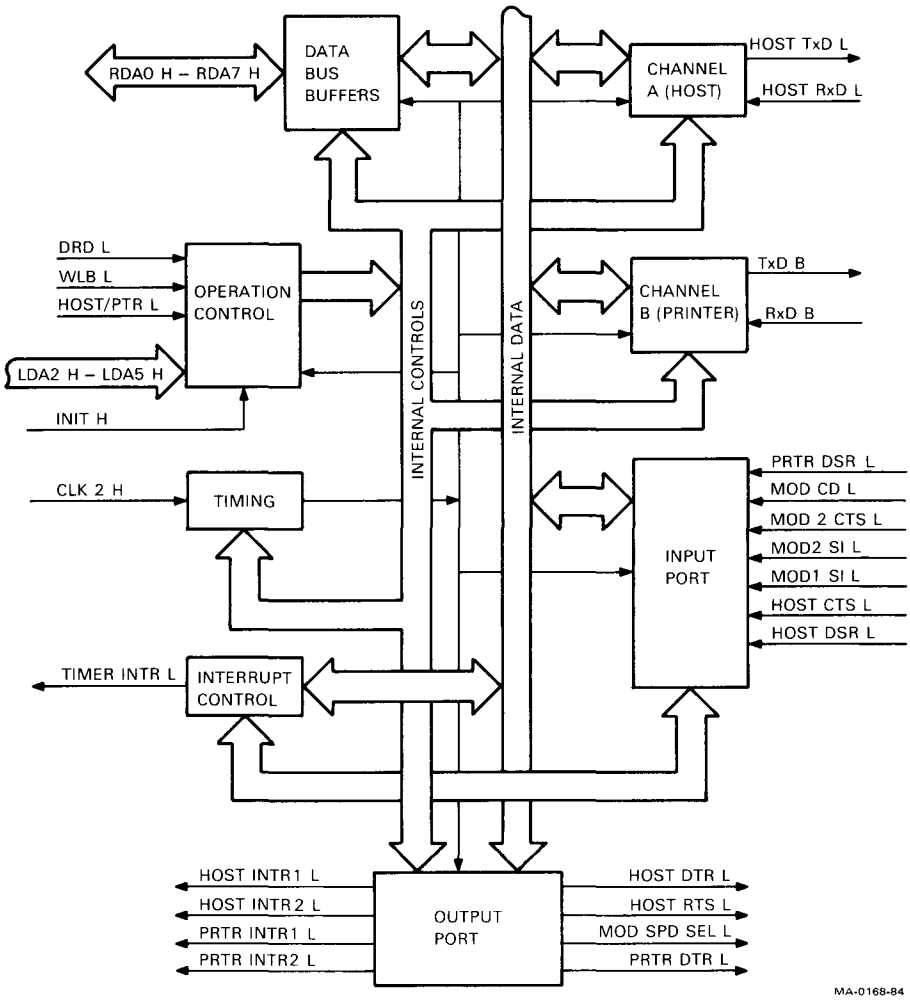


Figure 5-4 2681 DUART Internal Circuits Block Diagram

- Interrupt -- generates a programmable interrupt (TIMER INTR L) to the CPU logic.

- Output Port -- contains eight output ports programmed to provide interrupt outputs (HOST INTR1 L, HOST INTR2 L, PRTR INTR1 L, and PRNT INTR2 L), data terminal ready outputs (HOST DTR L and PRTR DTR L), and modem handshaking outputs (HOST RTS L and MOD SPD SEL L).

- Input Port -- contains state change detection devices, and seven input ports programmed to accept data set ready inputs (PRTR DSR L and HOST DSR L), and modem handshaking inputs (MOD CD L, MOD1 CTS L, MOD2 CTS L, MOD1 SI L, and MOD2 SI L).

Later in this chapter, Table 5-4 describes the signals shown in Figure 5-3 and Figure 5-4.

5.2.1.2 2681 DUART Addresses -- The CPU logic accesses various 2681 DUART internal registers to program control, read status, and data transfer to and from the DUART. CPU logic does this by addressing specific devices (LDA2 H -- LDA5 H), for read (COMM RD L) or write (COMM WR L) operations, while the DUART is enabled (HOST/PRTR L).

Table 5-1 identifies the registers that can be addressed by address, read/write operation, and the involved circuit activity. (Appendix D provides a complete description of the register bit values.)

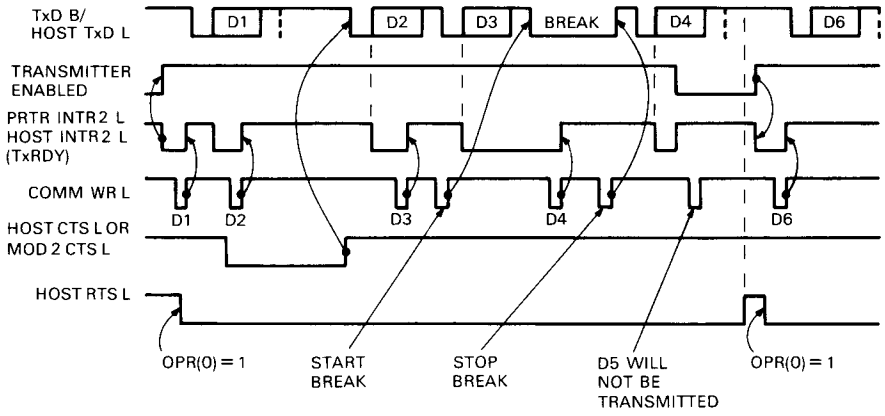
NOTE

Appendix D does not provide information for the 172070, 172072, 172074, and 172076 addresses. Two of these addresses are used simply to start (172070) or stop (172074) the counter, while the others are used to set (172072) or reset (172076) the output register bits.

5.2.1.3 2681 DUART Timing Diagrams -- Figure 5-5 is a timing diagram for DUART transmit data activity, and Figure 5-6 is a timing diagram for receive data activity.

Table 5-1 2681 DUART Addresses

Address	RD/WR	Circuit	Register
172000	RD	Host channel	Mode register 1 and 2
172002	WR	Host channel	Mode register 1 and 2
172004	RD	Host channel	Status
172006	WR	Host channel	Data clock select
172012	WR	Host channel	Command
172014	RD	Host channel	Receive data
172016	WR	Host channel	Transmit data
172020	RD	Input port	Input change
172022	WR	Timing	Auxiliary control
172024	RD	Interrupt	Interrupt status
172026	WR	Interrupt	Interrupt mask
172030	RD	Timing	Counter timer/upper
172032	WR	Timing	Counter timer/upper
172034	RD	Timing	Counter timer/lower
172036	WR	Timing	Counter timer/lower
172040	RD	Printer channel	Mode register 1 and 2
172042	WR	Printer channel	Mode register 1 and 2
172044	RD	Printer channel	Status
172046	WR	Printer channel	Data clock select
172052	WR	Printer channel	Command
172056	RD	Printer channel	Receive data
172060	WR	Printer channel	Transmit data
172064	RD	Input port	Input port
172066	WR	Output port	Output port configuration
172070	RD	Timing	Start counter command
172072	WR	Output port	Output bits command (set bits)
172074	RD	Timing	Stop counter command
172076	WR	Output port	Output bits command (reset bits)



NOTES
1. HOST RTS L IS USED ONLY BY AN EXTERNAL MODEM;
2. ALL MODEM HANDSHAKING SIGNALS ARE CONSIDERED TRUE FOR EXTERNAL OR INTEGRAL MODEM COMMUNICATION (MOD SPD SEL L OUTPUT AND MOD SI INPUTS WOULD AFFECT BAUD RATE OF TIMING FOR MODEM OPERATIONS, BUT NOT RELATIONSHIP OF TIMING SHOWN);
3. ALL DTR OR DSR SIGNALS ARE CONSIDERED TRUE;
4. CTS INPUTS ARE ACTIVE ONLY FOR EXTERNAL OR INTEGRAL MODEM COMMUNICATION;
5. HOST DTR L IS NOT USED BY THE 20mA I/F;
6. PRTR DSR L WILL BE SAMPLED BEFORE TxD B OUTPUT IF PRTR DSR L WAS NOT TRUE AT 2681 DUART POWER-UP.

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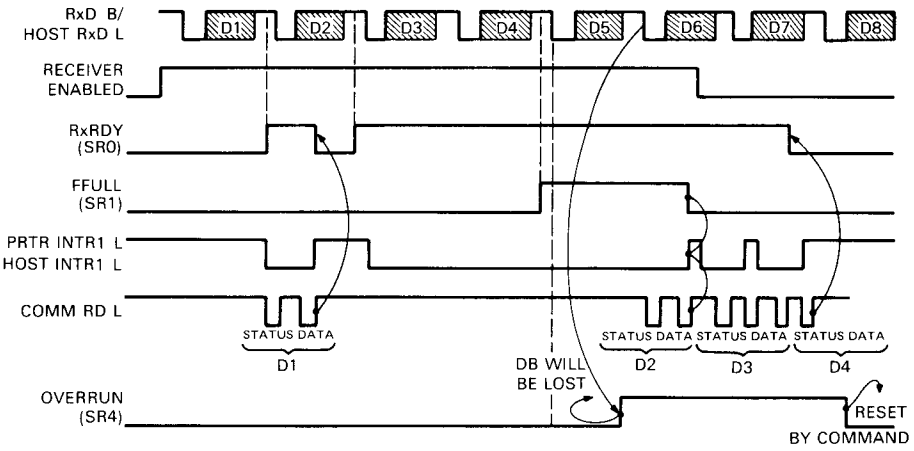
Figure 5-5 2681 DUART: Transmit Data Timing Diagram

5.2.2 Communication/Modem (Comm/Modem) Control

The comm/modem control circuitry provides:

- Storage for communication and modem control data received from the CPU logic.
- Information to the CPU logic about comm/modem controls and status.

Except chip select line outputs to the communication mux (CSLØ H -- CSL1H, used to define the interface to be enabled for host communication) all comm/modem control circuitry is dedicated to controlling the integral modem option.



NOTES

1. INTR1 SIGNALS ARE SHOWN ENABLED FOR RxRDY;
2. DTR AND DSR ARE CONSIDERED TRUE;
3. MODEM HANDSHAKING SIGNALS ARE CONSIDERED TRUE FOR EXTERNAL OR INTEGRAL MODEM COMMUNICATION, AND DISABLED FOR 20mA PORT, PRINTER PORT, AND EIA HOST PORT NULL-MODEM COMMUNICATION.

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Figure 5-6 2681 DUART: Receive Data Timing Diagram

5.2.2.1 Comm/Modem Control Circuits -- Figure 5-7 shows the following breakdown of comm/modem control.

- Communication Control Register (COMM CTRL REG) -- contains a write register for storing control data written by the CPU logic. The stored control data define the enabled interface (CSLØ H -- CSL1 H output to the communication mux). This register also contains controls for the integral modem, if installed, and a read register to enable CPU logic to verify the condition of write register bits.

- Modem Control Write Register (MOD CTRL WR REG) -- consists of three flip-flops (MOD A/B F/F, MOD SEL F/F, and OH D F/F) that are set and reset by CPU logic to provide controls for integral modem operation.

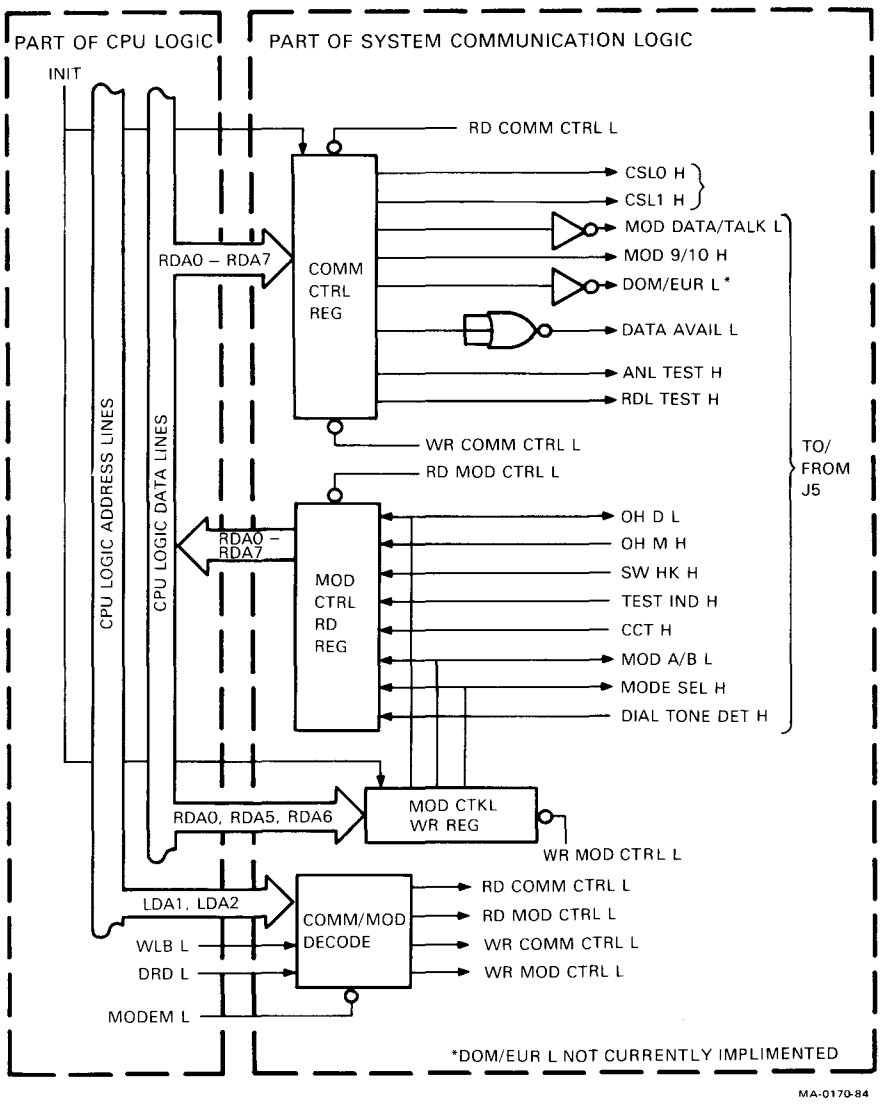


Figure 5-7 Communication/Modem (Comm/Modem) Control Block Diagram

- Modem Control Read Register (MOD CTRL RD REG) -- enables CPU logic to verify controls written to MOD CTRL WR REG, and provides integral modem status information.

- Communication/Modem Decode (COMM/MOD DECODE) -- enables CPU logic to access comm/modem control components by decoding read and write controls.

Figure 5-7 also shows three inverter devices (MOD DATA/TALK INVERTER, MOD DOM/EUR INVERTER, and DATA AVAILABLE GATE) used to invert control outputs from the COMM CTRL REG before sending those controls to the integral modem (via J5).

NOTE
The DOM/EUR L signal is not currently implemented at the integral modem option.

Later in this chapter, Table 5-4 describes the signals shown in Figure 5-7.

5.2.2.2 Comm/Modem Control Addresses -- The CPU logic accesses various comm/modem control registers to program control, or read status. The CPU logic does this by addressing a specific register (LDA1 H -- LDA2 H), for read (DRD L) or write (WLB L) operations, while the COMM/MOD DECODE is enabled (MODEM L).

Table 5-2 identifies the registers that can be addressed by address and read/write operation. (Appendix D provides complete descriptions of the register bit values.)

Table 5-3 shows how MOD SEL L and MOD A/B H signals combine with a speed select signal from the DUART (MOD SPD SEL L) to define the protocol emulated by the integral modem, while in full-duplex, asynchronous mode.

Table 5-2 Comm/Modem Control Addresses

Address	RD/WE	Register
177Ø04	RD	Comm control
177Ø04	WR	Comm control
177Ø06	RD	Modem control read
177Ø06	WR	Modem control write (MOD SEL F/F, MOD A/B F/F, OH-D F/F)

Table 5-3 Comm/Modem Control Definition of Integral Modem Option Protocol

Protocol	MOD SEL L	MOD SPD SEL L	MOD A/B H
Bell 212A, 300 BPS	Don't care	Low	High
Bell 212A, 1200 BPS	Don't care	High	High
Bell 103, Originate, 300 BPS	Low	Low	Low
Bell 103, Answer, 300 BPS	High	Low	Low

5.2.3 Communication Multiplexer (Comm Mux)

The comm mux directs the information flow between the 2681 DUART and one of the host interfaces: integral modem (via J5), EIA host interface, or 20 mA interface. CSL0 H -- CSL1 H inputs define which interface is enabled, with the value of CSL0 H -- CSL1 H determined by CPU logic programming the comm/modem control COMM CTRL REG.

Figure 5-8 shows the following breakdown of the comm mux.

- Comm Output Mux -- converts DUART data and ready signals to data and ready signals to the selected interface (only the data signal is passed on to the 20 mA interface).
- Comm Input Mux -- converts data and ready signals from the selected interface into data and ready outputs to the DUART (only a data signal is input from the 20 mA interface, with HOST DSR L developed from PULL UP).

Later in this chapter, Table 5-4 describes the signals shown in Figure 5-8.

5.2.4 Printer Interface (I/F)

The printer interface buffers communication between the terminal and any auxiliary device connected to the printer port.

Figure 5-9 shows the following breakdown of the printer interface.

- Line Buffers -- provide isolation between terminal and printer port communication lines.

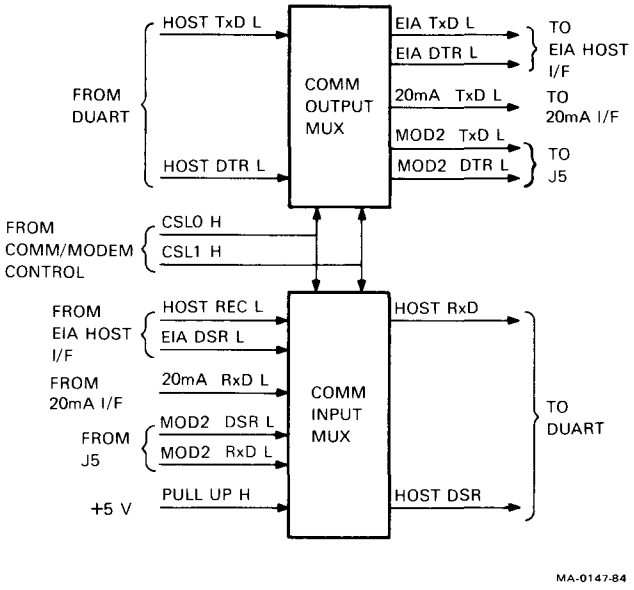


Figure 5-8 Comm Mux Block Diagram

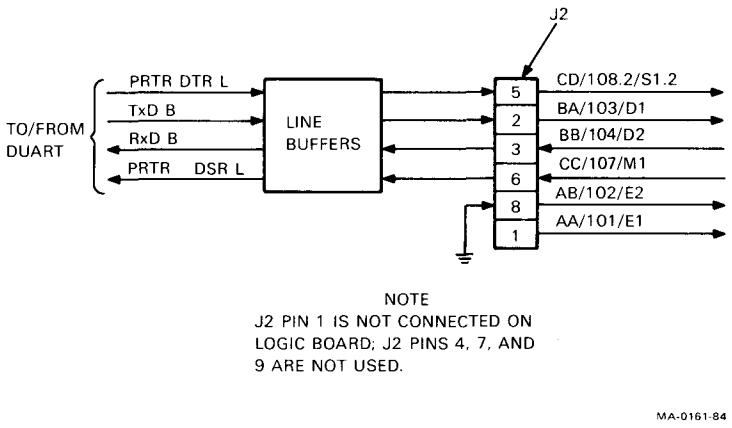


Figure 5-9 Printer Interface (I/F) Block Diagram

- J2 -- is a nine-pin EIA RS232C/RS423 connector used to connect the terminal to a local auxiliary device.

Later in this chapter, Table 5-4 describes the signals shown in Figure 5-9.

5.2.5 EIA Host Interface (I/F)

The EIA host interface buffers communication between the terminal and a host (or modem) connected to the EIA host port.

Figure 5-10 shows the following breakdown of the EIA host interface.

- Line Buffers -- provide isolation between terminal and EIA host port port communication lines.
- J3 -- is a 25-pin EIA RS232C/RS423 connector used to connect the terminal to a local or remote host (via modem).

Later in this chapter, Table 5-4 describes the signals shown in Figure 5-10.

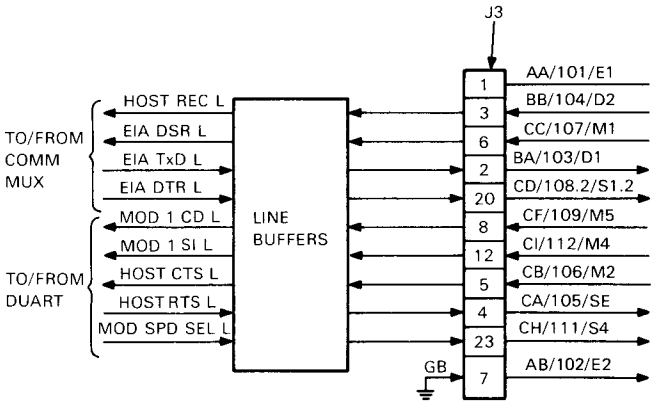
5.2.6 20 mA Interface (I/F)

The 20 mA interface buffers communication between the terminal and a local host connected to the 20 mA port.

Figure 5-11 shows the following breakdown of the 20 mA interface.

- Transmit Optoisolator -- provides isolation between the TTL level transmit data signal (20 mA TxD L) at the terminal, and 20mA level signals (T+/T-) on the 20 mA port communication lines.
- Receive Optoisolator -- provides isolation between the TTL level receive data signal (20 mA RxD L) at the terminal, and 20 mA level signals (R+/R-) on the 20 mA port communication lines.
- J4 -- is an eight-pin 20 mA connector used to connect the terminal to a local host.
- Loopback Connector -- is a troubleshooting aid that enables looping J4 signals for testing.

Later in this chapter, Table 5-4 describes the signals shown in Figure 5-11.



NOTE
J3 PIN 1 IS NOT CONNECTED ON LOGIC BOARD; J3 PINS 9–11, 13–19, 21–22, AND 24–25 ARE NOT USED.

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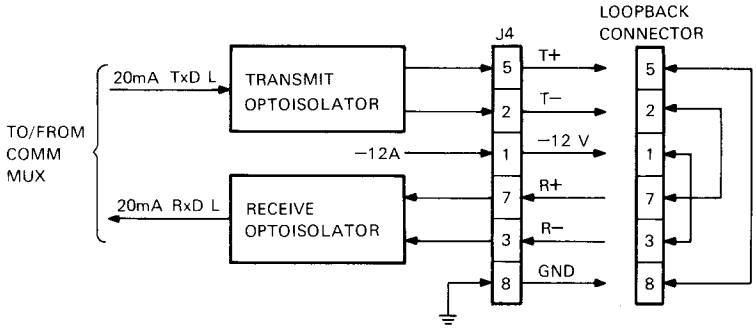
Figure 5-10 EIA Host Interface (I/F) Block Diagram



NOTE
J4 PINS 1 AND 8 PROVIDE OPERATIONAL VOLTAGE POTENTIALS FOR LOOPBACK TEST; PINS 4 AND 6 ARE NOT USED AT J4 OR AT LOOPBACK CONNECTOR.

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Figure 5-11 20mA Interface (I/F) Block Diagram

5.2.7 Integral Modem Option Connector (J5)

The integral modem option connector, J5, is a 30-pin device that provides connection between the logic board and an installed integral modem. Figure 5-12 is a pinout for J5.

Later in this chapter, Table 5-4 describes the signals shown in Figure 5-12.

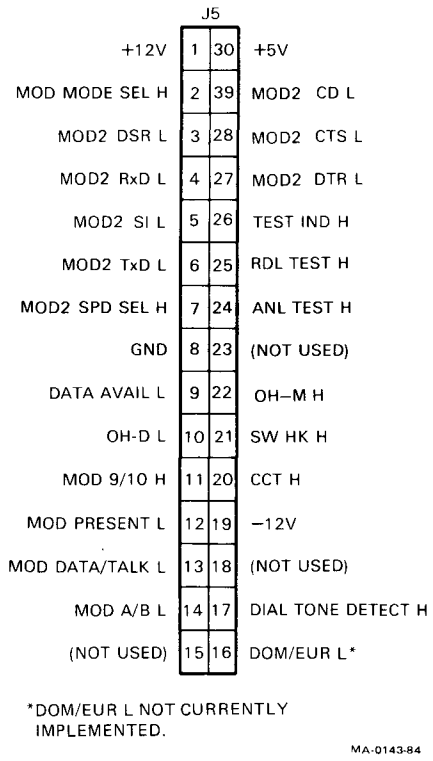


Figure 5-12 Integral Modem Option Connector (J5) Pinout

5.3 SIGNAL DESCRIPTIONS

Table 5-4 describes all the signals shown in this chapter. These descriptions are provided for reference, and are listed alphabetically by mnemonic. Numeric mnemonics are listed last.

5.4 SCHEMATIC REFERENCE INFORMATION

Table 5-5 identifies the logic board component coordinate, and schematic page and coordinate for each system communication logic component and circuit identifed in this chapter.

NOTE
The reference listing is based on Rev. C of the schematics (CS5415495-Ø-1).

Table 5-4 System Communication Logic Signal Descriptions

Signal Mnemonic	Signal Name	Description
AA/1Ø1/E1	Protective Ground	Not connected at terminal.
AB/1Ø2/E2	Signal Ground	Provides common ground.
ANL TEST H	Analog Loop Test High	Places integral modem in data loop test.
BA/1Ø3/D1	Data Output	Serial transmit data to port device.
BB/1Ø4/D2	Data Input	Serial data input from port device.
CA/1Ø5/SE	Request To Send	Request a path through external modem for transfer of data to remote host.

Table 5-4 System Communication Logic Signal Descriptions (Cont)

Signal Mnemonic	Signal Name	Description
CB/106/M2	Clear To Send	Indicates external modem is ready to transmit to remote host.
CC/107/M1	Data Set Ready	Indicates port device is ready for communication activity.
CCT H	Coupler Cut Through High	Indicates integral modem senses audio path to telephone line is ready.
CD/108.2/S1.2	Data Terminal Ready	Indicates terminal is ready for communication activity.
CF/109/M5	Carrier Detect	Indicates external modem senses good comm line.
CH/111/S4	Speed Select	Indicates receive speed greater than 600 bps selected in set-up.
CI/112/M4	Speed Indicator	Directs terminal to use transmit and receive speeds of 1200 bps regardless of set-up speeds.
CLK2 L	Clock 2 High	3.6864 MHz clock
COMM RD L	Comm Read Low	Enables read activity when DUART is selected (HOST/PRTR L active).
COMM WR L	Comm Write Low	Enables write activity when DUART is selected (HOST/PRTR L active).
CSL1 H	Chip Select Line High	Disables MOD 1 CD L at MOD CD GATE when integral modem (or 20 mA port) is selected.

Table 5-4 System Communication Logic Signal Descriptions (Cont)

Signal Mnemonic	Signal Name	Description
CSLØ H -- CSL1 H	Chip Select Lines Ø and 1 High	Defines interface signals to be passed by comm mux: integral modem (CSLØ H -- CSL1 both high), EIA host (CSLØ H --C SL1 H both low), or 2Ø mA (CLSØ H LOW, CSLI H high).
DATA AVAIL L	Data Available Low	Requests data path through integral modem.
DIAL TONE DETECT H	Dial Tone Detect High	Indicates integral modem senses telephone line ready for dialing.
DOM/EUR L	Domestic/European Low	Not currently used.
DRD L	Data Read Low	Enables read outputs (RD COMM CTRL L or RD MOD CTRL L) when COMM/MOD DECODE is selected (MODEM L active).
EIA DSR L	EIA Data Set Ready Low	Indicates external modem is ready for communication activity (buffered CC/1Ø7/M1).
EIA DTR L	EIA Data Terminal Ready Low	Indicates terminal is ready for communication activity (buffered CD/1Ø8.2/S1.2).
EIA TxD L	EIA Transmit Data Low	EIA host port serial transmit data (buffered BA/1-3/D1).
GND	Ground	Operational voltage potential outputs (also used as T+ with 2Ø mA port loopback connector.

Table 5-4 System Communication Logic Signal Descriptions (Cont)

Signal Mnemonic	Signal Name	Description
HOST CTS L	Host Clear To Send Low	Indicates host (or external modem) is ready to receive transmit data (buffered CB/106/M2).
HOST DSR L	Host Data Set Ready Low	Indicates host (or modem) is ready for communication activity.
HOST DTR L	Host Data Terminal Ready Low	Indicates terminal is is ready to transmit or receive.
HOST INTR1 L	Host Interrupt 1 Low	Indicates host receive data is present.
HOST INTR2 L	Host Interrupt 2 Low	Indicates DUART is ready for host transmit data.
HOST/PRTR L	Host/Printer Low	Enables DUART for read/write.
HOST REC L	Host Receive Low	EIA host port serial receive data (buffered BB/104/D2).
HOST RTS L	Host Request To Send Low	Requests data path through remote modem (buffered CA/105/SE).
HOST RxD	Host Receive Data	Host serial data.
HOST TxD L	Host Transmit Data Low	Host serial transmit data.
INIT H	Initialize High	System initialization signal.
LDA1 H -- LDA2 H	Latched Data Lines 1 and 2 High	Address input defining comm/modem control register to be written to (WLB L low), or read from (DRD L low), when COMM/MOD DECODE is enabled (MODEM L low).

Table 5-4 System Communication Logic Signal Descriptions (Cont)

Signal Mnemonic	Signal Name	Description
LDA2 H--LDA5 H	Latched Data Lines 2 through 5 High	Address input defining DUART internal register to be written to (COMM WR L and HOST/PRTR L both low), or read from (COMM RD L and HOST/PRTR L both low).
MOD 9/10 H	Modem 9/10 High	Defines integral modem to use 9-bit (high), or 10-bit characters (low).
MOD A/B L	Modem A/B Low	Defines integral modem emulation of BELL 212A (high), or BELL 103/V.21 (low).
MOD CD L	Modem Carrier Detect Low	Indicates good comm line has been detected by either the integral modem (MOD 2 CD L low to MOD CD GATE), or remote modem (MOD 1 CD L low to MOD CD GATE).
MOD1 CD L	Modem 1 Carrier Detect Low	Indicates external modem senses a good receive comm line (buffered CF/109/M5).
MOD2 CD L	Modem 2 Carrier Detect Low	Indicates integral modem senses a good receive comm line.
MOD2 CTS L	Modem 2 Clear To Sent Low	Indicates integral modem is ready to receive transmit data (EIA host interface uses HOST CTS L).
MOD DATA/ TALK L	Modem Data/Talk Low	Defines integral modem operation switched line communication as data (low), or talk (high).
MOD2 DSR L	Modem 2 Data Set Ready Low	Indicates integral modem is ready for communication activity.

Table 5-4 System Communication Logic Signal Descriptions (Cont)

Signal Mnemonic	Signal Name	Description
MOD2 DTR L	Modem 2 Data Terminal Ready Low	Indicates terminal is ready for communication activity.
MOD2 RxD L	Modem 2 Receive Data Low	Integral modem serial receive data.
MOD MODE SEL H	Modem Mode Select High	Selects mode for integral modem operation as either originate (low), or answer (high).
MOD PRESENT	Modem Present Low	Low whenever integral modem is installed.
MOD1 SI L	Modem 1 Speed Indicator Low	External modem signal defining receive/transmit speeds of 1200 bps regardless of set-up selection (buffered CI/112/M4).
MOD2 SI L	Modem 2 Speed Indicator Low	Integral modem signal defining receive/transmit speeds of 1200 bps regardless of set-up selection.
MOD SPD SEL L	Modem Speed Select Low	Indicates to modem (integral or external) that set-up selection for receive speed is greater than 600 bps (buffered CH/111/S4 for EIA host port).
MOD2 TxD L	Modem 2 Transmit Data Low	Integral modem serial transmit data.
MODEM L	Modem Low	Enable input to COMM/MOD DECODE.
OH D H	Off Hook Drive High	Drive signal for integral modem off hook relay.
OH M H	Off Hook Modem High	Indicates integral modem is off hook.

Table 5-4 System Communication Logic Signal Descriptions (Cont)

Signal Mnemonic	Signal Name	Description
PRTR DSR Ø L	Printer Data Set Ready Ø Low	Indicates printer port device is ready for communication activity. If inactive at power-on, DUART tests for active input before transmitting each character (buffered CC/107/M1).
PRTR DTR L	Printer Data Terminal Ready Low	Active ready output to printer port device from power on (buffered CD/108.2/S1.2).
PRTR INTR1 L	Printer Interrupt 1 Low	Indicates printer receive data is present.
PRTR INTR2 L	Printer Interrupt 2 Low	Indicates DUART is ready for printer transmit data.
PULL UP H	+5 V Pull Up High	Used by comm mux to develop HOST DST L during 20 mA port activity.
R+/R--	Receive +/Receive--	20 mA port serial receive data.
RD COMM CTRL L	Read Comm Control Low	Enables COMM CTRL REG to output control values.
RD MOD CTRL L	Read Modem Control Low	Enables MOD CTRL RD REG to output status.
RDAØ H -- RDA7 H	Data Bus Lines Ø through 7 high	Data transfer lines.
RDL TEST H Test High	Remote Data Loop Test	Places integral modem in data loop test of remote modem.
RxD B	Receive Data B	Printer port serial receive data (buffered BB/104/D2).
SW HK H	Switch Hook High	Indicates integral modem status of telephone switch hook.

Table 5-4 System Communication Logic Signal Descriptions (Cont)

Signal Mnemonic	Signal Name	Description
T+/T-	Transmit +/Transmit-	20 mA port serial transmit data.
TEST IND H	Test Indicator High	Indicates integral modem is in test mode.
TIMER INTR L	Timer Interrupt Low	Programmable interrupt.
TxD B	Transmit Data B	Printer serial data (buffered BA/103/D1).
Vcc	Voltage	+5 V operating voltage.
WLB L	Write Low Byte Low	Enables write outputs (WR COMM CTRL L or WR MOD CTRL L) when COMM/MOD DECODE is selected (MODEM L active).
WR COMM CTRL L	Write Comm Control Low	Enables COMM CTRL REG to input controls.
WR MOD CTRL L	Write Modem Control Low	Enables MOD CTRL WR REG to input controls.
+5 V	+5 V dc	Operating voltage output.
+12 V	+12 V dc	Operating voltage output.
-12 V	-12 V dc	Operating voltage output used at integral modem and 20 mA port loopback connector to provide R-.
20 mA RxD L	20 mA Receive Data Low	20 mA port serial receive data (isolated R+/R-).
20 mA TxD L	20 mA Transmit Data Low	20 mA port serial transmit data (isolated T+/T-).

Table 5-5 System Communication Logic Schematic References

Circuit/ Component	Logic Board Reference Numbers	Schematic Page	Coordinate
Comm CTRL RD REG	E60	7	C7
Comm CTRL WR REG	E59	7	D7
Comm input mux	E33	7	D5
Comm output mux	E34	7	D3
COMM/MOD decode	e57	5	b7
Data available gate	E54	17	C4
DUART	E24	8	D4
EIA host I/F buffers	E29-30,E37, E50-51,E66	8	A7-D7
J2	-	8	C2-D22
J3	-	8	A6-D6
J4	-	7	B1-C1
J5	-	17	C3-D3
MOD CD gate	E48,E66	9	B3
MOD CTRL RD REG	E58	7	B7
MOD CTRL WR REG (MOD A/B F/F)	E46	7	A5
MOD CTRL WR REG (MOD SEL F/F)	E73A	5	D2
MOD CTRL WR REG (OH D F/F)	E46	7	A6
MOD data/talk inverter	E61	17	C4
MOD DOM/EUR inverter	E47	17	D3
Printer I/F buffers	E32,E36	8	C2-D2
Receive optoisolator	E17,E52,R74-80, D6,C38,Q5-6	7	B2-B5
Transmit optoisolator	E17-18,E61, C36-37,D3-5,Q3-4	8	C2-C4

CHAPTER 6
VIDEO LOGIC

6.1 GENERAL

The video logic (shaded area in Figure 6-1) generates the outputs to drive a monochrome (VR2Ø1) or color (VR241) monitor device.

The video logic contains the circuits that store display data, process data out as video, and manipulate the stored video data as directed by the CPU logic.

The CPU logic communicates with the video logic to initialize operation, define patterns, define modes, define output color values, and identify new display data.

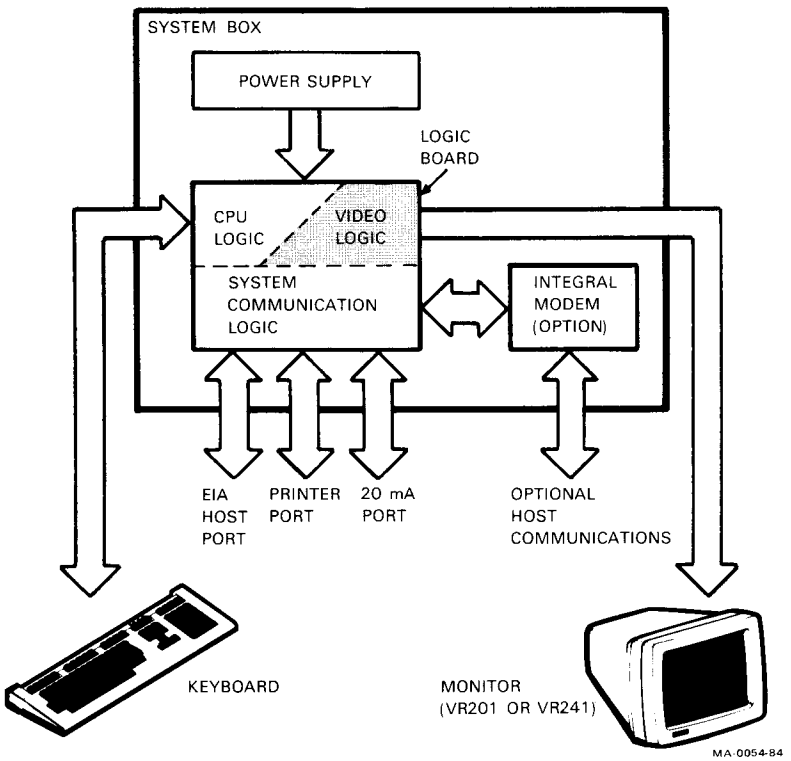


Figure 6-1 VT240-Series Terminal System Block Diagram

6.2 MAJOR CIRCUITS/COMPONENTS

Figure 6-2 is a block diagram that identifies the following major circuits/components that make up the video logic.

Character processor
Character processor memory
Video access
Graphics processor
Timing and control
Mode select
Bit map addressing
Hi/Lo byte select
Bit map write enable
Pattern select
Logic unit
Write data select
Bit map
Parallel-to-serial (P/S) converter
Output map
Digital-to-analog (D/A) converter

6.2.1 Character Processor (CP)

The T11 is the primary system CPU device. The character processor (CP) is a secondary CPU used to cut down T11 system overhead when the T11 processes data for display at the monitor.

Both the CPU and the CP can access graphics processor circuits via the video access (refer to section 6.2.3), but only one at a time. The CPU accesses the graphics processor (and related circuits) to read status, program operating parameters, or provide graphics image data for display. The CP processes text characters for display after the CPU defines which characters to be processed. This frees the CPU for other system tasks.

The CP (Figure 6-3) consists of the following circuits/components.

- 8085A-1 Microprocessor Device -- controls and performs all CP functionality.

- Handshake F/F -- coordinates CPU communication with the 8085A-2 and is set by WR BUF L going low (true) to tell the 8085A-2 (via SI and RST 6.5) that the CPU has data available. It is reset when the 8085A-2 reads the data (85RD BUF L goes low, or true), or when 8085 RESET L goes low (8085 RESET L is used to tell the 8085A-2 that the CPU wants to read data from the 8085A-2).

- 8085 Write (WR) Buffer -- passes CPU data to the 8085A-2. Data is clocked into the buffer by handshake F/F begin set, and output by 85RD BUF L going low (true).

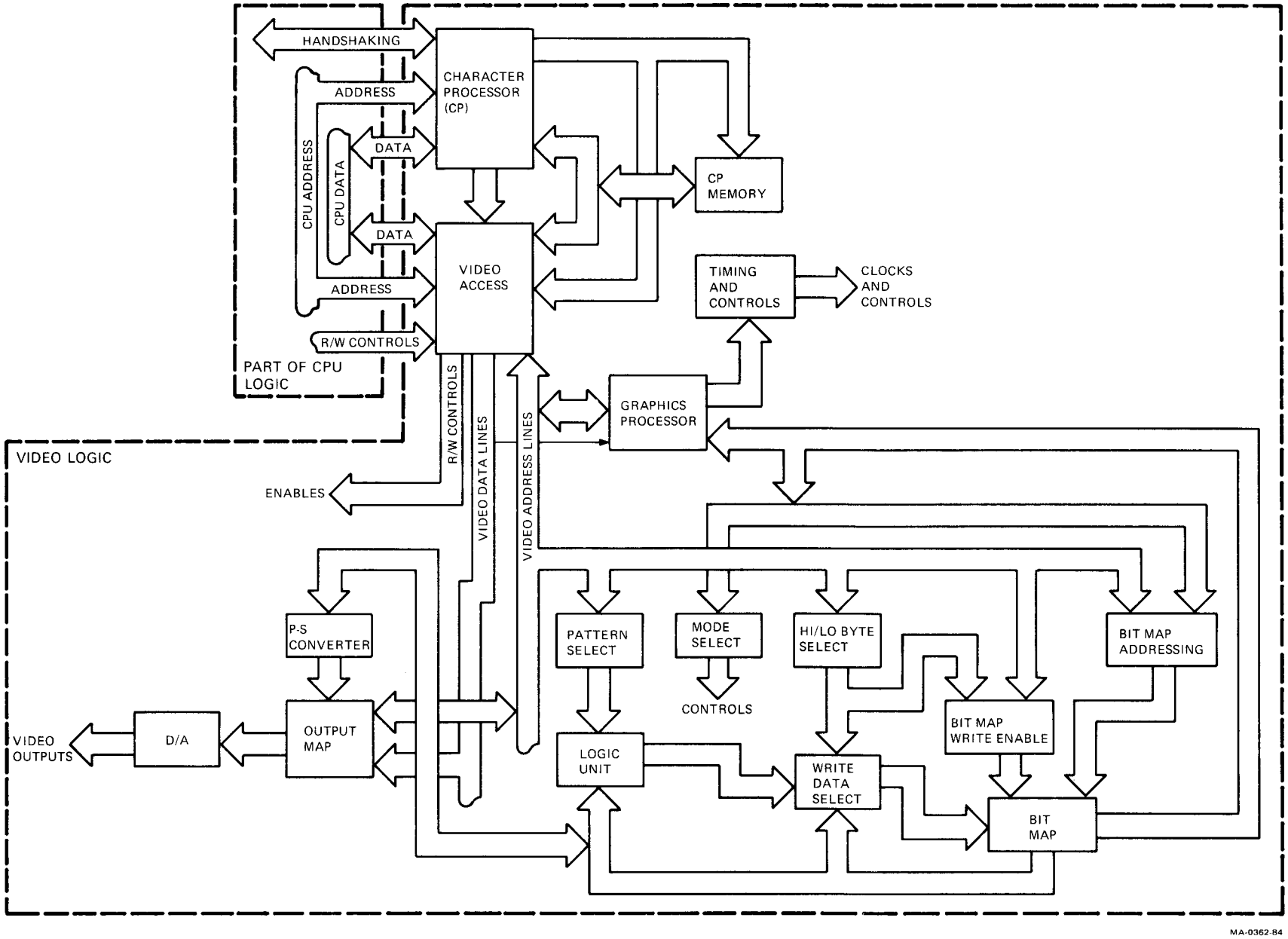


Figure 6-2 Video Logic Block Diagram

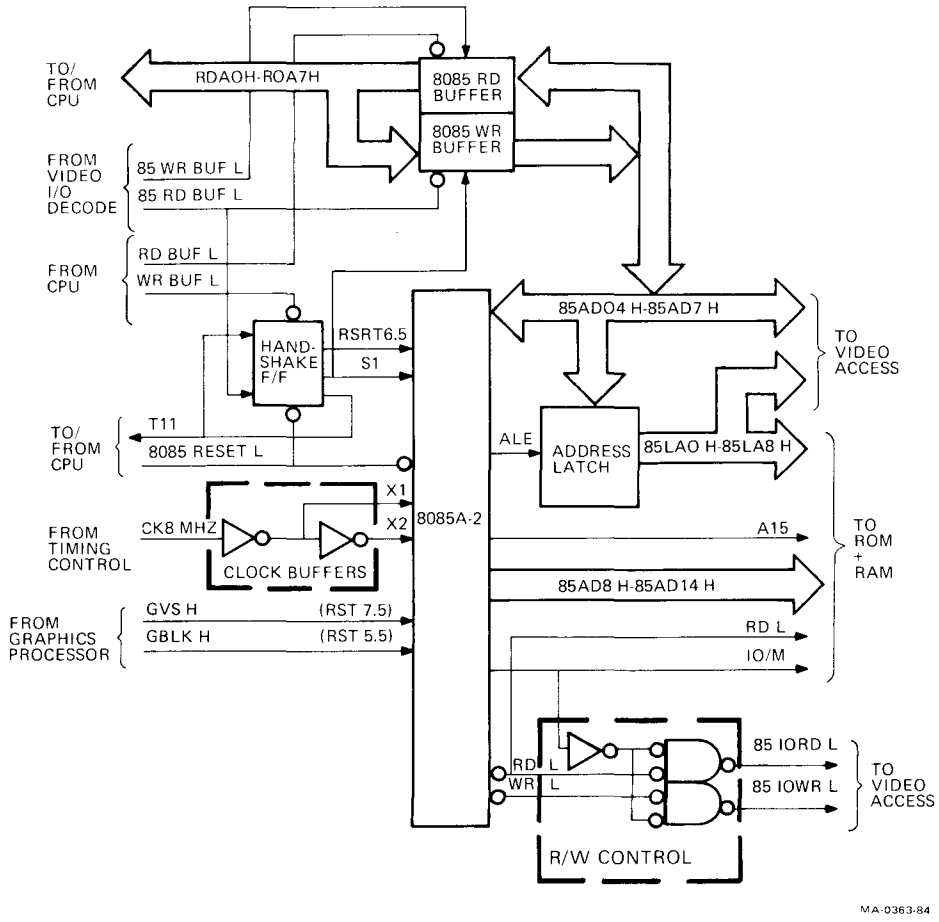


Figure 6-3 Character Processor (CP) Block Diagram

- 8085 Read (RD) Buffer -- Passes 8085A-2 to the CPU. Data is clocked into the buffer by the transition of the 85WR BUF L trail edge, and read out by RD BUF L going low (true).

- Address Latch -- Generates the address used by 8085A-2 (85LA0 H through 85LA7 H) to access either graphics processor I/O devices, or CP memory, with the address value clocked into latch by ALE.

- Read/Write (R/W) Control -- generates the read/write controls used by 8085A-2 to access I/O devices.

- Clock Buffers -- buffer and convert single CK 8 MHz input into two opposingly phased clocks (X1 and X2) to the 8085A-2.

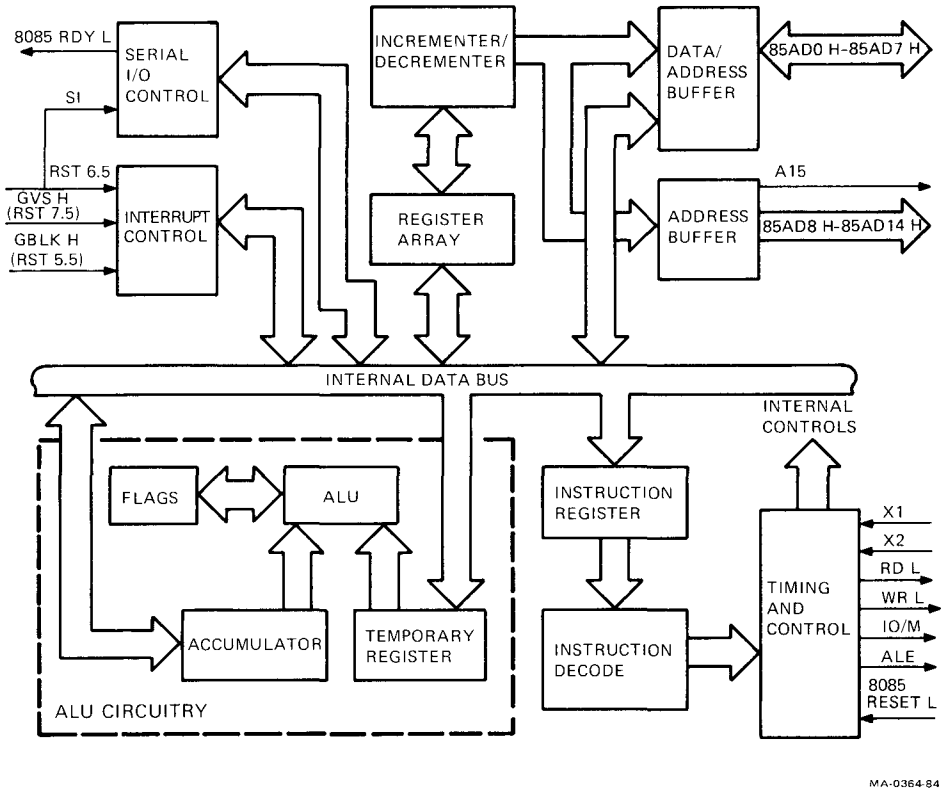


Figure 6-4 8085A-2 Microprocessor Device Internal Block Diagram

6.2.1.1 8085A-2 Microprocessor Device Internal Circuits -- Figure 6-4 is a block diagram that identifies the following major 8085A-2 internal circuits.

- Serial I/O Control -- is used for handshaking between the 8085A-2 and the T11.
- Interrupt Control -- monitors interrupt signal inputs (RST 5.5, RST 6.5 and RST 7.5) determine when an interrupt condition exists, and to force 8085A-2 to access the relevant interrupt handling instruction code in CP memory.
- Register Array -- includes six general purpose register devices for 8085A-2 functions, as well as a stack pointer and program counter.
- Incrementer/Decrementer -- generates the value to be used for addressing external memory and I/O devices.

- ALU Circuitry -- is responsible for all 8085A-2 arithmetic functions.

- Instruction Register -- stores the instructions to be processed.

- Instruction Decode -- decodes instruction information contained in the instruction register, and encodes the instruction requirements in terms of 8085A-2 machine cycles.

- Timing and Control -- generates all internal and external controls and timing signals.

- Data/Address Buffer -- is bidirectional buffer device used to input or output data, or to output the least significant eight bits of a memory or I/O device address.

- Address Buffer -- outputs the most significant eight bits of a memory or I/O device address.

Later in this chapter, Table 6-6 describes the signals shown in Figures 6-3 and 6-4.

6.2.1.2 8085A-2 Microprocessor Device Transactions -- The 8085A-2 is involved with the following three types of transactions.

Read/write by CPU logic
Read/write of CP memory
Read/write of graphics processor I/O device circuits

The CPU reads data from the 8085A-2 to determine operating conditions. The CPU writes data to the 8085A-2 to define the specific CP memory address of a character to be processed over to the graphics processor circuits.

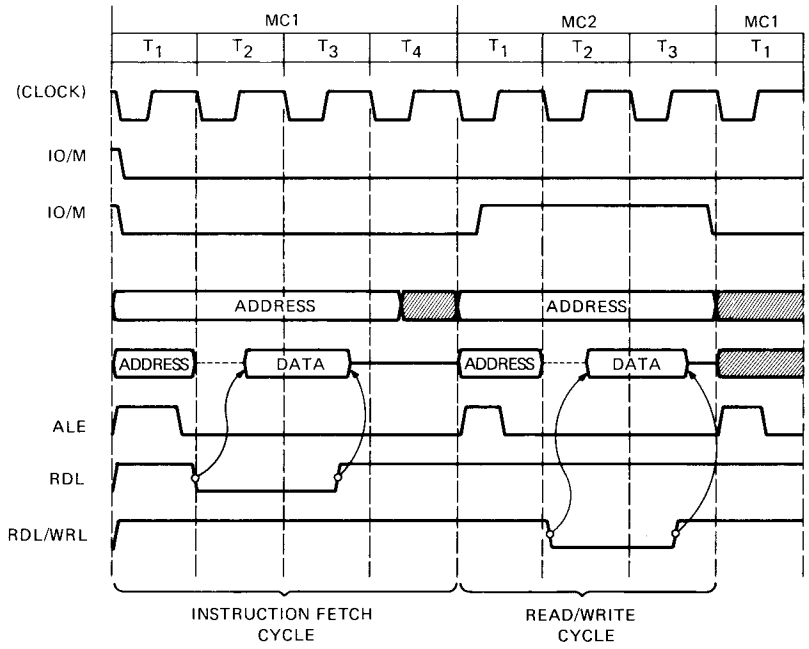
The 8085A-2 reads data from the CP memory to either access instruction codes, acquire character format data, use for scratch pad operations, or store character data for later processing.

The 8085A-2 reads data from the graphics processor circuits to obtain status information. The 8085A-2 writes data to the graphics processor circuits to define new data for display.

8085A-2 communicates with the CPU through handshaking. The CPU sets the handshaking F/F when the CPU has data to be written to the 8085A-2. The 8085A-2 resets this F/F when the data has been accepted. The 8085A-2 generates a ready signal (8085 RDY L low) when it has data to be read by the CPU.

8085A-2 communication with the graphics processor circuits is synchronized to the vertical synchronization (sync) period. The graphics processor generates two signals (GVS H and GBLK H). These signals are used as interrupt inputs to the 8085A-2, one true at the start of the vertical sync period (GVS H high), and the other true while the screen is blanked during vertical sync (GBLK H high). During the vertical sync period the 8085A-2 can affect the information to be displayed during the next screen refresh cycle.

Figure 6-5 is a timing diagram for 8085A-2 read/write transactions that involve either the CP memory, or graphics processor I/O circuits. Note that although memory access can occur at any time, the 8085A-2 is limited to I/O access only during vertical sync time (defined by GVS H and GBLK H interrupt inputs). Later in this chapter Table 6-6 describes the signals identified in these timing diagrams.



NOTES
1. IO/M SIGNAL FOR MEMORY READ/WRITE TRANSACTIONS;
2. IO/M SIGNAL FOR I/O DEVICE READ/WRITE TRANSACTIONS;
3. ALE LATCHES THE LOW ORDER BYTE OF ADDRESS INTO THE ADDRESS LATCH ON THE TRAILING EDGE;
4. RD L GOES LOW (TRUE) FOR READ TRANSACTIONS, WHILE WR L GOES LOW (TRUE) FOR WRITE TRANSACTIONS.

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Figure 6-5 Character Processor (8085A-2 Microprocessor Device) Read/Write Transactions

6.2.2 Character Processor (CP) Memory

CP memory provides the RAM and ROM memory needed for CP (8Ø85A-2) functions. The CP memory (Figure 6-6) consists of the following components.

- Character Processor (CP) RAM -- is a 2K X 8-bit device that provides for 8Ø85A-2 scratchpad operations, and stores data to be transferred to the graphics processor circuits during vertical synchronization periods, (including data for smooth scroll operations).

- Character Processor (CP) ROM -- has up to 32K X 8 bits of ROM that contains firmware that directs 8Ø85A-2 operations as well as character pattern data.

NOTE

CP ROM can consist of a single 32K device or two ROM devices with up to 32K storage. If a 32K ROM is used, it is installed in the ROM 7 position, and ROM 8 is not used.

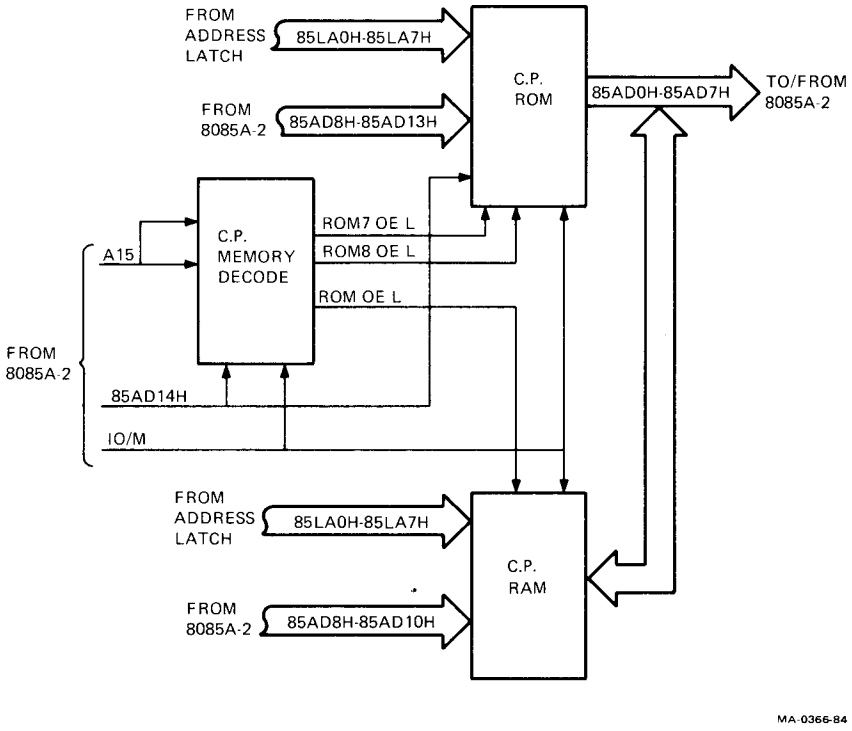


Figure 6-6 Character Processor (CP) Memory Block Diagram

- Character Processor (CP) Memory Decode -- decodes A15 and 85AD14 H inputs into either a ROM (ROM7 OE or ROM8 OE) or RAM (RAM OE) enable signal, when memory is to be accessed (IO/M low).

Table 6-1 identifies the address ranges of the CP memory components. Later in this chapter, Table 6-6 describes the signals shown in Figure 6-6.

Table 6-1 Character Processor Memory Addresses

Device		Hex Address Range	A15	85AD14 H
CP ROM 7	(16K)	0000H--3FFFH	Low	Low
CP ROM 8	(16K)	4000H--7FFFH	Low	High
CP ROM 7	(32K)	0000H--7FFFH	Low	Low
CP RAM	(2K)	8000H--87FFH	High	Low

6.2.3 Video Access

The video access circuit provides shared access of the graphics processor circuits by the CPU or character processor (CP). The CP also uses the video access circuit to generate read/write control signals used to communicate with the CPU (85 RD BUF L and 85 WR BUF L).

Only one processor can use the video access circuit at given time. Control over enabling access is the VID ACCESS L signal from the CPU logic. When VID ACCESS L is low (true), the CPU has access; when VID ACCESS L is high (false), the CP has access.

The video access circuit (Figure 6-7) consists of the following components.

- Video Address Mux -- consists of two mux devices that select CPU address values (LDA1 H -- LDA8 H, when VID ACCESS L is low), or CP address values (LDA0 H -- LDA7 H, when VID ACCESS L is high) to generate outputs that define an I/O circuit to be accessed (VA0 H -- VA7H).

- Video RD/WR Mux -- selects either CPU read/write control signals (GRD L and GWLB L, when VID ACCESS L is low), or CP control signals (85 IORD L and 85 IOWR L, when VID ACCESS L is high) to generate video read/write control signals (VIO RD L and VIO WR L).

- Video I/O Decoders -- decode address (VA4 H -- VA7 H) into specific read/write access signals for I/O circuits.

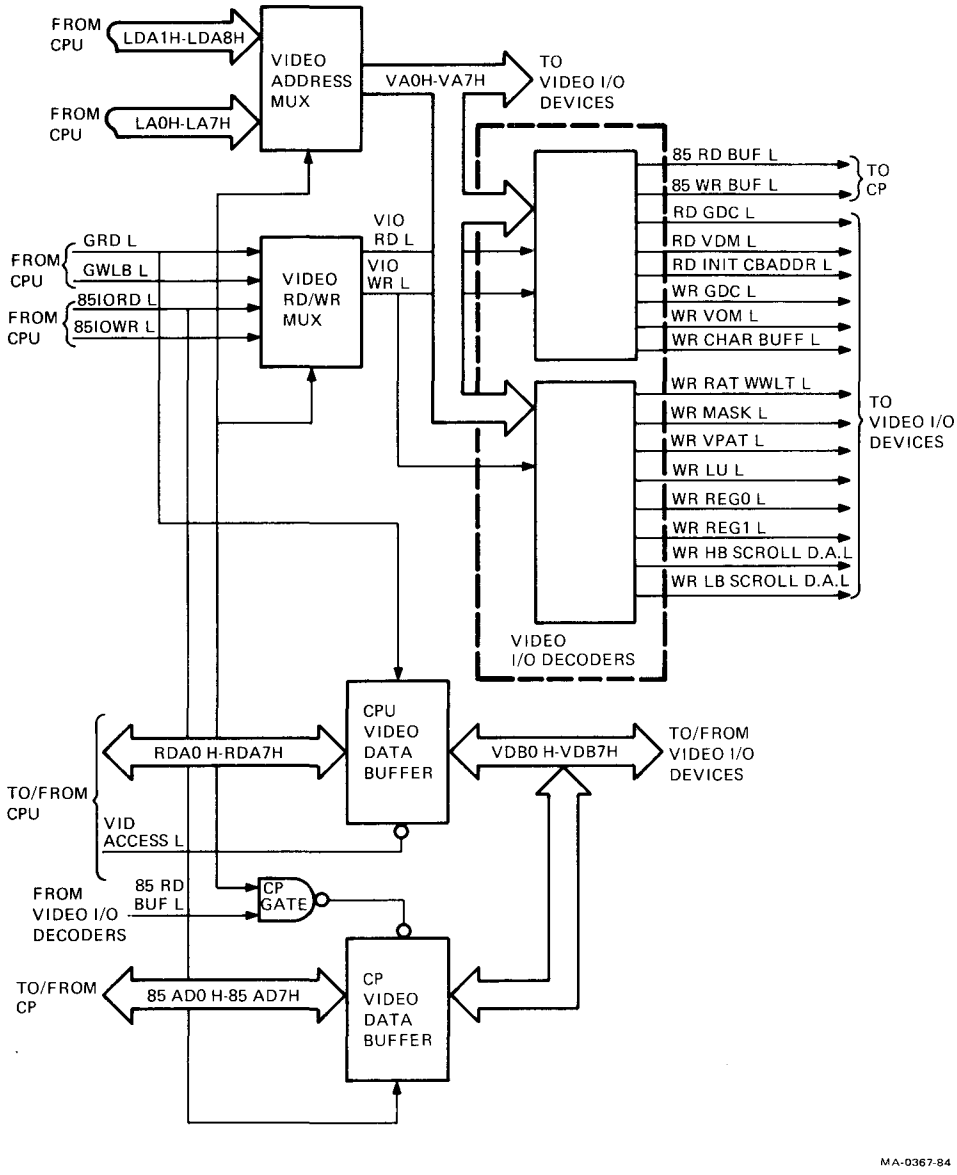


Figure 6-7 Video Access Block Diagram

- CPU Video Data Buffer -- is a bidirectional buffer device enabled by VID ACCESS L low for data transfer. The condition of GRD L defines the transfer direction (from VDB Ø H -- VDB 7 H to RDA Ø H -- RDA 7 H, when GRD L is low).

- CP Video Data Buffer -- is a bidirectional buffer device enabled by CP gate when the CPU is not accessing graphics processor circuits (VID ACCESS L is high), and the CP is not reading the 85 RD data buffer (85 RD BUF L is high). The direction of data transfer is determined by 85 IORD L (from VDB Ø H -- VDB 7 H to 85 ADØ H -- 85 AD7 H, when 85 IORD L is low, or true).

Table 6-2 identifies the CPU and CP addresses used to generate the various I/O read/write enable signals. Later in this chapter, Table 6-6 describes the signals shown in Figure 6-7.

Table 6-2 Video Access Circuit I/O Addresses

CPU Address Signal	CP Address Octal	Hex	Destination Device
RD GDC L	173ØØØ/173ØØ2	ØØ/Ø1	GDC
WR GDC L	174ØØØ/174ØØ2	ØØ/Ø1	GDC
RD VOM L	173Ø4Ø--173Ø76	1Ø-1F	Video output map
WR VOM L	174Ø4Ø--174Ø76	1Ø-1F	Video output map
85 RD BUF L	(Not accessed)	2Ø	85 RD data buffer, CP gate, handshake F/F
85 WR BUF L	(Not accessed)	2Ø	85 WR data buffer
RD INIT CB ADDR L	173140	3Ø	Character buffer
WR CHAR BUFF L	174140	3Ø	Character buffer
WR PAT MULT L	174400	8Ø	Pattern multiplier
WR MASK L	174440	9Ø	Write mask register
WR VPAT L	174500	AØ	Vector pattern register
WR LU L	174540	BØ	Logic unit register
WR REGØ L	174600	CØ	Register Ø
WR REGl L	174640	DØ	Register 1
WR HB Scroll DA L	174700	EØ	Scroll address
WR LB Scroll DA L	174740	FØ	Scroll address

6.2.4 Graphics Processor

The graphics processor is a PD7220 Graphics Display Controller (GDC). The GDC is a microprocessor device that performs the following tasks.

- Generates the basic video timing, including blanking and sync signals
- Directs modification of bit map memory values during drawing and data move activity

Figure 6-8 identifies the signals involved in GDC operation, as used in the VT240. Later in this chapter, Table 6-6 describes the signals shown in Figure 6-8.

6.2.4.1 PD7220 Graphics Display Controller (GDC) Internal Circuits -- Figure 6-9 is a block diagram that shows the following major GDC internal circuits, as used in the VT240.

- System Interface (I/F) -- communicates with either the CPU or CP via video access circuit to transfer data or status to the requesting device, or receive data or commands from the microprocessor device.
- FIFO Buffer -- is a 16-byte device that stores command information (communication between the system I/F and FIFO is on a separate bus from the PD7220 internal bus).
- Command Processor -- accesses and decodes commands stored in the fifo, distributing parameter information to the various internal circuits.
- Internal Bus Interface -- buffers communication between the system I/F and other internal circuits, and between the FIFO and the command processor.
- Parameter RAM -- is 16-byte RAM used to store parameters to be used repetitively during display and draw processes.
- Video Sync Generator -- generates raster timing signals, with timing based on clock input.
- Memory Timing Generator -- generates control signals for read-modify-write (RMW) bit map memory cycles.
- Drawing Processor -- calculates the addresses and positions of pixels for various graphic images to be drawn from a starting point and appropriate drawing parameters.

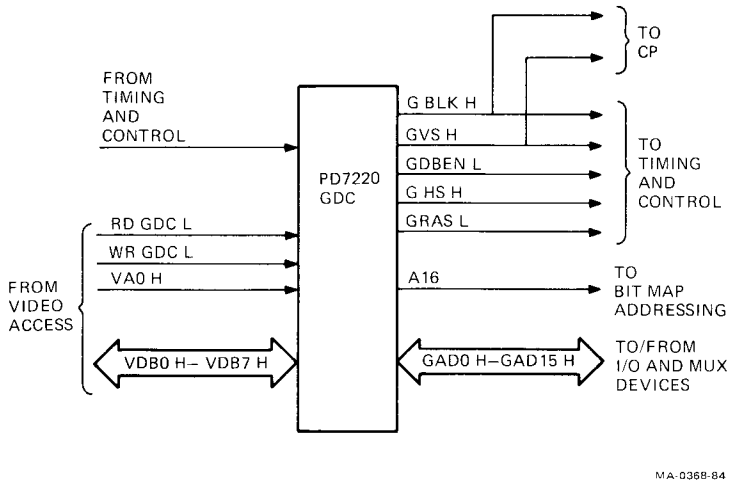


Figure 6-8 Graphics Processor Block Diagram

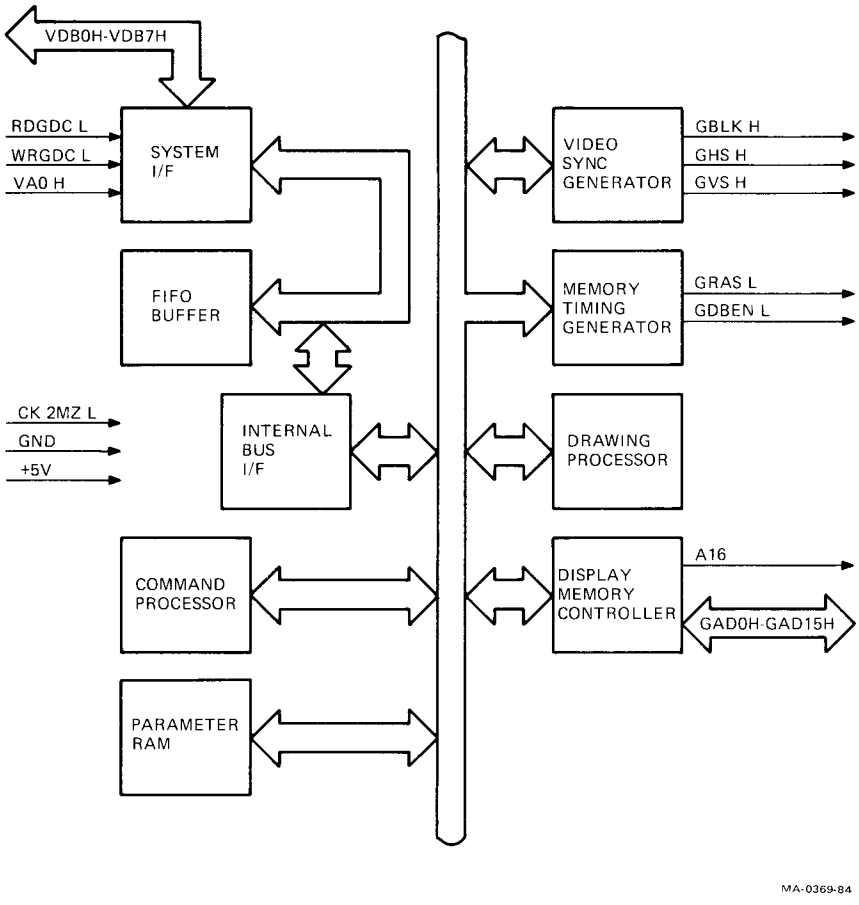


Figure 6-9 PD7220 GDC Block Diagram

- Display Memory Controller -- multiplexes the address and data information in and out of bit map memory, and modifies, as necessary, the bit map contents during the read-modify-write (RMW) cycles.

Later in this chapter, Table 6-6 describes the signals shown in Figure 6-9.

6.2.4.2 PD7220 Graphics Display Controller (GDC) Addresses -- The GDC can be accessed, through the video access circuit, by either the CPU or the CP for read and write transactions at either of the following two addresses.

- 173000 -- for a write of commands to GDC FIFO (WR GDC L and VA0 H, both low), or a read of data from FIFO (RD GDC L low and VA0 H low).

- 173002 -- for a write of parameter data to GDC FIFO (WR GDC L low and VA0 H high), or a read of status data from GDC status register (RD GDC L low and VA0 H high).

All write operations are to the GDC FIFO with the VA0 H signal defining the data as either commands (VA0 H low, for address 173000), or parameters (VA0 H high, for address 173002). Commands define a specific operation, type of parameter information to follow, or type of data to be read from the GDC by the CPU or CP.

Table 6-3 is a summary of the commands that can be written to the GDC.

NOTE

Appendix D provides a complete description of the bit values for the GDC status register. The manual does not give any further description of any other GDC register device.

Table 6-3 PD7220 GDC Commands Summary

Command	Bit Values 7 6 5 4 3 2 1 0	Description
Video Control		
RESET	Ø Ø Ø Ø Ø Ø Ø Ø	Resets GDC to idle state; Reset command can be followed by up to eight parameter bytes defining mode of operation, active display words per line, horizontal and vertical sync widths, horizontal and vertical front and back porch widths, and active display lines per video field.
VSYNC	Ø Ø Ø Ø 1 1 1 1	Generate and output vertical sync.
CCHAR	Ø 1 Ø Ø 1 Ø 1 1	Cursor and character characteristics command followed by three parameter bytes: parameter bytes define cursor on or off, lines per character row, cursor blink rate, blinking or steady cursor, cursor top and bottom line numbers in the row.
Display Control		
START	Ø Ø Ø Ø 1 Ø 1 1	Start display scanning.
STOP	Ø Ø Ø Ø 1 1 Ø Ø	Blank display.
CURS	Ø 1 Ø Ø 1 Ø Ø 1	Cursor position command followed by three parameter bytes: parameter bytes define the high and low byte of display address for both graphic and character operations, and in the case of graphic image cursor, an additional two bits of display address, and the dot address within the the defined address word.

Table 6-3 PD7220 GDC Commands Summary (Cont)

Command	Bit Values 7 6 5 4 3 2 1 0	Description
PRAM	0 1 1 1 x x x x	Defines a parameter RAM load command, with the starting address for loading into the RAM. From 1 to 16 parameter bytes can follow, each defining specific operational parameters.
PITCH	0 1 0 0 0 1 1 1	Pitch specification command followed by a single parameter byte defining the the pitch as a number of word addresses in the horizontal direction.
Drawing Control		
WDAT	0 0 1 0 0 0 1 0	Write data into display memory, with data transfer defined as a word and RMW cycle logical operation defined as reset to zero.
MASK	0 1 0 0 1 0 1 0	Mask register load command followed by two parameter bytes defining a mask to control which bits can be modified in the bit map memory during RMW cycles.
FIGS	0 1 0 0 1 1 0 0	Figure drawing parameters specify command followed by up to 11 parameter bytes: parameter bytes define type of drawing operation (such as straight line, or arc and circle), and various drawing parameters.
FIGD	0 1 1 0 1 1 0 0	Figure draw start command loading drawing parameters from the parameter RAM into the drawing processor, and starts drawing at the point defined by cursor and dot address values.

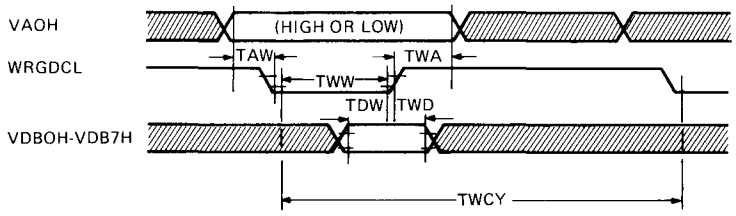
Table 6-3 PD7220 GDC Commands Summary (Cont)

Command	Bit Values 7 6 5 4 3 2 1 0	Description
GCHRD	0 1 1 0 1 0 0 0	Graphics character draw and area filling command initiates drawing or area filling based on pattern stored in parameter RAM, starting at point defined by cursor and dot address values.
Data Read		
RDAT	1 0 1 0 0 0 0 0	CPU/CP read of data from display memory command defining data read cycle to be a word, with first low then high bytes read.
CURD	1 1 1 0 0 0 0 0	CPU/CP read of cursor position, with position of word and dot addresses supplied to CPU/CP in five bytes.
DMA Control		
DMAR	1 0 1 0 0 1 0 0	CPU/CP DMA read request command defining transfer as a word, with low then high byte.
DMAW	0 0 1 0 0 1 0 0	CPU/CP DMA write request command defining transfer as a word, with low then high byte, and defining RMW cycle for defined word as replace with pattern supplied by the word.

6.2.4.3 PD7220 Graphics Display Controller (GDC) Transactions -- The GDC is involved in the following three basic transactions.

- Communication with either the CPU or CP to transfer command or display data to the GDC, or to transfer status or FIFO read back data to the CPU or CP
- Managing display data stored in bit map memory
- Providing basic control for display synchronization

Figures 6-10 through 6-15 are timing diagrams for various GDC operations. Later in this chapter, Table 6-6 describes the signals shown in these diagrams.



SYMBOL	PARAMETER	MIN.	MAX.	UNITS
TAW	ADDRESS SETUP TO WR	0		NS
TWA	ADDRESS HOLD FROM WR	0		NS
TWW	WR PULSE WIDTH	100		NS
TDW	DATA SETUP TO WR	80		NS
TWD	DATA HOLD FROM WR			NS
TWCY	WR PULSE CYCLE	4-TCLK		NS

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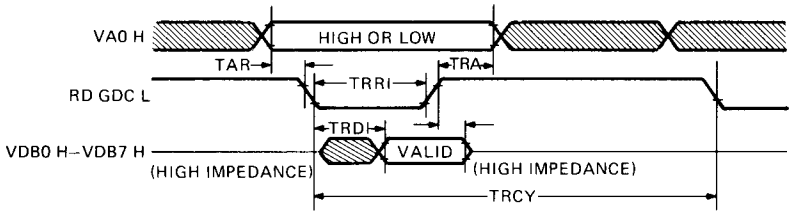
Figure 6-10 PD7220 GDC Timing Diagram: CPU/CP Write Transaction



SYMBOL	PARAMETER	MIN.	MAX.	UNITS
TAR	ADDRESS SETUP TO RD	0		NS
TRA	ADDRESS HOLD FROM RD	0		NS
TRRI	P DPULSE WIDTH	TRDI+20	140	NS
TRDI	DATA DELAY FROM RD		120	NS
TDG	DATA FLOATING FROM RD	0	100	NS
TRCY	RD PULSE CYCLE	4.TCLK		TCLK

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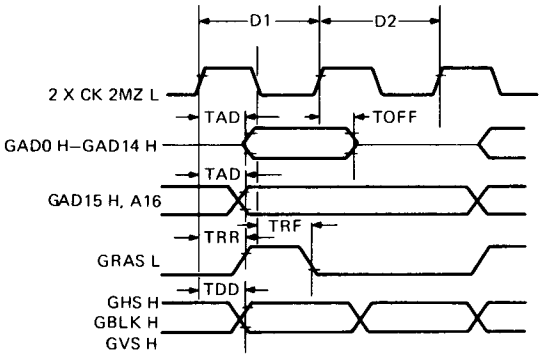
Figure 6-11 PD7220 GDC Timing Diagram: CPU/CP Read Transaction



SYMBOL	PARAMETER	MIN.	MAX.	UNITS
TAD	ADDRESS/DATA DELAY FROM: 2 X CCLK ↑		130	NS
TOFF	ADDRESS/DATA FLOATING FROM: 2 X CCLK ↑	10	130	NS
TRR	RAS↑DELAY FROM 2 X CCLK ↑	30	110	NS
TRF	RAS↓ DELAY FROM 2 X CCLK ↓		90	NS
TDD	VIDEO SIGNAL DELAY FROM 2 X CCLK		120	NS

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Figure 6-12 PD7220 GDC Timing Diagram: Display Timing

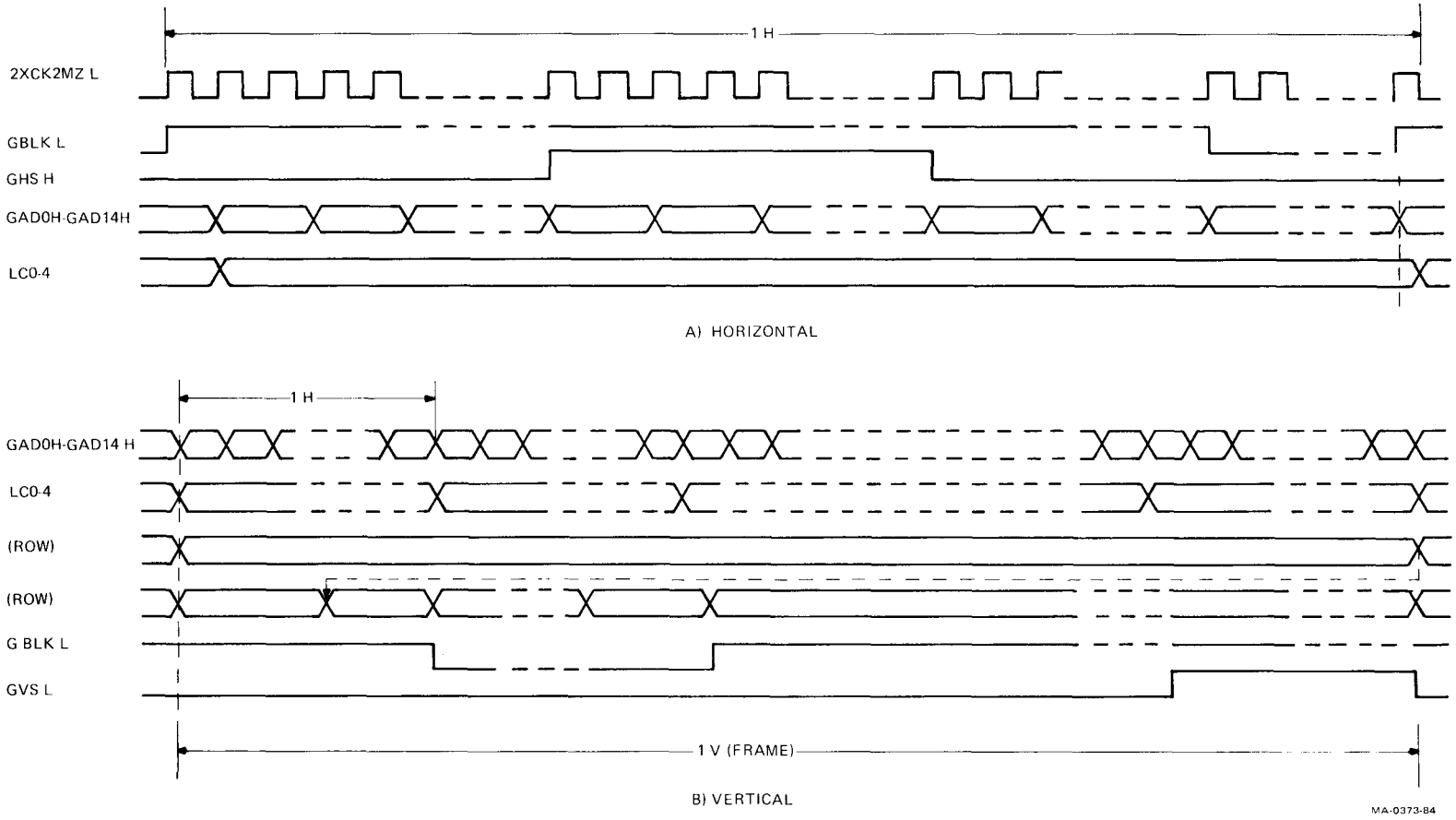


Figure 6-13 PD7220 GDC Timing Diagram: Video Sync Signals

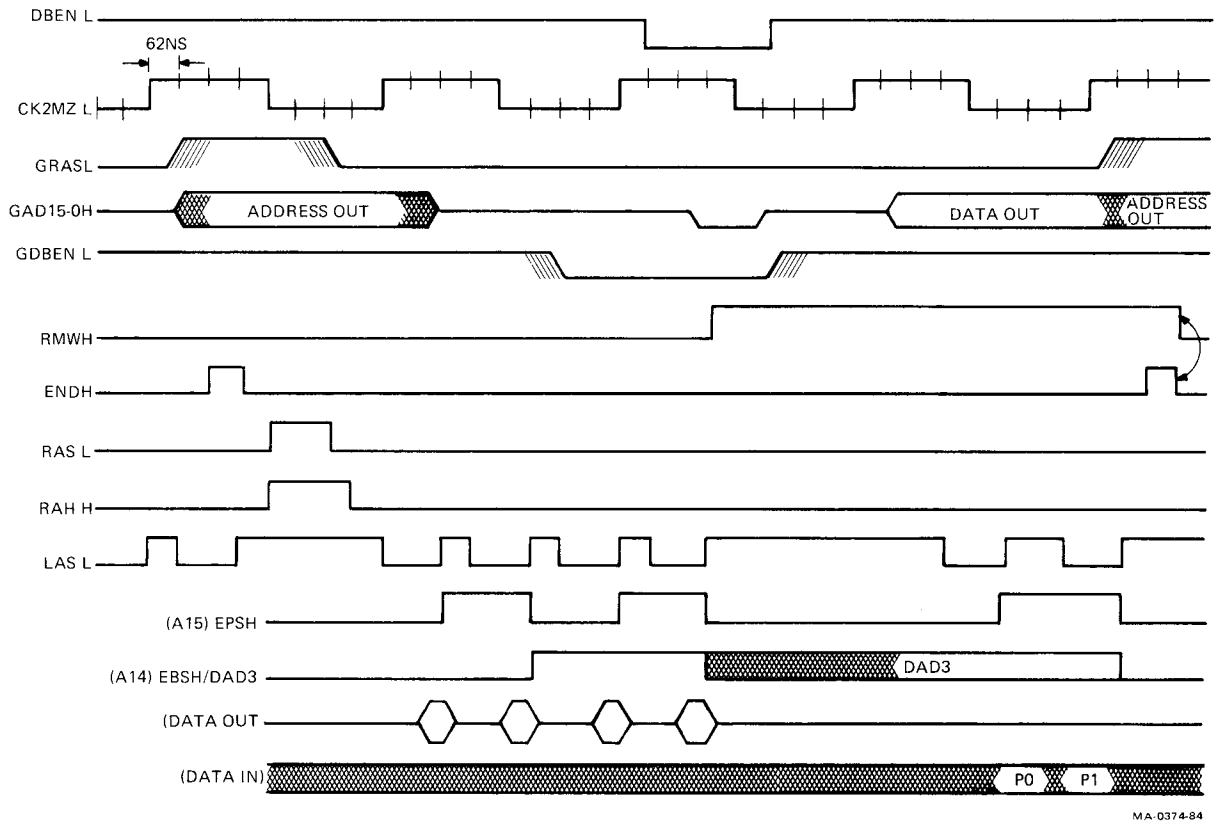


Figure 6-14 PD7220 GDC Timing Diagram: 2-Plane Write Transaction

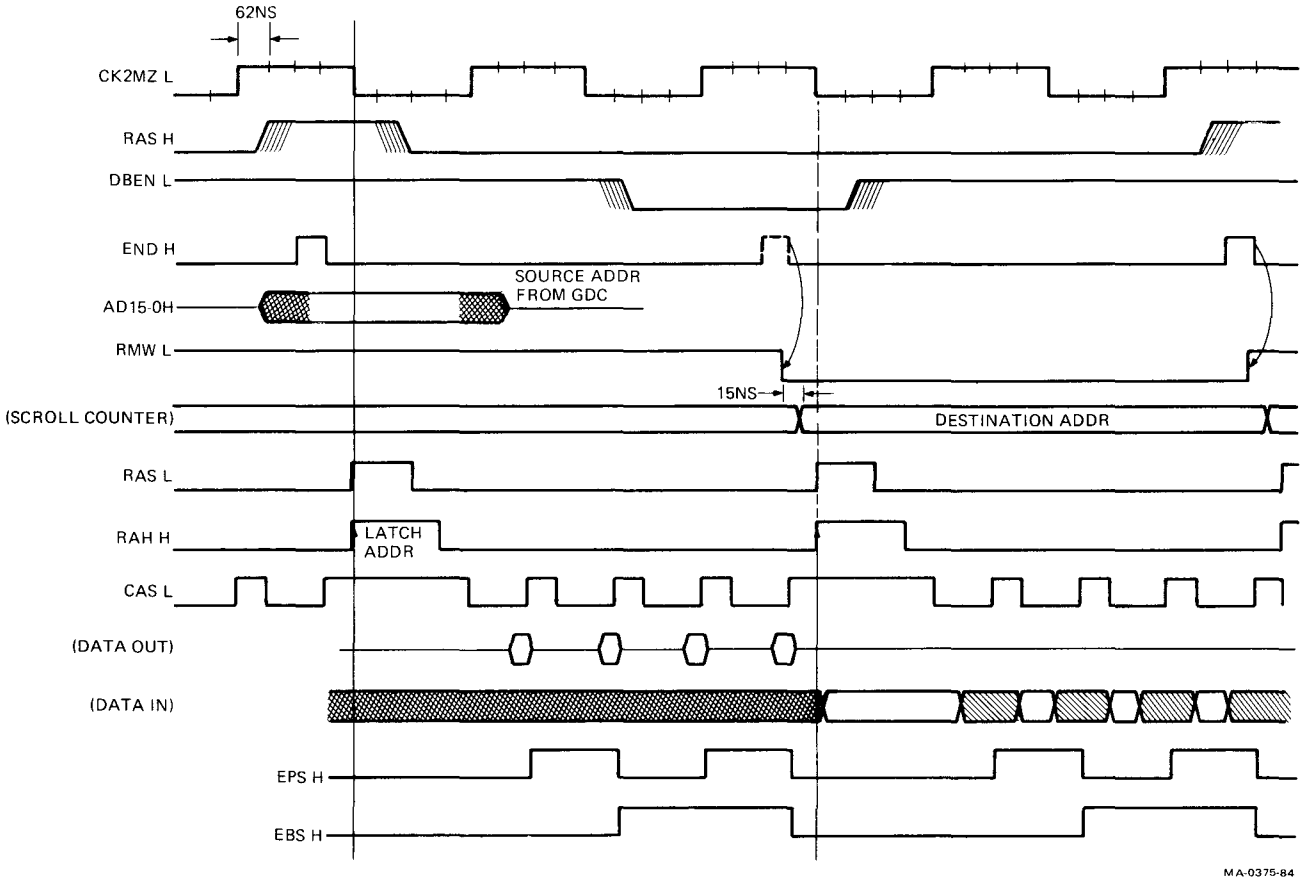


Figure 6-15 PD7220 GDC Timing Diagram: Video DMA Write Transaction

6.2.5 Timing and Control Circuits

The timing and control circuits (Figure 6-16) consist of the following circuits.

- Clock generator
- ROM address counter
- Timing signal generator
- BLANK generator
- BEN and STOP gates
- Read-modify-write (RMW) generator

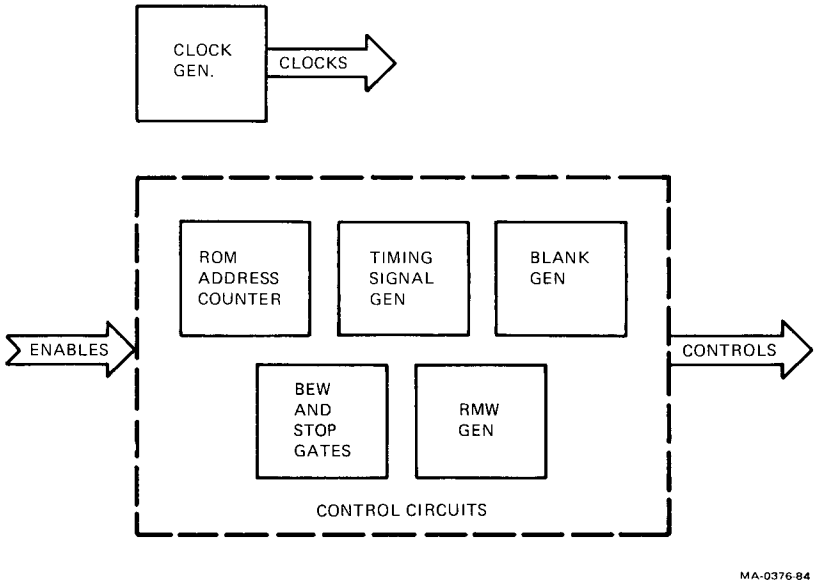


Figure 6-16 Timing and Control Block Diagram Circuits

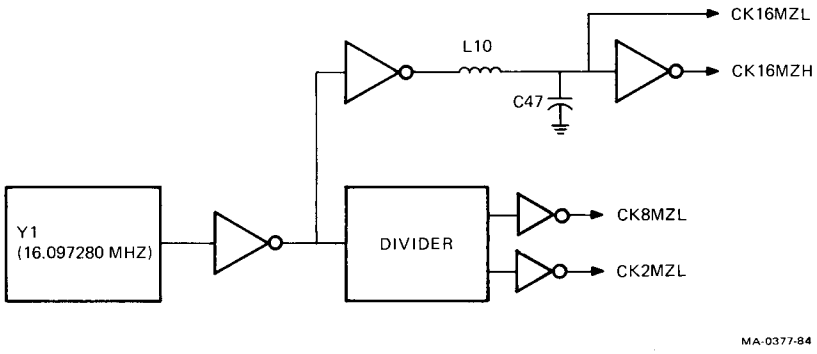


Figure 6-17 Clock Generator Block Diagram

6.2.5.1 Clock Generator -- The clock generator provides the basic timing signals used by various video logic components. The clock generator (Figure 6-17) consists of the following components.

- Y1 -- is an oscillator that provides basic clock (16.097280 MHz).
- L10, C47 -- is a filter for 16 MHz clock outputs.
- Divider -- generates 8 MHz (CK 8 MZ L) and 2 MHz (CK 2 MZ L) clocks from buffered input from Y1.

6.2.5.2 BEN and STOP Gates -- The bus enable (BEN) and stop (STOP) signal gates (Figure 6-18) consist of two inverters and two gates.

- The inverters buffer a bus enable input from the GDC (GD BEN L) into bus enable outputs to the RMW generator.
- The gates generate STOP L and DBEN L control outputs based on timing signal generator inputs and buffered GD BEN L signal.

Later in this chapter, Table 6-6 describes the signals shown in Figure 6-18.

6.2.5.3 ROM Address Counter -- The ROM address counter circuit provides a cyclical address output used by ROM devices in the timing signal generator and parallel-to-serial converter circuits. The ROM address counter (Figure 6-19) consists of the following circuits/components.

- Clear F/F -- clears the count of the ROM address clock whenever STOP L input from STOP gate is true (low).
- ROM Address Clock Counter -- generates address value output (AØ H -- A3 H) from CK 16MZ H input.

Later in this chapter, Table 6-6 describes the signals shown in Figure 6-19.

6.2.5.4 Timing Signal Generator -- The timing signal generator provides control for video logic activity by generating control outputs based on cyclically addressed ROM based firmware. The timing signal generator (Figure 6-2Ø) consists of the following components.

- SCROLL/STOP F/F -- determines high order bit of address to the timing signal ROM (TMØ) with a low address bit during scroll (SCROLL EN L low) or stop (STOP L low) conditions.
- TMØ -- is a 32 X 8-bit ROM device that contains firmware cyclically addressed by inputs from ROM address counter (AØ H -- A3 H);
- Timing Signal Buffer -- buffers TMØ outputs based on CK 16MZ H input.

Later in this chapter, Table 6-6 describes the signals shown in Figure 6-2Ø.

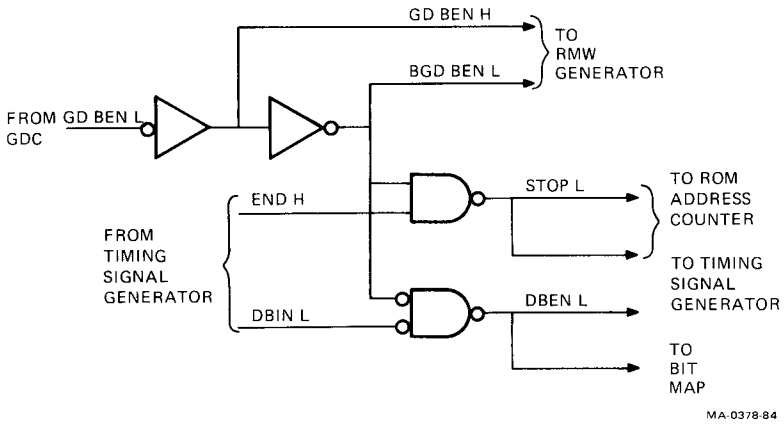


Figure 6-18 BEN and STOP Gates Block Diagram

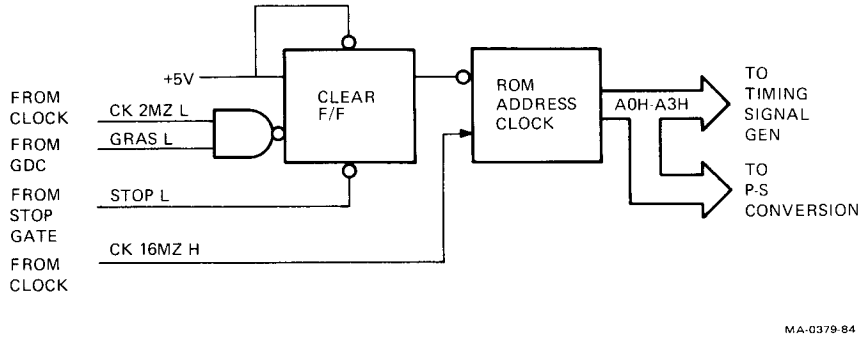


Figure 6-19 ROM Address Counter Block Diagram

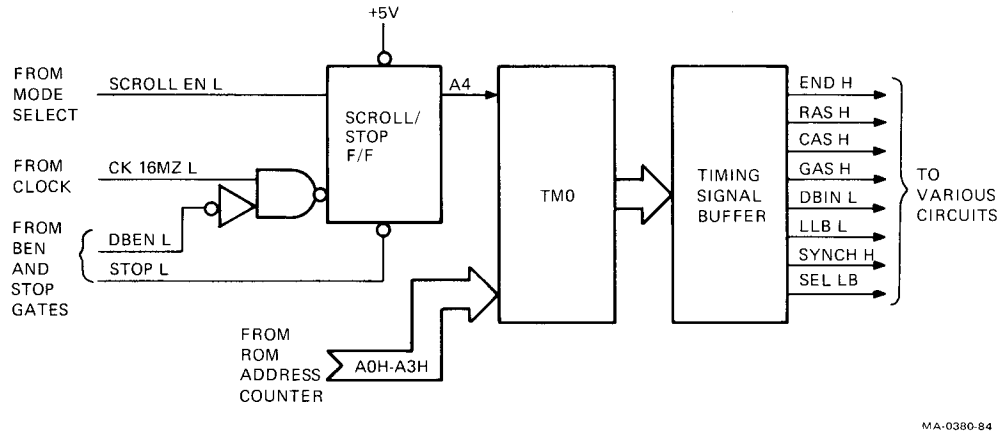


Figure 6-20 Timing Signal Generator Block Diagram

6.2.5.5 Read-Modify-Write (RMW) Generator -- The RMW generator generates RMW control signals used during RMW cycles that affect the bit map. The RMW generator (Figure 6-21) consists of the following components.

- RMW F/F -- generates RMW outputs based on the condition of bus enable inputs (GD BEN H and BGD BEN L which are always the inverse value of each other) on the trailing edge of END H input, or based on jamset input from ERASE F/F.
- ERASE F/F -- is clocked by the trailing edge of RAS H input, with a low output (when ERASE L input is true) forcing RMW F/F to output true RMW control signals.

Later in this chapter, Table 6-6 describes the signals shown in Figure 6-21.

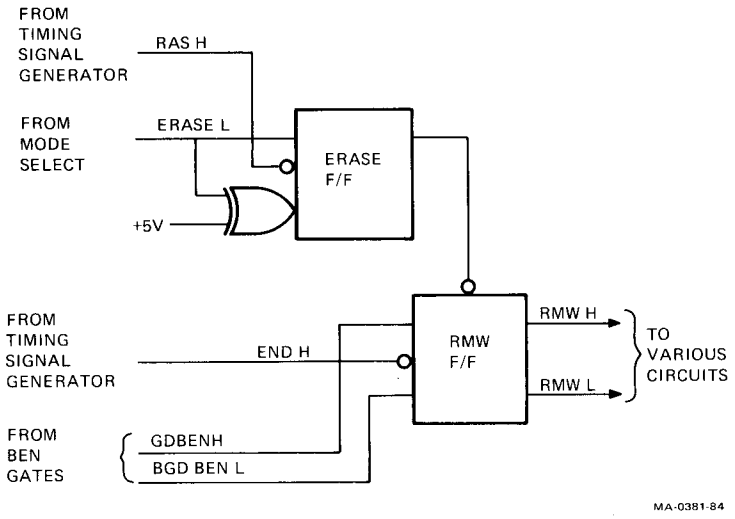


Figure 6-21 Read-Modify-Write (RMW) Generator Block Diagram

6.2.5.6 BLANK Generator -- The BLANK generator outputs blanking control signals which are based on blank input from GDC (G BLK H) and synchronized by timing signal generator inputs. The BLANK generator (Figure 6-22) consists of the following components.

- S BLANK F/F -- generates S Blank L from inverted GBLK H input, with output synchronized to RAH H input.
- BLANK F/F -- generates BLANK L and BLANK H from inverted GBLK H input, with outputs synchronized to SYNCH H input.
- BLANK Generator -- consists of BLANK I F/F, which generates BLANK I L output from BLANK L input, and D BLANK buffer, which generates D BLANK L output to D/A (Both are clocked by CK 16MZ H, with three clocks needed to reflect any change in BLANK L input at D BLANK L output.)

Later in this chapter, Table 6-6 describes the signals shown in Figure 6-22.

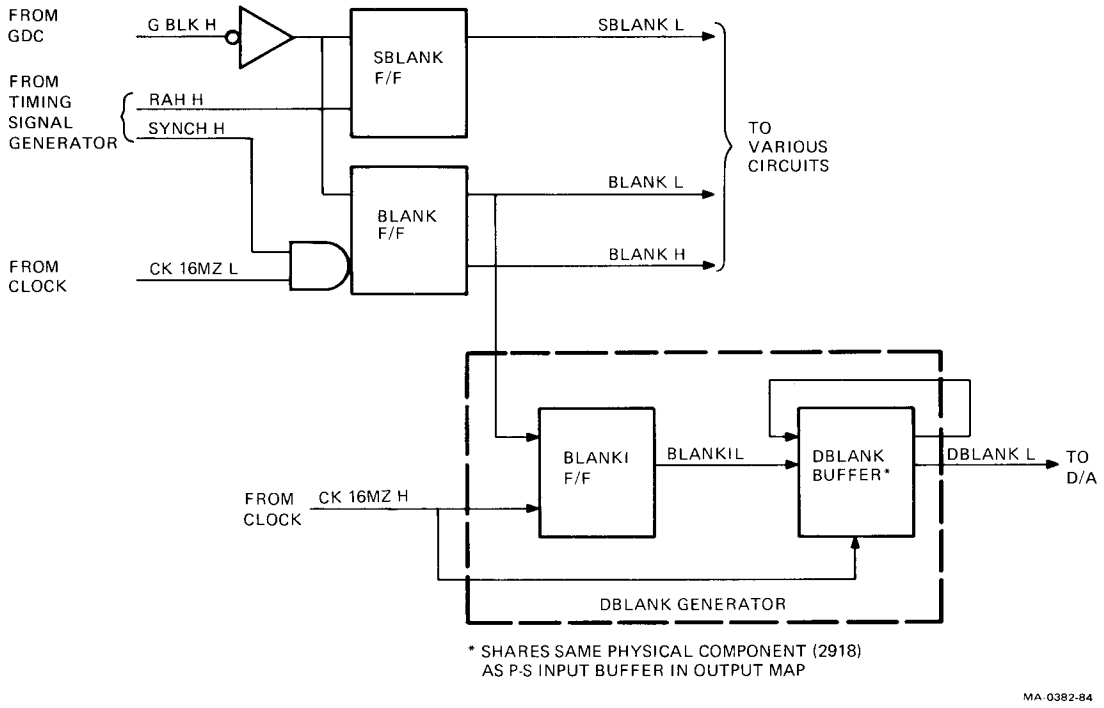


Figure 6-22 BLANK Generator Block Diagram

6.2.6 Mode Select

The mode select circuit (Figure 6-23) consists of two register devices, register zero (REG Ø) and register one (REG 1).

The mode select registers are programmed by the CPU or CP. The register values are used in conjunction with values programmed into the following video logic devices to define the video logic write mode.

- GDC (refer to section 6.2.4)
- Logic unit register in logic unit circuit (refer to section 6.2.11)
- Write mask latch in bit map write enable circuit (refer to section 6.2.9)
- Scroll address counter in bit map addressing circuit (refer to section 6.2.7.2)
- Vector pattern register in pattern select circuit (refer to section 6.2.1Ø)

Depending upon how these various components are programmed, the video logic can operate in one of the following six different write modes.

- Mode Ø (Read Back Mode) -- defines a read back of bit map for hardcopy and diagnostic purposes.

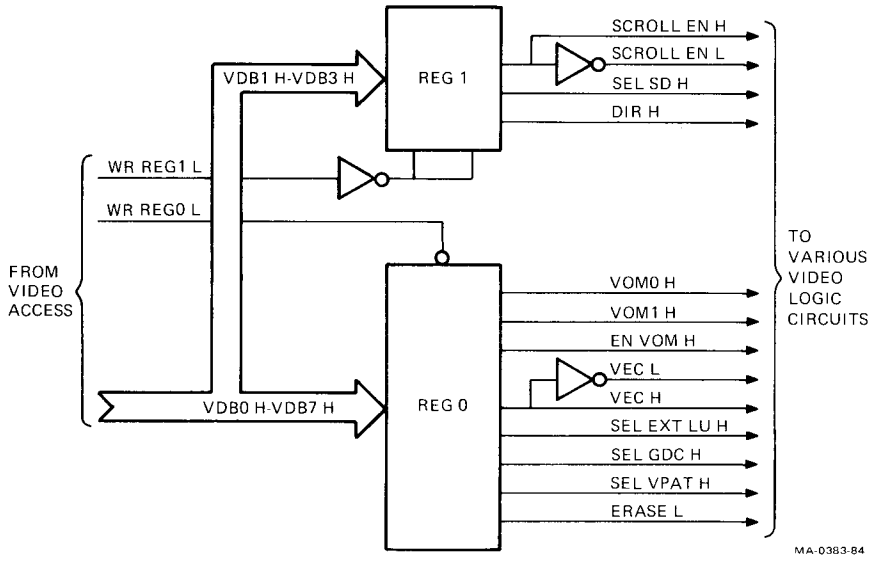


Figure 6-23 Mode Select Block Diagram

- Mode 1 (Text Mode) -- defines a write of character patterns one byte at a time with write mask set to appropriate values.

- Mode 2 (Vector Mode) -- defines vector writing

- Mode 3 (DMA Scroll Mode) -- defines byte write mode for scrolling with write mask set to all zeros.

- Mode 4 (Screen Erase Mode) -- defines erasing of the entire displayed frame to a specified backgraound intensity.

- Mode 5 (Word/Line Erase Mode) -- defines erasing of a 16-bit word location to a specifed background intensity in single GDC write cycle.

Appendix D and Table 6-6 (later in this chapter) provide descriptions of the bit values for the mode select registers. Appendix E provides descriptions of the bit values of for the various components used for each of the six write modes.

6.2.7 Bit Map Addressing Circuit

The bit map addressing circuit generates row and column addresses for accessing the bit map. The bit map addressing circuit (Figure 6-24) consists of the following circuits.

Plane and byte select
Address select
Row/column mux

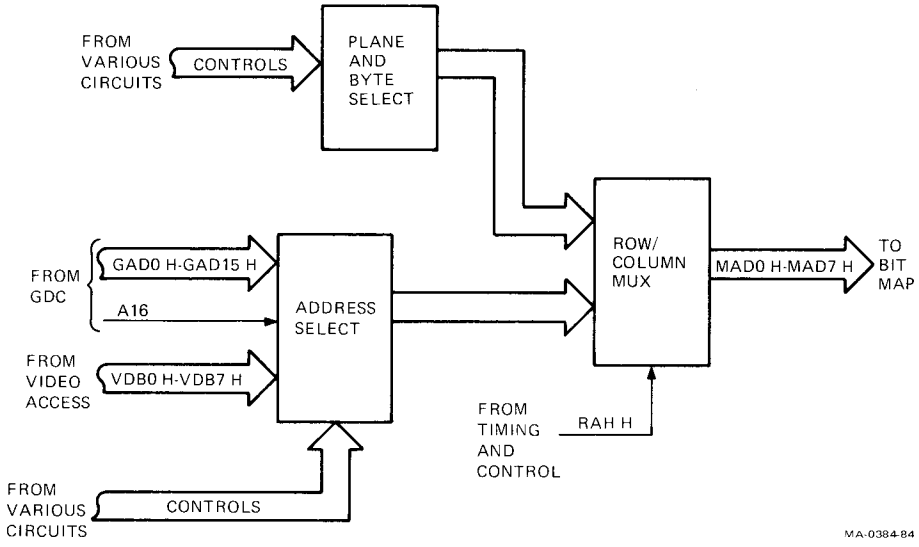


Figure 6-24 Bit Map Addressing Circuit Block Diagram

6.2.7.1 Plane and Byte Select -- The plane and byte select circuit has the following two functions.

- Generate plane (EPS H and EPS L) and byte select (EBS L) controls used by various video circuits
- Generate generate plane and byte select values used by row/column mux in the output of bits three and six of the high order byte of addressing.

The plane and byte select circuit (Figure 6-25) consists of the following circuits/components.

- DAD Generator -- ANDs inversion of LAD16 H with VEC L, and inversion of LB H with VEC H to output true DAD3 signals (DAD3 H high, DAD3 L low) when either ANDed pair are both highs.

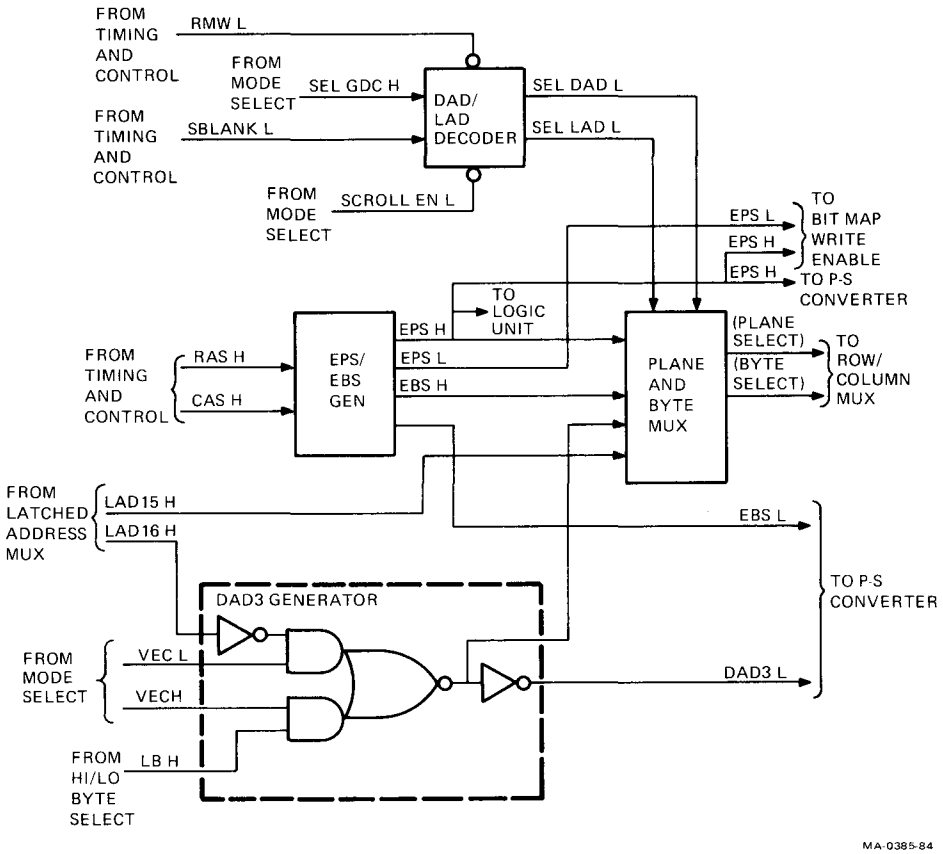


Figure 6-25 Plane and Byte Select Block Diagram

- EPS/EBS Generator -- consists of two serial F/Fs enabled by RAS H high (both reset whenever RAS H is false) to output true EPS H and EPS L signals on the trail edge of the first CAS H input (following RAS H going high), and true EBS H and EBS L signals on the trail edge of the second CAS H input.

- DAD/LAD Decoder -- decodes SEL GDC H input during screen blank intervals (S BLANK L input low) when enabled by SCROLL EN L true (low), with SEL DAD L output decoded for SEL GDC H low (with decode output ANDed with RMW L to output SEL DAD L that is tied to RMW L time), and SEL LAD L decoded for SEL GDC H high.

- Plane and Byte Mux -- selects plane and byte select values to be used by row/column mux for bits three and six of the high order byte of addressing.

Later in this chapter, Table 6-6 describes the signals shown in Figure 6-25.

6.2.7.2 Address Select -- The address select circuit has the following two functions.

- Select address values to be output to the row/column mux

- Generate LAD15 H -- LAD16 H output values based on GDC input whenever GDC address values are selected for output to the row/column mux LAD15 H -- LAD16 H values are used at the plane and byte select circuit to determine plane and byte select values to be supplied to the row/column mux.

The address select circuit (Figure 6-26) consists of the following components.

- Scroll Address Counter - consists of four counter devices clocked by RMW L that bare either down (DIR H true) or up (DIR H false) from a value loaded by either the CPU or CP (VDBØ H -- VDB7 H, WR LB SCROLL DA L, and WR HB SCROLL DA L inputs from video access), with the counter value output to latched address mux.

- Latched Address Mux -- consists of four mux devices selecting either scroll address counter (SADØ H -- SAD 13H) or GDC inputs (GADØ H-GAD13H, GAD15 H, and A16), RAS H latch the selected input values into the mux, and SCROLL EN H, in conjunction with RMW H, selects which values are latched (GDC for SCROLL EN H low).

Later in this chapter, Table 6-6 describes the signals shown in Figure 6-26.

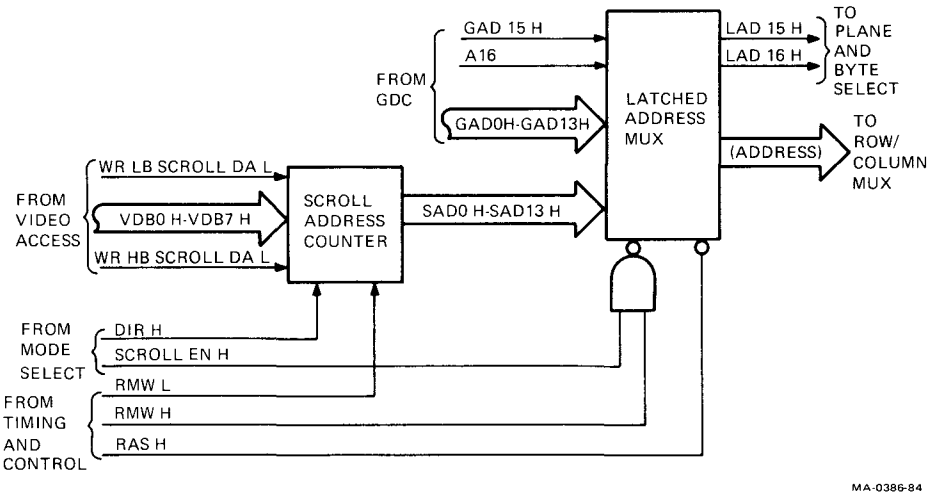


Figure 6-26 Address Select Block Diagram

6.2.7.3 **Row/Column Mux** -- The row/column mux (Figure 6-27) consists of the following two mux devices, each selecting inputs based on value of RAH H.

- RAH H high (true) -- the mux devices select "B" inputs to mux for row address values.
- RAH H low (false) -- The mux devices select "A" inputs for column address values.

Later in this chapter, Table 6-6 describes the signals shown in Figure 6-27.

6.2.8 High/Low (Hi/Lo) Byte Select

The hi/lo byte select circuit selects either GDC low order byte data (GADØ H -- GAD7 H) or GDC high order byte data (CAD8 H -- GAD15 H) for output to the mask select and write data select circuits (GDØ L -- GD7 L), during RMW cycles.

The hi/lo byte select circuit (Figure 6-28) consists of the following components.

- Hi/Lo Byte Mux -- is enabled by RMW L low (true) to select either low byte (select input low) or high byte inputs (select input high) for output as GDØ L -- GD7 L (GDØ L -- GD7 L are all high when RMW L is high).
- Mux Select Gate -- ANDs SEL GDC H with EPS L, and invert SEL GDC H with LB H to output select value to the hi/lo byte mux.

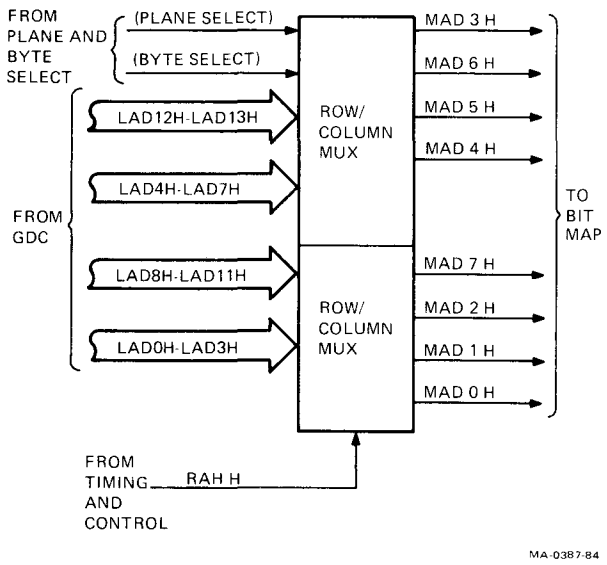


Figure 6-27 Row/Column Mux Block Diagram

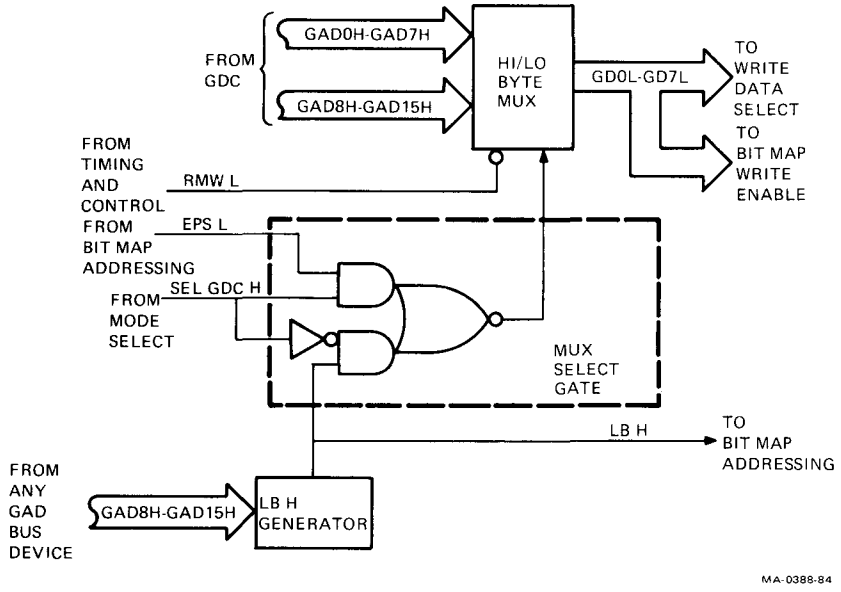


Figure 6-28 Hi/Lo Byte Select Block Diagram

- LB H Generator -- monitors GAD8 H -- GAD15 H bus lines to generate high (true) LB H output when any one of the high byte GAD signals is an active high (true).

Later in this chapter, Table 6-6 describes the signals shown in Figure 6-28.

6.2.9 Bit Map Write Enable

The bit map write enable circuit generates up to eight write enable signals for the bit map. This allows writing to the bit map to involve only a specific bit or bits, no bits, or all bits of a data byte during any given RMW cycle.

The bit map write enable circuit (Figure 6-29) consists of the following components.

- Mask Select Mux -- generates a write enable mask value based on either CPU/CP inputs (VDBØ H -- VDB7 H, when VEC H is low), or hi/lo byte select inputs originating at the GDC (GDØ L -- GD7 L, when VEC H is high).

- Write Mask Latch -- generates the write enable outputs during RMW L low, with the write enables based on the last enabled mask select mux input to the latch.

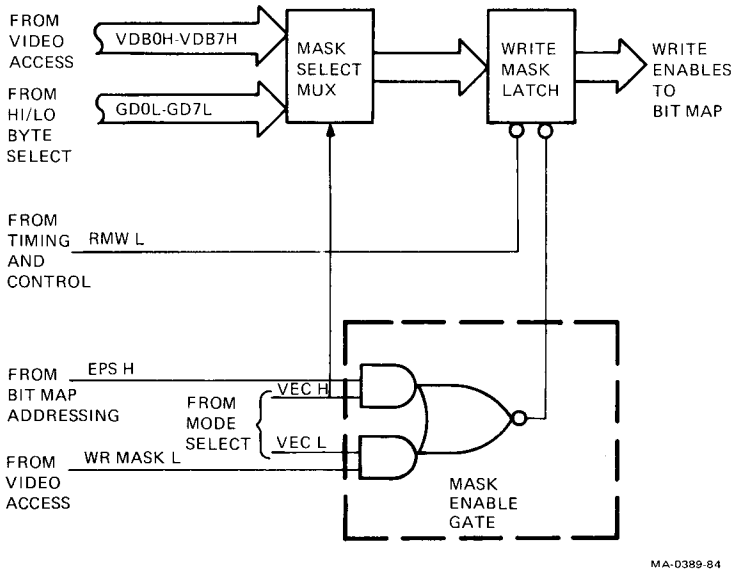


Figure 6-29 Bit Map Write Enable Block Diagram

- Mask Enable Gate -- ANDs EPS H true with VEC H true to enable loading of GDØ L -- GD7 L mask values passed by the mask select mux. Also ANDs VEC L false and WR MASK L true to enable loading of VDBØ H -- VDB7 H mask values passed by the mask select mux.

> **NOTE**
> **Write mask values from the mux are actually clocked into the latch by a low to high on the enable input: the trailing edge of EPS H when VEC inputs are true and the trailing edge of WR MASK L when VEC inputs are false.**

Later in this chapter, Table 6-6 describes the signals shown in Figure 6-29.

6.2.1Ø Pattern Select

The pattern select circuit stores character and vector patterns loaded by the CPU or CP and selects between these patterns for output to the logic unit.

The pattern select logic (Figure 6-3Ø) consists of the following circuits/components.

- Character Pattern Address Counter -- counts up from a zero starting value (loaded by RD INIT CB ADDR L low) with incrementing output used as the address value for character pattern buffer.

- Counter Clock Gate -- enables counting by character pattern address counter only when the character pattern bufffer is not being loaded.

- Character Pattern Buffer -- consists of two 32 X 4-bit RAM devices that provide 32 bytes of character pattern storage with patterns loaded (WR CHAR BUFF L low) or read (WR CHAR BUF L high) sequentially.

- Pattern Multiplier Register -- is programmed by the CPU (WR PAT MULT L low) with a multiplication factor (1 through 16) to be used for each vector pattern bit.

- Pattern Multiplier Counter -- enables the register clock gate whenever the number of clock inputs defined by the multiplication factor have been counted.

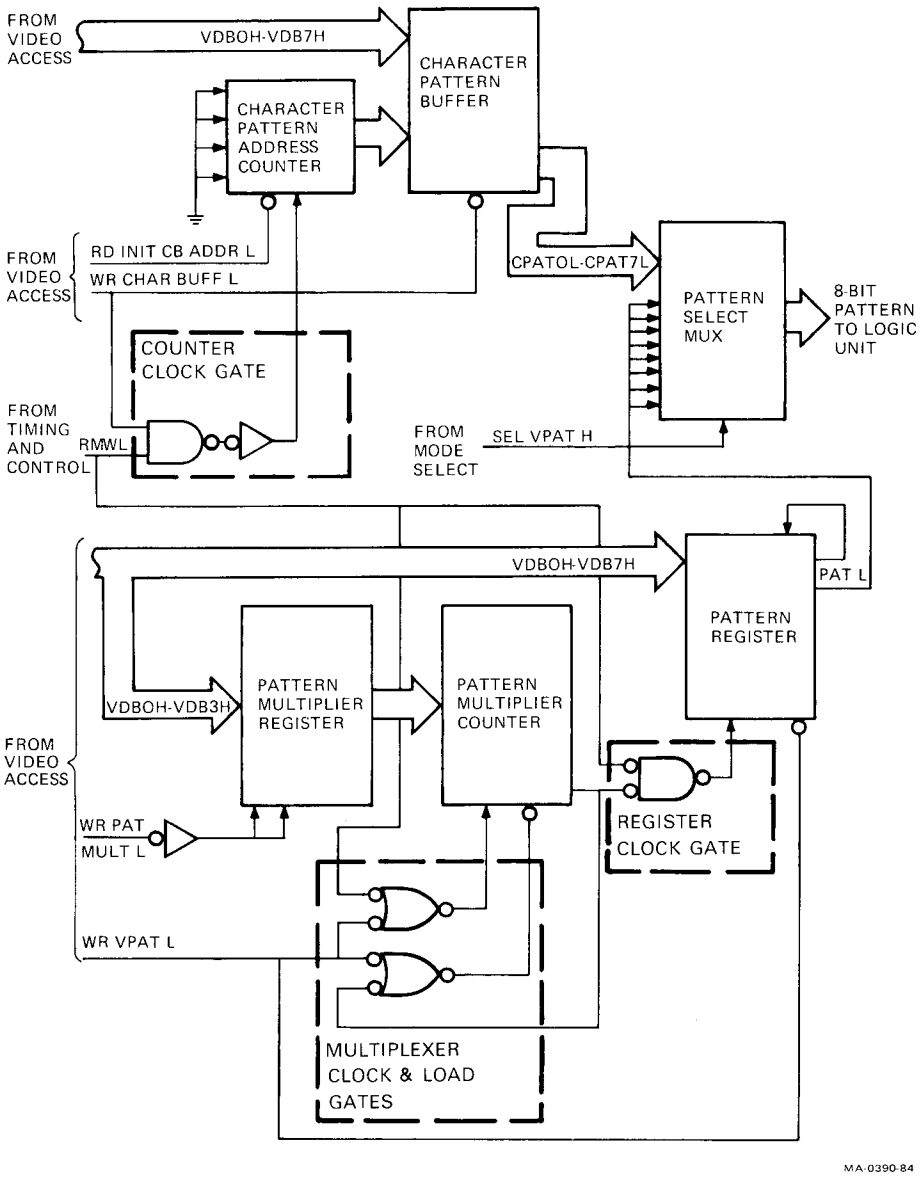


Figure 6-30 Pattern Select Block Diagram

- Multiplier Clock and Load Gates -- enables clocking of the pattern multiplier counter on RMW L cycles, and whenever a new pattern is loaded into the pattern register (WR VPAT L low). Reloads the pattern multiplier counter whenever the correct count has been achieved, or when a new pattern is loaded into the pattern register.

- Register Clock Gate -- enables RMW L to clock the pattern register only when the correct multiplication factor count has been sensed by the pattern multiplier counter.

- Pattern Register -- is an eight-bit recirculating shift register loaded by the CPU (WR VPAT L low) with vector pattern (the pattern is shifted through the register), and then output to the pattern select mux, one bit at a time (MSB first).

- Pattern Select Mux -- consists of two mux devices outputting eight bits of either character (SEL VPAT H low) or vector (SEL VPAT H high) pattern value to the logic unit.

Later in this chapter, Table 6-6 describes the signals shown in Figure 6-30.

6.2.11 Logic Unit

The logic unit converts data input from the bit map into new write pattern data output to the write data select circuit. This conversion is based on the pattern (either character or vector) input from the pattern select circuit, bit map data input from the bit map, and control values loaded into the logic unit circuit by the CPU or CP.

The logic unit circuit (Figure 6-31) consists of the following circuits/components.

- Logic Unit Register -- is loaded by CPU or CP (WR LU L low). Control values define write mode (MØ H -- M1 H at ØH for replace, 1H for overlay, and 3H for complement), single (SP H high) or two-plane (SP H low) writing, plane selection in single-plane mode of plane zero (PS H low) or plane one (PS H high), background intensity values for each plane (IBØ H and IB1 H), and foreground intensity values for each plane (IFØ H and IF1 H).

- Intensity Select Mux -- outputs background and foreground intensity values to the logic unit with plane zero values output when EPS H is low, and plane one values output when EPS H is high.

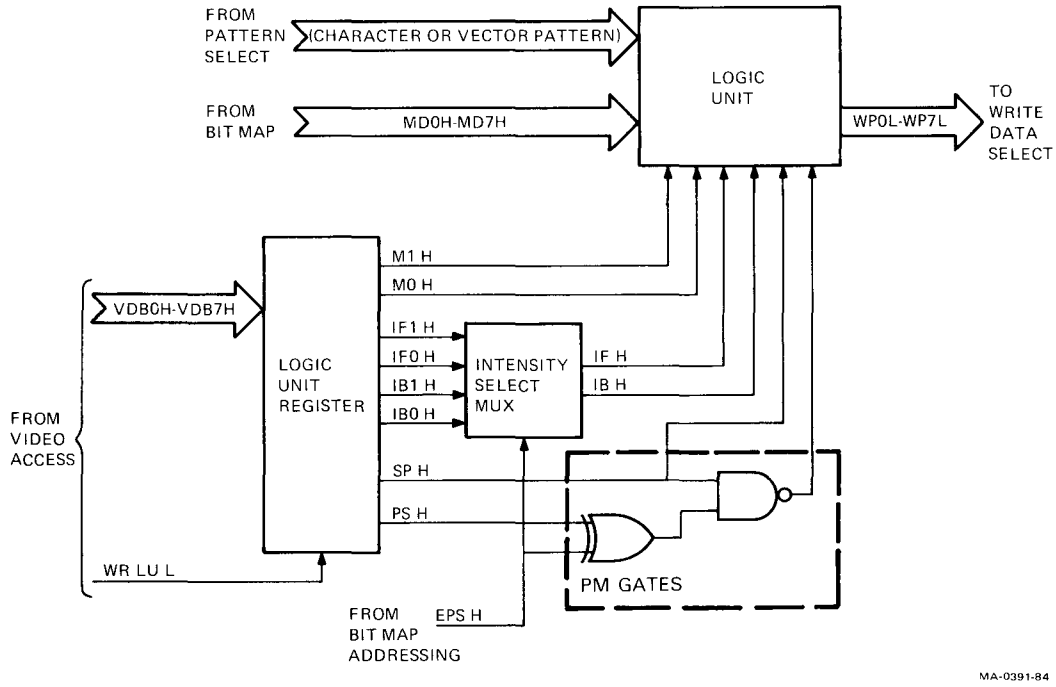


Figure 6-31 Logic Unit Block Diagram

- Plane Management (PM) Gates -- are used only during single-plane writing (SP H high) to provide a low output to the logic unit when EPS H and PS H are opposite values, and high to the logic unit when both signals have same value. Low to high transition indicates that intensity values for the selected plane are being passed by the intensity select mux.

- Logic Unit -- consists of two four-bit algorithm logic unit (ALU) devices that manipulate inputs from the bit map (MDØ H -- MD7 H), pattern select, and other logic unit components into a write pattern (WPØ L -- WP7 L) output to write data select circuit.

Appendix D provides a description of the logic unit register bit values. Later in this chapter, Table 6-6 describes the signal shown in Figure 6-31.

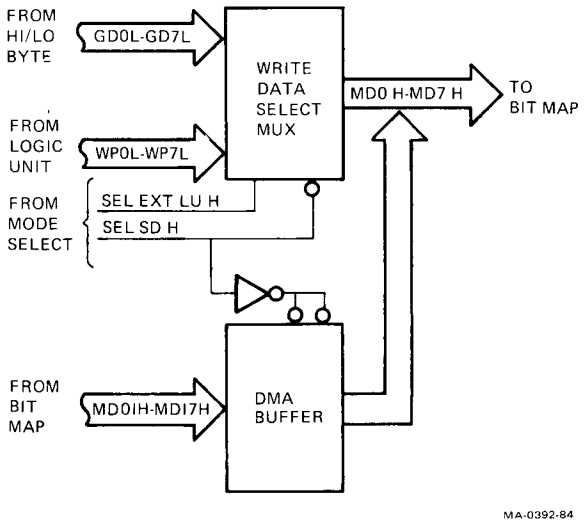


Figure 6-32 Write Data Select Block Diagram

6.2.12 Write Data Select

The write data select circuit passes data to the bit map from either the logic unit (when data is manipulated external to the GDC), to the hi/lo byte select (when data is manipulated internal to the GDC), or to the bit map (during DMA write mode).

The write data select circuit (Figure 6-32) consists of the following components.

- DMA Buffer -- generates data output to the bit map when DMA is enabled (SEL SD H high).
- Write Data Select Mux -- generates data output to the bit map when DMA is disabled (SEL SD H low), from either the hi/lo byte select (SEL EXT LU H low) or logic unit (SEL EXT LU H high).

Later in this chapter, Table 6-6 describes the signals shown in Figure 6-32.

6.2.13 Bit Map

The bit map provides the memory space for two-plane display. Each plane is an 800H X 327V pixel memory array, with two 800H X 240 pixel arrays for actual display and the remainder for set-up display purposes.

The bit map circuit (Figure 6-33) consists of the following components.

- Bit Map Memory -- is eight 64K X 1-bit RAM devices that provide 64K bytes of memory or the two-plane pixel array.
- Buffer Gates -- is enabled by VEC L high to pass bit map data outputs to the read back buffer.

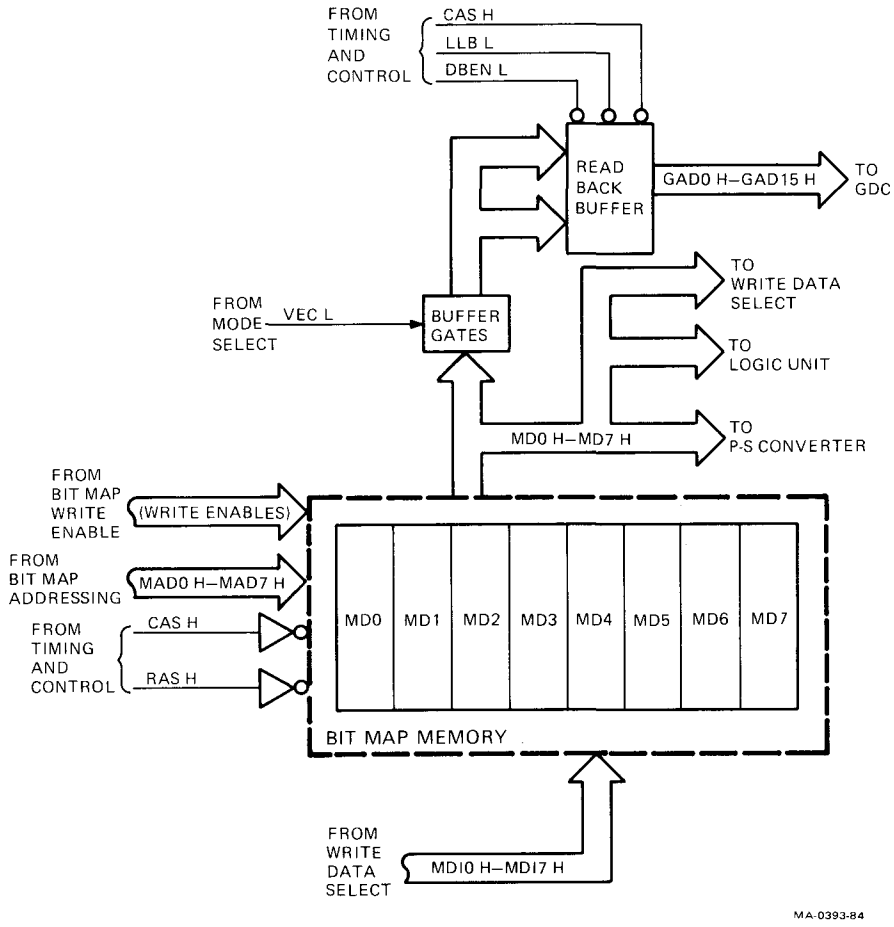


Figure 6-33 Bit Map Block Diagram

- Read Back Buffer -- is two eight-bit buffers, one for high byte output to the GDC (GAD8 H -- GAD15 H when DBEN L and CAS H are both low), and one for low byte output to the GDC (GADØ H -- GAD7 H when DBEN L and LLB L are both low).

Later in this chapter, Table 6-6 describes the signals shown in Figure 6-33.

6.2.14 Parallel-to-Serial (P/S) Converter

The P/S converter circuit changes parallel data input from the bit map into serial data output to the output map.

Four bytes of parallel data are input to the P/S converter circuit, two bytes for each plane (high byte and low byte). The parallel data is then converted to four bits of serial data output, two bits for each plane (high bit and low bit), and output as a two-bit value to the output map. Either the high-bit values for each plane or the low-bit values are passed to the output mux at one time.

The P/S converter circuit (Figure 6-34) consists of the following circuits/components.

- Bit Select (BS) Gate -- gates EBS 1 and DAD3 1 input with Scroll enable inputs to generate a BS H value to the gate decoder (BS H low for selecting the low order bit, BS H high for the high order bit).

- Gate Decoder -- is enabled by RMW L low to decode plane (EPS H) and bit (BS H) inputs into single gate enable output for the selected plane and bit (GØ one for plane zero low bit, G1 L for plane one low bit, G2 L for plane zero high bit, and G3 L for plane one high bit).

- CTØ/CT1 -- consists of two 64-byte ROM devices sequentially addressed by AØ H through A3 H and RMW H inputs to generate mode select value outputs to the P/S mode select buffer. One ROM is for screen blank conditions (CT1 enabled by BLANK L low) and one is for nonblank conditions (CTØ enabled by BLANK H low).

- P/S Mode Select Buffer -- outputs mode select values to P/S converters (four pairs of SØ H -- S1 H signals, pairs A through D, with one pair for the four P/S converter devices).

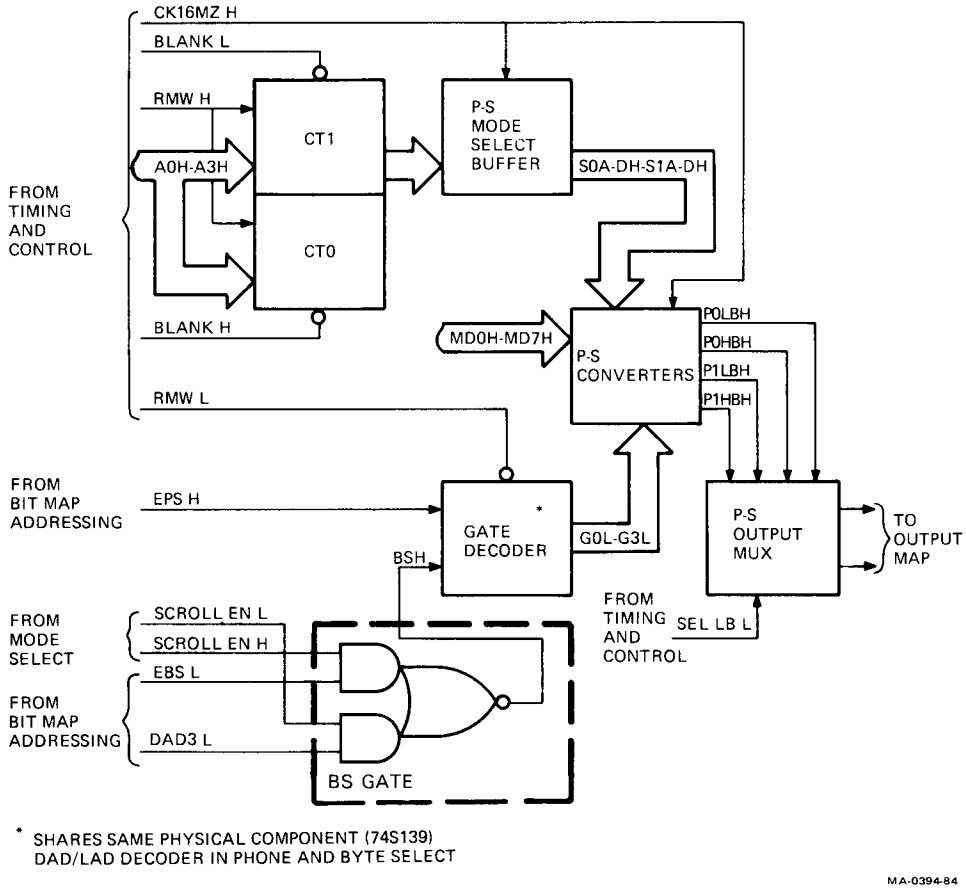


Figure 6-34 Parallel-to-Serial (P/S) Converter Block Diagram

- P/S Converters -- consists of four eight-bit shift/storage registers, one high byte and one low byte P/S converter for each plane. Each register is clocked by CK 64MZ H, gated by gate decoder input, and controlled by P/S mode select buffer input. Serial output from each is sent to the P/S output buffer.

- P/S Output Buffer -- selects either plane zero and one high bit values (PØ HB H, and Pl HB H when SEL LB L is high) or plane zero and one low bit values (PØ LB H and Pl LB H, when SEL LB L is low) for output to the output map.

Later in this chapter, Table 6-6 describes the signals shown in Figure 6-34.

6.2.15 Output Map

The output map generates color (blue, green, and red) and monochrome values to the D/A or conversion to video output for either a color (VR241) or monochrome (VR240) monitor.

The color and monochrome values are based on data programmed into the output map by the CPU or CP, and are accessed for output to the D/A by map select (VOMØ H -- VOMl H signals that originate at mode select) and bit-plane select (either PØ HB H -- Pl HB H or PØ LB H -- Pl LB H signals that originate at the P/S converter) values.

The output map memory space is organized into four 4 X 8-bit maps (mapØ through map3). Each map contains four bytes of D/A output values, two bits for each color and two bits for monochrome. Map select inputs define which map is to be selected, while bit plane inputs define the byte within that map to be output to the D/A.

The output map circuit (Figure 6-35) consists of the following circuits/components.

- Video Output Map (VOM) -- consists of two 16 X 4-bit RAM devices that provide memory for output map values, one RAM device for the upper four bits of mapØ through map3, and one for the lower four bits. Memory is written to by CPU or CP when WR VOM L is low, and VOM output when WR VOM L is high.

- VOM Address Select -- enables CPU or CP access when EN VOM H is low (address mux device passes VAØ H -- VA3 H inputs), and video logic access when EN VOM H is high (address mux passes VOMØ H -- VOMl H while the P/S input buffer passes PØ HB H -- P l HB H or PØ LB H -- Pl LB H).

- VOM Buffer -- buffers VOM data to the D/A and VOM read back register as four sets of two-bit cones (VRØ H -- VRl H for red, VGØ H -- VGl H for green, VBØ H -- VBl H for blue, and VMØ H -- VMl H for monochrome.

- VOM Read Back Register -- is enabled by RD VOM L low to pass values input from VOM (via VOM buffer) out to the CPU or CP.

Table 6-4 defines the VOM accessing scheme for both the CPU or CP and video logic access of each byte for each output map. Table 6-5 defines the intensity value associated with each of the two-bit color and monochrome values output to the D/A. Later in this chapter, Table 6-6 describes the signals shown in Figure 6-35.

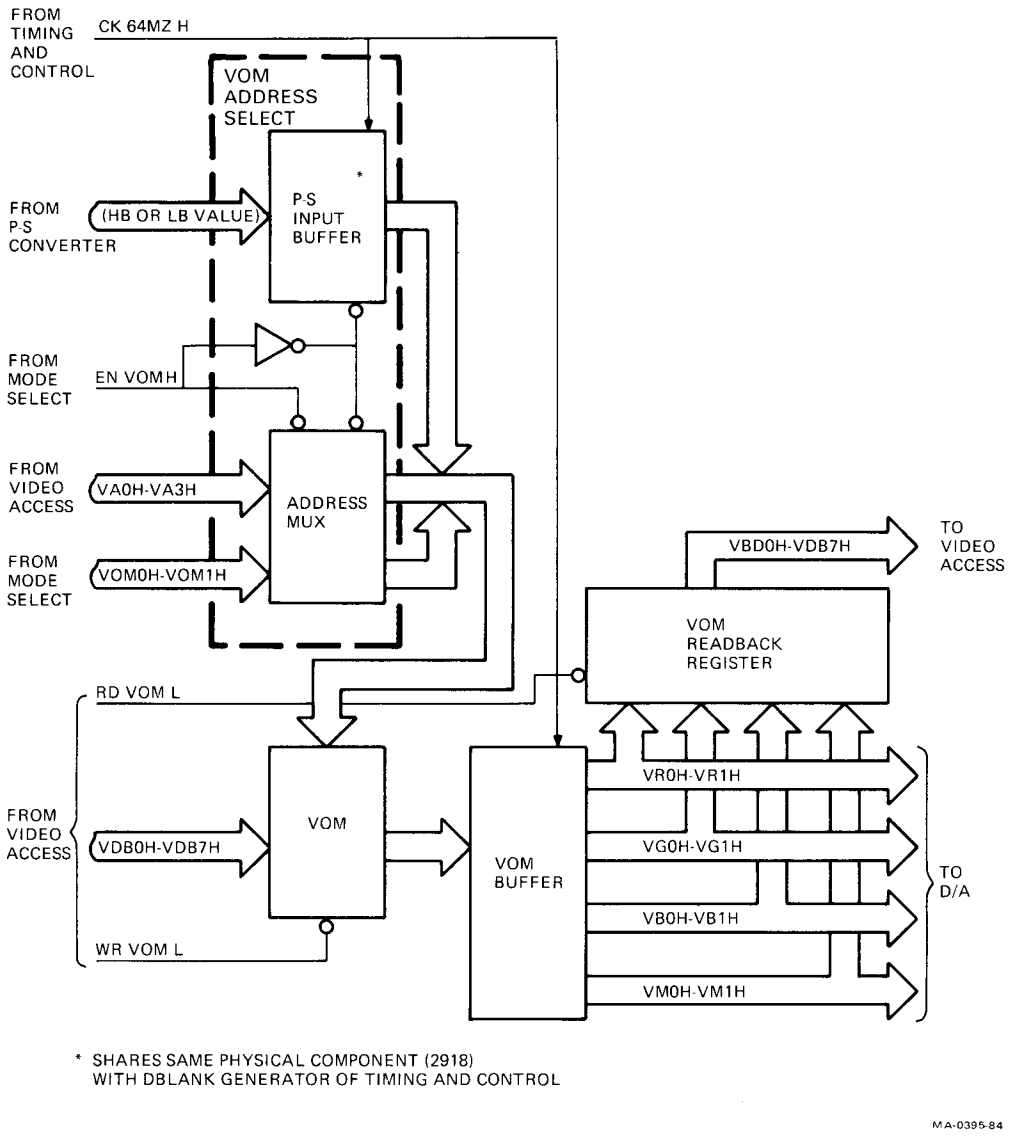


Figure 6-35 Output Map Block Diagram

Table 6-4 Video Output Map (VOM) Addressing

Processor Access (EN VOM H LOW)		Video Output Access (EN VOM H HIGH)				
MAP/Byte	CPU Address	CP Address	VOMØ H	--VOM1 H	PØ H	--P1 H*
MAPØ/BYTEØ	177ØØØ	1ØH	Ø	Ø	Ø	Ø
MAPØ/BYTE1	177ØØ2	11H	Ø	Ø	1	Ø
MAPØ/BYTE2	177ØØ4	12H	Ø	Ø	Ø	1
MAPØ/BYTE3	177ØØ6	13H	Ø	Ø	1	1
MAP1/BYTEØ	177Ø5Ø	14H	1	Ø	Ø	Ø
MAP1/BYTE1	177Ø52	15H	1	Ø	1	Ø
MAP1/BYTE2	177Ø54	16H	1	Ø	Ø	1
MAP1/BYTE3	177Ø56	17H	1	Ø	1	1
MAP2/BYTEØ	177Ø6Ø	18H	Ø	1	Ø	Ø
MAP2/BYTE1	177Ø62	19H	Ø	1	1	Ø
MAP2/BYTE2	177Ø64	1AH	Ø	1	Ø	1
MAP2/BYTE3	177Ø66	1BH	Ø	1	1	1
MAP3/BYTEØ	177Ø7Ø	1CH	1	1	Ø	Ø
MAP3/BYTE1	177Ø72	1DH	1	1	1	Ø
MAP3/BYTE2	177Ø74	1EH	1	1	Ø	1
MAP3/BYTE3	177Ø76	1FH	1	1	1	1

Table 6-5 Intensity Definition for Output Map Outputs

VxØ	H-Vx1 H*	Intensity
1	1	Ø (bright)
Ø	1	1 (normal)
1	Ø	2 (dim)
Ø	Ø	3 (dark)

* x is either R, G, B, or M.

6.2.16 Digital-to-Analog (D/A)

The D/A circuit converts two-bit color and monochrome value inputs from the output map into analog video signals output to the color (VR241) or monochrome (VR24Ø) monitors.

The D/A (Figure 6-36) consists of the following circuits/components.

- J8 -- is a 15-pin connector that provides video output to either color or monochrome monitors.

NOTE
J8 can also be used for output of keyboard data output.

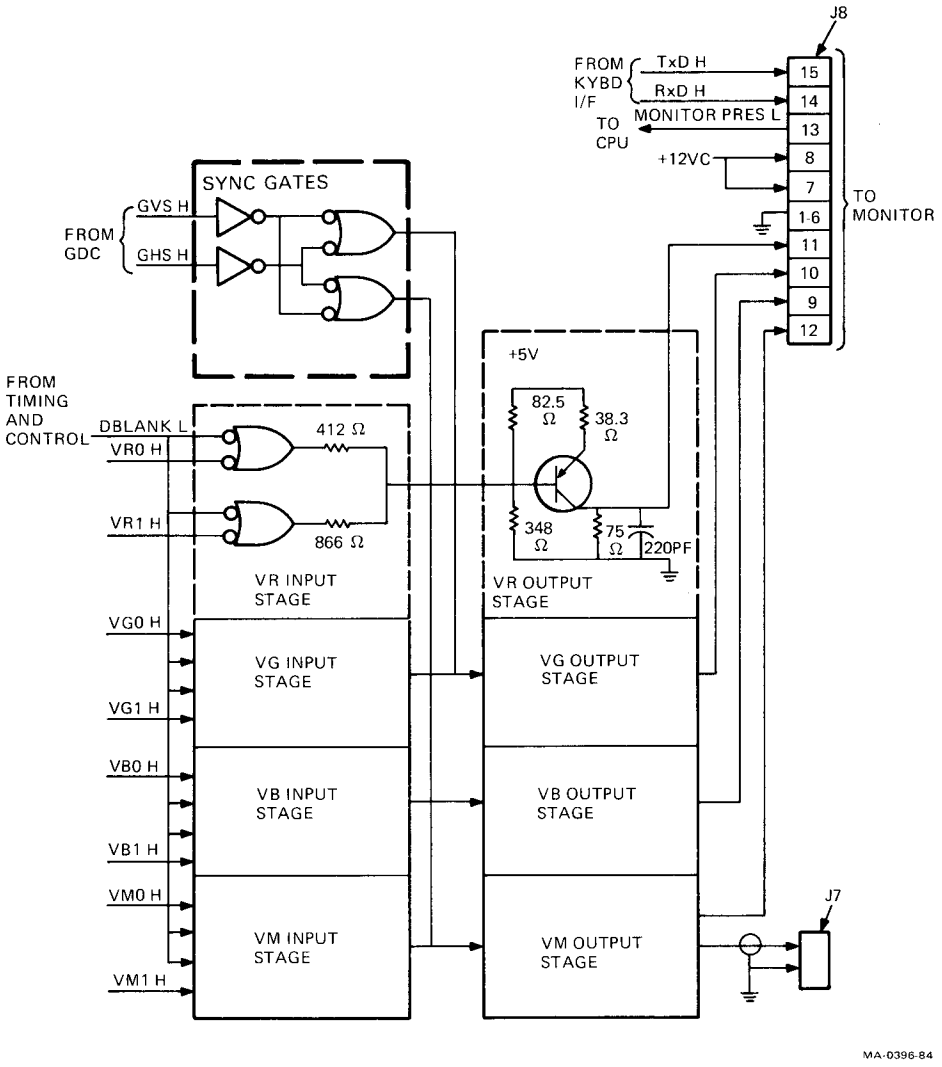


Figure 6-36 Digital-to-Analog (D/A) Block Diagram

- J7 -- is a BNC connector for video output to a monochrome monitor when keyboard data is not being output through J8, or for output to a slave monochrome monitor (monochrome monitor configured in addition to color monitor).

- Input Stages -- consists of four identical circuits, one for each color and monochrome values. Each stage provides a variable positive value biasing to the base of the corresponding output stage transistor (D BLANK L low or two low inputs from the output map will both result in cutting output stage voltage output to a level below the voltage needed for display).

- Sync Gates -- encode vertical (G VS H) and horizontal (G HS H) into monochrome and green (VG) outputs to the monitor by providing additional positive biasing to the output stage transistors and cutting output stage voltage to a value below the output for screen blanking.

- Output Stages -- consist of the following four similar PNP transistor networks that generate the actual video outputs to the monitor.

  VR output stage -- shown in Figure 6-36

  VB output stage -- identical to VR

  VG output stage -- has the 348 ohm resistor replaced by a 332 ohm resistor for input of sync value

  VM output stage -- has the 348 ohm resistor replaced by a 200 ohm resistor for input of sync value, and the capacitor is replaced by an NPN transistor network for developing two monochrome video outputs.

Table 6-6 describes the signals shown in Figure 6-36.

6.3 SIGNAL DESCRIPTIONS

Table 6-6 describes all the signals shown in this chapter. These descriptions are provided for reference, and are listed alphabetically by mnemonic. Numeric mnemonics are listed last.

6.4 SCHEMATIC REFERENCE INFORMATION

Table 6-7 identifies the logic board component coordinate, and schematic page and coordinate references for each video logic circuit and component identified in this chapter.

NOTE

The reference listing is based on Rev. C of the schematics (CS 5415495-0-1).

Table 6-6 Video Logic Signal Description

Signal Mnemonic	Signal Name	Description
AØ H -- A3 H	Address Ø through 3 High	Sequential counter derived address used by ROM devices in timing and control circuit (TMØ) and P/S converter (CTØ and CT1).
A15 H	Address Bit 15 High (CP)	Defines whether CP ROM (A15 H low) or CP RAM (A15 H high) is enabled when IO/M is low.
ALE	Address Latch Enable	Enables address latch to input 85ADØ H -- 85AD15 H signals from CP.
BGD BEN L	Buffered GDC Data Bus Enable Low	Buffered version of GD BEN L from GDC.
BLANK H/L	Blank High and Low	True control signals during screen blank periods developed from G BLK H high as synchronized by SYNC H and CK 16 MZ L.
BLANK I L	Blank Inverted Low	True (low) signal during screen blank periods developed from BLANK L and used to develop D BLANK L.
BS H	Bit Select High	Used by gate decoder in P/S converter circuit to define whether high (BS H high) or low (BS H low) order byte bit is to be gated.
CAS H	Column Address Strobe High	Timing signal generator output used to coordinate EPS H and EBS H generation with column address strobe of bit map (also disables input of bit map data into high order byte of bit map read back buffer when high).
CK2 MZ L	Clock 2 MHz Low	Clock used by GDC.
CK8 MZ L	Clock 8 MHz Low	Clock used by CP.

Table 6-6 Video Logic Signal Description (Cont)

Signal Mnemonic	Signal Name	Description
CK16 MZ H/L	Clock 16 MHz High and Low	Clocks used by various video logic circuits.
DAD3 H/L	Display Address Bit 3 High and Low	Used to generate byte select address value to row/column mux when SEL DAD L is low (scroll addressing of bit map rather than GDC access), and developed from LB H and VEC H during text mode, or VEC L and LAD16 H during vector mode.
D BEN L	Data Bus Enable Low	Enables GDC access to GDC data bus lines gated from BGD BEN L (buffered version of GD BEN L from GDC) and D BIN L are both true.
D BIN L	Data Bus Input Low	Control signal output of timing signal generator coordinating GDC access to GDC data bus lines by providing enable (D BIN L low) or disable (D BIN L high) to D BEN L gate.
D BLANK L	Display Blank Low	Active low during screen blank periods used at D/A to force all video signal outputs to blank level.
DIR H	Direction High	Control output from register one which defines whether scroll address counter is to increment (DIR H low) or decrement (DIR H high).
EBS H/L	Enable Bit Select High and Low	Coordinates byte select activity with EBS H and EBS L going to true condition on second CAS H true after RAS H true condition.
EN VOM H	Enable VOM High	Register one output defining GDC (EN VOM H low) or video logic (EN VOM H high) access of VOM.

Table 6-6 Video Logic Signal Description (Cont)

Signal Mnemonic	Signal Name	Description
END H	End High	Control output from timing signal generator used to generate STOP L low when GDC is not seeking access to GDC bus lines (BGD BEN L is high to stop gate), or to start RMW cycle when GDC is seeking access to GDC bus lines (GD BEN H high to RMW generator).
EPS H/L	Enable Plane Select High and Low	Coordinates plane select activity with EPS H and EPS L signals going true on first CAS H true after RAS H true condition.
ERASE L	Erase Low	Register Ø output defining erase condition when low.
GØ L -- G3 L	Gate Ø through 3 Low	Gate inputs to each of the four P/S converter devices, one gate for each, and one gate at a time active, defining which bit of which plane is processed.
GADØ H -- GAD15 H	Gate Ø through 15 High	GDC Address/Data Lines zero GDC bus lines used for transfer of data and address values.
G BLK H	GDC Blank High	GDC output defining screen blank condition.
GDØ L -- GD7 1	GDC Data Ø through 7 Low	Data originating at GDC as either GADØ H -- GAD7 H or GAD8 H -- GAD15 H and used for write data to bit map during GDC access of bit map.
GD BEN L	GDC Bus Enable Low	GDC output requesting access of GDC bus lines.
G HS H	GDC Horizontal Sync High	GDC output defining horizontal sync period.

Table 6-6 Video Logic Signal Description (Cont)

Signal Mnemonic	Signal Name	Description
G RAS L	GDC Row Address Strobe Low	GDC control output used at ROM address clock generator to start counter.
G RD L	GDC Read Low	Low input from CPU to video access circuit to access a video logic component for a read transaction.
G VS H	GDC Vertical Sync High	GDC output defining vertical sync period.
G WLB L	GDC Write Low Byte Low	Low input from GDC to video access circuit to access a video logic component for a write transaction.
IB H	Intensity, Background High	Defines background intensity factor to logic unit for either plane zero (developed from IBØ H) or plane 1 (developed from IBl H).
IBØ H -- IBl H	Intensity Bit Ø and 1, Background High	Background intensity values from logic unit register.
IF H	Intensity, Foreground High	Defines foreground intensity factor to logic unit for either plane zero (developed from IFØ H) or plane one (developed from IFl H).
IFØ H -- IFl H	Intensity Bit Ø and 1, Foreground High	Foreground intensity values from logic unit register.
IO/M	I/O or Memory	CP output defining access of I/O device (IO/M high) or memory (IO/M low).
LADl5 H	Latched Address Bit 15 High	Output from latched address mux during GDC access of bit map addressing defining plane selected (plane zero when LADl5 H is low, plane one when high).

Table 6-6 Video Logic Signal Description (Cont)

Signal Mnemonic	Signal Name	Description
LAD16 H	Latched Address Bit 16 High	Output from latched address mux during GDC access of bit map addressing defining which byte to be selected in text mode (low byte select when LAD16 H is low, high byte select when high, with LAD16 H value ignored in any mode other than text).
LB H	Low Byte High	Active high whenever any GDC bus high order bit (GAD8 H -- GAD15 H) is an active high.
LDA1 H -- LDA8 H	Latched Address Bit Ø through 8 High	Address values to be routed through map with value originating at GDC (SCROLL EN H low input to latched address mux) or scroll address counter (SCROLL EN H high).
LLB H	Load Low Byte High	Timing signals generator output enabling bit map output data to be loaded into bit map read back buffer when low.
MØ H -- M1 H	Mode Select Bit Ø and 1 High	Control outputs from logic unit register defining mode of operation to logic unit.
MADØ H -- MAD7 H	Memory Address Bit Ø through 7 High	Bit map address inputs for column and row addressing.
MDØ H -- MD7 H	Memory Data Output Bit Ø through 7 High	Bit map data output.
MDIØ H -- MDI7 H	Memory Data Input Ø through 7 High	Write data select circuit output to bit map from either GDC (GDØ L -- GD7 L), logic unit (WPØ L -- WP7 L), or bit map itself (MDØ H -- MD7 H).

Table 6-6 Video Logic Signal Description (Cont)

Signal Mnemonic	Signal Name	Description
MONITOR PRES L	Monitor Present Low	Status signal from monitor to CPU logic routed through monitor connector (J8).
PØ HB H	Plane Ø High Byte High	P/S converter devices output for single bit of plane Ø high order byte.
PØ LB H	Plane Ø Low Byte High	P/S converter devices output for single bit of plane Ø low order byte.
Pl HB H	Plane 1 High Byte High	P/S converter devices output for single bit of plane 1 high order byte.
Pl LB H	Plane 1 Low Byte High	P/S converter devices output for single bit of plane 1 low order byte.
PAT L	Pattern Low	Vector pattern based on pattern register data as multiplied by factor in pattern multiplier register.
PS L	Plane Select Low	Logic unit register value used during single plane write operations to define plane to be affected as plane Ø (PS L low) or plane 1 (PS L high).
RAH H	Row Address High Byte High	Timing signals generator output enabling row/column mux to pass low order address byte for row addressing (RAH H low), or high order address byte for column addressing (RAH H high).
RAM OE L	RAM Output Enable Low	Output from CP memory decoder enabling CP access of RAM.

Table 6-6 Video Logic Signal Description (Cont)

Signal Mnemonic	Signal Name	Description
RAS H	Row Address Strobe Low	Timing signals generator output coordinating activity during row addressing of bit map.
RD L	Read Low	Low output from CP when accessing either I/O device (IO/M high) or memory (IO/M low) for read.
RD BUF L	Read Buffer Low	Low input from CPU to read data from 8Ø85 RD buffer (also resets handshaking F/F).
RD GDC L	Read GDC Low	Low output from video access circuit when CPU/CP is to access GDC for read.
RD INIT CB ADDR L	Read to Initialize Character Address Low	Low output from video access circuit when CPU/CP wants to initialize character buffer address counter.
RD VOM L	Read VOM Low	Low output from video access logic when CPU/CP is to access VOM for read.
RDAØ H -- RDA7 H	Remote Data Bit Ø through 7 High	Data bus lines for transfer of data between video logic and CPU.
RMW H/L	Read-Modify-Write High and Low	Control signals true during RMW cycles.
ROM7 OE L -- ROM8 OE L	ROM 7 and 8 Output Enables Low	Low output from CP memory decode when CP is to access ROM (either ROM7 OE L low for 32K ROM or first 16K of ROM, or ROM8 OE L low when more than one ROM device is used and access is to be for data stored above first 16K of ROM).
RST 5.5	Reset 5.5	See G VS L.

Table 6-6 Video Logic Signal Description (Cont)

Signal Mnemonic	Signal Name	Description
RST 6.5	Reset 6.5	See SI.
RST 7.5	Reset 7.5	See G HS L.
RxD H	Receive Data High	Serial keyboard data input routed through the monitor connector (J8).
S BLANK L	Screen Blank Low	Control signal low during screen blank periods and developed from G BLK H high inverted input synchronized to RAH H.
SØ A H -- Sl A H	Select Mode Bit Ø and 1 A High	Mode select input to P/S converter device used to convert plane zero low order byte to serial data (PØ LB H).
SØ B H -- Sl B H	Select Mode Bit Ø and 1 B High	Mode select input to P/S converter device used to convert plane one low order byte to serial data (Pl LB H).
SØ C H -- Sl C H	Select Mode Bit Ø and 1 C High	Mode select input to P/S converter device used to convert plane zero high order byte to serial data (PØ HB H).
SØ D H -- Sl D H	Select Mode Bit Ø and 1 High	Mode select input to P/S converter device used to convert plane one high order byte to serial data (Pl HB H).
SADØ H -- SAD15 H	Scroll Address Bit Ø through 15 High	Address values input to bit map addressing from scroll address counter and used to develop bit map address values when GDC is not accessing the bit map.

Table 6-6 Video Logic Signal Description (Cont)

Signal Mnemonic	Signal Name	Description
SCROLL EN H/L	Scroll Enable High and Low	Control outputs from register one used to coordinate access of bit map, and with SCROLL EN H used with SEL SD H, with signals defining either DMA scroll of bit map (bit map data writen back into bit map without modification when both controls are true), GDC access of bit map (GDC modified data written into bit map when both controls are false), or logic unit access of bit map (logic unit modified data written to bit map when SCROLL EN H is high and SEL SD H is low).
SEL DAD L -- SEL LAD L	Select Display Address Low and Select Latched Address Low	Low outputs from DAD/LAD decoder only when SCROLL EN H is low (for GDC access of bit map), screen is blanked (S BLANK L low), with SEL LAD L low when read back mode is selected (SEL GDC H is high) and SEL DAD L low tied to RMW cycles (RMW L low) during other than read back mode (SEL GDC H low), with DAD/LAD outputs used at plane and byte mux to define select values for addressing the bit map, either EPS H and DAD 3 H (GDC access for other than read back mode, SEL DAD L low and SEL LAD L high), EPS H for both select values (GDC access for read back Mode, SEL DAD L high and SEL LAD L low), or EPS H and EBS H (access by other than GDC, both signals high).

Table 6-6 Video Logic Signal Description (Cont)

Signal Mnemonic	Signal Name	Description
SEL EXT LU H	Select External Logic Unit High	Control output from register zero enabling write data select mux to select logic unit data for output to the bit map in other than DMA scroll mode (SEL SD H low).
SEL GDC H	Select GDC High	Control output from register zero defining read back mode (SEL GDC H high) or other than read back mode (SEL GDC H low).
SEL LB L	Select Low Byte Low	Timing signals generator output to P/S converter selecting PØ HB H -- Pl HB H output to output map (SEL LB L high) or PØ LB H -- Pl LB H (SEL LB L low).
SEL SD H	Select Screen Data High	Control output from register one used to enable write data select circuit to output data to bit map from bit map (SEL SD H high), GDC (SEL SD H low and SEL EXT LU H low), or logic unit (SEL SD H low and SEL EXT LU H high).
SEL VPAT H	Select Vector Pattern High	Control output from register zero used to enable pattern select mux to output character (SEL VPAT H low) or vector (SEL VPAT H high) data to the logic unit.
SI	Serial Input	High input to CP whenever handshaking F/F has been set by CPU.
SP H	Select Plane High	Control output from logic unit register defining single plane (SP H high) or two-plane write tasks (SP H low).

Table 6-6 Video Logic Signal Description (Cont)

Signal Mnemonic	Signal Name	Description
STOP L	Stop Low	Low signal when END H is high and GDC is not seeking access to bus (BGD BEN L high), with STOP L used to clear timing signal generator to initial condition for start of new cycle.
SYNC H	Sync High	Control output from the timing signals generator used to synchronize blank signal generation.
TxD H	Transmit Data High	Serial keyboard data output routed through the monitor connector (J8).
VAØ H -- VA3 H	Video Address Bit Ø through 3 High	Address bits originating at CPU/CP and used to address VOM when VOM access by CPU/CP is enabled by EN VOM H low (VAØ H is also used for address input to GDC).
VA4 H -- VA7 H	Video Address Bit 4 through 7 High	Address bits originating at CPU/CP and used by video access to decode video logic I/O device to be enabled for read (VIO RD L low) or write (VIO WR L low).
VBØ H -- VB1 H	Video Blue Output Bit Ø and 1 High	Output map two-bit value to D/A CPU/CP blue.
VDBØ H -- VDB7 H	Video Data Bit Ø through 7 High	Data lines for transfer of data between video logic I/O devices (or VOM) and video access circuit.
VEC H/L	Vector Mode High and Ø Low	Control outputs from register defining vector mode (signals true) or text mode (signals false).
VGØ H -- VG1 H	Video Green Output Bit Ø and 1 High	Output map two-bit code to D/A CPU/CP green.

Table 6-6 Video Logic Signal Description (Cont)

Signal Mnemonic	Signal Name	Description
VID ACCESS L	Video Access Low	Low input to video access from CPU whenever CPU is to access video logic for read or write.
VIO RD L	Video I/O Read Low	Low to video I/O decode whenever CPU/CP is to access I/O device for read.
VIO WR L	Video I/O Write Low	Low to video I/O decode whenever CPU/CP is to access I/O device for write.
VMØ H -- VM1 H	Video Mono Output Bit Ø and 1 High	Output map two-bit code to D/A for mono.
VOMØ H -- VOM1 H	VOM Map Select Bit Ø and 1 High	Output from register zero defining which output map is to be addressed (mapØ -- map3) during video logic access of VOM.
VRØ H -- VR1 H	Video Red Output Bit Ø Ø and 1 High	Output map two-bit code to D/A for red.
WPØ L -- WP7 L	Write Pattern Ø through 7 Low	Data output from logic unit used as data for bit map when write data select circuit is enabled to pass logic unit inputs (SEL EXT LU H high and SEL SD H low).
WR L	Write Low	Low output from CP for write to I/O device (IO/M high) or memory (IO/M low).
WR BUF L	Write Buffer Low	Low input from CPU setting handshake F/F when CPU wants to write to CP.
WR CHAR BUF L	Write Character Buffer Low	Low output from video access for CPU/CP write to character buffer.
WR GDC L	Write GDC Low	Low output from video access for CPU/CP write to GDC.

Table 6-6 Video Logic Signal Description (Cont)

Signal Mnemonic	Signal Name	Description
WR HB SCROLL DA L	Write Scroll Display Address High Byte Low	Low output from video access for CPU/CP write of high byte data to scroll address counter.
WR LB SCROLL DA L	Write Scroll Display Address Low Byte Low	Low output from video access for CPU/CP write of low byte data to scroll address counter.
WR LU L	Write Logic Unit Low	Low output from video access for CPU/CP write to logic unit register.
WR MASK L	Write Mask Low	Low output from video access for CPU/CP write to write mask register.
WR PAT MULT L	Write Pattern Multiplier Low	Low output from video access for CPU/CP write to pattern multiplier register.
WR REGØ L	Write Register Ø Low	Low output from video access for CPU/CP write to register zero.
WR REGl L	Write Register 1 Low	Low output from video access for CPU/CP write to register one.
WR VOM L	Write VOM Low	Low output from video access for CPU/CP write to VOM.
WR VPAT L	Write Vector Pattern Low	Low output from video access for CPU/CP write to vector pattern register.
X1 -- X2	Clock Bit 1 and 2	Opposing phased clock inputs to CP.
85ADØ H -- 85AD7 H	8Ø85 Address/Data Bit Ø through 7 High	Data and low byte address lines (for address values to be latched into address latch).

Table 6-6 Video Logic Signal Description (Cont)

Signal Mnemonic	Signal Name	Description
85AD8 H -- 85AD13 H	8Ø85 Address/Data Bit 8 through 13 High	Address values output to CP ROM and RAM devices.
85AD14 H	8Ø85 Address/Data Bit 14 High	Address value used at CP memory decode to define enable o ROM7 (ROM7 OE L low) or ROM8 (ROM8 OE L low) and as most significant bit of ROM address.
85 IORD L	8Ø85 I/O Read Low	Low input to video access from CP R/W control when CP is to access I/O device for read.
85 IOWR L	8Ø85 I/O Write Low	Low input to video access from CP R/W control when CP is to access I/O dvice for write.
85LAØ H -- 85LA7 H	8Ø85 Latched Address Bit Ø through 7 High	Low order address for memory or I/O access by CP.
85RD BUF L	8Ø85 Read Buffer Low	Low output from video access when CP is to read data from 8Ø85 WR buffer input from CPU (also resets handshaking F/F).
85WR BUF L	8Ø85 Write Buffer Low	Low output from video access when CP is to write data to 8Ø85 RD buffer for CPU.
8Ø85 RDY L	8Ø85 Ready Low	Status signal output from CP to CPU.
8Ø85 RESET L	8Ø85 Reset Low	Reset input to CP from CPU.

Table 6-7 Video Logic Schematic References

Logic Board Circuit/Component	Schematic Reference Numbers	Page	Coordinate
Address latch	E1Ø3	9	C5
Ben and stop gates	E136,E137,E159	18	A4-A6/B3
Bit map memory	E141,E17Ø-E177	14	D1-D3
Blank F/F	E137,E157,E159	18	A1-A4
Blank I F/F	E116	18	A1
BS gate	E14Ø	18	C5
Buffer gates	E13Ø,E145	13	B5-C5
Character pattern address counter	E178	15	C7
Character pattern buffer	E185,E192	15	C5/D5
Clear F/F	E158,E159	18	B7
Counter clock gate	E77,E1Ø9	15	B7
CP	E1Ø1	9	A7-D7
CP gate	E1Ø9	1Ø	A5
CP memory decoder	E15Ø	9	B4
CP RAM	E1Ø2	9	A2
CP ROM 7	E1ØØ	9	C2
CP ROM 8	E131	9	C2
CP video data buffer	E1Ø8	1Ø	A3
CPU video data buffer	E1Ø7	1Ø	A6
CTØ	E187	18	D3
CT1	E188	18	C3
D blank buffer	E115	16	D4
DAD 3 generator	E77,E78,E93	13	C1-C3
DAD/LAD decoder	E136,E138	18	C1-C2
Divider	E167,E169	18	D5-D6
DMA buffer	E141,E179	13	B7
EPS/EBS generator	E16Ø	18	B3-B4
Erase F/F	E94,E121	18	B7
Gate decoder	E138	18	B2
GDC	E129	11	A8-D8
Handshaking F/F	E116	9	C7
HI/LO byte mux	E142,E143	13	C7-D7
Intensity select mux	E164	15	B7
J3	J3	17	A5
J8	J8	17	B5-D5
Latched address mux	E1Ø9,E114,E124,E125, E127	11	A5-C5
LB H generator	E78,E117,E141,E153, E154	13	A2-B2
Logic unit	E182,E183	15	C2-D2
Logic unit register	E163	15	B5
Mask enable gate	E93	14	C7
Mask select mux	E161,E162	14	C7-D7
Multiplier clock and load gates	E66,E72	12	B4
Mux select gate	E78,E14Ø	13	C7
Pattern multiplier counter	E65	12	B4

Table 6-7 Video Logic Schematic References (Cont)

Logic Board Circuit/Component	Schematic Reference Numbers	Page Coordinate
Pattern multiplier register	E64,E78	12 B5
Pattern register	E79	12 C2
Pattern select mux	E186,E19Ø	15 C4/D4
Plane and byte mux	E139	11 D4
PM gates	E94,E1Ø9	15 B2
P/S converters	E146,E147,E165,E166	16 A7-D7
P/S mode select buffer	E189	18 D2
P/S output mux	E129	16 D6
Read back buffer	E126,E144	13 A4/D4
Register Ø	E96,E191	16 B5-B6
Register 1	E122,E141	12 D4-D5
Register clock gate	E69	12 B2
RMW F/F	E119	18 A7
ROM ADDRESS CLOCK	E168	18 B6
Row/column mux	E12Ø,E128	11 B3-C3
R/W control	E117,E136	9 A6
S blank F/F	E157	18 B2
Scroll address counter	E11Ø-E113	A7-D7
Scroll/stop F/F	E137,E158,E159	18 C6-C8
Sync gates	E77,E83	17 B7/D7
Timing signal buffer	E148	18 B5
TMØ	E149	18 B5
VB input stage	E82,R1ØØ,R1Ø1	17 C7
VB output stage	E84,R98,R99,R1Ø2, R1Ø3,C45	17 C6
VG input stage	E82,R96,R97	17 C7
VG output stage	E84,R92-R95,C44	17 C6
Video address mux	E88,E1Ø4	1Ø C6-D6
Video I/O decoders	E76,E92,E117	1Ø C3/D3
Video RD/WR mux	E118	1Ø B6
VM input stage	E83,R1Ø6,R1Ø7	17 B7
VM output stage	E84,R1Ø4,R1Ø5,R1Ø8, R1Ø9,R112-R114,C46, C48,Q1	17 B6
VOM	E97,E98	16 A3/C3
VOM address select	E77,E95,E115	16 B5/C5/D4
VOM buffer	E99	16 B2
VOM read back buffer	E8Ø	16 B1
VR input stage	E81,R87,R88	17 D7
VR output stage	E84,R89-R91,R19Ø,C43	17 D6
Write data select mux	E18Ø,E181	14 A7-B7
Write mask latch	E156	14 D6
Y1	Y1,E167	18 C8
8Ø85 read buffer	E1Ø5	9 D4
8Ø85 write buffer	E1Ø6	9 D2

CHAPTER 7
LK201 KEYBOARD

7.1 GENERAL

The LK201 keyboard module (shaded area in Figure 7-1) is the user's interface to the terminal. The keyboard detects keystrokes, encodes them, and transmits and receives information to and from the CPU logic in the system box.

Communication between the keyboard and the CPU logic is full-duplex, serial, and asynchronous at 4800 bits-per-second (bps). The communication lines conform to EIA standard RS-423, which applies to imbalanced voltage interfaces.

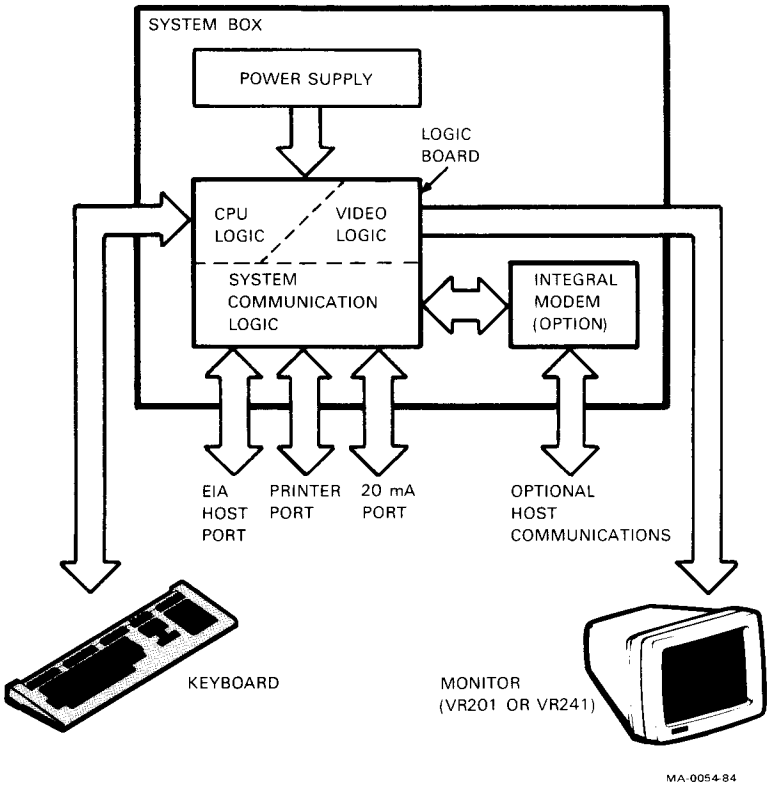


Figure 7-1 VT240-Series Terminal System Block Diagram

7.2 PHYSICAL DESCRIPTION

The keyboard used in the VT240 Series Terminal has 105 keys arranged in the following four groups (Figure 7-2).

- Main keypad (57 keys)
- Numeric keypad (18 keys)
- Special function keypad (20 keys)
- Editing keypad (10 keys)

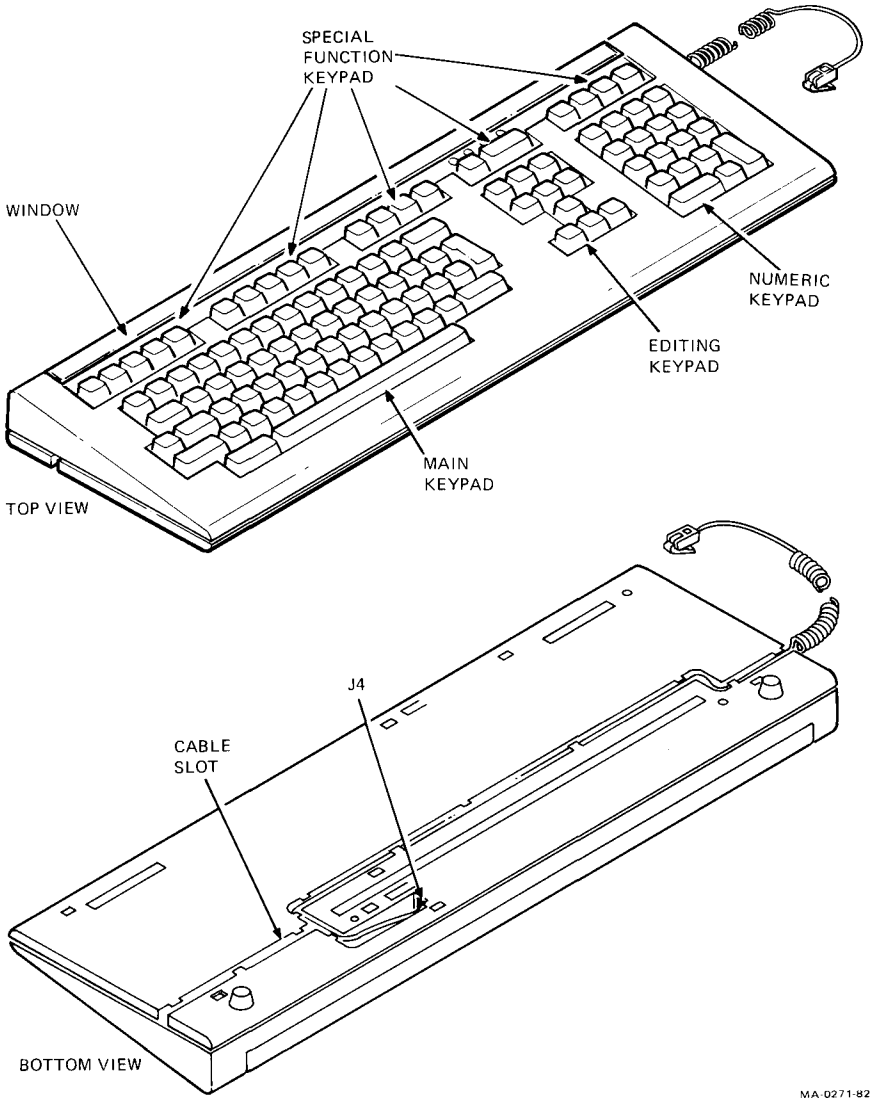


Figure 7-2 LK201 Keyboard

You can install the keycaps manually, but you need a special tool to remove them.

The keyboard circuitry is contained in a low profile cabinet that has a 30 mm nominal height from table top to home row. The keyboard case is made of two plastic shells that you can separate with a screwdriver. Nonslip plastic strips along the bottom prevent the keyboard from sliding on a table top. You can manually insert two feet in holes to raise the back edge of the keyboard.

You can lift a plastic window along the top edge above the special function keys to insert a user function label. The label, a thin paper strip, fits into the indented space and varies according to the application program.

A coiled cable (PN BCC01), with a four-pin modular connector on each end, connects the keyboard to the video monitor. The keyboard transmits four signals to the monitor, which pass unchanged to the system box via the video cable (Figure 7-3). The four signals are as follows.

- +12 V power to keyboard
- Ground to keyboard
- Serial out (transmit line from keyboard)
- Serial in (receive line to keyboard)

You can place the cable in a channel in the bottom case and the modular type telephone connector fits into jack J4. You can insert the cable in the channel on either side of the keyboard. Section 7.6 provides keyboard specifications.

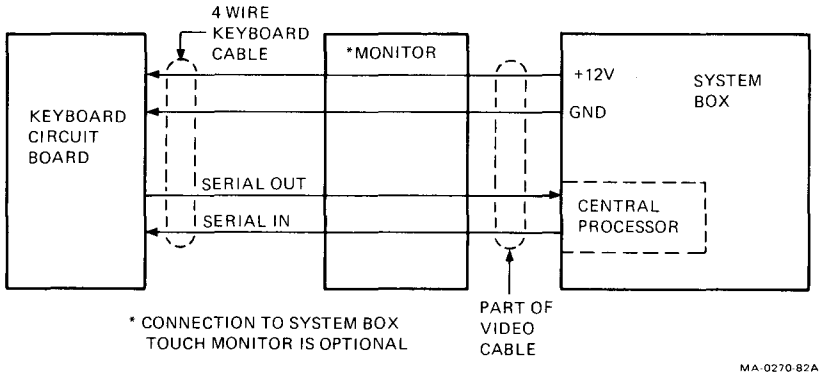


Figure 7-3 Keyboard Cable Connections

7.3 FUNCTIONAL DESCRIPTION

This section provides a functional description of the LK201 keyboard.

7.3.1 Keyboard Operation Overview

Figure 7-4 is a simplified block diagram of the keyboard circuitry. Everything except the block marked KEYBOARD SWITCH MATRIX is on the printed circuit board. This block represents the connections between the keyboard switches and the signals from the 8051 microprocessor.

The firmware in the 8051 eight-bit microprocessor controls the following three major keyboard operations at the same time.

1. Scans the keyboard to detect changes in the keyboard matrix

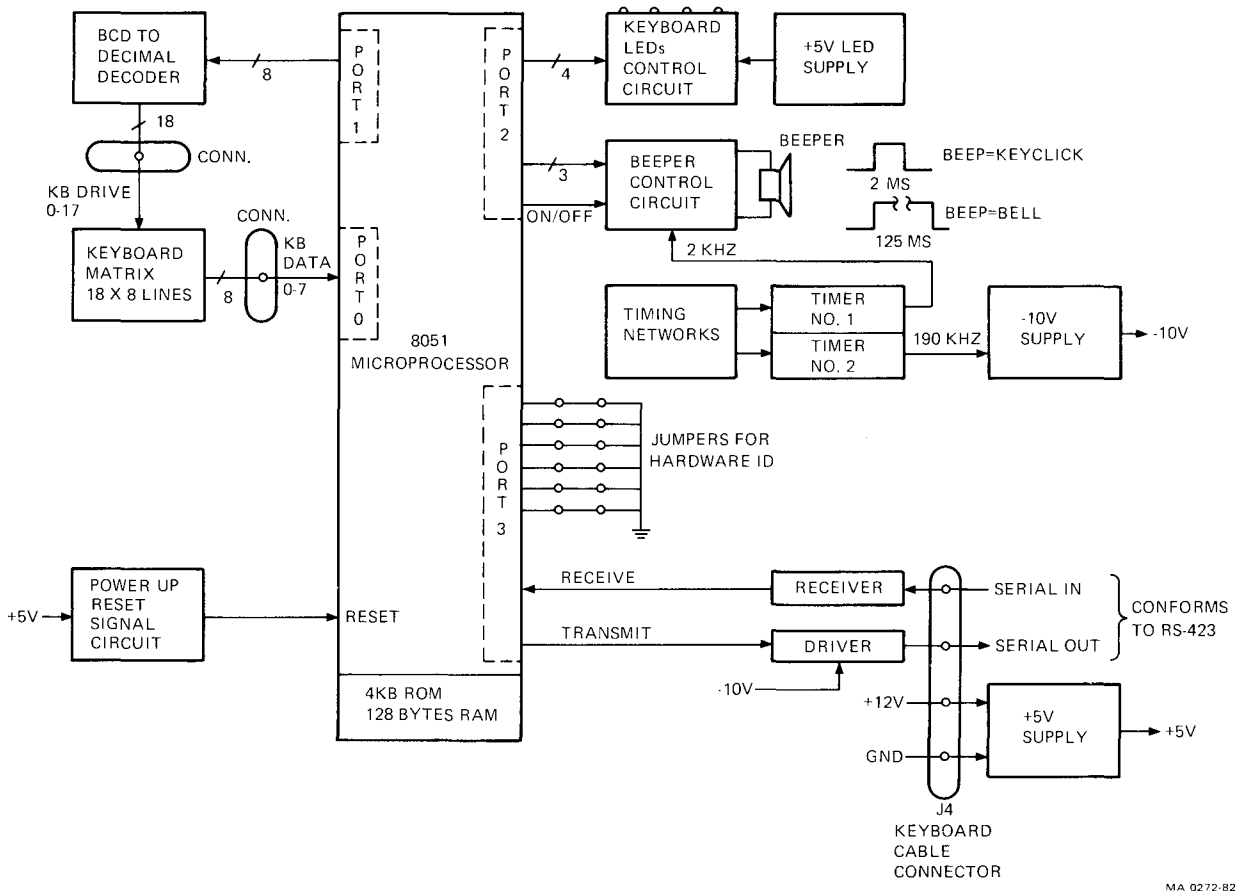


Figure 7-4 LK201 Keyboard Block Diagram

2. Transmits results of the keyboard scan to the CPU

3. Receives information from the CPU

7.3.1.1 Keyboard Scanning -- The keyboard switches are connected at the intersections of an 18 X 8 line matrix. This provides a fixed position identifier for each key.

The firmware scans the 18 line axis and detects a pressed or newly released key by reading the eight-line axis. The firmware then verifies the detected keystroke and changes this position information into an eight-bit code that is unique to that key.

7.3.1.2 Control of Audio Transducer and Indicators -- Two circuits control the audio transducer and the indicators. One circuit receives its inputs from the 8Ø51 and controls the transducer (beeper). A long beep represents the bell and a short beep represents the keyclick.

A separate circuit, controlled by a signal from the 8Ø51, controls each of the four indicators. The firmware, responding to commands received from the CPU, turns the indicators on or off.

7.3.2 Keyboard Firmware Functions

This section describes the keyboard firmware functions. The functions are divided into two categories: functions that cannot be changed by CPU instructions, and functions that can be changed by CPU instructions.

7.3.2.1 Functions Not Changed by CPU Instructions -- The following functions cannot be changed by instructions from the CPU.

Powerup test
Keycodes
Special codes

Power-Up Test
Upon power-up, the firmware performs a self-test in less than 7Ø ms. The test results are transmitted to the CPU in four bytes.

The keyboard indicators are lit during the self-test. The indicators blink once during the self-test routine. The indicators remain lit if the test is failed, but go off if the test is passed. The system module can also request a self-test at any time.

Keycodes
The keycodes represent fixed positions in the key switch matrix. The key associated with a particular matrix position is always represented by the same keycode.

Special Codes
There are 13 special codes transmitted by the keyboard. Four codes transmit the results of the power-up self-test. The other nine codes are status indicators or command acknowledgements.

7.3.2.2 Functions Changed by CPU Instructions -- The CPU can issue instructions to change some keyboard transmission characteristics and to control the keyboard indicators and beeper.

Upon completion of a successful power-up self-test, the firmware sets certain functions to predetermined conditions. These are referred to as default conditions. The conditions can be changed but they always come up to the default condition after a successful power-up self-test.

7.3.2.3 Firmware Functions Changed by CPU Instructions -- Certain firmware functions can be changed by commands (instructions) from the CPU. These commands are categorized as transmission commands and peripheral commands. Transmission commands contain a mode set command and an autorepeat rate set command. Peripheral commands contain a variety of commands. Refer to section 7.5.5.3 for more information on peripheral commands.

7.4 Detailed Keyboard Circuit Description

This section describes the keyboard circuit. Figure 7-4 shows the keyboard block diagram.

7.4.1 Keyboard Matrix Scanning

The key locations are arranged in an 18 X 8 line matrix. Each key switch is connected across a matrix intersection. This gives a fixed position for each key connected in the matrix. This matrix accommodates all 105 keys in the keyboard.

Figure 7-5 is a simplified block diagram of the matrix scanning circuit. Eight lines from PORT 1 of the 8051 microprocessor go to the binary coded decimal (BCD) inputs of two 74LS145 BCD-to-decimal decoders. Ten outputs from one decoder and eight outputs from the other decoder provide the drive lines for the matrix. These 18 lines are called KB DRIVE 0 -- 17.

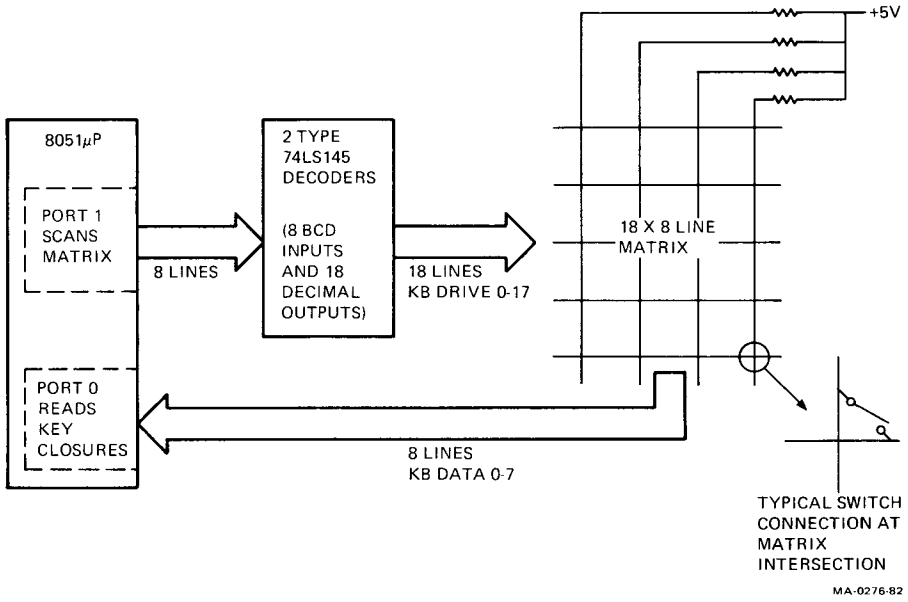


Figure 7-5 Matrix Scanning Block Diagram

The other axis of the matrix consists of eight lines tied to +5 V through pull-up resistors. These lines go to PORT Ø of the 8Ø51 microprocessor and are called KB DATA Ø -- 7.

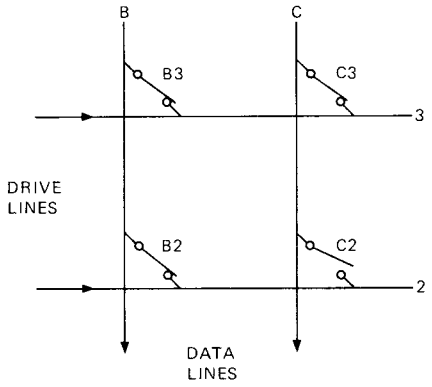
The 8Ø51 scans the 18 drive lines. Key closures are detected by reading the eight data lines. The complete matrix is scanned every 8.33 ms.

When a key closure is detected, it is scanned again to verify that it is really a key closure and not electrical noise.

Once the key closure is verified, the 8Ø51 firmware translates the position information into a key code and transmits it to the CPU. Transmission is handled by the Universal Asynchronous Receiver Transmitter (UART) in the 8Ø51.

A ghost key indication can occur when three of the four corners of a matrix rectangle are closed (Figure 7-6) causing what is known as a sneak path. The key positions in the matrix are arranged to avoid sneak paths. However, if a sneak path does occur, the firmware prevents the keycode for the key that caused the sneak path to be transmitted until one of the involved keys is released. This prevents transmission of ghost keys entirely.

Table 7-1 shows the keyboard matrix on the LK201-AA (American) keyboard. Keycap designations are listed for reference only; you can compare them to Figure 7-7 (A and B).



1. CONDITIONS ARE: SWITCHES B2, B3, AND C3 CLOSED, SWITCH C2 OPEN; LINE 2 IS BEING DRIVEN AND LINE C IS BEING READ.

2. INTERSECTION C2 IS BEING LOOKED AT. IT SHOULD NOT SHOW A KEY CLOSURE BECAUSE SWITCH C2 IS OPEN.

3. HOWEVER A SNEAK PATH IS PRESENT FROM LINE 2 THROUGH SWITCHES B2, B3, AND C3 TO LINE C. A GHOST KEY IS READ AT INTERSECTION C2.

MA-0273-82

Figure 7-6 Example of Ghost Key Generation

Table 7-1 Keyboard Matrix

Refer to Figure 7 (A and B). It shows the international matrix for the LK201 keyboard. The legends provided are from the LK201 keyboard and are provided for convenience only.

KB Drive	KB DATA 7	6	5	4	3	2	1	Ø
17	Reserved	F19	Reserved	F20	PF4	N (Note 1)	N,	ENTER
		G22		G23	E23	D23	C23	A23
16	F18	PF3	Reserved	N9	↓	N6	N3	N.
	G21	E22		D22	B17	C22	B22	A22
15	F17	PF2	Reserved	N8	N5	→	N2	NØ (See
	G20	E21		D21	C21	B18	B21	Note 2
14	PF1	NEXT SCREEN	REMOVE	↑	N7	N4	N1	NØ
	E20	D18	E18	C17	D20	C20	B20	A20
13	INSERT HERE	-	D0	PREV SCREEN	{ [	" '	Reserved	Reserved
	E17	E11	G16	D17	D11	C11		

NOTES

1. Note that NØ -- N9, N_, N,, refer to the numeric keypad.

2. NØ of the numeric keypad can be divided into two keys. Normally only the NØ keyswitch is implemented as a double size key.

3. The **RETURN** key also canb e divided into two keys. The one that is decoded as return is the **RETURN** (C13) key.

Table 7-1 Keyboard Matrix (Cont)

KB Drive	KB DATA 7	6	5	4	3	2	1	Ø
12	FIND	+ = E16	HELP E12	SELECT G15	}] D16	RETURN D12	 C13	\ B16
11	ADDTNL OPTIONS G14	X (delete) E13	Reserved	) Ø E1Ø	P D1Ø	See Note 3	: ; C1Ø	? / B1Ø
1Ø	Reserved	F12 G12	Reserved	F13 G13	(9 E09	O D09	L C09	. B09
9	Reserved	F11 G11	Reserved	Reserved	* 8 E08	I D08	K C08	. B08
8	Reserved	MAIN SCREEN GØ8	Reserved	EXIT GØ9	& 7 E07	U D07	J C07	M B07
7	Reserved	CANCEL GØ7	Reserved	RESUME GØ6	^ 6 E06	Y D06	H C06	N B06
6	Reserved	Reserved	Reserved	INTER-RUPT GØ5	% 5 E05	T D05	G C05	B B05
5	SETUP GØ2	F5 GØ3	Reserved	$ 4 E04	R D04	F C04	V B04	SPACE AØ1-AØ9

Table 7-1 Keyboard Matrix (Cont)

KB Drive	KB DATA 7	6	5	4	3	2	1	Ø
4	Reserved	PRINT SCREEN GØØ	Reserved	BREAK GØ1	# 3 EØ3	E DØ3	D CØ3	C BØ3
3	HOLD SCREEN G99	@ 2 EØ2	Reserved	TAB DØØ	W DØ2	S CØ2	X BØ2	> < BØØ
2	Reserved	Reserved	Reserved	~ EØØ	! 1 EØ1	Q CØ1	A BØ1	Z
1	CTRL C99	LOCK CØØ	COMPOSE A99	Reserved				
Ø	SHIFT B99,B11							

NOTES

1. Note that NØ -- N9, N_, N,, refer to the numeric keypad.

2. NØ of the numeric keypad can be divided into two keys. Normally only the NØ keyswitch is implemented as a double size key.

3. The **RETURN** key also canb e divided into two keys. The one that is decoded as return is the **RETURN** (C13) key.

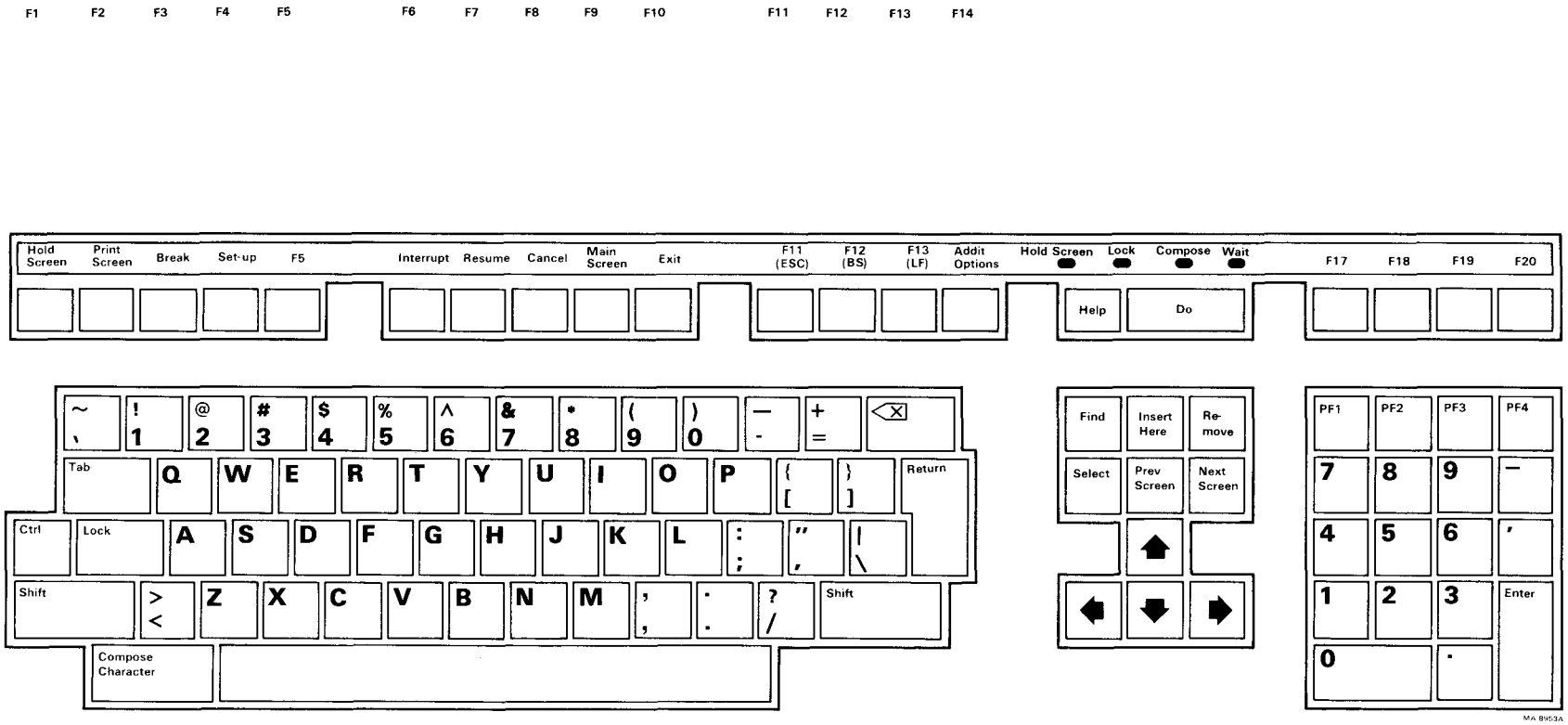
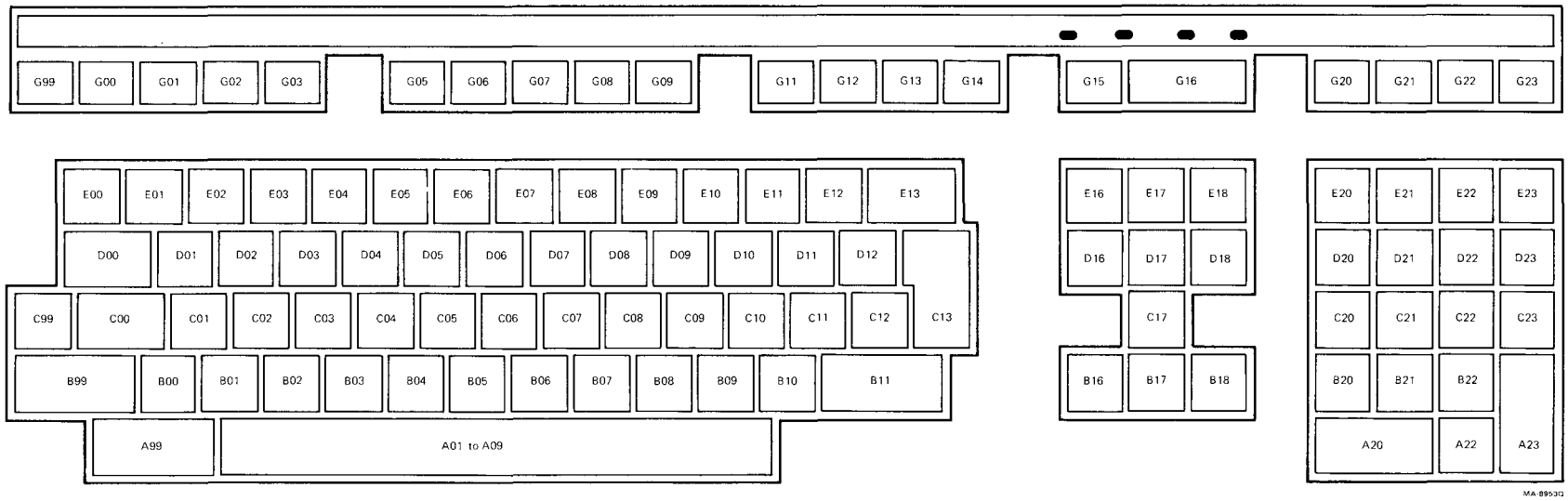


Figure 7-7A LK201-AA Keyboard Layout



NOTE: THE GRAPHIC CHARACTERS ARE SHOWN FOR ILLUSTRATION PURPOSES ONLY AND ARE NOT MEANT TO ASSIGN KEYCAP USAGE OR LEGENDS.

Figure 7-7B LK201-AA Keyboard Layout

7.4.2 Audio Transducer Control Circuit

Figure 7-8 shows the audio transducer or beeper control circuit. The beeper is driven by a transistor whose base is connected to a 2 kHz square wave from a 556 timer IC. This signal is biased by a network of four type 74LSØ5 open collector inverters. The 8Ø51 microprocessor controls all four inverters via the firmware. The on/off inverter connects directly to the transistor base. When the 8Ø51 puts a high on the on/off inverter input, its output goes low and removes the 2 kHz square wave from the transistor base. This cuts off the transistor and disables the beeper.

To turn on the beeper, the 8Ø51 puts a low on the ON/OFF inverter input. Its output goes high and allows the 2 kHz signal to reach the transistor base; this turns on the beeper. The firmware generates a keyclick (on for 2 ms) or a bell tone (on for 125 ms). The 8Ø51 sets up the three level control inverters by putting one of eight binary combinations on the inverter inputs. All highs give the softest sound and all lows give the loudest sound.

The firmware controls the keyclick and the bell tone independently. The bell tone is sounded only upon request from the system control processor. The keyclick is sounded (unless disabled) under the following conditions.

- When a key is pressed
- When a metronome code is sent
- When a command to sound the keyclick is received from the system control processor

7.4.3 Indicator (LED) Control Circuit

Figure 7-9 shows the LED indicator control circuit.

The control signal for each LED comes from PORT 2 of the 8Ø51 to the input of a type 74LSØ5 open collector inverter. The inverter output goes to the LED cathode; its anode is connected to +5 V. A separate +5 V source relieves the LED's load on the main +5 V supply.

A low signal from the 8Ø51 drives the inverter output high, which cuts off the LED. A high signal from the 8Ø51 drives the inverter output low. This provides a path to ground from the +5 V through the LED. The LED then turns on.

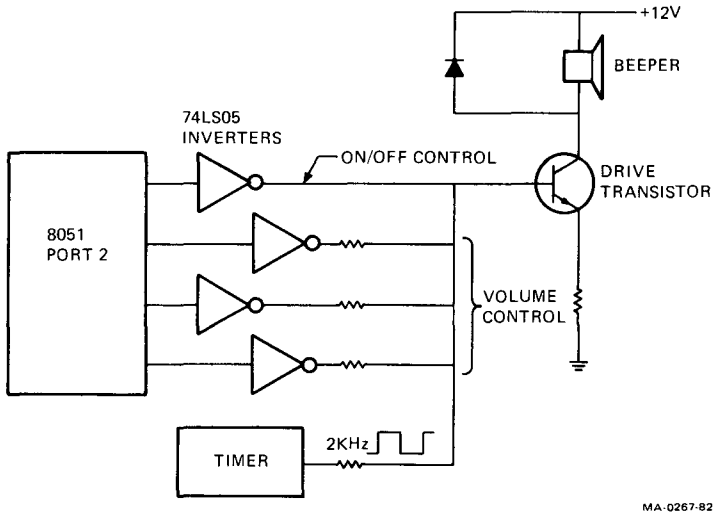


Figure 7-8 Beeper Control Circuit

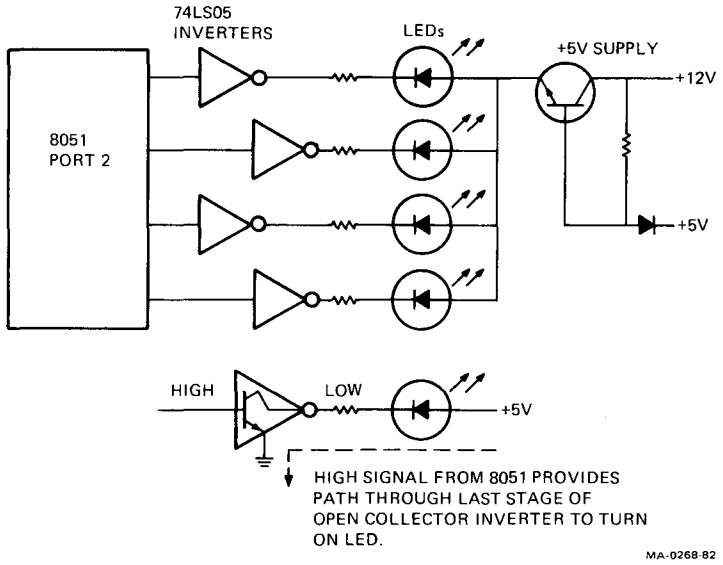


Figure 7-9 Indicator (LED) Control Circuit

7.4.4 Keyboard Communication

This section describe the keyboard communication.

7.4.4.1 Keyboard Transmit Mode -- The keyboard codes and a few other special codes are transmitted via a serial line output in PORT 3 of the 8051. The transmitted signal goes from the 8051 to a driver, through the keyboard cable, monitor, and video cable to the CPU. A UART within the 8051 controls the transmission.

Transmitted characters conform to a specific format. Each character is 10 bits long. The first bit is the start bit. It is always a logical zero (space). The next eight bits represent the encoded data. The last bit is the stop bit. It is always a logical one (mark). Figure 7-10 shows the character format.

7.4.4.2 Keyboard Receive Mode -- The firmware contains features that can be enabled by commands from the CPU. There are two categories of features: one sets keyboard transmission characteristics and the other controls keyboard peripherals. A peripheral command covers indicator control, bell and keyclick loudness, keyboard ID code, and reinstate keyboard. The commands come from the CPU and pass through the video cable, monitor, and keyboard cable to the receiver and into the 8051 via PORT 3. The commands go to the UART in the 8051.

Received characters conform to the same 10-bit format used for transmitted characters. The eight data bits are arranged in a specified protocol, depending on the command type.

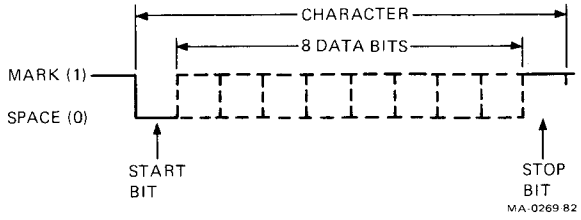


Figure 7-10 Keyboard Transmit and Receive Character Format

7.4.5 Reset Signal for 8051 Microprocessor

Whenever the system is turned on, the 8051 microprocessor in the keyboard must be reset. This allows the 8051 to start operating.

The reset signal generator is active only during powerup. The input is +5 V. The output is connected to the RESET input of the 8051. When power is turned on, the +5 voltage starts to rise from zero. The reset signal circuit output follows it and drops off when a steady state of +5 V is reached. This circuit holds the 8051 RESET input high (+3.5 V to +5 V) long enough to enable the reset action in the 8051. This action occurs only during powerup.

7.4.6 Hardware Keyboard Identification (ID)

At powerup, the keyboard performs a self-test and sends the results to the CPU. One piece of information to be sent is the keyboard hardware ID, which is read from hardwired jumpers.

There are six jumpers. Each jumper line goes from an input in PORT 3 of the 8051 to ground. All jumpers are installed so the keyboard hardware ID is zero.

7.4.7 Voltage Supplies

The only voltage sent to the keyboard is +12 V. However, +5 V and -10 V are also required. These voltages are derived from the +12 V.

There is a +5 V supply that handles most of the requirements for this voltage. The four keyboard LEDs have their own +5 V supply. A -10 V supply provides voltage for the driver in the serial out line.

7.5 KEYBOARD PROGRAMMING

This section describes the functions that the keyboard performs under system central processor control. This section also describes keyboard programming machine language, but does not describe high level user programming.

7.5.1 Keyboard Layout and Key Identification

Each keyboard key has a unique location. Each location is scanned, and when closure or release is detected, the location is verified. This is then decoded to an eight-bit keycode. Figure 7-7 shows the keyswitch locations. Table 7-2 shows the 14 functional divisions of the keyboard. Table 7-3 shows the divisions, keycaps, and keycodes.

Table 7-2 Keyboard Functional Divisions

Division	Description	Representation
1	48 graphic keys Spacebar	ØØØ1
2	Numeric keypad	ØØ1Ø
3	Delete character (E12)	ØØ11
4	Return (C13) Tab (DØØ)	Ø1ØØ
5	Lock (CØØ) Compose (A99)	Ø1Ø1
6	Shift (B99 and B11) CTRL (C99)	Ø11Ø
7	Horizontal cursors (B16 and B18)	Ø111
8	Vertical cursors (B17 and C17)	1ØØØ
9	Six keys directly above the cursor keys (D16 -- D18 and E16 -- E18)	1ØØ1
1Ø	Function keys (G99 -- GØ3)	1Ø1Ø
11	Function keys (GØ5 -- GO9)	1Ø11
12	Function keys (G11 -- G14)	11ØØ
13	Function keys (G15 -- G16)	11Ø1
14	Function keys (G2Ø -- G23)	1110

Table 7-3 Keycode Translation Table

Division	Position	Keycap	Keycode Decimal	Keycode Hexidecimal
Function Keys				
10	G99	Hold screen	086	56
	G00	Print screen	087	57
	G01	Break	088	58
	G02	Setup	089	59
	G03	F5	090	5A
	--	Reserved	091--098	5B--62
11		Reserved	099	63
	G05	Interrupt	100	64
	G06	Resume	101	65
	G07	Cancel	102	66
	G08	Main screen	103	67
	G09	Exit	104	68
	--	Reserved	105--110	69--6E
12	--	Reserved	111	6F
	--	Reserved	112	70
	G11	F11 (ESC)	113	71
	G12	F12 (BS)	114	72
	G13	F13 (LF)	115	73
	G14	Additional Options	116	74
		Reserved	117--122	75--7A
13	--	Reserved	123	7B
	G15	Help	124	7C
	G16	D0	125	7D
14	--	Reserved	126--127	7E--7F
	G20	F17	128	80
	G21	F18	129	81
	G22	F19	130	82
	G23	F20	131	83
	--	Reserved	132--135	84--87
6 Basic Editing Keys				
9	--	Reserved	136--137	88--89
	E16	Find	138	8A
	E17	Insert here	139	8B
	E18	Remove	140	8C
	D16	Select	141	8D
	D17	Previous screen	142	8E
	D18	Next screen	143	8F
	--	Reserved	144	90

Table 7-3 Keycode Translation Table (Cont)

Division	Position	Keycap	Keycode Decimal	Keycode Hexidecimal
Keypad				
2	--	Reserved	145	91
	A20	0	146	92
	--	Reserved	147	93
	A22	.	148	94
	A23	Enter	149	95
	B20	1	150	96
	B21	2	151	97
	B22	3	152	98
	C20	4	153	99
	C21	5	154	9A
	C22	6	155	9B
	C23	,	156	9C
	D20	7	157	9D
	D21	8	158	9E
	D22	9	159	9F
	D23	--	160	A0
	E20	PF1	161	A1
	E21	PF2	162	A2
	E22	PF3	163	A3
	E23	PF4	164	A4
		Reserved	165	A5
Cursor Keys				
7	--	Reserved	166	A6
	B16	Left	167	A7
	B18	Right	168	A8
8	B17	Down	169	A9
	C17	Up	170	AA
	--	Reserved	171--172	AB--AC
Shift, Lock CTRL, A99, and A10				
6	--	Reserved	173	AD
	B99,B11	Shift	174	AE
	C99	CTRL	175	AF
5	C00	Lock	176	B0
	A99	Compose	177	B1
	--	Reserved	178	B2

Table 7-3 Keycode Translation Table (Cont)

Division	Position	Keycap	Keycode Decimal	Keycode Hexidecimal
Special Codes				
		All ups	179	B3
		Metronome	180	B4
		Output error	181	B5
		Input error	182	B6
		KBD Locked acknowledge	183	B7
		Test mode acknowledge	184	B8
		Prefix to keys down	185	B9
		Mode change acknowledge	186	BA
		Reserved	187	BB
Delete				
3	E13	Delete (X)	188	BC
Return and Tab				
4	C13	Return	189	BD
	D00	Tab	190	BE
48 Graphics Keys and Spacebar				
1	E00	Tilde	191	BF
	E01	!1	192	D0
	D01	Q	193	C1
	C01	A	194	C2
	B01	Z	195	C3
	--	Reserved	196	C4
	E02	@2	197	C5
	D02	W	198	C6
	C02	S	199	C7
	B02	X	200	C8
	B00	><	201	C9
	--	Reserved	202	CA
	E03	#3	203	CB
	D03	E	204	CC
	C03	D	205	CD
	B03	C	206	CE
	--	Reserved	207	CF
	E04	$4	208	D0

Table 7-3 Keycode Translation Table (Cont)

Division	Position	Keycap	Keycode Decimal	Keycode Hexidecimal
	D04	R	209	D1
	C04	F	210	D2
	C04	V	211	D3
	A01--A09	Space	212	D4
	--	Reserved	213	D5
	E05	%5	214	D6
	D05	T	215	D7
	C05	G	216	D8
	B05	B	217	D9
	--	Reserved	218	DA
	E06	^6	219	DB
	D06	Y	220	DC
	C06	H	221	DD
	B06	N	222	DE
1	--	Reserved	223	DF
	E07	&7	224	E0
	D07	U	225	E1
	C07	J	226	E2
	B07	M	227	E3
	--	Reserved	228	E4
	C08	*8	229	E5
	D08	I	230	E6
	C08	K	231	E7
	B08	' '	232	E8
	--	Reserved	233	E9
	E09	(9	234	EA
	D09	0	235	EB
	C09	L	236	EC
	B09	. .	237	ED
	--	Reserved	238	EE
	E10	)0	239	EF
	D10	P	240	F0
	--	Reserved	241	F1
	C10	: ;	242	F2
	B10	? /	243	F3
	--	Reserved	244	F4
	E12	+ =	245	F5
	D12	}]	246	F6
	C12	| \	247	F7
	--	Reserved	248	F8

Table 7-3 Keycode Translation Table (Cont)

Division	Position	Keycap	Keycode Decimal	Keycode Hexidecimal
	E11	_ -	249	F9
	D11	{ [	250	FA
	C11	. ,	251	FB
	--	Reserved	252-255	FC-FF

NOTE
The legends under "keycap" are taken from the keycap legends of the LK201-AA (American).

Keycodes 00 through 64 are reserved. Keycodes 65 through 85 are unused.

7.5.2 Modes

This section describes the function of the keycode transmission modes. The mode set command allows any one of the 14 keyboard divisions to be set to any one of the following three modes. (Refer to section 7.5.7 for division defaults.)

- Down Only Mode -- The keyboard transmits a keycode when the key is pressed.
- Autorepeat Down -- The keyboard transmits a keycode when the key is first pressed. If the key is held down past the specified timeout period (usually 300 to 500 ms), a fixed metronome code is sent at the specified rate until the key is released.
- Down/up -- The keyboard transmits a keycode when the key is pressed and an "up code" when the key is released. If any other DOWN/UP keys are pressed, the "up code" is a repeat of the "down code." If no other DOWN/UP keys are pressed, the keyboard sends an ALL UPS code.

7.5.2.1 Special Considerations Regarding Autorepeat -- The autorepeat rate set command allows the following changes in the autorepeat mode.

- Autorepeat rate buffer association -- The buffer association can be changed for the selected keyboard division.
- The timeout and interval values can be changed in any one of the four autorepeat rate buffers.

- If multiple autorepeating keys are held down, metronome codes are still generated. The metronome codes apply to the keycode transmitted most recently. If the last key pressed is released, and any other keys are still down, the keycodes for those keys are retransmitted.

Example 1

The **a** key is held down. This produces the following transmission.

a metronome metronome

Now the **b** key is pressed. This produces the following transmission.

a metronome metronome b metronome metronome

Now the **b** key is released. This produces the following transmission.

a metronome metronome b metronome metronome a metronome met. . .

While metronome codes are being generated for an autorepeating key, a nonautorepeating keycode or special code may be transmitted. The keyboard transmits this special code instead of the next metronome code, and then returns to the autorepeated code. The keycode to be autorepeated is always the last byte transmitted.

Example 2

The **a** key is held down. This produces the following transmission.

a metronome metronome

Now the **SHIFT** key is pressed. This produces the following transmission.

a metronome metronome shift a metronome

Now the **SHIFT** key is released. This produces the following transmission.

a metronome metronome shift a metronome ALL UPS a metronome. . .

- If an autorepeating key is not to autorepeat (**CNTL C** for example), the system module must issue a temporary inhibit autorepeat command. This halts the transmission of any metronome codes or keyclicks for that key only. Metronome codes continue when another key is pressed. The command must be issued after the keycode for the autorepeating key is received.

- Autorepeat can be enabled and disabled independently of the division settings by using the enable/disable autorepeat commands. These commands apply to all keys on the keyboard. When autorepeat is disabled, internally the keyboard continues to autorepeat characters. However, it does not transmit metronome codes or keyclicks. When autorepeat is enabled, the keyboard transmits the metronome codes from the point they were before autorepeat was disabled. This may be within either the timeout or interval period, depending upon the time elapsed since the key was pressed.

- If the keyboard receives a request to change a division mode to autorepeat while a key is pressed, the keyboard makes the change immediately. After the specified timeout period, the keyboard transmits metronome codes for the pressed key. In place of the first metronome code, the keyboard transmits the keycode of the autorepeating key.

All autorepeating division modes can be changed to only down with one command. This and other autorepeat commands are grouped with the peripheral commands (refer to 6.5.5.3).

7.5.2.2 Special Considerations Regarding Down/Up Mode -- If two DOWN/UP keys are released simultaneously (within the same scan), and there are no other DOWN/UP keys down on the keyboard, only one ALL UPS code is generated.

7.5.2.3 Autorepeat Rates -- There are four buffers in the keyboard to store autorepeat rates. They are numbered zero through three. Each buffer stores the following two values. These values can be changed by the system module.

The timeout value
The interval value

The timeout value is the amount of time between the detection of a down key and the transmission of the first metronome code (defaults range from 300 to 500 ms). The interval value is the number of metronome codes per second (defaults to 30).

Each division is associated with one of the four buffers. Rates are taken from the associated buffer each time the autorepeat timers are loaded. This buffer-to-division association can be changed by the system module, or left to default.

7.5.3 Keyboard Peripherals

This section describes the peripherals available on the keyboard. The keyclick, bell, and LEDs are all considered keyboard peripherals. Refer to section 7.5.5.3 for information on system module control over these peripherals.

7.5.3.1 Audio -- The keyclick is a 2 ms beep and the bell is a 125 ms beep. The bell is sounded only upon request from the system module. The keyclick (if not disabled by the system module) sounds under the following three conditions.

When a key is pressed
When a metronome code is sent
When the system module receives a sound keyclick command

If either the **B11** or **B99** keys (the left and right **SHIFT** keys on the LK201) or the **C99** key (the **CNTL** key on the LK201) are pressed, the keyclick is not generated. However, if a command is sent from the system module to enable the keyclick on the **C99** key, the keyclick is generated (refer to section 7.5.5.3). Figure 7-7 shows the positions of these keys.

The keyclick or bell (or both) may be disabled. When the keyclick or bell is disabled, it does not sound. If the system module requests sound (refer to section 7.5.5.3) the keyclick or the bell does not sound.

Both the keyclick and bell may be independently set to one of the following eight volume levels.

000 -- highest
001
010 -- default
011
100
101
110
111 -- lowest

7.5.3.2 Indicators (LEDs) -- The system module normally transmits indicator control commands. However the following are exceptions.

- Upon powerup, the keyboard turns all LEDs off.
- After receiving the inhibit transmission command, the keyboard turns on the keyboard-locked LED. The LED is turned off after the keyboard receives a resume transmission command.

7.5.4 Keyboard-to-System Module Protocol

This section describes the keyboard-to-system module protocol.

7.5.4.1 Keycode Transmission -- The keyboard transmits single byte keycodes that reflect the keyboard matrix status. The eight-bit codes above 6410 are used for keycodes. Every key is identified by a unique keycode. There are no special codes for shifted or control keys.

Refer to Figure 7-7 and Tables 7-1 and 7-2 for complete keycode matrix translation table information.

7.5.4.2 Special Code Transmission -- There are 13 special codes. Nine codes have values above 6410 and four codes have values below.

The following nine special codes have values above 6410 (keycode value range).

ALL UPS	Keycode 179 (decimal), B3 (hexidecimal)
METRONOME CODE	Keycode 180 (decimal), B4 (hexidecimal)
OUTPUT ERROR	keycode 181 (decimal), B5 (hexidecimal)
INPUT ERROR	Keycode 182 (decimal), B6 (hexidecimal)
KBD LOCKED ACK	Keycode 183 (decimal), B7 (hexidecimal)
TEST MODE ACK	Keycode 184 (decimal), B8 (hexidecimal)
PREFIX TO KEYS DOWN	Keycode 185 (decimal), B9 (hexidecimal)
MODE CHANGE ACK	Keycode 186 (decimla), BA (hexidecimal)
RESERVED	Keycode 127 (decimal), 7F (hexidecimal)

ALL UPS -- indicates to the system module that a **DOWN/UP MODE** key was just released and no other **DOWN/UP** keys are pressed.

METRONOME CODE -- indicates to the system module that an interval has passed, a keyclick has been generated, and the last key received by the system module is still pressed.

OUTPUT ERROR -- indicates an output buffer overflow to the system module. The overflow occurred after receiving a keyboard inhibit command from the system module, and some keystrokes may be lost.

INPUT ERROR CODE -- indicates to the system module that the keyboard received a meaningless command, too many parameters, or too few parameters.

KEYBOARD LOCKED CONFIRMATION -- indicates to the system module that the keyboard received an inhibit transmission command (refer to section 7.5.5.3).

TEST MODE ACKNOWLEDGE -- indicates that the keyboard has entered test mode. This is a special mode used during the production test. If the system module receives this acknowledgement, it sends 8Ø hexidecimal. This terminates the test mode and jumps to powerup.

PREFIX TO KEYS DOWN -- indicates that the next byte is a keycode for a key already down in a division which has been changed to down/up (refer to section 7.5.5.4).

MODE CHANGE ACKNOWLEDGE -- indicates that the keyboard has received and processed a mode change command (refer to section 7.5.5.4).

RESERVED -- keycode 7F is reserved for internal use.

The following four special codes have values below the 641Ø range.

KEYBOARD ID (firmware)	Keycode Ø1 (decimal), Ø1 (hexidecimal)
KEYBOARD ID (hardware)	Keycode ØØ (decimal), ØØ (hexidecimal)
KEY DOWN ON POWER UP ERROR CODE	Keycode 61 (decimal), 3D (hexidecimal)
POWER UP SELF-TEST ERROR CODE	Keycode 62 (decimal), 3E (hexidecimal)

KEYBOARD ID -- is a two byte identification code, transmitted after the power-up self-test (refer to section 7.5.4.3). It is also sent on request from the system module (refer to section 7.5.5.3).

KEY DOWN ON POWER UP ERROR CODE -- indicates that a key was pressed on power up.

POWER UP SELF-TEST ERROR CODE -- indicates to the system module that the ROM or RAM self-test of the system module failed (refer to section 7.5.4.3).

7.5.4.3 Power Up Transmission -- Upon powerup, the keyboard performs a self-test in less than 70 ms, then transmits the self-test results to the system module in 4 bytes.

Byte 1	KBID (firmware) -- This is the keyboard identification (ID) stored in the firmware
Byte 2	KBID (hardware) -- This is the keyboard ID read from hardware jumpers
Byte 3	ERROR -- Two error codes indicate either the failure of the ROM or RAM self-test within the processor (3E hexidecimal), or a keydown on powerup (3D hexidecimal). No error is indicated by 00.
Byte 4	KEYCODE -- This byte contains the first keycode detected if there was a key pressed on powerup. No error is indicated by 00.

If the ROM self-test (CHECKSUM) fails and the error is critical, the keyboard is unable to transmit. Noncritical errors let the keyboard continue operating.

If the keyboard finds a key pressed on the first scan, it continues to look for an ALL UPS condition. The keyboard sends the corrected four-byte power-up sequence when the pressed key is released. This avoids a fatal error condition if a key is pressed by mistake while powering up.

The keyboard LEDs are lit during the power-up self-test. If the self-test passes, the keyboard turns the LEDs off. If a bell is selected on powerup, the system module can transmit a sound bell command to the keyboard. However, this should not be done until the system module receives the last byte of the four-byte sequence. The request for self-test tests the serial line and system module connection. The power-up self-test takes 70 ms or less.

The system module can request a jump to powerup at any time. This causes the LEDs on the keyboard to blink on and off (for the power-up self-test).

7.5.5 System Module to Keyboard Protocol

The system module controls both the peripherals associated with the keyboard and the keyboard transmit characteristics. Figure 7-11 shows the protocol for command and parameter transmission from the system module to the keyboard.

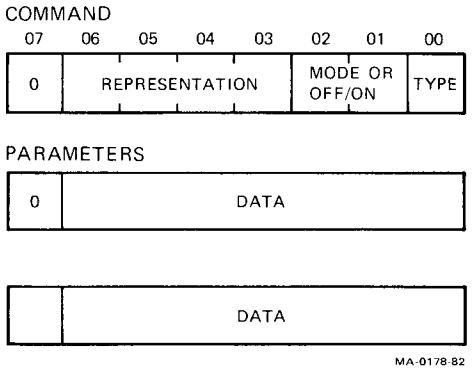


Figure 7-11 System Module to Keyboard Protocol

7.5.5.1 Commands -- There are two kinds of commands, commands that control keyboard transmission characteristics and commands that control keyboard peripherals. The low bit of the command is the TYPE flag. The TYPE flag is clear if the command is a transmission command, and set if the command is a peripheral command.

Transmission Commands	**Peripheral Commands**
Mode set	Flow control
Autorepeat rate set	Indicator
	Audio
	Keyboard ID
	Reinitiate keyboard
	Some autorepeat control
	Jump to test mode
	Reinstate defaults

The high order bit of every command is the PARAMS flag. If there are any parameters to follow, the PARAMS flag is clear. If there are no parameters to follow, the PARAMS flag is set.

7.5.5.2 Parameters -- The high order bit of every parameter is the PARAMS flag. This flag is clear if there are parameters to follow, and set on the last parameter. The remaining seven bits of the parameter are for data.

7.5.5.3 Peripheral Commands -- The following two commands can turn the data flow from the keyboard off and on.

- Inhibit Keyboard Transmission -- This command shuts off or locks the keyboard and turns on the keyboard locked LED. After receiving the inhibit command, the keyboard sends a special command to the system central processor. If the system central processor receives this code without requesting it, this indicates that noise on the line was interpreted as the inhibit command. The central processor then responds immediately with the resume keyboard transmission command.

- Resume Keyboard Transmission -- This command turns on or unlocks the keyboard and turns off the keyboard locked LED. If any keystrokes are lost, the keyboard responds with an error code.

Each keyboard LED can be turned on and off.

The following eight commands control the keyclick and bell sounds.

Disable keyclick
Enable keyclick and set volume
Disable CNTL keyclick
Enable CNTL keyclick
Sound keyclick
Disable bell
Enable bell and set volume
Sound bell

The following four commands are related to control over the autorepeat mode.

- Temporary Autorepeat Inhibit -- stops autorepeat for a specific key only. It resumes automatically when another key is pressed.

- Enable Autorepeat Across the Board -- starts transmission of metronome codes without affecting autorepeat timing or keyboard division.

- Disable Autorepeat Across the Board -- stops transmission of metronome codes without affecting autorepeat timing or keyboard division.

- Change All Autorepeat to Down Only -- changes all keyboard autorepeating divisions to down only mode.

The following are three other miscellaneous commands.

- Request Keyboard ID -- causes the keyboard to send the two byte ID (firmware and hardware). The keyboard does not jump to the power-up sequence.

- Reinitiate Keyboard -- causes the keyboard to jump to the power-up sequence. Transmission to the keyboard should be held until the host processor receives the last byte of the power-up self-test.

- Reinstate Defaults -- sets the following functions back to the default settings after a successful power-up self-test.

  Division mode settings
  Autorepeat interval and timeout rates
  Autorepeat buffer selections
  Audio volume
  Control key keyclick

To send a peripheral command, set the TYPE flag (low order bit). Bits six -- three contain a command representation from the chart below. Bits two and one specify on (Ø1), off (ØØ), or sound (11). Bit seven should be set if there are no parameters to follow.

Table 7-4 lists the peripheral commands (in hexidecimal).

Command	Representation
Flow control	ØØØ1
Indicator (LEDs)	ØØ1Ø
Keyclick	ØØ11
Bell	Ø1ØØ
Keyboard ID	Ø1Ø1
Keyclick for CNTL key	Ø111
Temporarily inhibit autorepeat	1ØØØ
Jump to test mode	1ØØ1
Change all autorepeat characters to down only	1Ø1Ø
Enable/disable autorepeat	11ØØ

The Jump to power-up command is FD hexidecimal.

Table 7-4 Peripheral Commands in Hexidecimal

Function	Hex	Parameters
Flow control		
Resume keyboard transmission	8B	None
Inhibit keyboard transmission	89	None
Indicators		
Light LEDs	13	Bit pattern
Turn off LEDs	11	Bit pattern
Audio		
Disable keyclick	99	None
Enable click, set volume	1B	Volume
Disable CTRL keyclock	B9	None
Enable CTRL keyclick	BB	None
Sound keyclick	9F	None
Disable bell	A1	None
Enable bell, set volume	23	Volume
Sound bell	A7	None
Autorepeat		
Temporary autorepeat inhibit	C1	None
Enable autorepeat across keyboard	E3	None
Disable autorepeat across keyboard	E1	None
Change all autorepeat to down only	D9	None
Other		
Request keyboard ID	AB	None
Jump to power up	FD	None
Jump to test mode	CB	None
Reinstate defaults	D3	None

The following are some of the peripheral commands.

- Flow Control -- The system module can lock the keyboard with the inhibit keyboard transmission command. When the keyboard is unlocked, it responds with an error code if any keystrokes were missed (refer to section 7.5.6.2).

- Indicators (LEDs) -- Figure 7-12 shows the LED parameter. Figure 7-13 shows the LED layout on the LK201 keyboard.

- Audio -- Figure 7-14 shows the audio volume parameter.

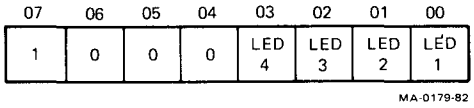


Figure 7-12 Indicator (LED) Parameter

Figure 7-13 Indicator (LED) Layout

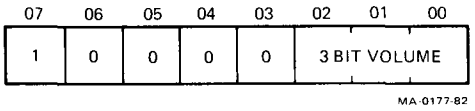


Figure 7-14 Audio Volume Parameter

The audio has the following volume levels.

```
000 -- highest
001
010
011
100
101
110
111 -- lowest
```

Either keyclick or bell (or both) can be disabled. When the keyclick or bell is disabled, it does not sound, even if the system module requests it.

The following are additional peripheral commands.

- Temporary Autorepeat Inhibit -- Stops autorepeat for this key only. Autorepeat automatically continues when another key is pressed.

- Disable/Enable Autorepeat Across Keyboard -- stop/start metronome code transmission without affecting autorepeat timing or division settings.

- Change All Autorepeat to Down Only -- changes division settings for all autorepeating divisions to down only.

- Request Keyboard ID -- causes keyboard to send a two-byte keyboard ID. Keyboard does not jump to powerup.

- Reinitiate Keyboard -- causes keyboard to jump to its powerup routine. The system module should not try to transmit anything to the keyboard until the last byte of the power-up sequence is received.

- Jump To Test Mode -- is a special test mode for production test.

- Reinstate Defaults -- sets the following functions back to the default settings after a successful power-up self-test.

  Division mode settings
  Autorepeat interval and timeout rates
  Autorepeat buffer selections
  Audio volume
  Control key keyclick

7.5.5.4 Mode Set Commands -- This section describes the mode set commands. This section does not provide information about division mode settings. Refer to section 7.5.2 for an explanation of transmission modes and rates.

- Each division on the keyboard has a unique four-bit representation (refer to section 7.5.1). Table 7-2 describes these representations.

- Each mode has a unique two-bit code.

Modes	Representation
Down only	ØØ
Autorepeat down	Ø1
Down/up	11

To set the key transmission mode on a particular keyboard division, the system module must send the PARAMS flag, then the keyboard division representation with the mode code, and then the TYPE flag (cleared).

Figure 7-15 shows a set main array to down/up.

The PARAMS flag is set to one if there are no parameters. The PARAMS flag is clear if there are parameters.

Autorepeat Rate Buffer Association -- If autorepeat mode is selected, the system module can transmit a parameter to change the buffer association of the selected division. Refer to section 7.5.2.3 for autorepeat rates and section 7.5.7 for default values.

Figure 7-16 shows a set main array to autorepeat, changing buffer association to buffer 3.

Autorepeat Rate Buffer Values -- At keyboard power-up time, the four autorepeat rate buffers contain default values (refer to section 7.5.2.3 for autorepeat rates and section 7.5.7 for defaults). The system module may change these values.

In the command byte, bit seven (PARAMS flag) should be clear, bits six -- three are 1111 (to indicate that this is a rate set command), bits two and one should be the buffer number (Ø -- 3), bit zero (TYPE flag) is clear.

There should be two parameters carrying the rate set data.

Figure 7-17 shows change rates in buffer 3.

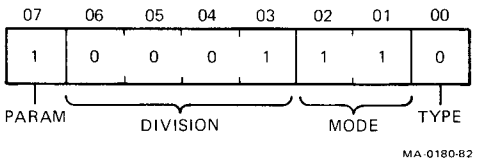


Figure 7-15 Set Main Array to Down/Up Example

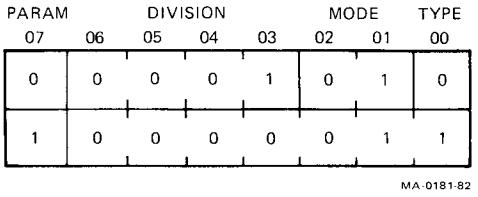


Figure 7-16 Set Main Array to Autorepeat Example

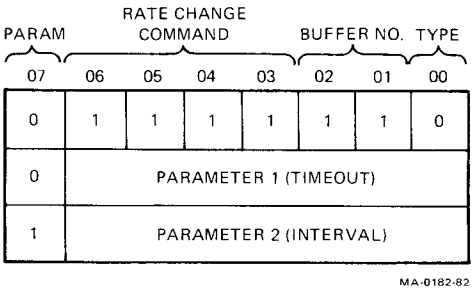


Figure 7-17 Change Rates in Buffer 3 Example

The first parameter specifies the timeout to the store in the selected buffer. The second parameter specifies the interval. (Refer to section 7.5.2.1 for definitions of these parameters.) For example, to set the autorepeat rate in buffer one, the system module firmware transmits 00000011 followed by two bytes of numeric parameters.

The autorepeat timeout is the transmitted number times 5 ms. To specify a rate of 5 ms delay, the first parameter received is 00000001. The maximum allowable time is 630 ms (01111110). The system module must not send 635 (01111111).

NOTE

This code (635) is reserved for internal keyboard use. 00 is an illegal value.

Autorepeat timeout is implemented as a multiple of 8.33 ms (the keyboard's internal scan rate). Timeout rates can vary $\pm$ 4.15 ms.

The autorepeat interval is the number of metronome codes per second. in order to specify a speed of 16 Hz, the second parameter received is 10010000. note that the high order bit is set because it is the last parameter. the highest value which may be sent is 124 (11111100).

The lowest rate which can be implemented by the keyboard is 12 Hz. values as low as 1 can be transmitted, but are translated to 12 Hz.

NOTE

The system module must not send 125 (11111101). This code is the power-up command.

7.5.6 Special Considerations

This section describes the special codes and related considerations.

7.5.6.1 Error Handling -- There are four error codes. The first two are sent at powerup if the self-test fails (refer to section 7.5.4.3). The other two codes are the INPUT ERROR code and the OUTPUT ERROR code.

The OUTPUT ERROR (B5 hexidecimal) is sent after the keyboard receives a resume transmission command, if the output buffer overflowed while the keyboard was locked.

The INPUT ERROR (B6 hexidecimal) is sent when the keyboard detects noise (unidentified command or parameter) on the line. B6 is also sent if the keyboard detects a delay of more than 100 ms when it expects a parameter.

7.5.6.2 Keyboard Locked Condition -- When the keyboard receives an inhibit transmission command, it lights the LOCKED LED and transmits one more byte. This is a special code that indicates the keyboard is locked (KEYBOARD LOCKED ACKNOWLEDGE). If the system module receives this code without a request, the code indicates that noise on the line was interpreted as an inhibit transmission command. The system module should immediately send the resume transmission command to unlock the keyboard.

The output first in the first out (FIFO) buffer in RAM is four bytes. When the keyboard is locked it attempts to store characters received from the keyboard. The keyboard stops scanning its matrix. When the keyboard is unlocked by the system module, it transmits all four bytes in the output buffer. If any keystrokes have been missed due to buffer overflow, the keyboard transmits an error code as the fifth byte (OUTPUT ERROR). Any keys that were not transmitted and are being pressed when the keyboard is unlocked are processed as new keys. An error code upon unlocking the keyboard indicates a possible loss of keystrokes to the system module.

The keyboard stops scanning its matrix when its buffer is full. However, it processes all incoming commands.

7.5.6.3 Reserved Code -- The number 7F (hexidecimal) is reserved for the internal keyboard input and output buffers that handle routines.

7.5.6.4 Test Mode -- The keyboard jumps into a test mode by command during production test. The keyboard transmits a special code to the system module to confirm the test mode. If the system module receives this code, it should send the byte 8Ø (hexidecimal) to continue. This causes a jump to power up.

7.5.6.5 Future Expansion -- Some keycodes are reserved for future use as special codes or keycodes. Table 7-5 lists these reserved codes.

Table 7-5 Keyboard Division Default Modes

Keyboard Division	Mode	AR Buffer
Main array	Autorepeat	Ø
Keypad	Autorepeat	Ø
Delete	Autorepeat	1
Cursor keys	Autorepeat	1
Return and tab	Down only	
Lock and compose	Down only	
Shift and control	Down/up	
Six basic editing keys	Down/up	

7.5.7 Default Conditions

The LK201 has the following default conditions.

- Certain keyboard divisions have specific default modes. Some divisions default to the autorepeat mode. Therefore, they have an associated buffer that contains the default values for timeout and interval. Timeout is the amount of time that the keyboard waits before starting to autorepeat a character. The rate of autorepeating a character is called the interval. Table 7-5 shows the default modes and Table 7-6 shows the default rates in the four keyboard division autorepeat rate buffers.

- The volume levels for the keyclick and bell have an eight-step range. The default volume levels for the keyclick and bell are the third loudest.

- For the LK201 keyboard, the **CNTRL** (control) key defaults to the no keyclick state.

7.5.7.1 **Audio Volume** -- Both keyclick and bell volumes are two decimal (010 binary) by default. The key in position C99 of the keyboard (the **CNTL** key in the LK201) does not generate a click unless enabled by the system module. The keys in position B99 and B11 (**SHIFT** keys on the LK201) never generate a keyclick.

Table 7-6 Default Rates in Autorepeat Buffers

Buffer Number	Timeout (ms)	Internal (Hz)
0	500	30
1	300	30
2	500	40
3	300	40

7.6 SPECIFICATIONS

Functional

Electronics	8-bit microprocessor, 4 KB of ROM, 256 bytes of RAM, 4 LEDs, transducer
Cord	1.9 m (6 ft) coiled, 4-pin telephone-type modular connectors, plugs into display monitor (PN BCCØ1)
Keypad	Sculptured key array
Home row key height	3Ø mm (1.16 in) above desk top
Keys	1Ø5 matte textured finish keys
Main keypad	57 keys
Numeric keypad	18 keys
Special function keypad	2Ø keys, firmware and software driven
Editing keypad	1Ø keys
Spacing	1.9 cm (Ø.75 in) center to center (single width keys)
Wobble	Less than Ø.5 cm (Ø.Ø2Ø in)
Diagnostics	Power-up self-test, generates identification upon passing test

Physical

Height	5 cm (2.Ø in) at highest point
Length	53.3 cm (21 in)
Width	17.1 cm (6.75 in)
Weight	2 Kg (4.5 lb)

CHAPTER 8
MONOCHROME MONITOR

8.1 GENERAL

This chapter describes the VR201 monochrome monitor (shaded area Figure 8-1).

NOTE
This manual does not describe the VT241 color monitor. Refer to the list of related documents in the introduction to this manual to identify VR241 documents.

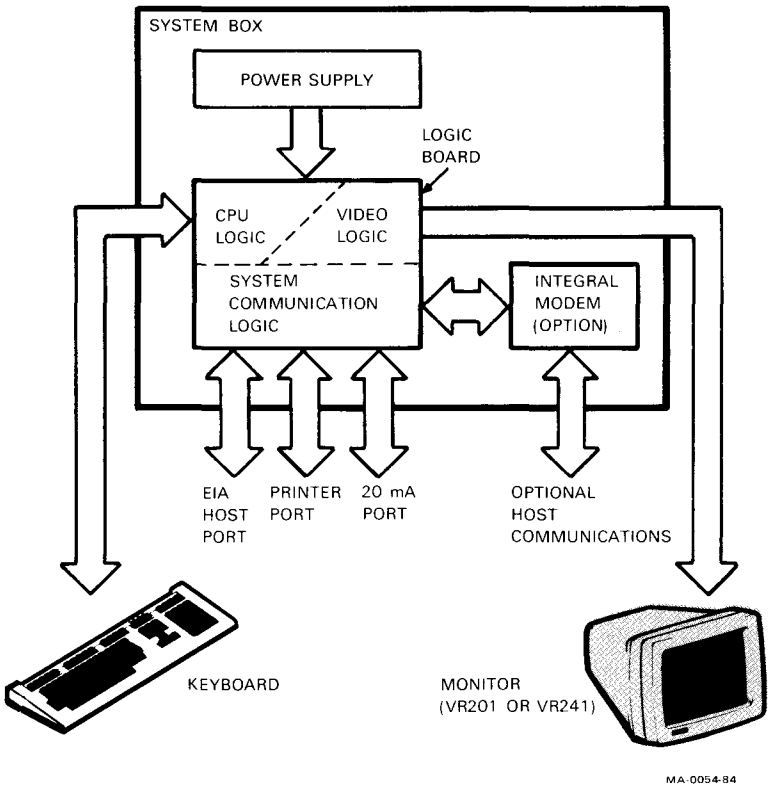


Figure 8-1 VT240-Series Terminal System Block Diagram

The VR2Ø1 monochrome monitor is a raster scan device for displaying alphanumeric and graphic video information. It provides a video display dependent on the composite video signal input from the video logic in the system box.

8.2 PHYSICAL DESCRIPTION

The VR2Ø1 monochrome monitor is enclosed in a wedge-shaped cabinet. The CRT face provides a 12.7 X 2Ø.3 cm (5 X 8 inches) viewing area on a screen that measures 3Ø.5 cm (12 inches) diagonally. A plastic button covers a screw on the cabinet rear. This screw holds the cabinet to the internal wire frame. The CRT and the monochrome monitor module are mounted inside this frame.

The frame has a metal shield and a metal finger stock that presses against the screw mounting bracket. This shield covers the entire inside of the cabinet to prevent electromagnetic radiation. A folding carrying handle is on the bottom rear of the cabinet.

The glass front of the monitor, the CRT face, is specially treated to reduce glare.

The monitor viewing angle is adjustable between +5 to -25 degrees. To adjust the angle, the operator pushes a release button on the right side (Figure 8-2). This causes a friction-lock foot to lower from the bottom of the cabinet housing.

The contrast and brightness controls are on the rear panel. Two connectors, J1 and J3, are on the rear of the monitor. J1 is a 15-pin D-type connector that connects to the system box with a cable (PN BCCØ2). J3 is a modular telephone jack that connects to the keyboard with another cable (PN BCCØ2).

The monochrome monitor has the following dimensions.

Height	24.38 cm (9.75 in)
Width	29.33 cm (11.73 in)
Depth	3Ø.57 cm (12.23 in)
Weight	6.6 kg (14.5 lb)

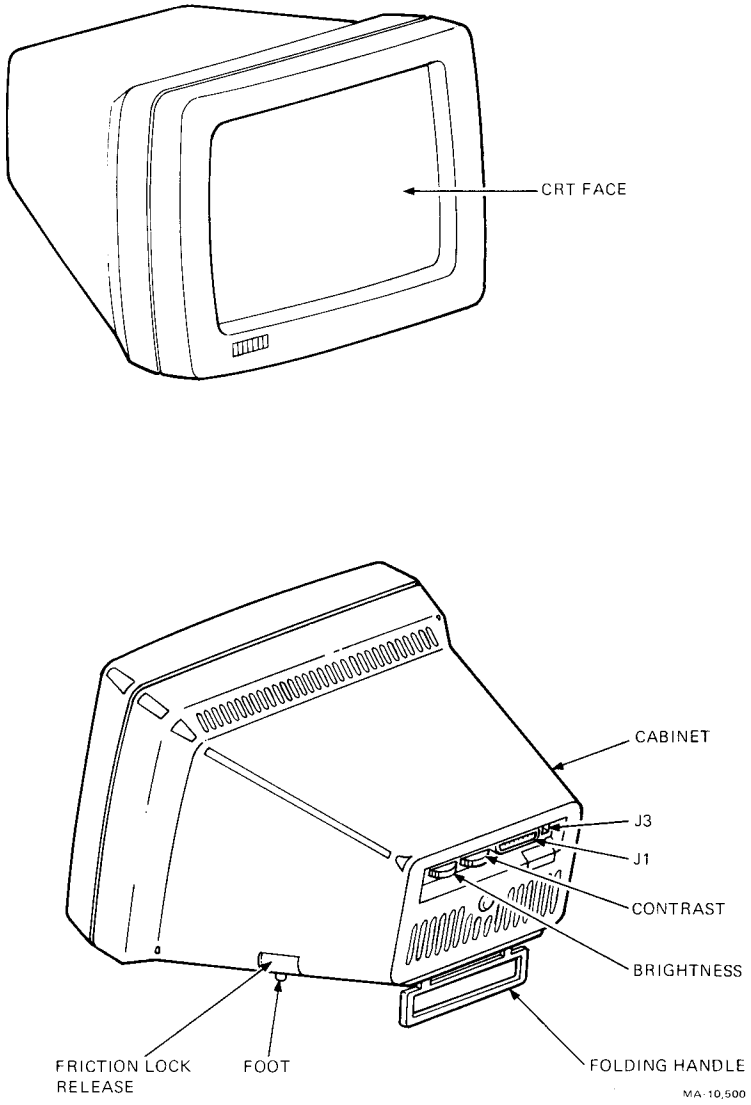


Figure 8-2 Monochrome Monitor Exterior View

8.3 FUNCTIONAL OVERVIEW

The VR2Ø1 monochrome monitor consists of two main components: a 12-inch diagonal CRT with a yoke assembly mounted on it, and an electronics module (Figure 8-3).

The monitor's primary function is to display. The monitor's secondary function is to route information between the system box and the keyboard. The keyboard connects with the monitor via J3 (Figure 8-3). J3 is hardwired on the module to J1, which connects to the system box.

The monitor module controls the CRT and the yoke assembly. A composite video signal is input to the module from the system box (Figure 8-3). This signal consists of two types of information: video data (refer to section 8.3.1), and sync data (refer to section 8.3.2).

The monitor module provides the following power to the CRT.

- Anode voltage
- Grid 1 voltage (brightness)
- Grid 2 voltage (cutoff)
- Grid 4 voltage (focus)
- Heater voltage
- Cathode voltage

The control inputs to the CRT refine the electron beam. The anode voltage attracts the beam to the faceplate and provides a single connection between the CRT and the module (Figure 8-3). P1 provides all other CRT inputs. P1 is mounted directly on the CRT and is hardwired to the module. Refer to section 8.7.7 for more information.

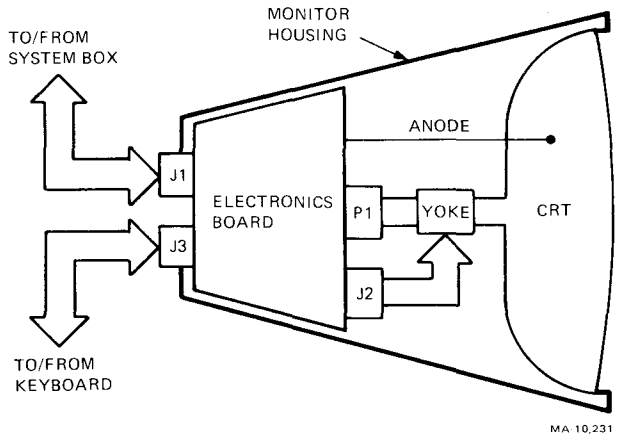


Figure 8-3 Monochrome Monitor Block Diagram

8.3.1 VIDEO Data

The monitor module uses the video portion of the signal to generate outputs to the CRT cathode. The CRT responds to the video by generating various intensities in the electron beam. The intensity of the beam depends on the amplitude of the video signal provided.

8.3.2 SYNC Data

The sync portion of the video synchronizes the generation of horizontal and vertical signals to the yoke assembly. The horizontal and vertical processor chips use peak detector circuits to separate the synchronizing signals. The yoke assembly, which connects to the electronics board via J2, consists of electromagnetic coils (Figure 8-3). These coils use the signals output by the module to generate magnetic fields which position the electron beam generated by the CRT. The horizontal signal to the yoke controls the sweep of the electron beam horizontally across the faceplate (each sweep is called a scan line). The vertical signal controls the positioning of the beam to a new scan line for vertical positioning.

8.4 MONOCHROME MONITOR SYSTEM COMMUNICATION

The monochrome monitor connects with both the system box and the keyboard. The system box connects to the monitor via J1, a 15-pin D-type subconnector. The keyboard connects via J3, a modular telephone jack.

J1 has three basic functions: supply video input used only at the monitor, supply operating voltages used by both the monitor and the keyboard, and transfer keyboard data (Figure 8-4). The operating voltage and keyboard data lines are hardwired from J1 to J3 on the electronics board.

Table 8-1 provides a pin-out for J1 that includes signal identifications and functional descriptions. Table 8-2 provides the same information for J3.

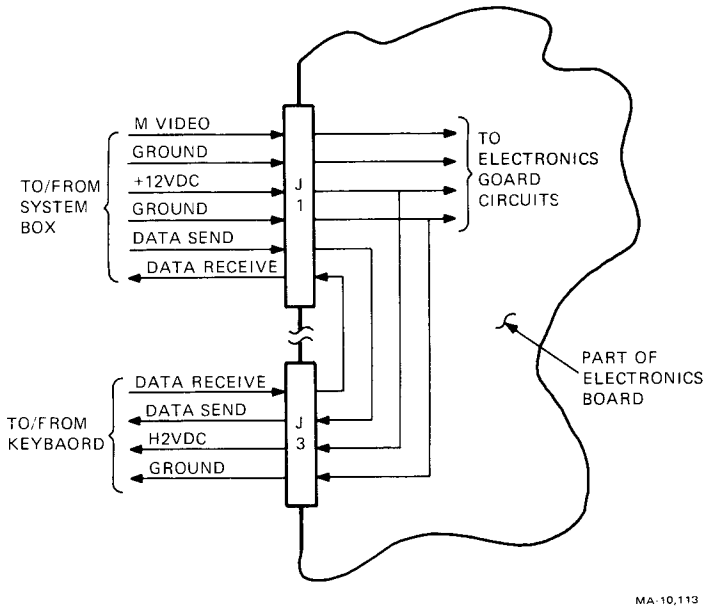


Figure 8-4 Monochrome Monitor System Communications Diagram

Table 8-1 J1 Pin-out

Pin(s)	Signal	Description
1--3	Not used	None
4	Ground	Video signal ground potential
5,6	Ground	Operational voltage ground potential
7,8	+12 Vdc	Operational voltage input
9--11	Not used	None
12	M Video	Composite video (refer to section 8.3.1)
13	Ground	Tied to pins 5 and 6
14	Data Receive	Serial data line from the keyboard output to the system box (via J3)
15	Data Send	Serial data line from the system box output to the keyboard (via J3)

Table 8-2 J3 Pin-out

Pin	Signal	Description
1	Data Send	Serial data line for output from the system box to keyboard (via J1, pin 15)
2	+12 Vdc	Output of operational voltage to keyboard (from J1, pins 7 and 8)
3	Ground	Operational voltage ground potential (from J1, pins 5, 6, and 13)
4	Data Receive	Serial data line for input from keyboard to system box (via J1, pin 14)

8.4.1 Composite Video Signal

The video input to the monitor is a composite of two types of signals, video and sync. There are different levels of illumination within the video signal, ranging from totally black to maximum brightness.

Figure 8-5 represents a typical composite video signal and identifies the major terms associated with it. This signal, used with the monochrome monitor, is dc-coupled to ground at the monitor module. Table 8-3 lists typical signal values.

Figure 8-6 shows the composite video signal and the sync portion of this signal. Table 8-4 describes the values for the sync components identified.

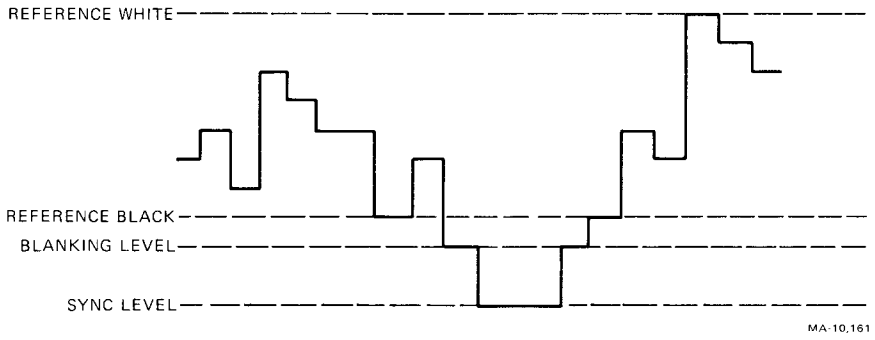


Figure 8-5 Composite Video Signal Representation

Table 8-3 Composite Video Values

Characteristics	Value
Output impedance	75 ohms, dc coupled to Ø V
Amplitude	1.Ø V peak-to-peak nominal (monitor accepts signals with peak-to-peak values of Ø.9 V through 1.5 V)
Reference black	Low limit of display value. It equals 3Ø percent of peak-to-peak value (Ø.3 V nominal), and is lowest voltage value amplified linearly at the electronics board.
Reference white	High limit of display value. It equals 1ØØ percent of peak-to-peak value (1.Ø V nominal), and is highest voltage value amplified linearly at the electronics board.
Blanking level	Voltage value which reduces CRT electron beam current below cutoff.
Sync level	Voltage level at which sync actions can take place; Ø V nominal (dc coupled video to ground).
Continuous input	+2.Ø V maximum (2.Ø V saturates the video amplifier unless the contrast thumbwheel adjustment is reduced).

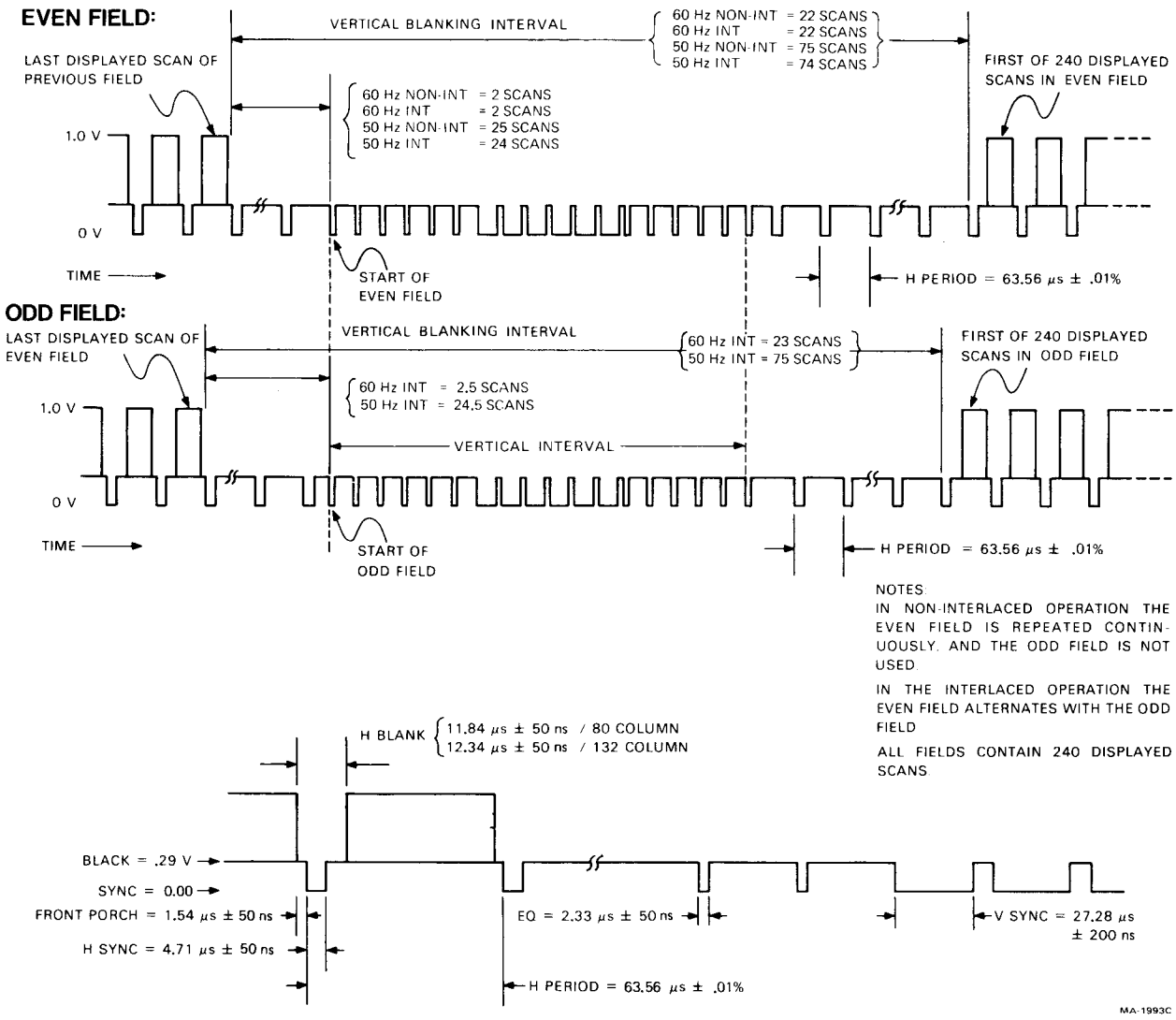


Figure 8-6 Composite Video Sync Timing Diagram

Table 8-4 Composite Video Sync Component

Component	Description
Vertical blanking interval	Period of time vertical retrace activity blanks the screen. Vertical retrace completes in less than 1.Ø ms, and within an allowed frequency range of 49 -- 61 times per second.
V Sync	Period of time the vertical deflection circuitry on the electronics board takes to synchronize the next frame.
H Sync	Time the horizontal deflection circuitry on the electronics board takes to synchronize for retrace.
H Period	Period of time for the horizontal scan plus horizontal blanking (63.5 ~s)
EQ	Equalizer pulse that synchronizes vertical deflection circuitry on electronics board for vertical retrace activity.
Front porch	Delay value between start of blanking and start of sync pulse.
Vertical interval	Period of time the actual synchronizing of the vertical deflection circuitry on the electronics board takes place. Consists of six EQ pulses, six V sync pulses, and six more EQ pulses.

8.5 CRT

The CRT provides the final video output, an electron beam, fired at a phosphor-coated faceplate.

Electron beam generation is controlled directly by the monitor module inputs. The module controls the yoke, which in turn controls positioning the beam at the faceplate.

The CRT contains an electron gun. The gun consists of the heater element, a cathode, three grids (G1, G2, and G4), an anode, and the faceplate, all encased in a vacuum.

The three grids control the beam generated by the gun, G1 for brightness, G2 for beam cutoff and G4 for focus.

G1 is directly affected by the brightness control thumbwheel. This lets operator adjust the background intensity of the display. G2 provides video sharpening capabilities. To do this, G2 acts as a gate, or valve, to the electron beam. A voltage, provided to G2, prevents the electron beam from passing to the faceplate unless the beam is a specific minimum intensity. G4 focuses the electron beam.

The CRT plugs directly into P1 which is hardwired onto the module. Through P1, the operating voltages for the heater element, the cathode, and the three grids are provided. The anode voltage is provided by a separate connection between the module and the CRT. Its ground goes to the CRT case. This ground reduces shock hazard and consists of three parts: a connection between the module and a terminal block on the yoke, a connection between the block and the CRT case, and a connection between the block and P1.

8.6 YOKE

The yoke is a set of electromagnetic devices mounted on the CRT neck. One device is for horizontal deflection of the electron beam, the other is for vertical deflection.

Currents to control the horizontal scan line are applied to the yoke's coil (inductance) through the width inductor and the linearity inductor. The vertical trace control current comes from the vertical processor chip.

The yoke connects to the electronics board through J2: pins two and three for the horizontal deflection magnetic coils, and pins one and four for the vertical.

8.7 MONITOR MODULE

The monitor module is made of discrete analog components. It can be divided into seven circuits to control the CRT and yoke.

Figure 8-7 is a block diagram of the module that shows the seven circuits. The figure also identifies the fuse for the power input (F1) and three connectors (a fourth connector, J3, which routes signals between J1 and the keyboard is not shown). The following sections describe each item shown in Figure 8-7.

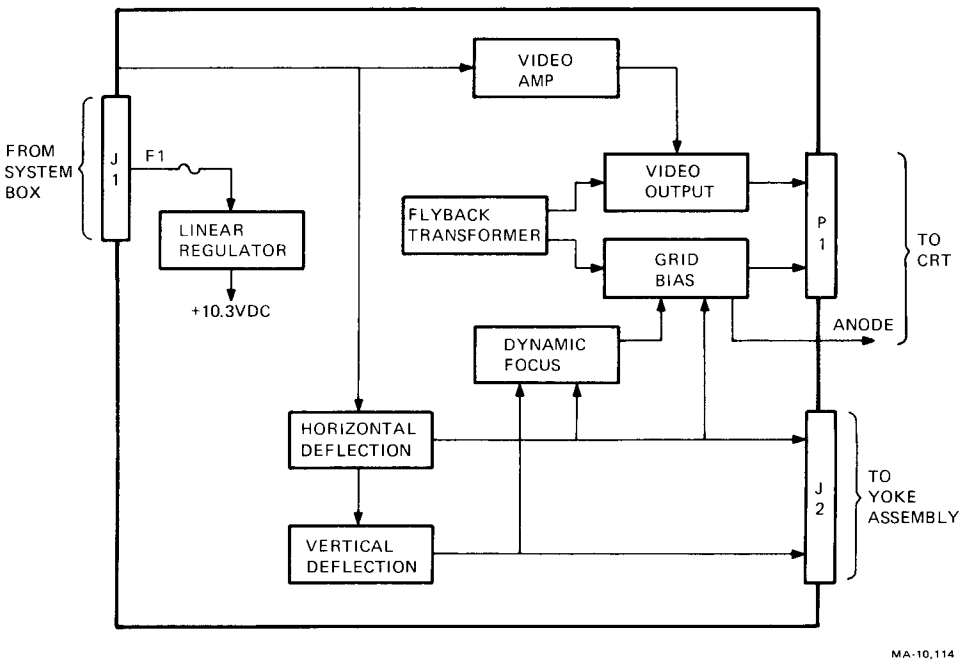


Figure 8-7 Monitor Module Block Diagram

8.7.1 Dynamic Focus

This circuit creates different focus voltages for different areas on the screen. Output from this circuit is tied to focus biasing circuitry within the grid bias circuit. This output offsets focus biasing based on horizontal and vertical deflection values. The circuit is primarily a single transistor which acts as a mixer for parabolic inputs from the horizontal and vertical deflection circuits. This changes focus biasing as a function of the position of the beam on the tube.

8.7.2 Grid Bias

This circuit generates CRT biasing values: focus (G4), cutoff (G2), and brightness (G1). These voltages are developed from the flyback transformer. Voltages from this transformer are routed to the G4 and G2 circuits. There are two resistor networks that each contain potentiometers for adjusting the bias in question, R43 for G4 (focus) or R12Ø for G2 (cutoff). The remaining bias circuit, G1 (brightness), is a resistor network between two voltage sources, +4Ø Vdc and -15Ø Vdc. This adjustment allows the operator to adjust the display background intensity. The voltage on G1 is adjustable from approximately Ø to -47 Vdc.

8.7.3 Horizontal Deflection

This circuit drives the CRT beam across the faceplate horizontally. This circuit contains the following elements.

- A horizontal processor
- A sync buffer circuit
- A horizontal driver and output
- RC networks that bias circuits internal to the horizontal processor
- A horizontal deflection generator output stage (width and linearity inductors, horizontal output transistor, damper diode, retrace capacitor, and yoke inductor)

An oscillator within the horizontal processor allows the horizontal deflection circuit to free run. The sync pulses then synchronize the operating running rate to the video input.

The sync buffer circuit amplifies the sync pulse and then applies it to the horizontal processor. When the horizontal output turns off, the electron beam flies back, returning the beam to the left of the screen. At the end of retrace, the conducting of the damper diode establishes a ramp of current in the yoke inductor. To make sure the output transistor is turned on at the proper time, the horizontal deflection IC also provides the correct timing on its output pulse. This allows the current ramp to continue after the damper diode stops conducting. The width coil portion of the output stage adjusts the width of the display. Two of the RC networks contain potentiometers for adjusting their biasing values: R211 for hold (horizontal) and R218 for centering (phase).

A secondary output from the generator is provided to the vertical deflection circuitry as a vertical sync signal.

8.7.4 Linear Regulator

This circuit provides power to the flyback transformer during initial powerup and also regulates the input voltage. During initial powerup, the +12 Vdc voltage is applied to the regulator. The voltage input (rising from Ø V to +12 Vdc) is shunted through a series of 4 diodes and then through the flyback transformer. This generates 4Ø Vdc at the input of L3ØØ to the regulator field effect transistor (FETs) sources. The FETs are then turned on and conduct the load current instead of the diodes. A precision zener diode plus the regulator transistor's VBE cause the circuit to provide 1Ø.3 Vdc regulated output.

8.7.5 Vertical Deflection

This circuit positions the CRT beam across the faceplate vertically. This ciruit contains the following elements.

- A vertical processor
- Various RC networks that bias circuits internal to the vertical processor
- An output filter network.

An oscillator within the vertical processor allows the vertical deflection circuit to free run. The sync pulses synchronize the vertical deflection to prevent vertical roll.

Three of the RC networks contain potentiometers for adjusting biasing values: R48 for hold (vertical), R50 for height, and R53 for linearity. At the beginning of each refresh cycle, the vertical processor receives a vertical sync pulse from the horizontal processor circuit. The horizontal processor detects the vertical sync pulse and sends it to the vertical processor. This sync pulse comes from the composite video input to the monitor module. The vertical sync pulse causes the beam to fly back vertically and begin a new frame.

8.7.6 Video Amplifier (Amp)

The video amp consists of an input and output stage. The video signal is applied to an input push/pull transistor network which is part of an encapsulated transistor array. The input is provided from R5, the contrast thumbwheel potentiometer. The operator can adjust the potentiometer for personal contrast preference. The potentiometer, R119, provides a preamplifier adjustment to preset the range that can be affected by the contrast thumbwheel. Biasing the input stage affects biasing the output stage, which is another transistor network. The more positive the input to the input stage, the more positive the output from the transistor network. This output is provided to the video output stage.

The video output stage provides the operating voltage for the CRT beam. The video output stage uses the voltage from the flyback transformer (40 Vdc) to generate its output. The sync pulses (horizontal and vertical) set the video output to or below the cutoff voltage so the operator does not see the retrace lines. Applying increased positive video amp signal decreases output to the CRT. This also increases the intensity of the CRT display.

8.7.7 Flyback Transformer

The flyback transformer is the high voltage power supply and is synchronized to horizontal deflection. The transformer generates the voltages used by the grid bias circuit (G1, G2, and G4), the anode voltage (12.5 kV nominal), and the 40 Vdc voltage used by the linear regulator and video amplifier.

WARNING

The monochrome monitor contains shock hazard voltages. Use extreme caution when servicing the monitor.

There is a high voltage (12 kV nominal) on the anode lead and the anode cup on the side of the CRT.

To avoid shock, use the following procedure when discharging the anode.

1. Turn off system power and connect the monitor cable.

2. Attach the clip lead of the anode discharge tool to the metal frame.

3. Hold the tool by its insulated handle. Using one hand, carefully slide the tip of the tool under the plastic anode cap until it touches the anode. Avoid scratching or poking the glass CRT envelope.

4. Once discharged, remove the tool and clip lead.

There is also 700 Vdc on the monitor module near the flyback transformer. Use caution when performing adjustments in this area. This area is covered with a protective shield.

CAUTION

Before removing the system module monitor cable, turn off system power. Static discharge in the CRT can damage the monitor module and/or keyboard electronics.

Make sure the system power is off before connecting or disconnecting the monitor's cable for service or to move the

the monitor. When performing adjustments, secure the monitor's cable to the monitor with its thumbscrews so the cable does not loosen.

If you do not follow this procedure, you can damage monitor and/or keyboard components.

8.7.8 J1

This connector provides the voltage and video signals to the electronics board. Refer to section 8.4 for the J1 pin-out and signal descriptions.

8.7.9 J2

This connector provides the horizontal and vertical deflection currents between the electronics board and the yoke assembly. It is a four-pin connector. Pins one and four are used for vertical deflection, pins two and three are used for horizontal deflection.

8.7.10 P1

This connector mounts on the electronics board that the CRT plugs into. Figure 8-8 shows the P1 pin-out.

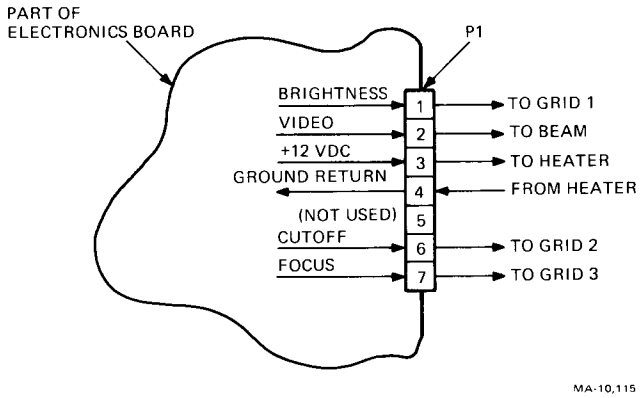


Figure 8-8 Monitor Module P1 Pinout

CHAPTER 9
POWER SUPPLY

9.1 GENERAL

The system box power supply (shaded area in Figure 9-1) converts ac input to the dc voltages required by the logic board.

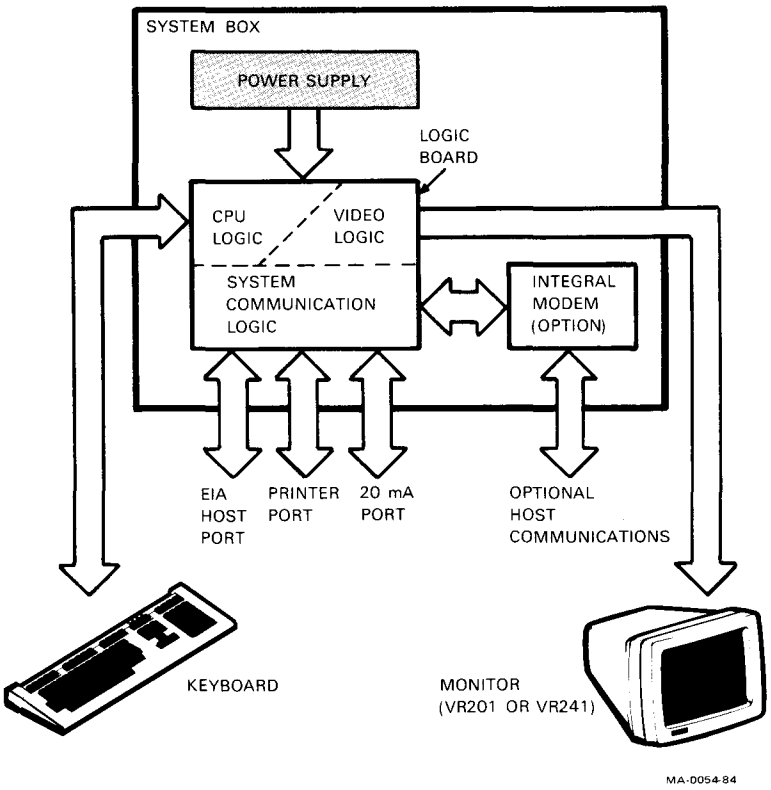


Figure 9-1 VT240-Series Terminal System Block Diagram

9.2 MAJOR CIRCUITS/COMPONENTS

The power supply (Figure 9-2) consists of various components and circuits, including circuits physically mounted on the logic board. The power supply has the following major circuits and components.

- AC input and fan components.
- Power supply 1 (PS1)
- DC power input connector (J1)
- +5 V input circuit
- +12 V input circuits
- -12 V input circuit
- DC power Okay

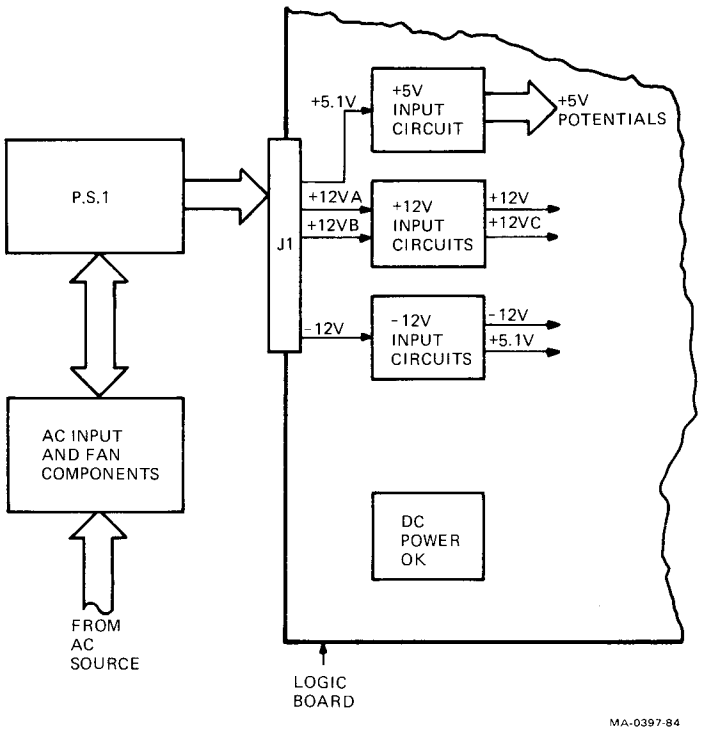


Figure 9-2 Power Supply Block Diagram

9.2.1 AC Input And Fan Components

The ac input components provide for ac input, including voltage range selection (115 Vac or 230 Vac), while the fan (B1) provides neccessary cooling for the PS1 (refer to section 9.2.2).

The AC input and fan components (Figure 9-3) consist of the following items.

- Fan Assembly -- includes the fan (B1, a +12 Vdc powered device) and connector P1.
- J1 -- provides PS1 connector for fan assembly.
- S1 -- provides the voltage selection switch.
- S2 -- provides the power on/off switch that connects ac input to the PS1 (via the PS1 LN connector, a two-pin quick disconnect jack).
- F2 -- provides a 3 amp, 250 Vac input line fuse.

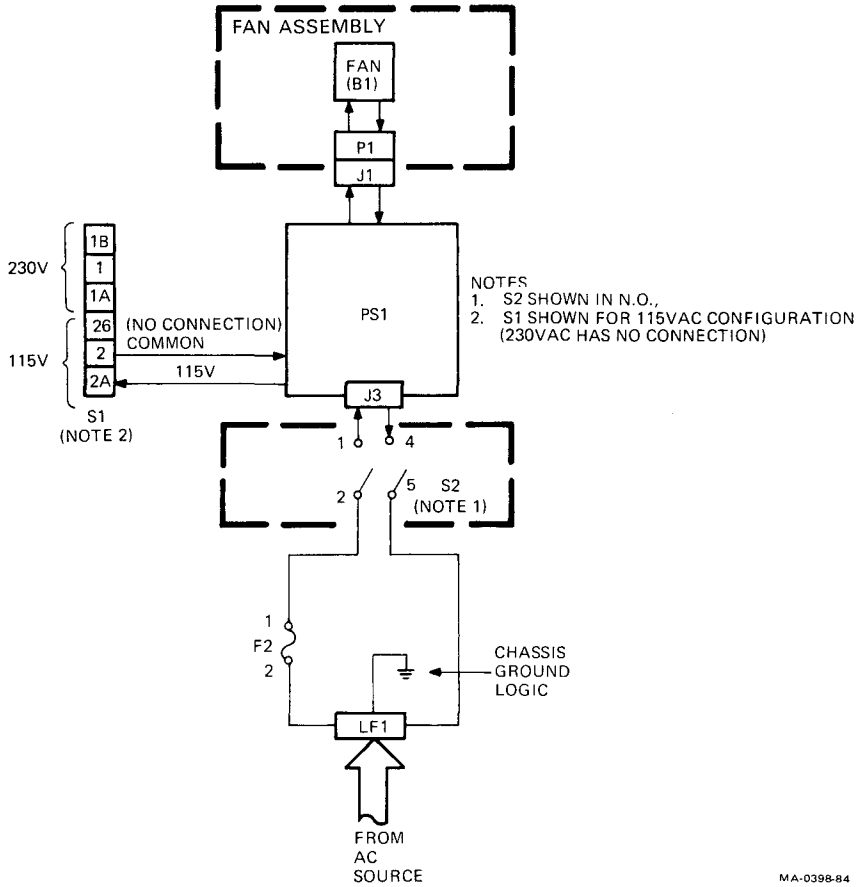


Figure 9-3 AC Input and Fan Components Block Diagram

- Line Filter 1 (LF1) -- filters the ac input, which is connected by the system box power cord directly into the LF1.

- Chassis Ground Lug -- provides a ground connection for the ac input ground from LF1.

Figure 9-4 shows the physical location of the ac input and an components, as well as the PS1.

9.2.2 Power Supply 1 (PS1)

The PS1 is manufactured by Astec Corporation for the VT240 Series terminal according to specifications outlined in the VT240 Power Supply Purchase Specification (PS 3021383-0-0).

The PS1 electrical components (Figure 9-5) are all located on a single PCB. The PS1 consist of the following circuits/components.

- J1 -- provides the connector for routing +12 VA to the fan.

- J2 -- provides the 19-pin connector for routing dc potentials to the system box logic board.

- J3 -- provides the two-pin connector to input ac from the on/off switch.

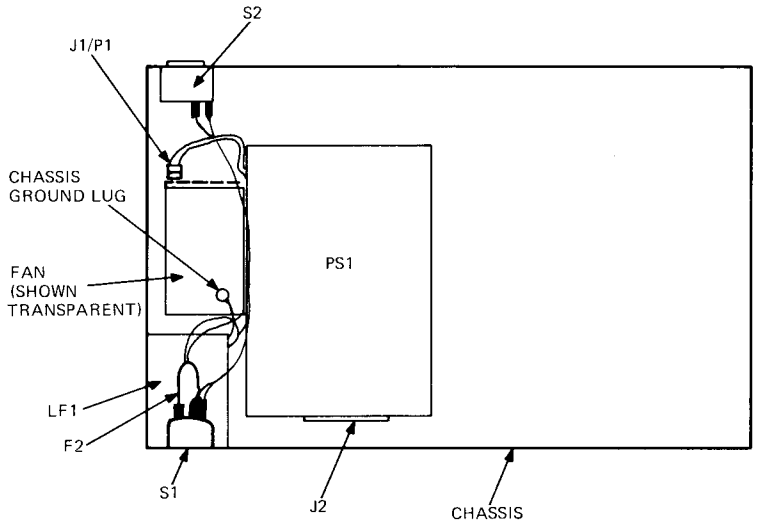


Figure 9-4 Physical Location of Power Supply Components

- Switch Pin Connectors -- connect to the voltage selection switch (S1, pins 2 and 2A), for 115 Vac, and have no connection for 230 Vac (the power supply recognizes 230 Vac selection with no connection to the voltage select switch, or when connection is made to 115 Vac pins of switch and switch is in 230 Vac position).

- Input Regulation -- consists of components responsible for ac input, and regulation of isolation, inrush current, undervoltage, overvoltage, and high voltage transient conditions.

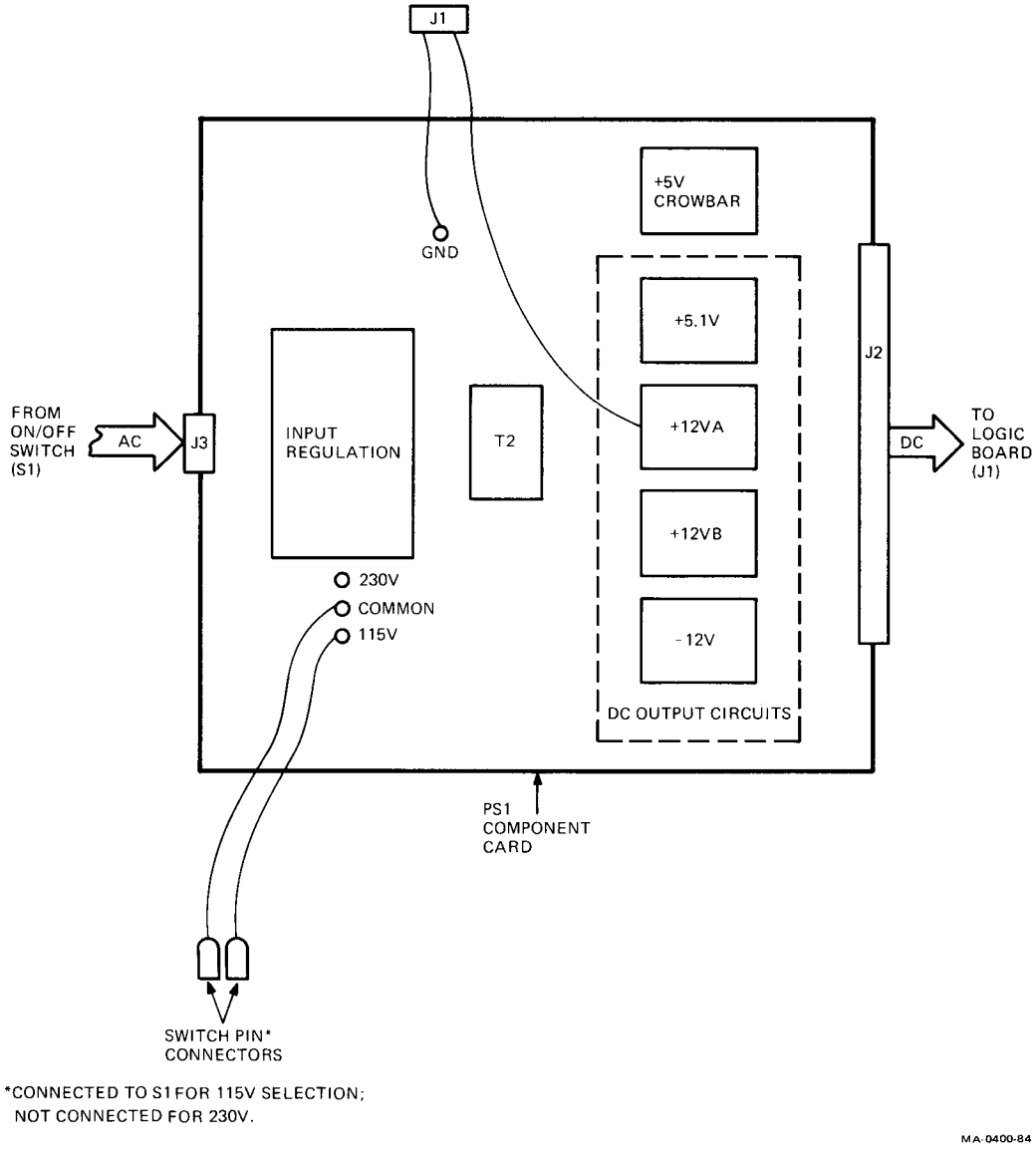


Figure 9-5 Power Supply 1 (PS1) Block Diagram

- T2 -- transforms regulated ac input into secondary voltages used by the dc output circuits to generate the required dc potentials.

- DC Output Circuits -- generate the dc potentials output from the PS1 (+12 VA, +12 VB, +5.1 V, and -12 V).

- +5.1 V Crowbar -- provides overvoltage protection on +5.1 V output of maximum output of 6.9 V.

Figures 9-6 is a circuit schematic of the input regulation circuits; Figure 9-7 is a circuit schematic of the dc output circuit, and Figure 9-8 is a circuit schematic of the +5.1 V crowbar circuits. Figure 9-9 shows the layout of the PS1 components on the PCB.

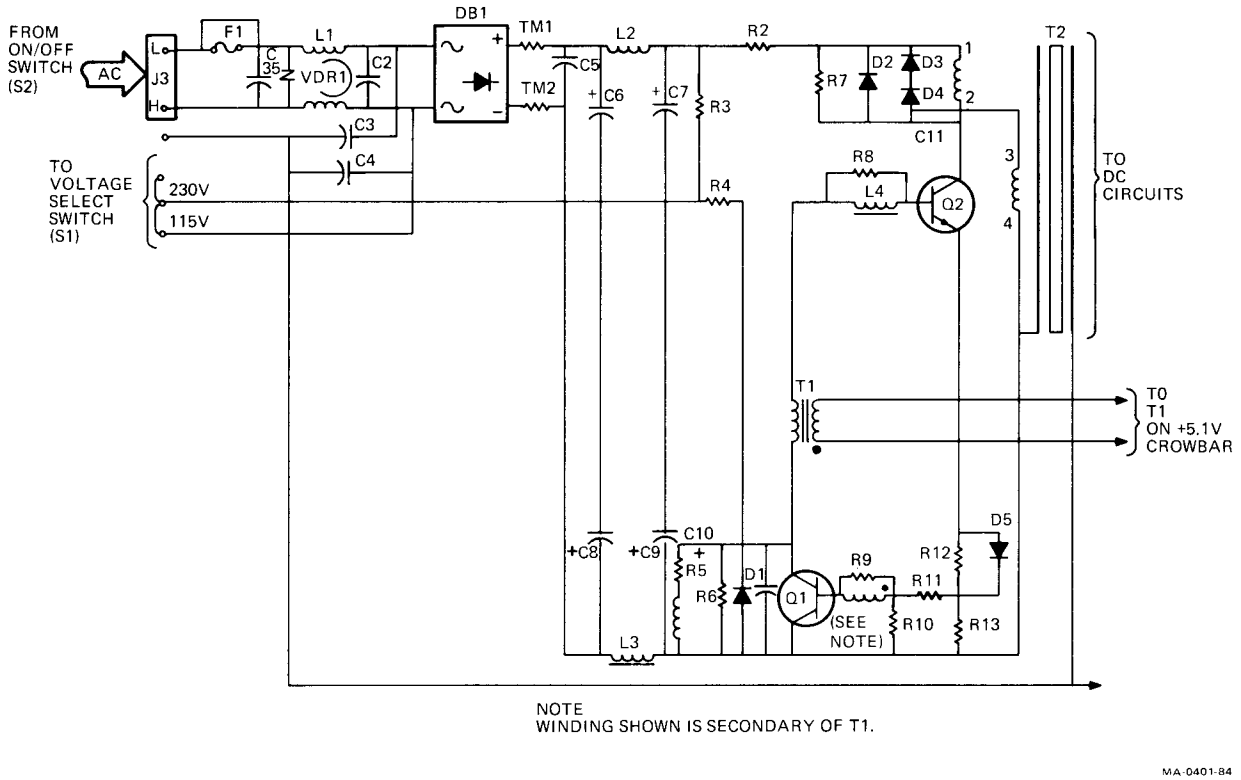


Figure 9-6 Input Regulation Circuitry

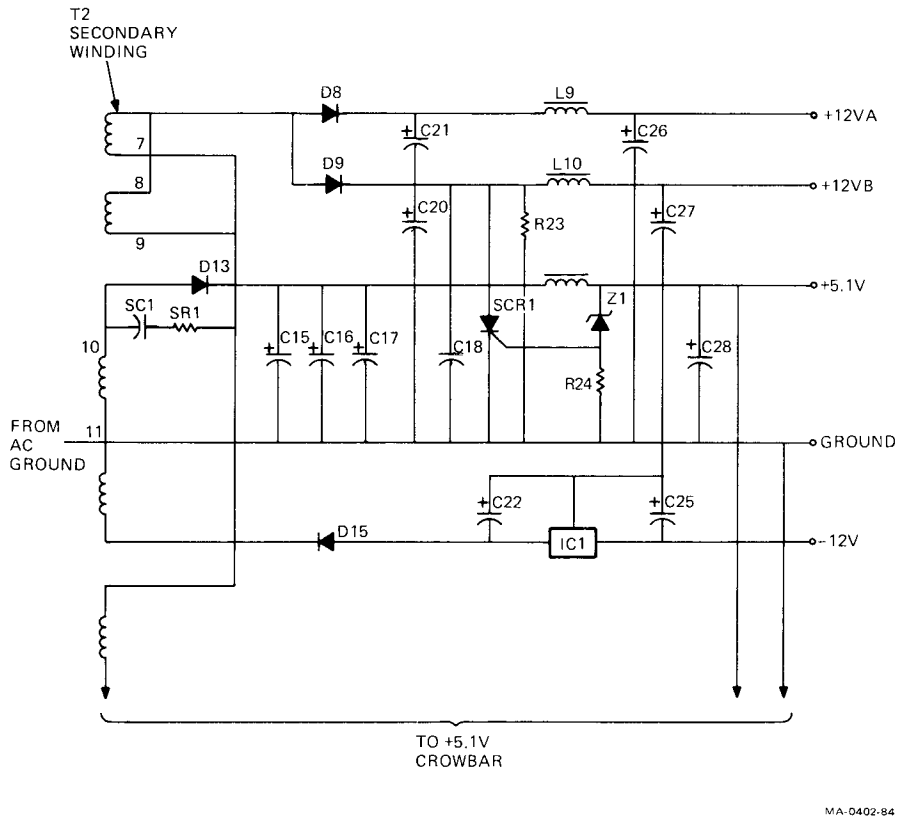


Figure 9-7 DC Output Circuits

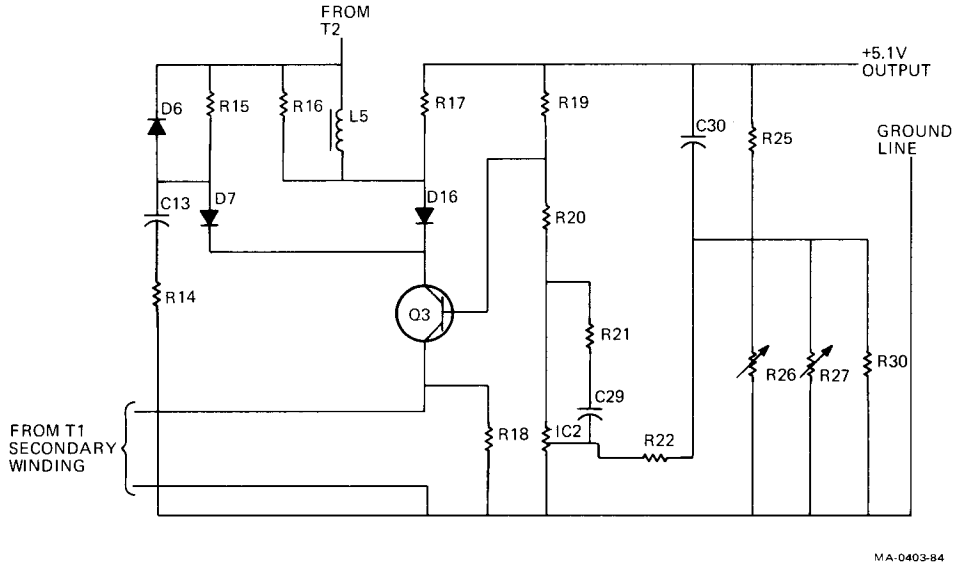


Figure 9-8 +5.1 V Crowbar Circuit

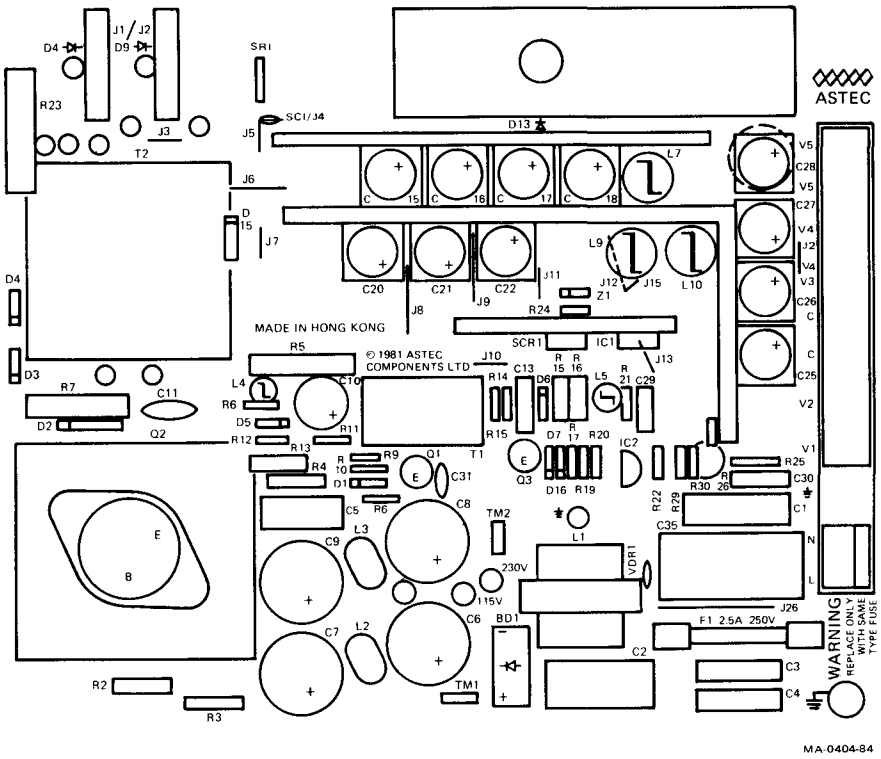


Figure 9-9 PS1 Component Layout

Table 9-1 lists the component values for the PS1 components shows in Figures 9-6, 9-7, and 9-9. Table 9-2 provides specification information for the ac voltages. Table 9-3 provides the same information for dc voltages. Refer to section 9.2.3 (a description of J1 on the logic board) for a pin-out for J2.

Table 9-1 Power Supply 1 (PS1) Components

Code	Type	Description
C1	MP capacitor	0.1 uF, +20%, 250 V
C2	MP capacitor	0.22 uF, +10%, 250 V
C3,C4	MP capacitor	2200 pF, +10%, 250 V
C5	Poly capacitor	0.1 uF, +10%, 400 V
C6-C9	Elect capacitor	100 uF, +20%, 250 V
C10	Elect capacitor	470 uF, +50, -10%, 250 V
C11	CER capacitor	1000 pF, +20%, 3 KV, Z5P
C12,C14,C19,C23, C24,C32-C34	--	Not used
C13	Poly capacitor	0.22 uF, +10%, 100 V
C15-C18,C20,C21	Elect capacitor	1000 uF, +100, -10%, 10 V
C22	Elect capacitor	220 uF, +100, -10%, 25 V
C25	Elect capacitor	100 uF, +50, -10%, 25 V
C26,C27	Elect capacitor	680 uF, +100, -10%, 16 V
C28	Elect capacitor	1000 uF, +50, -10%, 25 V
C29	Poly capacitor	0.022 uF, +20%, 100 V
C30	Poly capacitor	0.22 uF, +10%, 100 V
C31	CER capacitor	0.01 uF, +20%, 100 V, Z5U
D1	Rectifier	RGP10A
D2-D4	Rectifier	RGP10M
D5,D13	Rectifier	RGP15B
D6,D7,D16	Silicon diode	1N4606
D8,D9	Rectifier	3S4M
D10,D12,DI4,D17-D19	--	Not used
D13	Schottky diode	S15S4
DB1	Bridge rectifier	KBL08
F1	Fuse	2.5 A, 250 V
IC1	Regulator	--
IC2	Regulator	--
IC3,IC4	--	Not used
L1	Choke	Common mode assy
L2,L3	Choke	Toroid
L4	Choke	BASE, 2.2 uH
L5	Choke	1.5 mH
L6,L8,L11	--	Not used
L7,L9,L10	Choke	Coil assy
Q1	NPN transistor	2SD592NC or 2SD467C
Q2	NPN transistor	--
Q3	PNP transistor	2SB621NC or 2SB561C

Table 9-1 Power Supply 1 (PS1) Components (Cont)

Code	Type	Description
R1,R27,R28,R31-R33	--	Not used
R2	Metal film	Ø.75, +5%, 1 W
R3,R4	Metal oxide film	1ØØ K, +5%, 1 W
R5	Metal oxide film	39, +5%, 2 W
R6	Carbon film	1.2 K, +5%, 2 W
R7	Metal oxide film	12Ø, +5%, 2 W
R8	Carbon film	5.6, +5%, 1/4 W
R9,R2Ø	Carbon film	68, +5%, 1/4 W
R1Ø,R11	Carbon film	1Ø, +5%, 1/4 W
R12,R17	Carbon film	8.2, +5%, 1/4 W
R13	Metal film	Ø.33, +5%, 1 W
R14	Carbon film	33, +5%, 1/4 W
R15	Carbon film	27Ø, +5%, 1/2 W
R16	Metal oxide film	22Ø, +5%, 1 W
R18	Carbon film	33Ø, +5%, 1/4 W
R19	Carbon film	56, +5%, 1/4 W
R21	Carbon film	12 K, +5%, 1/4 W
R22	Carbon film	47O, +5%, 1/4 W
R23	--	22Ø, +5%
R24	Carbon film	12, +5%, 1/4 W
R25	Metal film	2.7 K, +1%, 1/4 W
R26	--	2.1 K, +1%
R29	Carbon film	68Ø, +5%, 1/4 W
R3Ø	Carbon film	68, +5%, 1/4 W
SC1	CER capacitor	Ø.Ø1 uF, +2Ø%, 1ØØ V, Z5U
SCR1	Rectifier	SCR C122U
SR1	Carbon film resistor	1Ø, +5%, 1/4 W
TM1,TM2	Thermistor	4, +1Ø%
VDR1	Voltage rectifier	VDR 26Ø Vac
Z1	Zener diode	5.6 V, +5%, 1 W at 4Ø mA

Table 9-2 Input Voltage Specifications

Specification	Value
115 Vac	
Nominal voltage	120 Vac
Minimum voltage	90 Vrms
Maximum votage	128 Vrms
Input line current	2.2 Arms (maximum)
Line frequency	47 Hz -- 63 Hz
Power factor	Watts = (RMS V X RMS A)
Inrush current	>0.60 surge current at first application of input voltage may be reached for 1/2 cycle of input line, with repetitive peaks of exponentially decaying amplitude for up to 10 more cycles.
Surge Current	25 A (peak) (thermisters cold)
Input Power	120 W (max) at full rated dc output load of 77 W.
Efficiency	0.65 (minimum) output power to input power ratio.
Undervoltage	Provides minimum of 5 millisecond hold-up at 90 Vrms during power outage.
Overvoltage	150 Vac for 1 second (maximum)
Transients	Low energy transient of 300 V peak spike with no more than 0.2 watt seconds of energy per spike; High energy transient of 1 KV peak spike with no more than 2.5 wattseconds of energy per spike.
230 Vac	
Nominal voltage	240 Vac
Minimum voltage	180 Vrms
Maximum votage	268 Vrms
Input line current	1.1 Arms (maximum)
Line frequency	47 Hz -- 63 Hz
Power factor	Watts = (RMS volts X RMS amps)
Inrush current	>0.60 surge current at first application of input voltage may be reached for 1/2 cycle of input line, with repetitive peaks of exponentially decaying amplitude for up to 10 more cycles.
Surge current	25 A (peak) (thermisters cold)
Input power	120 W (maximum) at full rated dc input load of 77 W.

Table 9-2 Input Voltage Specifications (Cont)

Specification	Value
Efficiency	Ø.65 (minimum) output power to input power ratio.
Undervoltage	Provides minimum of 5 millisecond hold-up at 18Ø Vrms during power outage.
Overvoltage	3ØØ Vac for 1 second (maximum)
Transients	Low energy transient of 3ØØ V peak spike with no more than Ø.2 watt seconds of energy per spike; High energy transient of 1KV peak spike with no more than 2.5 watt seconds of energy per spike.

Table 9-3 Output Voltage Specifications

Voltage	Specification	Value
+5.1 V	Nominal output	+5.1 V
	Minimum load	4 A
	Maximum load	6.5 A
	Ripple and noise	5Ø mV peak-to-peak (maximum) (see note)
	Total regulation	+3% to -5%
	Long term stability	Ø.1%/1ØØØ hr
	Overcurrent	No damage for any permanent overcurrent averaging 7.8 A or less, with peak current of 1Ø A or less in any 1Ø second period, or for a permanent short circuit.
	Overvoltage	6.9 V (maximum) with crowbar protection
+12 Va	Nominal output	+12 V
	Minimum load	Ø.2 A
	Maximum load	1.Ø A (includes Ø.12 A fan load)
	Ripple and noise	15Ø mV peak-to-peak (maximum) (see note)
	Total regulation	+5% to -5%
	Long term stability	Ø.1%/1ØØØ hr
	Overcurrent	No damage for any permanent overcurrent averaging 1.2 A or less, with peak current of 2 A or less in any 1Ø second period, or for a permanent short circuit (short circuit current specified as Ø.5 A maximum).

Table 9-3 Output Voltage Specifications (Cont)

Voltage	Specification	Value
+12 VB	Nominal output	+12 V
	Minimum load	Ø A
	Maximum load	2.35 A
	Ripple and noise	1ØØ mV peak-to-peak (maximum) (see note)
	Total regulation	-5% to +16.66% for Ø A to Ø.2 A, -5% to +5% for Ø.2 A to 2.35 A
	Long term stability	Ø.1%/1ØØØ hr
	Overcurrent	No damage for any permanent overcurrent averaging 2.8 A or less, with peak current of 3 A or less in any 1Ø second period, or for a permanent short circuit (short circuit current specified as 1 A maximum).
-12 V	Nominal output	-12 V
	Minimum load	Ø.Ø3 A
	Maximum load	Ø.3 A
	Ripple and noise	5Ø mV peak-to-peak (maximum) (see note)
	Total regulation	+5% to -5%
	Long term stability	Ø.1%/1ØØØ hr
	Overcurrent	No damage for any permanent overcurrent averaging Ø.5 A or less, with peak current of 2 A or less in any 1Ø second period, or for a permanent short circuit (short circuit current specified as 5ØØ mA maximum).

NOTE

Ripple and noise values are shown as measured with Tektronix P6Ø46 differential probe, with scope set for >1ØØ MHz bandwidth.

9.2.3 DC Power Input Connector (J1)

J1 provides dc input to the logic board. J1 connects with J2 of the PS1 via a ribbon cable (PN 17-00428-01). Figure 9-10 shows the connection between the logic board and the PS1, including pin-outs for both connectors.

9.2.4 +5 V Input Circuit

The +5 V input circuit develops all +5 V operating potential required by the logic board components from +5.1 V input originating at the PS1.

Figure 9-11 shows the components that make up the +5 V input circuit, as well as the various +5 V operating potentials developed by this circuit.

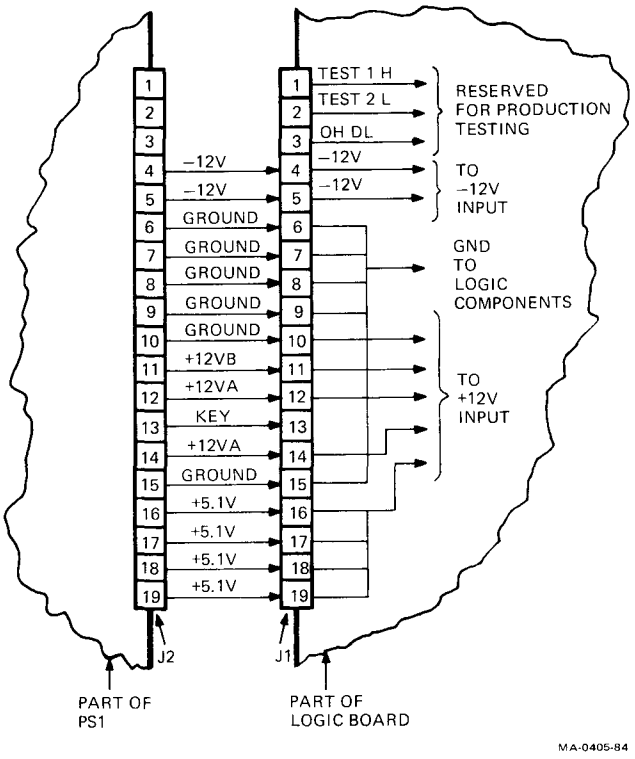


Figure 9-10 Logic Board DC Power Input Connector

9.2.5 +12 V Input Circuit

The +12 V input circuit develops all +12 V operating potential required by the logic board components, as well as the +12 V sent from the logic board to the keyboard module, from +12 V inputs originating at the PS1.

Figure 9-12 shows the components that make up the +12 V input circuit, as well as the two +12 V operating potentials developed by this circuit.

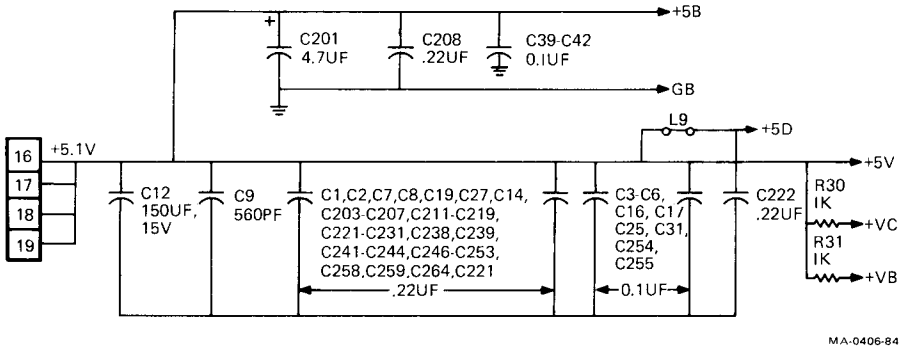


Figure 9-11 +5 V Input Circuit

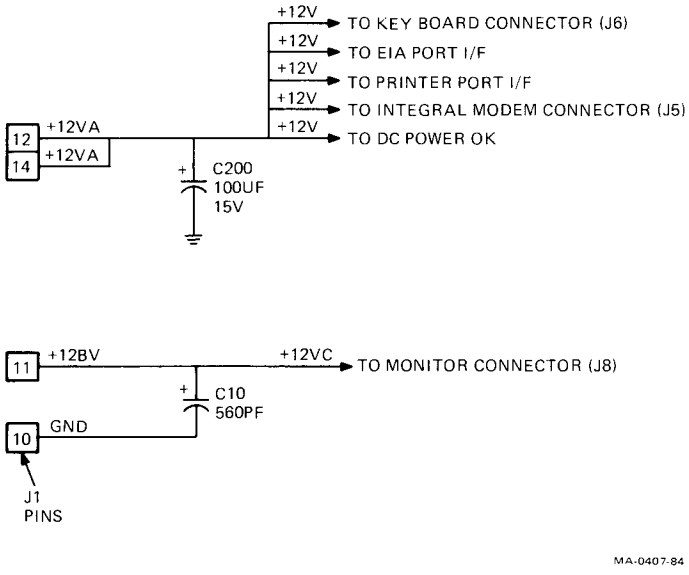


Figure 9-12 +12 V Input Circuit

9.2.6 -12 V Input Circuit

The -2 V input circuit develops the -12 V and -5.1 V operating potential required by the logic board components from -12 V input originating at the PS1.

Figure 9-13 shows the components that make up the -12 V input circuit, as well as the three operating potentials developed by this circuit.

9.2.7 DC Power Okay Circuit

The dc power Okay circuit provides visual indication of dc input to the logic board. Figure 9-14 shows that +5 V, +12 V, and -12 V potentials are applied as inputs to the dc power okay circuit. When all three inputs are present, Q2 is properly biased, and D2, a light emitting diode (LED), lights.

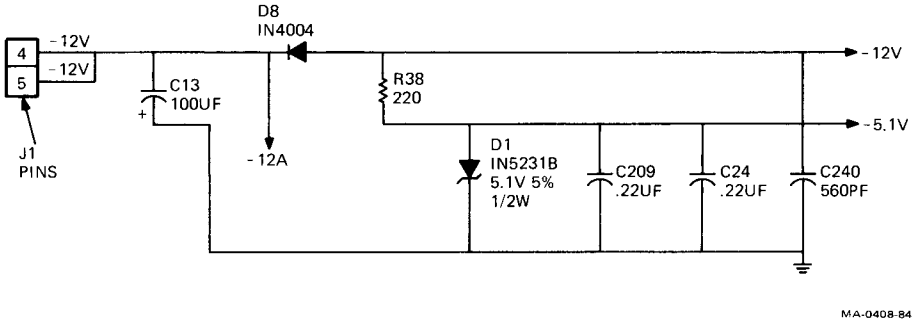


Figure 9-13 -12 V Input Circuit

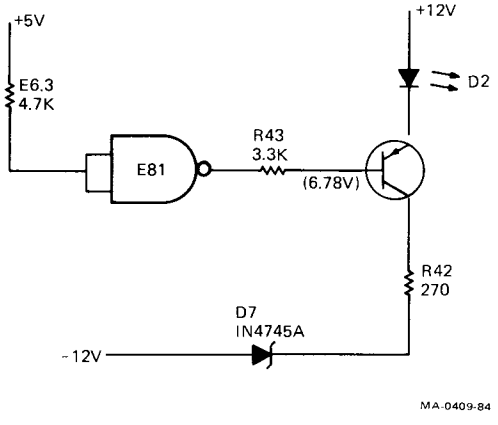


Figure 9-14 DC Power OK Circuit

CHAPTER 10
INTEGRAL MODEM OPTION

10.1 GENERAL

The Integral Modem/Auto Dialer option (shaded area in Figure 10-1) enables the same communications line to be used by a telephone for normal voice communication or by the VT240 terminal for data communication. Also, this option lets the user dial up a host computer by using the terminal keyboard instead of a telephone set.

The modem has three operating modes accessible through the VT240 terminal: data mode, talk mode, and dialer mode.

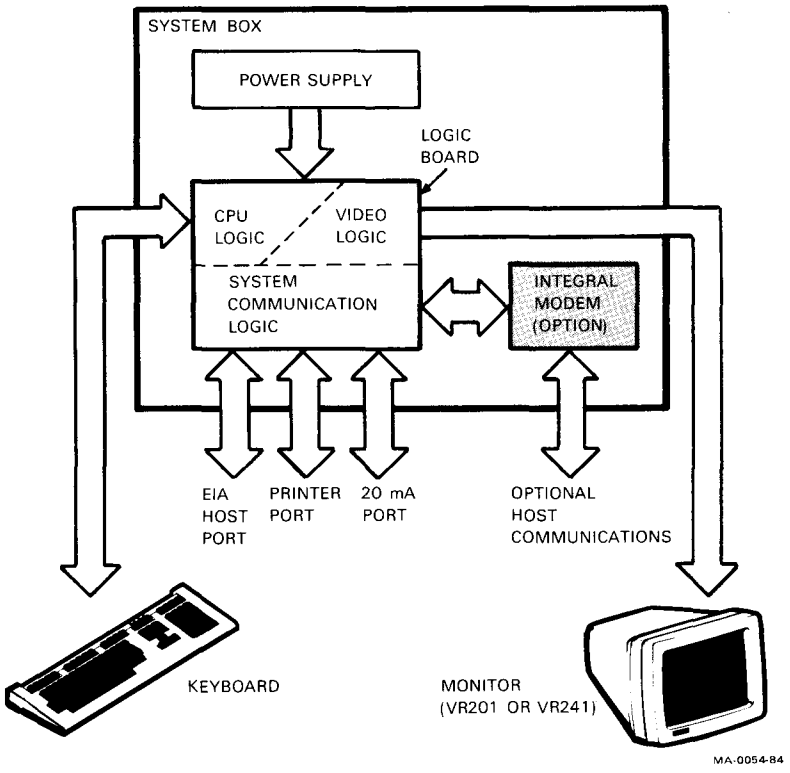


Figure 10-1 VT240-Series Terminal Block Diagram

DATA MODE
This mode sets the terminal for communicating data with the host computer. In this mode, you cannot use the telephone for voice communication.

TALK MODE
Talk mode allows you to use the telephone for normal voice communication.

DIALER MODE
This mode lets you:

- Use the keyboard to dial a telephone number
- Use a single keystroke to redial the last telephone number dialed
- Recall and dial stored telephone numbers

10.1.1 Compatibility and Features

The integral modem is operationally compatible with the following two devides.

- Bell 103J data set
- Bell 212A data set

The modem contains the following features.

- Direct connect telephone line interface
- Automatic answer
- Automatic originate (dialing)
- Test modes
- Speed control
- Keyboard control

10.1.2 Functional Description

The integral modem connects to the system communication logic on the system logic board. This modem is a full-duplex, asynchronous, binary serial data communications device. It is used to transmit and receive data over a two-wire switched telephone network (in compliance with FCC part 68) at 300 or 1200 bits per second. Low-speed operation (300 bps) is asynchronous, binary, and frequency shift keying (FSK). High-speed operation (1200 bps) is bit-synchronous (character-asynchronous) and quaternary differential phase shift keying (QDPSK).

10.1.3 Physical Description

The modem board is a 5.2 inch X 10 inch PC board that contains the modem and telephone line interface (TLI). The modem connects to the system logic board via a 30-pin stack connector (Figure 10-2). The telephone line and the telephone set connect to the TLI standard miniature telephone jacks.

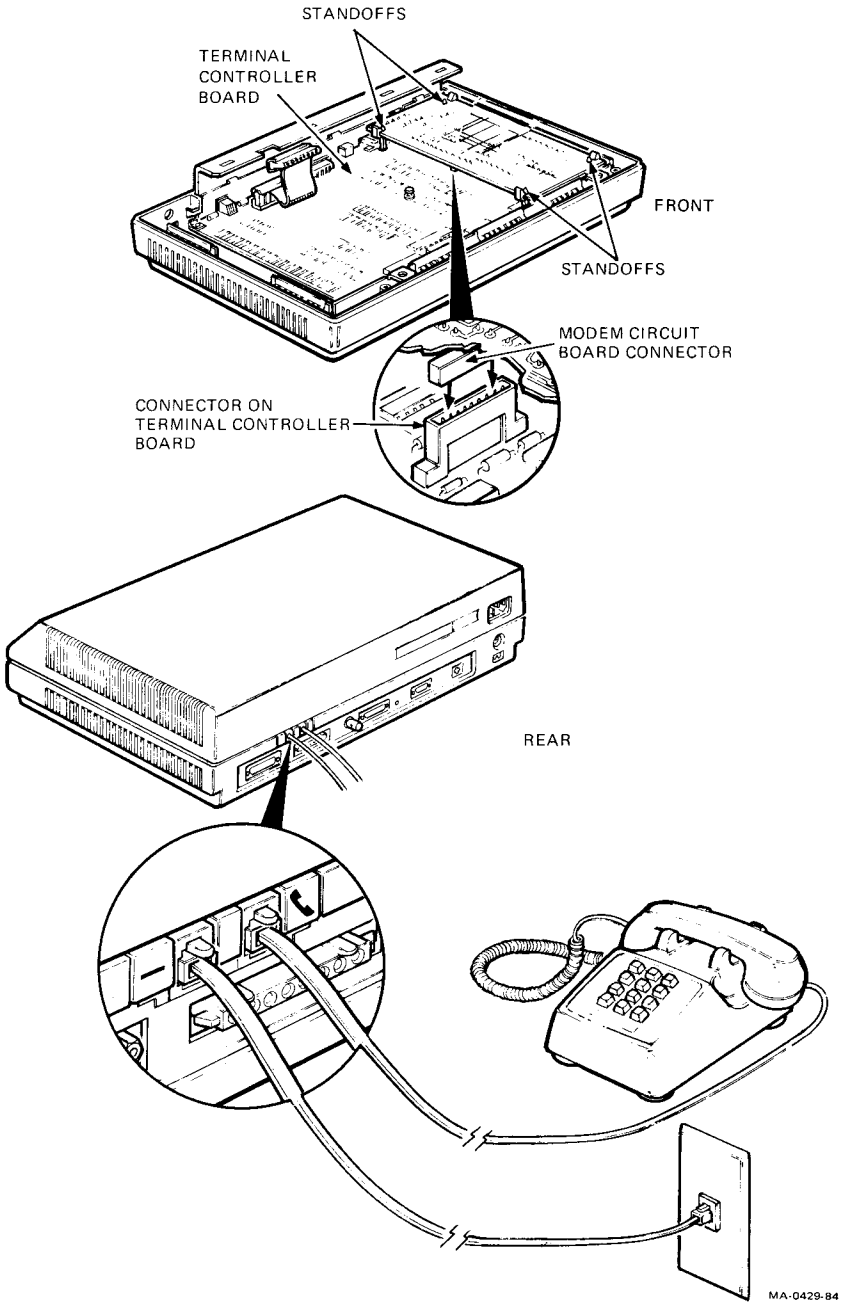


Figure 10-2 Physical Description

10.1.3.1 Power Requirements -- The Integral Modem option has the following voltage requirements.

+12 Vdc ±5% at 200 mA	100 mV peak-to-peak (maximum) ripple
-12 Vdc ±5% at 200 mA	100 mV peak-to-peak (maximum) ripple
+ 5 Vdc ±5% at 200 mA	50 mV peak-to-peak (maximum) ripple

10.1.3.2 Temperature and Humidity -- The Integral Modem option has the following temperature and humidity requirements.

Operating temperature	5o -- 50oC
Relative humidity	0% -- 95%

10.2 MAJOR CIRCUITS

The Integral Modem has the following major circuits (Figure 10-3).

- Talk/data relay
- Switch hook detector
- Ring detector
- Hook relay
- Line interface circuit
- Dial tone detect
- Audio coupler
- Master clock
- Modem control LSI chips

10.2.1 Talk/Data Relay Circuit

The talk/data relay circuit (Figure 10-4) connects the telephone line to either the handset or the modem. The position of the talk/data switch on the VT240 keyboard determines whether the handset or modem is connected. When the talk/data switch is pressed, the TALK/DATA signal is inverted and passed through the stack connector to the modem module.

When the TALK/DATA signal is low, the relay circuit is in talk mode. The telephone circuit's tip/ring leads connect to the telephone handset, and disconnects the modem. When the talk/data signal is high, the talk/data circuit is in data mode. The telephone circuit's tip/ring leads connect to the modem and the telephone handset is disconnected and unusable.

The TALK/DATA signal is inverted and becomes the output signal Talk. This signal is sent to the modem LSI circuit.

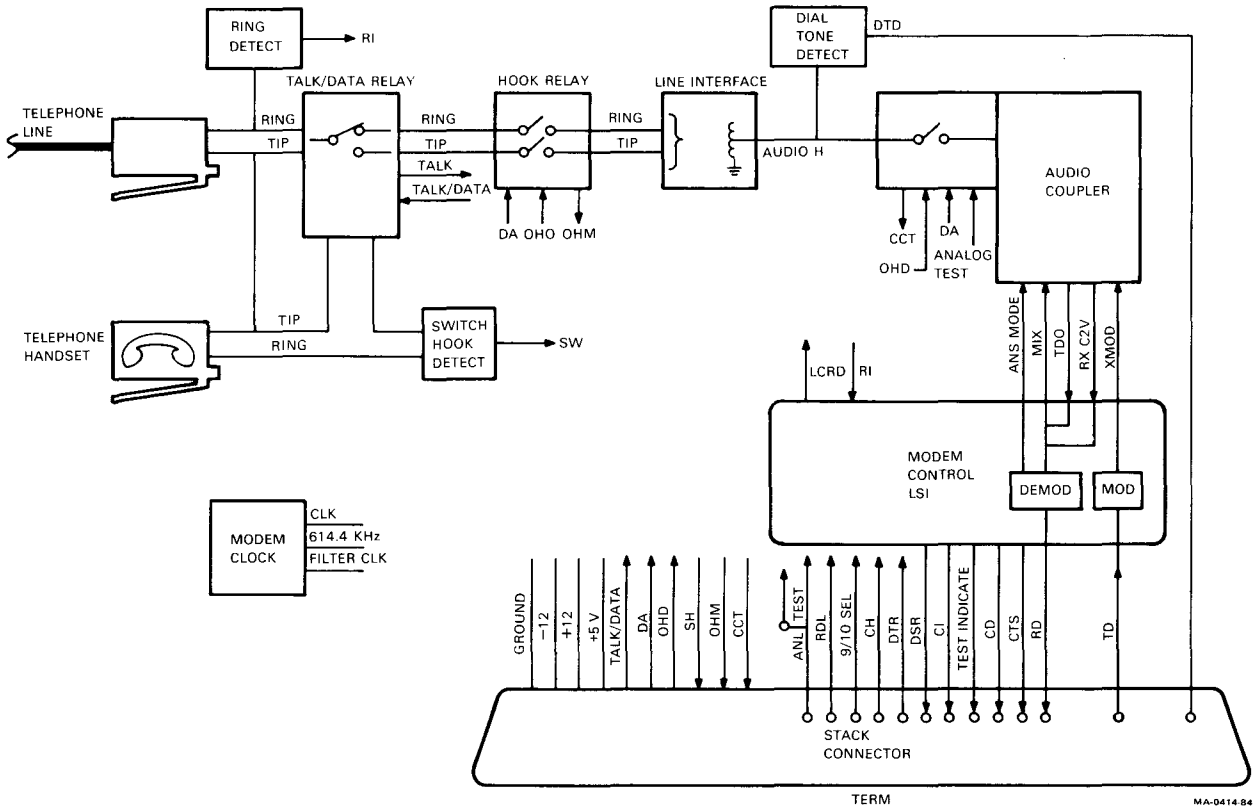


Figure 10-3 Block Diagram

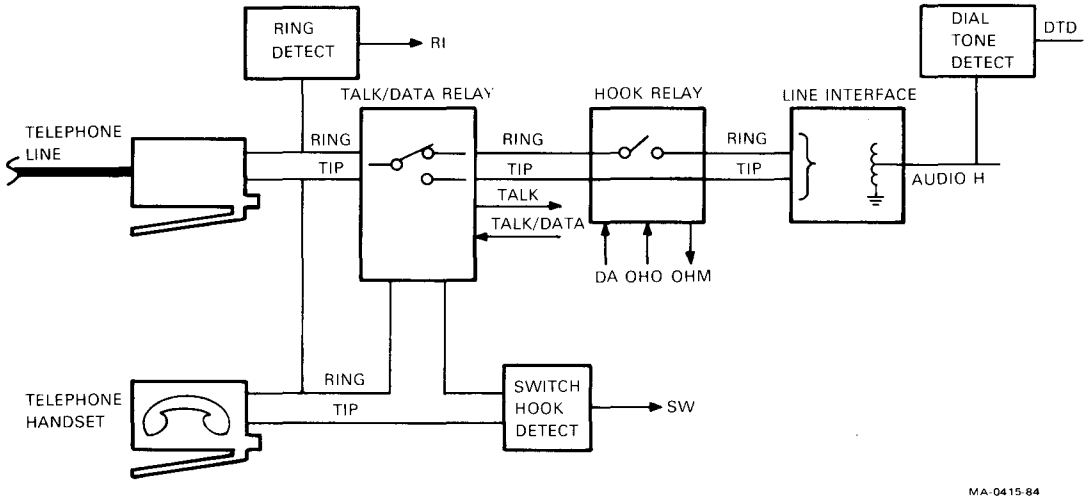


Figure 10-4 Talk/Data Relay

10.2.2 Switch Hook Detector Circuit

The Switch Hook Detector circuit (Figure 10-4) senses current flow in the telephone handset circuit and generates the signal SH. If the telephone handset is in the off-hook state, current will flow through the telephone tip/ring circuit. The off-hook current flow is detected by the switch hook detector and the SH signal is generated. This signal is passed to the modem control LSI circuit and also to the terminal (via the stack connector).

10.2.3 Ring Detector Circuit

The ring detector circuit (Figure 10-4) senses the high voltage, (20 Hz) ringing signal from the telephone circuit's tip lead and generates the ring indicate signal RI. The high voltage ringing signal is sampled from the tip lead. This lead is common to the telephone handset connector and the telephone line connector (RJ11). The RI signal is sent to the modem control LSI circuit.

The automatic answer mode is initiated when a valid RING signal is detected (assuming a DTR signal is also present).

10.2.4 Hook Relay Circuit

The hook relay circuit (Figure 10-4) connects the tip/ring leads from the talk/data relay to the protective circuit and is used to "pulse dial" the telephone system during the automatic dialing mode. The signal OHD is passed from the terminal through the stack connector, and operates the Hook Relay. The signal OH is inverted, becomes OHM, and is returned to the terminal through the stack connector.

During the pulsed dialing sequence, data from the terminal keyboard is pulse-formed by the terminal microcode. This generates the signal DA, data available.

10.2.5 Line Interface Circuit

The line interface circuit (Figure 10-4) terminates the telephone company's tip/ring circuit. It provides lightning protection and a full duplex interface between the coupler cut through (CCT) circuit and the telephone system. The protection circuit is used to transmit and receive frequency modulated multiplexed data signals. During auto answer mode, this circuit is the source for the dial tone signal for the modem.

Since the line interface circuit is full duplexed, it converts the telephone systems's tip/ring current loop signal to the hybrid ground reference signal (AUDIO H). It also converts the AUDIO H signal to the telephone system current loop standards.

10.2.6 Dial Tone Detect Circuit

When a 350 Hz dial tone is present on the AUDIO H line (Figure 10-4), the dial tone detect circuit outputs the signal DTD. This signal is passed to the terminal via the stack connector. The terminal's microcode senses the DTD signal, and during auto originate (AUTO-CALL) mode detects the presence of an available telephone line.

10.2.7 Audio Coupler Circuit

The audio coupler circuit contains the following elements (Figure 10-5).

- Hybrid amplifier
- High/low filter
- Filter circuit
- Coupler cut through relay
- Mix circuit
- Limiter amplifier threshhold detector

Hybrid Amplifier
The hybrid ampifier (IC E2) splits the signal AUDIO H into full-duplex transmit data (AUD XMIT), and receive data (FILTER A) channels.

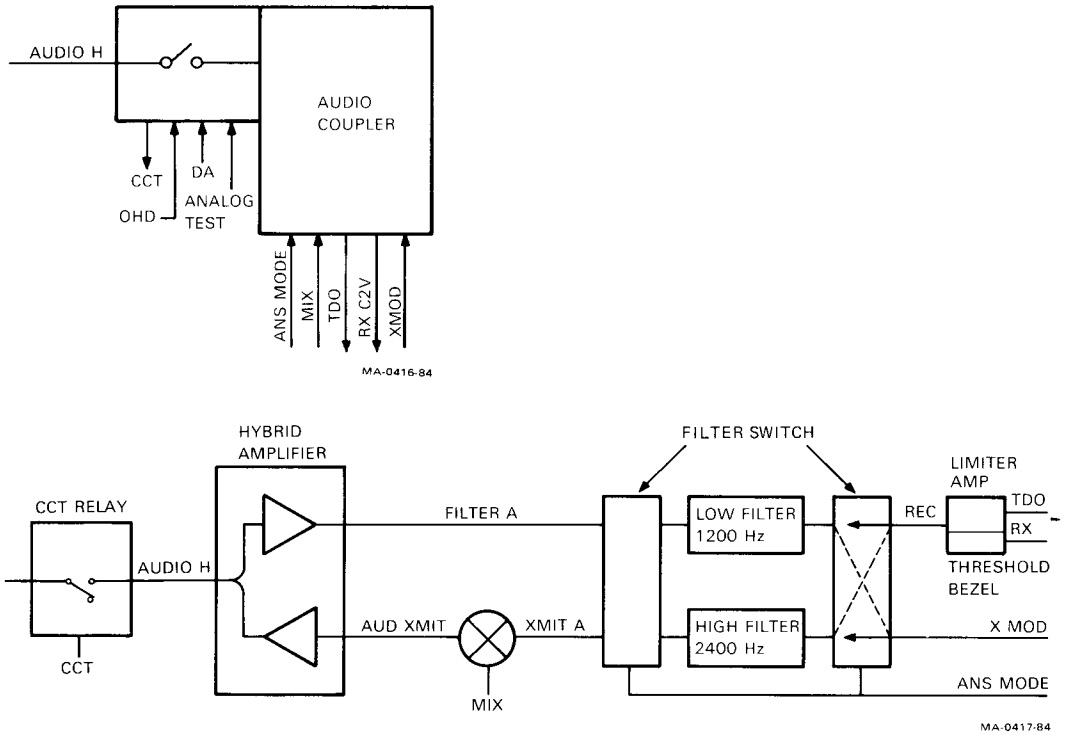


Figure 10-5 Audio Coupler

High/Low Filter

The high/low filter (IC E1Ø) is a combination high and low bandpass filter. The high bandpass frequency is 19ØØ to 29ØØ Hz with a center frequency of 24ØØ Hz. The low bandpass frequency is 7ØØ -- 17ØØ Hz, with a center frequency of 12ØØ Hz.

Filter Switch

The filter switch (IC E7) is an analog switch which reconfigures the high/low bandpass filter's inputs and outputs. The configuration of the bandpass filters depends on which of the following three possible modes the modem is in.

- **Orginate**
  When the modem is in the orginate mode (Figure 1Ø-6) , the transmit data signal (XMOD) has a carrier frequency in the 7ØØ to 17ØØ Hz range. The receive data signal (FILTER A) may have a carrier frequency of 19ØØ -- 29ØØ Hz. The filter input switch routes the XMOD signal into the low bandpass filter and outputs the signal XMIT A to the hybrid amplifier. The FILTER A signal is routed to the high bandpass filter and output as the signal REC.

- **Answer**
  When the modem is in the answer mode (Figure 1Ø-7), the transmit data signal (XMOD) has a carrier frequency in the 19ØØ -- 29ØØ Hz range. The receive data signal (FILTER A) has a carrier frequency in the 7ØØ -- 17ØØ Hz range. The filter input switch routes the XMOD signal into the high bandpass filter and outputs the signal XMIT A to the HYBRID amp. The FILTER A signal is routed to the low bandpass filter and output as the signal REC.

- **Loopback Test**
  When the modem is in the loopback test mode (Figure 1Ø-8), the data signal XMOD is passed through the low bandpass filter and inputs to the mix circuit. The mix circuit, when in the test mode, doubles the frequency of the XMIT A signal and is outputted as the signal AUD XMIT. The AUD XMIT signal loops back through the hybrid amplifier. AUD XMIT then is input to the high bandpass filter as receive data.

Coupler Cut Through Relay (CCT)

The coupler cut through relay circuit (Figure 1Ø-5) extends the AUDIO H signal path from the protective circuit to the audio coupler. The relay is open during test mode and when the modem is idle. The CCT relay is operated by the CCT signal. The CCT signal is generated when the DA and OHD signals are asserted from the terminal. CCT is sent to the terminal via the stack connector and is sensed by the terminal microcode.

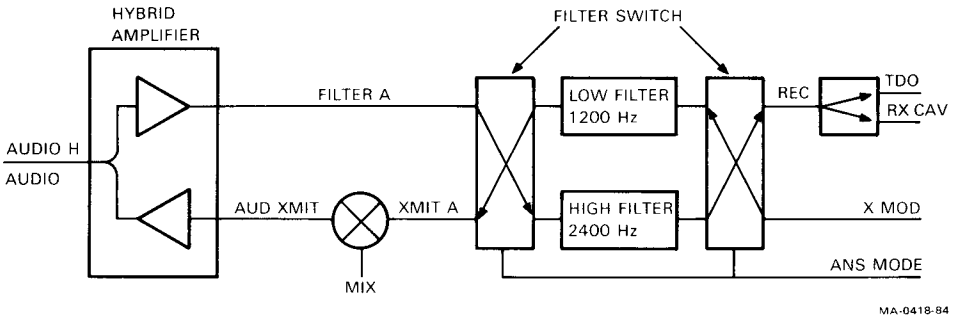


Figure 10-6 Originate Mode

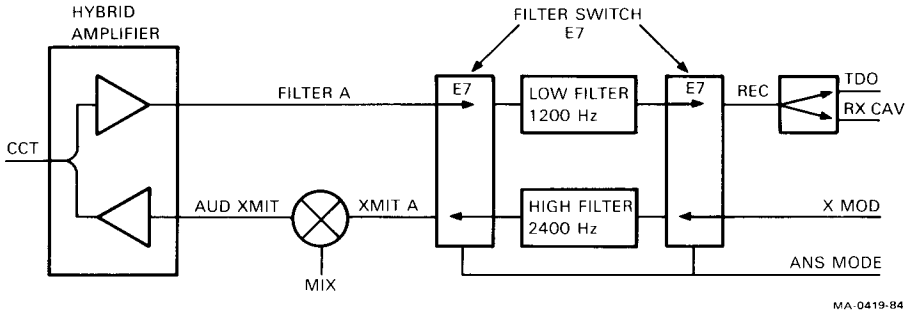


Figure 10-7 Answer Mode

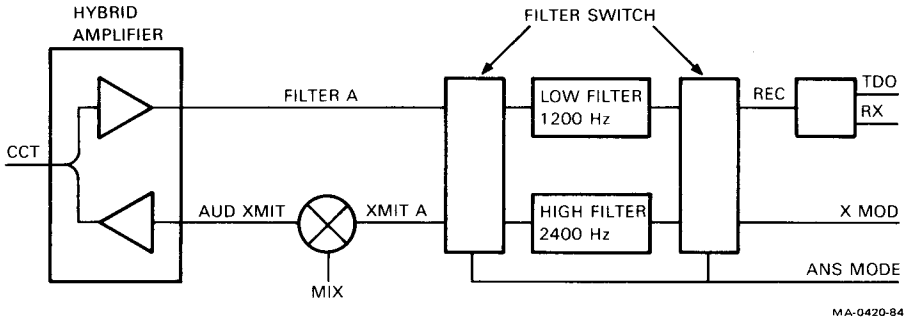


Figure 10-8 Test Mode

Mix Circuit

During normal operation the mix circuit (Figure 10-5) receives the transmit data signal XMIT A and outputs the AUD XMIT signal. In loopback test mode, the mix circuit doubles the frequency of the transmit data signal.

Limiter Amplifier Threshold Detector

The receive data signal REC is presented to a threshold and zero crossing detector (Figure 10-5), and output as the signals RX CAR and TD0.

10.2.8 Master Clock Circuit

The master clock circuit (Figure 10-9) consists of the components Y1 and E43. Y1 generates a square wave clock signal with a frequency of 4.9152 MHz which is then divided into the following four subfrequency signals.

CLOCK A
CLOCK B
FILTER CLOCK
614.4 kHz

10.2.9 Modem Control LSI Circuit

The modem control LSI circuit (Figure 10-10) consists of two large scale integration (LSI) chips that perform the following tasks.

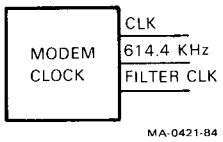


Figure 10-9 Modem Clock

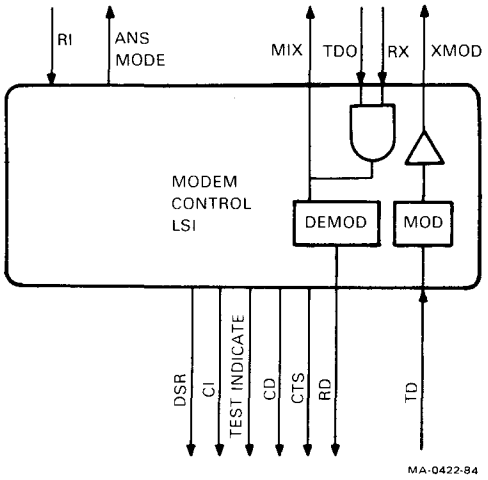


Figure 10-10 Modem Control LSI

Data Modulation/Demodulation
The data signal transmit data (TD) is received by the LSI chips from the terminal via the stack connector and outputs as the signals MOD1, MOD2, and MOD3 to the summing amplifier. The summing amplifier outputs the signal X MOD to the audio coupler. Received data is demodulated from the signals TDO and RX CARR and output to the terminal as the signal RD via the stack connector.

Modem Control and Configuration
The modem control circuit configures the modem for the desired mode and speed of operation: test mode, originate mode, and autoanswer mode. The signal data rate select (CH), is input from the terminal via the stack connector and causes the modem control LSI circuit to set the high or low speed originate mode. If the modem is in the autoanswer mode, the modem control LSI circuit self-configures the modem to the speed of the remote modem. The signal speed mode indication (CI) is output to the terminal via the stack connector and detected by the terminal's microcode.

Modem Control Signal Generator
The circuit also detects the presence of a valid received data carrier and inputs the signal carrier detect (CD) back to the terminal. The circuit generates the control signals CTS and DSR. These signals are sent to the terminal. The input control signals DTR, 9/10 SELECT, and CH are received from the terminal. These signals inform the modem control LSI circuit of the bit count of the transmitted data byte. This is necessary for the transmission of high speed QDPSK di-bits.

10.3 TERMINAL INTERFACE SIGNAL DESCRIPTION

The interface signals are those signals transmitted through the 30-pin stack connector, either from the system logic board to the modem, or from the modem to the system logic board (Figure 10-11).

NOTE
The signal states and impedances for the interface circuits are in accordance with TTL low power Schottky specifications.

Output high level	2.4 V minimum 5.25 V maximum
Output low level	0.4 V maximum
Output low current sink	8.0 mA maximum
Output high current source	400 mA maximum
Input low level	0.8 V maximum
Input high level	2.0 V minimum
Input high current	0.1 mA maximum
Input low current source	0.4 mA maximum

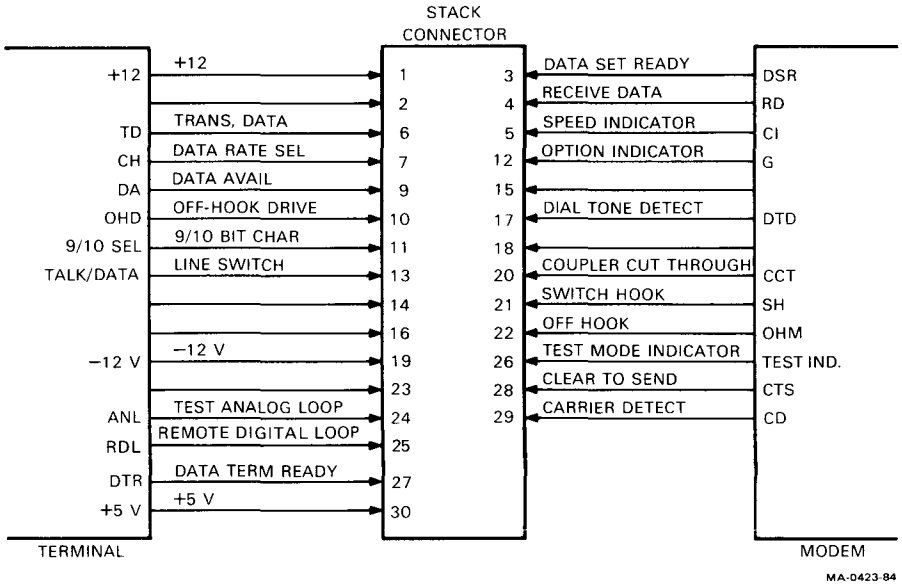


Figure 10-11 Stack Connector

10.3.1 Signal States

Table 10-1 shows the active and initialized states of the interface signals.

The transmitted and received data signals are considered in the marking state when the circuit voltage is more positive than +2 V with respect to signal ground, and in the spacing condition when the voltage on the circuit is more negative than +2 V with respect to signal ground. The signal is considered off when it is more positive than +0.8 V with respect to signal ground.

State	Voltage
Marking	> +2 V
Spacing	< +2 V
Off	> +.8 V

10.3.2 Interface Signals

The following sections describe the interface signals.

10.3.2.1 Transmitted Data (TD) -- Signals on this circuit are generated by the terminal and transmitted to the modem. A positive voltage signal is considered a binary one (or mark) condition. A zero voltage signal is considered a binary zero (or space) condition. The transmitting terminal holds this circuit in the mark state when no data is being transmitted. This is true during intervals between characters and words as well.

Table 10-1 Interface Signal Levels

Pin	Name	Description	Source	Active Level	Initialized Level
1	+12 V	Voltage	Term	--	--
2	--	--	--	--	--
3	DSR	Data set ready	Modem	Low	High
4	RD	Receive data	Modem	Low=space	High
5	CI	Speed indicator	Modem	Low=1200 bps	--
6	TD	Transmit data	Term	Low=space	High
7	CH	Data rate select	Term	High=1200 bps	High
8	GND	Voltage	--	--	--
9	DA	Data available	Term	Low=CCT	High
10	OHD	Off hook--drive	Term	Low=OH relay	High
11	9/10.SEL	9 or 10 bit char C	Term	Low=10 bit	Low
12	G	Option indication	Modem	--	--
13	TALK/DATA	Line switch	Term	Low=data	High talk
14	--	--	--	--	--
15	--	--	--	--	--
16	--	--	--	--	--
17	DTD	Dial tone detect	Modem	H=Active	--
18	Hybrid Out	Reserved	Modem	--	--
19	12 V	Voltage	Term	--	--
20	CCT	Coupler cut through	Modem	L=Attached	--
21	SH	Switch hook	Modem	L=Line Current	--
22	OHM	Off hook	Modem	L=Off hook	--
23	--	--	--	--	--
24	ANL	Test analog loop	Term	H+Test	Low
25	RDL	Remote digital loop	Term	H-Test	Low
26	Test Ind	Test mode indicator	Modem	L=Test	--
27	DTR	Date term ready	Term	L=On	--
28	CTS	Clear to send	Modem	L=On	--
29	CD	Carrier detect	Modem	L=On	--
30	+5 V	Voltage	Term	--	--

10.3.2.2 Received Data (RD) -- Signals on this circuit are generated by the demodulator in response to telephone line signals. The received data circuit is clamped to the marking state whenever the interface circuit carrier detector (CD) is idle.

10.3.2.3 Clear to Send (CTS) -- An on condition of the clear to send circuit indicates to the terminal that the modem transmits any signal present on the transmit data (TD) circuit. If CTS is off, the modem internally clamps transmit data to the mark condition and ignores the TD circuit. If a remote digital loop is initiated, the local CTS circuit turns off until the remote modem is in the digital loop test mode.

10.3.2.4 Data Set Ready (DSR) -- This signal originates in the modem to indicate its status. The on condition indicates the modem is in the data mode and is connected to the communication channel (or is in analog loop test mode). The on condition does not mean that a communication channel has been completely established, however.

10.3.2.5 Signal and Power Ground -- This circuit establishes a common ground reference for interface circuits and dc power.

10.3.2.6 Carrier Detect (CD) -- Carrier detector on indicates that a data carrier is being received and has been received for at least 155 milliseconds. This circuit differentiates a good data carrier from message circuit noise or out-of-band signals. This circuit turns off if the received data is clamped to the marking state.

10.3.2.7 Speed Indication (CI) -- This circuit is on when the modem is in the high-speed data mode (or the high-speed analog loop test mode). At all other times the circuit is in the off state.

Since an answering modem automatically adapts to the speed of the originating station, it ignores its own speed selector. In this case, the speed selector and the speed mode circuit will not match.

10.3.2.8 Data Terminal Ready (DTR) -- This circuit provides a means for the terminal to control the connection of the modem to the communication channel (and to control the analog loop test mode). The on condition is required to maintain a connection to the communication channel. The on condition must also be present to enter the data mode, either manually or automatically. If this circuit is off for more than 50 milliseconds during a data call, a disconnect sequence is initiated.

For automatic answering applications, the presence of an off condition on this circuit does not inhibit the operation of the ring indication (RI) circuit. This circuit (DTR) must be turned on to automatically answer an incoming call.

For the analog loop test mode, this signal must be on at the same time with the analog loop (ANL) signal.

10.3.2.9 Data Rate (Speed) Select (CH) -- This signal enables the terminal to select high-speed mode (1200 bits per second), or low-speed mode (300 bits-per-second) via the modem A/B speed mode circuit.

10.3.2.10 Dial Tone Detect (DTD) -- This signal is generated by the modem whenever the phone line is ready for dialing (dial tone) after off hook. The terminal checks this condition before dialing.

10.3.2.11 Line Switch (Talk/Data) -- This signal is generated by the terminal's firmware and is activated by a dedicated keyboard switch. This signals talk mode or data mode to the modem.

10.3.2.12 Data Available (DA) -- This signal is generated by the terminal to request a data transmission path cut through. For pulse dialing, the terminal disables the DA signal after detecting a dial tone before generating the dial pulses corresponding to the called number.

10.3.2.13 Off Hook Drive (OH-D) -- The terminal generates this signal to drive the off hook relay. When the signal is low, the relay is on.

10.3.2.14 9 or 10 Bit Character (9/10 SEL) -- This signal is generated by the terminal to select 9 or 10 bits-per-character mode. A low signal indicates 10-bit mode.

10.3.2.15 Coupler Cut Through (CCT) -- The modem generates this signal after off hook. It indicates that the audio path to the telephone line is ready.

10.3.2.16 Switch Hook (SW) -- The modem uses this signal to indicate to the terminal the status of the switch hook.

10.3.2.17 Off Hook Modem (OH-M) -- The modem uses this signal to indicate to the terminal that it (the modem) is "off the hook".

10.3.2.18 Analog Loop Test (ANL) -- This interface signal tests modem A by forcing the transmitter (modulator) and receiver (demodulator) into the same mode. This allows data from the terminal to loop through the modem and back for a local modem test.

10.3.2.19 Remote Data Loopback Test (RDL) -- This interface signal causes the local 212A modem to put the remote 212A modem into a data loop. Data from the terminal is then transmitted from the local modem to the remote modem and back again, thus checking the local and remote modems and the line.

10.3.2.20 Test Mode Indicate (Test IND) -- The modem generates this signal whenever it is in the test mode.

APPENDIX A
SPECIFICATIONS

GENERAL

This appendix lists the VT240/VT241 video terminals specifications.

Physical

System box	Height: 10.2 cm (4 in) Width: 45.7 cm (18 in) Depth: 30.5 cm (12 in) Weight: 7.2 Kg (16 lbs)
Keyboard	Height: 5.1 cm (2.0 in) Width: 53.3 cm (21.0 in) Depth: 17.1 cm (6.75 in) Weight: 2.0 kg (4.5 lbs)
Monochrome monitor	Height: 29.2 cm (11.5 in) Width: 34.9 cm (13.75 in) Depth: 31.1 cm (12.25 in) Weight: 6.4 kg (14 lb) Adjustable Tilt: $+5^{\circ}$ -- -25°
Color monitor	Height: 32.4 cm (12.75 in) Width: 38.0 cm (15 in) Depth: 42.1 cm (17.0 in) Weight: 16.6 kg (36.6 lb)

Environmental

Operating	Temperature: 10° -- 40°C (50° -- 104°F) Relative Humidity: 10% -- 90% Maximum Wet Bulb: 28°C (82°F) Minimum Dew Point: 2°C (36°F) Maximum Altitude: 2.4 km (8000 ft)
Storage	Temperature: -40° -- 66°C (140° -- 151°F) Relative Humidity: 0% -- 95% Maximum Altitude: 9.1 km (30000 ft)

Electrical

Line voltage (switch selectable)	90 -- 128 Vac (100 -- 120 RMS nominal) single-phase, 3-wire
	180 -- 268 Vac (220 -- 240 RMS nominal) single-phase, 3-wire
Line frequency	47 -- 63 Hz
Power cord	Detachable, 3-conductor, grounded

Display

Format	24 lines X 80 characters or 24 lines X 132 characters
Character	7 X 9 dot matrix in 10 X 10 cell for 80 columns
	5 X 9 dot matrix in 6 X 10 cell for 132 columns
Character size	3.35 mm X 2.0 mm for 80 columns
	3.35 mm X 1.3 mm for 132 columns
Active display size	202 mm X 115 mm (8 X 5 in)
Character set	ASCII, DEC Supplemental, Special Graghics, UK, loadable 80 or 132 column font
	Control characters (using control representation mode) 80-column font only
Character attributes	Reverse video, underline, bold, blinking (maximum of 100 characters), alternate character ROM
Cursor Type	Blinking block cursor or blinking underline cursor

Keyboard Characteristics

General	105 key detachable unit with a 1.9 m (6.0 ft) coiled cord with a 4-pin telephone-type modular connector. Word processing and data processing versions are available in 15 languages.
Keypad	Sculptured key array, matte texture finish keys, home row key height is 30mm (1.18 in) above desk top
Key Size	1.27 cm (0.5 in) square
Key Spacing	1.9 cm (0.75 in) center-to-center (single-width keys)
Numeric keypad	18 keys
Function keys	36 keys, firmware and software driven
Visual indicators	4 LED indicators: hold, lock, wait, and compose
Audible signals	Keyclick: provides audible feedback for each keystroke. Bell: sounds when BEL character is received, when approaching right margin, and for compose errors. Multiple Bell: sounds on error in set-up save or recall operation.

APPENDIX B
VT240/VT102 DIFFERENCES

This appendix describes the major differences between a VT102 terminal and the VT240 terminal operating in a VT100 mode.

Feature	VT102	VT240
LEDs	Programmable	Not programmable
Alternate character ROM	Socket for OEM supplied character ROM	Down-line loadable character set
Screen freeze	NO SCROLL key	HOLD SCREEN key
Printer port connector	25 pin	9 pin
Screen refresh	50/60 Hz	60 Hz only
Set-up	Display in English only	Display in three languages, and display does not affect software
RIS function	Performs power-up self-test	Does not perform power-up self-test
132 Column font horizontal resolution	7 pixels with 2 pixels between characters	5 pixels with 1 pixel between characters
Off-line/local	Off line mode disconnects modem	Local mode does not disconnect modem

Feature	VT102	VT240
Communication	Full-duplex and half-duplex mode	Full-duplex mode only, and does not affect software
	Transmit speed limitation of 60 characters-per-second, regardless of baud rate	Optional transmit speed limitation of 150 characters-per-second
	Selectable passive or active 20 mA	Passive 20 mA only
Terminal IDs	ESC [? 6 c	CSI ? 62; 1;2;3;4;6;7;8 c (primary) CSI > 2;Pv;Po c (secondary)

APPENDIX C
VT240/VT125 DIFFERENCES

This appendix describes the functional differences between a VT125 terminal and a VT240 terminal operating in a ReGIS graphics mode.

Difference Area	VT125	VT240
Screen size (displayed pixels)	768 X 240 displayed pixels	800 X 240 displayed pixels
Screen clipping	Pixels outside defined screen addressing range but inside visible screen are drawable	Pixels outside defined screen addressing range but inside visible screen are not drawable (clipped)
Offscreen bit-map memory	Offscreen memory for graphics	No offscreen memory for graphics
Screen addressing (picture aspect ratio)	Scales X and Y directions independently when mapping	Maintains picture aspect ratio when mapping
Screen addressing (integral scaling)	Uses integral divisions to map screen addressing range to physical pixels	General scaling algorithm for mapping screen addressing range to physical pixels
Screen addressing (decimal fractions)	Ignores digits after a decimal point in screen addressing parameters and coordinates	Fractional digits significant in screen addressing parameters and coordinates
Screen scaling (zoom)	Supports screen scaling	Does not support scaling

Difference Area	VT125	VT240
Screen offset	Images moved off screen eventually wrap back	Images moved off screen are lost
	Allows offset on single-pixel boundaries horizontally and vertically	Scrolls image on 16-pixel boundaries horizontally, and single-pixel boundaries vertically
	When image is moved origin moves with image	When image is moved origin remains fixed at point defined by screen addressing command
Shading	Shading to horizontal base line only	Shading to horizontal and vertical baseline
Character shading	Uses italic attribute when drawing shaded area with character fill	Does not use italic attribute when drawing shaded area with character fill
Size of position stack	10 entries	32 entries
		Images that rely on on position stack overflow at eleventh entry may not execute on VT240
		Stack underflow and overflow are reportable errors
Writing controls	Custom writing control command ReGIS W(W)	Default writing mode
Graphics text	Zero character is slashed	Zero character is not slashed

Difference Area	VT125	VT240
Image control on optional external monitor	Provides for: • Optional external monitor on which same image is displayed • Optional external monitor on which only graphics image (no text image) is displayed (can be controlled separately)	Provides only for optional external monitor on which same image is displayed as on standard monitor
VT105 emulation	Yes	No
ANSI text and graphics	Can scroll text over graphics	Text and graphics must scroll together
Display ReGIS	Graphics images and ReGIS commands used to generate them can appear simultaneously on entire screen	ReGIS commands used to display graphics images appear on line 24 of screen
Overlaying text and graphics	Text can overlay graphics in same display region	Text drawn in display region as graphics replaces graphics image
Erasing command	Erases text and graphics separately	Erases text and graphics at same time
Changing output	Changes only presentation of graphics image	Changes presentation map of text as well as graphics image
Terminal IDs	ESC [? 12;Pvt00;Pf;Pvc	CSI ? 62;1;2;3;4;6;7;8 c (primary) CSI > 2;Pv;Po c (secondary)

APPENDIX D
REGISTER BIT VALUES

171000 (WR)

07	06	05	04	03	02	01	00
S1	S2	EP	PEN	L2	L1	B2	B1

(RDA7 H) ◄——————————————————► (RDA0 H)

NOTE
FOLLOWING A POWER UP SEQUENCE, OR AN INTERNAL RESET CONDITION IN THE 8251A, THE 8251A MUST FIRST BE PROGRAMMED FOR MODE OF OPERATION, AND THEN FOR COMMAND INFORMATION, WITH BOTH ACTIONS OCCURRING AT ADDRESS 172000.

BIT VALUES		
BIT 6–7	00	INVALID
	10	1 STOP BIT PER TRANSMIT CHARACTER
	01	1½ STOP BITS PER TRANSMIT CHARACTER
	11	2 STOP BITS PER TRANSMIT CHARACTER
BIT 5	0	ODD PARITY GENERATION CHECK
	1	EVEN PARITY GENERATION CHECK
BIT 4	0	PARITY DISABLED
	1	PARITY ENABLED
BIT 2–3	00	5 BITS PER CHARACTER
	10	6 BITS PER CHARACTER
	01	7 BITS PER CHARACTER
	11	8 BITS PER CHARACTER
BIT 0–1	00	SYNC MODE
	10	BAUD RATE FACTOR OF 1X
	01	BAUD RATE FACTOR OF 16X
	11	BAUD RATE FACTOR OF 64X

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Figure D-1 8251A USART: Command Register (Mode Instruction Format, Asynchronous Mode)

171000 (WR)

07	06	05	04	03	02	01	00
EH	IR	RTS	ER	SBRK	RxE	DTR	TxEN

(RDA7 H) ◄——————————————————► (RDA0 H)

NOTE
FOLLOWING A POWER UP SEQUENCE, OR AN INTERNAL RESET CONDITION IN THE 8251A, THE 8251A MUST FIRST BE PROGRAMMED FOR MODE OF OPERATION, AND THEN FOR COMMAND INFORMATION, WITH BOTH ACTIONS OCCURRING AT ADDRESS 172000.

BIT VALUES		
BIT 7	0	DISABLE SEARCH FOR SYNC CHARACTERS
	1	SEARCH FOR SYNC (NO EFFECT IN ASYNC)
BIT 6	0	INACTIVE
	1	INTERNAL RESET
BIT 5	–	NOT USED
BIT 4	0	INACTIVE
	1	RESET ERROR FLAGS
BIT 3	0	NORMAL OPERATION
	1	FORCE TxD CONSTANT LOW
BIT 2	0	RECEIVE ENABLE DISABLED
	1	RECEIVE ENABLE ENABLED
BIT 1	0	DTR DISABLED
	1	DTR FORCED LOW (GENERATING LPBK EN L)
BIT 0	0	TRANSMIT ENABLE DISABLED
	1	TRANSMIT ENABLE ENABLED

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Figure D-2 8251A USART: Command Register (Command Data Format)

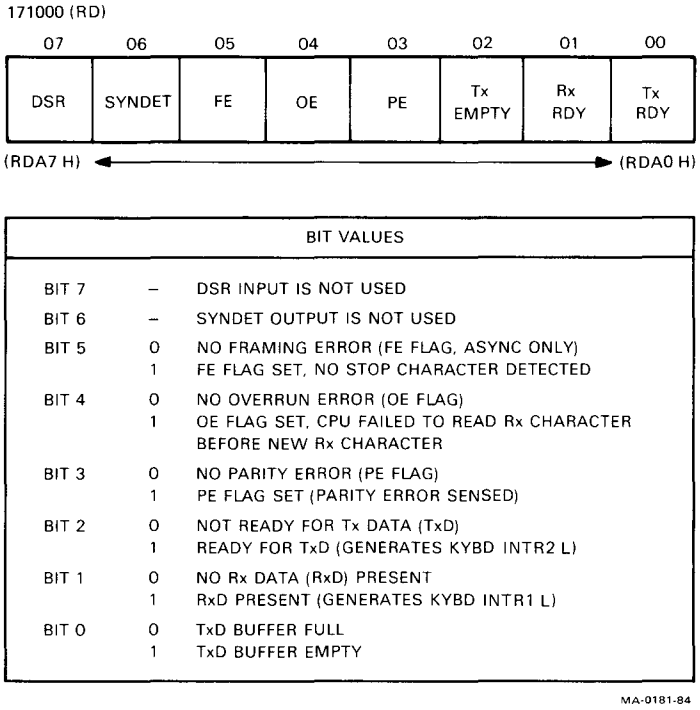
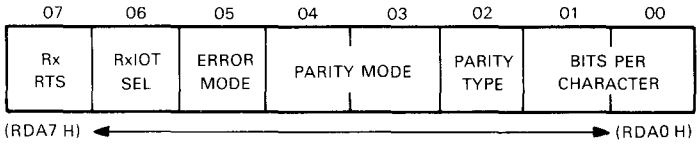


Figure D-3 8251A USART: Status Register

(MR1A) ADDRESS 172000(RD)/172002(WR)
(MR1B) ADDRESS 172040(RD)/172042(WR)



BIT VALUES		
BIT 7	0	RxRTS DISABLED
	1	RxRTS ENABLED
BIT 6	0	INTERRUPT ON RxRDY
	1	INTERRUPT ON FFULL
BIT 5	0	CHARACTER ERROR MODE
	1	BLOCK ERROR MODE
BIT 3–4	00	WITH PARITY
	01	FORCE PARITY
	10	NO PARITY
	11	SPECIAL MODE
BIT 2	0	EVEN PARITY
	1	ODD PARITY
BIT 0–1	00	5 BITS PER CHARACTER
	01	6 BITS PER CHARACTER
	10	7 BITS PER CHARACTER
	11	8 BITS PER CHARACTER

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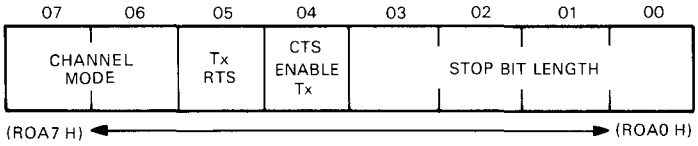
Figure D-4 2681 DUART: Mode Register 1 (MR1) (Channel A and B)

(MR2A) ADDRESS 172000(RD)/172002(WR)
(MR2B) ADDRESS 172040(RD)/172042(WR)



BIT VALUES		
BIT 6–7	00	NORMAL MODE
	01	AUTO ECHO MODE
	10	LOCAL LOOP MODE
	11	REMOTE LOOP MODE
BIT 5	0	TxRTS DISABLED
	1	TxRTS ENABLED
BIT 4	0	NO CTS REQUIRED FOR Tx
	1	CTS REQUIRED FOR Tx
BIT 0–3	0000*	0.563 BIT STOP CHARACTER
	0001*	0.625 BIT STOP CHARACTER
	0010*	0.688 BIT STOP CHARACTER
	0011*	0.750 BIT STOP CHARACTER
	0100*	0.813 BIT STOP CHARACTER
	0101*	0.875 BIT STOP CHARACTER
	0110*	0.938 BIT STOP CHARACTER
	0111*	1.000 BIT STOP CHARACTER
	1000	1.563 BIT STOP CHARACTER
	1001	1.625 BIT STOP CHARACTER
	1010	1.688 BIT STOP CHARACTER
	1011	1.750 BIT STOP CHARACTER
	1100	1.813 BIT STOP CHARACTER
	1101	1.875 BIT STOP CHARACTER
	1110	1.938 BIT STOP CHARACTER
	1111	2.000 BIT STOP CHARACTER

* ADD .5 BIT FOR 5 BITS PER CHARACTER OPERATION

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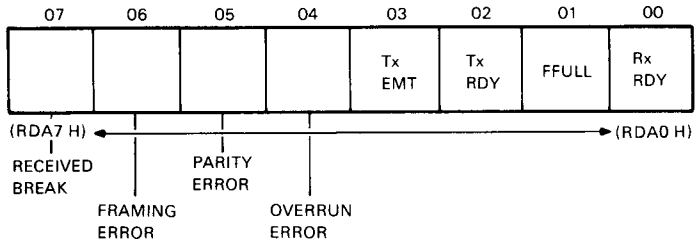
Figure D-5 2681 DUART: Mode Register 2 (MR2) (Channel A and B)

(SRA) ADDRESS 172004(RD)
(SRB) ADDRESS 172044(RD)



BIT VALUES		
BIT 7	0	NO BREAK DETECTED
	1	RECEIVE BREAK DETECTED
BIT 6	0	NO ERROR
	1	FRAMING ERROR
BIT 5	0	NO ERROR
	1	PARITY ERROR
BIT 4	0	NO ERROR
	1	OVERRUN ERROR
BIT 3	0	Tx NOT EMPTY
	1	Tx HOLDING AND SHIFT REGISTERS EMPTY
BIT 2	0	Tx HOLDING REGISTER FULL
	1	Tx HOLDING REGISTER EMPTY
BIT 1	0	Rx FIFO NOT FULL
	1	Rx FIFO FULL
BIT 0	0	NO Rx DATA WAITING
	1	Rx DATA IN FIFO

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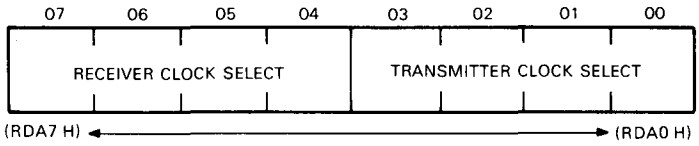
Figure D-6 2681 DUART: Status Register (SR) (Channel A and B)

DCSRA ADDRESS 172006 (WR)
DCSRB ADDRESS 172046 (WR)



BIT VALUES		
BIT 0–3 OR 4–7	BAUD RATE SET 1	BAUD RATE SET 2
0000	50	75
0001	110	110
0010	134.5	134.5
0011	200	150
0100	300	300
0101	1200	1200
0110	1050	2000
0111	2400	2400
1000	4800	4800
1001	7200	1800
1010	9600	9600
1100	38.4K	19.2K
1101	TIMER	TIMER
1110	IP4-16X(RxCA)	IP4-16X(RxCA)
1110	IP6-16X(RxCB)	IP6-16X(RxCB)
1110	IP3-16X(TxCA)	IP3-16X(TxCA)
1110	IP5-16X(TxCB)	IP5-16X(TxCB)
1111	IP4-1X(RxCA)	IP4-1X(RxCA)
1111	IP6-1X(RxCB)	IP6-1X(RxCB)
1111	IP3-1X(TxCA)	IP3-1X(TxCA)
1111	IP5-1X(TxCB)	IP5-1X(TxCB)

NOTES

1. RxC AND TxC ARE ALWAYS 16X EXCEPT FOR 1111 CONDITION;
2. SET SELECTION MADE BY ACR BIT 7.

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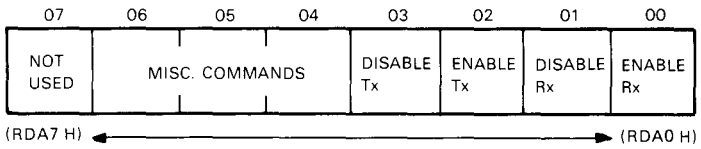
Figure D-7 2681 DUART: Data Clock Selection Register (DCSR) (Channel A and B)

(CRA) ADDRESS 172012(WR)
(CRB) ADDRESS 172052(WR)



BIT VALUES		
BIT 7	–	ALWAYS 0
BIT 4–6	000	NOT USED
	001	RESET MODE REGISTER (MR) POINTER
	010	RESET Rx
	011	RESET Tx
	100	RESET ERROR STATUS
	101	RESET CHANNEL BREAK CHANGE INTERRUPT
	110	START BREAK
	111	STOP BREAK
BIT 3	0	NO COMMAND
	1	TERMINATE Tx AND RESET TxRDY AND TxEMT STATUS BITS
BIT 2	0	DISABLE Tx
	1	ENABLE Tx
BIT 1	0	NO COMMAND
	1	TERMINATE Rx IMMEDIATELY
BIT 0	0	DISABLE Rx
	1	ENABLE Rx

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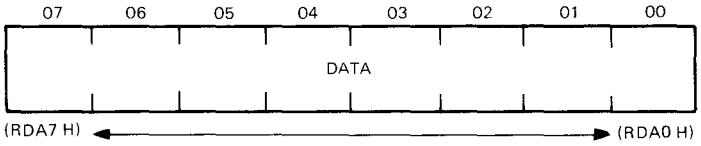
Figure D-8 2681 DUART: Command Register (CR) (Channel A and B)

(RDRA) ADDRESS 172014(RD)
(RDRB) ADDRESS 172056(RD)
(TDRA) ADDRESS 172016(WR)
(TDRB) ADDRESS 172060(WR)



BIT VALUES		
BIT 0–7	–	DATA RECEIVED FROM HOST (RDRA) DATA RECEIVED FROM PRINTER (RDRB) DATA TO TRANSMIT TO HOST (TDRA) DATA TO TRANSMIT TO PRINTER (TDRB)

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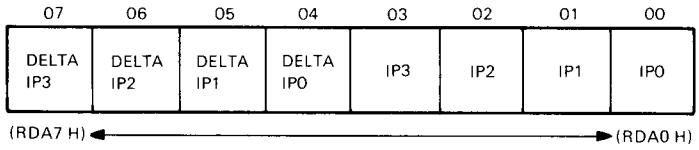
Figure D-9 2681 DUART: Receive/Transmit Data Registers (RDR/TDR) (Channel A and B)

ADDRESS 172020 (RD)



BIT VALUES		
BIT 7	0	NO CHANGE OF STATE DETECTED AT IP3
	1	CHANGE OF STATE DETECTED AT IP3
BIT 6	0	NO CHANGE OF STATE DETECTED AT IP2
	1	CHANGE OF STATE DETECTED AT IP2
BIT 5	0	NO CHANGE OF STATE DETECTED AT IP1
	1	CHANGE OF STATE DETECTED AT IP1
BIT 4	0	NO CHANGE OF STATE DETECTED AT IP0
	1	CHANGE OF STATE DETECTED AT IP0
BIT 3	0/1	CURRENT STATE OF IP3
BIT 2	0/1	CURRENT STATE OF IP2
BIT 1	0/1	CURRENT STATE OF IP1
BIT 0	0/1	CURRENT STATE OF IP0

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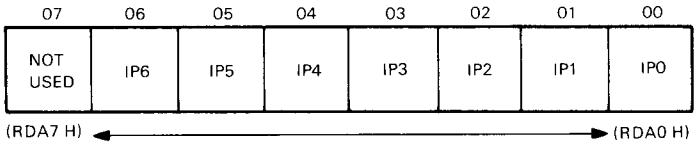
Figure D-1Ø 2681 DUART: Input Change Register (ICR)

ADDRESS 172064 (RD)



BIT VALUES		
BIT 6	0/1	CURRENT STATE OF IP6 (MOD2 SI L)
BIT 5	0/1	CURRENT STATE OF IP5 (HOST DSR L)
BIT 4	0/1	CURRENT STATE OF IP4 (MOD2 CTS L)
BIT 3	0/1	CURRENT STATE OF IP3 (MOD SI L)
BIT 2	0/1	CURRENT STATE OF IP2 (MOD CD L)
BIT 1	0/1	CURRENT STATE OF IP1 (PRTR DSR L)
BIT 0	0/1	CURRENT STATE OF IP0 (HOST CTS L)

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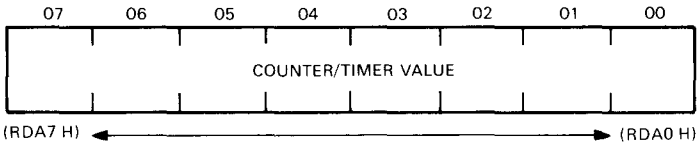
Figure D-11 2681 DUART: Input Port Register (IPR)

(CTUR) ADDRESS 172030(RD)/172032(WR)
(CTLR) ADDRESS 172034(RD)/172036(WR)



BIT VALUES	
BIT 0–7	LEAST SIGNIFICANT BYTE OF COUNTER OR TIMER MODE (CTLR)
	MOST SIGNIFICANT BYTE OF COUNTER OR TIMER MODE (CTUR)

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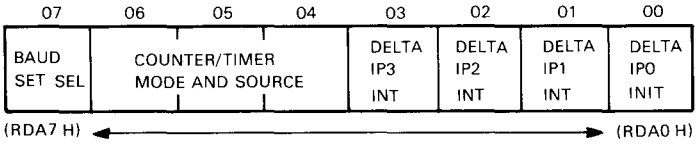
Figure D-12 2681 DUART: Counter Timer/Upper (CTUR) and Lower (CTLR) Registers

ADDRESS 172022(WR)



BIT VALUES		
BIT 7	0	SELECT BAUD RATE SET 1
	1	SELECT BAUD RATE SET 2
BIT 4–6	000	COUNTER MODE – EXTERNAL (IP2) SOURCE
	001	COUNTER MODE – TxCA AT 1X CLOCK OF CHANNEL A Tx
	010	COUNTER MODE – TxCB AT 1X CLOCK OF CHANNEL B Tx
	011	COUNTER MODE – CRYSTAL OR EXTERNAL CLOCK (CLK) DIVIDED BY 16
	100	TIMER MODE – EXTERNAL (IP2) SOURCE
	101	TIMER MODE – EXTERNAL (IP2) SOURCE DIVIDED BY 16
	110	TIMER MODE – CRYSTAL OR EXTERNAL (CLK) SOURCE
	111	TIMER MODE – CRYSTAL OR EXTERNAL (CLK) SOURCE DIVIDED BY 16
BIT 3	0	NO INTERRUPT ON CHANGE OF STATE
	1	SET ISR BIT 7 ON DETECT OF CHANGE OF STATE AT IP2
BIT 3	0	NO INTERRUPT ON CHANGE OF STATE
	1	SET ISR BIT 7 ON DETECT OF CHANGE OF STATE AT IP2
BIT 3	0	NO INTERRUPT ON CHANGE OF STATE
	1	SET ISR BIT 7 ON DETECT OF CHANGE OF STATE AT IP3
BIT 2	0	NO INTERRUPT ON CHANGE OF STATE
	1	SET ISR BIT 7 ON DETECT OF CHANGE OF STATE AT IP2
BIT 1	0	NO INTERRUPT ON CHANGE OF STATE
	1	SET ISR BIT 7 ON DETECT OF CHANGE OF STATE AT IP1
BIT 0	0	NO INTERRUPT ON CHANGE OF STATE
	1	SET ISR BIT 7 ON DETECT OF CHANGE OF STATE AT IP0

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Figure D-13 2681 DUART: Auxiliary Control Register (ACR)

ADDRESS 172024(RD)

07	06	05	04	03	02	01	00
INPUT PORT CHANGE	DELTA BREAK B	RxRDY/ FFULL B	TxRDY B	COUNTER READY	DELTA BREAK A	RxRDY/ FFULL A	TxRDY A

(RDA7 H) ◄——————————► (RDA0 H)

BIT VALUES		
BIT 7	0	NO INTERRUPT
	1	INPUT PORT CHANGE OF STATE DETECTED
BIT 6	0	NO INTERRUPT
	1	CHANGE IN BREAK STATE DETECTED (CH. B)
BIT 5	0	NO INTERRUPT
	1	RxRDY/FFULL CONDITION (CH. B)
BIT 4	0	NO INTERRUPT
	1	TxRDY CONDITION (CH. B)
BIT 3	0	NO INTERRUPT
	1	COUNTER READY CONDITION
BIT 2	0	NO INTERRUPT
	1	CHANGE IN BREAK STATE DETECTED (CH. A)
BIT 1	0	NO INTERRUPT
	1	RxRDY/FFULL CONDITION (CH. A)
BIT 0	0	NO INTERRUPT
	1	TxTDY CONDITION (CH. A)

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Figure D-14 2681 DUART: Interrupt Status Register (ISR)

ADDRESS 172026(WR)

07	06	05	04	03	02	01	00
INPUT PORT CHANGE	DELTA BREAK B	RxRDY/ FFULL B	TxRDY B	COUNTER READY	DELTA BREAK A	RxRDY/ FFUL A	TxRDY A

(RDA7 H) ◄——————————► (RDA0 H)

BIT VALUES		
BIT 7	0	INTERRUPT DISABLED
	1	INPUT PORT CHANGE OF STATE INTERRUPT ENABLED
BIT 6	0	INTERRUPT DISABLED
	1	CHANGE IN BREAK STATE INTERRUPT ENABLED (CH. B)
BIT 5	0	INTERRUPT DISABLED
	1	RxRDY/FFULL INTERRUPT ENABLED (CH. B)
BIT 4	0	INTERRUPT DISABLED
	1	TxRDY INTERRUPT ENABLED (CH. B)
BIT 3	0	INTERRUPT DISABLED
	1	COUNTER READY INTERRUPT ENABLED
BIT 2	0	INTERRUPT DISABLED
	1	CHANGE IN BREAK STATE INTERRUPT ENABLED (CH. A)
BIT 1	0	INTERRUPT DISABLED
	1	RxRDY/FFULL INTERRUPT ENABLED (CH. A)
BIT 0	0	INTERRUPT DISABLED
	1	TxTDY INTERRUPT ENABLED (CH. A)

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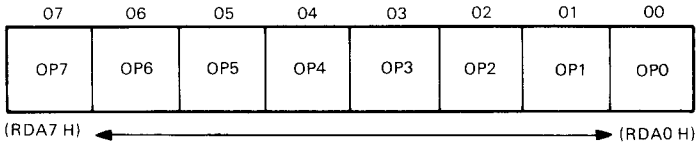
Figure D-15 2681 DUART: Interrupt Mask Register (IMR)

ADDRESS 172066(WR)



BIT VALUES		
BIT 7	0	NOT USED
	1	CONFIGURE OP7 AS COMPLIMENT OF TxRDYB
BIT 6	0	NOT USED
	1	CONFIGURE OP6 AS COMPLIMENT OF TxRDYA
BIT 5	0	NOT USED
	1	CONFIGURE OP5 AS COMPLIMENT OF Rx INTERRUPT (RxRDY/FFULL B)
BIT 4	0	NOT USED
	1	CONFIGURE OP4 AS COMPLIMENT OF Rx INTERRUPT (RxRDY/FFULL A)
BIT 3	0	COMPLIMENT OP3 FOR MOD SPD SEL L FALSE OUTPUT
	1	COMPLIMENT OP3 FOR MOD SPD SEL L TRUE OUTPUT
BIT 2	0	COMPLIMENT OP2 FOR HOST DTR L FALSE OUTPUT
	1	COMPLIMENT OP2 FOR HOST DTR L TRUE OUTPUT
BIT 1	0	COMPLIMENT OP1 FOR PRTR DTR L FALSE OUTPUT
	1	COMPLIMENT OP1 FOR PRTR DTR L TRUE OUTPUT
BIT 0	0	NOT USED
	1	CONFIGURE OP0 AS COMPLIMENT OF ENABLED RTSA

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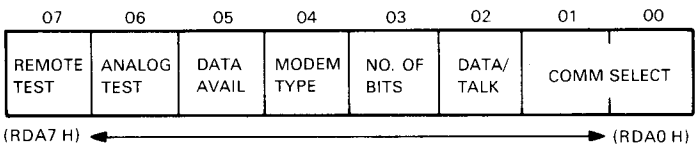
Figure D-16 2681 DUART: Output Port Configuration Register (OPCR)

ADDRESS 177004(WR)
ADDRESS 177004(RD)



BIT VALUES		
BIT 7	0	REMOTE TEST DISABLED
	1	REMOTE TEST ENABLED
BIT 6	0	ANALOG TEST DISABLED
	1	ANALOG TEST ENABLED
BIT 5	0	NO DATA AVAILABLE
	1	DATA AVAILABLE
BIT 4	0	DOMESTIC MODEM TYPE BELL 103
	1	EUROPEAN MODEM TYPE V.21
BIT 3	0	10 BITS PER CHARACTER
	1	9 BITS PER CHARACTER
BIT 2	0	TALK MODE
	1	DATA MODE
BIT 0–1	00	EIA HOST PORT
	01	NO CONNECTION
	10	20 mA PORT
	11	INTEGRAL MODEM

NOTE:
BIT 4 IS OVERRIDDEN BY MCWR
BIT 5 ON (1)

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Figure D-17 Comm/Modem Control: Comm Control Write (CCWR) and Read Registers (CCRD)

ADDRESS 177006(WR)

07	06	05	04	03	02	01	00
NOT USED	MODE SELECT	MODEM EMULATE	NOT USED	NOT USED	NOT USED	NOT USED	OFF HOOK DRIVE

(RDA7 H) ◄——► (RDA0 H)

BIT VALUES		
BIT 6	0	ORIGINATE MODE
	1	ANSWER MODE
BIT 5	0	EMULATE V.21 OR BELL 103
	1	EMULATE BELL 212A
BIT 0	0	ENABLE OFF HOOK DRIVE
	1	DISABLE OFF HOOK DRIVE

NOTE:
BIT 5 ON (1) OVERRIDES CCWR
BIT 4

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Figure D-18 Comm/Modem Control: Modem Control Write Register (MCWR)

ADDRESS 177006(RD)

07	06	05	04	03	02	01	00
DIAL TONE DETECT	MODE SELECT	MODEM A/B	CUT	TEST IND	SWITCH HOOK	OFF HOOK MODEM	OFF HOOK DRIVE

(RDA7 H) ◄——► (RDA0 H)

BIT VALUES		
BIT 7	0	DIAL TONE DETECTED
	1	NO DIAL TONE DETECT
BIT 6	0	OUTPUT OF MCWR BIT 6 SELECTS ORIGINATE MODE
	1	OUTPUT OF MCWR BIT 6 SELECTS ANSWER MODE
BIT 5	0	OUTPUT OF MCWR BIT 5 SELECTS BELL 103 OR V.21
	1	OUTPUT OF MCWR BIT 5 SELECTS BELL 212A
BIT 4	0	COUPLER CUT THROUGH CONDITION
	1	NO COUPLER CUT THROUGH CONDITION
BIT 3	0	INTEGRAL MODEM IN TEST MODE
	1	INTEGRAL MODEM IN NORMAL MODE
BIT 2	0	SWITCH HOOK CONDITION
	1	NO SWITCH HOOK CONDITION
BIT 1	0	OFF HOOK MODEM CONDITION
	1	NO OFF HOOK MODEM CONDITION
BIT 0	0	OUTPUT OF MCWR BIT 0 ENABLES OFF HOOK DRIVE
	1	OUTPUT OF MCWR BIT 0 DISABLES OFF HOOK DRIVE

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Figure D-19 Comm/Modem Control: Modem Control Read Register (MCRD)

ADDRESS 173000 (RD/CPU)
ADDRESS 00H (RD/CP)

07	06	05	04	03	02	01	00
NOT USED	H BLANK	VS	DMA	DRAW	FIFO EMPTY	FIFO FULL	DATA READY

(VDB7 H) ◄——————————————► (VDB0 H)

BIT VALUES		
BIT 7	–	NOT USED
BIT 6	1	HORIZONTAL BLANKING ACTIVE
	0	HORIZONTAL BLANKING INACTIVE
BIT 5	1	ENABLE VERTICAL RETRACE
	0	DISABLE VERTICAL RETRACE
BIT 4	1	DMA TRANSFER OCCURRING
	0	NO DMA TRANSFER OCCURRING
BIT 3	1	GRAPHIC FIGURE DRAWING IN PROGRESS
	0	NO DRAWING IN PROGRESS
BIT 2	1	ALL COMMANDS PROCESSED
	0	COMMAND AVAILABLE FOR PROCESSING
BIT 1	1	FIFO FULL
	0	FIFO NOT FULL
BIT 0	1	DATA AVAILABLE FOR CPU/CP
	0	NO DATA AVAILABLE

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Figure D-20 PD7220 GDC Status Register

ADDRESS 174600 (WR/CPU)
ADDRESS C0H (WR/CP)

07	06	05	04	03	02	01	00
ERA	SVP	SGDC	SLU	SVEC	EVOM	SM1	SM0

(VDB7 H) ◄——————————————► (VDB0 H)

BIT VALUES		
BIT 7	0	ERASE SCREEN ENABLED
	1	DISABLE SCREEN ERASE.
BIT 6	0	SELECT CHARACTER BUFFER PATTERN FOR LOGIC UNIT
	1	SELECT VECTOR PATTERN REGISTER PATTERN FOR LOGIC UNIT
BIT 5	0	SELECT OTHER THAN READ BACK MODE
	1	SELECT READ BACK MODE
BIT 4	0	BYPASS EXTERNAL LOGIC UNIT
	1	SELECT EXTERNAL LOGIC UNIT
BIT 3	0	ENABLE TEXT MODE AND WRITE MASH BATCH
	1	SELECT VECTOR MODE
BIT 2	0	DISABLE VOM OUTPUT, ENABLE WRITING TO VOM
	1	ENABLE VOM, NORMAL DISPLAY
BIT 0–1	00	SELECT MAP 0
	01	SELECT MAP 1
	10	SELECT MAP 2
	11	SELECT MAP 3

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Figure D-21 Video Logic Mode Select Register 0

ADDRESS 174640 (WR/CPU)
ADDRESS D0H (WR/CP)

07	06	05	04	03	02	01	00
NOT USED	NOT USED	NOT USED	NOT USED	SEN0	SEN1	SDI	NOT USED

(VDB7 H) ◄——► (VDB0 H)

BIT VALUES		
BIT 3–2	00	DISABLE DMA SCROLL AND LINE ERASE MODES
	01	NOT USED
	10	ENABLE LINE ERASE
	11	ENABLE DMA SCROLL
BIT 1	0	COUNT UP (INCREMENT)
	1	COUNT DOWN (DECREMENT)

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Figure D-22 Video Logic Mode Select Register 1

ADDRESS 174540 (WK/CPU)
ADDRESS B0H (WR/CP)

07	06	05	04	03	02	01	00
M1	M0	IF1	IF0	IB1	IB0	SP	PS

(VDB7 H) ◄——► (VDB0 H)

BIT VALUES		
BIT 6–7	00	REPLACE WRITING
	10	OVERLAY WRITING
	01	(NOT USED)
	11	COMPLIMENT WRITING
BIT 5	0/1	FOREGROUND INTENSITY VALUE PLANE 1
BIT 4	0/1	FOREGROUND INTENSITY VALUE PLANE 0
BIT 3	0/1	BACKGROUND INTENSITY VALUE PLANE 1
BIT 2	0/1	BACKGROUND INTENSITY VALUE PLANE 1
BIT 1	0	2 PLANE WRITING
	1	SINGLE PLANE WRITING
BIT 0	0	PLANE 0 SELECTED
	1	PLANE 1 SELECTED

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Figure D-23 Video Logic Unit Register

APPENDIX E
VIDEO LOGIC WRITE MODE PROGRAMMING OVERVIEW

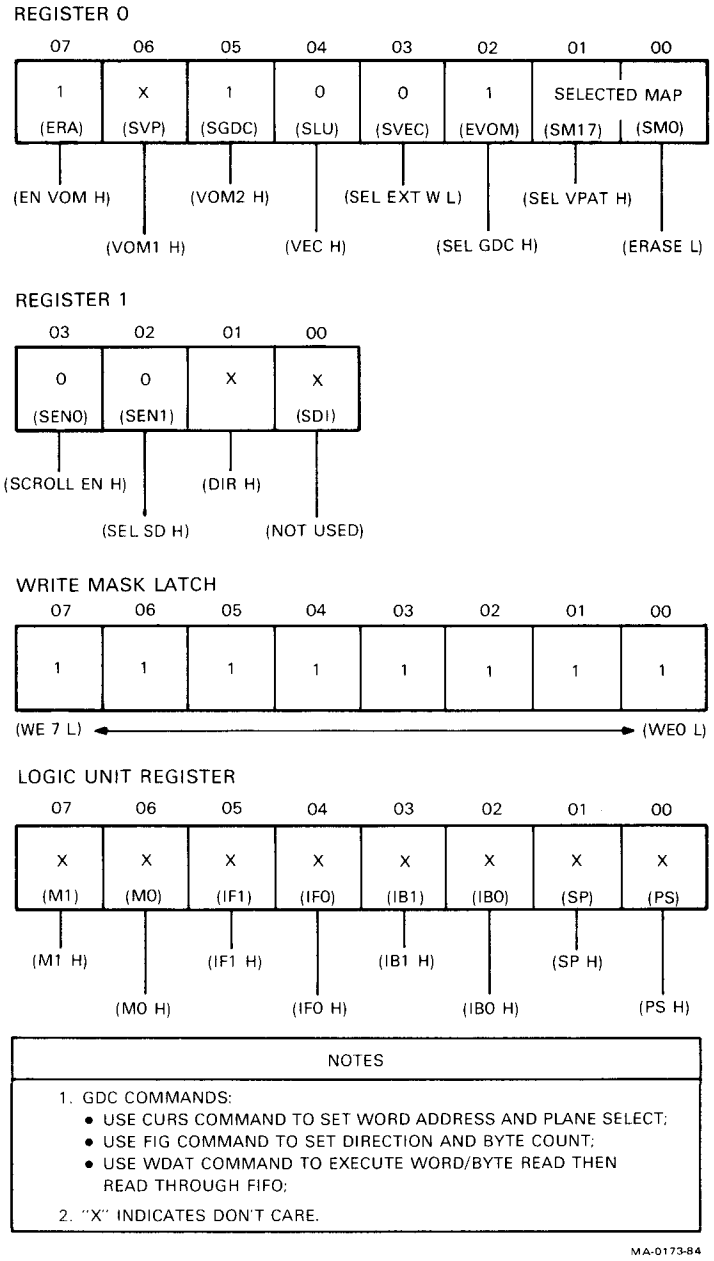

Figure E-1 Mode Ø (Read Back Mode) Programming Values

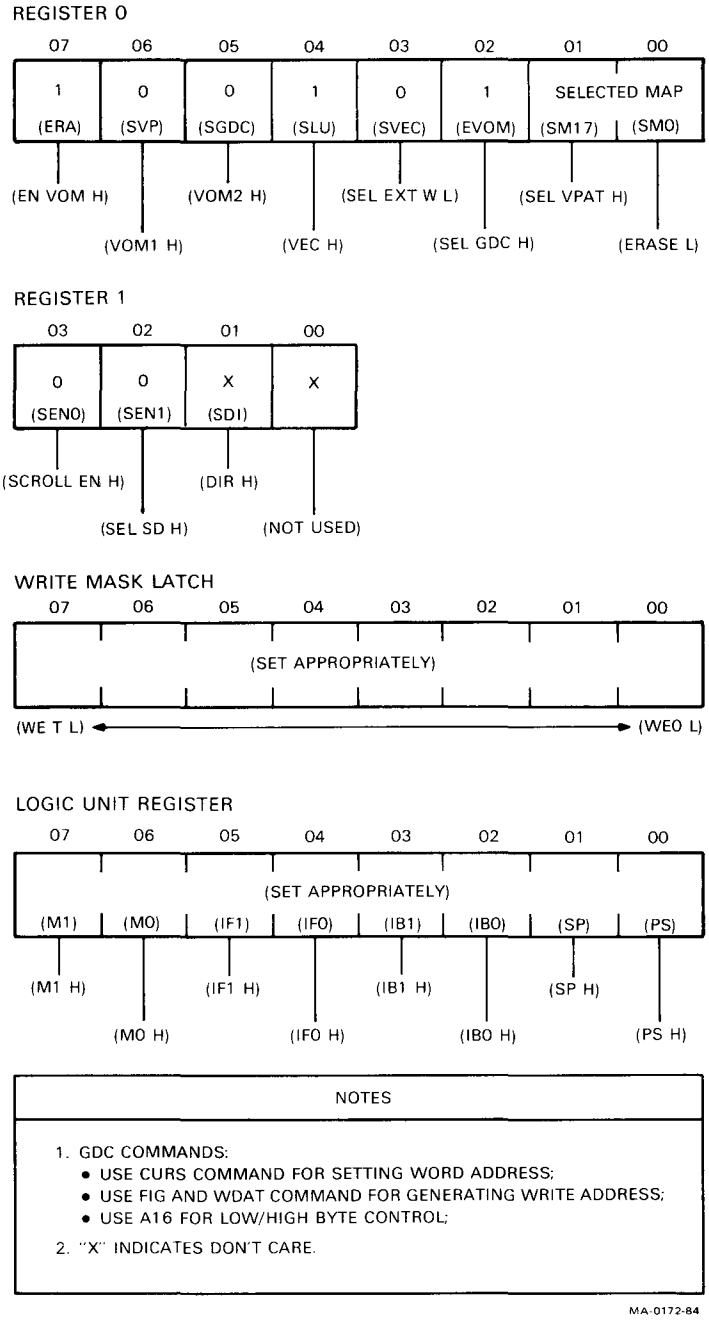

Figure E-2 Mode 1 (Text Mode) Programming Values

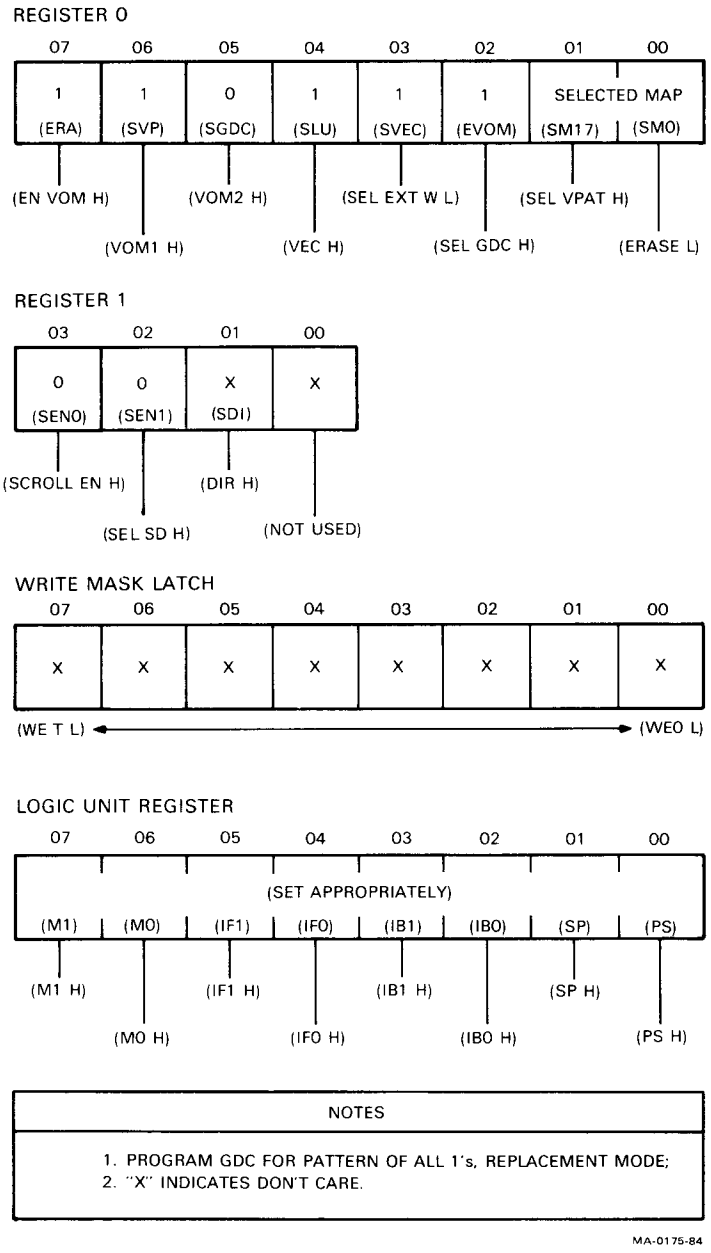

Figure E-3 Mode 2 (Vector Mode) Programming Values

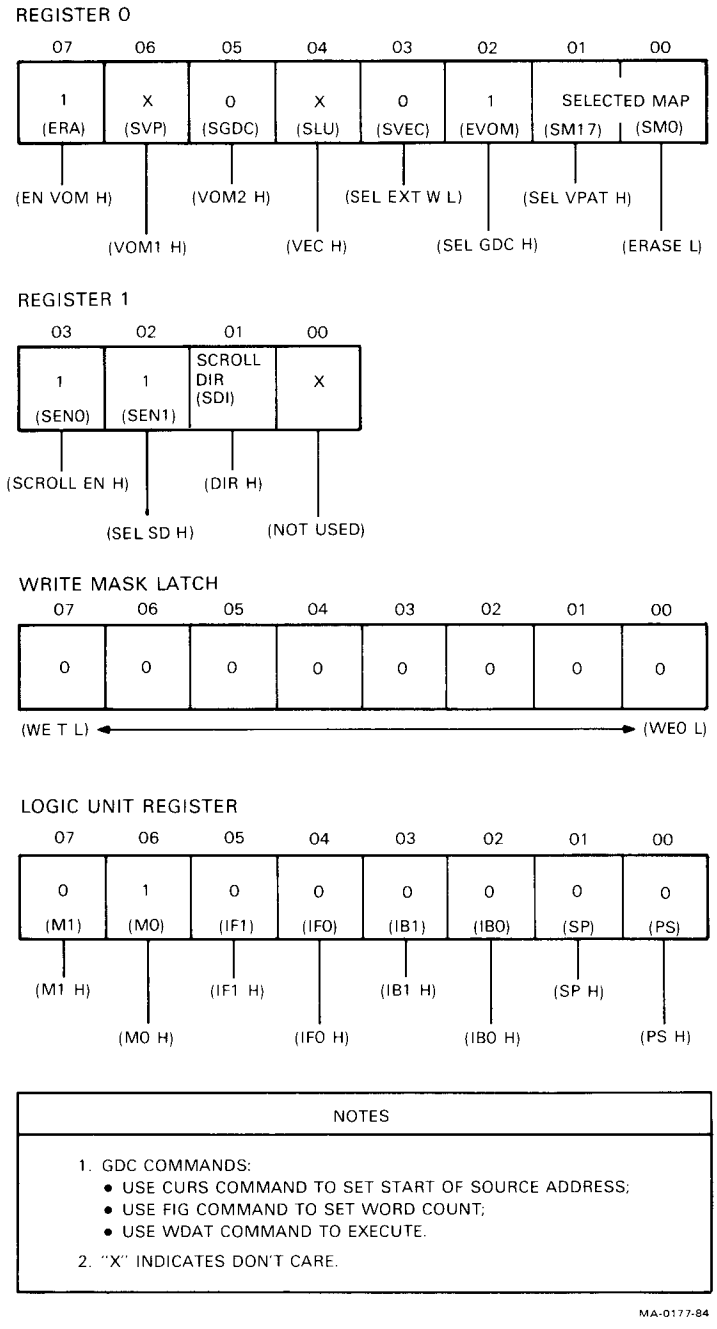

Figure E-4 Mode 3 (DMA Scroll Mode) Programming Values

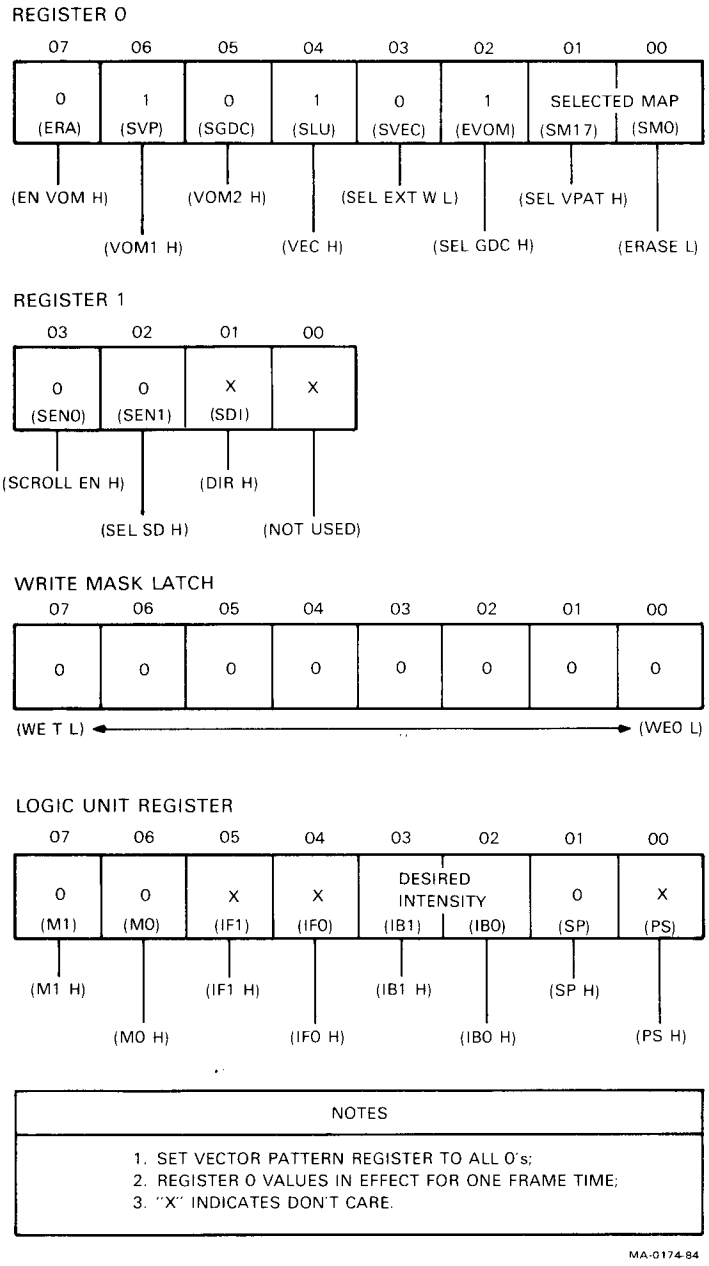

Figure E-5 Mode 4 (Screen Erase Mode) Programming Values

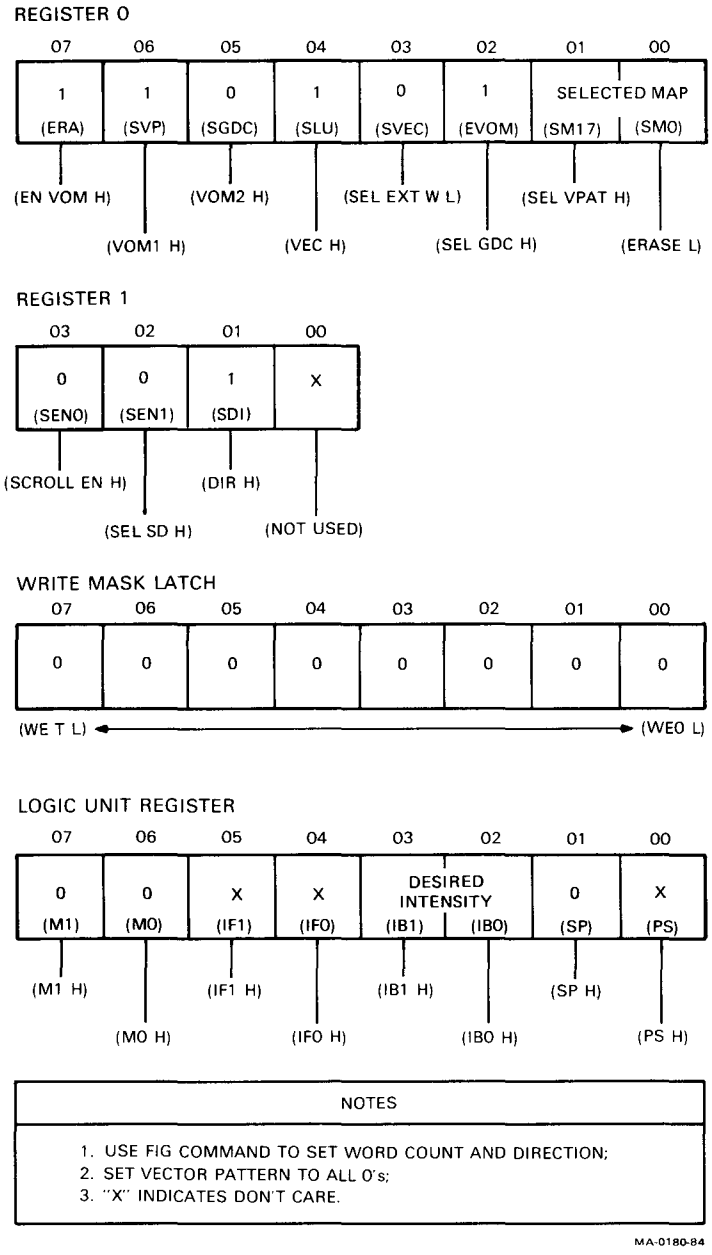

Figure E-6 Mode 5 (Word/Line Erase Mode) Programming Values

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(k)	Ease of Use	○1	○2	○3	○4	○5
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