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DMC11 IPL

microprocessor

technical manual

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PREFACE

This manual provides the user with information concerning the installation, operation, and maintenance of the DMC11 microprocessor.

- Chapter 1 provides an introduction and overall functional description of the DMC11 Microprocessor.

- Chapter 2 contains interfacing and installation information for two microprocessor options and four associated line unit options.

- Chapter 3 includes information necessary for operation of the DMC11 via the PDP-11 program.

- Chapter 4 contains a detailed description of the DMC11 operation.

- Chapter 5 provides information for servicing the DMC11 to the Field Replaceable Unit (modules and cables). Procedures for running the diagnostics are also included.

- The Appendices contain appropriate supplementary information.

The *DMC11 IPL Synchronous Line Unit Maintenance Manual* (EK-DMCLU-MM-002) and the DMC11 Engineering Drawings (DMC11-0-8) provide additional information which draws the entire system together.

CHAPTER 1
INTRODUCTION

1.1 SCOPE

This chapter contains a brief introduction to DMC11 operation. The term DMC11 as used throughout this manual denotes the communication subsystem consisting of a microprocessor module and a line unit module.

1.2 DMC11 GENERAL DESCRIPTION

The DMC11 is a microprocessor-based, intelligent, synchronous communication controller residing as a Direct Memory Access (DMA) or Non-Processor Request (NPR) device on the PDP-11 UNIBUS.

The DMC11 ensures reliable data transmission by implementing the DIGITAL Data Communication Protocol (DDCMP) in firmware using a high-speed microprocessor. The DDCMP detects errors on the channel connecting the systems by using a 16-bit Cyclic Redundancy Check (CRC-16). Errors are corrected, when necessary, by automatic retransmissions. Sequence numbers in message headers ensure that messages are delivered in proper order with no omissions or duplications.

A number of advantages are offered by the DMC11 over conventional communication interfaces which require a combination of hardware and software to implement a protocol. Programming is greatly simplified and extensive communications expertise is no longer required when programming the DMC11. PDP-11 memory and processor time are not wasted with instructions implementing the protocol. As a direct result, throughput is enhanced because the DMC11 operates at high speeds and is not delayed when the processor has to perform high priority tasks.

The DMC11 microprocessor provides parallel data interfaces between any PDP-11 family central processor and a given DMC11 line unit. With the microprocessor/line unit combination, computers can be configured for either remote or local applications. There are two versions of the DMC11 microprocessor: the DMC11-AR (M8200-YA module) which supports remote applications and the DMC11-AL (M8200-YB module) which supports local applications. The DMC11-AR microprocessor operates with either the DMC11-DA or the DMC11-FA line unit (M8201 module); the DMC11-AL operates with either the DMC11-MA line unit (M8202-YA module) or the DMC11-MD line unit (M8202-YD module).

For remote operation, the computers are connected by common carrier facilities. DMC11-ARs can be configured to interface with synchronous modems of up to 19.2K bps for modems that conform to the EIA RS232-C interface standard and up to 56K bps for modems that conform to the CCITT V.35/DDS interface standard. A typical configuration for remote applications is illustrated in Figure 1-1.

For local operations, DMC11-ALs can be configured for high-speed operation of 56K bps or 1M bps over triaxial cables. A typical configuration for local applications is illustrated in Figure 1-2.
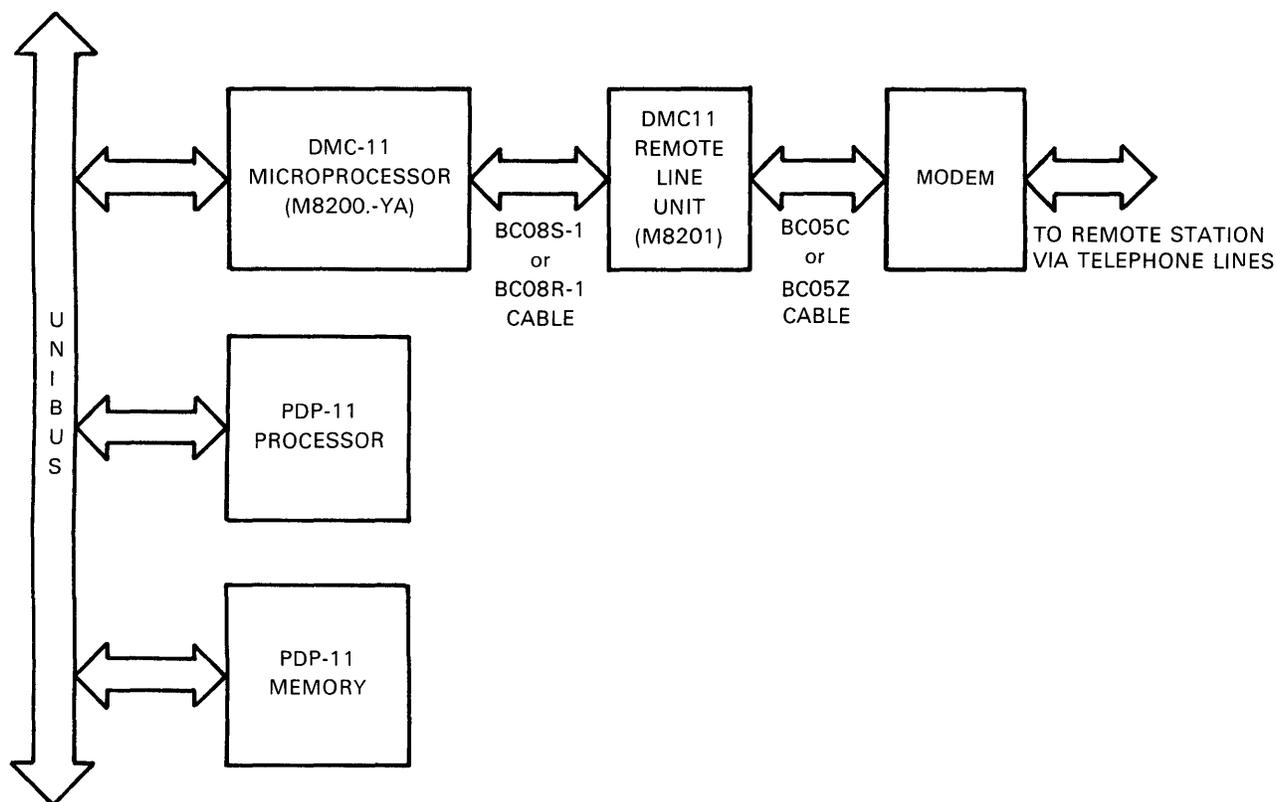
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Figure 1-1   DMC11 Remote Line Unit Interface

Both the DMC11-DA and DMC11-FA line unit versions of the M8201 module contain modem control and level conversion logic that is compatible with EIA RS232-C/CCITT V.24 and CCITT V.35/DDS interface standards. The DMC11-DA is shipped with a cable that accommodates only the EIA RS232-C/CCITT V.24 interface. This line unit has a maximum speed of 19.2K bps. The DMC11-FA is shipped with a cable that has a maximum speed of 56K bps and accommodates only the CCITT V.35/DDS interface standard.

The DMC11-MA (M8202-YA) and DMC11-MD (M8202-YD) line unit versions have built-in integral modems. The DMC11-MA operates at a speed of 1M bps over triaxial cables up to a maximum distance of 1 km (3281 ft) with a Belden 8232 or equivalent cable and 2 km (6562 ft) with a Belden 8233 or equivalent cable. The DMC11-MD operates at a speed of 56K bps over triaxial cables up to a maximum distance of 3 km (9843 ft) with a Belden 8232 cable and 6 km (19,685 ft) with a Belden 8233. The triaxial cable is not included with either option. (This cable is not available from DIGITAL, see *DMC11 IPL Synchronous Line Unit Maintenance Manual*, EK-DMCLU-MM-002, for cable specifications.)

The line unit is not a stand-alone device. It must be used with a DMC11 or equivalent microprocessor. Refer to the *DMC11 IPL Synchronous Line Unit Maintenance Manual* for complete coverage of the DMC11 line units.

1.3   DMC11 SYSTEM OPERATION
Operation of the DMC11 is initiated and directed by a user-produced program residing in the PDP-11 [main Central Processing Unit (CPU)] memory. A user program is a device driver or an equivalent

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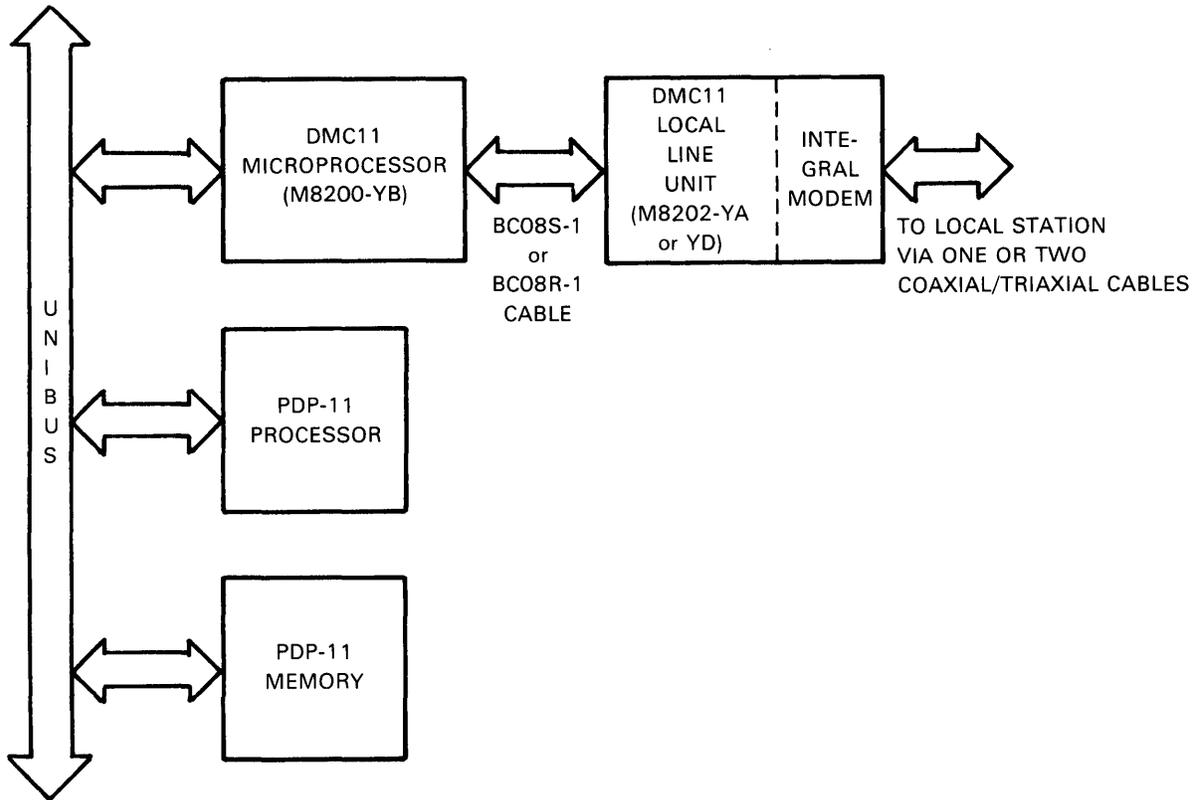
Figure 1-2   DMC11 Local Line Unit Interface

routine that interfaces to the DMC11. Communication between the user program and the DMC11 is provided by four Control and Status Registers (CSRs), which are integral to the DMC11 microprocessor. These four 16-bit registers are used for control input, status output, the receiving or transmitting buffer to the DMC11, and the receiving or transmitting buffer returns from the DMC11.

The first two registers in this group have a fixed format and serve as the command header for the second two registers. The second two registers form a two-word data port for the exchange of unique control/status information between the DMC11 and the user program. The contents of the data port are specified by an identification field in the command header. Other specific fields in the two-word command header control interrupt enabling and status bits for command transfer handshakes between the main CPU and the DMC11.

A user program issues a command to the DMC11 by setting up the input command header and requesting use of the data port when the DMC11 grants permission to use the data port. The user program then passes the command to the DMC11 in the pertinent CSRs. The DMC11 interprets the command and performs the specified actions. Similarly, the DMC11 issues a command to the user program by storing the command in the pertinent CSRs and notifying the user program that a command is available for retrieval and processing.

Message data received or transmitted by the DMC11 is written into or read from user program assigned buffers in main CPU memory. The DMC11 accesses these buffers through NPRs to a UNIBUS address. A UNIBUS address is an 18-bit address used by an NPR device to access a device on the UNIBUS or a location in main CPU memory.

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1.3.1 Command Structure
The transfer of information between the DMC11 microprogram and the user program requires implementation of a six-function command structure. The functions of commands are described briefly in this section and in greater detail in Chapter 3.

1.3.1.1 Initialization Command – This command is used to clear all condition-sensitive logic in the DMC11 microprocessor/line unit and place the microprocessor in the initialized state. The Initialization command must be issued by the user program prior to startup of the DMC11 or after fatal error restart.

1.3.1.2 Base In Command – This command is used to assign a starting address of an area in the CPU's main memory that is 128 words in length where the DMC11 can store a snapshot (copy) of its internal memory. The transfer of the DMC11's memory contents to core memory only takes place on fatal error conditions. The DMC11's internal memory contains DDCMP link information for error reporting and error recovery which can be used when the DMC11 enters the protocol start-up sequence. The Base In command must be the first command issued after MASTER CLEAR via the Initialization command, system initialization, or power failure. After assigning this Base In command with the RESUME bit clear, the DMC11 enters the protocol start-up sequence and the link can now become active. There are two reasons for storing this information in both the DMC11's memory and the CPU's memory: (1) the DMC11's memory is volatile (RAM), whereas most of the CPU's memory is the non-volatile type (CORE), allowing excellent error recovery without a loss of link integrity, and (2) allowing the operating system easy access to the DMC11's memory contents without affecting the DMC11's operation. Base Table information can only be read for status and must never be altered by the operating system.

1.3.1.3 Control In Command – This command defines the characteristics of the DMC11 such as half-duplex or full-duplex mode and normal DDCMP or DDCMP maintenance mode. The Control In command must be issued to the DMC11 following a Base In command.

1.3.1.4 Buffer Address In Command – The PDP-11 program issues this command to assign either a transmit or receive buffer to the DMC11 by specifying an 18-bit address plus a 14-bit character count for transmit or receive operation. There can be a maximum of seven transmit buffers and seven receive buffers assigned to the DMC11 at any given time.

1.3.1.5 Buffer Address Out Command – When the DMC11 has successfully completed a receive operation (the CRC check was good) or a transmit operation (the transmitted message was acknowledged), the buffer is returned to the PDP-11 by a Buffer Address Out command.

1.3.1.6 Control Out Command – The DMC11 issues this status command to inform the PDP-11 of some error condition which is either fatal or non-fatal. Non-fatal errors can be corrected by removing the error condition. Fatal errors cause the protocol to terminate and require initialization of the DMC11.

1.3.2 DMC11 Operation Sequencing
The normal sequence of operation is represented in the flow chart of Figure 1-3.

The PDP-11 program initializes the DMC11 (MASTER CLEAR), assigns a 128-word Base Table via the Base In command, sets up the proper mode by the Control In command, and then assigns transmit and receive buffers via the Buffer Address/Character Count In (BA/CCI) commands. After receiving the Base In command, the DMC11 initiates the protocol start-up sequence. The Control In command sets the DMC11 in either half-duplex or full-duplex mode, and normal DDCMP or DDCMP maintenance mode.

NOTE
The start-up sequence involves exchange of STRT,
STACK, and ACK messages between two DMC11s
(see Appendix D).

At this point, the DMC11 is in the DDCMP running mode. Any transmit buffer assigned to the DMC11 causes the DMC11 to NPR (via DMA) the data from the PDP-11 memory and be transmitted on the serial line.

On transmit, the DMC11 generates the DDCMP header and generates and transmits CRC characters. On receive, the DMC11 NPRs the received data to the PDP-11 memory, provided there are receive buffers assigned. The DMC11 processes the received header, checks the CRC characters, and controls acknowledgement of properly received data messages. The DMC11 performs message sequencing, link management, CRC error checking, retransmission, and some error reporting to the PDP-11.

INITIALIZE
DMC11 — VIA MASTER CLEAR

ASSIGN 128-
WORD BASE TABLE ←→ VIA BASE IN COMMAND

DMC11 INITIATES THE
PROTOCOL START UP ——→
SEQUENCE

SET UP PROPER
MODE
HALF-OR FULL-DUPLEX — VIA CONTROL IN COMMAND
NORMAL DDCMP OR
DDCMP MAINTENANCE

DMC11 IN DDCMP RUNNING MODE
AFTER COMPLETION OF DDCMP START SEQ.

ASSIGN TRANSMIT &
RECEIVE BUFFERS ←→ VIA BUFFER ADDRESS/CHARACTER
COUNT IN COMMANDS

TRANSMIT   RECEIVE

DMC11 (1) GENERATES DDCMP
PROTOCOL HEADER, (2) GEN-
ERATES AND TRANSMITS CYCLIC
REDUNDANCY CHECK (CRC)
CHARACTERS

DMC11 (1) PROCESSES
THE RECEIVED HEADER, (2)
CHECKS CRC CHARACTERS, (3)
CONTROLS ACKNOWLEDGEMENTS (ACKS) OF
PROPERLY RECEIVED DATA MES-
SAGES AND NEGATIVE ACKS (NAKS) FOR
ERROR MSGS.

THE DMC11 PERFORMS
MESSAGE SEQUENCING,
CRC ERROR CHECKING,
RETRANSMISSION,
SOME ERROR REPORTING
TO THE PDP-11, AND
LINK MANAGEMENT

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Figure 1-3   DMC11 Operation Sequencing

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2.1 SCOPE

This chapter provides all the necessary information for a successful installation and subsequent check-out of the DMC11 microprocessor subsystem.

2.2 UNPACKING AND INSPECTION

Inspect the container and contents for damage. If any damage is found, notify the customer, record it on the LARS form and take appropriate action.

There are two microprocessor options and four line unit options. Ensure that the contents agree with the required parts associated with the option selected. Table 2-1 identifies the option, related parts and descriptions.

2.3 MECHANICAL PACKAGING

The DMC11 consists of a microprocessor module (hex) and a line unit module (notched hex). These modules plug into any DD11-B (Revision E or later), DD11-C, DD11-D or equivalent SPC system unit. The microprocessor module must always plug into either slot 2 or 3 in the DD11-B or DD11-C. The line unit module may be installed into any of the remaining slots. If two DMC11s are installed into a single DD11-B, then the line unit module plugs into slot 1 or 4.

The line unit does not interface with the UNIBUS, but picks up power and ground from the back-plane, so module edge connectors A and B are not required. As a result, the corner of the module in the vicinity of the A and B connectors has been removed. This allows the M8201 and M8202 to be installed in the end SPC slots of the DD11-B, C, or D system interfacing units. The module plugs into connectors C, D, E, and F, and fits over the UNIBUS cable connector or short length (approximately 2 1/2 inches) UNIBUS terminator that is installed in end slot connectors A and B.

The two modules are interconnected by a BERG 40-pin connector and a one-foot BC08S-1 cable. A BC08R-1 cable can be used instead of a BC08S-1 if the need arises (the shipping list requires a BC08S-1).

2.4 PRE-INSTALLATION CONSIDERATIONS

Installation of the DMC11 microprocessor/line unit should be done in three phases. The microprocessor is installed first, the line unit is installed second, then modules are checked and verified via the diagnostic programs.

2.4.1 Configuration Considerations

The DMC11 is located in the floating address space. Therefore, the address allocation is not the limiting factor. The total DMC11 throughput rate forms a more severe limitation on the number of DMC11s in a system.

Table 2-1 Microprocessor/Line Unit Options and Parts

Option	Parts	Description	Prerequisite
DMC11-AR	1. M8200-YA	Microprocessor with DDCMP microcode for remote applications	PDP-11
		Used with M8201 line unit only	
	2. BC08S-1	Cable to interconnect microprocessor and line unit	
	3. EK-DMCMP-TM-002	*DMC11 IPL Micropro-cessor Technical Manual*	
	4. MP00076	*Customer Print Set* (DMC11)	
	5. ZJ-216-RB	Software LIB KIT*	
DMC11-DA	1. M8201	Line unit for remote applications	DMC11-AR
	2. BC05C-25	Cable for EIA/CCITT V.24 interface	
	3. H325	Modem test connector	
	4. EK-DMCLU-MM-002	*DMC11 IPL Synchronous Line Unit Maintenance Manual*	
DMC11-FA	1. M8201	Line unit for remote applications	DMC11-AR
	2. BC05Z-25	Cable for CCITT V.35/ DDS interface	
	3. H3250	Cable test connector	
	4. EK-DMCLU-MM-002	*DMC11 IPL Synchronous Line Unit Maintenance Manual*	
DMC11-AL	1. M8200-YB	Microprocessor with DDCMP microcode for local applications	PDP-11
		Used with M8202-XX line units only	

Table 2-1 Microprocessor/Line Unit Options and Parts (Cont)

Option	Parts	Description	Prerequisite
	2. BC08S-1	Cable to interconnect microprocessor and line unit	
	3. EK-DMCMP-TM-002	*DMC11 IPL Micropro-cessor Technical Manual*	
	4. MP-00076	*Customer Print Set* (DMC11)	
	5. ZJ-216-RB	Software LIB KIT*	
DMC11-MA	1. M8202-YA	Line unit with 1 MEG BPS integral modem	DMC11-AL
	2. 12-12528-00	Cable test connector	
	3. EK-DMCLU-MM-002	*DMC11 IPL Synchronous Line Unit Maintenance Manual*	
DMC11-MD	1. M8202-YD	Line unit with 56K BPS integral modem	DMC11-AL
	2. 12-12528-00	Cable test connector	
	3. EK-DMCLU-MM-002	*DMC11 IPL Synchronous Line Unit Maintenance Manual*	

*ZJ-216-RB Software Library Kit contains the following diagnostic programs:

- CZDMC Microprocessor Basic W/R and μP Test

- CZDME Line Unit DDCMP Test

- DZDMF Line Unit Bit Stuff Test

- CZDMG CROM and Jump Test

- DZDMH DMC11 free-running tests

- DZDMO DMC11 Overlay for Interprocessor Test Program

A single DMC11 at 1M bps and in full-duplex mode is capable of transferring 250,000 × 8-bit characters per second (125,000 character/sec × 2 directions). Because the DMC11 performs 16-bit word transfers via NPR transactions to memory, approximately 125,000 NPRs per second or the rate of 8 microseconds/NPR is generated.

High-speed DMC11s of 1M bps must be placed before all devices on the UNIBUS (including UNIBUS repeaters), except unbuffered NPR devices such as RK11s.

2.4.2 Power Requirements
Check the power supply before and after installation to ensure against overloading. The microprocessor/line unit total current requirements for the +5 volt supply is approximately 8 amperes. Additionally, the line unit requires ±15 volts for the silos, level conversion logic, and integral modem. Power requirements for the microprocessor/line units are listed below.

M8200 microprocessor + 5 volts @ 5.0 amps

M8201 line unit	+ 5 volts @ 3.0 amps
	+ 15volts @ 0.03 amps
	− 15volts @ 0.31 amps
M8202 line unit	+ 5 volts @ 3.0 amps
	+ 15volts @ 0.18 amps
	− 15volts @ 0.46 amps

2.4.3 Backplane
The DMC11 requires two hex SPC slots, preferably two adjacent ones (refer to Section 2.3, Mechanical Packaging, for details). Section 2.6.1 provides preinstallation checkout procedures concerning backplane slots, wire runs, and power supply pin locations.

2.5 DEVICE AND VECTOR ADDRESSES

2.5.1 Device Address Assignment
DMC11 addresses are selected from the floating address space and are assigned as follows:

- The floating address space starts at location 760010_8 and extends to location 764000_8.

- The devices are assigned addresses in the following sequence:

  1. DJ11s
  2. DH11s
  3. DQ11s
  4. DU11s
  5. DUP11s
  6. LK11-As
  7. DMC11s
  8. DZ11s
  9. KMC11s
  10. LPP11s
  11. VMV21s
  12. VMV31s
  13. DWR70s
  14. RL11/RLV11 (for second device, only if two or more are used)

- The first address of a new device type must start on a module 10_8 boundary, and a gap of 10_8 must be left between the last address of one device type and the first address of the next device type.

  The 10_8 gap must also be left for devices that are not installed in the system, but are passed in the priority ranking list.

- Multiple devices of the same type must be assigned contiguous addresses. Reassignment of other device types already in the system may be required to make room for additional ones. Examples of DMC11 address assignments are provided in Section 2.5.3.

- Both the DH11 and VMV31 require an address size of 20_8 per device installed in the system. Also because of hardware requirements, the DH11's address must start on a multiple of 20_8, such as 760020, 760040, 760060, and 760100.

2.5.2 Vector Address Assignment

DMC11 vector addresses are selected from the floating vector address space and are assigned as follows.

- The floating vector address space starts at location 300_8 and proceeds up to location 777_8.

- Floating vector addresses are assigned to devices sequentially and by device type as indicated below.

Table 2-2 Vector Address Assignment

Floating Vectors		Vector Size	Octal Modules
1.	DC11	4	10
2.	KL11/DL11-A,B	4	10
3.	DP11	4	10
4.	DM11-A	4	10
5.	DN11 Lines	2	4
6.	DM11-BB/DH11 MCU	2	4
7.	DR11-A	4	10
8.	DR11-C	4	10
9.	PA611-Reader	2	10
10.	PA611-Punch	2	10
11.	LPD11	4	10
12.	DT11	4	10
13.	DX11	4	10
14.	DL11-C,D,E	4	10
15.	DJ11	4	10
16.	DH11	4	10
17.	GT40	8	10
18.	LPS11	12	10
19.	DQ11	4	10
20.	KW11-W	4	10
21.	DU11	4	10
22.	DUP11		10
23.	DV11		10
24.	DV11 MCU	2	4

Table 2-2 Vector Address Assignments (Cont)

Floating Vectors		Vector Size	Octal Modules
25.	LK11-A	4	10
26.	DWUN	4	10
27.	DMC11	4	10
28.	DZ11	4	10
29.	KMC11	4	10
30.	LPP11	4	10
31.	VMV21	4	10
32.	VMV31	4	10
33.	VTV01	4	10
34.	DWR70	4	10
35.	RL11/RLV11 (for second device, only if two or more are used)	2	4
36.	RX02	2	4
37.	TS11	2	4
38.	LPA11-K	4	10
39.	IP11/IP300	2	4

- If any device type is not used in a system, address assignments move up to fill the vacancies.

- If additional devices are to be added to the system, the same device types must be assigned contiguously after the original devices; devices not included in the initial system configuration must be assigned addresses which are relevent to their position in the sequence. Reassignment of devices already in the system may be required. Examples of DMC11 vector address assignments are provided in Section 2.5.3.

2.5.3 Examples of Device and Vector Address Assignment

Example 1

The first device requiring address assignment in this example is a DH11 (No. 2 in the device address assignment sequence; No. 16 in the vector address assignment sequence).

The only devices used are:

    2 DH11s
    2 DQ11s
    1 DUP11
    1 DMC11

Device (Option)	Device Address	Vector Address	Comment
	760010		Gap left for DJ11 (No. 1 on device address assignment sequence) which is not used.
DH11	760020	300	First DH11
DH11	760040	310	Second DH11
	760060		Gap between the last DH11 used and the next device.
DQ11	760070	320	First DQ11
DQ11	760100	330	Second DQ11
	760110		Gap between the last DQ11 used and the next device.
	760120		Gap left for DU11s not used.
DUP11	760130	340	Only one DUP11
	760140		Gap left between DUP11 and next device.
	760150		Gap left for LK11-As not used.
DMC11	760160	350	Only one DMC11
	760170		Gap left after the last device (in this case, the DMC11) to indicate that none follow.

Example 2

The only devices used in this example are:

    1 DJ11
    1 DH11
    2 DQ11s
    2 DUP11s
    2 DMC11s

Device (Option)	Device Address	Vector Address	Comment
DJ11	760010	300	Only one DJ11
	760020		Gap left between DJ11 and the next device.
	760030		Gap. The next device, DH11, must start on an address boundary that is a multiple of 20.

Device (Option)	Device Address	Vector Address	Comment
DH11	760040	310	Only one DH11
	760060		Gap left between DH11 and next device.
DQ11	760070	320	First DQ11
DQ11	760100	330	Second DQ11
	760110		Gap left between DQ11 and next device.
	760120		Gap left for DU11s not used.
DUP11	760130	340	First DUP11
DUP11	760140	350	Second DUP11
	760150		Gap left between the last DUP11 and next device.
	760160		Gap left for LK11-As not used.
DMC11	760170	360	First DMC11
DMC11	760200	370	Second DMC11
	760210		Gap left after the last device (in this case the DMC11) to indicate that none follow.

Example 3

Only one of each of the following devices are used in this example:

    DC11
    DJ11
    DH11
    GT40
    DQ11
    DUP11
    DMC11

Device (Option)	Device Address	Vector Address	Comment
DC11		300	DC11 has a fixed device address.
DJ11	760010	310	Only one DJ11
	760020		Gap left between DJ11 and the next device.

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Device (Option)	Device Address	Vector Address	Comment
	760030		Gap. The next device, DH11, must start on an address boundary that is a multiple of 20.
DH11	760040	320	Only one DH11
	760060		Gap left between DH11 and next device.
GT40		330	GT40 has a fixed device address.
DQ11	760070	340	Only one DQ11
	760100		Gap left between DQ11 and next device.
	760110		Gap left for DU11s not used.
DUP11	760120	350	Only one DUP11
	760130		Gap left between DUP11 and the next device.
	760140		Gap left for LK11-As not used.
DMC11	760150	360	Only one DMC11
	760160		Gap left after the last device (DMC11) to indicate that none follow.

2.5.4 Interrupt Priority
Interrupt priority is selected by a priority plug on the M8200 microprocessor module. This plug is preset to select priority 5 (BR5).

2.5.5 UNIBUS Loading

M8200-YX microprocessor:

    1 UNIBUS DC load
    3 UNIBUS AC loads

M8201 or M8202-YX line unit:

    No UNIBUS loads

2.6 MODULE INSTALLATION AND CUSTOMIZATION

2.6.1 Preinstallation Checkout Procedure
Before installing the microprocessor module, perform the following:

1. **Place high-speed DMC11s (1M bps)** before any UNIBUS repeaters.

2. **Prepare the backplane slot** that will accept the M8200-YA/YB microprocessor by removing the NPR GRANT (NPG) wire between pins CA1 and CB1.

Do not remove the wire at the slot that will accept the M8201 or M8202-YX line unit.

When the M8200 is removed, the NPR GRANT wire must be replaced.

3. **Refer to Table 2-3** and ensure that the power supply voltages at the respective backplane pins are within the tolerances indicated.

Table 2-3 Power Supply Voltages

Backplane Pin	Minimum	Voltage Nominal	Maximum
C1A2	+4.75V	+5.0V	+5.25V
C1B2	-14.25V	-15.0V	-15.75V
C1U1	+14.25V	+15.0V	+15.75V

4. **Verify** that jumper W1 on the M8200-YA/YB is installed.

NOTE
This jumper should not be removed in the field. Removal is only done at the factory to inhibit the oscillator in the microprocessor clock logic during automated module testing.

5. **Refer to Sections 2.5.1 and 2.5.3 to determine the DMC11 address.** In the floating address space (addresses 760010 through 764000), bits 13 through 17 are always ones (a function of the PDP-11 processor). Appendix A shows the PDP-11 memory organization and addressing conventions. Bits 3 through 12 are selected by switches in the address decoding logic (see Table 2-4). With the switch ON (closed), the decoder looks for a zero on the associated UNIBUS address line. Bits 0, 1, and 2 are decoded to select one of eight registers. Device address selection switches are contained in one DIP switch package located in position E113 as shown in Figure 2-1. All 10 switches in the package are used. Correlation between switch numbers and address bit numbers is shown in Table 2-4. The ON and OFF positions and the switch numbers are marked on the package. The switches are rocker type and are pushed to the desired position (see Figure 2-1).

6. **Refer to Sections 2.5.2 and 2.5.3 to determine the DMC11 vector address.** Each drive interrupt vector requires four address locations (two words) which implies only even-numbered addresses. A further constraint is that all vector addresses must end in a 0 or 4. The vector address is specified as a three digit, binary-coded, octal number using UNIBUS data bits 0–8. Because the vector must end in 0 or 4, bits 1 and 0 are not specified (they are always 0) and bit 2 determines the lease significant octal digit of the vector address (0 or 4).

The interrupt control logic generates two vector addresses: RDI interrupts generate vector addresses of the form XXO, and RDO interrupts generate vector addresses of the form XX4. For this method of operation, the state of bit 2 is selected by the logic, not by a switch. The two most significant octal digits of the vector address are determined by switches in lines 3–8 (Table 2-5). With the switch OFF (open), a 0 is generated on the associated UNIBUS data line; with the switch ON (closed), a 1 is generated on the associated UNIBUS data line.

The vector address selection switches are contained in one DIP package located in position E76 (Figure 2-1). Only six of the ten switches in the package are used for the vector address. The correlation between switch numbers and bit numbers is shown in Table 2-5. The ON and OFF positions and the switch numbers are marked on the package. The switches are rocker types pushed to the desired position.

Table 2-4   Guide for Setting Switches to Select Device Addresses

| Switch No. | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | Device |
Bit No.	12	11	10	9	8	7	6	5	4	3	Address
										OFF	760010
									OFF		760020
									OFF	OFF	760030
								OFF			760040
								OFF		OFF	760050
								OFF	OFF		760060
								OFF	OFF	OFF	760070
							OFF				760100
						OFF					760200
						OFF	OFF				760300
					OFF						760400
					OFF		OFF				760500
					OFF	OFF					760600
					OFF	OFF	OFF				760700
				OFF							761000
			OFF								762000
			OFF	OFF							763000
		OFF									764000

- Switch is OFF (open) to respond to logical 1 on the UNIBUS.

- Switch numbers are physical positions in switch package 1.
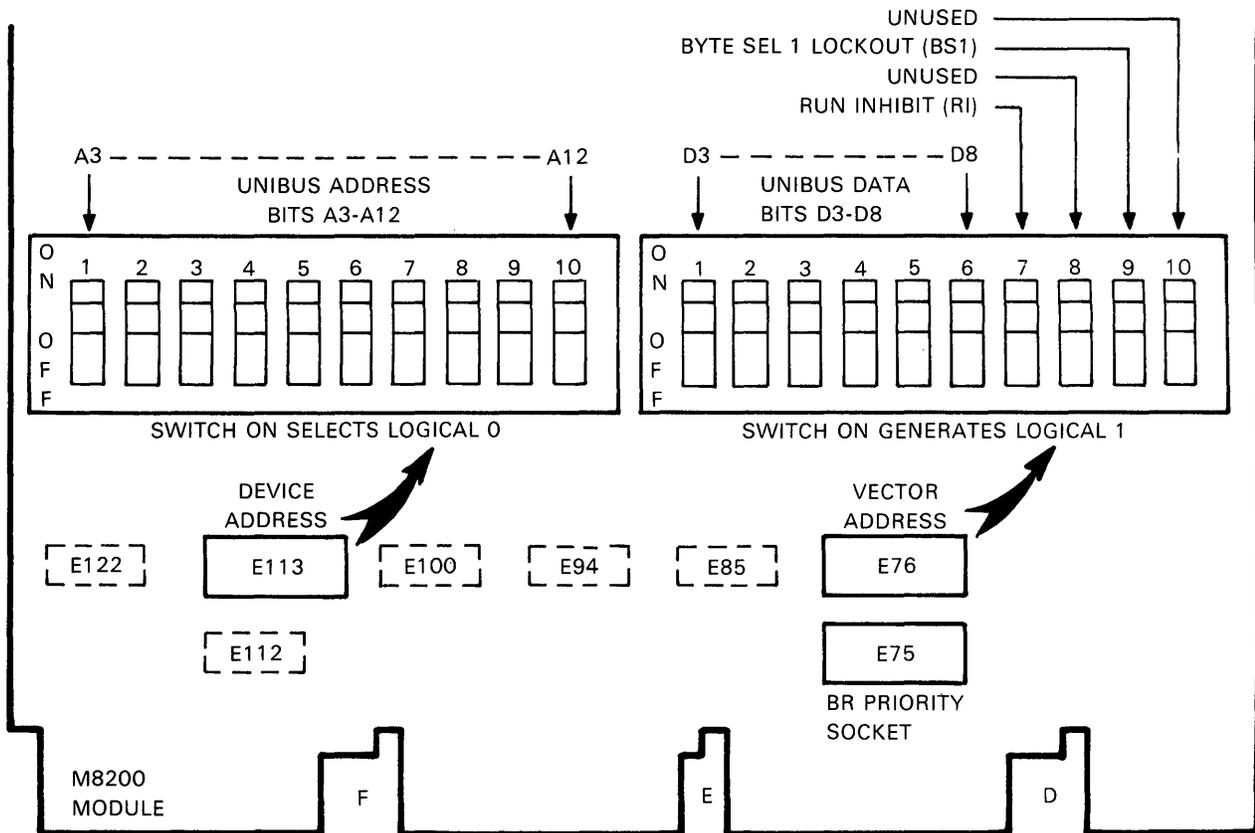
Figure 2-1 Microprocessor Device and Vector Address Switches

Table 2-5 Guide for Setting Switches
to Select Vector Address

| Switch No. | 6 | 5 | 4 | 3 | 2 | 1 | Vector |
Bit No.	8	7	6	5	4	3	Address
		ON	ON				300
		ON	ON			ON	310
		ON	ON		ON		320
		ON	ON		ON	ON	330
		ON	ON	ON			340
		ON	ON	ON		ON	350
		ON	ON	ON	ON		360
		ON	ON	ON	ON	ON	370
	ON						400
							--
	ON		ON				500
							--
	ON	ON				600	
							--
	ON	ON	ON				700

- Switch is ON (closed) to produce a logical 1 on the UNIBUS.

- Switch numbers are physical positions in switch package 2.

7. **Refer to vector address DIP - E76 in Figure 2-1.** Verify that switches 7 and 9 are both OFF.

- RUN INHIBIT (RI) switch 7 is normally set to OFF. Initialization of the micro-processor directly sets the RUN flip-flop which allows the microcode to be executed immediately. If there is an internal malfunction or execution of a faulty microcode, it is possible for the DMC11 to hang the bus. In this case, it would not be possible to load the diagnostics to determine the fault. Placing the RUN INHIBIT switch 7 to ON clears the RUN flip-flop and allows the diagnostics to be loaded.

- BYTE SEL1 LOCKOUT switch 9 inhibits all maintenance functions and capabilities to allow the PDP-11 program to directly clear the RUN bit and halt the micro-processor.

NOTE
Some diagnostics will not run if switch 7 and/or switch 9 are ON.

- Switches 1 through 6 are used for the vector address.

- Switches 8 and 10 are not used.

8. **Verify that the 8 ROMS** in the upper right-hand corner of M8200-YX are of the correct number and installed in the proper location.
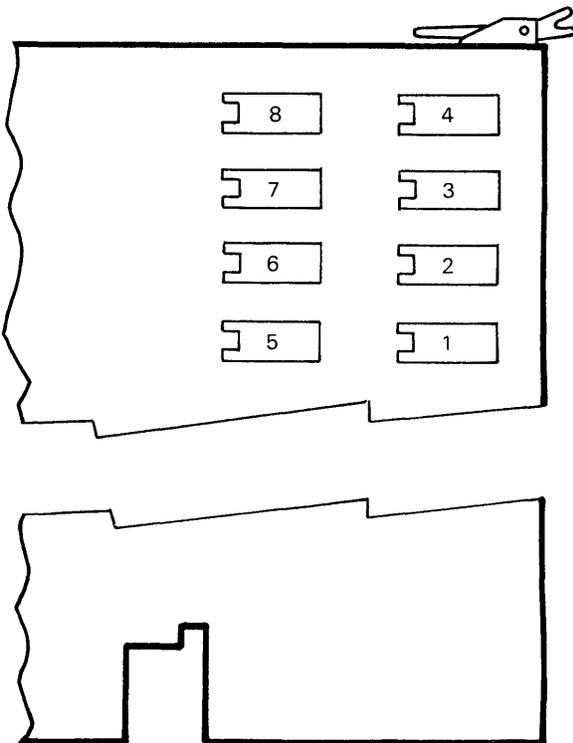
	REMOTE M8200-YA	LOCAL M8200-YB
ROM 1	630A9	622A9
ROM 2	631A9	623A9
ROM 3	632A9	624A9
ROM 4	633A9	625A9
ROM 5	634A9	626A9
ROM 6	635A9	627A9
ROM 7	636A9	628A9
ROM 8	637A9	629A9

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9. **Verify that the BR5 priority plug** on the M8200-YA/YB module is installed properly.

10. **Set up and check all appropriate switch settings and jumpers** on the M8201 or M8202-YA/YD line unit in accordance with the recommendations in Chapter 2 of the *DMC11 IPL Synchronous Line Unit Maintenance Manual* (EK-DMCLU-MM-002).

11. **If the DMC11 is to be set up for Remote Load Detect (RLD) application, refer to Appendix F** for proper switch settings of SW2 and SW3 on the M8201/M8202-YA/YD line unit module.

- SW2   E87 on M8201
         E90 on M8202

- SW3   E88 on M8201
         E91 on M8202

12. **Refer to** *DMC11 IPL Synchronous Line Unit Maintenance Manual* (Part no. EK-DMCLU-MM-002) for additional details concerning switch and jumper configurations for M8201 and M8202 modules.

2.6.2 Installation Procedures

Additional illustrations relevant to the following procedures and figures are contained in the DMC11 Engineering Drawings (DMC11-0-8). Perform the following steps taking every precaution in routing the cables and inserting the modules to ensure that cable wires are not broken (in the cable bending process) and that ROM chips and the BR plug are not unseated by contact with adjacent modules.

1. Power down the system.

2. Using cable BCO8S-1/BCO8R-1 (which is a one-foot long, 40 conductor, flat mylar cable with H856 female connectors at each end), insert one end of the cable into the H854 male connector on the M8200-YA/YB microprocessor module, as illustrated below.
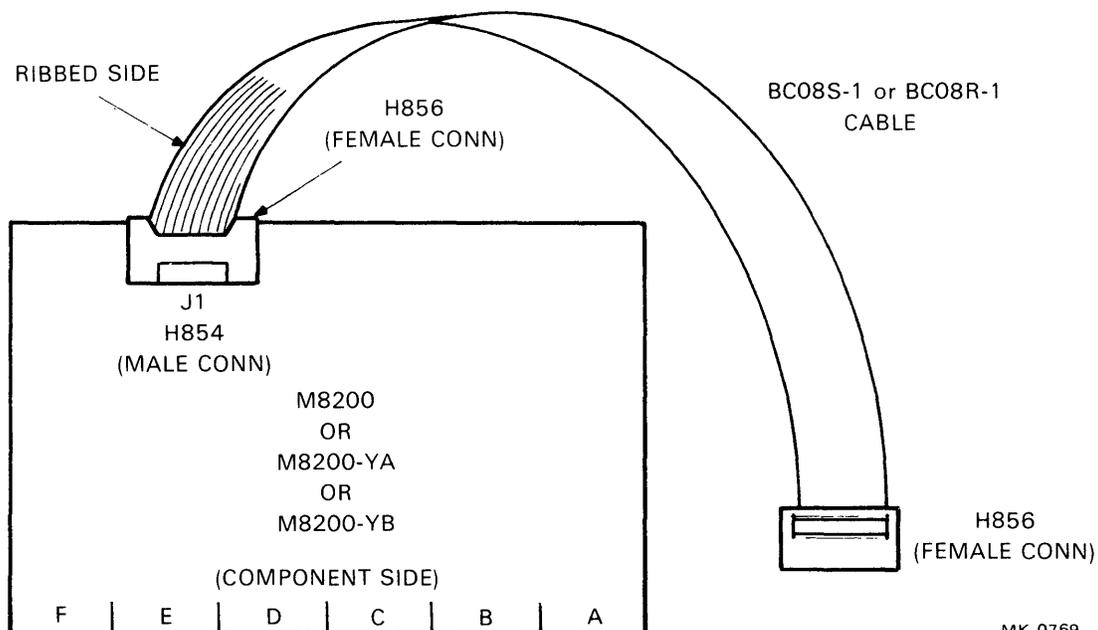
Figure 2-2   Inserting BC08S-1/BC08R-1 Cable into Microprocessor

LIFT TAB
TO OPEN

LOCK TAB

M8200
OR
M8200-YA
OR
M8200-YB
SIDE 1

COMPONENT SIDE

RIBBED
SIDE

BC08R-1
or
BC08S-1
CABLE

J1

LOCK TAB

TO OPEN

SLIDE INTO
MICROPROCESSOR
SLOT

BACKPLANE

A B C D E F

- LIFT TAB LOCKS OPEN AS SHOWN
- SLIDE BOARD IN SLOWLY.
- AVOID HITTING ADJACENT
  MODULE TO PROTECT
  ROM CHIPS AND BR PLUG.
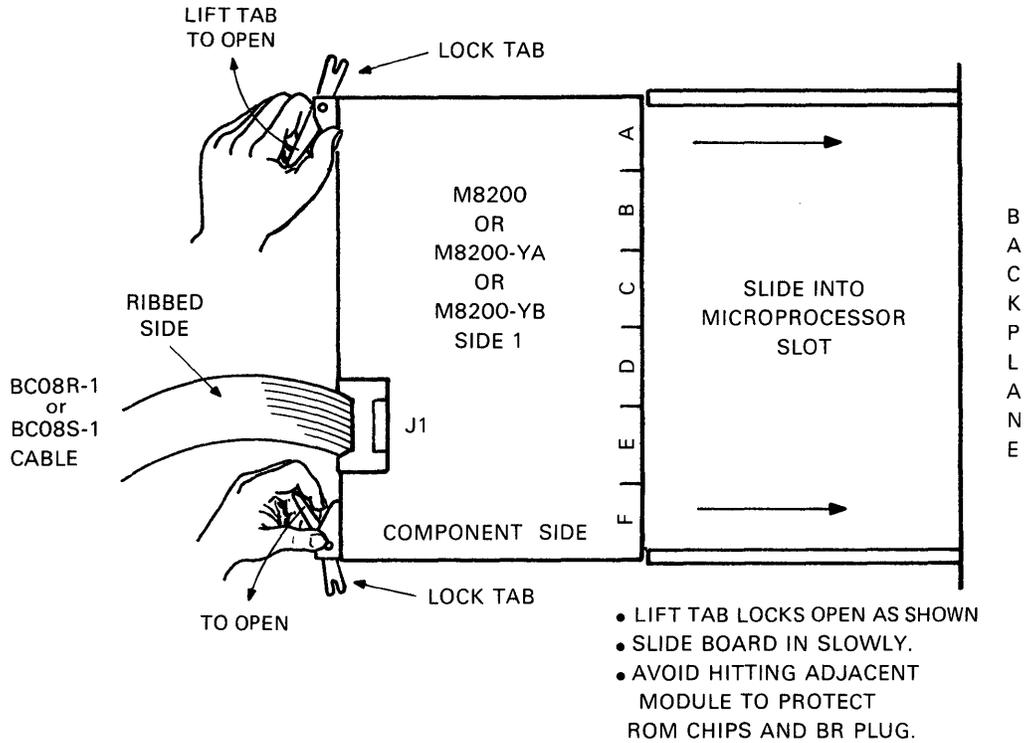
MK-0770

Figure 2-3   Inserting Microprocessor Module (View 1)

VIEW 2

- ENSURE THAT
  MODULE IS PROPERLY
  SEATED.
- PRESS LOCK TABS
  AS SHOWN.

PRESS

M8200
OR
M8200-YA
OR
M8200-YB
SIDE 1

BACKPLANE

A B C D E F

BC08R-1
or
BC08S-1
CABLE

J1

PRESS

COMPONENT SIDE
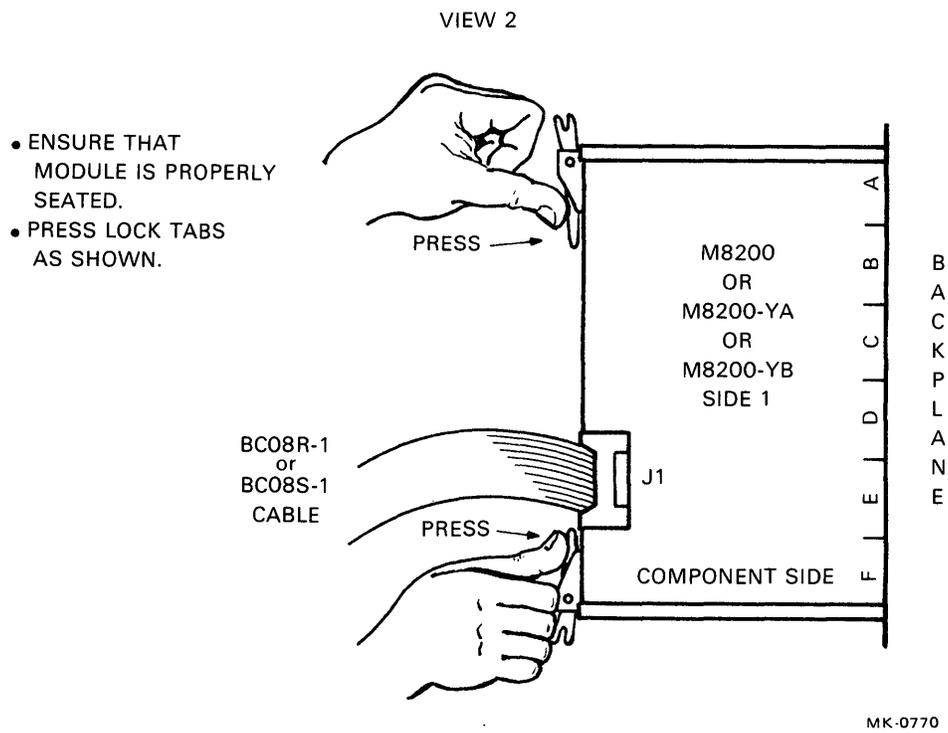
MK-0770

Figure 2-4   Inserting Microprocessor Module (View 2)

2-16

3. Locate the proper backplane slot and remove the NPG wirewrap jumper between backplane pins CA1 and CB1.

NOTE
The NPG wire must be replaced if the micro-processor is removed from the system.

4. Insert the microprocessor module M8200-YA/YB into the proper backplane slot as shown in views 1 and 2 which follow (see Figure 2-6).

5. Locate the proper backplane slot and insert line unit module M8201 or M8202-YA approx-imately three-quarters of the way into the slot as shown in the following illustration.

NOTE
Before installing the line unit module, ensure that the jumpers and switches are set correctly for current in-stallation.

Considerations:

a. Module type (SP1)

b. Satellite operation requiring RLD capability,

SP2 = PASSWORD
SP3 = BOOT OFFSET

c. Physical half- or full-duplex configuration, W6 on M8202 type line unit

6. Interconnect the line unit and microprocessor by connecting the opposite end of BC08S-1/BC08R-1 cable into the line unit as shown in the previous illustration.

7. Install a BC05C-25 or BC05Z-25 cable into J2 on the M8201 line unit (see Figure 2-6). The BC05Z-25 cable is a heavier cable and more difficult to route. Ensure that the connector for either cable is inserted properly; proper orientation is simplified by the label, "this side up" provided on the connector. The M8202 contains coaxial cables that are soldered and strain-relieved on the module.

8. Slowly insert the line unit the remaining distance into the slot. Ensure that the module is seated properly.

9. Route the cables as shown in Figure 2-6.

• Allow enough slack on the cables to avoid any sharp bends in any cables. Notice the long loop recommended in Figure 2-6.

• Excess cable length of the BC08S-1/BC08R-1 must be folded very carefully and placed against appropriate module as shown in Figure 2-6.

NOTE
Steps 11 and 12 are required for checkout pro-cedures.

LINE UNIT
3/4 OF THE WAY IN SLOT

1   LINE UNIT

J2
ON M8201

I/O CABLE

MICROPROCESSOR

SMOOTH
(SHIELDED)
SIDE

H854

J1

BC08R-1 or BC08S-1
CABLE

J1

RIBBED
SIDE

B
A
C
K
P
L
A
N
E

A
B
C
D
E
F
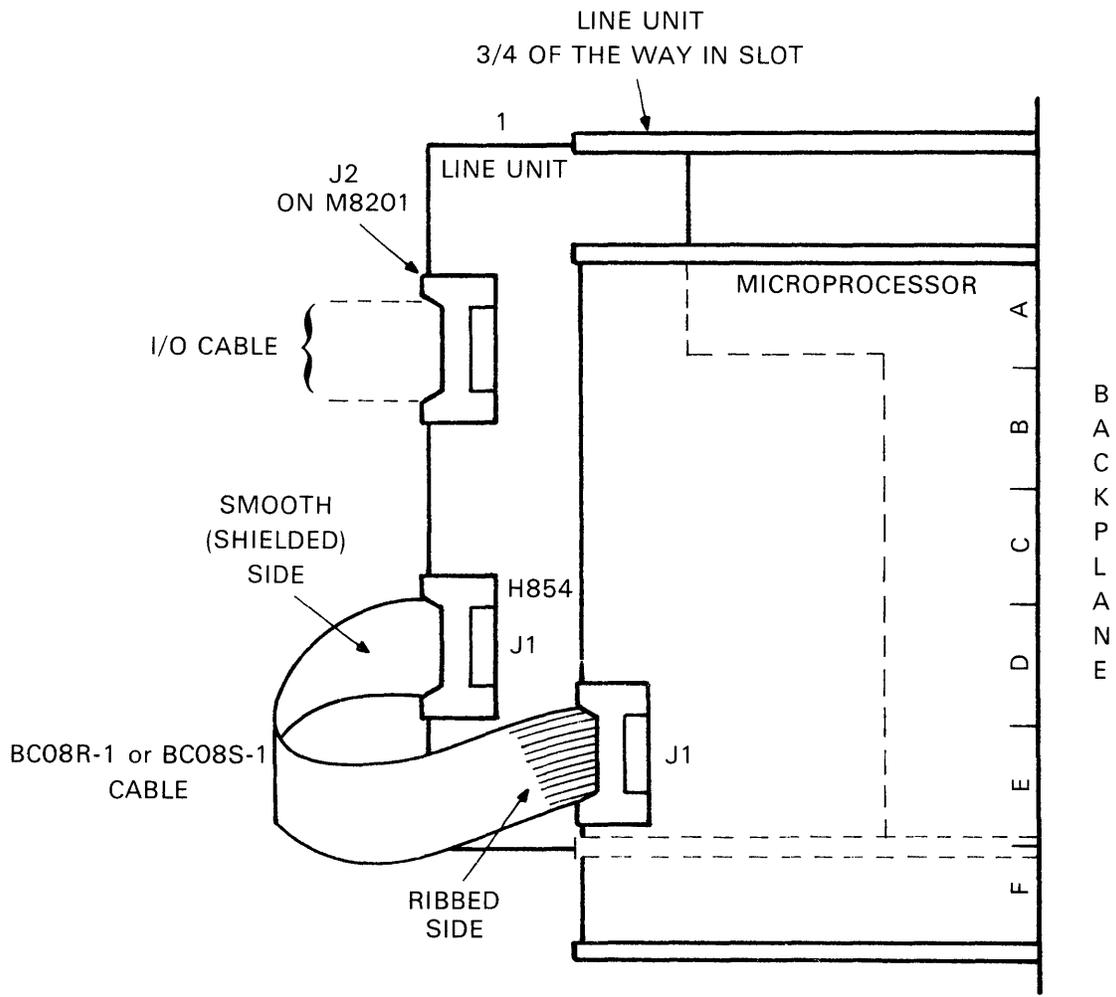
MK-0771

Figure 2-5   Inserting Line Unit Module and BC08S-1/BC08R-1 Cable

2-18

SIDE VIEW OF BA11-F BOX

SEE FIGURE 2-3

SEE FIG. 2-5
LOCAL APPL
HALF - FULL
DUPLEX

REC

J2

M8201
LU

M8200-YA
μP

M8200-YB
μP

M8202-YA
LU

XMIT

T2

M8202-YA
COMP. SIDE

XMIT

DD11-B/C
4-SLOT BACKPLANE

A THIS SIDE UP UU

BC05C-25
OR
BC05Z-25
CABLE
(SEE FIGURE 2-3)

M8201
LINE UNIT

BC08S-1 or BC08R-1
1 FOOT CABLES
FLAT MYLAR

M8202-YA
LINE UNIT

UPS

FOLD EXCESS
CABLE
AGAINST
LU MODULE

FOLD EXCESS
CABLE AGAINST
LU MODULE

J1   J1   J1   J1

NOTE:
    IF SPACE IS NOT AVAILABLE TO FOLD
    BC08S-1 CABLES AGAINST LINE UNIT
    MODULE, EXTEND EXCESS CABLE ALONG
    EDGES OF MODULES. EXERCISE CAUTION
    TO AVOID DAMAGING CABLES WHEN
    CLOSING DRAWER.

MK-0772

Figure 2-6   Typical Cable Routing (BA11-F Box)

10. Power up the system. At the proper backplane pins, ensure that the power supply voltages are within the tolerances given in Table 2-3.

11. Tie the two coaxial pigtails together via a 12-12528 test connector. See M8202-YA/YD in Figure 2-7. This is unnecessary if HDX and W6 on the M8202 are installed.

12. Connect M8201 cables to the respective test connectors as shown in Figure 2-7.

2.6.2.1 Installation in a BA11-K Box – The installation procedure for modules and associated cabling is similar to the one given in Section 2.6.2. Cable routing is less of a problem because the cables exit the module from the handle edge, requiring less cable bending en route to exiting the expander box. More space is available at the top of the drawer, allowing ease in cable routing without the need for sharp bending and close fitting of the cables, particularly when a BC05Z-25 one-inch diameter cable is installed.

2.6.2.2 Installation in a DD11-D Backplane – The DD11-D is a nine-slot backplane (see Figure 2-8). When installing the modules in the DD11-D, follow the cable routing procedures and exercise caution as indicated in Section 2.6.2.
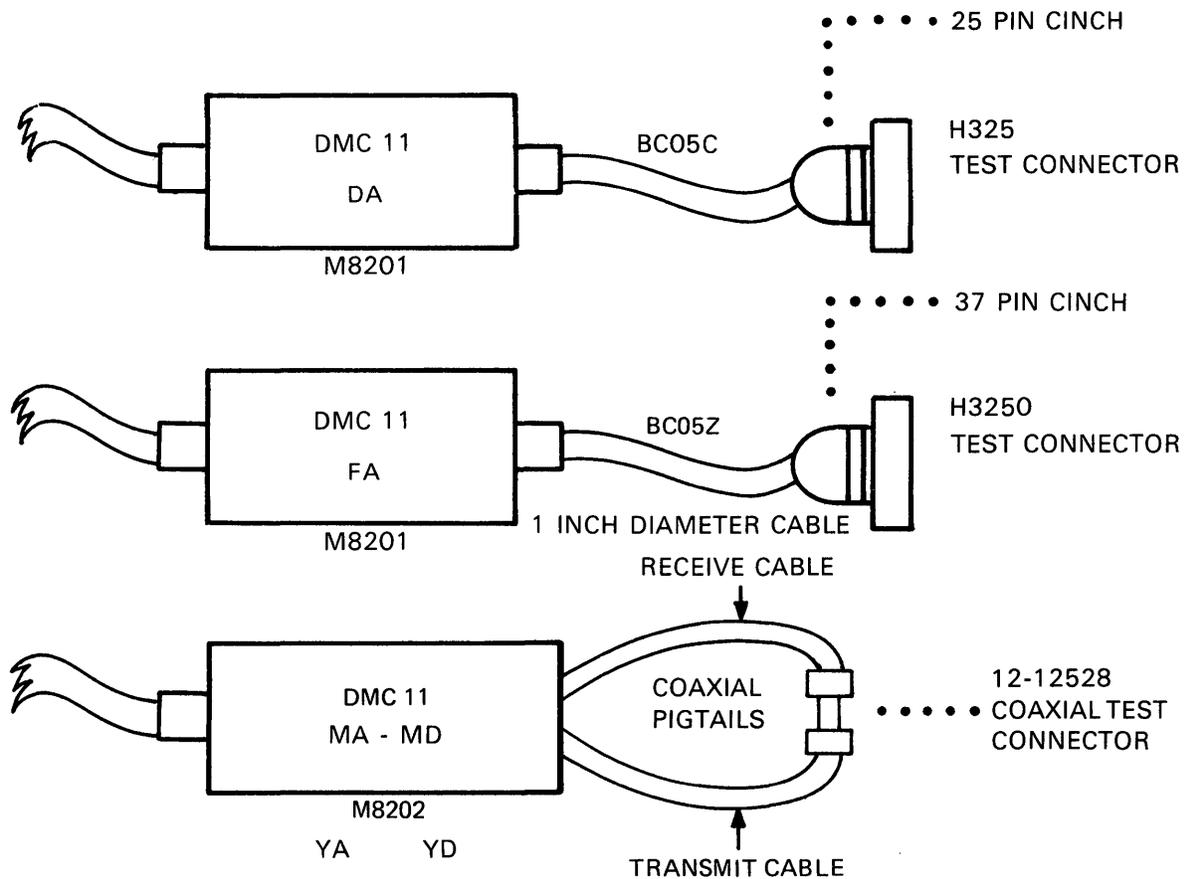
MK-0773

Figure 2-7   DMC11 Line Unit Turnaround Test Connectors

2-20

SLOTS

```
        9   8   7   6   5   4   3   2   1
```

VIEWED
FROM MODULE
HANDLES
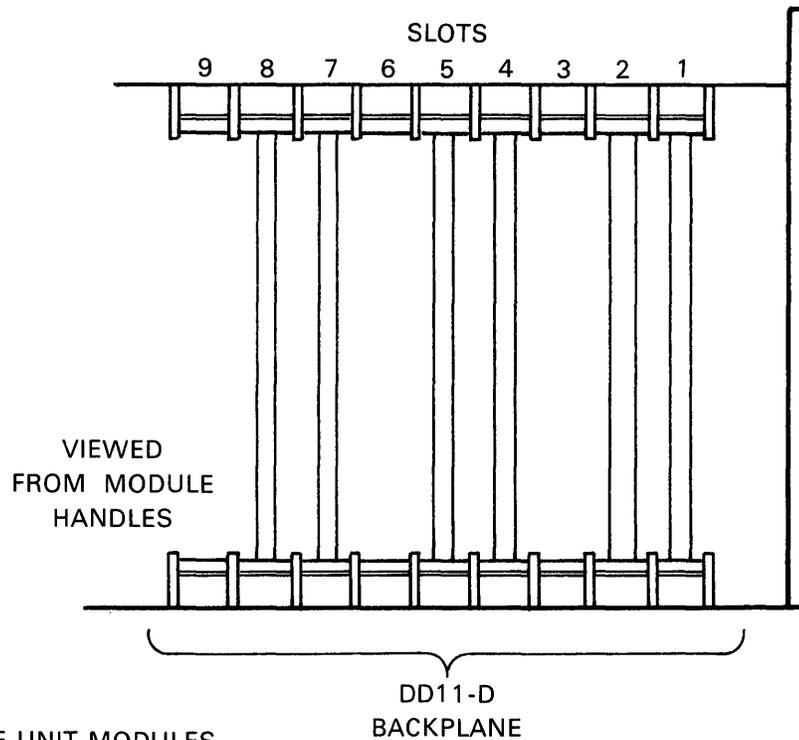
DD11-D
BACKPLANE

SLOTS 1, 4, 7 = LINE UNIT MODULES
SLOTS 2, 5, 8 = MICROPROCESSOR MODULES
NOTE: INSTALL MODULES AND
 ROUTE CABLES WITH CARE
 AS INDICATED IN PREVIOUS
 SECTIONS.

MK-0774

Figure 2-8 DD11-D Backplane

The nine slots available in the DD11-D imply that four sets (each set being a microprocessor and a line unit) can be installed. However, as each set draws approximately 8 amps, four sets may create unserviceable cable routing as well as an overloading problem on certain power supplies. It is recommended that a maximum of three DMC11 sets be installed in a given DD11-D. Slot selection for a three-set installation is shown in Figure 2-8.

2.6.3 Checkout Procedure

1. Run the following diagnostic programs (with the test connector installed) to ensure proper operation of the microprocessor and line unit (see Chapter 5). Each program should be run through at least three passes with zero in the console switch register.

 CZDMC DMC11 basic W/R and microprocessor tests

 CZDME DMC11 DDCMP mode line unit tests

 DZDMF DMC11 bit stuff mode line unit tests

 CZDMG DMC11 CROM and Jump Test

 DZDMH DMC11 free-running tests

2. Run the DEC/X11 System Exerciser with the CXDMCB0, DMC-11 module to ensure proper system level operation.

NOTE

1. **To fully exercise the system under DEC/X11 as configured above, it is recommended that bit 0 of switch register No. 1 (SR1) be set to 1 and test connector H325, H3250, or 12-12528 be installed. This sets the DMC11 to run in external loopback mode. The data rate for the M8201 is 10K bps and for the M8202-YX is the integral modem speed.**

2. **An interpretation of a "soft error" as reported by DEC/X11 is provided in Chapter 5 of this manual.**

3. Remove test connector H325, H3250, or coaxial test connector 12-12528 from the end of the cable.

4. Connect the modem cables to the modem or another DMC11 as shown in Figure 2-9. For the M8201 line unit, connect to the modem. For the M8202-YA/YD, connect to another DMC11.

5. Run the Interprocessor Link Test program to ensure proper installation of the cables and proper operation of the communication channel. Refer to Appendix G for the Link Test procedure.
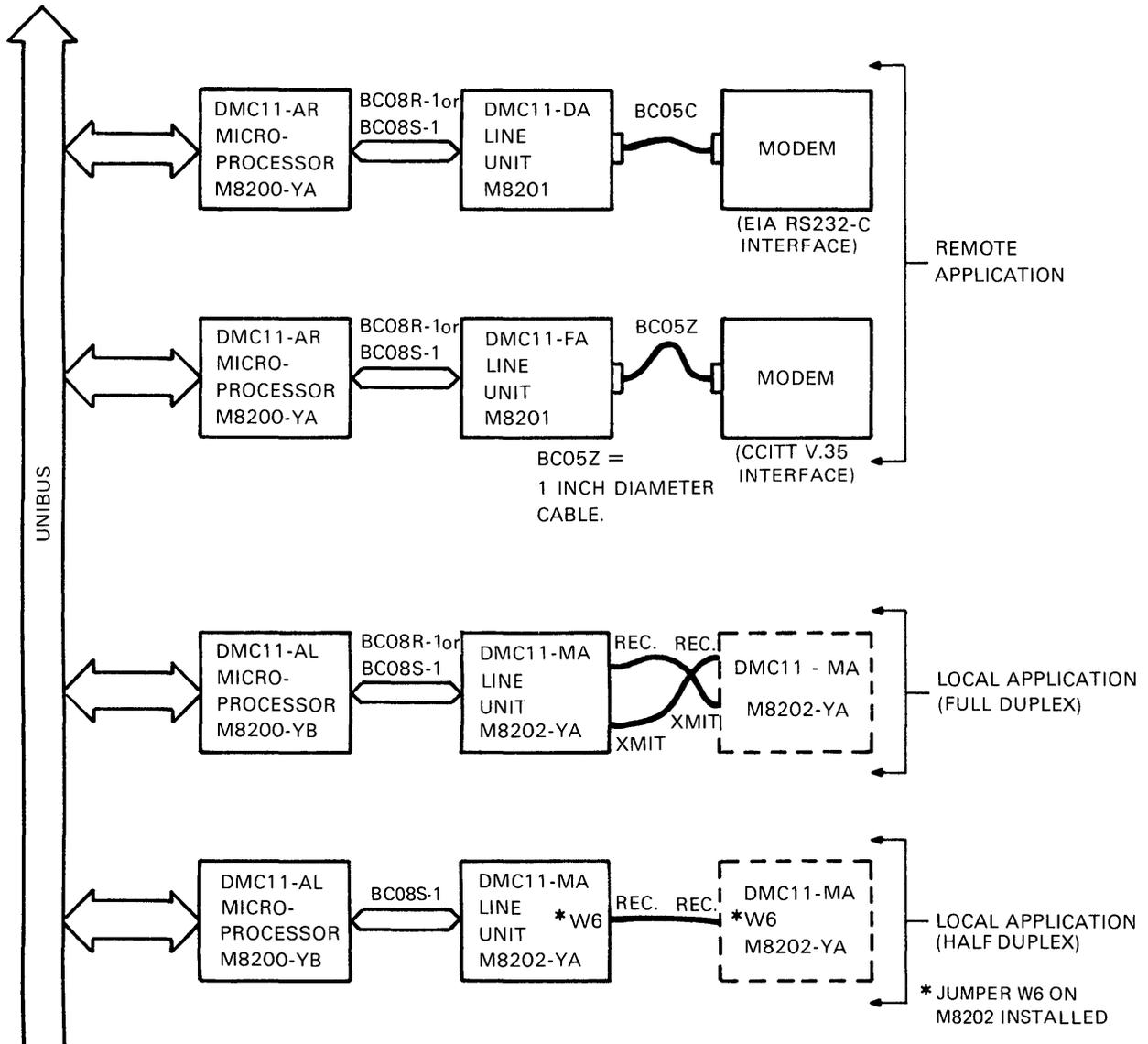
Figure 2-9   DMC11 Cabling

CHAPTER 3
PROGRAMMING INFORMATION

3.1 INTRODUCTION
This chapter contains general information necessary for PDP-11 programming of the DMC11 microprocessor. The information is presented by operational categories such as input transfers and output transfers. Also included are descriptions of the UNIBUS control and status registers, microprocessor control and status registers, and line unit control and status registers. The following major areas of concern are discussed.

- Interrupt vectors

- Priority selection

- PDP-11 programming information

- DMC11 programming information

3.2 INTERRUPT VECTORS
The DMC11 generates two vector addresses: XX0 and XX4.

An interrupt through vector address XX0 is generated by the microprocessor when:

1. The PDP-11 has set IEI,
2. The PDP-11 requests the port (SEL 4 and 6) for input of a command to the DMC11, and
3. The port becomes available, that is, no output command pending and the microprocessor has no higher priority functions to perform (such as transmit and receive data processing).

The XX0 interrupt occurs in conjunction with the setting of READY IN (RDI).

An interrupt through vector address XX4 is generated by the microprocessor when:

1. The PDP-11 has set IEO,
2. The microprocessor has status or error information to give to the PDP-11 (it has placed the information in port SEL 4 and 6), and
3. The microprocessor has no higher priority functions to perform (such as transmit or receive data processing).

The XX4 interrupt occurs in conjunction with the setting of READY OUT (RDO).

3.3 PRIORITY SELECTION
The priority for the interrupts is selectable on the microprocessor via a plug-in priority selection plug. The microprocessor is shipped with a plug that establishes BR5 as the priority level.

3.4 PDP-11 PROGRAMMING INFORMATION

Programming DMC11s is simplified in that the DMC11 implements the DDCMP (Digital Data Communication Protocol) in the DMC11 microprogram. Although thorough understanding of the DDCMP is not required, some familiarity with the protocol operation is useful in interpreting the significance of the various error counters provided to assess the quality of the circuit connecting the two computers. If a DMC11 is to communicate with a different communication device which uses a software implementation of DDCMP, the person programming the software implementation should consult the DDCMP standard document, *DDCMP*, version 4.0 (Order No. AA-D599A-TC), and Appendix I.

3.4.1 UNIBUS Control and Status Registers

Communication of control and status information between the PDP-11 and the DMC11 is accomplished through four 16-bit UNIBUS Control and Status Registers (CSRs). These registers are both byte and word addressable. The eight bytes composing the four registers are assigned the following addresses: 76XXX0, 76XXX1, 76XXX2, 76XXX3, 76XXX4, 76XXX5, 76XXX6, and 76XXX7, with the word addresses being the four even numbered addresses. The eight byte addresses are designated BSEL0 through BSEL7 and the four word addresses are SEL0, SEL2, SEL4 and SEL6. The symbolic addresses and format of the CSRs are shown in Figure 3-1.

3.4.2 Command Structure

The command set for the DMC11 can be categorized as input and output commands. As opposed to received and transmitted data, input commands are issued to the DMC11 by the main CPU; output commands are issued to the main CPU by the DMC11.

3.4.2.1 Input Commands – Input commands provide the vehicle for the main CPU to initialize, set up, and assign receive or transmit buffers to the DMC11. These commands are listed below in the correct order of user program issuance.

Initialization	is used to MASTER CLEAR the DMC11 and place it in the initialized state.
Base In	is the only command allowed to be assigned to the DMC11 after initialization; it allows the DMC11 to enter the DDCMP start-up states.
Control In	is used to set the DMC11 in either half-duplex or full-duplex mode, and maintenance or normal mode.
Buffer Address In	is used to assign transmit or receive buffers to the DMC11.

Detailed format and field descriptions of each command are provided in Section 3.4.3.

The PDP-11 program requests the data port (SEL 4 and 6) for input commands by setting REQUEST IN (RQI), Bit 5 of BSEL 0. The DMC11 grants the request by setting READY IN (RDI), B7 of BSEL 0. The setting of RDI by the microprocessor may be delayed by any of the following conditions.

- The DMC11 is using the data port for output commands.

- For a full-duplex DMC11, the DMC11 may be busy receiving and transmitting data such that servicing of input commands or supplying output commands is delayed.

3-2

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
BSEL 1	RUN	MCLR	/////	STEP LU	LU LOOP	ROM 0	ROM 1	STEP UP	RDI	IEI	RQI	/////	/////	IN RCV	INPUT COMMAND		BSEL 0 SEL 0
BSEL 3	/////////////////////////////////								RDO	IEO	/////	/////	/////	OUT RCV	OUTPUT COMMAND		BSEL 2 SEL 2
BSEL 5																	BSEL 4 SEL 4
BSEL 7	DATA PORT FOR BA/CC, BASE, AND CNTL FORMATS																BSEL 6 SEL 6
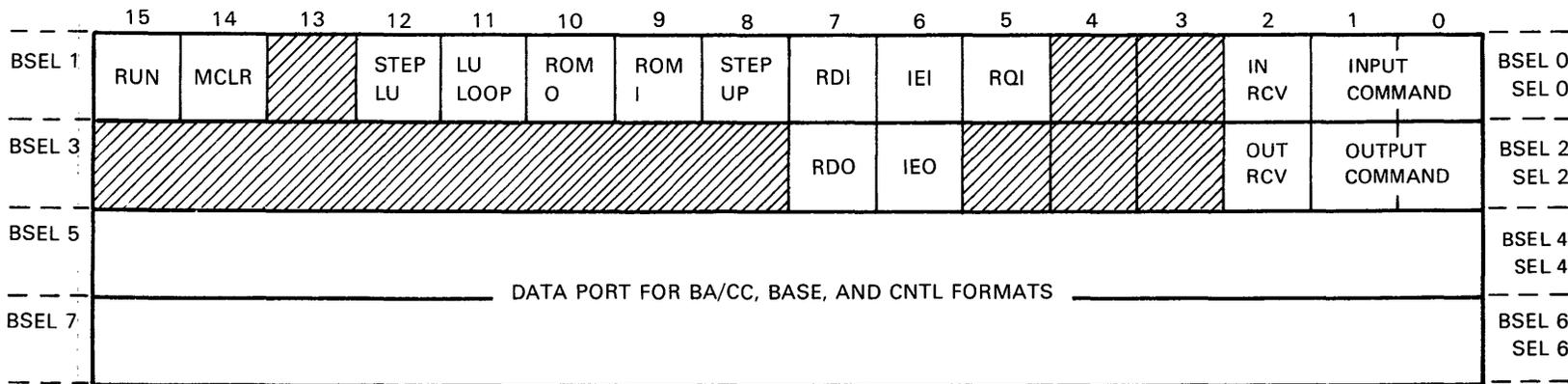
MK-0776

Figure 3-1 Unibus Control and Status Registers (CSRs) (Symbolic Addresses and Formats)

3.4.2.2 Output Commands – Output commands provide the vehicle for the DMC11 to provide information to the main CPU. DMC11 uses the output commands to convey two categories of information:

Buffer Address Out is used to post normal completions of transmit or receive operations to the user program.

Control Out is used to convey the detection of error conditions.

Detailed format and field descriptions for each command are provided in section 3.4.4.

3.4.2.3 CSRs Bit Assignments – The four 16-bit CSRs are both word and byte addressable. Bytes BSEL 0, 1, and 2 are used to set up input commands, maintenance bits, and output commands; BSEL 3 is not used. Bytes BSEL 4, 5, 6, and 7 are data ports which are defined in greater detail in the following sections. Figure 3-2 is a summary of the control and status registers and data port usage for input and output commands.

NOTE
The control and status registers are implemented with Random Access Memory (RAM). At power on, the CSRs all come up as ones. As part of the microprocessor initialization microprogram, only bytes BSEL 0, 1, and 2 are cleared. Then, bit 15 of SEL 0 (RUN) is set by the microprogram at the end of its initialization subroutine. SEL 0 must not be written by the PDP-11 until bit 15 has been set by the microprogram.

3.4.2.4 BSEL 0 – Input Register – BSEL 0 is the low byte of address 76XXX0 (see Figure 3-2). Table 3-1 describes the bit functions of BSEL 0.

3.4.2.5 BSEL 1 – Maintenance Register – BSEL 1 (maintenance register) is the high byte of address 76XXX0 (Figure 3-2). Switch #9 (E76) on the microprocessor module, BSEL 1 LOCKOUT (normally OFF), can be turned on to prevent the PDP-11 program from directly setting or clearing RUN, or performing other maintenance functions in BSEL 1. BSEL 1 LOCKOUT disables the DMC11's capability to initialize an unattended PDP-11 computer system, but does not inhibit the program MASTER CLEAR (bit 14). Table 3-2 describes the bit functions of BSEL 1.

NOTE
During program access of BSEL1, care must be taken to avoid inadvertent clearing of the RUN bit. This stops the MP clock, stopping the DMC11.

3.4.2.6 BSEL 2 – Output Register – BSEL 2 is the low byte of address 76XXX2 (Figure 3-2). This register contains control information relative to output command transfers from the DMC11 to the PDP-11 program. Table 3-3 describes the bit functions of BSEL 2.

3.4.2.7 BSEL 3 – Reserved – This register is not used.

3.4.2.8 Base Input (BASE I) Command Format – SEL4 and bits 14 and 15 of SEL6 provide the first address of a reserved block of addresses in the PDP-11 memory (see Figure 3-2). The block size is 256 bytes. Upon assigning the BASE I address to the microprocessor, the PDP-11 program must not modify any locations within the assigned block.

Bit positions: 11 10 9 8 7 6 5 4 3 2 1 0

SEL 0 register: bit 7 = RDI, bit 6 = IEI, bit 5 = RQI, bits 4–3 = (reserved/hatched), bit 2 = IN RCV, bits 1–0 = INPUT COMMAND
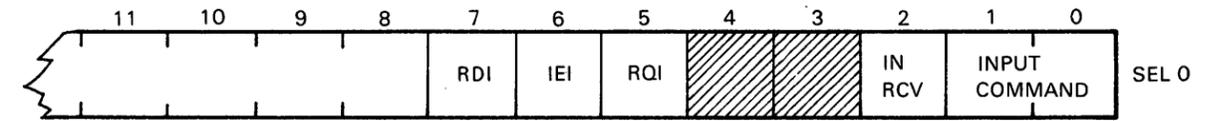
INPUT COMMAND	IN RCV BIT 2	INPUT COMMAND BIT 1	BIT 0
BASE IN	0	1	1
CONTROL IN	0	0	1
RECEIVE BUFFER/CC IN	1	0	0
TRANSMIT BUFFER/CC IN	0	0	0

BASE IN COMMAND FORMAT

SEL 4: BUS ADDRESS

SEL 6: BA17,16 | (hatched) | RE-SUME | (hatched) ...

CONTROL IN COMMAND FORMAT

SEL 4: (hatched)

SEL 6: ... DDCMP HD | (hatched) | DDCMP MAINT | (hatched) ...

BUFFER ASSIGNMENT (BA/CC IN) COMMAND FORMAT

SEL 4: BUS ADDRESS

SEL 6: BA 17,16 | CHARACTER COUNT

DATA PORT USAGE
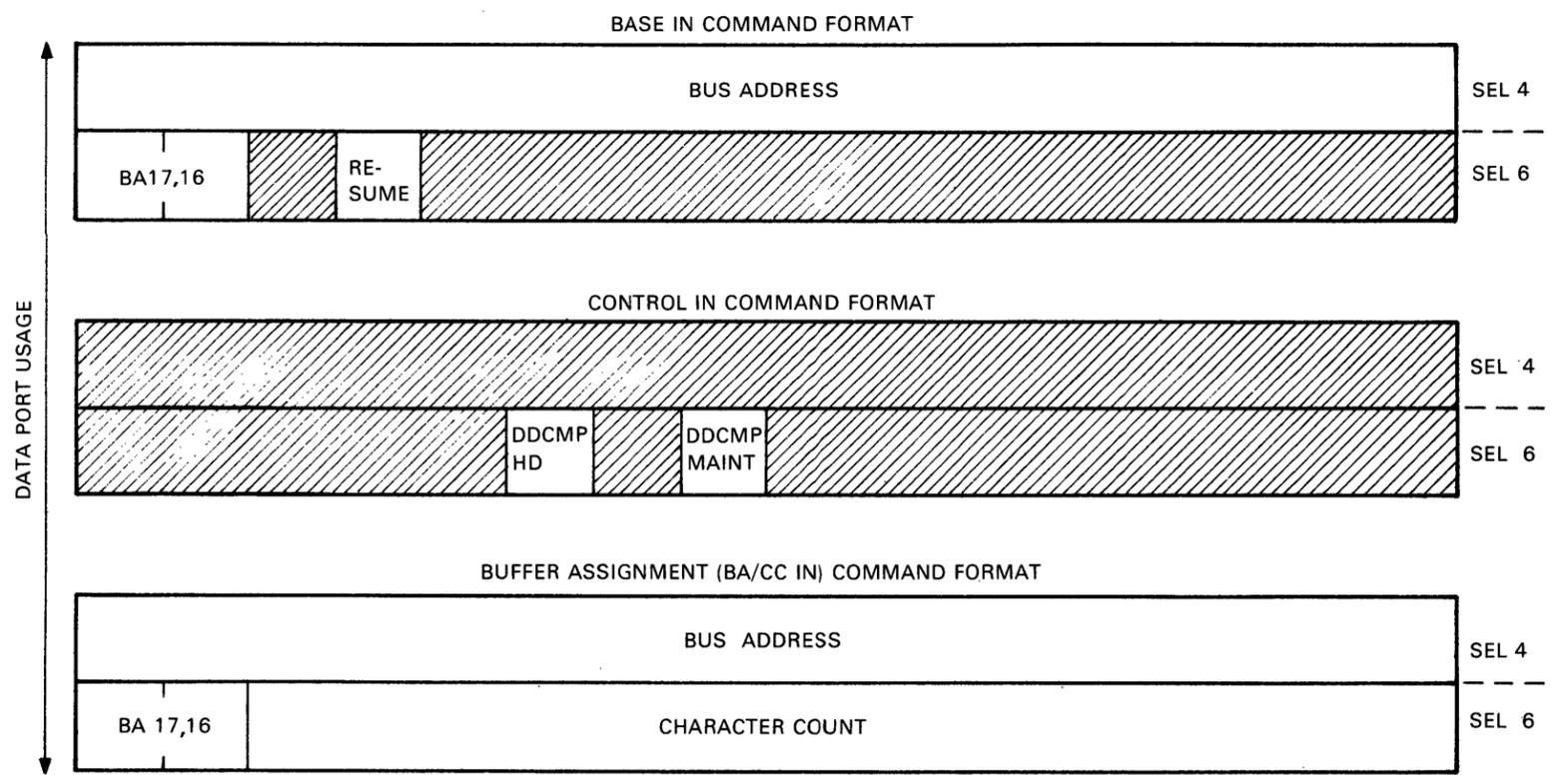
MK-0777

Figure 3-2 Summary of Control and Status Registe
Input Commands (Sheet 1 of 2)
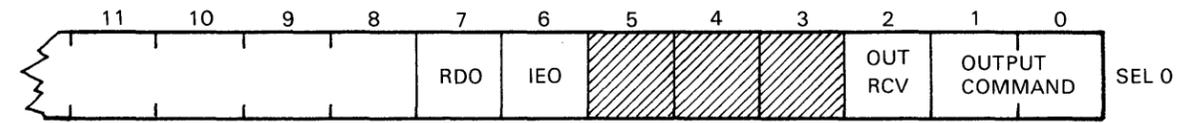
		OUT RCV BIT 2	OUTPUT COMMAND BIT 1	BIT 0
OUTPUT COMMAND				
CONTROL OUT		0	0	1
RECEIVE BA/CC OUT		1	0	0
TRANSMIT BA/CC OUT		0	0	0

CONTROL OUT COMMAND FORMAT

BUFFER ASSIGNMENT (BA/CC OUT) COMMAND FORMAT
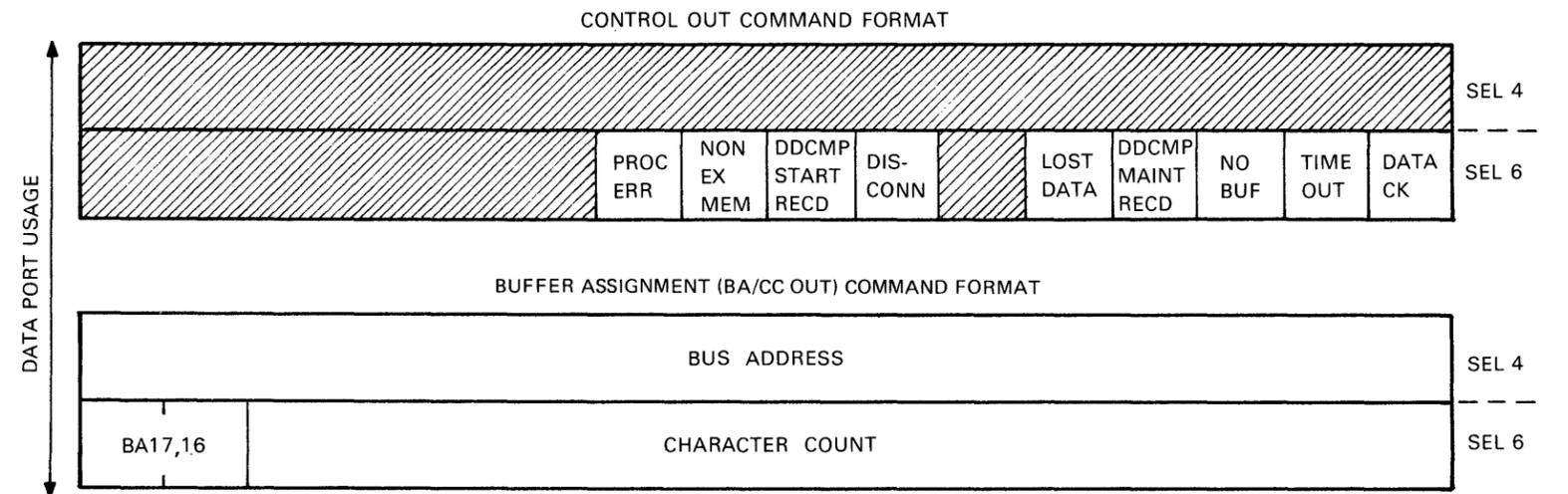
MK-0778

Figure 3-2 Summary of Control and Status Registers:
Output Commands (Sheet 2 of 2)

Table 3-1   BSEL 0 Bit Functions

Bits	Name	Description	Reference Section
0,1	Input command	These bits are encoded to define the type of input command from the PDP-11 program to the micro-processor.	3.4.3.2 3.4.3.3 3.4.3.4
2	IN RCV	Defines the PDP-11 buffer address (BA/CCI) command as either a transmit or receive operation: Clear "0" = transmit operation Set "1" = receive operaton Cleared by DMC11 upon completion of the input command transfer.	3.4.3.4
3,4	RESERVED	Not used (causes no action)	
5	REQUEST IN(RQI)	Serves as an interlock bit in requesting the use of the data port: Set by the PDP-11 to request use of the data port. Cleared by the PDP-11 when the data port has been loaded.	3.4.3.2 3.4.3.3 3.4.3.4
6	INTERRUPT ENABLE IN (IEI)	When set, allows the DMC11 to interrupt to vector address XX0 if RDI (bit 7 of BSEL 0) is set.	3.4.3.2 3.4.3.3 3.4.3.4
7	READY IN (RDI)	RDI is a DMC11 response to RQI indicating to the PDP-11 that it may load the data port (BSEL 4-7). Cleared by the DMC11 (following PDP-11 clearing of RQI) to indicate to the PDP-11 that the data port has been read and the input command transfer is complete.	3.4.3.2 3.4.3.3 3.4.3.4

Within the "Input command" description (Bits 0,1):

Bit 1	Bit 0	Definition
0	0	Buffer Address/ Character Count In (BA/CCI) command
0	1	Control In (CNTL I) command
1	0	Reserved
1	1	Base Input (BASE I) command

Table 3-2 BSEL 1 Bit Functions

Bit	Name	Description
8–12	Maintenance Bits	Reserved for maintenance use. (Refer to Chapter 5, Section 5.2, for bit descriptions.)
13	RESERVED	
14	MASTER CLEAR (MCLR)	When set, MASTER CLEAR initializes both the microprocessor and the line unit hardware (this bit is self-clearing). The microprocessor clock is enabled and the RUN bit is asserted. The DMC11 microcode is also placed in the initialized state.
15	RUN	Controls the microprocessor clock. This bit is set by BUS initialization or MASTER CLEAR which enables the microprocessor clock. RUN can be set or cleared for maintenance purposes from the UNIBUS.

Table 3-3 BSEL 2 Bit Functions

Bit	Name	Description
0, 1	Output Command	These bits are encoded to define the type of data transfer from the microprocessor to the PDP-11 program: Bit 1 Bit 0 Description 0 0 Buffer Address and Character Count Out (BA/CCO) 0 1 Control Output 1 0 Reserved 1 1 Reserved
2	OUT RCV	Defines a completed buffer (BA/CCO) by the DMC11 as either a transmit or receive. Clear "0" = transmit buffer Set "1" = receive buffer
3–5	RESERVED	
6	INTERRUPT ENABLE OUT (IEO)	When set, enables the DMC11, upon asserting RDO, to generate an interrupt to vector address XX4.
7	READY OUTPUT (RDO)	Asserted by the DMC11 to indicate that the data port (BSEL 4–7) contains data for the output command defined by bits 0–2 of BSEL 2. Bit 7 must be cleared by the PDP-11 program after the data port has been read.

Bit 12 of SEL6 is called RESUME. If this bit is clear when a BASE I command is assigned, the DMC11 is placed in the DDCMP start state. If set when a BASE I command is assigned, the microprocessor resumes DDCMP operation as specified by the contents of the Base Table in the PDP-11 memory. See Section 3.4.3.2 for BASE I information.

3.4.2.9 Control Input (CNTL I) Command Format – The CNTL I format provides a means of setting the DMC11 in half-duplex or full-duplex mode, normal or maintenance mode. The control bits are located in SEL 6 as shown in Figure 3-2 and described in Table 3-4. CNTL I must be executed following BASE I.

**Table 3-4   SEL 6 Bit Functions Associated
with Control In**

Bit	Name	Description
0–7	RESERVED	Unused
8	DDCMP MAINTENANCE (DDCMP MAINT)	When set by the PDP-11, the microprocessor enters the DDCMP maintenance code where it remains until it is subsequently initialized.
9	RESERVED	
10	DDCMP HALF-DUPLEX (DDCMP HD)	When set, DDCMP half-duplex operation is selected. When cleared, DDCMP full-duplex operation is selected.
11,12,13	RESERVED	

3.4.2.10   Buffer Assignment (BA/CCI and BA/CCO) Command Formats – The formats for BA/CCI and BA/CCO are the same (see Figure 3-2). SEL4 contains the least significant 16 bits (0–15) of the 18-bit bus address (BA). The two most significant bits (16 and 17) of this address are contained in bits 14 and 15 of SEL6. The remaining 14 bits (0–13) of SEL6 contain the character count (CC) in positive notation, not 2's complement notation.

The microprocessor can stack a maximum of seven BA/CCs each for transmitting and receiving.

The BA/CCI command supplies new receive or transmit message buffers to the microprocessor.

For buffer completion reporting, BA/CCO returns the receive or transmit buffers to the PDP-11 that were successfully transferred by the microprocessor.

For buffer assignment commands, the CC represents:

1.   The number of characters to be transmitted, or
2.   The maximum size of a receive buffer.

For buffer completion status, the CC represents:

1.   The number of characters in a buffer which was successfully transmitted, or
2.   The number of characters in a buffer which was received successfully.

3.4.2.11 Control Output (CNTL O) Command Format – The CNTL O command provides a means of informing the PDP-11 program of error conditions involving the DMC11 hardware, PDP-11 program, communications channel, or the remote station.

The control bits and associated octal error codes are located in SEL 6 as shown in Table 3-5.

3.4.3 Input Commands (Format Descriptions)
The DMC11 executes the following four forms of input commands (listed in the correct order of user program issuance):

- Initialization

- Base In

- Control In

- Buffer Address In

NOTE
The programming procedure flow charts provided in this section illustrate the non-interrupt mode for input command servicing. The intent is to demonstrate a way of programming the DMC11, but should not be interpreted as the only way.

The PDP-11 program should set bits 0–2 of BSEL 0 to indicate the type of transfer and set bit 5, RQI, to request the port. These bits may be set by a single instruction. The microprocessor responds by setting bit 7, RDI, when the port has been assigned to the PDP-11 program. When RDI has been set, the PDP-11 program should load the desired data into the data port (BSEL 4-7); then clears RQI. The microprocessor takes the data and clears RDI, which completes the transfer.

Bit 6 of BSEL 0, Interrupt Enable Input (IEI), controls whether the PDP-11 program receives an interrupt (to Vector XX0) when the microprocessor has set RDI. Because of interrupt and service time, it is most efficient for the PDP-11 program to have input interrupts disabled and simply scan RDI one or more times until it has been set by the microprocessor. While the PDP-11 program is waiting, it must be prepared to accept an output transfer because the microprocessor may have seized the port in the interim (which takes priority over input).

Use of interrupts is convenient if the PDP-11 program finds RDI clear after several scans; it can enable interrupts by setting IEI with a BIS instruction. Following the setting of IEI and while waiting for RDI, the PDP-11 should ensure that IEI was set successfully. The DMC11 interrupts the PDP-11 (to vector XX0) when the microprocessor has set RDI. The PDP-11 program gets the interrupt in all cases, even if the microprocessor has already set RDI at the time the program sets IEI. The program can bypass any scanning if IEI is set when the program sets RQI.

**Table 3-5 Sel 6 Bit Functions Associated
with Control Out**

Error Code (Octal)	Bit	Name	Description	Error Class
1	0	DATA CHECK	Indicates that a retransmission threshold has been exceeded at the receiving end. More than eight consecutive retransmissions have been requested via negative acknowledgements (NAKs) that were sent because of bad header, CRC, or bad data CRC, etc.	Non-fatal
2	1	TIME-OUT	Indicates that the DMC11 has not received a proper response for some outstanding messages from the remote end of the link for a specified period (time-out interval), a broken communications channel or a failure at either end of the link for a single outstanding message. This specified period is approximately eight reply timer intervals, normally about 24 seconds.	Non-fatal

NOTE
If the DMC11 is in half-duplex mode and a message is retransmitted 8 times due to receipt of a NAK for any reason (such as line noise or no buffer availability), then the timeout interval will be very short (approximately equal to the time required to retransmit eight times).

Error Code (Octal)	Bit	Name	Description	Error Class
4	2	NO BUF	Indicates that a message was received but no buffer was available; reported at receive end only.	Non-fatal

NOTE
The DMC11 will request retransmission via NAKS eight times before reporting this error.

Error Code (Octal)	Bit	Name	Description	Error Class
10	3	DDCMP MAINTENANCE RECEIVED	Indicates that a message in the DDCMP maintenance format has been received while running in normal DDCMP mode. The message causing this condition is lost and the PDP-11 must reinitialize the DMC11 to enter the maintenance mode.	Fatal
20	4	LOST DATA	Indicates that the received message is longer than the supplied buffer; reported at the receive end only.	Fatal
	5	RESERVED		

Table 3-5 Sel 6 Bit Functions Associated
with Control Out (Cont)

Error Code (Octal)	Bit	Name	Description	Error Class
100	6	DISCONNECT	Remote operation only; indicates that an ON-to-OFF transition of the modem Data Set Ready (EIA Interface Circuit CC) has been detected after the data link has been started.	Non-fatal
			NOTE **On applications using switched network services via dial-up modems, the ON-to-OFF transition of the Data Set Ready could mean the connection has been terminated and a redial or call setup is required.**	
200	7	DDCMP START RECEIVED	Indicates that a DDCMP start message was received when the protocol was in the running state.	Fatal
400	8	NON-EXISTENT MEMORY (NXM)	Indicates that a UNIBUS address time-out has occurred. This could have been caused by the PDP-11 program specifying an invalid transmit, receive buffer address, or count, by a defective PDP-11 memory or other hardware error. This error will only be reported at the end of transmit or receive message processing.	Fatal
			NOTE **NXM is only checked for data buffers (TX and RX messages). It is not reported for UNIBUS timeouts which occur during a Base Table Access or when writing into locations 24 and 26.**	
			Performance Note Because NXM is only checked at the end of a buffer, every access to the NXM causes a 20 μsec pause in UNIBUS activity. This could affect performance of other system components, such as disks, tapes, and communication devices.	
1000	9	PROCEDURE ERROR	Indicates a procedure error on the part of the PDP-11 program where the requested input command cannot be honored because of a programming error. This error can be caused by the following:	Fatal

Table 3-5   Sel 6 Bit Functions Associated
with Control Out (Cont)

Error Code (Octal)	Bit	Name	Description	Error Class
			• specifying an invalid code in BSEL 0, bits 1 and 0 such as a code of 1 0 (2),	
			• trying to issue a CNTL I command before supplying a base address,	
			• trying to assign a base address a second time, or	
			• trying to issue a BA/CCI command before supplying a base address.	
			The PDP-11 program may create a procedure error by issuing a BASE I command a second time as a means of shutting down the DMC11 in an orderly manner. For remote operation, Data Terminal Ready (EIA Interface Circuit CD) will be cleared as a result of this error, ceasing transmit receive activity.	
			NOTE 1. On fatal errors, the DMC11 will exit from the DDCMP running state. The DMC11 must then be initialized via MASTER CLEAR, BASE I/CNTL I, and BA/CC sequences. 2. Non-fatal errors are reported by the DMC11 to inform the PDP-11 program of some error conditions. Once the error condition is removed, the DMC11 will proceed normally.	

The PDP-11 program may clear IEI at any time other than when awaiting RDI.

NOTE
1. When a MOV instruction is used to write to SEL 0, bit 15 (RUN bit) of SEL 0 must always be set. In this case a BIS instruction is recommended.

2. The PDP-11 program should not begin a new input transfer until the previous transfer has been completed. If the PDP-11 program wishes to begin a new transfer immediately, it should check that RDI has been cleared before setting RQI; this can be done by scanning RDI until it has been cleared.

3.4.3.1 Initialization Command – The initialization command is the first command issued by a user program at start up time to MASTER CLEAR the DMC11 and place it in the initialized state. The power up sequence and UNIBUS INIT signal also initializes the DMC11. In the initialized state, the DMC11 does not send or receive messages on the serial line but checks the incoming serial data for enter MOP message for remote load detection.

In the initialized state, only the BASE I command can be assigned to the DMC11 without causing a procedure error. A procedure error causes the DMC11 to write the PDP-11 physical memory location 0 to 400 $_8$ with the content of the DMC11 memory. This action could cause the PDP-11 operating system or program to fail because the PDP-11 low core has been modified. **Never** assign any command to the DMC11 other than a BASE I command after power up, system initialization, or DMC11 MASTER CLEAR.

Initialization of the DMC11 by the PDP-11 is done by setting the MASTER CLEAR bit in BSEL 1. The program should not access the CSRs for 2 microseconds following MASTER CLEAR. See Figure 3-3 for the programming procedure for initialization command. The recommended procedure is to write MCLR (bit 14) with a one (1) and then wait for RUN bit 15 to be set by the DMC11 to signal the end of initialization, for example:

```
        MOV 040000,SELO        ;SET MASTER CLEAR BIT
   A:   TST SELO               ;WAIT FOR RUN BIT TO BE SET
        BPL A                  ;
        .                      ;
        .                      ;PROCEED TO DO BASE IN
        .
```

NOTE
The MASTER CLEAR bit is self-clearing.

3.4.3.2 Base In Command – Figure 3-4 illustrates the format for the BASE I command which is the only command allowed after DMC11 initialization (Power Up, System Initialization, or MASTER CLEAR).

3-14

INITIALIZATION COMMAND

```
        ╭─────────────╮
        │    ENTER    │
        ╰─────────────╯
               │
               ▼
        ┌─────────────────┐
        │ SET MASTER      │
        │ CLEAR BIT VIA   │
        │ MOV/BIS #40000, │
        │ SEL 0           │
        └─────────────────┘
               │
               ▼◄──────────────┐
        ┌─────────────────┐    │
        │ WAIT FOR        │    │
        │ SETTING OF      │    │
        │ RUN BIT         │    │
        └─────────────────┘    │
               │               │
               ▼               │
            ╱╲                 │
          ╱    ╲               │
        ╱  RUN   ╲   YES        │
       ╱ BIT STILL ╲───────────┘
        ╲ CLEARED ╱
          ╲    ╱
            ╲╱
             │
             NO
             │
             ▼
```

<<INITIALIZATION EXIT:
DO BASE IN COMMAND
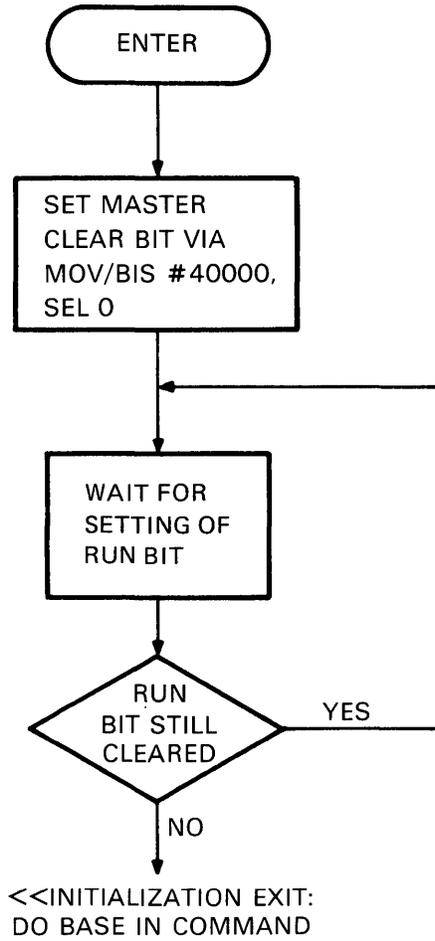
                                    MK-0779

Figure 3-3   Programming Procedure for Initialization Command

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
BSEL 1	RUN	MCLR	▨			MAINTENANCE			RDI	IEI	RQI 1	▨		IN RCV	INPUT COMMAND 1 1		BSEL 0 SEL 0
BSEL 3	▨								RDO	IEO	▨			OUT RCV	OUTPUT COMMAND		BSEL 2 SEL 2
	BASE ADDRESS																SEL 4
	BA17,16	▨	RE-SUME	▨													SEL 6
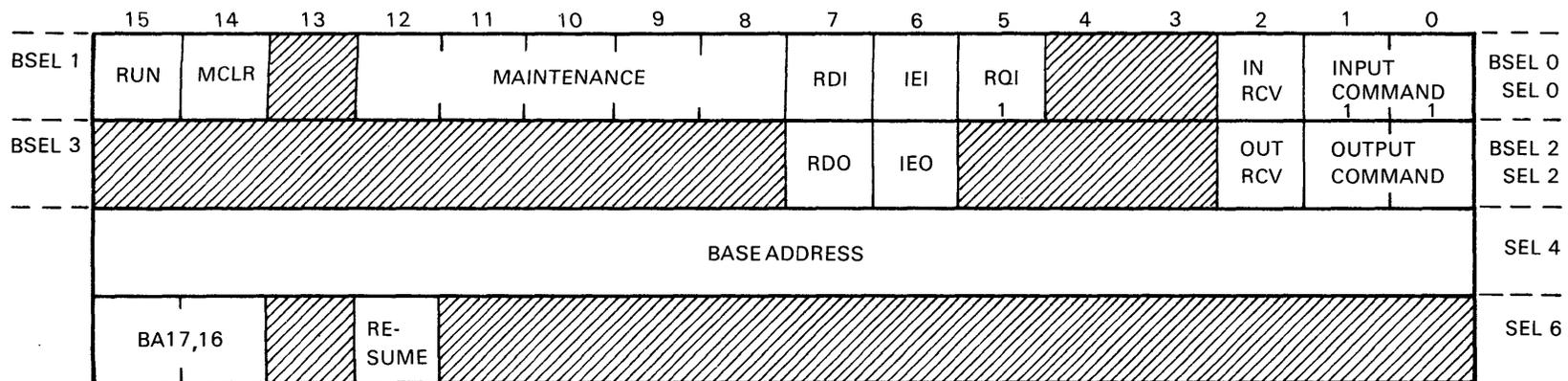
MK-0780

Figure 3-4   Base In Command Format

The user program:

- Sets up the BASE I command type (1 1) in SEL 0, bits 1 and 0, and sets bit 5 of SEL 0 for a request in RQI. Bit 6 of SEL 0, IEI, is set by the user program to permit the DMC11 to interrupt the main CPU when the data port (SEL 4 and 6) is available (RDI is set). This can be done using the MOVB or BISB instruction.

- Bit 7 (RDI) of SEL 0 is set by the DMC11 in response to the user program setting of RQI informing the user program that data can be transferred into SEL 4 and 6.

- After loading the base address into SEL 4 and 6, the user program clears RQI.

- After reading the base address from SEL 4 and 6, the DMC11 clears RDI.

(See Figure 3-5)

The command BASE I assigns a Base Table (128-word table in PDP-11 memory) to the DMC11. The Base Table then belongs to the DMC11 until it is MASTER CLEARed by INIT or MASTER CLEAR. The PDP-11 program may examine, but must not alter, the contents of the Base Table. The Base Table is described in Section 3.5.2.

Normally, the BASE I command is issued with the RESUME bit (bit 12 of SEL 6) cleared which conditions the DMC11 to enter the DDCMP start-up state of the DDCMP. With the BASE I command the RESUME bit set command causes the DMC11 to:

- Use the contents of the currently assigned Base Table as the initial state of the protocol.

- Copy the 200_8 bytes of the Base able in the PDP-11 memory, starting at the specified Base Table address, to DMC11 internal memory (RAM). The DMC11 internal memory is used to store protocol constants, variables, state variables, error counter, and transmit/receive buffers.

- Force the DMC11 to resume operation where it was last stopped by means of an orderly shutdown of the DMC11 (refer to Section 3.5.5, Shutdown of the DMC11). There will be no DDCMP start sequence in this case.

3.4.3.3 Control In Command – Upon completion of the BASE I command, the PDP-11 program must perform a CNTL I command to set the DMC11 in half-duplex mode, full-duplex mode, normal DDCMP, or maintenance (MOP) mode. Figure 3-6 illustrates the format for the CNTL I command and Figure 3-7 shows the programming procedure for CNTL I.

The user program:

- Sets up the CNTL I command type (0 1) in SEL0, bits 1 and 0, and sets bit 5 of SEL 0 for a request in (RQI). Bit 6 of SEL 0, (IEI), is set by the user program to permit the DMC11 to interrupt the PDP-11 when the data port is available (RDI is set). These bits can be set using a BISB or MOVB instruction.

- When the data port (SEL 4 and 6) is available, bit 7 of SEL 0 (RDI) is set by the DMC11 in response to the setting of RQI by the user program.

- Following the receipt of RDI, the PDP-11 program loads the control information into SEL 4 and 6.

- After the half-duplex/full-duplex mode bit 10 of SEL 6 and/or the DDCMP maintenance bit 8 of SEL 6 is/are set up, the user program clears RQI.

- After reading the control information from SEL 4 and 6, the DMC11 clears RDI.

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BASE IN COMMAND
FROM:
INITIALIZATION
EXIT

SET UP COMMAND
TYPE AND RQI
IN SELB 0 VIA
MOVB/BISB
#43, SELB 0

NOTE: IF INTERRUPT DRIVEN INPUT
SERVICING IS DESIRED,
INTERRUPT ENABLE INPUT
(IEI) COULD BE SET, IN WHICH CASE,
THE INSTRUCTION COULD BE
MOVB/BISB #143 SELB 0

WAIT FOR
SETTING OF
RDI

RDI
STILL
CLEARED   YES

NOTE: IF INTERRUPT DRIVEN INPUT SERVICING
HAS BEEN SELECTED EARLIER,
THE SETTING OF THE RDI
BIT, BY THE DMC11, IS ACCOM-
PANIED BY INTERRUPTING TO
VECTOR, XX0.

NO

LOAD 18 BITS BASE
ADDRESS WITH
RESUME BIT CLEARED
TO SEL AND SEL 6

CLEAR RQI BIT
IN SELB 0 VIA
BICB #40,
SELB 0

SET OUTPUT
INTERRUPT
ENABLE BIT
IN BSEL 2

NOTE: FOR INPUT
COMMANDS, NON-INTERRUPT
MODE IS ILLUSTRATED,
FOR OUTPUT COMMANDS,
INTERRUPT MODE IS
ILLUSTRATED.

<<BASE IN EXIT:
TO DO CONTROL IN

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Figure 3-5   Programming Procedure for Base In Command

3-18

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
BSEL 1	RUN	MCLR			MAINTENANCE				RDI	IEI	RQI 1			IN RCV	INPUT COMMAND 0	1	BSEL 0 SEL 0
BSEL 3									RDO	IEO				OUT RCV	OUTPUT COMMAND		BSEL 2 SEL 2
																	SEL 4
						DDCMP HD		DDCMP MAINT									SEL 6
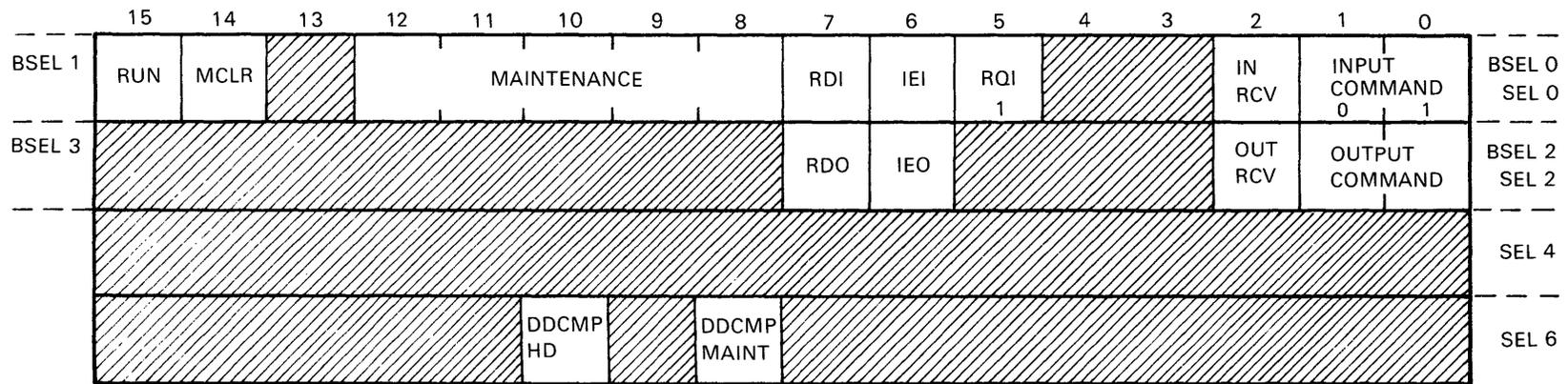
MK-0782

Figure 3-6   Control In Command Format
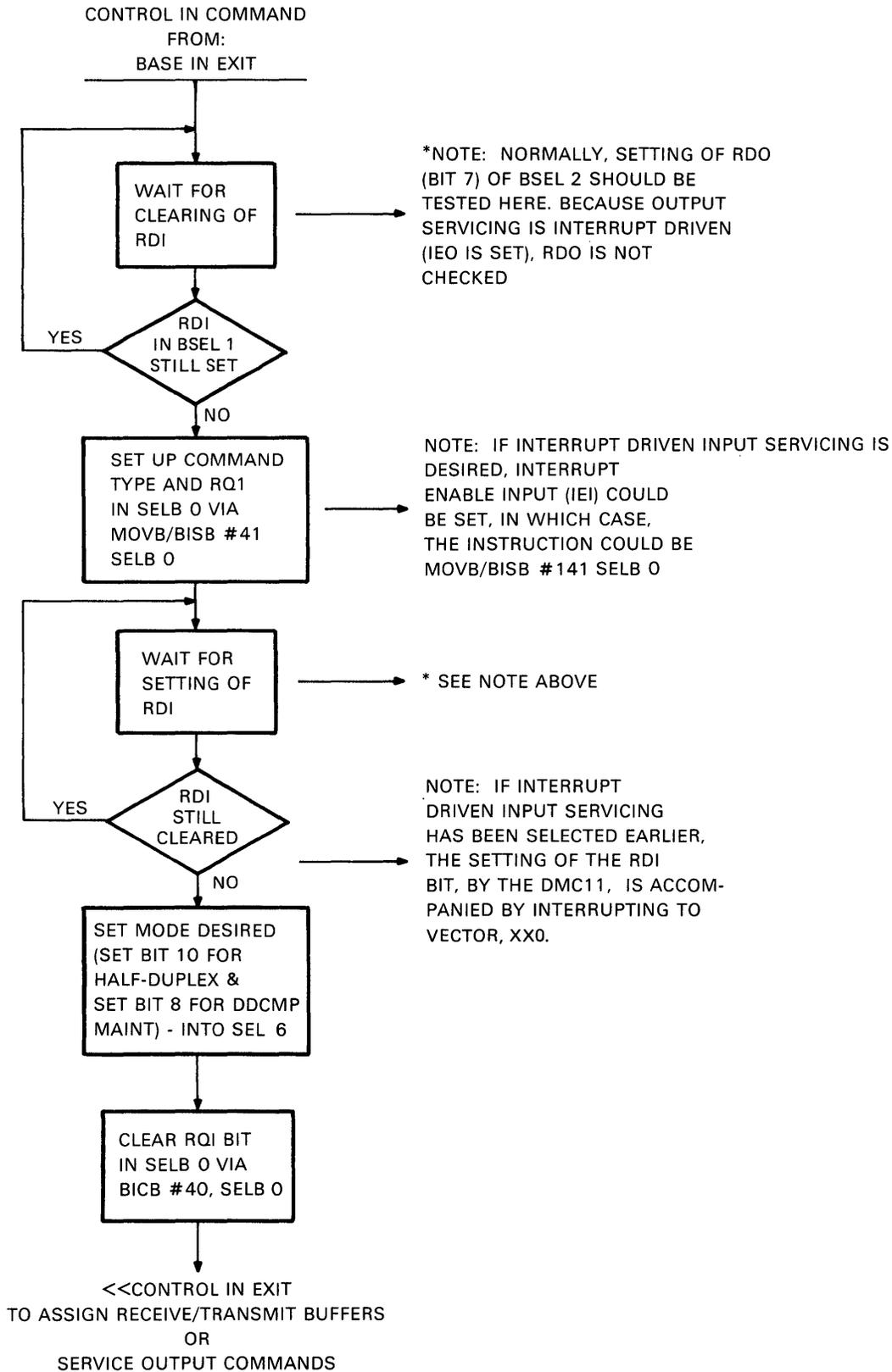
Figure 3-7 Programming Procedure for Control In Command

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3.4.3.4 Buffer Address/Character Count In Command – The command format is presented in Figure 3-8. This command provides the user program with the mechanism for assigning transmit and receive buffers (see Figure 3-9).

<div align="center">

CAUTION

In order to assign a transmit or receive buffer to the DMC11, it is imperative that successful BASE I and CNTL I commands have been previously issued to the DMC11. Otherwise, a procedure error will occur which will write into the PDP-11 low memory area and subsequently crash the operating system software.

</div>

The user program:

- Sets up the command type (0 0) in bits 1 and 0 of SEL 0.

- Bit 2 of SEL 0 is cleared for transmit buffer address and set for receive buffer address. Bit 6 of SEL 0, IEI, is set by the user program to permit the DMC11 to interrupt the main CPU when the data port is available. These bits can be set using the MOVB or BISB instruction.

- Bit 5 of SEL 0 is set for RQI.

- When the data port is available, bit 7 of SEL 0, RDI, is set by the DMC11 to inform the user program that data can be loaded into SEL 4 and 6.

- In response to RDI, the PDP-11 program loads SEL 4 with the low-order 16 bits of the buffer address, bits 15 and 14 of SEL 6 with the high-order bits of the address, and bits 13 through 0 of SEL 6 with the 14-bit character count.

- After the user program has cleared RQI, the DMC11 reads SEL 4 and 6, then clears RDI.

For data transmission, the PDP-11 program may queue up to seven buffers by supplying buffers to the DMC11 at a faster rate than the DMC11 returns them. The PDP-11 program must not assign more than seven transmit buffers to the DMC11 at any given time. Otherwise, data integrity may be lost.

Buffers from 1 to 16,383 bytes long may be used, but the buffer size should be limited to a practical maximum size which is dependent on the error rate of the communications facility. Each buffer corresponds to a single DDCMP data message. With high speed (1M bps) DMC11s, maximum message size is limited by CPU type and UNIBUS activity because of the need for prolonged periods of frequent memory access.

For data reception, the PDP-11 may queue up to seven empty buffers by supplying them to the DMC11 at a faster rate than the DMC11 returns them. The PDP-11 program must not try to assign additional receive buffers if seven are already outstanding, or data integrity may be lost. The character count for the receive buffer must be large enough to accommodate the longest message expected. The PDP-11 should ensure that a receive buffer is always assigned.

<div align="center">

CAUTION

A receive buffer starting at an odd address boundary should not be assigned to the DMC11. Doing this may create a race condition in the DMC11 and cause the system (UNIBUS) to hang. This is a catastrophic system failure requiring system initialization.

</div>

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
BSEL 1	RUN	MCLR	/////			MAINTENANCE			RDI	IEI	RQI	/////////////		IN RCV	INPUT COMMAND 0 0		BSEI 0 / SEL 0
BSEL 3	//////////////////////////////////								RDO	IEO	///////////////			OUT RCV	OUTPUT COMMAND		BSEL 2 / SEL 2
	TRANSMIT/RECEIVE BUFFER ADDRESS																SEL 4
	BA17,16		CHARACTER COUNT														SEL 6
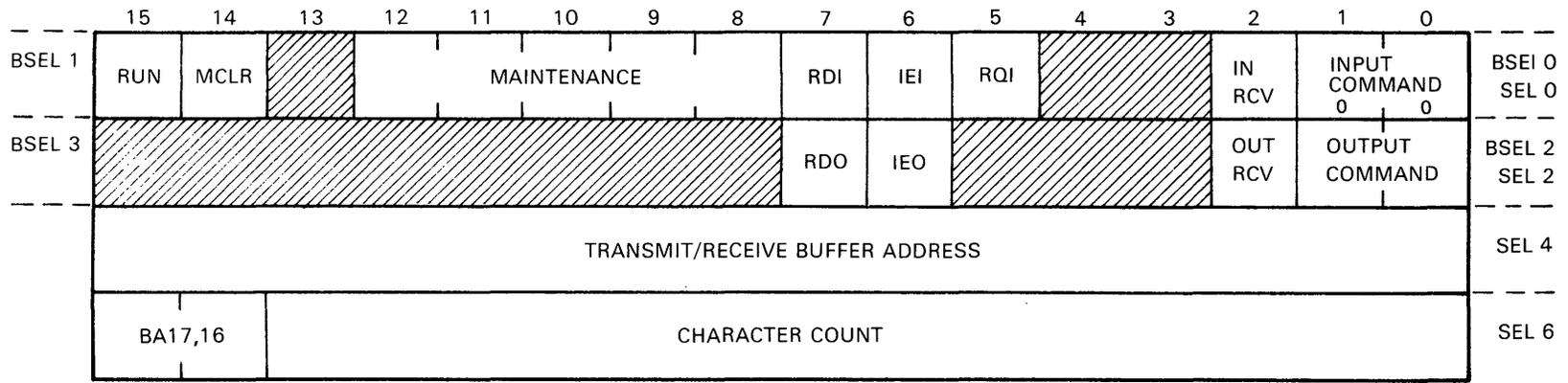
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Figure 3-8   Buffer Address/Character Count In Command Format
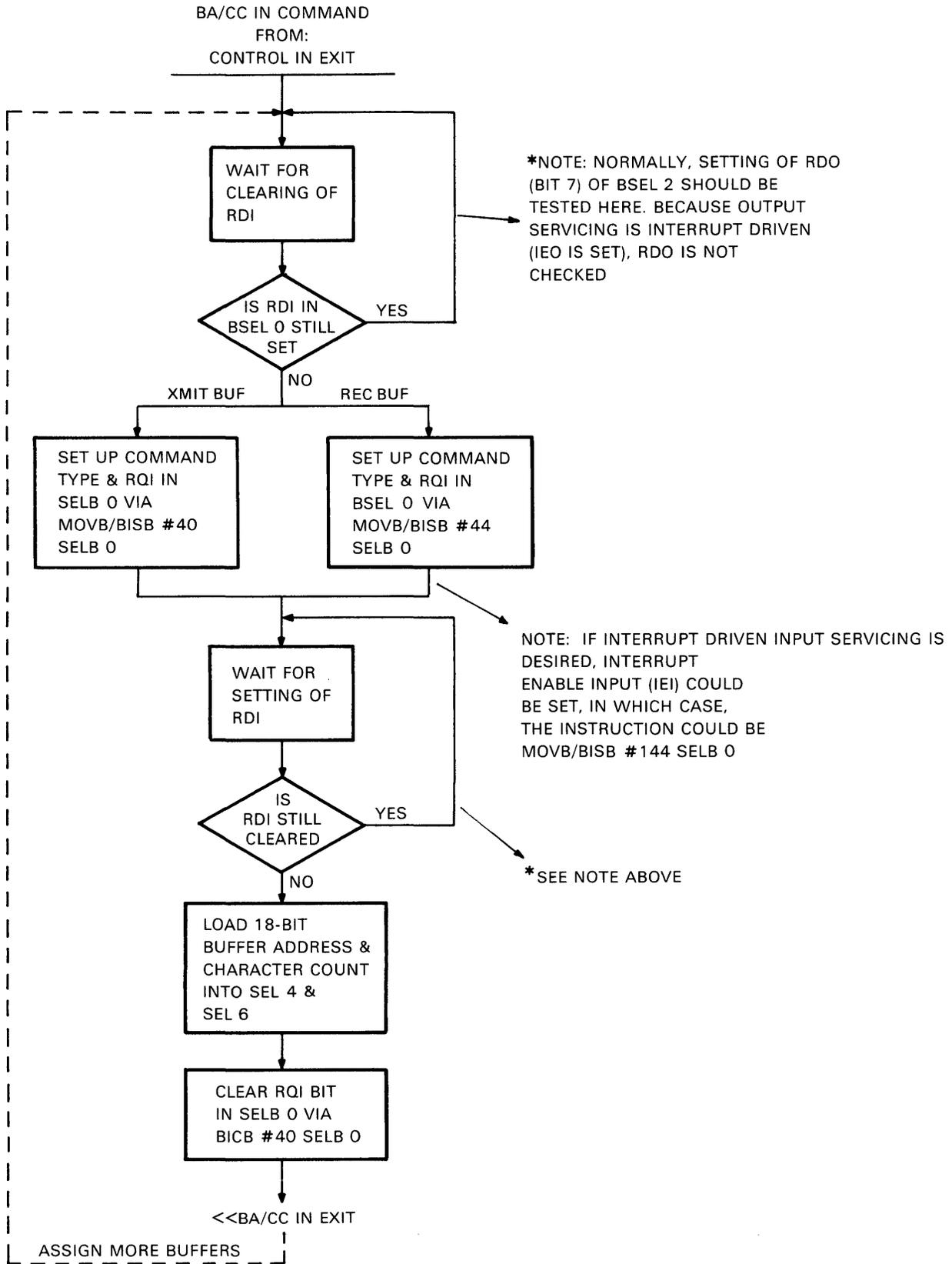
Figure 3-9 Programming Procedure for BA/CCI Command

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3.4.4 Output Command (Format and Field Descriptions)
The DMC11 communicates with the CPU by the following two categories of information.

1. Buffer Address/Character Count Out (BA/CCO) – Information pertinent to the normal completion of data transfers.

2. Control Out (CNTL O) – Information concerning detection of an error condition.

NOTE
The programming procedure flowchart (see Figure 3-10) illustrates the interrupt mode for output command servicing. The intent is to demonstrate a way of programming, but should not be interpreted as the only way.

3.4.4.1 Buffer Address/Character Count Out (BA/CCO) Command – This command is used to post the normal completion of data transfer operations to the user program. The command format is presented in Figure 3-11. BA/CCO occurs upon successful completion of a transmit or receive buffer.

RX (Bit 2=1)   The message has been received with no errors and transferred to the buffer in main memory. An ACK response is sent to the sending station.

TX (Bit 2=0)   An ACK response has been received for the transmitted message, indicating error-free reception at the receiving station.

The DMC11 issues output commands in two steps. First, the data pertinent to the command being issued is stored in SEL 4 and 6. Once this data storage is complete, the DMC11 sets the RDO bit and command identity bits in BSEL 2 and generates an interrupt through vector XX4 if the IEO bit is set. If the command issued is a Buffer Address Out (BAO), the IN RCV (bit 2) is set to 1 to indicate that the completion posted involves a receive data operation, or cleared to designate a completion posting for a transmit data operation. Generally, processing an output command involves the following steps:

*   The user program checks for RDO set. This can be done through periodic checking or by waiting for an interrupt, assuming that interrupts are enabled.

*   When RDO is detected as set, the user program checks BSEL 2, bits 0, 1, and 2, to determine the type of completion (receive or transmit, fatal or non-fatal error), then reads SEL 4 and 6, and processes as necessary.

*   Upon reading the data port (SEL 4 and 6), the user program clears RDO to inform the DMC11 of port availability. (See NOTE in Section L of Appendix I.)

3.4.4.2 Control Out (CNTL O) Command – The DMC11 informs the PDP-11 program of unusual or error conditions involving the communications channel, remote end of the link, DMC11 hardware, or PDP-11 program by means of a CNTL O command. Some errors are advisory in nature and normal operation may continue. Others are fatal and require the PDP-11 program to initialize the DMC11. Figure 3-12 illustrates the format for this command.

The DMC11 issues a CNTL O command in two steps. First, the data error code is loaded into SEL 6. Then, the DMC11 sets the RDO bit in SEL 2. If the IEO bit is set, an interrupt is generated to vector XX4. The error code is listed and explained in Table 3-5. To process the CNTL O command, follow the steps given in Section 3.4.4.1.

OUTPUT COMMANDS SERVICING
PROCEDURE*

* NOTE:
    IN THIS PROCEDURE, THIS
    ROUTINE IS ENTERED VIA
    AN INTERRUPT TO VECTOR XX4.

```
                    ┌─────────────┐
           YES      │  IS         │
      ┌─────────────│  RDO IN     │
      │             │  BSEL 2     │
      │             │  CLEARED    │
      │             └─────────────┘
      │                   │ NO
      │                   ▼
      │             ┌──────────────┐              ┌──────────────┐
      │             │  IS IT       │   YES        │  CONTROL     │   YES
      │             │  CONTROL OUT,│──────────────│  OUT WITH    │────────┐
      │             │  BSEL 2 BITS │              │  FATAL       │        │
      │             │  1, 0 = 0, 1 │              │  ERROR       │        │
      │             └──────────────┘              └──────────────┘        │
      │                   │ NO                          │ NO             │
      │                   ▼                             ▼                │
      │             ┌──────────────┐  ┌──────────────┐                   │
      │             │  IS IT       │  │ RECEIVE BA/CCO│                   │
      │             │  A RECEIVE   │YES│ HANDLE THE   │                   │
      │             │  BA/CCO, BSEL 2│─│ SUCCESSFULLY │                   │
      │             │  BIT 2 = 1   │  │ RECEIVED BUF │                   │
      │             └──────────────┘  └──────────────┘                   │
      │                   │ NO              │                            │
      │                   ▼                 │      ┌──────────────┐      │
      │             ┌──────────────┐        │      │ TAKE APPROPRIATE│   │
      │             │ TRANSMIT BA/CCO│      │      │ ACTION TO    │◄─────┘
      │             │ HANDLE THE   │        │      │ CORRECT ERROR│
      │             │ SUCCESSFULLY │        │      │ CONDITIONS   │
      │             │ TRANSMITTED  │        │      └──────────────┘
      │             │ BUFFER       │        │            │
      │             └──────────────┘        │            │
      │                   │◄────────────────┘            │
      │                   ▼                              │
      │             ┌──────────────┐                     │
      │             │ CLEAR RDO    │                     │
      │             │ IN BSEL 2    │                     │
      │             └──────────────┘                     │
      └───────────────────┤                              │
                          ▼                              │
                    << RETURN                            │
                                           ┌──────────────┐
                                           │ LOG ERROR    │
                                           │ AS FATAL     │
                                           └──────────────┘
                                                 │
                                                 ▼
                                    ┌───────────────────────┐
                                    │ ON FATAL ERROR, DMC11 │
                                    │ EXITS FROM THE DDCMP  │
                                    │ RUNNING STATE, THE    │
                                    │ DMC11 MUST BE REINITIALIZED│
                                    │ VIA MASTER CLEAR FOLLOWING│
                                    │ ITS OCCURENCE         │
                                    └───────────────────────┘
```

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Figure 3-10   Programming for Output Commands Servicing Procedure

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
BSEL 1	RUN	MCLR				MAINTENANCE			RDI	IEI	RQI			IN RCV	INPUT COMMAND		BSEL 0 SEL 0
BSEL 3									RDO	IEO				OUT RCV	OUTPUT COMMAND 0 0		BSEL 2 SEL 2
	TRANSMIT/RECEIVE BUFFER ADDRESS																SEL 4
	BA17,16			CHARACTER COUNT													SEL 6
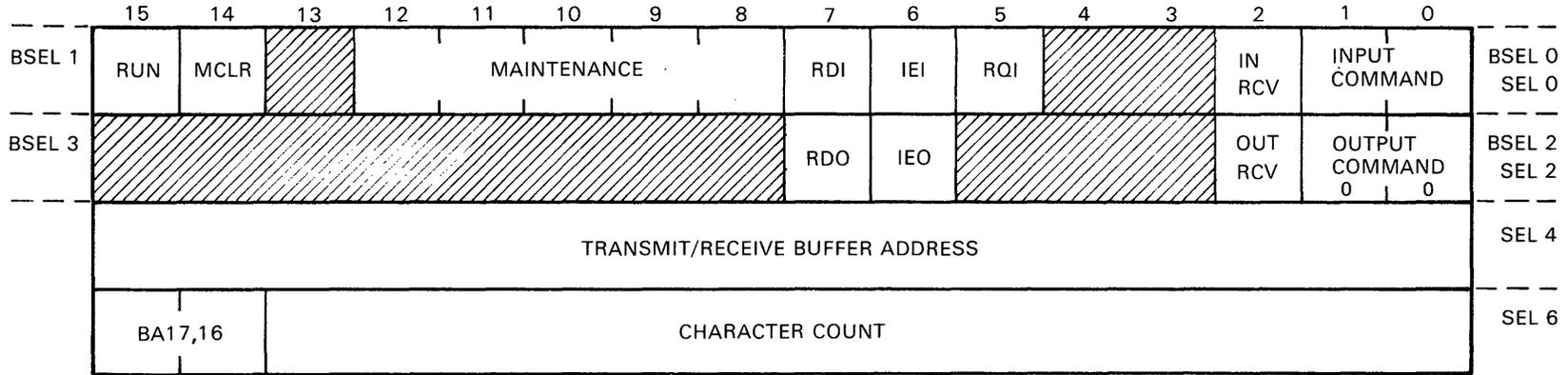
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Figure 3-11   Buffer Address/Character Count Out Command Format

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
BSEL 1	RUN	MCLR				MAINTENANCE			RDI	IEI	RQI			IN RCV	INPUT COMMAND		BSEL 0 SEL 0
BSEL 3									RDO	IEO				OUT RCV	OUTPUT COMMAND 0 1		BSEL 2 SEL 2
																	SEL 4
							PROC ERR	NON EX MEM	DDCMP START RECD	DIS-CONN		LOST DATA	DDCMP MAINT RECD	NO BUF	TIME OUT	DATA CK	SEL 6
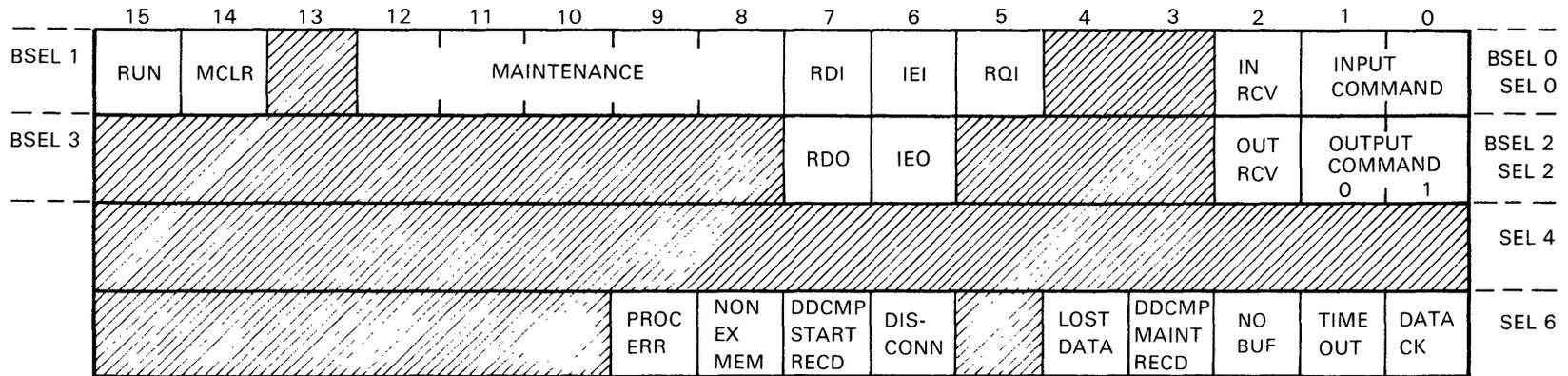
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Figure 3-12   Control Out (CNTL O) Command Format

3.5 PROGRAMMING HINTS

3.5.1 DMC11 Start-Up
Start-up is the process of initializing the protocol states and variables, and synchronizing both stations on a link. The DDCMP start-up sequence is initiated once the DMC11 is assigned a BASE I command with the RESUME bit cleared. The PDP-11 program is not informed of the completion or failure to complete the start-up sequence. The PDP-11 must wait for the buffer return from the DMC11 after a successful transmission or reception of a data message. It is recommended that a BASE I command with the RESUME bit cleared be issued to the DMC11 and be followed by a CNTL I command to set the DMC11 in either full-duplex or half-duplex mode, normal DDCMP, or maintenance mode.

3.5.2 DMC11 MASTER CLEAR
DMC11 master clear can be performed by either system initialization, power fail, or setting bit 14 of SEL 0. When master clearing the DMC11 by the software, consideration must be given to current activity within the DMC11 microprocessor and its line unit.

In DDCMP mode (normal operation), an RDO for a receive buffer completion is given to the PDP-11 as soon as the BCC for the received message is verified. Following PDP-11 notification, the ACK for the message is placed in the transmit silo for response to the station that sent the message. If software initializes the DMC based on receipt of the RDO, it is likely that the ACK will not be sent; the ACK message may not have been shifted onto the serial line before the clear signal initialized the line unit.

Similarly, in DDCMP maintenance mode an RDO for transmit completion is indicated to the PDP-11 as soon as the last data character of the message is placed in the transmit silo. Again, software initialization immediately following the RDO clears the line unit and aborts the message.

In both of the above cases there is a worst case delay which must be timed by software, prior to initialization. The delay consists of the time required to transmit possibly 64 characters in the silo, two characters of CRC and one character in the shift register, at the serial line rate (a total of 67 characters or 536 bits).

A timer should be programmed as part of the initialization routine. This code would only be executed when the DMC11 is to be initialized after one of the following:

- RDO for BA/CCO signaling RECEIVE DONE for DDCMP message, or

- RDO for BA/CCO signaling TRANSMIT DONE in DDCMP maintenance mode.

To calculate the delay required, the following formula should be used:

$$T = \frac{536}{X} + Y$$

where:

    T   = the time delay in seconds.
    X   = the serial line speed in bits per second.
    536 = the total number of bits that should be considered as being in transit.
    Y   = the clear to send (CTS) delay time in seconds.

Examples

1. For link with M8202-YA line units (1M bps):

$$T = \frac{536}{1,000,000} + 0.0001$$

T = .000636 sec. or 636 microseconds.

2. For a link using M8201 and 2400 bps modem, with a 150 ms. CTS delay.

$$T = \frac{536}{2,400} + 0.15$$

T = .373 sec. or 373 milliseconds.

When the DMC11 is cleared during operation, even with worst case timing, there is no guarantee that data in the silo reaches its destination, that is, an ACK which is given the time to be transmitted, but gets garbled on the line, is not recognized at the destination. Clearing the DMC11 that sent the ACK may cause the other end to time out (looking for a valid response). Failure to provide enough delay time before MASTER CLEARing the DMC11 results in a protocol hang condition in normal DDCMP mode and the loss of the MOP message in DDCMP maintenance mode.

3.5.3 Error Reporting
On start up, the DMC11 is assigned a BASE I command which allocates to the DMC11 a 400_8 byte long Base Table from the PDP-11 memory. The DMC11 uses part of this Base Table for keeping a copy of error counters, transmit and receive buffer queues, and protocol constants and variables. The DMC11 Base Table is shown in Figure 3-13.

3.5.3.1 Cumulative Error Counters – The DMC11 keeps six cumulative error counters. Upon occurrence of any fatal errors, the DMC11 updates the Base Table. Approximately every second an attempt may be made to update the error counters. This attempt is only successful if the microcode is in its idle loop. Cumulative error counters are listed in Table 3-6.

3.5.3.2 Threshold Counters – The DMC11 has two threshold counters which notify the PDP-11 program of a persistent error condition. Threshold counters operate by counting consecutive errors of a given class and trigger a notification to the user when the threshold value of eight has been reached. The threshold counters are identified as NAKS Transmitted and REPS Transmitted.

When the NAKS Transmitted threshold counter reaches a count of eight, a CNTL O command is generated by the DMC11 with an error code of 1 (DATA CHECK ERROR) or an error code of 4 (NO BUF) in BSEL 6. When the REPS Transmitted threshold counter reaches a count of eight, a CNTL O command is generated with an error code of 2 (TIME OUT ERROR) in BSEL 6. These errors are not fatal. Once the error condition is removed, the DMC11 proceeds normally.

3.5.4 Power Fail Recovery
The DMC11 stores the protocol information internally in RAM memory. DMC11 power fail recovery may not be successful because the contents of the DMC11 memory will have been lost after power failure. Therefore, the software should be designed to reinitialize the DMC11 using software-maintained information about transmit and receive messages pending.

Table 3-6 Cumulative Error Counters

PDP-11 Base Address	Trans/Rec	Error
Base + 5	NAKS Received	All { No Buffer Available, Bad Header BCC, Bad Data BCC
Base + 6	NAKS Sent	No Buffer Available
Base + 7	NAKS Sent	Bad Header BCC
Base + 10	NAKS Sent	Bad Data BCC
Base + 11	REPS Sent	
Base + 12	REPS Received	

3.5.5 Shutdown of the DMC11

The PDP-11 program may shut down the DMC11 by creating a procedure error, that is, issue a BASE I command a second time. After successfully assigning this second BASE I command (which forces a procedure error), the DMC11 terminates protocol, returns all successfully received data messages, and all acknowledged transmitted data messages, posts all CNTL O currently queued, and finally posts a CNTL O command with an error code of 1000_8 (Proc Err) in SEL 6. The software should handle all these buffer returns and CNTL O commands from the DMC11 until the CNTL O with the error code of 1000_8 is processed.

NOTE

When shutting down the DMC11, it is the responsibility of the PDP-11 program to ensure that there is no outstanding transmit buffer at either end of the link. Otherwise, a situation could occur where one station shuts down after receiving the good message and sending out an ACK. This ACK could be lost and the remote station will not complete the transaction. This is an increasing problem on dial half-duplex links where the line goes on hook before the transmission is completed.

When a procedure error is forced, the DMC11 updates the Base Table in the PDP-11 memory via DMA transfers. If there is a hardware problem in memory or the Base Table assigned to the DMC11 is located in nonexistent memory, the DMC11 will not detect this condition.

There are some illegal ways of generating procedure errors on the DMC11, such as issuing the following commands to the DMC11 before it is assigned a Base Table via a BASE I command.

- A CNTL I command

- A transmit or receive BA/CCI command

- An invalid code of (1 0) in BSEL 0, bits 1 and 0 in an input command

BASE TABLE ADDRESS (PDP-11 BASE ADDRESS +)	INTERNAL DMC-11 MEMORY	MICROPROCESSOR MAIN MEMORY ASSIGNMENTS	
	000000	NAKSR=0	;NAKS RECD--DYNAMIC
	000001	NAKST=NAKSR+1	;NAKS TMTED--DY&NAMIC
	000002	REPSR=NAKST+1	;REPS RECD--DYNAMIC
	000003	REPST=REPSR+1	;REPS TMTED--DYNAMIC
BASE + 0	000004		
BASE + 1	000005		
BASE + 2	000006	NP=REPST+3	;CONSTANT 0
BASE + 3	000007	NTLR=NP+1	;NAKS-MSG NO BUFFERS CUMUL.
BASE + 4	000010	NHDR=NTLR+1	;NAKS-MSG HEADER BAD
BASE + 5	000011	NDATR=NHDR+1	;NAKS-DATA BAD
BASE + 6	000012	NTLS=NDATR+1	;NAK SENT--NO BUFFERS
BASE + 7	000013	NHDS=NTLS+1	;NAK SENT BAD HEADER
BASE + 10	000014	NDATS=NHDS+1	;NAK SENT BAD DATA
BASE + 11	000015	REPCS=NDATS+1	;REPS SENT CUMUL
BASE + 12	000016	REPCR=REPCS+1	;REPS RECD CUMUL
BASE + 13	000017	BASE=REPCR+1	;CORE TABLE BASE ADDRESS
BASE + 16	000022	SRC=BASE+3	;START OF INPUT CHAIN--NEXT RECV DONE
BASE + 17	000023	ERC=SRC+1	;END OF INPUT CHAIN
BASE + 20	000024	RCL1=ERC+1	;RECEIVE LINK #1
BASE + 25	000031	RCL2=RCL1+5	; " " #2
BASE + 34	000036	RCL3=RCL2+5	; " " #3
BASE + 37	000043	* RCL4=RCL3+5	
BASE + 44	000050	RCL5=RCL4+5	
BASE + 51	000055	RCL6=RCL5+5	
BASE + 56	000062	RCL7=RCL6+5	
BASE + 63	000067	STC=RCL7+5	;START OF OUTPUT CHAIN---NEXT TMT DONE
BASE + 64	000070	ETC=STC+1	;END OF TRANSMIT CHAIN
BASE + 65	000071	TML1=ETC+1	;TRANSMIT LINK #1
BASE + 73	000077	TML2=TML1+6	; " " #2
BASE + 101	000105	TML3=TML2+6	; " " #3
BASE + 107	000113	** TML4=TML+6	
BASE + 115	000121	TML5=TML4+6	
BASE + 123	000127	TML6=TML5+6	
BASE + 131	000135	TML7=TML6+6	
BASE + 137	000143	TML8=TML7+6	
BASE + 145	000151	T=TML8+6	;TYPE FIELD
BASE + 146	000152	ST+T+1	;SUBTYPE FIELD
BASE + 147	000153	ISP17=ST+1	;MSG ACKED IMAGE
BASE + 150	000154	IMG10=ISP17+1	;IMAGE OF BIT 1 OF SP10
BASE + 151	000155	IMG11=IMG10+1	;IMAGE OF SP11
BASE + 152	000156	IMG12=IMG11+1	;IMAGE OF SP12
BASE + 153	000157	IMG14=IMG12+1	;IMAGE OF SP14
BASE + 154	000160	IMG16=IMG14+1	;IMAGE OF SP16
BASE + 155	000161	IMG17=IMG16+1	;IMAGE OF SP17
BASE + 156	000162	TYPTAB=IMG17+1	;TYPE TABLE--- ;72 TYPE TABLE REP ;73 " " NAK

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Figure 3-13 DMC11 Base Table

(Sheet 1 of 2)

```
BASE + 160        000164        TYPSTT=TYPTAB+2        ;74 TYPE TABLE START
                                                      ;75  "   "   STACK
                                                      ;
                                                      ;
BASE + 163        000167        BC=TYPSTT+3           ;RECEIVE BYTE COUNT
BASE + 165        000171        ISP11=BC+2            ;SP11 IMAGE
BASE + 166        000172        ISP12=ISP11+1         ;SP12 IMAGE
BASE + 167        000173        INCONS=ISP12+1        ;IN CONTROL CSR IMAGE
BASE + 170        000174        RTHRS=INCONS+1        ;RECV THRESHOLD LINK
```

;ALL LOCATIONS FROM 200 ON ARE NOT WRITTEN OUT DURING A TABLE UPDATE

```
                  000210        TABST=210             ;TABLE UPDATE STATE
                  000211        PRTST=TABST+1         ;PORT STATE
                  000240        NXTINT=240            ;NEXT INTERRUPT POSITION
                  000241        NXTSP=NXTINT+1        ;END OF INTERRUPT CHAIN
                  000242        INTSTK=NXTSP+1        ;STACK OF INTERRUPTS
                  000400        MMEND=400             ;MAIN MEMORY END
```

*	LOCATION	DESCRIPTION
	1 BIT 0	BUFFER ASSIGNED FLAG
	2	ADDRESS LOW BYTE
RCL #	3	ADDRESS HIGH BYTE
	4	EXTENDED MEMORY BIT & CHARACTER COUNT HIGH BYTE
	5	CHARACTER COUNT LOW BYTE

**	LOCATION	DESCRIPTION
	1 BIT 0	BUFFER ASSIGNED FLAG
	BIT 1	TRANSMITTED FLAG
	2	MESSAGE NUMBER
TML #	3	ADDRESS LOW BYTE
	4	ADDRESS HIGH BYTE
	5	EXTENDED MEMORY & CHARACTER COUNT HIGH BYTE
	6	CHARACTER COUNT LOW BYTE

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Figure 3-13 DMC11 Base Table
(Sheet 2 of 2)

CAUTION
These illegal procedure errors force the DMC11 to update 200₈ bytes of its memory to the PDP-11 memory starting at physical location 0. This action corrupts the PDP-11 low core area and causes serious software failure.

NOTE
After a power failure, the operating software must immediately MASTER CLEAR the DMC11 and assign a BASE I command and CNTL I command before attempting to use the DMC11. Otherwise, an ILLEGAL PROCEDURE ERROR is created and the operating system fails.

3.5.6 Modem Control

For a DMC11-AR microprocessor, Data Terminal Ready (DTR) is asserted continously after a DMC11 MASTER CLEAR. DTR is dropped as a result of any fatal error or procedure error. The recommended procedure for disconnecting the link is to assign a second BASE I command and allow a minimum of 150 ms before issuing the Initialization command. When the DMC11 has entered the DDCMP running mode (start-up sequence completed), an ON-to-OFF transition of DATA SET READY causes the DMC11 to generate a CNTL O command with an error code of 100₈ (DIS-CONNECT ERROR). Note that the DMC11-AR, after assignment of a base address, attempts to send a start message. This causes the M8201 Line Unit to assert REQUEST TO SEND (RTS) and wait for CLEAR TO SEND and MODEM READY signals from the modems. Problems may result with some modems and their ability to work with an Automatic Calling Unit (ACU) of the BELL 801 type or equivalent.

The sequence of events are:

- ACU makes the call

- Receiving modem answers

- Receiving modem puts out a carrier and answer tone simultaneously.

Because the request to send from the DMC11 is on, ACU then interprets these events as a line busy condition and terminates the call. For DMC11-AR programming procedures in Auto-Dial/Auto Answer Applications, see Appendix J.

NOTE

1. The DMC11-AR does not monitor a carrier detect signal.

2. The DMC11-AR drops REQUEST TO SEND for about 1-bit time at the end of the last abutted data message before sending a trailing ACK. The 1-bit drop of RTS causes some delay by the modem in returning CLEAR TO SEND. The delay could be as long as a regular RTS - CTS delay of the modem (typically about 150 ms). To prevent extra delay for every data message, multiple buffers can be assigned to the DMC11 as opposed to single buffering. Some modems may react strangely to the 1-bit RTS drop and lost bit synchronization. It is recommended that users ask the manufacturer about a proposed modem concerning this occurrence. Modems adversely affected by the 1-bit RTS drop time should be avoided.

3.5.7 Maintenance Mode

DDCMP maintenance messages are used for down-line program loading, maintenance and control of satellite computer systems. These functions are controlled and performed by higher level software.

The DMC11 provides data link control for Maintenance Operation Protocol (MOP) which requires error-free transmission and reception on a data link. In DDCMP maintenance mode, the DMC11 provides modem control, message framing, bit error detection (CRC Checking), and CRC generation.

Messages in DDCMP message format are subject to error checking, but are unsequenced, unacknowledged, and not retransmitted automatically by the DMC11. Maintenance messages can only be sent and received while the microprocessor is in the DDCMP maintenance state. The PDP-11 program may cause the microprocessor to enter this state by a CNTL I transfer with bit 8 (DDCMP MAINT), and bit 10 (DDCMP HD) of SEL 6 set.

If a maintenance message is received while in the running (DDCMP) state, the microprocessor performs a CNTL O transfer with DDCMP MAINT RECD set in SEL 6. The PDP-11 program must then initialize the device to the maintenance state to transfer messages in maintenance format. The message causing the error notification is lost.

NOTE

Once the DMC11 is given a BASE I command, it sends a start message every second. When the PDP-11 program sets the DMC11 in DDCMP maintenance mode, the start is aborted. A "hang" condition could be created on a two-wire half-duplex link between the DMC11 and a non-DMC11 device as shown in the following example.

Example

The restart steps of a satellite computer system sequence are:

1. The Non-DMC11 system sends a MOP message.

2. The DMC system receives MAINT RECV'D. (For a maintenance message other than EN-TER MOP, see Section 3.5.8 for a description of the ENTER MOP message.)

3. The DMC system initializes the DMC and does BASE I.

4. DMC sends STRT.

5. The DMC system does CNTL I to set MAINT mode.

6. DMC aborts STRT.

7. The Non-DMC11 system sees aborted STRT or STRT with a noise HIT.

8. The DMC system gives maintenance message to the DMC.

9. DMC transmits the maintenance message and the non-DMC11 system resends MOP message simultaneously.

A hang-up occurs because both ends transmit simultaneously on a two-wire HDX link. The problem can be corrected in a number of ways.

1. Non-DMC11 system does not retransmit MOP request on bad response but instead waits for a time-out period.

2. DMC system should do a receive buffer BA/CCI command immediately following CNTL I at step 5 above and wait for the non-DMC11 system to time-out and retransmit.

3. DMC and Non-DMC11 systems should transmit at different time-out intervals.

Once in DDCMP maintenance mode, maintenance messages can be sent and received like data messages. On transmission, the data portion of the message is taken from the assigned buffer with the DMC11 generating the header and CRCs. On reception, only the data portion is placed in the available assigned buffer. Messages not in DDCMP maintenance format, having incorrect CRCs or no receive buffer are simply discarded. No errors are reported when in this mode. In the maintenance mode, the DMC11 transmitter does not wait for the SELECT flag. Line turnaround must be controlled by higher level software, that is, does not transmit until receipt of receive BA/CCO.

The data portion of the maintenance message may contain any data that is desired, but ordinarily it conforms to the DIGITAL MOP formats. When operating in conformance with MOP, the DMC11 must be operated in a single buffered manner, causing a line turn-around after each message is transmitted. When a host computer wishes to restart a satellite computer system, it must send the appropriate MOP messages as described in Section 3.5.8.

In order to exit maintenance mode, the PDP-11 program must initialize the DMC11 and supply a base address with the RESUME bit clear.

3.5.8 Remote Load Detect

Whenever the microprocessor is running, it is constantly scanning the serial line for a DDCMP maintenance message containing an ENTER MOP MODE data field as illustrated in Figure 3-14. What happens when this particular message is received depends on the setting of two switch packs on the DMC11 line unit (M8201 or M8202).

```
| CODE | PASSWORD |
```

WHERE:

CODE(1 BYTE) = 6

PASSWORD (X BYTES) =   A PASSWORD THAT MUST MATCH BEFORE THE RECEIVING STATION
ENTERS THE MOP MODE. IF THE PASSWORD IS SENT OVER A DDCMP
LINK IN THE MAINTENANCE MODE, THE LINK ENTERS THE DDCMP
MAINTENANCE MODE (DUE TO THE MAINTENANCE MODE ENVELOPE),
BUT THE MODE ONLY ENTERS THE MOP MODE (E.G., RESPOND TO LOAD
REQUESTS) IF THE PASSWORD MATCHES.

THE PASSWORD NUMBER CAN BE VARIABLE. THE DMC11 CHECKS ANY
PASSWORD NUMBER SPECIFIED BY THE CHARACTER COUNT MINUS
ONE IN THE HEADER. THE MAINTENANCE OPERATION MODE (MOP)
SPECIFICATION (VERSION 2.0) RECOMMENDS THE PASSWORD
NUMBER OF FOUR (4).

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Figure 3-14   Enter MOP Mode Format

- If the DMC11 is not currently in the DDCMP running state (given BASE I and CNTL I commands), this message is ignored.

- If the DMC11 is in the DDCMP running state, a CNTL O command is generated with an error code of 10_8, DDCMP MAINT received (a fatal error).

- If the DMC11 is currently in the DDCMP maintenance mode, this message is received and given to the PDP-11 program if a receiver buffer is assigned. If no receive buffer is available, the message is ignored.

If the line unit switch pack No. 2 is set to a value other than all ones (377_8), then reception of the enter MOP message causes the following actions to happen:

- The DMC11 verifies that the first byte is code 6.

- Each password following code 6 is compared against the content of switch pack No. 2 for a match. If the password and switch pack No. 2 do not match, then the following actions occur.

  - If the DMC11 is not currently in the DDCMP running state (given BASE I and CNTL I commands), this message is ignored.

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- If the DMC11 is in the DDCMP running state (start-up sequence completed after BASE I and CNTL I commands), a CNTL O command is generated with an error code of 10_8, DDCMP MAINT received (a fatal error).

- If the DMC11 is currently in DDCMP maintenance mode, this message is ignored.

- If each password matches the content of switch pack No. 2, then 173000 plus the content of switch pack No. 3 (E88 on the M8201, E91 on the M8202) is loaded into location 24_8 (PDP-11 physical memory location) via a DMA. Location 26_8 is loaded with 00000.

- The DMC11 then generates an AC LO on the system to simulate a system power failure to transfer control to a primary boot residing in a boot Read Only Memory (ROM). This boot ROM is an option and is sold separately.

NOTE
1. **Switch pack No. 3 on the line unit contains three octal digits (XXX) which are used to form an entry point to a boot ROM. The address formed is 173XXX.**

2. **On PDP-11/04, 11/34, and 11/40 CPU types, RLD is not recommended for unattended satellite operation.**

3. **On PDP-11/04, 11/34, and 11/40 CPU types, DMA activities (NPRs) are not allowed when the CPU is in the halted state. The REMOTE LOAD DETECT (RLD) might not work if the system halts when the DMC11 is in the process of doing an NPR for transmit, receive, or base update. In this case, the NPR is not completed, the DMC11 hangs up, and never sees the ENTER MOP message on the serial line. To overcome this situation, an operator must reset the system by pressing the RESET or INIT switch on the CPU console.**

On CPUs with a KY11-LB console, operator action must be in the following sequence:

1. CNTL INIT
2. CNTL HALT
3. CNTL HALT

This action clears the DMC11 and KY11-LB, allowing DMC11 reception of enter MOP and subsequent AC LO simulates the power fail of the CPU.

Figure 3-15 is an example of the setup procedures and required handshakes to complete an RLD operation. It is assumed that the DMC11 line unit at the remote station has the password for RLD set up in switch pack No. 2 and a correct offset from 173000 to enable entry of the DMC11 boot code in the ROM BOOT.

SOFTWARE AT HOST	DMC11 #1	SERIAL LINE	DMC11 #2	DMC11 BOOT CODE IN BOOT ROM (M9301-YJ/M9312)
1 – INITIALIZE DMC11 2 – BASE IN TO DMC11 3 – CONTROL IN TO DMC11 WITH SEL 6 = 2400 4 – BA/CCI FOR RECEIVE WITH CHARACTER COUNT OF 256 5 – BA/CCI FOR TRANSMIT WITH CHARACTER COUNT OF 5. TRANSMIT BUFFER IN PDP-11 MEMORY SHOULD LOOK LIKE 6 0 0 0 0 (PASSWORD = 0)	1 – TRANSMIT ENTER MOP MESSAGE 2 – DO A BA/CCO ON TRANSMIT DONE	DLE $MOP 6$	1 – CHECK THE FIRST BYTE = 6 2 – COMPARE PASSWORD (PSW) RECEIVED WITH PSW SELECTED IN LINE UNIT SWITCH 2 3 – IF ALL PSWs MATCH, DMA THE FOLLOWING TO PDP-11 MEMORY 24/173XXX, 26/0 XXX = LINE UNIT. SW3 4 – PULL AC LO ON UNIBUS	

NOTE (1)

IN DDCMP MAINTENANCE, THERE IS NO RETRANSMISSION;
BA/CCO FOR A TRANSMIT OPERATION DOES NOT ASSURE
SUCCESSFUL RECEPTION AT THE REMOTE END, THE SOFTWARE
MUST KEEP A REPLY TIMER OF 3 SECONDS TO RETRANSMIT THE
MESSAGE WHEN NO REPLY IS RECEIVED WITHIN THAT TIME

NOTE (2)

XXX MUST BE THE OFFSET
FROM 173000 OF THE
DMC11 BOOT CODE IN
M9301-YJ/M9312

PROGRAM CONTROL IS PASSED TO DMC11
BOOT CODE WHICH DOES THE FOLLOWING:
1 – INITIALIZE DMC11
2 – BASE IN TO DMC11
3 – CONTROL IN TO DMC11 WITH SEL6 = 2400
4 – BA/CCI FOR RECEIVE WITH A CHARACTER COUNT OF 4092
5 – BA/CCI FOR TRANSMIT WITH CHARACTER COUNT OF 4. TRANSMIT BUFFER IN PDP-11 MEMORY SOULD BE 10, 14, 1, 0 (MOP 8: REQUEST SECONDARY BOOT)
6 – SEE NOTE 1

7 – VERIFY MOP CODE = 0 AT LOCATION 0 THEN DO A SYSTEM RESET
8 – JUMP TO LOCATION 6 TO PASS PROGRAM CONTROL TO NEWLY LOADED PROGRAM

SOFTWARE AT HOST	DMC11 #1	SERIAL LINE	DMC11 #2
6 – CHECK VALIDITY OF REQUEST SECONDARY BOOT MESSAGE RECEIVED 7 – DO A BA/CCI RECEIVE WITH CHARACTER COUNT OF 256. 8 – DO A BA/CCI TRANSMIT WITH CHARACTER COUNT OF (X + 12). THE TRANSMIT BUFFER CONTAINS MOP 0 MEMORY LOAD WITH TRANSFER ADDRESS AS FOLLOWS: CODE (1 BYTE) = 0 LOAD NUMBER (1 BYTE) = 0 LOAD ADDRESS (4 BYTES) = 0 0 0 0 IMAGE DATE LOADED = X BYTES TRANSFER ADDRESS (4 BYTES) = 6 0 0 0 9 – SEE NOTE 1	3 – DO A BA/CCO RECEIVE TO PDP-11 4 – TRANSIT MOP 0 (MEMORY LOAD WITH TRANSFER ADDRESS) 5 – DO A BA/CCO TRANSMIT	DLE $MOP 8$ DLE $MOP 0$	1 – TRANSMIT REQUEST SECONDARY BOOT MESSAGE (MOP 8) 2 – DO A BA/CCO TRANSMIT 3 – DO A BA/CCO RECEIVE TO PDP-11

MK-0869

Figure 3-15   Example Set Up Procedure for RL

3.5.9 Performance Degradation on the DMC11-AL

The following are some of the conditions which could create performance degradation.

- When the receiver of DMC11-AL is actively receiving data, there is no port servicing and therefore the transmit/receive buffer assignments (BA/CCI), transmit/receive buffer returns (BA/CCO), and error reporting via CNTL O are delayed.

NOTE
If the DMC11-AL is receiving a data message and part of the data is lost because the transmission line is broken or the other DMC11-AL failed to finish transmission of the entire message, the receiving DMC11-AL will not service the port until all the missing data are received.

- When, on rare occasion, data traffic is very low on the full-duplex 1M bps DMC11-AL, acknowledgment of the transmitted data message could take a very long time (up to one second). The very low condition is defined as single buffering DMC11-AL and the data is flowing in only one direction where the completion of one data transmission will initiate the next. This condition can be avoided by multi-buffering the DMC11.

- When running a 1M bps, full-duplex DMC11 on a system with other high-speed DMA devices, there is a high probability of bus latency occurrence. This may be a problem for systems which cannot tolerate degradation because of latency errors. In some cases, DMC11 throughput may be reduced to zero, that is, heavy UNIBUS activity may prevent the DMC11 from completing any messages. Latency errors are detected by the DMC11 as BCC errors causing the DMC11 to initiate automatic error recovery (described below in detail).

If recovery fails because of prolonged latency conditions, the DMC11 spends all of its time attempting to recover. The DMC11 must service the character and complete the NPR in $8\mu s$. If this requirement is not satisfied, Data Late occurs; however, it is more likely to occur on an 11/70 system when the message size is large.

An even worse case condition may occur for a large size message where the DMC11 is single buffered.

1. DMC11 No. 1 sends a large message (for example, 1K byte) to the DMC11 No. 2.

2. DMC11 No. 2 receives part of the message; because of the occurrence of DATA LATE, a large portion of the message is lost.

3. DMC11 No. 2 continues to wait for the data that was lost to satisfy its character count before resetting the receiver.

4. Because DMC11 No. 1 is single-buffered (completion of one transmission initiates the next transmission), DMC11 No. 1 sends ACK every second and REP every 3 seconds until the transmitted message is acknowledged or a retransmission is requested by DMC11 No. 2.

5. The ACKs and REPs at DMC11 No. 2 are counted as part of the lost data until the missing number of characters is satisfied. Only then will the DMC11 No. 2 detect a BCC error and reset the receiver.

6. At DMC11 No. 1, for every eight REPs sent out (about 24 seconds), a time-out is reported via CNTL O; repeated every 24 seconds.

7. After DMC11 No. 2 detects the BCC error and resets the receiver, DMC11 No. 2 requests a retransmission.

8. The time required for eventual completion of the message transmission depends on system activities.

- Occurrence of serious system degradation due to latency can be reduced or totally avoided by careful system hardware and software configurations. Consider the following actions:

  1. Reduce DMC message length. On an 11/70 system, a character count of 256 bytes is recommended. Optimum count may require empirical derivation using actual system loading.

  2. Multi-buffer the DMC11. Assign more than one message buffer to both transmitter and receiver rather than only one buffer assignment at a time.

  3. Reduce DMC11 serial line speed; 56K bps may work as well as (or better than) a 1M bps line speed. This action may be true when:

     a. Software overhead prevents keeping the serial line busy.

     b. Excessive latency at 1M bps degrades system performance to a greater degree than running at 56K bps speeds.

  4. Multiplex UNIBUS DMA activity in software. Synchronize device operation to prevent contention for UNIBUS/MEMORY time.

  5. Off-load main CPU. Modularize system functions into subsystems, such as front end processing, reducing UNIBUS contention problems.

- For a DMC11-AL in half-duplex mode under a No-ReceiveBuffer-Available condition, the transmitting DMC11 generates a time-out via a CNTL O after eight retransmissions in less than a couple of seconds instead of 24 seconds. At about the same time, the receiving DMC11 generates a NO BUFFER AVAILABLE via CNTL OUT. The sequence of events is shown in Figure 3-16.

  Because neither time-out nor NO BUFFER AVAILABLE on a DMC11 is fatal, the software can recover from this situation if handled properly. At the receiving station, the software can either assign multiple receive buffers, or on NO BUFFER AVAILABLE notification from DMC11, assign some more receive buffers. At the transmitting system, the software must wait long enough for the remote system to assign additional receive buffers either by counting eight or more time-outs from the DMC11 or via other means of waiting.

```
CPU #1              DMC #1              DMC #2              CPU #2

ASSIGNS
A TRANS-
MIT BUFFER  ──────▶ TRANSMIT DATA ───────────▶

                                        NO RCV BUFFER

                                        SEND NAK
                        ◀───────────

            SELECT TIME OUT
            SEND REP                    SEND NAK
                        ───────────▶

                                        (REP RECEIVED)
                        ◀───────────

            RETRANSMIT
            DATA
                        ───────────▶


            ────────────────────────────────────────
                        REPEATED THE SEQUENCE
                              6 TIMES
            ────────────────────────────────────────

            RETRANSMIT
            DATA
                        ───────────▶

                                        NO RCV BUFFER,

                                        SEND NAK
                        ◀───────────

                                        NO BUF/CONT. 0. ──────────────▶

            SELECT TIME OUT,
            SEND REP.
                        ───────────▶

                                        SEND NAK
            TIME OUT/CONT. O            (REP RECEIVED)
    ◀───────────────────

                        ◀───────────

            RETRANSMIT
            DATA
                        ───────────▶


            ────────────────────────────────────────
                    THIS COULD GO ON FOREVER
            ────────────────────────────────────────
```
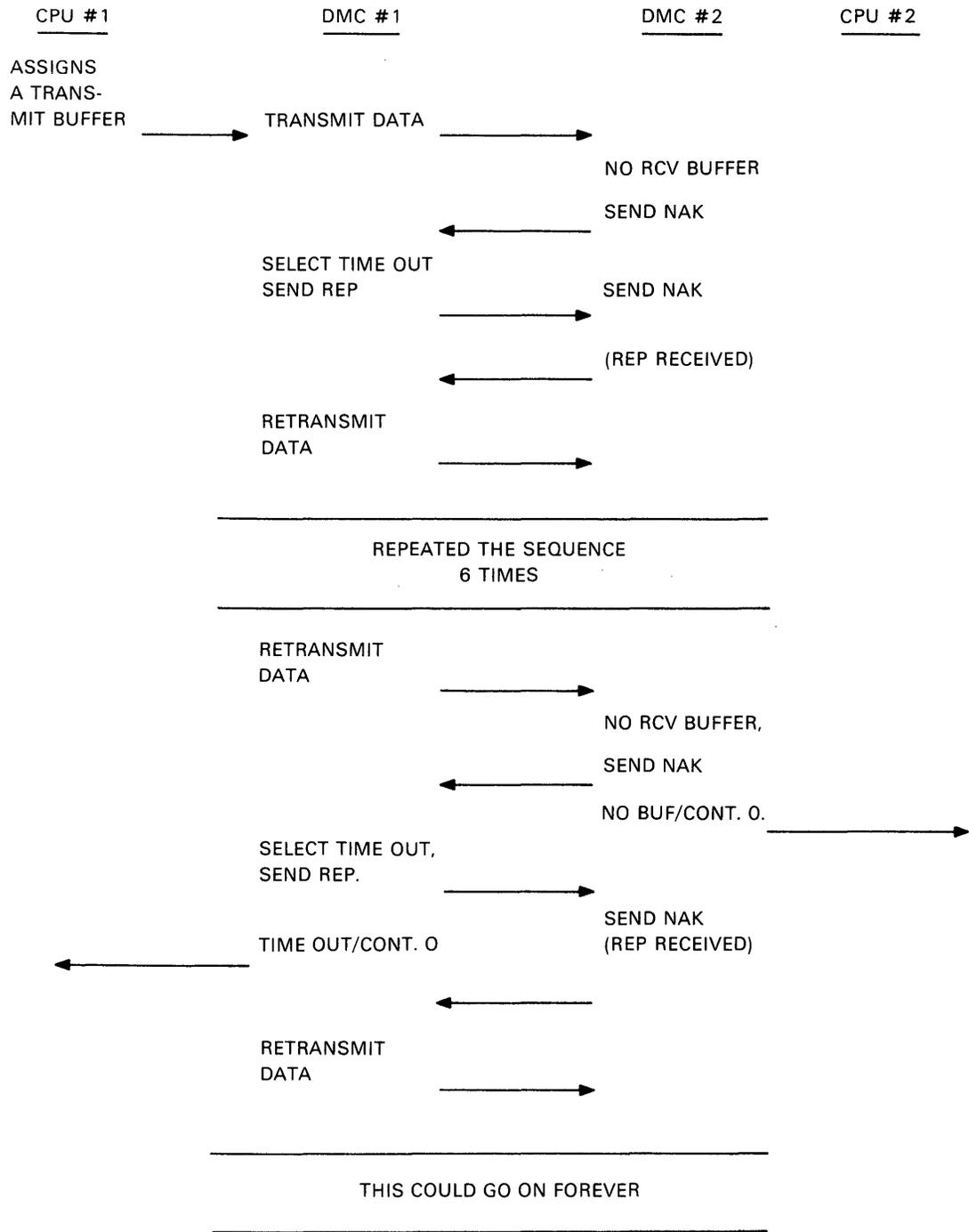
                                                            MK-0870

Figure 3-16   DMC11 Problem in High-Speed Code

- In half-duplex mode, if the remote DMC11 is down or the link is broken, the DMC11 **may not** report these conditions to the software, via time-out/CNTL O with an error code of 2.

  Condition A – If at the time of the link or remote DMC11 failure, the DMC11 has some outstanding transmit buffers (waiting for acknowledgment), then the conditions are reported as time-out.

  Condition B – If at the time of the line or remote DMC11 failure, the DMC11 does not have any outstanding transmit buffers (waiting for acknowledgments), then this condition is not reported. Even if more transmit buffers are assigned later, they are not transmitted, but entered into the transmit queue and therefore no time-out is ever reported.

  Condition B is not recoverable. In half-duplex mode time-out/CNTL O does not work properly.

CHAPTER 4
DETAILED DESCRIPTION

4.1 SCOPE
This chapter provides a detailed description of the DMC11 logic and a general description of the DMC11 microinstruction word formats.

4.2 MICROPROCESSOR DESCRIPTION

4.2.1 Introduction
The following discussion includes a detailed description of each register and associated logic in the DMC11 microprocessor. Figures 4-1 and 4-2 illustrate a general block diagram showing registers and all internal data paths. Throughout the chapter, reference these diagrams in all discussion relevant to data flow.

At times it becomes important to know the contents of registers relative to other registers as well as machine timing. Figure 4-3 shows this relationship with respect to the master clock.

4.2.2 DMC11/CPU Structures
The DMC11 microprocessor is a parallel 16-bit instruction, 8-bit data path microcomputer. Its architecture and instruction set are optimized for the character processing environment specific to network communications and other I/O-oriented systems. The DMC11 instruction cycle has a period ranging from 300 to 330 ns, and microinstructions are executed from a 1K × 16-bit control store referred to as the control ROM (CROM). Microinstructions executed from the CROM can access all DMC11 internal registers as well as a 256 × 8-bit data RAM.

Within the instruction cycle period, the DMC11 can (1) execute internal register-to-register transfers, (2) initiate bus requests (interrupt the main CPU), (3) initiate NPR transactions, and (4) perform transfers between an internal register and data memory. In addition, the DMC11 can perform a wide range of arithmetic and logical functions on internally transferred data. (The main CPU is defined as the resident PDP-11 processor and its associated memory.)

All internal registers and data paths are 8 bits wide. In addition, the Control and Status Registers (CSRs) are both word and byte addressable from the UNIBUS, but byte addressable only from the DMC11.

The microprogram can read from or write into all internal registers and memories, except the microinstruction memory (CROM), the memory address register (MAR), and the program counter (PC). The CROM can be addressed for microinstruction execution only through the PC, and the MAR can only be written into.

The DMC11 microprocessor executes two major classes of microinstructions: Branch and Move. Branch class microinstructions implement conditional and unconditional program jumps as well as subroutine entry and return. Move class instructions provide for interregister and intermemory data transfers and for logical and arithmetic operations on the transferred data.

Figure 4-1 is an overall block diagram of the DMC11. It shows the structure of the processor and the data paths connecting that structure. This section summarizes the structural components accessed through internal buses, by direct microinstruction execution and over the UNIBUS, as well as the Arithmetic Logic Unit (ALU), which is accessible to all internal registers.

4.2.2.1 INBUS/OUTBUS and INBUS*/OUTBUS* Register Definition – INBUS/OUTBUS and INBUS*/OUTBUS* refer to two register groups or categories within, and accessed by, the microprocessor. This terminology is used in microinstruction formatting. It defines the group of registers to be accessed by the microprocessor and whether the particular register is used as a source or destination for data.

- The "*" indicates one register group; the absence of the "*" indicates the other register group.

- The "IN" portion of the term identifies the specific register as the data source.

- The "OUT" portion of the term identifies the specific register as the destination for data.

- The "BUS" portion of the term does not refer to a physical BUS.

- The following terms are synonymous:

  OUTBUS and OUT
  INBUS* and IBUS*
  OUTBUS* and OUT*
  INBUS and IBUS

Registers in the "*" group (IBUS*/OUT*) are located in the multiport RAM:

CSR Bytes 0-7	(Registers 0 to 7 are read/write)
NPR Control	(Register 10 is read/write)
μP Miscellaneous	(Register 11 is read/write)

Registers in the INBUS/OUTBUS group located in the microprocessor:

IN DATA LB	Register 0 – R/W = low byte	DMA data from memory to the
IN DATA HB	Register 1 – R/W = high byte	microprocessor
OUT DATA LB	Register 2 – R/W = low byte	DMA data from the microprocessor to
OUT DATA HB	Register 3 – R/W = high byte	memory
IN BA <7:0>	Register 4 – R/W = low byte	DMA address for data from memory
IN BA <15:8>	Register 5 – R/W = high byte	to the microprocessor
OUT BA <7:0>	Register 6 – R/W = low byte	DMA address for data from the micro-
OUT BA <15:8>	Register 7 – R/W = high byte	processor to memory
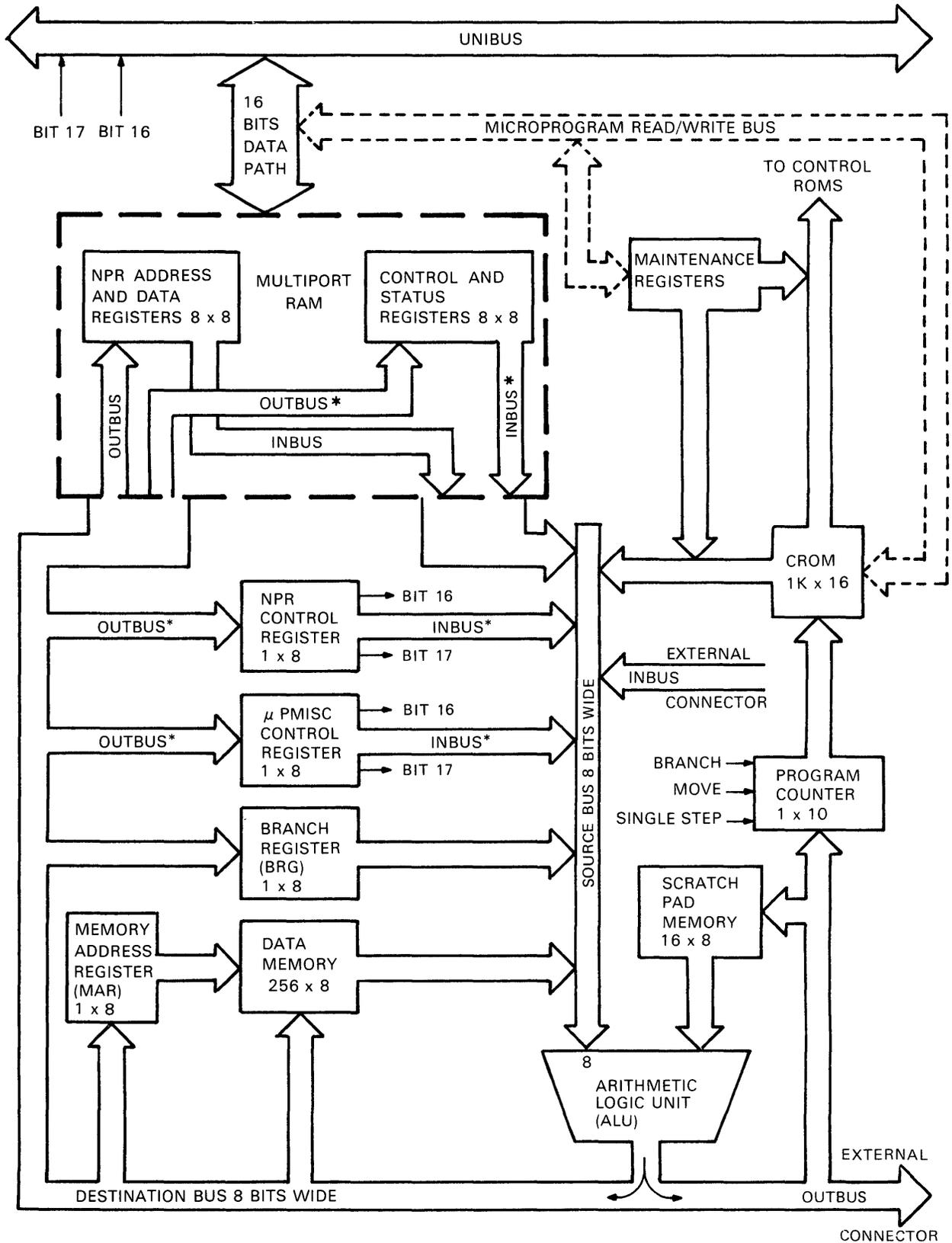
Figure 4-1 DMC11 Register and Data Path Structure

MK-0816
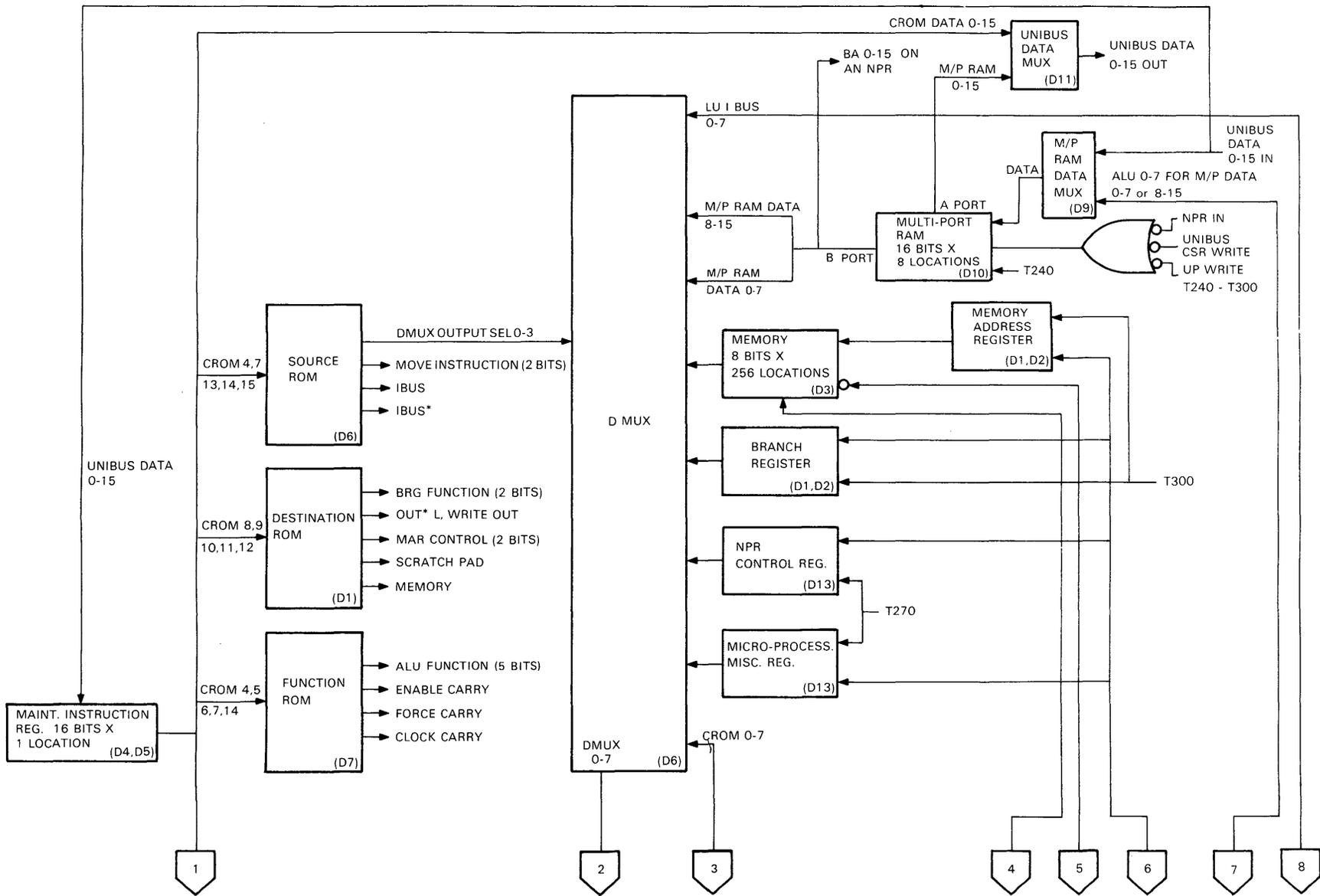
Figure 4-2   Microprocessor Block Diagram (Sheet 1 of 2)

4-4

MK-0817

Figure 4-2 Microprocessor Block Diagram (Sheet 2 of 2)

```
        T150              T240        T0                     T150              T240       T0
         |                 |          |                       |                 |         |
         |                 |          |                       |                 |         |


BALU      ┌─────────────────────────────────────────┐
          │          LAST INST RESULT OPERAND         │
          └─────────────────────────────────────────┘


PC                    ┌───────────────────────────────────────────┐
                      │       (PC+1) OR LAST INST RESULT OPER       │
                      └───────────────────────────────────────────┘


CROM                       ┌───────────────────────────────────────┐
                           │         CURRENT INSTRUCTION             │
                           └───────────────────────────────────────┘


MAR                    ┌───────────────────────────────────────────┐
                       │          LAST INST RESULT OPERAND           │
                       └───────────────────────────────────────────┘


BRG                    ┌───────────────────────────────────────────┐
                       │          LAST INST RESULT OPERAND           │
                       └───────────────────────────────────────────┘


SCRATCH PAD              ┌─────────────────────────────────────────┐
                         │        CURRENT INST "A" OPERAND           │
                         └─────────────────────────────────────────┘


MULTIPORT RAM            ┌─────────────────────────────────────────┐
                         │        CURRENT INST "B" OPERAND           │
                         └─────────────────────────────────────────┘


ALU                         ┌─────────────────────────────────────────┐
                            │       CURRENT INST RESULT OPERAND         │
                            └─────────────────────────────────────────┘
```
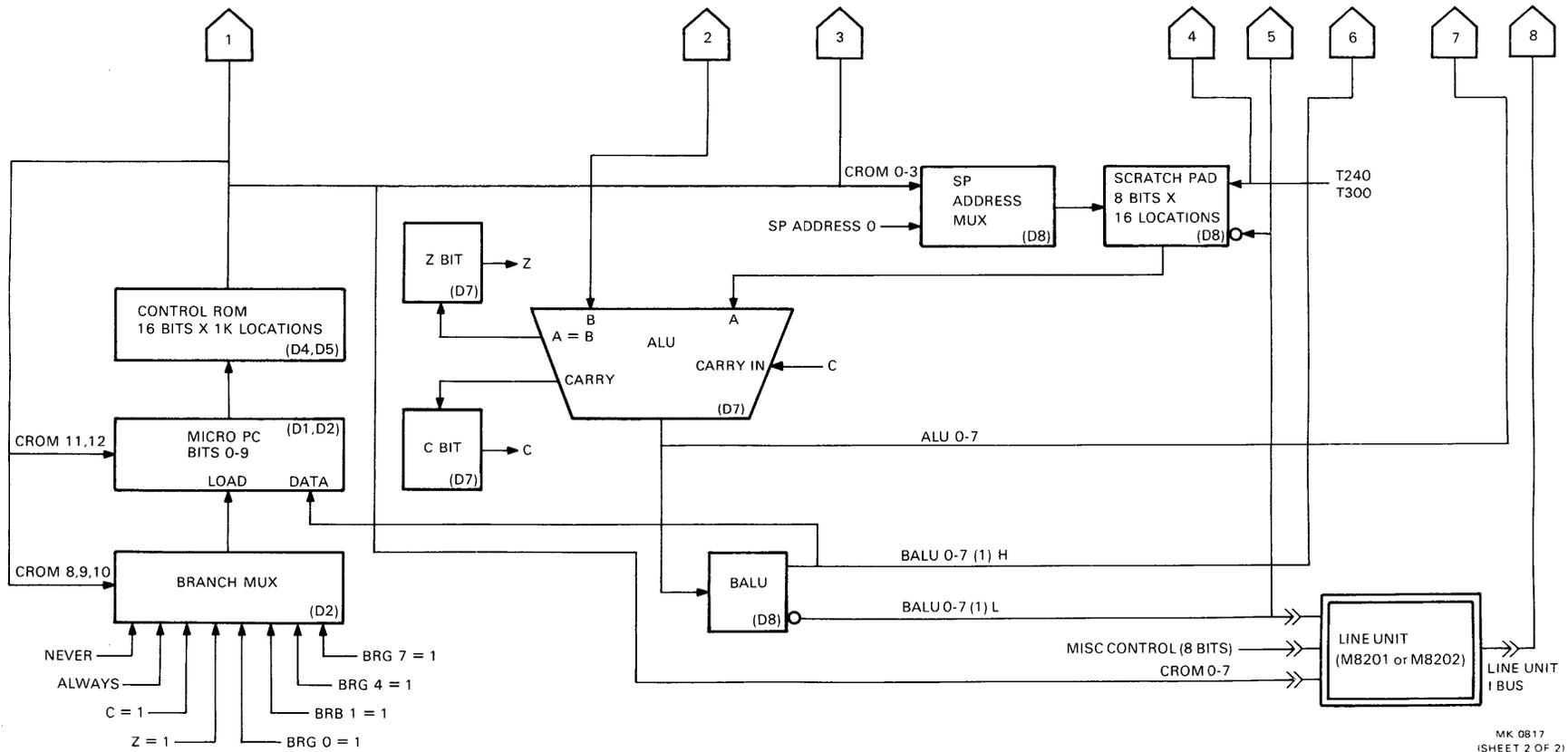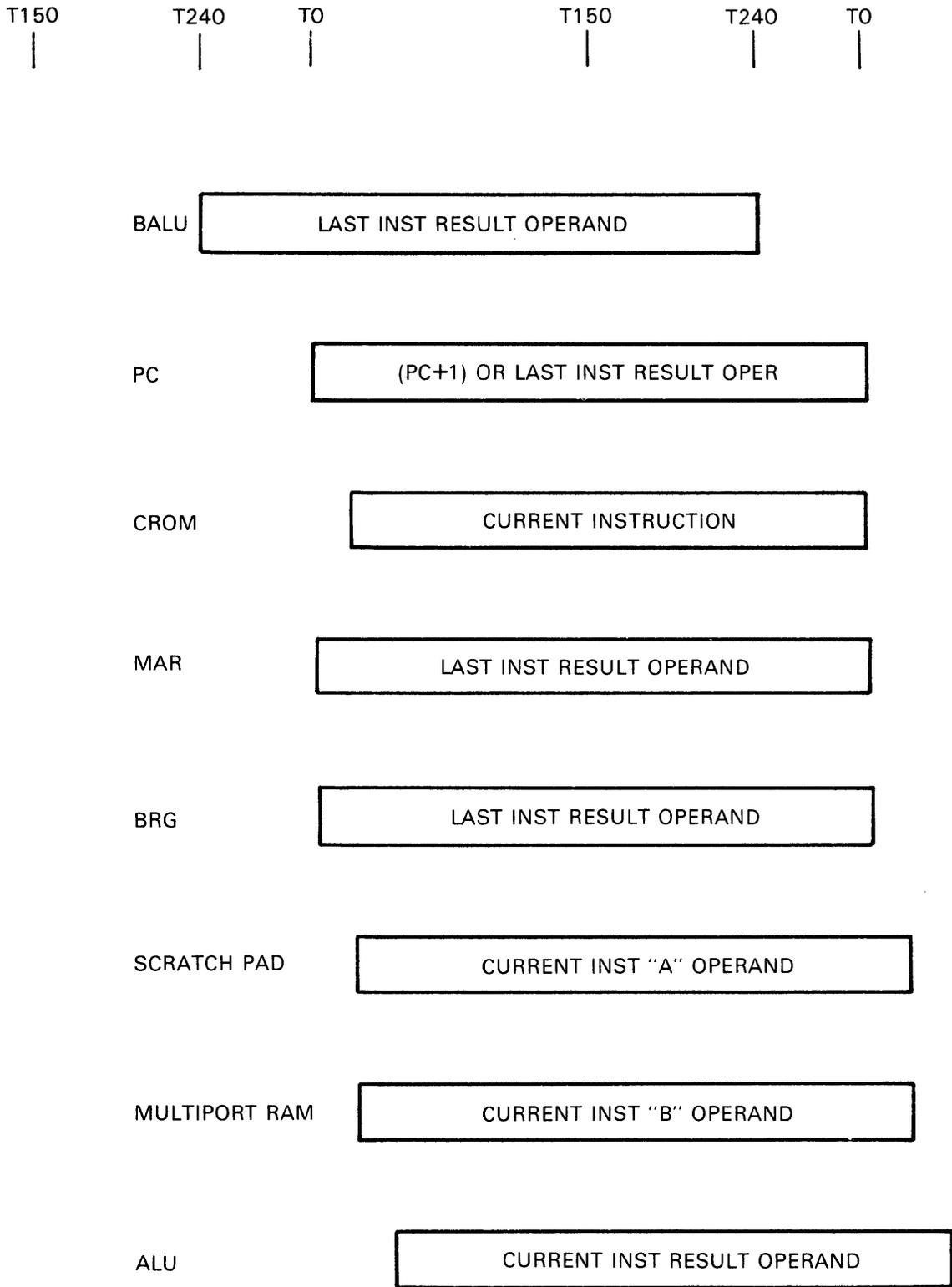
MK-0790

Figure 4-3   Microprocessor Register Timing

Registers in the INBUS/OUTBUS group located in the line unit*:

IN DATA SILO	Register 10 – Read = Receive data FIFO
OUT CONT	Register 11 – R/W = Output Control
OUT DATA SILO	Register 10 – Write = Transmit data FIFO
IN CONT	Register 12 – R/W = Input Control
MODEM CONT	Register 13 – R/W = Modem Control
SYNC REG	Register 14 – R/W = SYNC Character/Secondary Address
LNDSW REG	Register 15 – Read only = Switch Pack No. 2 Password
BM873 REG	Register 16 – Read only = Switch Pack No. 3 Boot Offset
MAINT REG	Register 17 – R/W = Maintenance

4.2.2.2 Multiport RAM – The multiport RAM is a 16-byte random-access memory divided into two 8-byte sections that are addressed as INBUS*/OUTBUS* registers and INBUS/OUTBUS registers. One section contains the CSRs for the DMC11 microprocessor, and the other serves as an address and data port for NPR transfers. As shown in Figure 4-1, the multiport RAM interfaces directly with the UNIBUS for bidirectional transfer of data words or bytes and the 16 low-order bits of a UNIBUS address. This memory is byte addressable from the microprocessor; the two 8-byte sections can be accessed by the microprogram for both read and write operations. The UNIBUS CSRs are accessed as INBUS*/OUTBUS* registers and NPR address/data interfaces through the INBUS/OUTBUS registers. From the UNIBUS, the CSRs are both word and byte addressable and can be read from and written into by the main CPU or another NPR device. (A detailed description of the multiport RAM is provided in Section 4.2.10.)

4.2.2.3 NPR Control Register – The NPR control register is an 8-bit formatted register that enables the microprogram to control input and output NPR transactions. This register also contains the two high-order bits of the UNIBUS address for an input NPR transaction. Note that an input NPR transaction involves the transfer of data from main CPU memory to the microprocessor. Conversely, an output NPR transaction involves transfer of data from the multiport RAM to main CPU memory.

The NPR control register is a read/write register and is addressed as a register in the INBUS*/OUTBUS* category. (NPR control bit descriptions are provided in Section 4.2.11.1.)

4.2.2.4 Microprocessor Miscellaneous Control Register – The microprocessor miscellaneous control (μPMISC) register is an 8-bit register that contains various control and function bits necessary for operation of the DMC11. For example, this register contains a one-second interval timer bit and a bit that flags the addressing of a nonexistent main CPU memory location by the microprocessor (NXM error).

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* Detailed descriptions of these registers are provided in the *DMC11 IPL Synchronous Line Unit Maintenance Manual*, Part No. EK-DMCLU-MM-002.

Specific bits are also available to the microprogram to control initiation of bus requests over the UNIBUS and to specify one of two vectors for appropriate interrupt processing. In addition, this register contains the two high-order UNIBUS address bits for an output NPR transaction. The μPMISC CONT register is R/W and is addressed as a register in the INBUS*/OUTBUS* category. (See Section 4.2.11.2 for bit descriptions.)

4.2.2.5 External Connector – The DMC11 microprocessor is equipped with an external connector that supports eight parallel data input lines and eight parallel data output lines. These lines provide the DMC11 with direct access to a high-speed peripheral device such as a DMC11 line unit.

Eight internal 8-bit register addresses are assigned to the supported line unit accessible by the microprocessor only. As shown in Figure 4-18, these registers (physically located in the external line unit) are read as IBUS registers and written as OUTBUS registers through the external connector.

4.2.3 Microinstruction Word Formats

Two different microinstructions can be executed by the DMC11 microprocessor. They are the Move and Branch microinstructions. These microinstructions reside as permanent microcodes in a read-only memory defined as the control ROM (CROM). The CROM has enough storage capacity to store a microprogram of 1024 words. Each microinstruction word is sixteen bits long.

4.2.3.1 Branch Instruction – Figure 4-4 illustrates the word format of the Branch microinstruction. Bits 13–15 are the operation code defining the microinstruction as a branch. The operation code defines further the source operand from which the partial branch address is developed. The branch address is the address of the next microinstruction, should the branch condition be satisfied.

The condition under which the branch is to occur is defined by bits 8–10. The resultant branch address is partially defined by bits 0–7 of the microinstruction. These eight bits are combined with microinstruction bits 11 and 12 to form the complete 10-bit branch address capable of addressing any of the 1024 locations within the CROM.

Three Branch microinstructions exist, each defining a different source operand from which to develop the eight low bits of the branch address.

4.2.3.2 4₈ – Branch Immediate (I)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	BAB		CONDITION			IMMEDIATE ADDRESS							
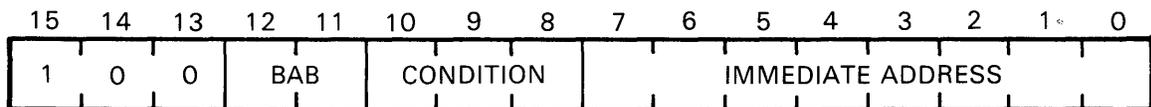
MK-0839

The microprogram branches if the condition specified by microinstruction bits 8–10 is met. The 10-bit branch address is the result of combining microinstruction bits 0–7 with the Branch Address Bits (BABs) – bits 11 and 12.

4.2.3.3 6₈ – Branch Memory (MEM)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	BAB		CONDITION			ALU FUNCTION				SP ADRS			
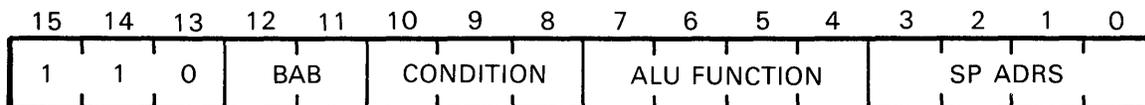
MK-0840

This microinstruction combines two operands in the ALU under control of the ALU FUNCTION bits (bits 4–7). When combined with microinstruction bits 1 and 12, the result operand produces a 10-bit branch address. One operand is from a MEM storage location and the other is from the scratchpad memory (SP). Microinstruction bits 0–3 address the operand in the SP while the MEM operand is from the location addressed by the current contents of the MAR. The desired address would have been loaded into the MAR by a previous instruction other than the Branch under execution. The condition for the branch is defined by the CONDITION CODE, bits 8–10. Figure 4-4 defines the ALU FUNCTION CODES that are possible with this microinstruction.

4.2.3.4 7_8 – Branch Register (BRG)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	BAB		CONDITION			ALU FUNCTION				SP ADRS			

MK-0820
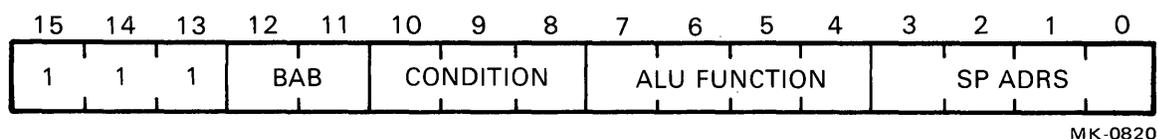
With this microinstruction, the contents of the BRG and an SP memory location are operated on to generate the partial Branch address. Bits 0–3 specify the SP location and bits 4–7 define the ALU FUNCTION to perform on the two operands.

4.2.3.5 Move Instruction – Like the Branch, Move is a highly versatile microinstruction. When combined with the Branch in a microprogram, the combination produces a DMC-11 microprocessor of high versatility and power. In all, five variations of the Move microinstruction exist, each specifying a different source for the operand. The source is defined by the operation code. Figure 4-5 illustrates the Move microinstruction word format.

The operation code is defined by bits 13–15. Bits 11 and 12 specify the function to perform on the MAR. According to bits 11 and 12, the MAR can remain unmodified, incremented, or loaded from the Buffered ALU (BALU). The destination of the result operand is defined by microinstruction bits 8–10. The low byte of the microinstruction is operation code dependent further defining input addresses, ALU function, and output addresses.

The ALU Function field (see Figure 4-5) microinstruction bits 4–7, define the operation to be performed on the two operands. These four bits and operation code bit 14 serve as the address input to the Function ROM (FROM). The FROM microword controls the ALU inputs. Common to all five Move microinstructions are the MAR Function field and the Destruction field. The MAR can be unmodified as per the previous paragraph. The MAR increment and load function sets up the MEM operand for the next microinstruction where necessary. The Destination field, as the name implies, specifies the destination of the result operand. Three of the eight possible destination references are microprocessor discrete registers, that is, BRG, MEM, and BRG shifted and consequently need no further address definition. The specific location in MEM was predefined with a previous microinstruction. Four destination references require still further address definition. These include OUTBUS, registers OUTBUS*, registers SP, and SP/BRG. The four low order bits (bits 0–3) of the microinstruction provide a specific destination address within OUTBUS, registers OUTBUS* or the SP memory when any of these are referenced as a destination.

When destinations OUTBUS register and OUTBUS* register are microprogrammed, SP address 0 is presented to ALU input A. Thus, if Move instruction MEM or BRG is used, all 16 ALU functions are available to operate on the two source operands (SP0 and MEM or BRG).

4-9

BRANCH

```
 ┌──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┐
 │15       13│12  11│10      8│7                  0│
 └──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┘
```

OP CODE
DEFINED

SOURCE
OPERAND

1 0 0	BRANCH ADD-RESS BITS 9,8	BRANCH CONDITION	BRANCH ADDRESS	
1 1 0			ALU FUNCTION	SCRATCH PAD ADDRESS
1 1 1				

```
0 0 0 — RESERVED
0 0 1 — UNCONDITIONAL BRANCH
0 1 0 — BRANCH IF C BIT IS SET
0 1 1 — BRANCH IF Z BIT IS SET
1 0 0 — BRANCH IF BRG BIT 0 IS SET
1 0 1 — BRANCH IF BRG BIT 1 IS SET
1 1 0 — BRANCH IF BRG BIT 4 IS SET
1 1 1 — BRANCH IF BRG BIT 7 IS SET
```

THESE TWO BITS COMBINED WITH THE EIGHT BIT ALU OUTPUT FORM THE COMPLETE TEN BIT ADDRESS.

1 0 0 — IMMEDIATE: BITS 0-7 OF THE MICROWORD COMBINED WITH BITS 11 AND 12 FORM THE BRANCH ADDRESS.

1 1 0 — MEM: THE MEM CONTAINS THE SOURCE OPERAND TO BE COMBINED WITH THE SP MEMORY OPERAND AS DEFINED BY THE ALU FUNCTION BITS.

1 1 1 — BRG: THE BRG CONTAINS THE SOURCE OPERAND TO BE COMBINED WITH THE SP MEMORY OPERAND AS DEFINED BY THE ALU FUNCTION BITS.

ALU FUNCTION		CODE
2's COM SUB	(A-B)	1110
1's COMP SUB	(A-B-1)	1111
ADD	(A,B)	0000
ADD W/C	(A,B,C)	0001
SUB W/C	(A-B-C)	0010
INC A	(A,1)	0011
A PLUS C	(A,C)	0100
2A	(A,A)	0101
2A W/C	(A,A,C)	0110
DEC A	(A-1)	0111
SEL A	(A)	1000
SEL B	(B)	1001
A OR $\bar{B}$	(A+$\bar{B}$)	1010
A AND B	(AB)	1011
A OR B	(A+B)	1100
A X OR B	(A⊕B)	1101

NOTES:

C = CARRY
W/C = WITH CARRY
C AND Z ARE SET/CLEARED WITH MOVE INSTRUCTIONS.
A = ARITHMETIC OR SCRATCH PAD (SP) SIDE OF ALU.
B = LOGIC OR DMUX SIDE OF ALU.

MK-0829

Figure 4-4   Branch Microinstruction Word Format

4-10

MOVE

| 15 | 13 | 12 | 11 | 10 | 8 | 7 | | | | | | | | 0 |

0 0 0	MAR FUNC-TION FIELD	DESTINATION FIELD	IMMEDIATE OPERAND	
0 0 1			INPUT ADRS	OUTPUT ADRS
1 0 1			INPUT ADRS	OUTPUT ADRS
0 1 0			ALU FUNCT	OUTPUT ADRS OR SCRATCH PAD ADRS
0 1 1			ALU FUNCT	
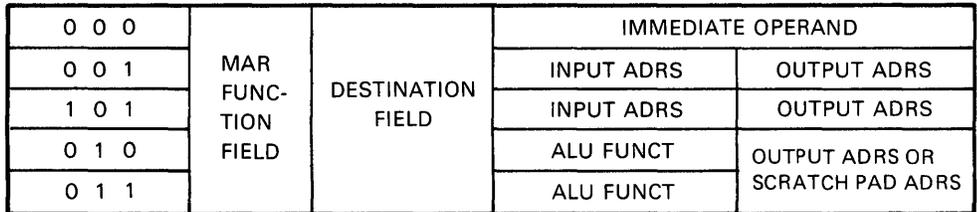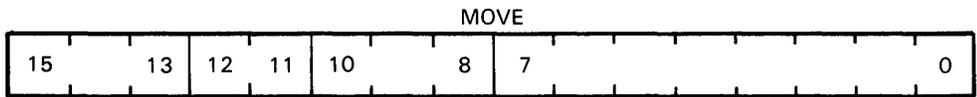
```
0 0 0 — NO OPERATION
0 0 1 — BRG
0 1 0 — OUTBUS* (SPO→A)
0 1 1 — BRG RIGHT SHIFTED ONE BIT
1 0 0 — OUTBUS (SPO→A)
1 0 1 — MEM
1 1 0 — SCRATCH PAD
1 1 1 — SCRATCH PAD AND BRG
```

```
0 0— RESERVED NO EFFECT
0 1— RESERVED NO EFFECT
1 0— LOAD MAR
1 1— INCREMENT MAR
```

```
0 0 0 — IMMEDIATE OPERAND IN BITS 0-7 OF
        MICROINSTRUCTION.

0 0 1 — IBUS IS OPERAND SOURCE DEFINED BY
        MICROINSTRUCTION BITS 4-7 AND
        DESTINATION DEFINED BY BITS 8-10.

1 0 1 — IBUS* IS OPERAND SOURCE DEFINED BY
        MICROINSTRUCTION BITS 4-7 AND DESTINATION
        DEFINED BY BITS 8-10.

0 1 0 — MEM IS OPERAND SOURCE OPERATED ON AS
        DEFINED BY ALU FUNCTION (BITS 4-7).

0 1 1 — BRG IS OPERAND SOURCE OPERATED ON AS
        DEFINED BY ALU FUNCTION (BITS 4-7).
```

ALU FUNCTION		CODE		
2's COM SUB	(A-B)	1110		
1's COMP SUB	(A-B-1)	1111		
ADD	(A,B)	0000		
ADD W/C	(A,B,C)	0001	MOV INST CLOCK C (NOTE 1)	
SUB W/C	(A-B-C)	0010		
INC A	(A,1)	0011		
A PLUS C	(A,C)	0100		MOV INST CLOCK Z (NOTE 2)
2A	(A,A)	0101		
2A W/C	(A,A,C)	0110		
DEC A	(A-1)	0111		
SEL A	(A)	1000		
SEL B	(B)	1001		
A OR B	(A+B)	1010		
A AND B	(AB)	1011		
A OR B	(A+B)	1100		
A X OR B	(A⊕B)	1101		

NOTES:
1. IF ADD FUNCTION, C IS SET TO INDICATE CARRY OR OVERFLOW.
   IF SUB FUNCTION, C IS CLEARED TO INDICATE BORROW OR SIGN CHANGE.

2. Z IS SET WHEN ALU OUT IS ALL 1S.

3. C = CARRY
   W/C = WITH CARRY
   A = ARITHMETIC OR SCRATCH PAD (SP) SIDE OF ALU.
   B = LOGIC OR DMUX SIDE OF ALU.

MK-0830

Figure 4-5   Move Microinstruction Word Format

The BRG right shift destination performs a right shift on bits 7 to 0. Bit 0 is passed through the ALU B side before returning to BRG bit 7 during a Move type BRG instruction. This allows all 16 ALU functions with the SP to be used for the possible alteration of the data bit which was returned to BRG bit 7.

Instruction types MOV I, MOV IBUS, MOV IBUS*, and MOV MEM may also be used with a BRG right shift. However, in these cases, ALU bit 0 is a function of sources I, IBUS register, and IBUS* register, while MOV MEM, which is similar to MOV BRG, is a function of MEM and SP as selected by the 16 ALU functions.

4.2.3.6 0₈ - Move Immediate (I)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	MFF		DEST			IMMEDIATE OPERAND							
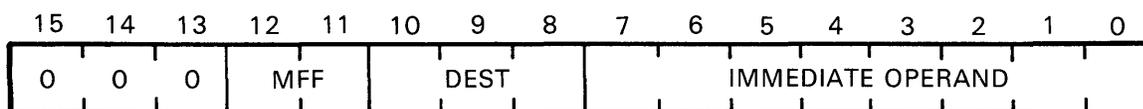
MK-0837

The operand (microinstruction bits 0–7), is moved to the destination as specified by microinstruction bits 8–10.

With the MOVE IMMEDIATE, the destination reference is normally limited to the BRG, MEM, and the MAR. The other possible destination references are useable; however, they require special consideration since the same data is used both as an operand and destination address.

4.2.3.7 1₈ - Move INBUS (IBUS)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	MMF		DEST			ALU FUNCTION				OUTPUT ADRS			
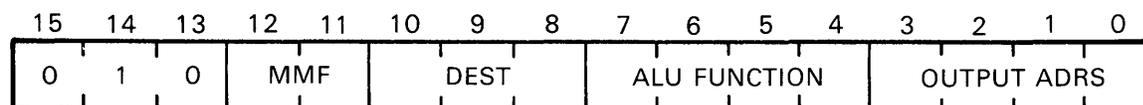
MK-0835

The operation code specifies the IBUS register as the source operand. However, since the IBUS register is a block of sixteen 8-bit words, additional address information must be provided by the INPUT ADDRESS portion of the microinstruction (bits 4–7). In cases where the Destination field specifies data blocks, that is, OUTBUS, OUTBUS*, or the SP microinstruction bits 0–3 specify the byte position within the block as the destination. In addition, the operand can also be clocked into the MAR when so indicated by the MAR Function field microinstruction word, bits 11 and 12.

4.2.3.8 5₈ - Move INBUS* (IBUS*)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	MFF		DEST			INPUT ADRS				OUTPUT ADRS			
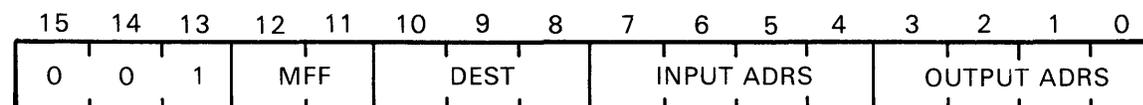
MK-0838

This microinstruction is similar to the Move IBUS microinstruction with the exception that the Move IBUS* addresses the IBUS* register block of words.

4.2.3.9 2_8 – Move Memory (MEM)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	MFF		DEST			INPUT ADRS				OUTPUT ADRS			

MK-0819
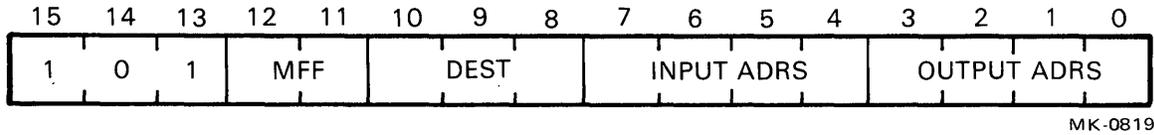
The Move MEM microinstruction performs either an arithmetic or logical operation on two designated operands and deposits the result operand into the specified destination address. One of the two operands is from MEM while the second is from the SP. The specific location within the SP memory is defined by the microinstruction OUTPUT ADDRESS field (bits 0-3).

The result operand is moved to the destination as specified by the Destination field (microinstruction bits 8-10).

When the SP or MEM is designated as the destination, then the respective source operand is destroyed by delivery of the result operand.

4.2.3.10 3_8 – Move Branch Register (BRG)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	MFF		DEST			ALU FUNCTION				OUTPUT ADRS			

MK-0836
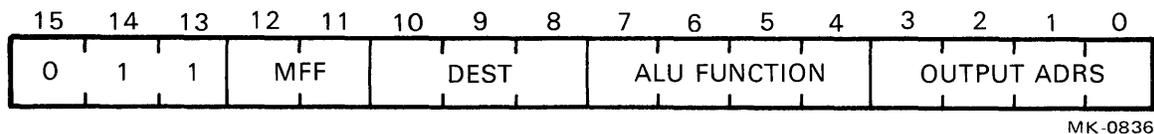
The operation of the Move BRG microinstruction is similar to the Move MEM with one exception. The two operands of this microinstruction are the contents of the BRG and the SP. If the microinstruction specifies either the SP or the BRG as the destination, then the respective source operand is destroyed by the delivery of the resultant operand.

4.2.4 CROM, MAR, BR, PC and Branch MUX

The basic microprogram stored in the CROM is addressed by a 10-bit PC (see Figure 4-6). The PC operates in two modes. It can be either incremented or parallel loaded from the BALU. The Branch Multiplexer (Branch MUX) output determines which function occurs. A low condition on the Branch MUX output causes the PC to load, that is, branch. The PC is always altered on the trailing edge of T240. Eight bits of the branch address come from the BALU, while the two high order bits come directly from the microinstruction word (bits 12 and 11).

CROM bits 8-10 determine which one of eight inputs is selected by the Branch MUX. The truth table in Figure 4-6 lists the selection codes controlling the MUX. Note that the Branch MUX is disabled when executing any Move microinstruction. Conversely it would be enabled for all Branch microinstructions.

Using the BRG, the microprocessor has the ability to shift a byte of data one bit position to the right, each time the appropriate microinstruction is executed. Data is rotated to the right with BALU 0 in the loop. BALU 0 gates to BRG7 while BRG0 passes through the ALU and is subsequently clocked into BALU 0.

4-13
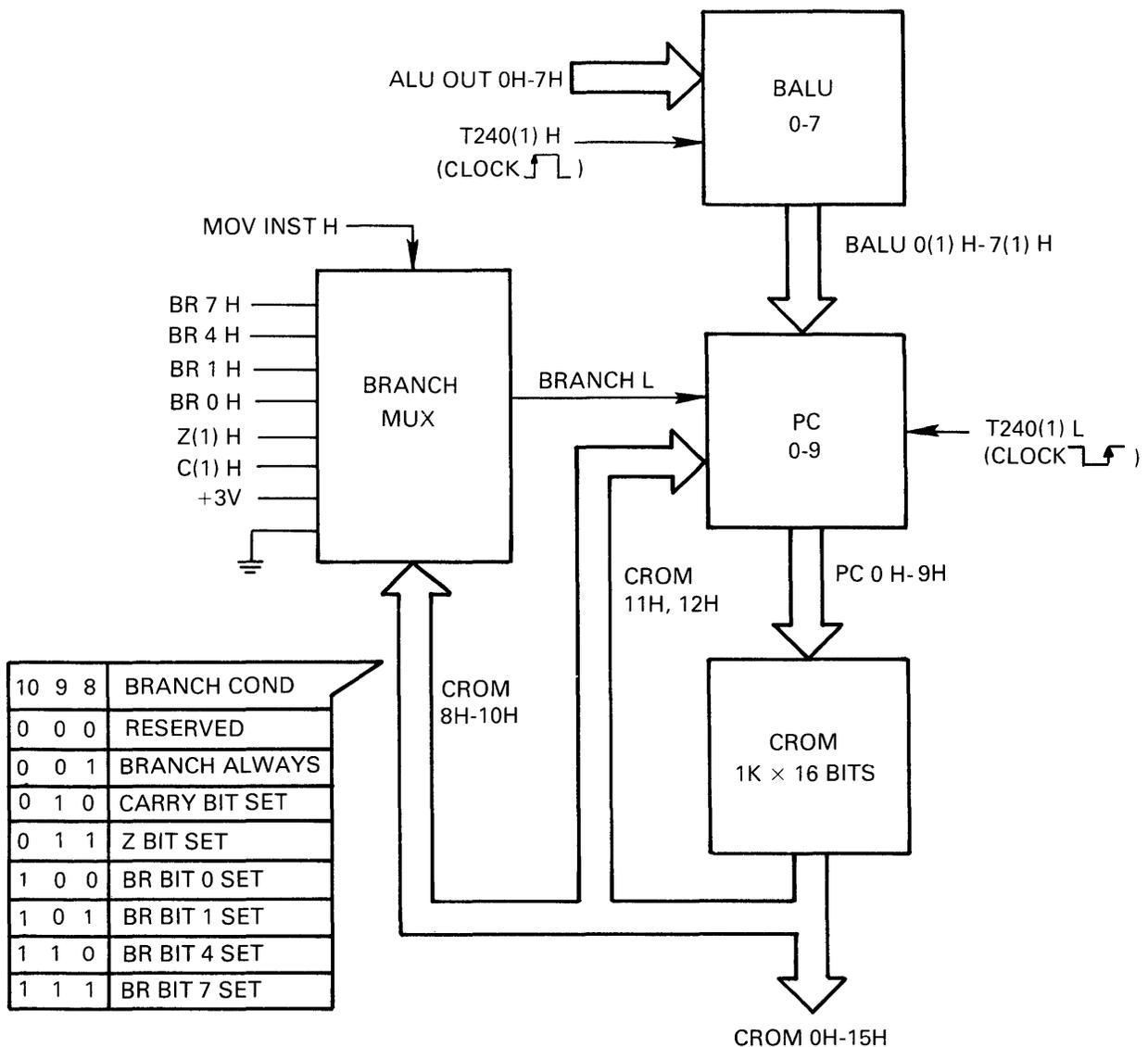
Figure 4-6   Block Diagram of Program Counter Control Logic

Control of the BRG is determined by the two inputs S0 and S1. With these two control signals, the BRG can load data, shift data, or recirculate data.

See the truth table in Figure 4-7. While S0 and S1 determine what function to perform, the clock signal, CLOCK MAR, BRG L, determines when to do it. This BRG clock always occurs on the trailing edge of T240 when executing a MOV microinstruction.

Main memory (MEM) with 256 locations is addressed by the 8-bit MAR. Like the PC, the MAR can be parallel loaded from the BALU outputs or incremented on the trailing edge of the clock signal CLOCK MAR, BRG L. Clocking always occurs on the trailing edge of T240 during execution of a Move microinstruction. Two bits of the Destination ROM (DROM) microword determine the function to perform on the MAR (MAR LD L and MAR INC EN L).

4-14
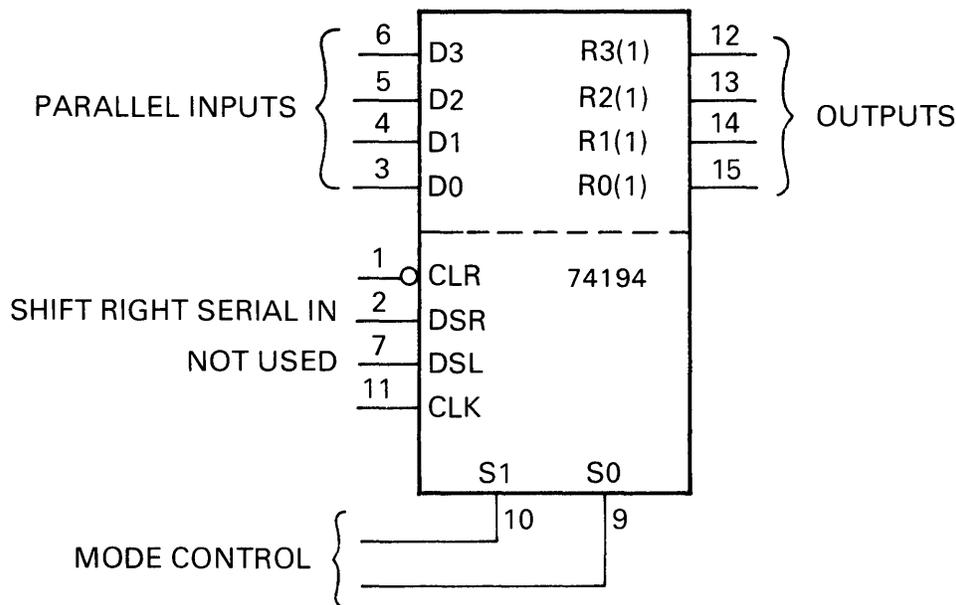
74194 TRUTH TABLE

S1	S0	FUNCTION
1	1	PARALLEL LOAD
0	1	SHIFT RIGHT
1	0	NOT USED
0	0	HOLD (INHIBIT CLOCK)

REFER TO
D1 & D2 OF
M8200 PRINT SET

THE BRG IS COMPOSED OF TWO 74194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS.

MK-0793

Figure 4-7 Configuration of the B Register

As previously discussed, the DROM microword controls the MAR and the BRG. It also has four additional bits to control writing into MEM, SP memory, SP/MAR, and the OUTBUS*. Microinstruction bits 8–12 form the DROM address which in the Move microinstruction represents the Destination field and MAR Function field. The DROM is shown in Figure 4-8 and the DROM map is shown in sheet D20 of the print set.

4.2.5 Main Memory (MEM)
Eight integrated circuit chips constitute the 256 location main memory. Each chip stores one bit of an 8-bit byte. Stored in the memory are items such as message headers and commonly used protocol messages.

4-15

```
                5610/6331
                 D ROM
                            1
                        D8 ─────  BRG S0 H
                            2
                        D7 ─────  BRG S1 H
  CROM 8 H  ──10──  A0    D6 ──3── OUT *L
  CROM 9 H  ──11──  A1        4
                        D5 ─────  WRITE OUT H
  CROM 10 H ──12──  A2    D4 ──5── MAR LD EN H
  CROM 11 H ──13──  A3        6
                        D3 ─────  MAR INC EN L
  CROM 12 H ──14──  A4    D2 ──7── WRITE SP H
                            9
                        D1 ─────  WRITE MEM H

              ──○ CE
          ═══

        32 WORDS × 8 BITS
```

REFER TO D1 OF
M8200 PRINT
SET
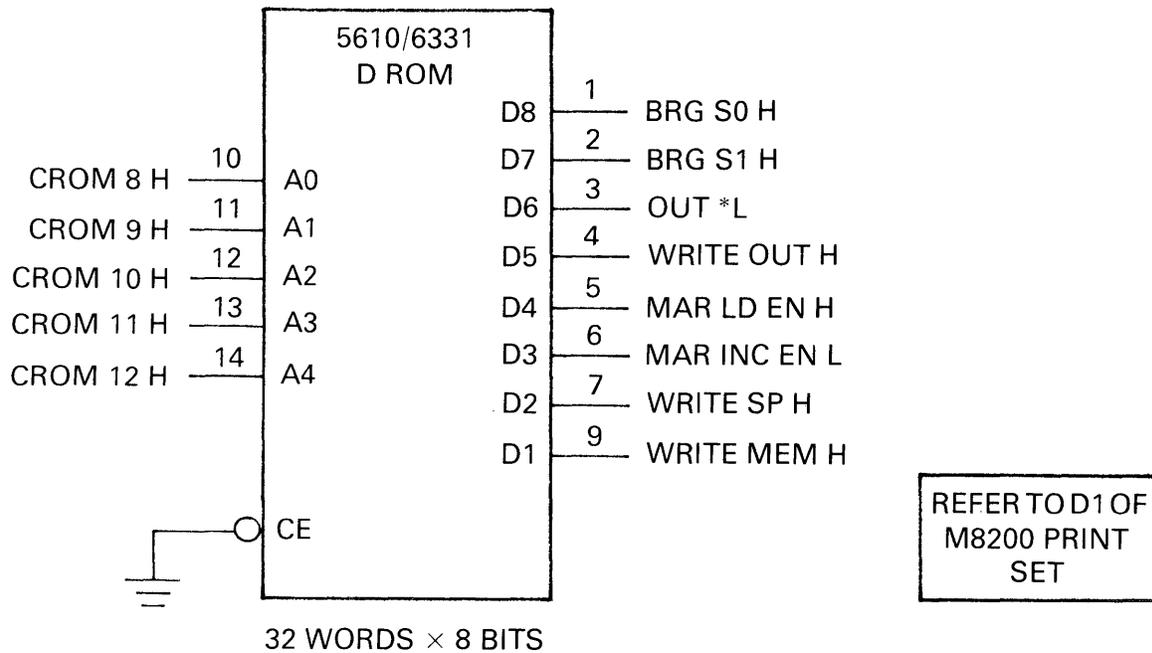
SEE PRINT SET SHEET D20 FOR DROM MAP.

MK-0794

Figure 4-8   Configuration of DROM

Memory addressing is accomplished using the MAR, while write data is gated directly from the BALU outputs. Write timing is controlled through the function WRITE MEM L, originating at the DROM. The memory contents can be sourced with the Move microinstructions and two of the three Branch microinstructions. Operation code 6_8 can only read MEM contents.

The MEM output feeds the Data multiplexer (DMUX) input and is selected with a code of 2_8 for a Move or 6_8 for a Branch. The DMUX selects the MEM output during execution of the Move MEM or Branch MEM microinstruction.

4.2.6   CROM and the Maintenance REG

The CROM is the heart of the microprocessor system through which complete system control is exercised. Stored within the CROM is the unique microprogram necessary for execution of the DDCMP. This stored microprogram utilizes the two powerful microinstructions discussed at the beginning of this chapter. A total of 1024 memory storage locations are available for the microprogram through the use of eight integrated circuit chips. Each chip stores four bits of the microinstruction in 512 storage locations. Addressing is done with the 10-bit PC.

Fields within microinstructions read from the CROM become the addresses for a second-level microword contained within three additional ROMs, DROM, FROM, and SROM (Source ROM).

In addition, certain microinstruction bits directly control gating and timing operations throughout the microprocessor.

4-16

Each ROM chip has a chip enable input (pin 13) which must be asserted low in order to enable the chip. Because these chips are tri-state devices, a disabled chip presents a high impedance (high Z) output allowing the wire ORing of outputs, thus expanding total memory capacity. In the microprocessor, two memory chips (each storing 512 4-bit words) have their outputs wired together forming a memory of 1024 locations. The appropriate chip is selected with signal PC9 (pin 13, E34 page D2 of the *Print Set*).

A maintenance feature of the microprocessor allows the PDP-11 software to simulate the CROM outputs through the use of the Maintenance Register. The output of the Maintenance Register is wire ORed with the CROM output. With the CROM disabled and the Maintenance Register enabled, the contents of the register become the system microinstruction. The register is loaded from the UNIBUS data receivers when Select 6 (SEL 6) of the CSRs is loaded from the PDP-11 and ROM I (Bit 9) in BSEL 1 is asserted. ROM I also deselects the CROM (high Z outputs).

4.2.7 DMUX and SROM
The DMUX is an 8-bit wide, eight-to-one multiplexer, whose output feeds the B input of the ALU. Input selection is controlled by three bits originating at the SROM. The DMUX and associated truth table are shown in Figure 4-9.

The SROM is a 32-location ROM containing an 8-bit microword. The SROM is shown in Figure 4-10 and the SROM map is shown in sheet D20 of the print set. The SROM is addressed directly by the CROM (bits 13–15, 4 and 7). Note that three of these bits (15, 14, 13) are the microinstruction operation code.

4.2.8 ALU and Associated Logic
With the ALU, the microprocessor can execute ten arithmetic and six logical operations on any data presented to its A and B inputs (see Figure 4-11).

The ALU is built around two 74S181 integrated circuit chips, each accommodating four bits or one half byte. Four functional inputs feed the ALU while three others output from it. Two of the inputs are 8-bit operands. A third input, CARRY IN, is a carry function which can be inserted under control of the microprocessor. The fourth and final input is a 5-bit function bus defining the type of operation to perform on the two operands and carry in. This operation is defined by the FROM microword. The FROM is shown in Figure 4-12 and the FROM map is shown on sheet D20 of the print set.

The result of any logical or arithmetic operation appears asynchronously at the ALU's output data bus and on the leading edge of T240, and is clocked into the BALU. Another output Z becomes asserted when the ALU output is all 1s. The third and final output is the carry bit. Both the carry bit and the A = B output are clocked into storage flops, under control of the FROM microword.

Insertion of a carry occurs under one of two conditions defined by the FROM. A carry insert can be forced with FORCE C H or inserted as a function of the C flip-flop with ENABLE C H.

4.2.9 Scratchpad Memory (SP)
The only way to present an operand to the ALU A input is through the SP memory. The SP contains sixteen locations, all addressable by CROM bits 0–3. Two type 3101 integrated circuits chips, each storing one-half byte, comprise the complete memory.

Addressing is controlled by a 74157 multiplexer, supplying one of two possible inputs as a 4-bit address to the SP. Selection is by DI WRITE OUT H, which when asserted selects a hardwired input address of zeroes. The default input is CROM bits 0–3. This signal is a bit in the DROM microword. The DROM also controls writing into the SP. Data is written from the BALU output.

4-17
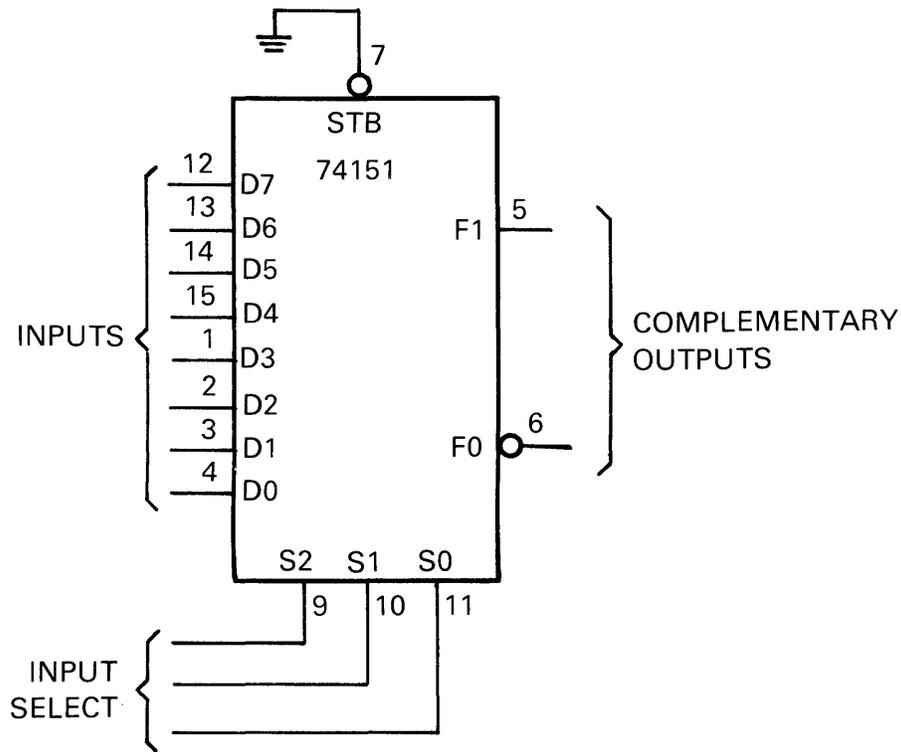
74151 TRUTH TABLE

SELECT			INPUT
S2	S1	S0	
H	H	H	D7-μP MISC REG
H	H	L	D6-NPR CNTL REG
H	L	H	D5-BPORT ODD BYTE
H	L	L	D4-BPORT EVEN BYTE
L	H	H	D3-BRG
L	H	L	D2-MEM
L	L	H	D1-LU IBUS
L	L	L	D0-CROM 0-7

REFER TO D6
OF M8200
PRINT SET

THE DMUX IS COMPOSED OF EIGHT 74151 MULTIPLEXERS.

MK-0795

Figure 4-9   Configuration of DMUX

4-18

```
               ┌─────────────────┐
               │    5610/6331    │
               │     S ROM       │
               │                 │  9  ┐
               │             D8 ├─────┤
               │             D7 ├─ 7  ├  DMUX SRC
 CROM 15 H  14 │ A4          D6 ├─ 6  │
 CROM 14 H  13 │ A3          D5 ├─ 5  ── MOV INST H
 CROM 13 H  12 │ A2          D4 ├─ 4  ── MOV INST L
 CROM 7 H   11 │ A1          D3 ├─ 3  ── IBUS* H
 CROM 4 H   10 │ A0          D2 ├─ 2
               │             D1 ├─ 1  ── IBUS  H
               │                 │
           ──○─┤ CE              │
               │                 │
               └─────────────────┘
```

REFER TO D6
OF M8200
PRINT SET

32 WORDS × 8 BITS
SEE PRINT SET SHEET D20 FOR SROM MAP.
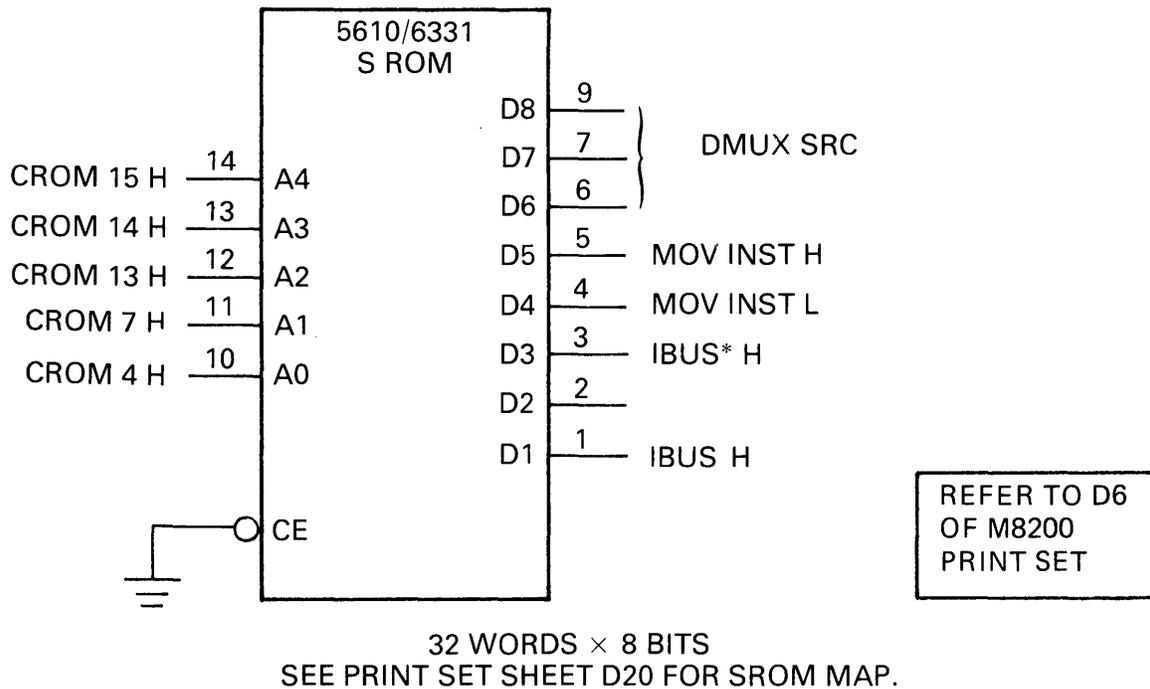
Figure 4-10   Configuration of SROM

4.2.10 Multiport RAM

The multiport RAM is an 8-word random access memory having the capability of being simultaneously accessed from two sources. Each word is sixteen bits in length. A total of four chips comprise the multiport RAM with each chip containing 8-bit wide storage locations. A functional description of the chips follow (refer to Figure 4-13).

Two independent read outputs are available, one referenced as the A PORT (pins 8, 9, 10, and 11) and the other as the B PORT (pins 13, 14, 15, and 16). Note that each read bus is four data bits wide.

Associated with each read port is an address input. Valid data appears at the A PORT output for the location addressed by the A PORT address input (pins 6, 5, and 4). A unique feature of this memory is that another location can be simultaneously addressed by presenting this second address to the B PORT address output. The read enable input (pin 7 for A and pin 17 for B) is tied low, enabling read data from either port.

Although data can be read from both ports, it can be written only through one port, the A PORT. This is done by presenting the desired address to the A PORT ADDRESS INPUT while simultaneously presenting data to the A PORT WRITE DATA INPUT (pins 3, 2, 22, and 21). The necessary timing is supplied through pins 1 and 23.
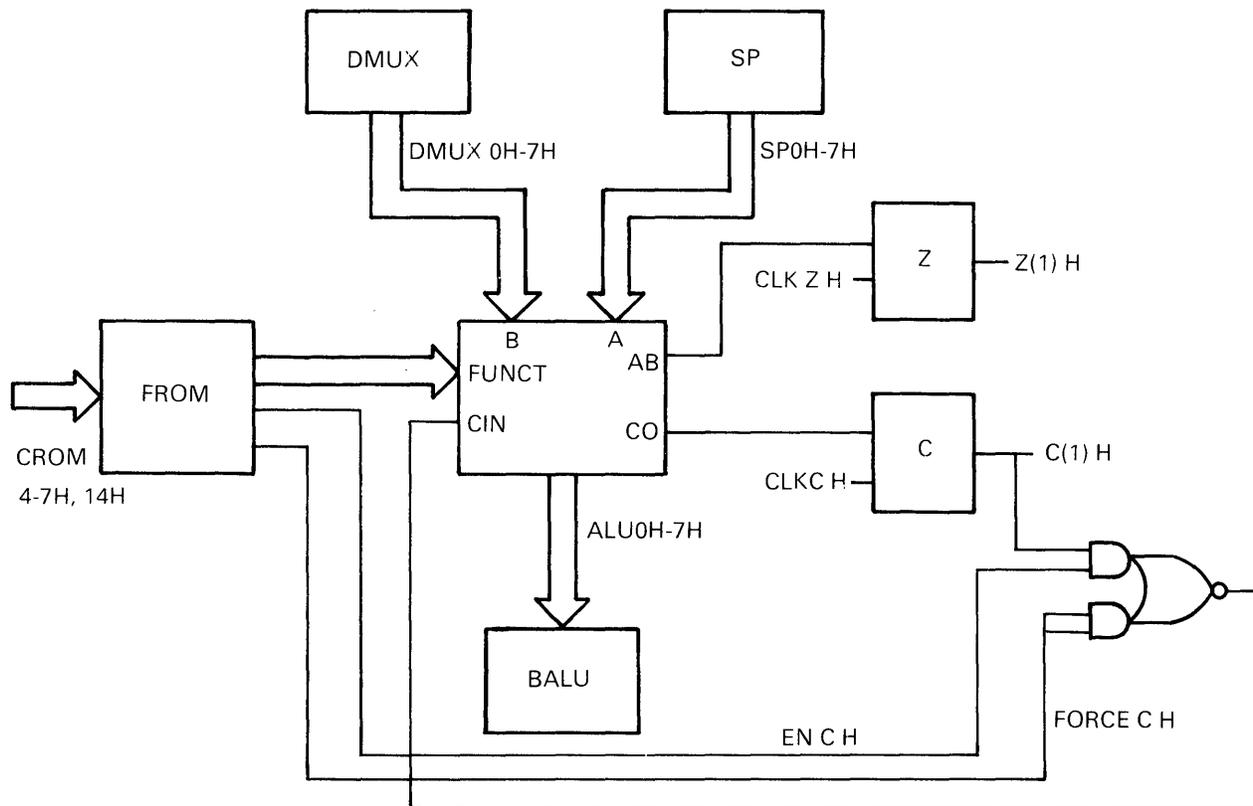
Figure 4-11   ALU and Associated Logic
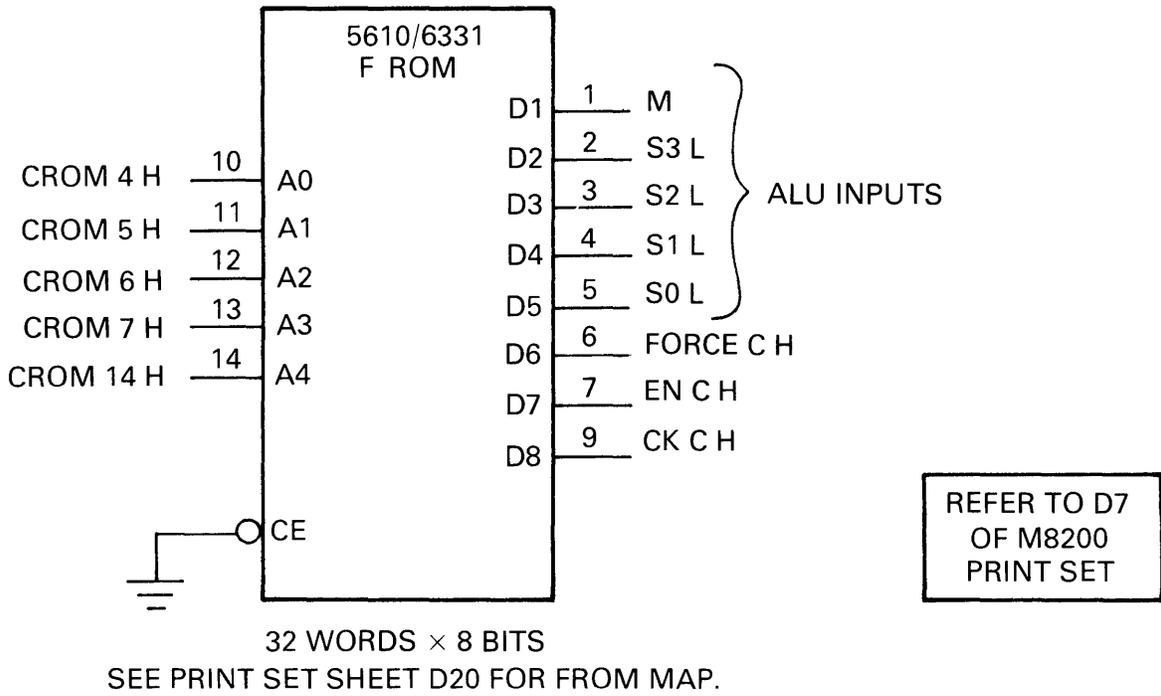
MK-0797

MK-0798

Figure 4-12   Configuration of FROM
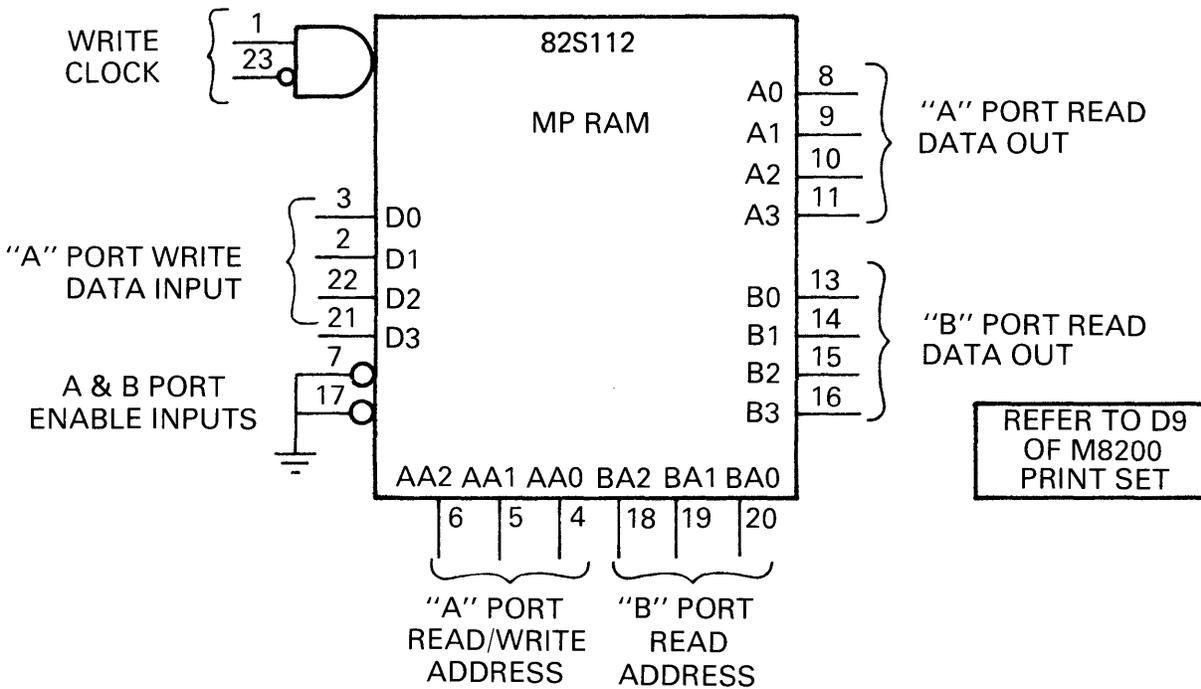
MK-0799

Figure 4-13   Multiport RAM

4-21
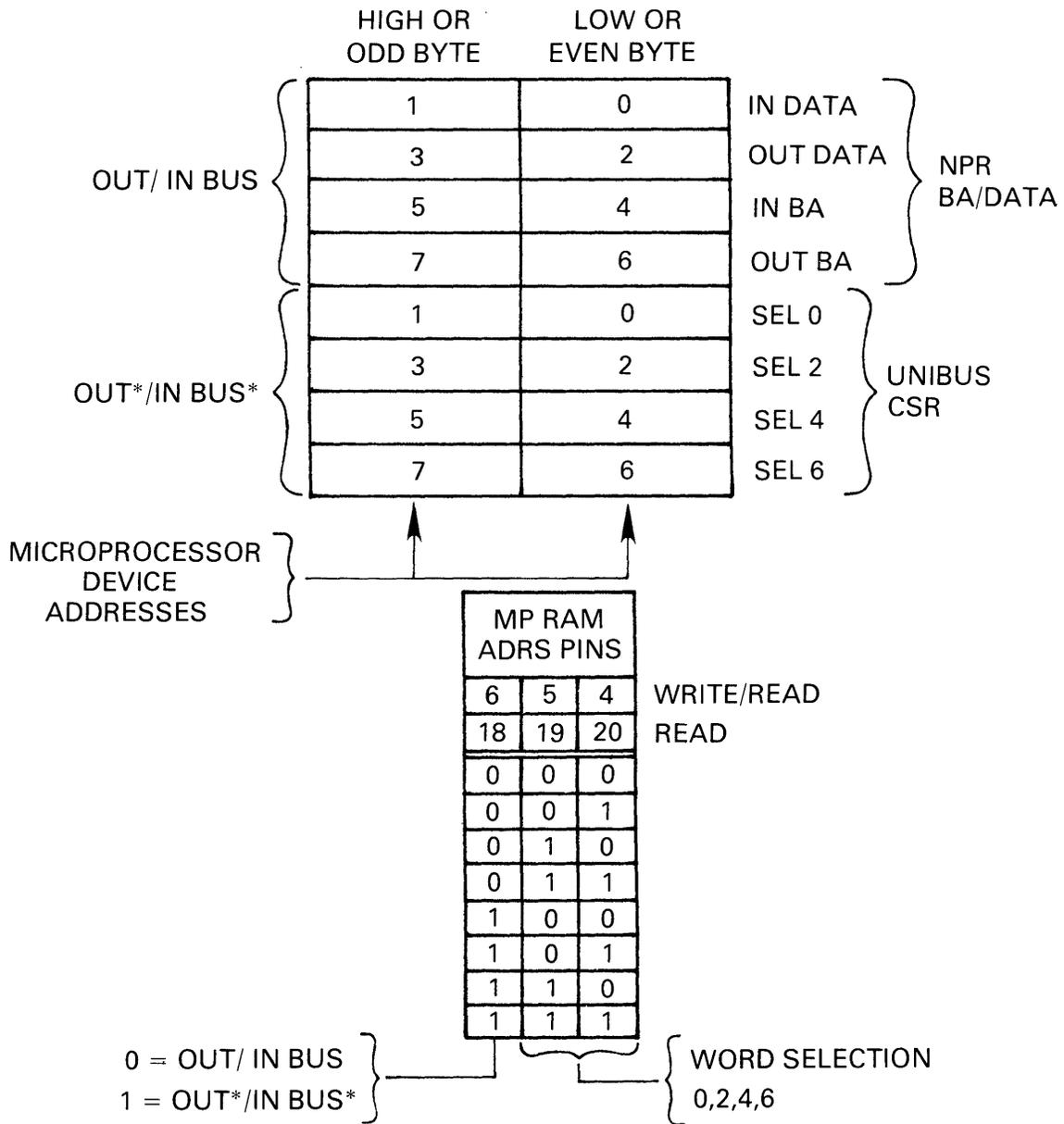
Figure 4-14   Multiport RAM Addresses

MK-0800

The multiport RAM address assignments are shown in Figure 4-14. Note that the memory is divided into two blocks, one block in four words associated with the OUT/IBUS registers and the other with OUT*/IBUS* registers. Stored in the memory as OUT/IBUS register addresses are both data and addresses of the data for NPR transfers with the PDP-11 memory. These multiport RAM memory locations are applicable during NPR cycles. Additionally, the OUT*/IBUS* register addresses shown are the UNIBUS CSRs as addressed from either the microprocessor or the UNIBUS.

The block diagram in Figure 4-15 illustrates the relative position of the multiport RAM within the microprocessor architecture. Shown are the three output loads, the two data input sources, and the addressing schemes.

The B PORT output data bus feeds both the UNIBUS address bus drivers and the DMUX. However, because the DMUX is only eight bits wide and the RAM output is sixteen bits, the RAM output is fed to the DMUX on two separate inputs.

When the microprocessor executes NPR cycles, the bus address will be fetched from the RAM through the B PORT and clocked into the bus drivers by NPR MASTER. The two RAM locations where the bus address is stored is defined by the B PORT address multiplexer with MP READ CYCLE low. This results in addressing either location two or three, as determined by OUT NPR. On an OUT NPR, data comes from the A PORT of the RAM through a multiplexer and onto the UNIBUS.

The remaining input to the B PORT address multiplexer becomes active during a particular Move microinstruction (X)1) and in turn gates the addressed data either to the high byte or to the low byte input on the DMUX. Bits 5, 6, and 15 determine the RAM address. Bit 15 determines which group is to be addressed, the IBUS or IBUS* registers. The location within the selected group is addressed by bits 5 and 6. The appropriate byte is selected by the DMUX.

With the A PORT, both reading and writing must be considered. The A PORT output bus feeds a 2-to-1 multiplexer which feeds the UNIBUS data bus drivers. Data is written into the RAM through another 2-to-1 multiplexer which selects either the UNIBUS data receivers or the ALU output as the data to be written.

There are three conditions under which data is written into the multiport RAM: (1) an input NPR cycle, (2) loading a CSR by the PDP-11, and (3) writing by the microprocessor. MP WRITE CYCLE is asserted when the microprocessor executes a write cycle. This condition then selects the ALU output to be written into the RAM (as illustrated in Figure 4-15). On the other hand, the UNIBUS data receivers are selected as the RAM input data for both NPR cycles and CSR loading.

A full word from the UNIBUS or one byte at a time from the microprocessor can be written into the multiport RAM. This is controlled by HB WRITE L and LB WRITE L. When writing the ALU output, the 8-bit byte can be written into either the high or low byte position. Bit zero of the microinstruction (CROM0) determines the byte position. During NPR cycles, full words are always written into the RAM. When writing into a CSR, the PDP-11 instruction determines the write control condition with C0 and A0.

The A PORT addressing is determined through two levels of multiplexing (see Figure 4-15). CROM bits 1 and 2 determine addressing with the first multiplexer when the microprocessor writes into the RAM. The second input to this multiplexer is an output of another multiplexer under the control of NPR MASTER. During the execution of NPR cycles, one of two fixed locations (location 0 or 1) is always addressed. Which location is addressed is a function of desired data transfer direction. CSR addressing is determined by the UNIBUS address bits A01 and A02, and always references the four high RAM addresses.
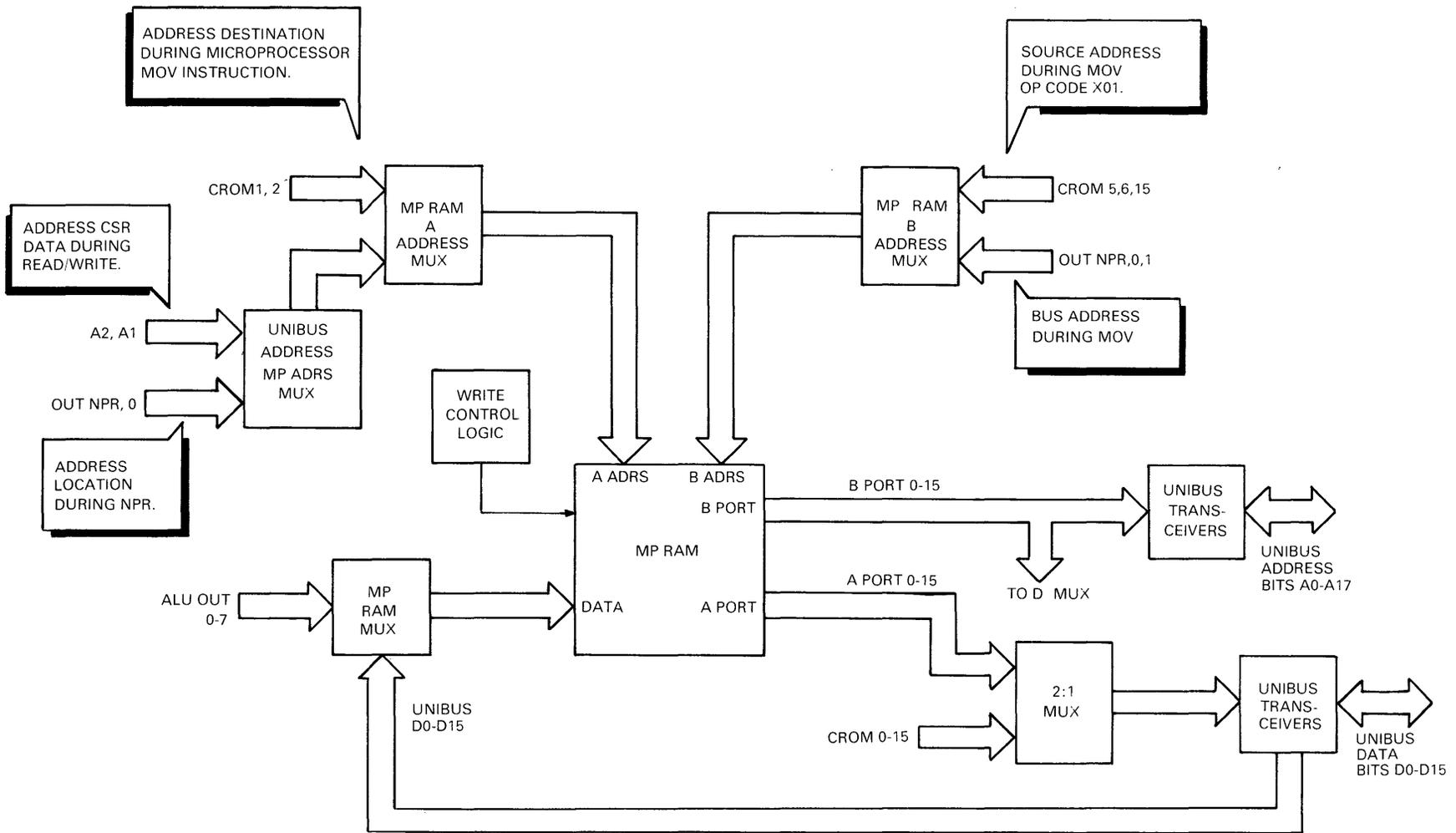
MK 0801

Figure 4-15   Block Diagram of Multiport RAM and Associated Logic

4.2.11 INBUS/OUTBUS and INBUS*/OUTBUS* Registers

The UNIBUS Control and Status Registers are physically located in the multiport RAM. The RAM capacity is 128 bits arranged as sixteen 8-bit bytes, which is equivalent to eight 16-bit words.

There are two additional byte-sized hardware registers that are listed in the OUTBUS*/INBUS* category. They are the NPR Control Register (10_8) and the Microprocessor Miscellaneous Register (11_8). The microprocessor has the capability of addressing 32 byte-sized registers. As a convention, it has been decided to show 16 assigned under each category, that is, OUTBUS*/INBUS* registers (Figure 4-16) and OUTBUS/INBUS registers (Figure 4-17). As a result, six undefined registers 12-17 (octal) are listed under OUTBUS*/INBUS*. These registers do not exist physically. The line unit device registers, 10_8-17_8 have been added to the OUTBUS/INBUS register category. These registers are physically located in the line unit. Address 10_8 is listed twice because two line unit registers use the same address. The In Data Silo is read only and the Out Data Silo is write only. Therefore, there are nine registers in the line unit.

DMC11 REGISTER DESIGNATION	BITS									
	7	6	5	4	3	2	1	0		
INCON	BYTE 0								0	
MAIN	BYTE 1								1	
OCON	BYTE 2								2	
	BYTE 3								3	UNIBUS CSRS AS VIEWED FROM MICROPROCESSOR.
PORT1	BYTE 4								4	
PORT2	BYTE 5								5	
PORT3	BYTE 6								6	
PORT4	BYTE 7								7	
NPR	BYTE XFER			OUT NPR	IN BA 17	IN BA 16	R/W	NPR RQ	10	NPR CONT
UBBR	BUS RQ	VECT-OR		PGM CLK	OUT BA17	OUT BA16	AC LO	NON EX	11	μP MISC
	XX4							MEM		
									12	UNASSIGNED. ADDRESSABLE BUT NOT PHYSICALLY PRESENT.
									13	
									14	
									15	
									16	
									17	

MK-0802

Figure 4-16   OUTBUS*/INBUS* Assigned Addresses

DMC11 REGISTER DESIGNATION / BITS

Designation	7	6	5	4	3	2	1	0	Addr	
INDAT1	IN DATA LB								0	
INDAT2	IN DATA HB								1	
ODAT1	OUT DATA LB								2	
ODAT2	OUT DATA HB								3	
IBA1	IN BA7:0								4	
IBA2	IN BA 15:8								5	
OBA1	OUT BA 7:0								6	
OBA2	OUT BA 15:8								7	
RCVDAT	IN DATA SILO								10	
TMTCON	OUT CLR	OUT ACT	SW	OUT RDY			TEOM	TSOM	11	OUT CONT
TMTDAT	OUT DATA SILO								10	
RCVCON	IN CLR	IN ACT	LU LOOP	IN RDY			BLK END	BCC MATCH	12	IN CONT
MODEM	RING	DTR	RS	HD	MOD RDY	CS	SW	SW	13	MODEM CONT
SYNC	SYNC CHAR/SECONDARY ADRS								14	
LINDSW	PASSWORD (SW PACK #2)								15	
BM873	BOOT-OFFSET (SW PACK #3)								16	
	QO	QI	SI	OCOR	ICIR		LU CLK	DDCMP MODE	17	MAINT

LINE UNIT REGISTERS (addresses 11–17)

MK-0803

Figure 4-17   OUTBUS/INBUS Assigned Addresses

The physical arrangement of OUTBUS*/INBUS* registers and OUTBUS/INBUS registers is shown in Figure 4-18.

The detailed discussion of the Line Unit CSRs is contained in the *DMC11 IPL Synchronous Line Unit Maintenance Manual* (EK-DMCLU-MM-002).

4.2.11.1   NPR Control Register 10 – Refer to Figure 4-16. NPR Control bit descriptions are provided in Table 4-1.

4.2.11.2 Microprocessor Miscellaneous Register 11 – Refer to Figure 4-16. Miscellaneous register bit descriptions are provided in Table 4-2.

4.2.11.3 OUTBUS/INBUS Assigned Addresses – Refer to Figure 4-17. Register byte descriptions of the OUTBUS/INBUS registers is provided in Table 4-3.
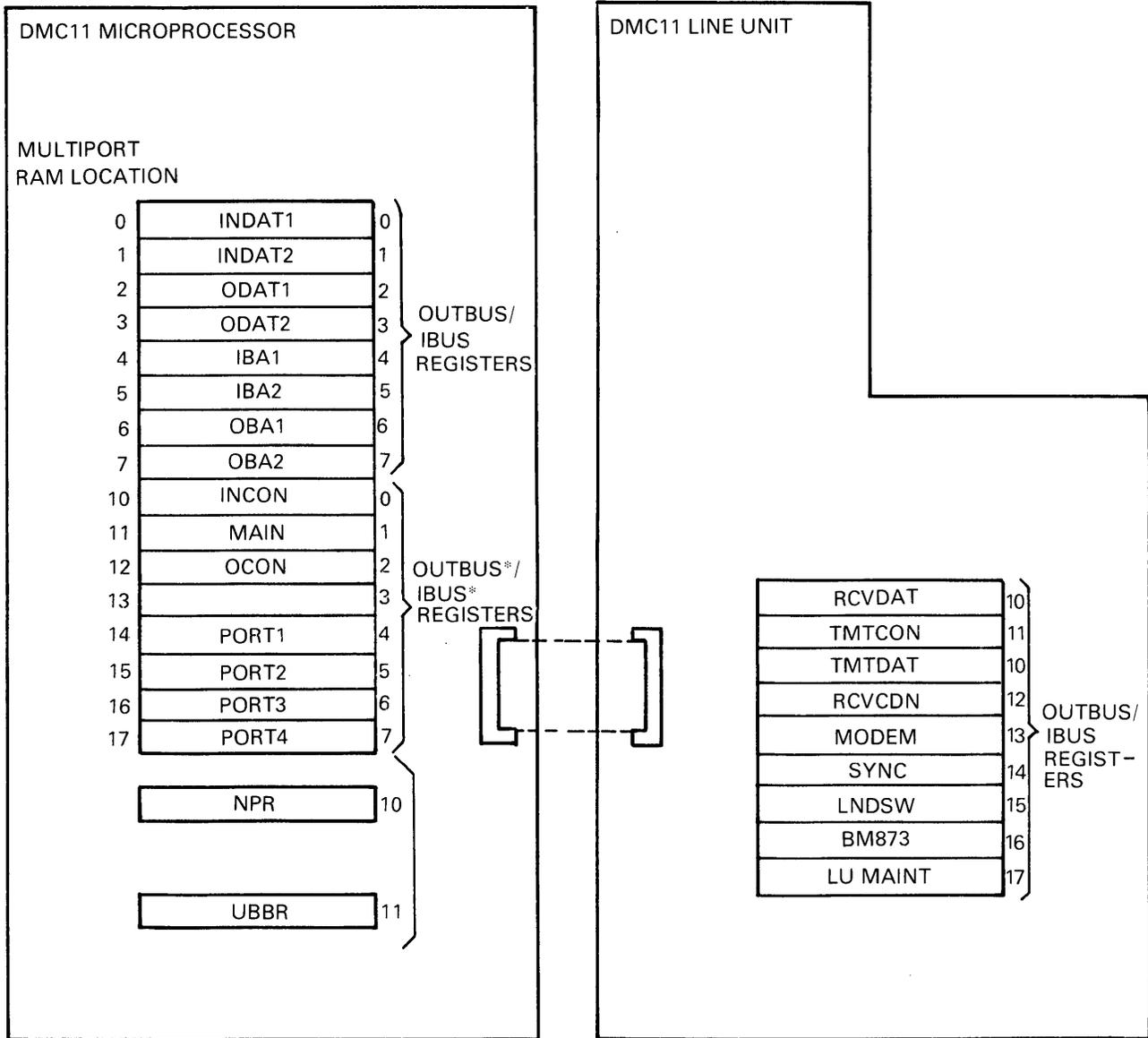
Figure 4-18   Physical Arrangement of Registers

MK-0804

Table 4-1   NPR Control Register (OUTBUS*/INBUS*
Register Group) REG 10 Bit Description

Bit	Name	Description
0	NPR REQUEST (NPR RQ) (R/W)	This bit can be set only by the microprogram. It initiates an NPR cycle for data transfers (bidirectional) between the microprocessor and memory. This bit is used in conjunction with OUT NPR (bit 4) and BYTE TRANSFER (bit 7) to determine the direction of the data transfer and whether a word or byte is to be transferred to memory. It is automatically clocked clear by D15 NPR DONE H when the NPR has been completed. Bit 7 (BYTE XFER) controls word/byte selection.

The data for NPR/DATA IN is loaded into OUTBUS/INBUS Registers 0 and/or 1. The data for NPR/DATA OUT is read from OUTBUS/INBUS Registers 2 and/or 3.

When BYTE XFER is set, the state of the BA least significant bit (0) is used to select the byte. The truth table for the type of transaction, as selected by these bits, is shown below.

(C1)	(C0)	BA0	UNIBUS TRANSACTION
0	0	0	DATI
0	0	1	DATI
0	1	0	Illegal
0	1	1	Illegal
1	0	0	DATO
1	0	1	DATO
1	1	0	DATOB (Low Byte)
1	1	1	DATOB (High Byte)

Table 4-1 NPR Control Register (OUTBUS*/INBUS*
Register Group) REG 10 Bit Descriptions (Cont)

Bit	Name	Description
1	READ/WRITE (R/W)	This read/write bit provides no function and may be treated in the microcode as a flag or state indicator.
2,3	IN BA 16 and IN BA (R/W)	These are the PDP-11 memory extension 17 bits used during an IN NPR (C1 = 0) transaction (DMA transfer from memory to the microprocessor).
4	OUT NPR (R/W)	This bit is used in association with NPR RQ (bit 0). It controls the direction of DMA data between the microprocessor and memory. When set, data direction is from the microprocessor to memory. The details of the inter-relationship between these bits are covered in the description of NPR RQ (bit 0).
5,6	RESERVED	Non-existent bits, always read as 0.
7	BYTE XFER (C0)(R/W)	This bit is used in association with OUT NPR to indicate a byte transfer to the PDP-11 memory. When this bit is set, the PDP-11 uses address bit A0 for byte selection. If A0 is a 0, OUT DATA <7:0> is stored in the low byte of the PDP-11 memory. If A0 is a 1, OUT DATA <15:8> is stored in the high byte of the PDP-11 memory. If BYTE is clear during an OUT NPR operation, OUT DATA <15-0> is transferred to the PDP-11 memory as a word.

Table 4-2 Miscellaneous Register (REG II)
(OUTBUS*/INBUS* Register Group)
Bit Descriptions

Bit	Name	Description
0	NON-EX MEM (R/W)	During an NPR, this bit is set approximately 20μs after a non-existent memory location is addressed by the microprocessor with no slave SYNC response. At this time, the NPR logic releases the UNIBUS. This is an error condition, indicating: • Incorrect address provided by software • Memory failure • Address Logic failure • UNIBUS failure
1	AC LOW (R/W)	Set by the microprogram to initiate a power fail sequence at the main CPU. This bit clears automatically upon completion of the sequence.
2,3	OUT BA 16 and OUT BA 17 (R/W)	These are the PDP-11 memory extension bits used during an OUT NPR transfer; DMA transfer from the microprocessor to memory.

Bit	Name	Description
4	PGM CLK R/W	This bit acts as a timer for the microprocessor. It can be read to determine lapse time for time out, flag testing, etc. When written, it starts a one- second retriggerable one-shot.
		When read, it indicates 0 output of the retriggerable 1-shot with a one-second pulse.
		As long as the bit is written to a 1 at less than one second intervals, the 1-shot remains asserted and this bit is read as a 0. If the 1-shot times out, this bit is read as a 1.
		The program clock causes no hardware action. Its use is totally dependent upon microprogram implementation.
5	RESERVED	Nonexistent bit, always read as 0.
6	VECTOR AT XX4 (R/W)	If this bit is set when BR RQ (bit 7) is set, vector address XX4 is generated. If it is cleared when BR RQ is set, vector address XX0 is generated. Address XX0 is associated with RDI and address XX4 is associated with RDO.
7	BUS RQ (R/W)	When set, this bit initiates a Bus Request via the UNIBUS at BR level 4, 5, 6, or 7. The microprocessor is shipped with a BR5 priority plug installed. This bit can only be set and is clocked clear by the hardware after the BR has been completed by signal D16 BR DONE H. This bit is also cleared by BUS INIT, but not by MCLR (bit 14 of SEL 0).

Table 4-3   OUTBUS/INBUS Registers Byte Descriptions

Register	Name	Description
0, 1	IN DATA	Low byte (register 0) and high byte (register 1) of NPR data to be transferred from the PDP-11 memory.
2, 3	OUT DATA	Low byte (register 2) and high byte (register 3) of NPR data to be transferred to the PDP-11 memory.
4, 5	IN BA	Contains BUS Address (BA) bits 0–15 during an NPR transfer from the PDP-11 memory. Bit 0 of register 4 is BA bit 0 and bit 7 of register 5 is BA bit 15.
6, 7	OUT BA	Contains Bus Address (BA) bits 0–15 during an NPR transfer to the PDP-11 memory. Bit 0 of register 6 is BA bit 0 and bit 7 of register 7 is BA bit 15.

4.2.12 Maintenance CSR (BSEL 1)

Refer to Figure 16. A number of maintenance features are available for the DMC11 through the use of the MAINTENANCE CSR. The MAINTENANCE CSR address is 76XXX1 and can be referenced via a word or byte transfer. With this feature, the PDP-11 diagnostic program can read the contents of the CROM, write into the MAINTENANCE INSTRUCTION register (thereby substituting the CROM microword), step either or both the microprocessor and the line unit, and loop transmitted data through the line unit back to the microprocessor for verification.

15	14	13	12	11	10	9	8	DATA BITS
RUN	MCLR	////	STEP LU	LU LOOP	ROM O	ROM I	STEP µ P	BSEL 1
7	6	5	4	3	2	1	0	DATA BITS AS VIEWED FROM THE MICRO-

MK-0811   PROCESSOR.
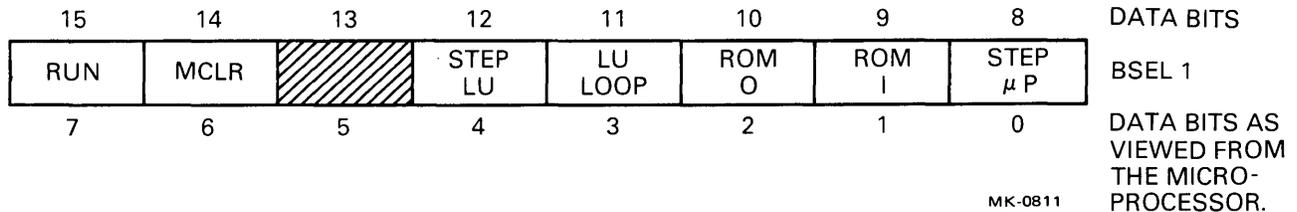
The MAINTENANCE CSR byte format is illustrated above with the logic shown on drawing D17 of the M8200 *Print Set*. Five of the bits are stored in the microprocessor each time the MAINTENANCE CSR byte is written from the PDP-11. D09–D12 are stored in a 74174, while D15 is stored in a 74S74 on the leading edge of LD BSEL 01L (provided the BYTE SEL 01 LOCK OUT switch is off). This switch must be off to enable all diagnostic features. When on, the RUN INHIBIT switch prevents the RUN flop from setting. This switch must be off to enable the microprocessor to enter RUN mode. The two remaining bits D14 and D08 pulse the microprocessor when written as a 1 by the PDP-11.

> **NOTE**
> All eight bits of BSEL 1 are written to the multiport RAM, as well as the five internal flip-flops. A read of BSEL 1 always gives the contents of the MP RAM, and may not be representative of the internal flip-flops. For example, if BSEL 1 Lockout Switch is ON, and the RUN INHIBIT Switch is ON, the PDP-11 moves all ones to BSEL 1; examination of BSEL 1 reads as all 1s, yet the internal flip-flops have not been set.

4.2.12.1 Step LU H – This signal, a function of bit 12, feeds directly to the line unit interface controlling the stepping of the line unit. When set, it clocks the line unit transmitter and when it is cleared it clocks the line unit receiver (completes 1-bit time).

4.2.12.2 LU Loop H – This signal, a function of bit 11, feeds directly to the line unit enabling the internal loopback feature. With this feature, the diagnostic program can transmit known data which the line unit then sends back to the microprocessor as received data. The program then performs a comparison on transmitted data and received data to determine if any errors had occurred.

4.2.12.3 ROM OUT H – Under control of bit 10, the diagnostic program can read the contents of the CROM in order to determine the validity of machine cycling. A combination of the CROM OUT H and A2H (a read of SEL 4 or 6) gate the CROM microword specified by the Program Counter through a multiplexer. The output of the multiplexer is used to drive the UNIBUS data lines. This means that a second instruction, a DATI with an address of XXXXX4$_8$, must be executed following the setting of ROM OUT. This enables the multiplexer on print D11 to select the CROM microword and feed it to the UNIBUS data lines.

4-31

4.2.13 Microprocessor Clock

The basic clock consists of six JK flip-flops interconnected as a shift register generating six discrete time intervals. Each time interval is asserted for a period of 60 nsec. However, due to unique clocking, four time intervals overlap resulting in an overall clock period of 300 nsec instead of the expected 360 nsec. Figure 4-19 illustrates the clock sequencing. Note the overlap of T90 with T60 and T240 with T210. These clock signals are distributed throughout the microprocessor to clock registers and provide system timing.

A 33.33 Mhz oscillator generates the timing used to clock the shift register. However, before being applied to the clock inputs of the shift register, the oscillator output (CK) first passes through a control flop (WAIT SYNC) and a divide-by-two flop (SYSTEM CLOCK). (See drawing D14 in the *Print Set.*) The control flop WAIT SYNC stops the clock when the multiport RAM is being accessed and allows the clock to continue only when the multiport RAM becomes available. This clock hold state is in effect with WAIT SYNC in the reset state. But with WAIT SYNC set, SYSTEM CLOCK toggles with each high to low transition on its clock input. Both outputs of SYSTEM CLOCK (Q AND Q) are used as shift register clocks.

```
     T0   T30  T60  T90  T120 T150 T180 T210 T240 T270 T300 T330 T360
      |    |    |    |    |    |    |    |    |    |    |    |    |

T0       ┌──────┐                                      ┌──────┐
         │ 0-60 │                                      │ 0-60 │
         └──────┘                                      └──────┘

T60                ┌────────┐
                   │ 60-120 │
                   └────────┘

T90                  ┌────────┐
                     │ 90-150 │
                     └────────┘

T150                        ┌─────────┐
                            │ 150-210 │
                            └─────────┘

T210                              ┌─────────┐
                                  │ 210-270 │
                                  └─────────┘

T240                                  ┌─────────┐
                                      │ 240-300 │
                                      └─────────┘
```
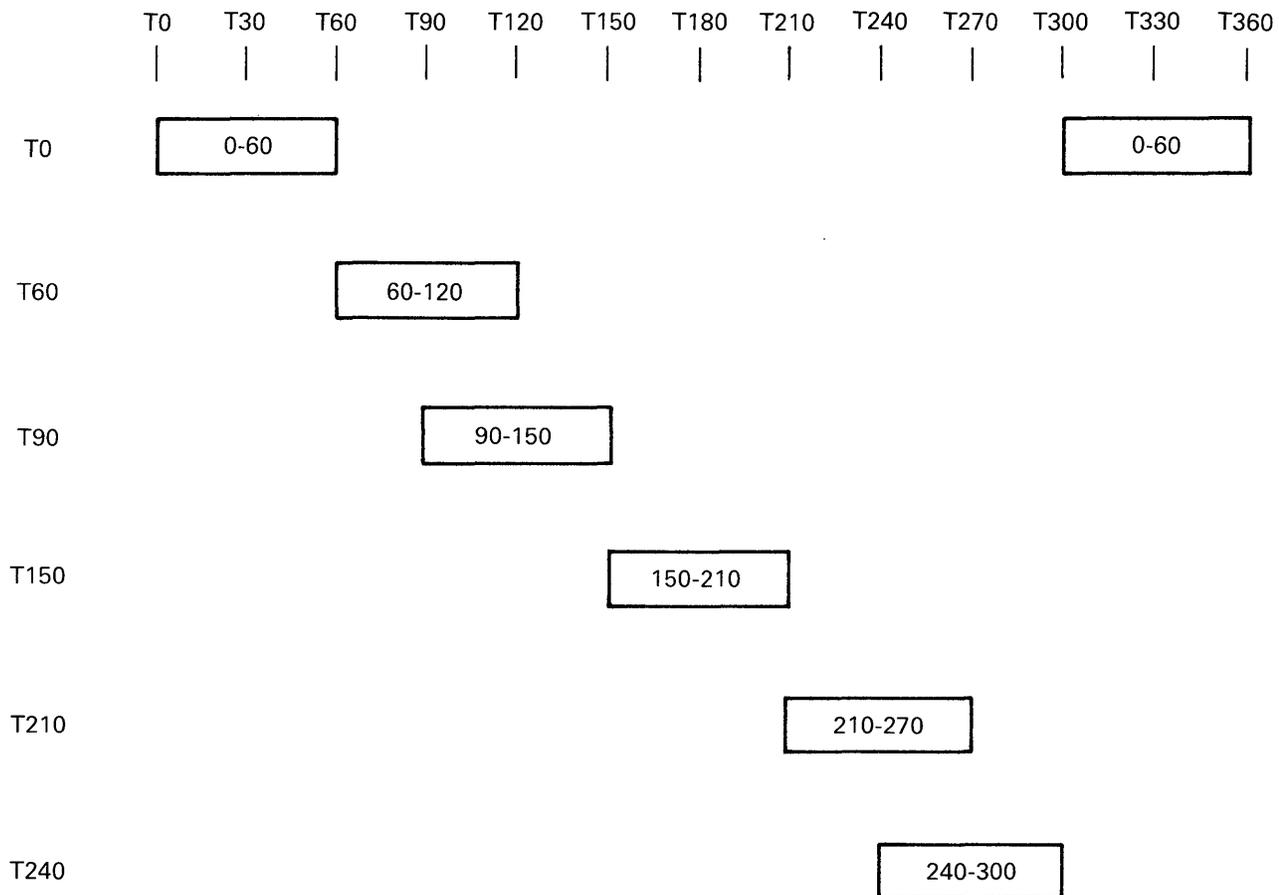
MK-0805

Figure 4-19   Clock Sequence

Refer to drawing D14 for the following logic analysis. Note that the flip-flops T0 through T240 are wired as a right-shifting shift register with T240's output dropping off into the bit bucket. T0's JK inputs are wired to toggle T0 when the four flip-flops T60, T90, T150, and T210 are all reset and RUN SYNC is set. Note that the shift register does not use the same clock source for all positions. T90, T150, and T210 are clocked by the Q output of SYSTEM CLOCK, while T0, T60, and T240 are clocked by SYSTEM CLOCK's Q output. The aforementioned overlap of time intervals is generated by using these two clocks 180° out of phase.

Given the initial conditions of RUN SYNC and WAIT SYNC both set, and the shift register all zeroes, results in a high condition on both the J and K inputs to T0 placing T0 in the toggle mode. The next time SYSTEM CLOCK sets, T0 will set. This point in time is refered to as "time 0" (see Figure 4-20). With T0 set, the set input to T60 is qualified while simultaneously the toggle input to T0 remains asserted. Therefore, on the next SYSTEM CLOCK occurring 60 nsec later, T60 sets and T0 resets. From this point, the clock functions as a shift register. When the bit reaches T240, a new bit is regenerated at the inputs to T0.

MK-0806
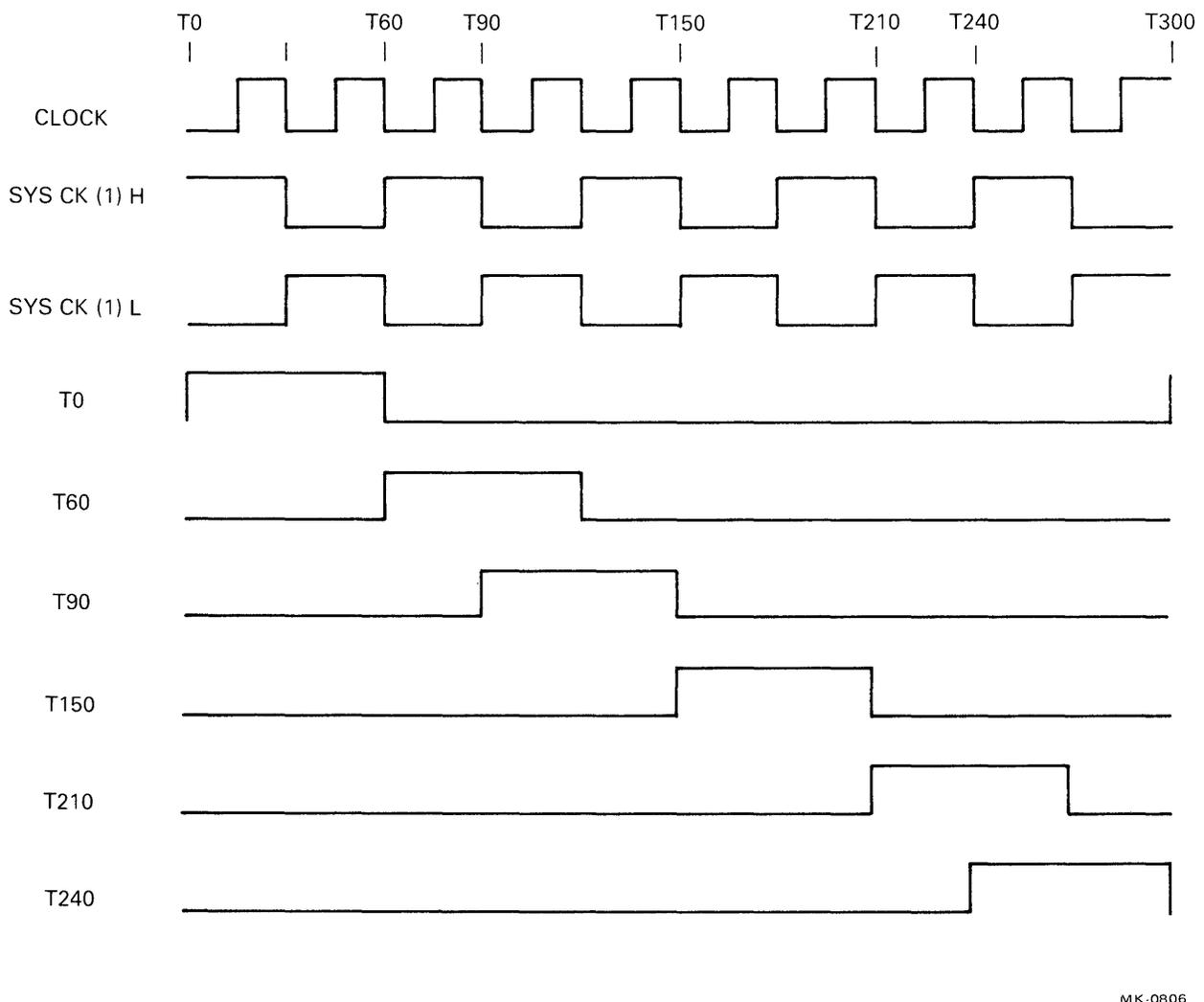
Figure 4-20   System Clock Timing Diagram

4-33

The microprocessor cycling can be halted by stopping the SYSTEM CLOCK, this is done by resetting the RUN flop. When the RUN flop is reset, RUN SYNC allows the clock shift register to complete the current clock cycle and stop with the shift register cleared.

In Step Mode, each STEP MC L pulse sets RUN SYNC, allowing one complete clock cycle (T0 – T240) to occur.

4.2.14 Address Selection Logic

Drawing D16 illustrates the logic used to recognize a DMC11 microprocessor address. The JK flop OSSYN sets upon address recognition. The assigned address is configured with ten switches, each switch associated with a unique address bit. Address bits A3 through A12 are available for configuration, allowing an addressing range of four words within the DMC11 microprocessor.

The logic compares the switch code with the respective address bits using two comparator chips whose outputs are wire OR connected. When the inputs are equal bit for bit, the comparator outputs go high. The remaining high-order address bits, A13–A17, all of which must be true, are ANDed with MSYN to produce a set condition on the inputs to OSSYN. On the next clock (CK) OSSYN sets. BOSSYN is asserted 130 nsec later, acknowledging bus master.

4.2.15 NPR Control Logic

Initiation of an NPR cycle is under complete control of the microprogram. To initiate an NPR cycle, a Move microinstruction referencing the OUTBUS* register is executed, moving bit 0 to Register 10_8. This microinstruction sets NPR RQ. Once NPR RQ sets, the logic then executes the NPR cycle asynchronously with respect to the microprogram.

Figure 4-21 illustrates the timing sequence for an output NPR cycle. The requirements for execution are: (1) a UNIBUS address, (2) data gated to the UNIBUS, (3) a DATO defined via C0 and C1, and (4) assertion of master sync (MSYNC). Drawing D15 contains the relevant logic. The addressed unit (slave) then recognizes its address and interprets the control lines. After gating the data from the UNIBUS, the slave acknowledges receipt of the data by asserting slave sync (SSYN).

Refer to Figure 4-21 and drawing D15 for the following discussion. First, the standard handshake for bus control takes place. The timing begins with the assertion of NPR RQ (1) which in turn generates the bus signal DATA BUS NPR L. The central processor then responds with DATA BUS NPG IN H, provided no other device was already queued up for bus mastership. When BUS NPG IN H does arrive at the microprocessor, it resets BUS NPR L following a delay of 70 nsec. In addition, further propagation of the grant signal to other devices is prevented by the microprocessor. The grant signal also sets selection acknowledge (SACK), acknowledging to the central processor the reception of the grant signal. At this point, the microprocessor becomes the next bus master as soon as the current master relinquishes control. The microprocessor monitors BBSY to determine when to take control.

Once the previous bus master relinquishes the bus and provided the microprocessor is queued up to be next [SACK(1) H], the microprocessor then takes control by asserting BUS BBSY L. Simultaneously, SACK is reset and NPR MASTER is set. The actual data transfer can now take place.

The address is gated to the UNIBUS with NPR MASTER as well as C0 and C1. Data, on the other hand, is gated to the data bus under control of DATA BUS L. These three conditions occur simultaneously during an OUTPUT NPR cycle. On the leading edge of NPR MASTER, a 150 nsec delay is triggered, at the conclusion of which BUS MSYN is asserted. The slave gates in the data off the UNIBUS and responds with SSYN, indicating acceptance of the data.
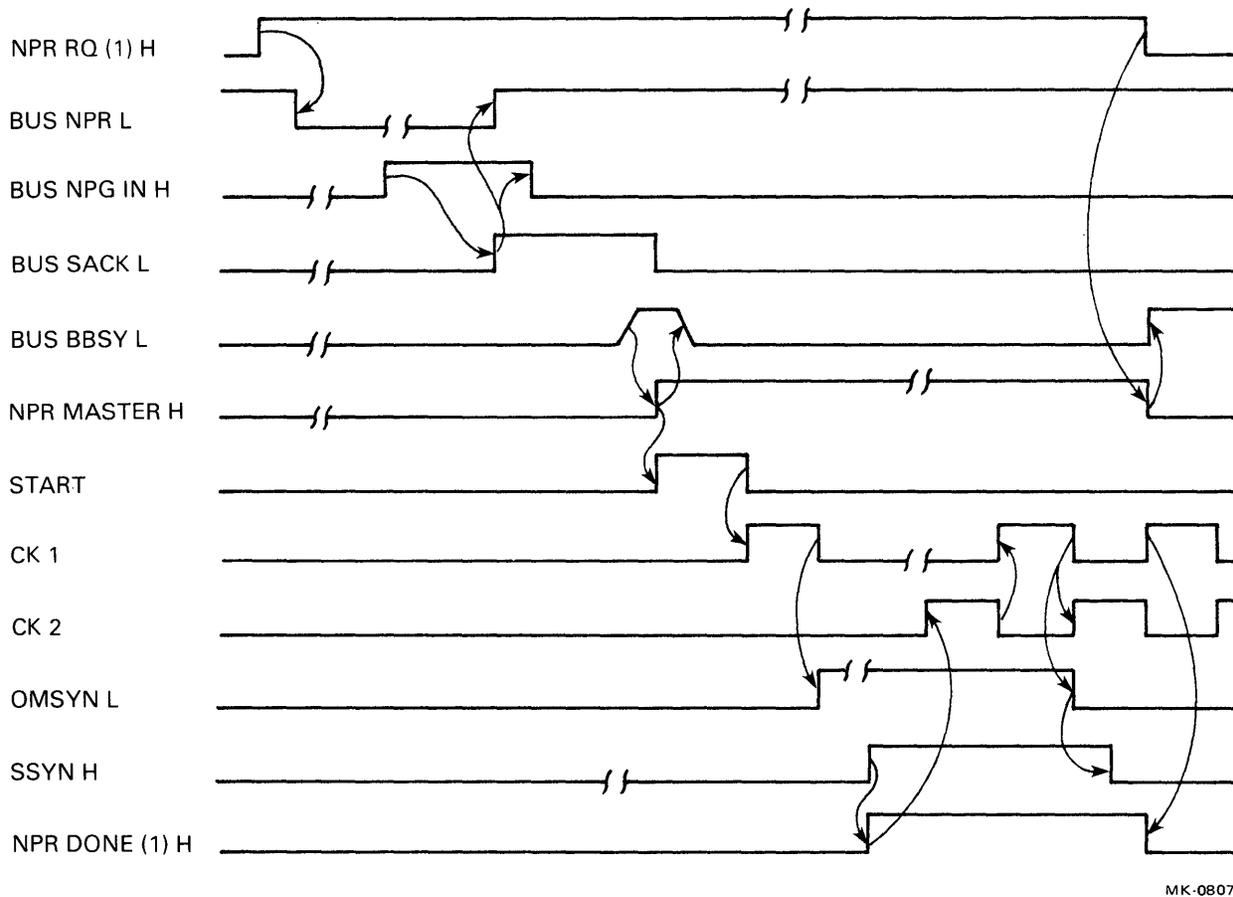
Figure 4-21 NPR Output Timing Diagram

INPUT NPR cycle timing illustrated in Figure 4-22 is, for the most part, similar to the OUTPUT NPR cycle. In this case, the microprocessor waits for the addressed slave to respond with data and BUS SSYN. The microprocessor then loads the data into the multiport RAM and acknowledges receipt by dropping BUS MSYN and subsequently terminating the NPR cycle.

4.2.16 Interrupt Control Logic
Execution of an interrupt cycle is accomplished through a two-phase operation. First, bus mastership must be gained and then the actual INTERRUPT cycle is executed.

Figure 4-23 illustrates the timing sequence for execution of an INTERRUPT cycle. The entire process is initiated with the assertion of BR RQ in the Microprocessor Miscellaneous Register. A Move micro-instruction having an output address of 11_8, with bit 7 of the operand equal to a 1, sets BR RQ.

With both BR MASTER and SACK still reset, the condition is satisfied to generate BUS BR L. BUS BR L feeds the priority plug which in turn generates the appropriate bus request signal to the central processor. The interrupt logic then stalls, awaiting the bus grant signal from the PDP-11 processor. When bus grant arrives (BUS BG IN), it sets SACK and resets BUS BR L. At this point, the micro-processor becomes the next bus master after the current bus master relinquishes bus control. When this happens, BR MASTER (1) H sets, beginning the INTERRUPT cycle. BUS INTR L is asserted while the microprocessor logic simultaneously places the interrupt vector address onto the data bus. The operation is concluded when the central processor acknowledges receipt of the interrupt with BUS SSYN.

4-35
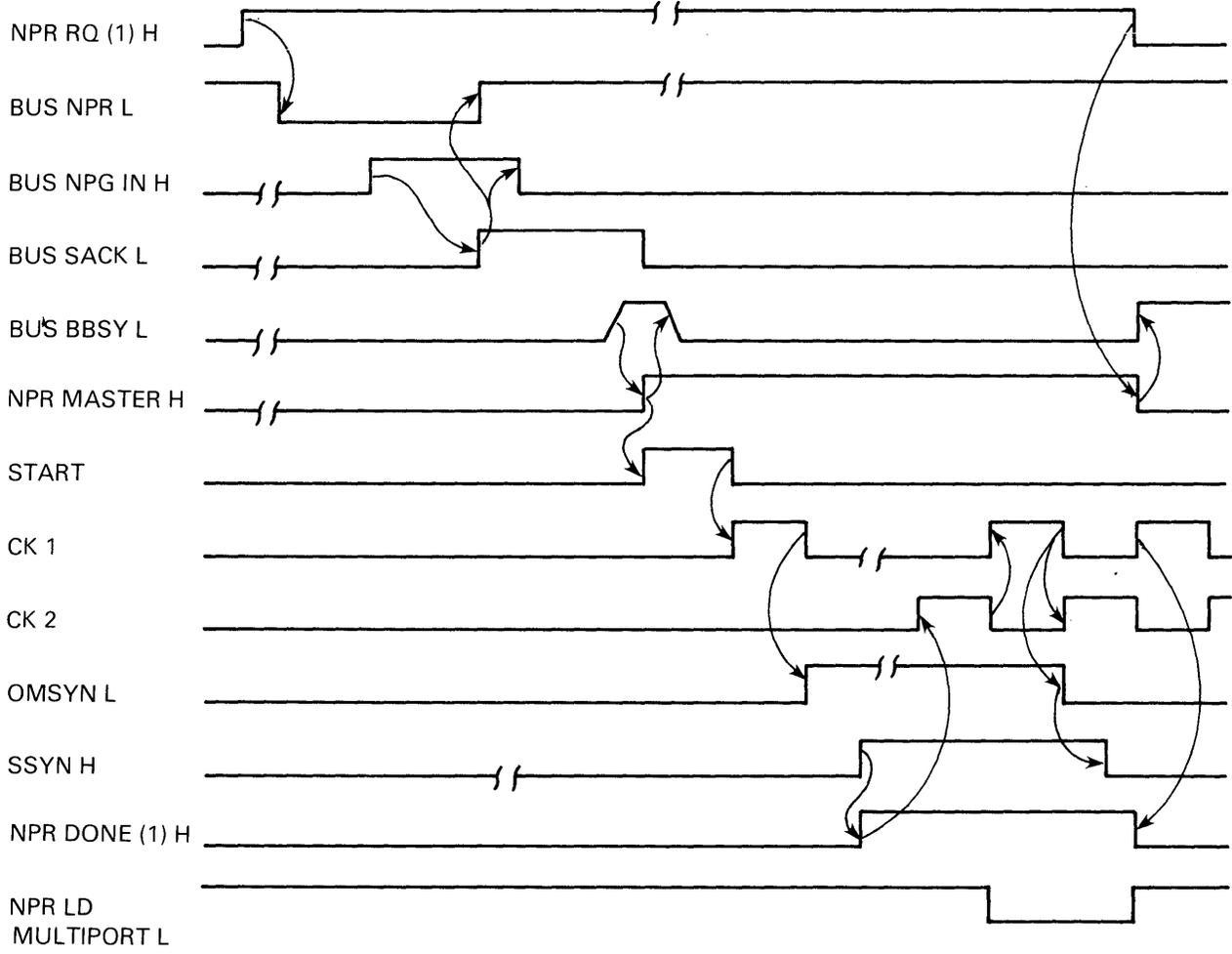
Figure 4-22 NPR Input Timing Diagram

BR RQ H

BUS BR L

BG IN H

BUS SACK L

BUS BSSY L

BR MASTER (1) H

BUS INTR L

BUS VECTOR ADRS

SSYN H

BR DONE H
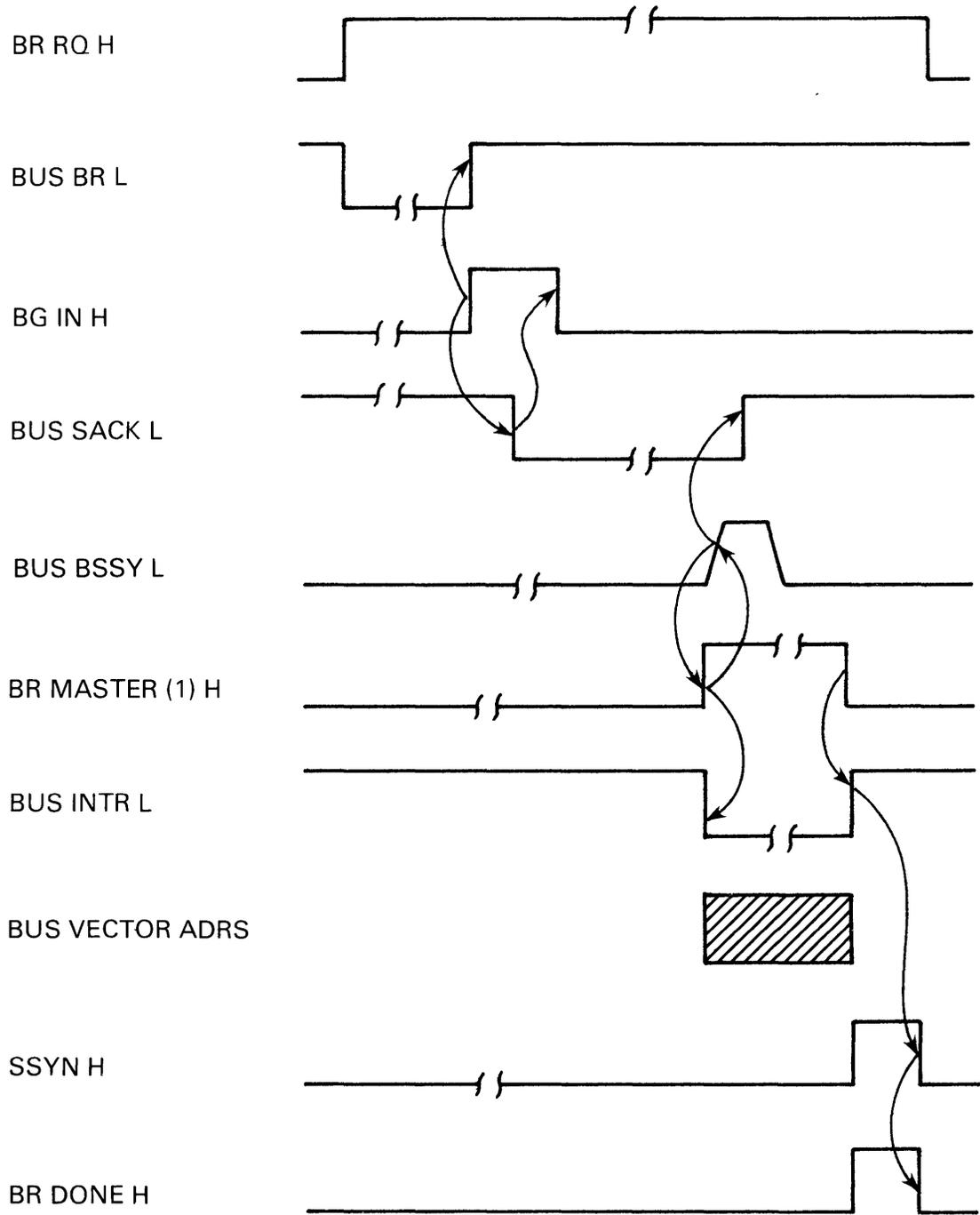
MK-0809

Figure 4-23   Interrupt Timing Diagram

4.2.17 Line Unit Interface
Interconnection between the microprocessor and the line unit is accomplished via the line unit interface. The interface cable carries 33 signal lines between the two units, of which eight originate in the line unit and the remaining 25 in the microprocessor.

4.2.17.1 LU IBUS 0 H – LU IBUS 7 H – These eight lines are the line unit input bus. This bus originates in the line unit and delivers data to the microprocessor from the register addressed by the microword (CROM 0–CROM 3).

4.2.17.2 BALU0L – BALU7L – These eight lines are the microprocessor output bus. The data goes to the buffered ALU register and then to the interface on to the line unit.

4.2.17.3 IBR L/IBR*H – This signal acknowledges to the line unit receipt of data, and is asserted during T240.

4.2.17.4 BT240 – BT240 is used to synchronize the line unit with the microprocessor (not used by DMC11 line units M8201, M8202 - YA/YD).

4.2.17.4 OBW L – This signal is the output data strobe. The line unit uses this signal to clock or strobe the output data into an internal register (not used by DMC11 line units M8201, M8202-YA/YD).

4.2.17.5 OUT * L – When asserted low, this signal indicates to the line unit that the destination of data for the current microinstruction is a register in the OUT* group. The line unit registers are in the INBUS/OUTBUS group; therefore the line unit register address decoder is disabled by D3 OUT*L.

4.2.17.6 CROM 0 L – CROM 7 L – These CROM bits are the input/output address used by the line unit to address internal registers. The output registers are addressed by CROM 0–3 and the input registers with bits CROM 4–7.

4.2.17.7 Clear – This signal initializes the line unit, placing it in a reset state.

4.2.17.8 LU Loop – With this diagnostic function, the line unit loops data from its transmitter to its receiver.

4.2.17.9 Step LU – This signal commands the line unit to shift data by 1 bit per cycle of the STEP LU line.

4.2.18 Typical System Timing
Typical system timing is illustrated in Figures 4-24 and 4-25. Figure 4-24 shows applicable signals used in an output cycle along with typical line unit logic. Note that the address is valid from T90 through T300 while the data for the cycle in question is valid from approximately T270 through the next T240. The data is strobed into an internal register with the low-to-high transition of OBW L.

Input bus timing is illustrated in Figure 4-25. Again, the address is valid for the same period as in the output cycle (T90–T300). The line unit then places data onto the input bus during its T5 time, which approximately coincides with T160–T240 in the microprocessor. The microprocessor acknowledges receipt of the line unit data by asserting IBR during T240–T300.

4-38
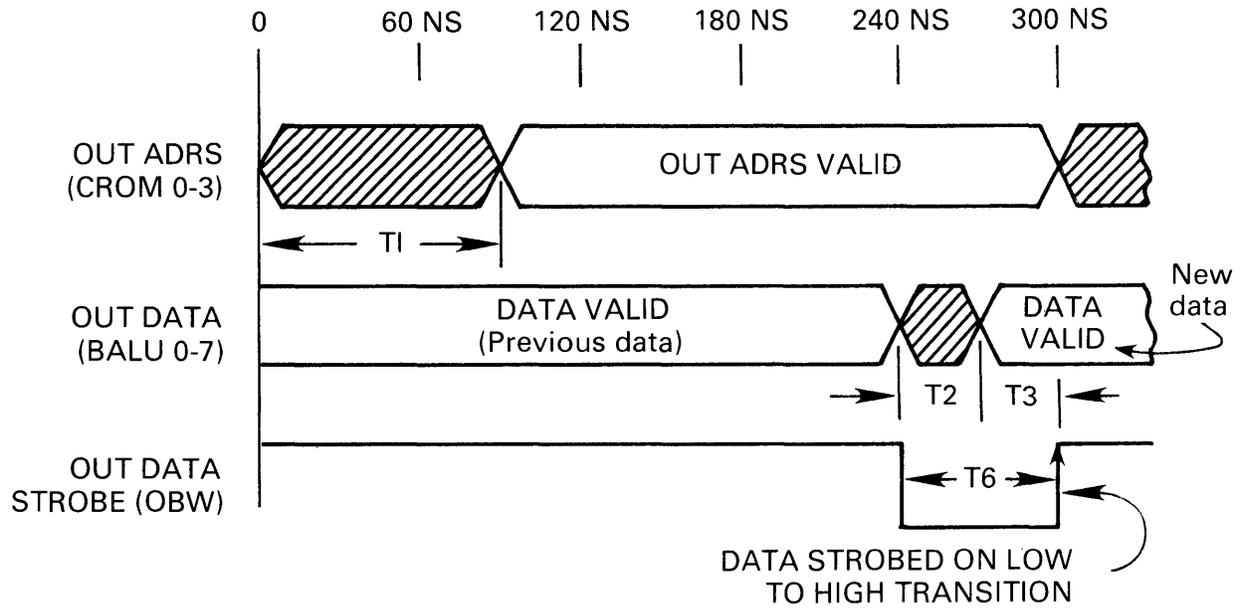
Figure 4-24 Typical Output Bus Timing
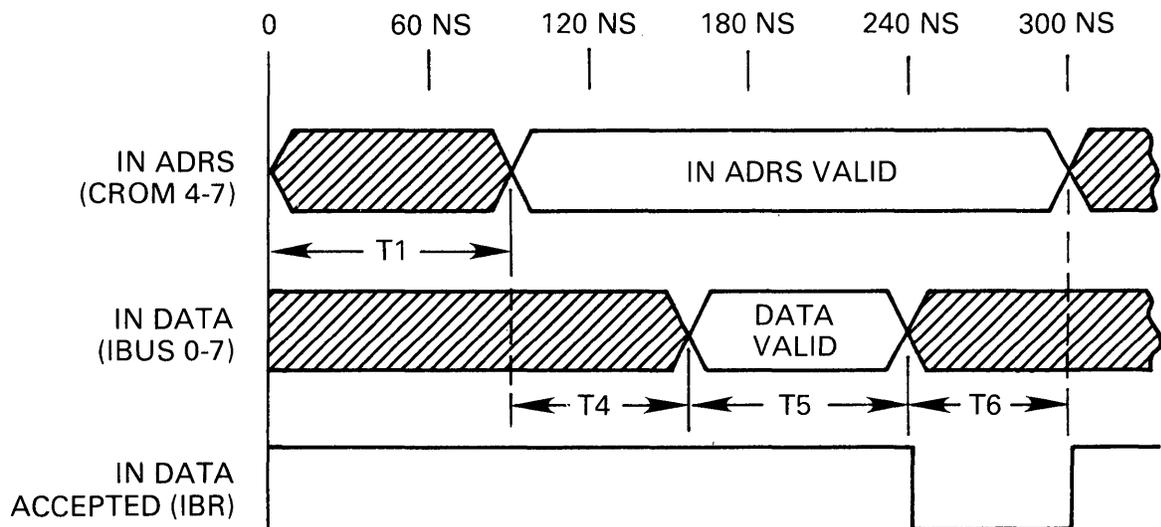
Figure 4-25 Typical Input Bus Timing

5.1 SCOPE

Servicing the DMC11 is based on the maintenance functions contained in the CSRs and the maintenance philosophy established for this product. This chapter covers the maintenance modes, preventive and corrective maintenance, and includes the DMC11 diagnostics.

5.2 MAINTENANCE FUNCTIONS/MAINTENANCE MODES

The maintenance functions are available to the DMC11 via the maintenance CSR (BSEL 1). Maintenance and system tests constitute the maintenance modes.

5.2.1 Maintenance Register (BSEL 1)

This register contains the high byte of address 76XXX0. A brief description of the CSR byte is provided in Chapters 3 and 4. The byte format and bit descriptions are provided in detail in this section.

15	14	13	12	11	10	9	8	DATA BITS
RUN	MCLR	/////	STEP LU	LU LOOP	ROM 0	ROM I	STEP μ P	BSEL 1

MK-0812
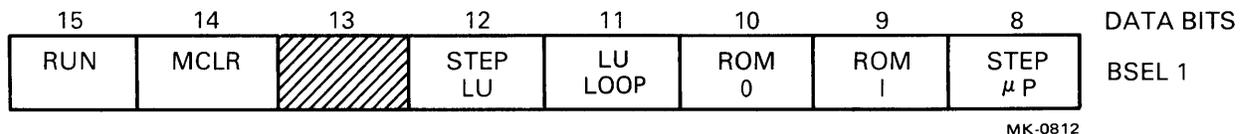
BSEL 1 contains all maintenance functions including MASTER CLEAR and is not intended for normal user communications between the PDP-11 program and the microprocessor. These functions override all other control functions. All bits are read/write; only MASTER CLEAR is functional if the BSEL 1 LOCK OUT switch is set (see DMC11 Engineering Drawings - DMC11-0-8).

Table 5-1 describes the bit functions of BSEL 1.

5.2.2 Maintenance Modes

The DMC11 microprocessor can be tested by two basic modes:

- Maintenance Mode

- System Test (free-running) Mode

The DMC11 line unit can be tested by three basic modes:

- Single Step Internal Maintenance Mode

- System Test Internal Maintenance Mode

- External Maintenance Mode

Table 5-1 BSEL 1 Bit Descriptions

Bit	Name	Description
8	STEP P (Step Microprocessor)	When bit 8 is set, it steps the microprocessor through one instruction cycle which is composed of five 60 nsec pulses. The RUN flip-flop should be cleared before executing this control function.
9	ROM I (ROM Input)	Bit 9 is set and directs the contents of BSEL 6 and 7 as the next microinstruction to be executed by the microprocessor when STEP P is asserted.
10	ROM O (ROM Output)	Bit 10 is set and modifies the source paths for BSEL 4 through 7 to contain the contents of the addressed CROM. If ROM OUT and STEP P are asserted, then the next CROM address will be output to BSEL4 through 7.
11	LU LOOP (Line Unit Loop)	Bit 11 is set and connects the line unit's serial line out back to its serial line in. This loop back is done at the TTL level before level conversion.

When the LU LOOP bit is set and the RUN bit (bit 15) is cleared, the STEP LU clock is the only one available for shifting data in or out.

When the LU LOOP bit is set and the RUN bit is set, data is clocked at 10K bps for the M8201 and 20K bps for the M8202.

If the LU LOOP bit is cleared and the RUN bit is set, the loop back test connector is required. |

LU LOOP	RUN	CLOCK SOURCE	bps	Mode
Set	Clear	STEP LU (bit 12) via PRO-GRAM		Single Step Internal Maintenance
Set	Set	MAINTENANCE CLOCK	10K M8201; 20K M8202	System Test Internal Maintenance
Clear	Set	MAINTENANCE CLOCK (M8201)	10K M8201	External Maintenance
		INTEGRAL MODEM CLOCK (M8202)	line unit speed M8202	

Table 5-1 BSEL 1 Bit Descriptions (Cont)

Bit	Name	Description
		NOTE The DMC11 must be set up in full-duplex mode to run in any loopback maintenance mode. For external loopback mode, test connectors H325/H3250 or 12-12528 are required on the M8201 or M8202-XX respectively.
12	STEP LU (Step Line Receiver)	When bit 12 is asserted, the transmitter shifts; when it is negated, the receiver shifts. This control function is used in conjunction with LU LOOP bit 11 to simulate transmit and receive clocks for line unit maintenance in Single Step Maintenance mode.
13	Reserved	
14	MCLR (MASTER CLEAR)	When bit 14 is set, MCLR initializes both the microprocessor and the line unit. This bit is self clearing. The microprocessor clock is enabled and the RUN bit is asserted, placing the DMC11 in the initialized state.
15	RUN	RUN controls the microprocessor clock: bit 15 is set by BUS initialization or MASTER CLEAR which enables the microprocessor clock. RUN can be cleared for maintenance by RUN INHIBIT switch (E76). See D17 of the M8200 Print Set. Switch BST is provided to prevent RUN from being cleared by a runaway microcode program when the microprocessor malfunctions. Further discussion of the RUN INHIBIT switch is contained in Chapter 2, Installation.

5.2.2.1 Maintenance Mode – The Maintenance Mode can be invoked using selected bits of BSEL 1. These can be used to halt the microprocessor (clear bit 15), step the microprocessor (set bit 8), examine the current CROM location (assert bit 10 and examine SEL 6), and override the current CROM instruction with a different instruction and execute that instruction (load SEL 6 with the new instruction, assert bits 8 and 9, then clear bit 8).

NOTE
1. Be sure that BSEL 1 LOCK OUT (switch 9, E76) is OFF to allow access to the maintenance bits in BSEL 1.

2. With the LOCK OUT switch ON, it is still possible to MASTER CLEAR the microprocessor by setting bit 14 of BSEL 1.

5.2.2.2 System Test – System Test Mode tests the functionality of the microprocessor and line unit running at full speed and utilizing the control ROM.

NOTE
RUN INHIBIT (switch 7, E76) must be off to use this mode and ensure normal operating conditions.

5.2.2.3 Single Step Internal Maintenance Mode – This mode is selected by the PDP-11 program setting LU LOOP and clearing RUN bits 11 and 15 of BSEL 1 respectively. This mode allows checking of most of the line unit without disconnecting the M8201 from the modem or the M8202 from the triaxial cable. Line unit signal D15 SEND H is asserted to keep the transmitter active. The transmitter output is looped back at TTL level to become the receiver input. Line unit REQUEST TO SEND (RTS) and DATA TERMINAL READY (DTR) signals are held unasserted. The clocking source is the D17 STEP LU signal from the microprocessor which becomes D3 STEP LU at the line unit. The PDP-11 program generates the clock signal which sets STEP LINE UNIT bit 12 of BSEL 1.

5.2.2.4 System Test Internal Maintenance Mode – This mode is selected by the PDP-11 program setting LINE UNIT LOOP bit 11 of BSEL 1. This mode allows the program to perform an off-line system test by free-running the DMC11 and checking the line unit without disconnecting the M8201 from the modem or the M8202 from the triaxial cable. The transmitter output is looped back at TTL level to become the receiver input. The clock source is the DMC11 maintenance clock which is 10 KHz for the M8201 and 20 KHz for the M8202 line units.

5.2.2.5 External Maintenance Mode – External Maintenance Mode is selected by the PDP-11 program setting the DMC11 in normal running mode and terminating the cables with a test connector. For the M8201 line unit:

- The modem must be disconnected and the test connector must be connected to the BC05C-25 cable. For the DMC11-DA option (EIA/CCITT V.24 interface), use connector H325. For the DMC11-FA option (CCITT V.35 interface), use connector H3250 (see Figure 2-3 in Chapter 2).

- The 10 KHz internal clock used for clocking the M8201 is looped back in the H325 test connector to simulate modem transmit and receive clocks.

- The modem control signals are tested to ensure the proper level conversion and cable paths exist. The signals are looped back in the H325 connector as follows:

  - Transmitted data is returned as received data.

  - REQUEST TO SEND is returned as CLEAR TO SEND.

  - DATA TERMINAL READY is returned as RING and DATA SET READY.

For the M8202 line unit:

- The triaxial cables must be disconnected and the 12-12528 triaxial adapter must be used to connect the coaxial pigtails attached to the modules. This setup tests all the transmitter and receiver logic as well as the integral modem and pigtails.

- The integral modem clock supplies clocking for the M8202.

External Maintenance Mode provides complete checking of the line unit including level conversion logic and associated cables.

5.3 MAINTENANCE PHILOSOPHY
The Field Replaceable Unit (FRU) for any DMC11 is the failing module or cable. Spare parts are not stocked for module repair in the field. One reason for this is the time and equipment necessary for component level troubleshooting and repair.

- Typical applications of the DMC11 do not permit lengthy troubleshooting sessions which require the associated system to be down for that period.

- Effective component level repair of a DMC11 requires, at a minimum, a 16-channel logic analyzer.

Training of field service personnel in the maintenance of the DMC11 is not directed to the logic gate level, but to functional and application level troubleshooting, using diagnostics for fault isolation to the FRU. Changing ICs should only be done during implementation of Field Change Orders (FCOs), a major reason for installing CROMs in sockets.

Replacement of CROMs requires removing installed CROMs and inserting new ones. An FCO with procedures on how to replace CROMs is normally accompanied by a change to the diagnostics.

When replacing CROMs:

- Be careful not to bend the IC leads.

- Inspect the IC chip after insertion to ensure no leads are bent under the chip.

- Ensure that CROMs are firmly seated and are in their proper sockets; otherwise, erratic operation of the DMC11 may result.

5.4 PREVENTIVE MAINTENANCE (PM)
There is no specific DMC11 PM schedule. It is recommended that the DMC11 be given a general check (for such things as voltages and connections) and when system PM is performed.

A complete checkout of the device by running all diagnostics and if possible, the interprocessor test, is required after handling the DMC11 modules or cables for the following reasons. Special care must be exercised in all cases.

- The DMC11 is susceptible to seating problems.

- Control ROM (CROM) chips installed in sockets are easily dislodged during removal and replacement of the M8200 module or adjacent modules. The CROM chips may inadvertently come in contact with the etch side of the adjacent module.

- AMP connectors recommended for use in DMC11 cabling permit destruction of pin/wire connections. Servicing personnel must only twist the ring on the pigtail connector, while firmly holding the raised ridge portion of the cable and connector. If the wrong part (such as the body of the cable end connector) is twisted, the wires are separated from the pins.

5.5 CORRECTIVE MAINTENANCE

Because the FRU is a module or cable, all corrective action should be directed to isolation of the failing FRU. The DMC11 diagnostics are designed as an aid in the isolation process and as such, should be run starting with the basic microprocessor test and continuing to the interprocessor test. The diagnostics are listed in the proper sequence of execution below.

Diagnostic	Description
CZDMC	DSC-W/R-Micro-Proc-Test (formerly Basic Microprocessor Test)
CZDME	DDCMP-MD-LN-UNIT-TST (formerly Line Unit Test)
DZDMF	DMC Bit Stuff Line Unit Test
CZDMG	DMC ROM and Jump Test
DZDMH	DMC Free-Running Test
DZDMO	DMC ITEP-OVERLAY Interprocessor Test

The testing sequence allows progressive expansion of testing, based on successful completion of the previous test. All tests from DZDMC through DZDMG check the DMC11 logic without running the actual CROM microcode.

NOTE
The following sections reference DMC11 micro-processor internal components, such as, IBUS/OUTBUS Registers, IBUS*/OUTBUS* Registers, Scratchpad Registers (SPX), Branch Registers (BRG), Main Memory, Memory Address Register (MAR), and Arithmetic Logic Unit (ALU). Chapter 4 describes these components in detail.

5.5.1 CZDMC Diagnostics

CZDMC tests operation of DMC11 SEL0 through SEL6 registers, microprocessor instructions, and NPR operations; DMC11 microcode is not used. The microinstruction is loaded into SEL6 and single-stepped to test the IBUS Register, IBUS* Register, SP, Main Memory and ALU.

A summary of tests performed (test numbers in octal) are shown below. For greater detail, refer to diagnostics listings.

TESTS 1–30 test DMC11 register selection; read/write functions of the DMC11 registers SEL0 through SEL6.

TEST 31 tests the DMC11 microprocessor by loading a microinstruction in SEL6 and verifying that the instruction is executed properly.

TESTS 32–37 test read/write functions of DMC11 IBUS* registers 0 to 11.

TESTS 40–50 test read/write functions of DMC11 IBUS registers 0 to 7.

TEST 51 tests the read/write function of the DMC11 Branch Register.

TESTS 52 and 53 test read/write functions of the DMC11 Scratchpad registers 0 to 15.

TESTS 54–57 test the capability of the DMC11 to interrupt vectors XX0 and XX4, and verify that the DMC11 will only interrupt at its designated priority level.

TESTS 60–62 test the capability of the DMC11 to perform NPR/DATO, NPR/DATI, and NPR/DATOB transactions.

TESTS 63 and 64 test the extended memory addressing capability of the DMC11 by performing NPR/DATO and NPR/DATI using BA bits 16 and 17.

TESTS 65 and 66 test the capability of the DMC11 to report a non-existent memory error by performing an NPR/DATO and NPR/DATI to a non-existent memory location.

TEST 67 is an NPR test using DATO to NPR a binary count of 0-377.

TESTS 70–73 test read/write functions and addressing of DMC11 internal Main Memory and MAR.

TESTS 74–134 test each function of the ALU.

TEST 135 tests the program clock bit in the DMC11 Miscellaneous Register (IBUS* Register 11).

TEST 136 tests DMC11's capability to force a power fail and verify that the CPU will trap to location 24.

TEST 137 is a DMC11 microprocessor noise test, performed by writing 1s and 0s in IBUS* Register, IBUS Register, Scratchpad, Main Memory, etc. and reading them back.

NOTE
CZDMC test 136 asserts AC LO on the UNIBUS to
test the capability of the DMC11 to force a power
fail recovery in the system. On PDP-11/40, PDP-
11/45, PDP-11/60, and PDP-11/70 types of proces-
sors, if the bootstrap module has the power-on boot
enabled, the program control is seized by the boot-
strap ROM program and diagnostics will not run
successfully. The reason for this is that on the afore-
mentioned PDP-11s, the AC LO asserted by the
DMC11 causes the CPU to assert DC LO on the
UNIBUS, which causes the bootstrap ROM to exe-
cute a power-on boot if it is enabled. The POWER-
ON BOOT ENABLE switch on the bootstrap mod-
ule (switch 2 – SW2 – on the M9301-XX module)
must be set to OFF.

5.5.2 CZDME DMC11 Line Unit Tests
CZDME loads microinstructions into SEL6 and single steps the microprocessor to check the following functions of the line unit.

- Read/write functions of the Line Unit Register

- Line Unit Clock

- Transmitter and Out Data Silo

- DDCMP specific transmitter functions

- Receiver logic and DDCMP specific functions

- CRC Operation on transmit and receive

- Half-Duplex Test

- DDCMP Cable Data Test

5.5.3 DZDMF DMC11 Bit Stuff Line Unit Tests
DZDMF loads microinstructions into SEL6 and single steps the microprocessor to check out the following functions of the line unit.

- Line unit registers read/write tests

- Out Data Silo and Bit Stuff Protocol specific transmitter function tests

- In Data Silo and Bit Stuff Protocol specific receiver function tests

- CRC Operation and Bit Stuff Cable Data Test

5.5.4 CZDMG DMC11 CROM and Jump Test
CZDMG:

- Verifies the contents of the CROMs by comparing each CROM location with a copy of the correct microcode imbedded in the diagnostic.

- Verifies code for both the DMC11-AR and AL versions.

- Has facilities for supporting only one copy of microcode for each microprocessor type (AR and AL).

- Identifies the expected version of microcode by listing the chip part numbers at the respective revision level.

Comparison errors are reported if a defective ROM is encountered or if the diagnostic is run on a wrong revision of microcode. All variations of the Jump microinstruction are also tested by loading microinstructions into SEL6 and single stepping the microprocessor.

The following list is a summary of the tests performed (test numbers in octal):

TEST 1 types, on the console, the part numbers of the CROMs which are supported by this revision.

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TEST 2 is run only on a DMC11 (DMC with writtable control store) to load the CRAM with the DDCMP microcode.

TEST 3 tests the DMC11 Branch Register right shift.

TEST 4 checks each ROM location and compares it to a software copy of the microcode. Jump Immediate microinstructions are also tested.

TESTS 5–22 test Jump instructions by loading the microinstructions into SEL6 and single-stepping the microprocessor.

5.5.5 DZDMH DMC11 Free-Running Tests

The DMC11 microprocessor and line unit are checked out in freerunning mode. This test is the most comprehensive check of the DMC11. All error reporting features and interrupt-driven transmit and receive data are checked.

The DZDMH diagnostic:

- Is the first diagnostic in the sequence to turn on the DMC11 RUN bit and execute CROM code.

- Performs a good functional check of most of the DMC11 capabilities.

- Runs in loopback mode and may be run with or without a turnaround connector.

Note that when DZDMH is used with an M8202 line unit, it is assumed that a turnaround connector is installed. Errors are reported if no turnaround connector is installed.

If a turnaround connector is installed, the following data rates are used with respective line units:

DMC11-DA/FA - M8201 – 10K bps

DMC11-MA - M8202-YA – 1M bps

DMC11-MD - M8202-YD – 56K bps

For M8202 type line units, the data is transferred from transmitter to receiver at full integral modem speed. This transfer performs a good check of the DMC11's capability to talk to itself at full speed.

For M8201 type line unit, the maintenance clock speed of 10K bps may or may not be near normal operating speed; however, use of the H325 or H3250 turnaround connector allows testing of the level converters and cables.

Running in local loop mode establishes a confidence level from which expansion to interprocessor testing may begin.

The following list is a summary of the tests performed.

TEST 1 runs DMC11 microcode to transmit a message and then receive and check the message using Line Unit Loop Mode.

TEST 2 is an overrun test which sends a message with no receive buffer available; it verifies that an overrun error occurs.

TEST 3 is a lost data test which sends a message of greater length than the receive buffer; it verifies that a lost data error occurs.

TEST 4 is a transmit non-existent memory test which loads a transmit BA that will time out; it verifies that a non-existent memory error occurs.

TEST 5 is a receive non-existent memory test which loads a receive BA that will time out; it verifies that a non-existent memory error occurs.

TEST 6 is a processor error test which does a BASE I transfer request after a BASE I has been set up; it verifies that a processor error occurs.

TEST 7 is a processor error test which does an RQI with an illegal 10 code; it verifies that a processor error occurs.

TEST 10 is a half-duplex test which sets half-duplex and LU LOOP, sends a message, and verifies that none are done.

TEST 11 is a resume test which sends and receives a buffer and shuts down the DMC. A MASTER CLEAR is then issued and a BASE I command with the RESUME bit set is given, another buffer is sent and received, and data is checked.

TEST 12 is a data test (interrupt driven exerciser) which repeatedly queues up to seven receive buffers and seven transmit buffers and checks data when all seven buffers are received. Transmit counts range from 2 to 104. Data is a binary count pattern. The resume function is checked in this test. Test 12 uses the turnaround connector if it is present; otherwise, the LU LOOP bit is set.

5.5.6 DZDMO – DMC11 Overlay for Interprocessor Test Program (ITEP)
This test is used to isolate various interconnect problems between systems. Through a methodical series of tests, failures are identified in level converters, cables and connections, modems, lines between modems, and modem incompatibilities.

ITEP has been useful in identifying new or modified software problems. In this role, ITEP is used to isolate the hardware from the system software. Typically, if ITEP runs, the system software should run. ITEP provides a controlled environment for test purposes often unavailable in operating systems. ITEP can be used for loop testing, providing the ability to incrementally test larger (or smaller) segments of the communications link. For instance, if a failure occurs when running in Modem Analog Loop Mode rather than in Cable Loop Mode (with an H325 connector), the probability of a modem or modem interface fault is increased.

ITEP is more of a confidence test than a true diagnostic, and provides a GO/NO-GO indication of the integrity of the communications link. ITEP is often used for installation acceptance, as well as confirmation of a corrective action.

An ITEP feature not provided in any of the stand-alone diagnostics is the capability of checking out the REMOTE LOAD DETECT (RLD). The DMC11 Overlay for Interprocessor Test program is designed to verify the proper operation of a complete communications link from one PDP-11 system to another or to a communication test center. The program must be used in conjunction with the Interprocessor Test Monitor program (DZITA) on a PDP-11 system with a DL11 interface. Two tests for the DMC11 are selectable by the parameter locations provided in ITEP.

TEST 1 is a link test which provides a GO/NO-GO test (a confidence check) on the communications link (could be either half-duplex or full-duplex).

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<u>TEST 2</u> is a bootstrap test which checks the ability of a DMC11 to boot another DMC11 using Maintenance Operation (MOP) messages. The bootstrap test requires an M9301-YJ (UNIBUS terminator with bootstrap) or equivalent boot module at one station.

The RLD feature of the DMC11 is checked out; the host sends an Enter MOP Message to a remote station to initialize the entire system and cause program control to be transferred to a Boot ROM program (such as the one contained in an M9301-YJ). The Boot ROM program then requests a program (or in true on-line application, a secondary Boot program) to be down-line loaded and eventually execute that program.

Only the down-line load feature of the DMC11 can be checked; a remote station sends a program REQUEST MOP MESSAGE, and the Host with its DMC11 running ITEP will down-line load a program to the remote station.

NOTE
1. Refer to Appendix F for detailed operating procedures of the Bootstrap testing under the ITEP program.

2. Refer to Appendix H for detailed operating procedures of the link test, ITEP program.

3. Refer to the diagnostic listings for detailed operating procedures of CZDMC, CZDME, DZDMF, CZDMG, and DZDMH diagnostics. A copy of the operating procedures for the DZDMH is included in Appendix I for ease of reference.

5.5.7 DEC/X11 DMC11 Module
The DEC/X11 DMC11 module, DMCA, is designed to exercise up to and including four consecutively addressed DMC11 synchronous interfaces. One pass of the DMCA module consists of transmitting and receiving seven buffers of 100 characters, 100 times for each selected device.

It is recommended that bit 0 of the DMCA switch register 1 (SR1) be set to 1 and that a test connector be installed (H325 or H3250 for M8201 line units; 12-12528 for M8202s) when running DEC/X11 (as indicated in the checkout procedures in Chapter 2).

Installing the test connector and setting bit 0 of SR1 allows the DMCA to run in external loopback mode and therefore generates more activity on the UNIBUS.

External loopback mode for:

- M8201 is run at 10K bps

- M8202-YA is run at 1M bps

- M8202-YD is run at 56K bps

5.5.8 Soft Error Reports Under DEC/X11
Soft errors indicate errors which occurred causing a message retransmission. These errors are not reported to the PDP-11 unless they exceed a threshold of seven on any given message. A cumulative count of soft errors is kept in DMC11 RAM memory. The RAM memory is written to PDP-11 memory (beginning at the assigned base address) whenever a fatal DMC error occurs.

DEC/X11 forces a fatal procedure error on the DMC after each pass. The reason for this is to force a Base Table update, allowing the DEC/X11 module to check the cumulative error counters.

The soft error report may be used in the isolation of certain DMC11 failures from UNIBUS loading or latency problems.

The DMC has no Data Late bit or capabilities for detecting the fact that it did not obtain BUS mastership in time to service the synchronous line. The DMC sees such a condition as an error in the synchronous data stream (a BCC error) and the DDCMP causes the message to be retransmitted. This occurrence causes incrementation of the cumulative error counters in DMC11 RAM memory.

A process of elimination must be used to determine whether soft errors (BCC) are caused by BUS latency or possible failing DMC11 hardware.

Typically, the DMC11 should show no errors when running in a local loopback mode. This is normally a noise-free circuit. Therefore, any soft error reports should be examined and the cause isolated.

If soft errors are reported while running a DMC on a fully loaded system (other devices being exercised simultaneously), they may be due to BUS latency. This may be verified by running only the DMC DEC/X11 module with only one DMC enabled. If the soft errors cease, a latency condition is indicated.

If soft errors persist while running only the DMC DEC/X11 module, the DMC device diagnostics should be run. The problem could be a faulty DMC11 or cable.

SR1 (bit 0) may be used in the isolation process. If bit 0 is set, DEC/X11 does not set line unit loopback and uses an external turnaround. By running with bit 0 clear, a TTL loopback is performed, eliminating the possiblity of the cable/turnaround connector being faulty.

With M8201 line units, bit 0 clear eliminates the EIA level converters. The bit rate is 20K bps.

With M8202 line units, bit 0 clear eliminates the integral modem. The bit rate is 10K bps.

5.5.9 Examination of DMC11 Internal Components
Following are some procedure examples for examining DMC11 memory and Scratchpad registers.

Example 1: Examine DMC11 memory

Procedures	Comments
1. Load 0 SEL0	;To clear Run bit and stop the ;microprocessor
2. Load 010XXX to SEL6	;Microinstruction LDMAR IMM,OPR ;is loaded into SEL6 where XXX is an ;eight bit memory address which is ;loaded into MAR
3. Load 1400 to SEL0	;Set ROM In and STEP P bits
4. Load 055224 to SEL6	;Load microinstruction OUT* MAR, SELB, PORT1, INMAR to SEL6 to read memory content pointed to by MAR to SEL4. MAR is incremented.
5. Load 1400 to SEL0	;

| 6. | Examine SEL4 low byte for memory content | ;Low byte of SEL4 contains content of memory location under examination. |

Example 1 (Cont)

| 7. | Go to Step 5 for examination of consecutive memory locations | ;
;
; |

NOTE
**Refer to the DMC11 Base Table layout in Chapter 3
for DMC11 main memory assignments.**

Example 2: Examine DMC11 Scratchpad registers

Procedures	Comments
1. Load SEL0 with 0	;To clear RUN bit
2. Load SEL6 with 0606XX	;SEL 6 is loaded with microinstructions. BR, SELA, SPX where XX is 0–17, Scratchpad Register content of SP is loaded into the Branch Register.
3. Load SEL0 with 1400	;Set ROMIN and single step the microprocessor.
4. Load SEL6 with 061224	;Microinstruction OUT BR, SELB, PORT1 where content of SPX (from BR) is loaded into SEL4 low byte.
5. Examine BSEL4 for content of SPX	;Low byte of SEL 4 contains contents of Scratchpad X.

5.6 POSSIBLE OVERLOADING OF MAINTENENANCE CLOCK SIGNAL
During the fault isolation process, it may become necessary to use a serial line monitoring device. Such a device is often used in verification of transmit/receive data at a point between the modem and the DMC11 line unit.

In some cases, the additional load of the monitor on the TRANSMIT SIG ELEMENT TIMING signal (pin 24) may cause data errors or a complete failure to occur. These conditions are due to overloading and signal degradation which usually happens when attempting to use an H325 connector or a null modem with the monitor. The problem may be alleviated by soldering a wire jumper across R45 (a 75 ohm resistor in series with the clock driver) on the M8201 module. The jumper must be removed when testing is complete.

NOTE
**The DMC11 clock output is not normally used as a
clock source except for diagnostic purposes. How-
ever, some applications may require use of this clock
source and, as such, could require a jumper across
R45 for reliable operation.**

5.7 DDCMP MESSAGE FORMAT FOR DMC11
Table 5-2 reflects the various DDCMP messages as they appear on the serial link. This chart is useful in data analysis with the use of a serial link analyzer.

Table 5-2 DDCMP Message Decode for DMC11-AR & AL

Type of Message	Code	Class	Count Bits 7-0	Flag 2 Bits	Count Bit 13-8	Response	Sequence	Address Point To Point
Start Message	Bits	00000101	00000110	1 1	000000	00000000	00000000	00000001
	Hex	0 5	0 6		C 0	0 0	0 0	0 1
	ASC11	ENQ	ACK		@	NUL	NUL	SOH
Start Acknowledge-ment	Bits	00000101	00000111	1 1	000000	00000000	00000000	00000001
	Hex	0 5	0 7		C 0	0 0	0 0	0 1
	ASC11	ENQ	BEL		@	NUL	NUL	SOH
Acknowledgement	Bits	00000101	00000001	1 1	000000	No. Last Good Msg. Rcvd.	00000000	00000001
	Hex	0 5	0 1		C 0	"	0 0	0 1
	ASC11	ENQ	SOH		@	"	NUL	SOH
Data Message	Bits	10000001	No. of Char.	S Q	No. of Char.	"	No. Msg. Sent	00000001
	Hex	8 1	"	S Q	"	"	"	0 1
	ASC11	SOH	"	S Q	"	"	"	SOH
Negative Acknow-ledgement BCC Header Error	Bits	00000101	00000010	1 1	000001	"	00000000	00000001
	Hex	0 5	0 2		C 1	"	0 0	0 1
	ASC11	ENQ	STX		A	"	NUL	SOH
Negative Acknow-ledgement BCC Data Error	Bits	00000101	00000010	1 1	000010	"	00000000	00000001
	Hex	0 5	0 2		C 2	"	0 0	0 1
	ASC11	ENQ	STX		B	"	NUL	SOH
Negative Acknow-ledgement Buf-fer Unavailable	Bits	00000101	00000010	1 1	001000	"	00000000	00000001
	Hex.	0 5	0 2		C 8	"	0 0	0 1
	ASC11	ENQ	STX		H	"	NUL	SOH
Negative Acknow-ledgement Recei-ver Overrun	Bits	00000101	00000010	1 1	001001	"	00000000	00000001
	Hex	0 5	0 2		C 9	"	0 0	0 1
	ASC11	ENQ	STX		I	"	NUL	SOH
Negative Acknow-ledgement Mes-sage Too Long	Bits	00000101	00000010	1 1	010000	"	00000000	00000001
	Hex	0 5	0 2		D 0	"	0 0	0 1
	ASC11	ENQ	STX		P	"	NUL	SOH
Negative Acknow-ledgement Header Format Error	Bits	00000101	00000011	1 1	010001	"	00000000	00000001
	Hex	0 5	0 2		D 1	"	0 0	0 1
	ASC11	ENQ	STX		Q	"	NUL	SOH

Table 5-2 DDCMP Message Decode
for DMC11-AR & AL (Cont)

Type of Message	Code	Class	Count Bits 7-0	Flag 2 Bits		Count Bit 13-8	Response	Sequence	Address Point to Point
Reply Message	Bits	00000101	00000011	1	1	00000000	00000000	No. Last Msg. Sent	00000001
	Hex	0 5	0 3			C 0	0 0	"	0 1
	ASC11	ENQ	ETX			@	NUL	"	SOH
Negative Acknowledgement Reply Response	Bits	00000101	00000010	1	1	000011	No. Last Good Msg. Rcvd.	00000000	00000001
	Hex	0 5	0 2			C 3	"	0 0	0 1
	ASC11	ENQ	STX			C	"	NUL	SOH
Maintenance Message	Bits	10010000	No. of Char.			No. of Char.	00000000	00000000	00000001
	Hex	9 0	"			"	0 0	0 0	0 1
	ASC11	DLE	"			"	NUL	NUL	SOH

The PDP-11 memory is organized in 16-bit words consisting of two 8-bit bytes. Each byte is address-able and has its own address location; low bytes are even numbered and high bytes are odd numbered. Words are addressed at even numbered locations only and the high (odd) byte of the word is automat-ically included to provide a 16-bit word. Consecutive words are therefore found in even numbered addresses. A byte operation addresses an odd or even location to select an 8-bit byte.

The UNIBUS address word contains 18 bits identified as A(17:00). Eighteen bits provide the capability of addressing 256K bytes of memory locations, each of which is an 8-bit byte. This also represents 128K 16-bit words. In this discussion, the multipler K equals 1024 so that 256K represents 262,144 locations and 128K represents 131,072 locations. The maximum memory size can be used only by a PDP-11 processor with a memory management unit that utilizes all 18 address bits. Without this unit, the processor provides 16 address bits which limits the maximum memory size to 64K (65,536) bytes or 32K (32,768) words.

Figure A-1 shows the organization for the maximum memory size of 256K bytes. In the binary system, 18 bits can specify 2^{18} or 262,144 (256K) locations. The octal numbering system is used to designate the address. This provides convenience in converting the address to the binary system that the proces-sor uses as shown below.

The highest 4K word address (8K bytes) locations (760000–777777) are reserved for internal general registers and peripheral devices. As a result, programmable memory locations cannot be assigned in this area; therefore, the user has 248K bytes or 124K words to program.

A PDP-11 processor without the memory management unit provides 16 address bits that specify 2^{16} or 65,536 (64K) locations (Figure A-2). The maximum memory size is 65,536 (64K) bytes or 32,768 (32K) words. Logic in the processor forces address bits A(17:16) to 1s if bits A(15:13) are all 1s when the processor is master allowing address generation in the reserved area with only 16-bit control.

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	ADDRESS BIT
0	0	1	0	0	1	1	1	1	1	1	0	0	0	0	0	1	0	BINARY
	1			1			7			6			0			2		OCTAL

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Bit 13 becomes a 1 first at octal 160000 which is decimal 57,344. This is the beginning of the last 8K bytes of the 64K byte memory. The processor converts locations 160000–177777 to 760000–777777 which relocates these last 8K bytes (4K words) to the highest locations accessible by the bus. These are the locations that are reserved for internal general register and peripheral device addresses; therefore, the user has 57,344 (56K) bytes or 28,672 (28K) words to program.

A-1
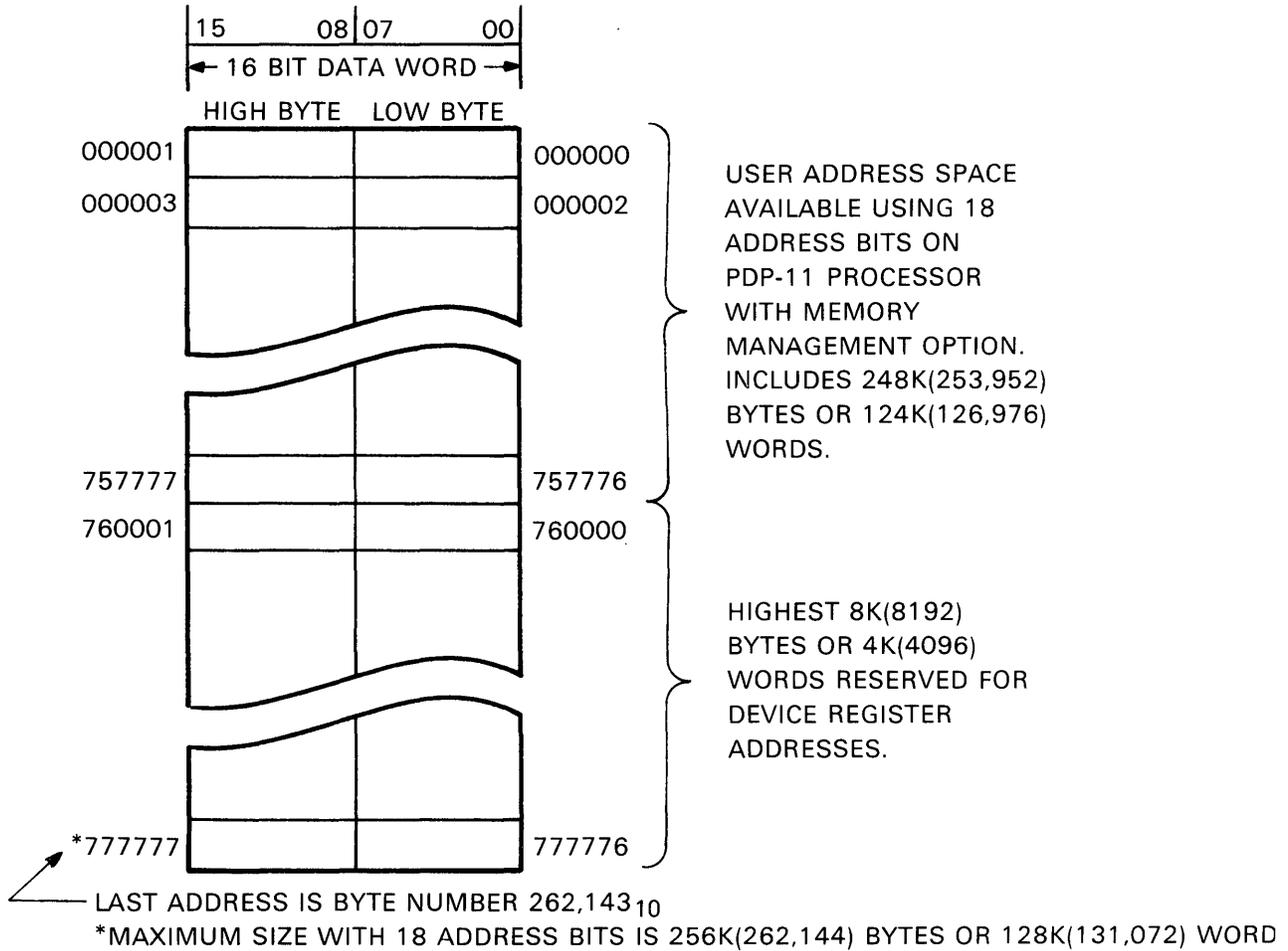
Figure A-1   Memory Organization for Maximum Size Using 18 Address Bits

```
         15        08 07        00
        |← 16 BIT DATA WORD →|
        HIGH BYTE   LOW BYTE
000001 ┌──────────┬──────────┐ 000000
000003 ├──────────┼──────────┤ 000002
       │          │          │
       ~          ~          ~

       ~          ~          ~
157777 ├──────────┼──────────┤ 157776
160001 ├──────────┼──────────┤ 160000
       │          │          │
       ~          ~          ~

       ~          ~          ~
*177777└──────────┴──────────┘ 177776
```

USER ADDRESS SPACE
AVAILABLE USING 16
ADDRESS BITS ON
PDP-11 PROCESSOR
WITHOUT MEMORY
MANAGEMENT OPTION.
INCLUDES 56K (57,344)
BYTES OR 28K (28,672)
WORDS.

ADDRESSES 160000-
177777 ARE CONVERTED
TO 760000-777777 BY
THE PROCESSOR. THUS,
THEY BECOME THE
HIGHEST 8K (8192) BYTES
OR 4K(4096) WORDS
RESERVED FOR DEVICE
REGISTER ADDRESSES.

LAST ADDRESS IS BYTE NUMBER 65,535$_{10}$
*MAXIMUM SIZE WITH 16 ADDRESS BITS IS 64K (65,536) BYTES OR 32K(32,768) WORDS.

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Figure A-2   Memory Organization for Maximum Size Using 16 Address Bits

A-3

Memory capacities of 56K bytes (28K words) or less do not have the problem of interference with the reserved area because designations less than 160000 do not have a binary 1 in bit A13. No addresses are converted and there is no possibility of physical memory locations interfering with the reserved space.

PDP-11 core memories are available in 4K word or 8K byte increments. The highest locations of various size core memories are shown below.

Memory Size		Highest Location
K words	K bytes	(octal)
4	8	017777
8	16	037777
12	24	057777
16	32	077777
20	40	117777
24	48	137777
28	56	157777

B.1 INTRODUCTION

The logic symbology used in the PDP-11 manuals and engineering logic is generally consistent with *Graphic Symbols for Logic Diagrams* (MIL-STD-806B). Certain symbols are modified by DIGITAL to allow direct reading of logic functions in detailed logic diagrams that show explicit electrical connections between logic elements. The modifications and other conventions are explained in the following paragraphs.

B.2 UNIBUS SIGNAL LEVELS

The UNIBUS has 56 dedicated signal lines. Negative logic is used for 51 lines and the remaining 5 lines, BG(7:4) and NPG, use positive logic.

The definitions of positive and negative logic are:

Positive Logic
      Signal asserted: high = logical 1 = +3V
      Signal at rest: low   = logical 0 = 0V

Negative Logic
      Signal asserted: low = logical 1 = 0V
      Signal at rest: high = logical 0 = +3V

In the logic diagrams, the signal name mnemonic is followed by an H or L to indicate the asserted state (logical 1) of the signal to be high (+3V) or low (ground or 0V). Using this convention, a grant line is called BUS BG2 H and a data line is called BUS D12 L.

B.3 EQUIVALENT GATE SYMBOLS

In the detailed logic diagrams, the gate symbols show the active state of the gate output. A small circle at the output shows that the active state is low (L). The absence of a small circle at the output shows that the active state is high (H).

A large number of NAND and NOR gates are used in DIGITAL logic. The symbols for the NAND and NOR gates show an active low output. Frequently, an active high output is required from a NAND or NOR gate. In this case, a logically equivalent symbol is used to retain the concept of direct reading of logic functions.

For the NAND gate, the logically equivalent negated-input OR gate is used to show the active high output. For the NOR gate, the logically equivalent negated-input AND gate is used to show the active high output. These gate symbols and associated truth tables are shown in Figure B-1.

VOLTAGE
TRUTH TABLE

A	B	C
L	L	H
H	L	H
L	H	H
H	H	L	ACTIVE

NAND
$C = \overline{AB}$

VOLTAGE
TRUTH TABLE

A	B	C
L	L	H
H	L	H
L	H	H
H	H	L

ACTIVE (for rows 1-3)

NEGATED INPUT OR
$C = \overline{A} + \overline{B}$

VOTAGE
TRUTH TABLE

A	B	C
L	L	H
H	L	L
L	H	L
H	H	L

ACTIVE (rows 2-4)

NOR
$C = \overline{A + B}$

VOLTAGE
TRUTH TABLE

A	B	C
L	L	H	ACTIVE
H	L	L	
L	H	L	
H	H	L	

NEGATED INPUT AND
$C = \overline{A}\,\overline{B}$
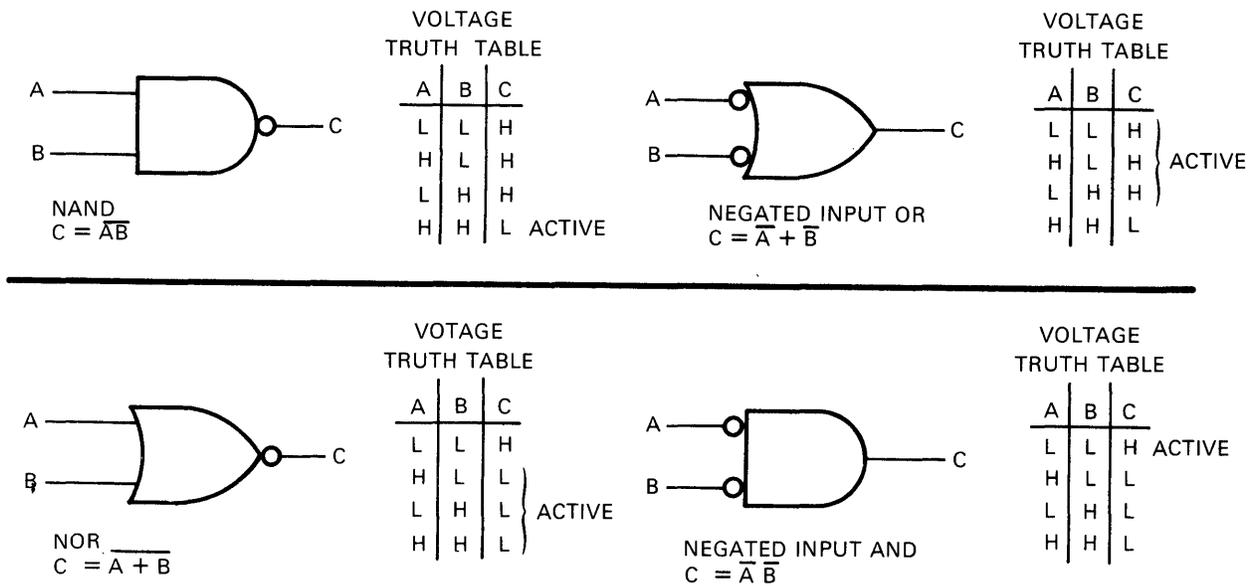
MK-0823

Figure B-1   Logically Equivalent Gates

B.4   4-OUTPUT TERMINAL FLIP-FLOP SYMBOLOGY

The 7474 D-type flip-flops in the engineering logic diagrams are shown as 4-output terminal devices. Most other users (and the IC manufacturers) show them as 2-output terminal devices, which represents only the physical output connections. Both the 4-output symbol and the 2-output symbol are shown in Figure B-2.

The flip-flop is a 2-state device with a pair of complementary outputs. The 4-output terminal symbology defines the polarity of the outputs for each state of the flip-flop. In this discussion, the states are set and reset which are obtained by clocking the flip-flop with its D input high or low, respectively. These states can also be obtained by enabling the PRESET and CLEAR inputs which override the clock. In Chapter 4 of this manual (as in most other DIGITAL manuals) the distinction between set/reset and preset/clear is not maintained. A flip-flop is said to be either set or cleared, regardless of the method used to obtain the state.

In the 4-output symbol (Figure B-2), the flip-flop name is NRA and the output signal designations contain the name, state (asserted or not asserted), and polarity (high or logical 1) or L (low or logical 0); that is, assuming positive logic conventions in which H = 1 = +3V and L = 0 = 0V. For example, NRA (0) L means that this output is low when the flip-flop is reset (cleared). Usually, the PRESET input is placed near the 1-output because it directly sets the flip-flops; the CLEAR input is placed near the 0-output because it directly resets the flip-flop. Physically, nothing has changed; flip-flop operation is still the same and there are two electrical outputs (pin 9 for the 1-output and pin 8 for the 0-output).

The 4-terminal symbol and signal designators allow direct reading of logic functions in detailed logic diagrams that show explicit electrical connections between the flip-flop outputs and other logic elements. The correct output polarity, pin number, and flip-flop state are read at a glance. This is not possible with the 2-terminal symbol without mental translations. A comparative example is shown in Figure B-3.

4 OUTPUT TERMINAL SYMBOL (DEC USAGE)   2 OUTPUT TERMINAL SYMBOL (OTHER USAGE)
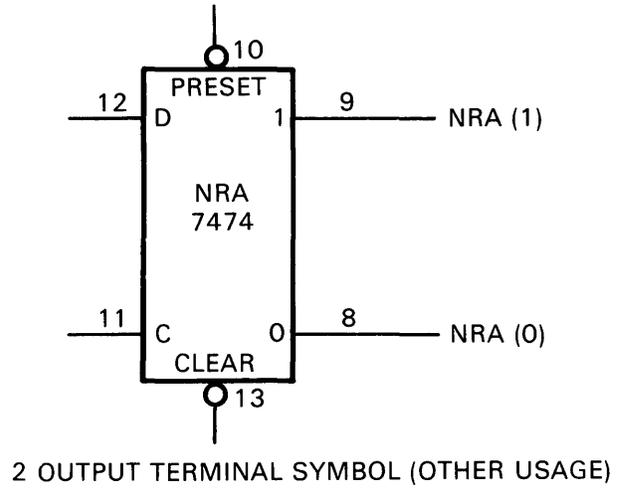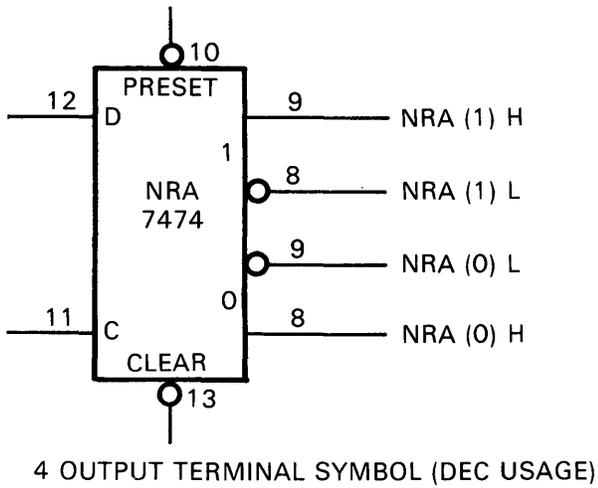
MK-0834

Figure B-2   Flip-Flop Logic Symbology

TWO OUTPUT TERMINAL DESIGNATION   FOUR OUTPUT TERMINAL DESIGNATION
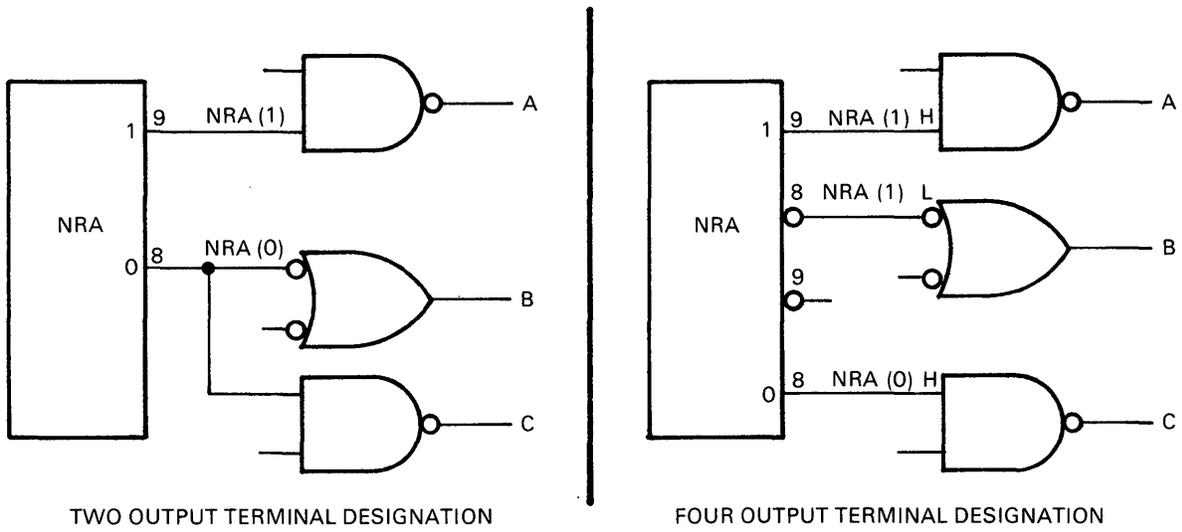
MK-0824

Figure B-3   Electrical Connections to Outputs of 2-Terminal and 4-Terminal Flip-Flops

B-3

B.5 REDEFINED 4-OUTPUT TERMINAL FLIP-FLOPS

Logically speaking, a redefined flip-flop is asserted (set) when clocked with a low signal on its D-input. Graphically, this is accomplished by reversing the output pin assignments and placing a circle on the D-input. The PRESET and CLEAR input pin designations are interchanged because their logical functions are reversed: PRESET directly resets the flip-flop, and CLEAR directly sets the flip-flop. Physically, the flip-flop operation is still the same. Redefinition is used to retain consistency in graphically representing the asserted state of a flip-flop in a detailed logic diagram; specifically, to produce the asserted state with a low signal on the D-input.

Pin designations and outputs for a standard 4-output terminal flip-flop and a redefined 4-output terminal flip-flop are shown in Figure B-4.
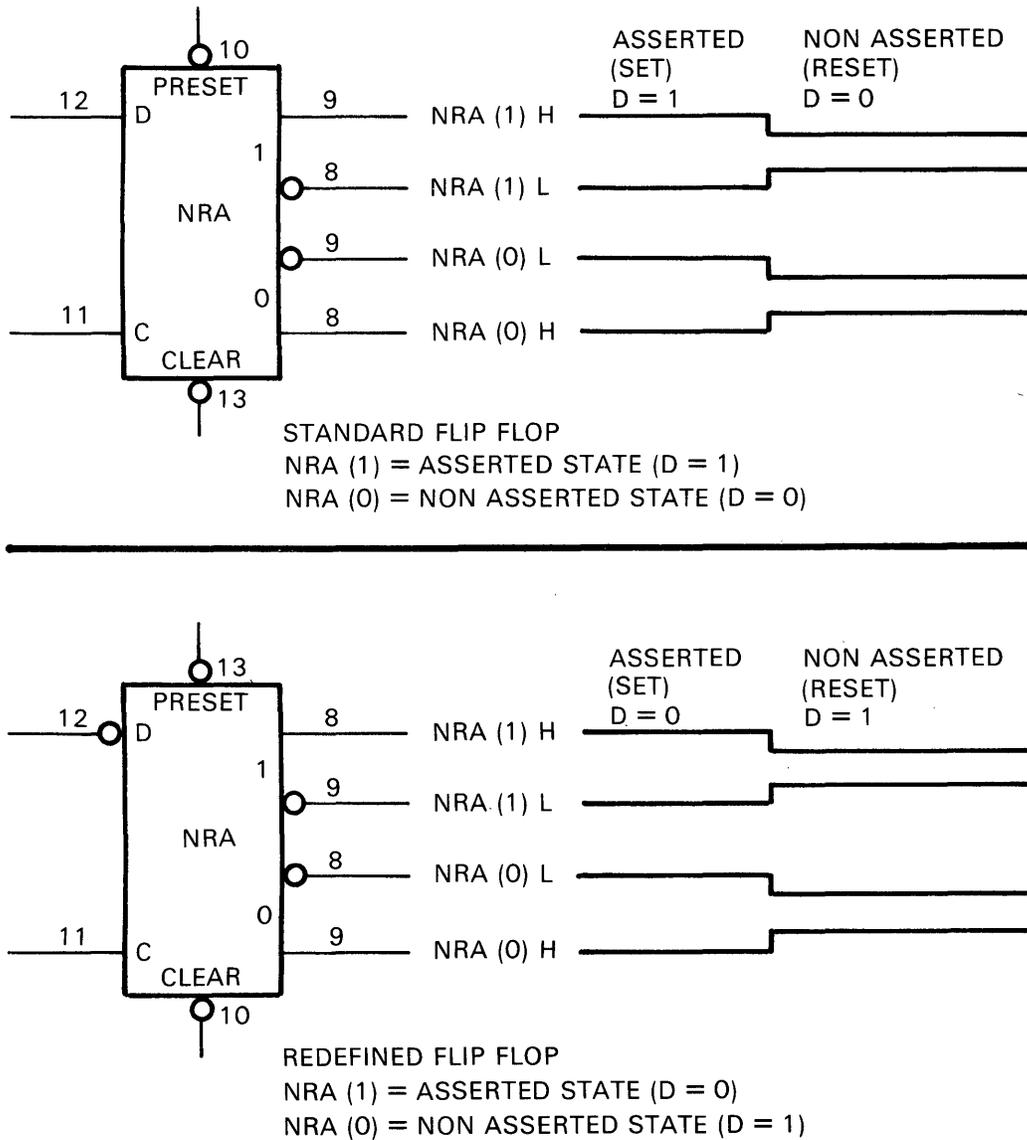
MK-0825

Figure B-4   Standard and Redefined 4-Terminal Flip-Flops

This appendix contains a discussion of the principles of synchronous serial data transmission and reception, followed by descriptions of the synchronous receivers and transmitters used in the DV11 Synchronous Multiplexer.

C.1 BINARY DATA TRANSFER METHODS

Bits of binary data are commonly transferred between digital machines by changes in current or voltage. Data may be transferred in serial over a single line, or in parallel over several lines at once. The transfers may be synchronous, in which the exact departure or arrival time of each bit of information is predictable, or they may be asynchronous, in which case the data may be transferred at non-uniform rates. Aspects and applications of these data transfer modes will now be discussed.

C.1.1 Parallel vs Serial

In parallel transmission, each bit of the set of bits that represent a character has its own wire. An additional wire called the "strobe" or "clock" lead notifies the receiver unit that all of the bits are present on their respective wires so that the voltages on the wires can be sampled. Figure C-1 schematically depicts the parallel transfer of the 8-bit character, 11000001.

+3V	1	+3V
+3V	1	+3V
0V	0	0V
0V	0	0V
0V	0	0V
0V	0	0V
0V	0	0V
+3V	1	+3V

+3V / 0 ⎍⎍ _____ STROBE _____ ⎍⎍ +3V / 0
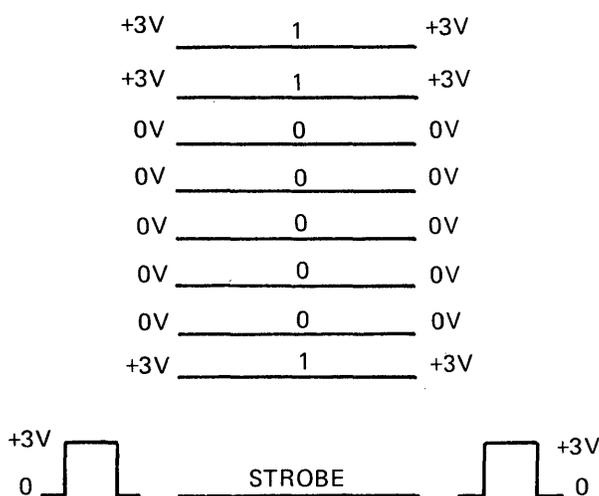
MK-0814

Figure C-1   Parallel Data Transfer

In serial transmission, the bits that represent a character are sent down a single wire one after the other.

Computers and other high-speed digital machines generally operate on parallel data, so data is transferred in parallel between these devices wherever they are in close physical proximity. However, as the distance between the devices increases, the multiple wires not only become more costly, but the complexity of the line drivers and receivers increases, due to the increased difficulty of properly driving and receiving signals on long wires.

Serial transmission is generally used where the cost of the communication medium (wires) is sufficiently high that a relatively complex transmitter/receiver system is justified. The more complex system will serialize the bits that represent the character, send them over a single line, and reassemble them in parallel form at the reception end.

Conversion from parallel to serial and from serial to parallel is typically done with shift registers. In most data communications applications, serial transmission is preferable to parallel transmission.

C.1.2 Asynchronous vs Synchronous

Because of the mechanism design in early serial teleprinters, and to facilitate fail-safe operation, serial teleprinter systems have adopted the convention that an idle line (no data being sent) is one in which current is flowing. Data transmission occurs when the current in the line is interrupted in a specified fashion. By convention, the idle (current flowing) state is called the I state or MARK condition, and the lack-of-current state is called the 0 state or SPACE condition. To start the receiving teleprinter mechanism, the line is brought to the 0 state for 1-bit time. (This is called the START bit.) For the next eight successive bit times, the line is conditioned to a 1 state or 0 state, as required, to represent the character being sent. To allow the receiving teleprinter mechanism to coast back to a known position in time for the beginning (START bit) of the next character, one or more bit times of 1 state (idle) are sent. This period is called the STOP bit interval.

Except for the requirement that the line be idle for at least the STOP bit interval, the transmission of the next character can begin at any time. The lack of a continuous synchronous agreement between the transmitter and the receiver (specifically, the lack of a clocking signal within or accompanying the data channel) causes this type of transmission to be called asynchronous, literally, without synchronization.

A typical asynchronous receiver contains an interval clock and a system for detecting the 1-to-0 transition that indicates the beginning of a start bit. The internal clock delays one-half bit time, checks to see that the start bit condition is still on the line and then makes eight successive samples, 1-bit time apart, to determine the eight bits being sent.

Although modern asynchronous receivers do not require a stop interval for mechanism coasting purposes, they do require a stop interval to guarantee that each character will begin with a 1-to-0 transition, even if the preceding character was all zero bits. This requirement for a 1-to-0 transition, to indicate the beginning of each character, causes a complete character to require 10 bit times, only 8 of which contain real data. The other 20 percent of the line time is used strictly for timing purposes. The asynchronous character format is shown in Figure C-2.

Synchronous communications require either a separate rate clock lead from the transmission point to the reception point (in addition to the data lead) or a modem that includes the clock information with the data. In the case of a modem, the clock is recovered from the signal sidebands by the modem and is brought out of the modem as a separate lead. This indicates to the data communications hardware (typically a computer interface) the appropriate instant to sample the data on the received data lead.

The inclusion of the clock in the data stream or in a separate lead keeps the transmitter and receiver in sync, hence the term synchronous communication. Synchronous character format is shown in Figure C-3.
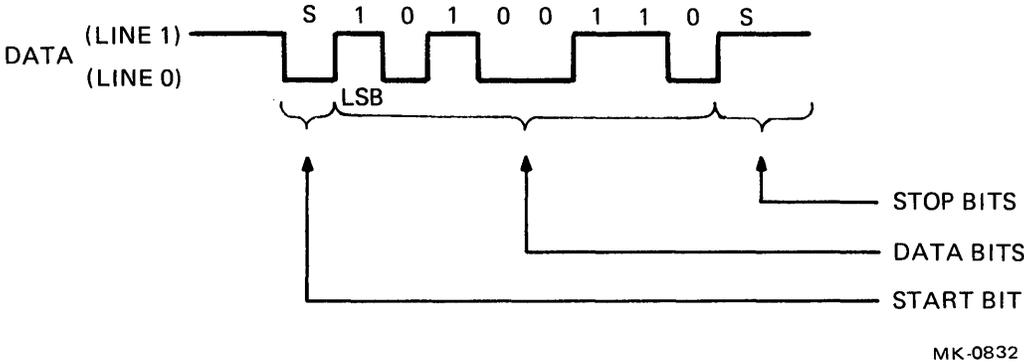
Figure C-2   Asynchronous Character Format
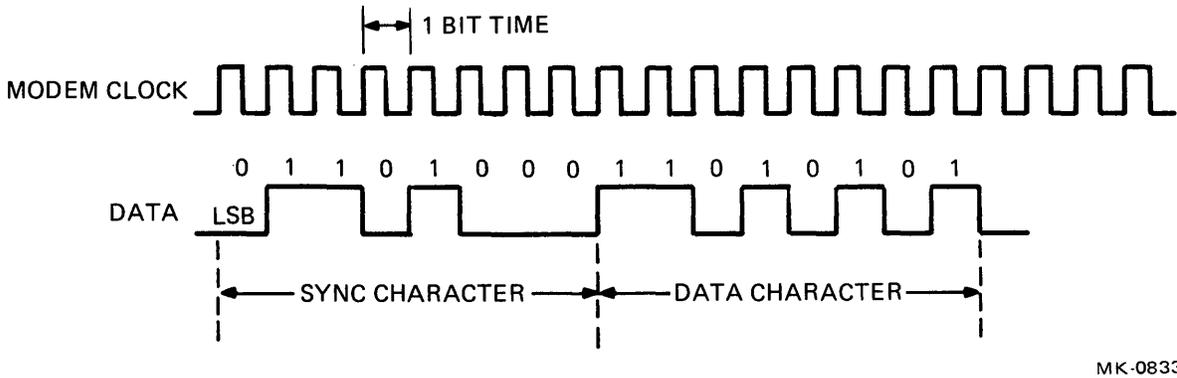
Figure C-3   Synchronous Character Format

C.1.3   Synchronizing at the Receiver

Since start and stop bits are not required in synchronous communications, all bits are used to transmit data; therefore, there is not the 20 percent waste characteristic of asynchronous communication. However, the character framing information provided by the start and stop bits is absent, so another method of determining which groups of bits constitute a character must be provided.

In Figure C-4, bits 1-8 might be one character and bits 9-13 part of another character, or bit 1 may be part of one character, bits 2-9 part of a second character, bits 10-13 part of a third character, and so on. The delimiting or framing of each actual character is accomplished by defining a sync character. The sync character is usually chosen such that its bit arrangement is significantly different from that of any of the regular characters being transmitted. Thus, when a sync character is preceded and followed by regular characters, there is no possible successive pattern of bits that equal the bit patterns of the sync character, except those eight bits that actually are the sync character.

Figure C-4   Serial Bit Stream

Typical synchronous receiver units are placed in a sync search mode by either hardware or software whenever a transmission begins, or whenever a data dropout has occurred and the hardware or software determines that resynchronization is necessary.

Synchronization is accomplished by the hardware shifting eight bits into a shift register and comparing those eight bits (as a parallel word) to the sync character which has been set in a register. If a match occurs, the receiver begins shifting in bits and raising a "character available" flag every eight bits. If no match is realized, the receiver shifts in a new bit from the line, shifts all bits recorded to date (thus shifting the oldest bit off the end), and does a new parallel comparison to the sync character. The process continues until the sync character is framed.

To decrease the probability that a receiver will synchronize on a bit combination that is not the intended sync character but rather a combination of other characters, synchronous receivers are frequently arranged to synchronize on two successive sync characters.

D.1 DDCMP

DDCMP (Digital Data Communications Message Protocol) was developed to provide full-duplex message transfer over existing standard hardware.

D.1.1 Controlling Data Transfers

The DDCMP message format is shown in Figure D-1. A single control character is used in a DDCMP message and is the first character in the message. Three control characters are provided in DDCMP to differentiate between the three possible types of messages:

    SOH – data message follows
    ENQ – control message follows
    DLE – bootstrap message follows

Note that the use of a fixed-length header and message size declaration obviates the requirement for extensive message and header delimiter codes.

SYN	SYN	SOH	COUNT 14 BITS	FLAG 2 BITS	RESPONSE 8 BITS	SEQUENCE 8 BITS	ADDRESS 8 BITS	CRC-1 16 BITS	DATA (ANY NUMBER OF 8-BIT CHARACTERS UP TO 2_{14})	CRC-2 16 BITS
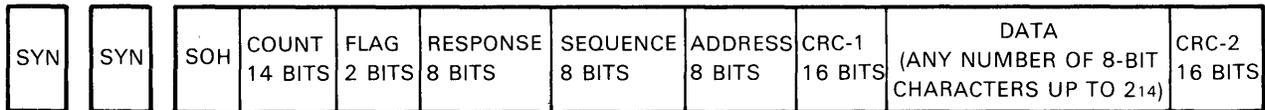
MK-0827

Figure D-1   DDCMP Data Message Format

Figure D-2 shows a simple example of data exchange.

D.1.2 Error Checking and Recovery

DDCMP uses CRC-16 for detecting transmission errors. When an error occurs, DDCMP sends a separate NAK message. DDCMP does not require an acknowledgement message for all data messages. The number in the response field of a normal header or in either the special NAK or ACK message specifies the sequence number of the last good message received. For example, if messages 4, 5, and 6 have been received since the last time an acknowledgement was sent and message 6 is bad, the NAK message specifies number 5 which says "message 4 and 5 are good and 6 is bad." When DDCMP operates in full-duplex mode, the line does not have to be turned around; the NAK is simply added to the sequence of messages for the transmitter.

DMC #1

① SENDS A STRT (START) MESSAGE WHICH
MEANS: "I WANT TO BEGIN SENDING DATA
TO YOU AND THE SEQUENCE NUMBER OF MY
FIRST MESSAGE WILL BE 1."

DMC #2

② SENDS A STRT (START) MESSAGE WHICH
MEANS: "I WANT TO BEGIN SENDING DATA
TO YOU AND THE SEQUENCE NUMBER OF MY
FIRST MESSAGE WILL BE 1."

③ RECEIVES STRT MESSAGE.

④ SENDS A STACK (START ACKNOWLEDGE)
MESSAGE WHICH MEANS: "OK WITH ME."

⑤ RECEIVES STACK.

⑥ SENDS DATA MESSAGES WITH A RESPONSE FIELD
SET TO 0 AND THE SEQUENCE FIELD SET TO 1.
WHICH MEANS: "I AM LOOKING FOR YOUR
MESSAGE 1." OTHER MESSAGES MAY BE SENT
AT THIS TIME (I.E., MESSAGES 2, 3, ETC.)
WITHOUT WAITING FOR A RESPONSE.

⑦ RECEIVES DATA MESSAGE 1 AND CHECKS IT FOR
SEQUENCE AND CRC ERRORS. IF THERE IS A
SEQUENCE ERROR, GO TO 12. IF THERE IS NO
ERROR, GO TO 9.

⑧ A CRC ERROR WAS DETECTED. COMPUTER B
SENDS A NAK MESSAGE WITH THE RESPONSE
FIELD SET TO 0. WHICH MEANS: "ALL MESSAGES
UP TO 0 (MODULO 256) HAVE BEEN ACCEPTED
AND MESSAGE 1 IS IN ERROR."

⑨ COMPUTER A RECEIVES NAK, RETRANSMITS.
MESSAGE 1 AND ANY OTHER MESSAGES SENT
SINCE (I.E., 2, 3, ETC.) IF ALREADY SENT.

⑩ SENDS ACK RESPONSE OF 1 EITHER IN A
SEPARATE ACK MESSAGE OR IN THE RESPONSE
FIELD OF A DATA MESSAGE.

⑪ RECEIVES ACK AND RELEASES MESSAGE 1.

⑫ CONTINUES SENDING MESSAGES.

⑬ DISCARD MESSAGE AND WAIT FOR PROPER
MESSAGE 2.

⑭ TIMES OUT DUE TO LACK OF RESPONSE
FOR MESSAGE 2. SENDS A REPLY FOR
MESSAGE 2.

⑮ SEND NACK RESPONSE OF 1 IN THE
RESPONSE FIELD.

⑯ RETRANSMITS MESSAGE 2 AND
FOLLOWING MESSAGES

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Figure D-2   DDCMP Sample Handshaking Procedure

When a sequence error occurs in DDCMP, the receiving station does not respond to the message. The transmitting station detects, from the response field of the messages it receives (or via timeout), that the receiving station is still looking for a certain message and sends it again. For example, if the next message the receiver expects to receive is 5, but receives 6 instead, the receiver will not change the response field (which contains a 4) of its data messages. The receiver will say, "I accept all messages up through message 4 and I'm still looking for message 5."

D.1.3 Character Coding

DDCMP uses ASCII control characters for SYN, SOH, ENQ and DLE. The remainder of the message, including the header, is transparent.

D.1.4 Data Transparency

DDCMP defines transparency by use of a count field in the header. The header is of fixed length. The count in the header determines the length of the transparent information field, which can be 0 to 16,383 bytes long. To validate the header and count field, it is followed by a CRC-16 field; all header characters are included in the CRC calculation. Once validated, the count is used to receive the data and to locate the second CRC-16, which is calculated on the data field. Thus, character stuffing is avoided.

D.1.5 Data Channel Utilization

DDCMP uses either full- or half-duplex circuits at optimum efficiency. In the full-duplex mode, DDCMP operates as two dependent one-way channels, each containing its own data stream. The only dependency is the acknowledgements which must be sent in the data stream in the opposite direction.

Separate ACK messages are unnecessary, reducing the control overhead. Acknowledgements are simply placed in the response field of the next message for the opposite direction. If several messages are received correctly before the terminal is able to send a message, all of them can be acknowledged by one response. Only when a transmission error occurs or when traffic in the opposite direction is light (no data message to send) is it necessary to send a special NAK or ACK message, respectively.

In summary, DDCMP data channel utilization features include:

1. The ability to run on full- or half-duplex data channel facilities.

2. Low control character overhead.

3. No character stuffing.

4. No separate ACKs when traffic is heavy; this saves on extra SYN characters and inter-message gaps.

5. Multiple acknowledgements (up to 255) with one ACK.

6. The ability to support point-to-point and multipoint lines.

D.2 PROTOCOL DESCRIPTION

DDCMP is a very general protocol; it can be used on synchronous or asynchronous, half- or full-duplex, serial or parallel, and point-to-point or multipoint systems. Most applications involving protocols are half- or full-duplex transmission in a serial synchronous mode; that operating environment will therefore be emphasized in this description.

The header is the most important part of the message, because it contains the message sequence numbering information and the character count, the two most important features of DDCMP. Because of the importance of the header information, it merits its own CRC block check, indicated in Figure D-3 as CRC 1. Messages that contain data, rather than just control information, have a second section which contains any number of 8-bit characters (up to a maximum of 16,363) and a second CRC (indicated in Figure D-3 as CRC 2).

Before the message format is discussed in greater detail, the message sequencing system should be explained because most of the header information is directly or indirectly related to the sequencing operation.

In the DDCMP, any pair of stations that exchange messages with each other number those messages sequentially starting with message number 1. Each successive data message is numbered using the next number in sequence, modulo 256. Thus, a long sequence of messages would be numbered 1,2,3,...254,255,0,1,... The numbering applies to each direction separately. For example, station A might be sending its messages 6,7,8 to station B, while station B is sending its messages 5,6,7 to station A. Thus, in a multipoint configuration where a control station is engaged in two-way communication with 10 tributary stations, there are 20 different message number sequences involved – one sequence for messages from each of the 10 tributaries to the control station and one sequence for messages from the control station to each of the 10 tributaries.

Whenever a station transmits a message to another station, it assigns its next sequential message number to that message and places that number in the sequence field of the message header. In addition to maintaining a counter for the sequentially numbered messages which it sends, the station also maintains a counter of the message numbers received from the other station. It updates that counter whenever a message is received with a message number exactly one higher than the previously received message number. The contents of the received message counter are included in the response field of the message being sent, to indicate to the other station the highest sequenced message that has been received.

When a station receives a message containing an error, that station sends a negative acknowledge (NAK) message back to the transmitting station. DDCMP does not require an acknowledgement for each message, as the number in the response field of a normal header (or in either the special NAK or positive acknowledgement message ACK) specifies the sequence number of the last good message received. For example, if messages 4,5, and 6 have been received since the last time an acknowledgement was sent, but message 6 is bad, the NAK message specifies number 5 which says "messages 4 and 5 are good and 6 is bad." When DDCMP operates in the full-duplex mode, the line does not have to be turned around; the NAK is simply added to the messages for the transmitter.

When a station receives a message that is out of sequence, it does not respond to that message. The transmitting station will detect this from the response field of the messages which it receives; if the reply wait timer expires before the transmitting station receives an acknowledgement, the transmitting station will send a REP message. The REP message contains the sequence number of the most recent unacknowledged message sent to the distant station. If the receiving station has correctly received the message referred to in the REP message (as well as the messages preceding it), it replies to the REP by sending an ACK. If it has not received the message referred to in sequence, it sends a NAK containing the number of the last message that it did receive correctly. The transmitting station will then retransmit all data messages after the message specified in the NAK.

The numbering system for DDCMP messages permits up to 255 unacknowledged messages outstanding, a useful feature when working on high delay circuits such as those using satellites.

| SYN | SYN | | CLASS | COUNT 14 BITS | FLAG 2 BITS | RESPONSE 8 BITS | SEQUENCE 8 BITS | ADDRESS 8 BITS | CRC 1 16 BITS | INFORMATION ANY NUMBER OF 8-BIT CHARACTERS | CRC 2 16 BITS |

NOTE 6   *NOTE 2*   *NOTES 3,4*   *NOTE 5*

→ NOTE 1

		XXXXXXXX	XXXXXXXXXXXXXX	XX	XXXXXXXX	XXXXXXXX	XXXXXXXX
SOH – DATA MESSAGES		10000001	CHARACTER COUNT	QS	RESP #	MESSAGE#	ADDRESS
ENQ { ACKNOWLEDGEMENT		00000101	00000001000000	QS	RESP #	00000000	ADDRESS
NEGATIVE ACKNOWLEDGE		00000101	00000010--------	QS	RESP #	00000000	ADDRESS

REASONS:			
	BCC HEADER ERROR	000001	
	BCC DATA ERROR	000010	
	REP RESPONSE	000011	
	BUFFER UNAVAILABLE	001000	
	RECEIVER OVERRUN	001001	
	MESSAGE TOO LONG	010000	
	HEADER FORMAT ERROR	010001	

ENQ { REPLY MESSAGE		00000101	00000011000000	QS	00000000	LSTMESS#	ADDRESS
START MESSAGE		00000101	00000110000000	11	00000000	00000000	ADDRESS
START ACKNOWLEDGEMENT		00000101	00000111000000	11	00000000	00000000	ADDRESS
DLE MAINTENANCE MESSAGE		10010000	CHARACTER COUNT	11	00000000	00000000	ADDRESS

NOTES:

1. ONLY THE DATA MESSAGE AND THE MAINTENANCE MESSAGE HAVE CHARACTER COUNTS, SO ONLY THESE MESSAGES HAVE THE INFORMATION AND CRC2 FIELDS SHOWN IN THE MESSAGE FORMAT DIAGRAM ABOVE.

2. "RESP-#" REFERS TO RESPONSE NUMBER. THIS IS THE NUMBER OF THE LAST MESSAGE RECEIVED CORRECTLY. WHEN USED IN A NEGATIVE ACKNOWLEDGE MESSAGE, IT IS ASSUMED THAT THE NEXT HIGHER NUMBERED MESSAGE WAS NOT RECEIVED, WAS RECEIVED WITH ERRORS, OR WAS UNACCEPTED FOR SOME OTHER REASON. SEE "REASONS."

3. "MESSAGE#" IS THE SEQUENTIALLY ASSIGNED NUMBER OF THIS MESSAGE. NUMBERS ARE ASSIGNED BY THE TRANSMITTING STATION MODULO 256; I.E., MESSAGE 000 FOLLOWS 255.

4. "LSTMESS#" IS THE NUMBER OF THE LAST MESSAGE TRANSMITTED BY THE STATION. SEE THE TEXT DISCUSSION OF REP MESSAGES.

5. "ADDRESS" IS THE ADDRESS OF THE TRIBUTARY STATION IN MULTIPOINT SYSTEMS AND IS USED IN MESSAGES BOTH TO AND FROM THE TRIBUTARY. IN POINT TO POINT OPERATION, A STATION SENDS THE ADDRESS "1" BUT IGNORES THE ADDRESS FIELD ON RECEPTION.

6. "Q" AND "S" REFER TO THE QUICK SYNC FLAG BIT AND THE SELECT BIT. SEE TEXT.

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Figure D-3   DDCMP Message Format in Detail

D.3 MESSAGE FORMAT

With the above background, it is now time to explore the various DDCMP message formats in full detail, as shown in Figure D-3. The first character of the message is the class of message indicator, represented in ASCII with even parity. There are three classes of messages: data, control, and maintenance. These are indicated by class of message indicators SOH, ENQ, and DLE respectively. The next two characters of the message are broken into a 14-bit field and a 2-bit field. The 14-bit field is used in data and maintenance messages to indicate the number of characters that will follow the header and form the information part of the message. In control messages, the first 8 bits of the 14-bit field are used to designate what type of control message it is; the last 6 bits are generally filled up with zeros. The exception is in NAK messages where the last six bits are used to specify the reason for the NAK. The 2-bit field contains the quick sync and select flags.

The quick sync flag is used to inform the receiving station that the message will be followed by sync characters; the receiver may wish to set its associated synchronous receiver hardware into sync search mode and sync strip mode. This will re-establish synchronization and syncs will be discarded until the first character of the next message arrives. The purpose of this is to permit the receiving station to engage any hardware sync-stripping logic it might have and prevent it from filling its buffers with sync characters. The select flag is used to indicate that this is the last message which the transmitting station is going to transmit and that the addressed station is now permitted to begin transmitting. This flag is useful in half-duplex or multipoint configurations, where transmitters need to get turned on and off.

The response field contains the number of the last message correctly received. This field is used in data messages and in the positive and negative acknowledge types of control message. Its function should be evident from the preceding discussion of sequence control.

The sequence field is used in data messages and in the REP type of control message. In a data message, it contains the sequence number of the message as assigned by the transmitting station. In a REP message, it is used as part of the question, "Have you received all messages up through message number (specify) correctly?"

The address field is used to identify the tributary station in multipoint systems and is used in messages both to and from the tributary. In point-to-point operation, a station sends address 1, but ignores the address field on reception.

In addition to the positive and negative acknowledgement and REP types of control message, there are also start and start acknowledge control messages. These are used to place the station which receives them in a known state. In particular, they initialize the message counters, timers, and other counters. The start acknowledge message indicates that this has been accomplished.

Figure D-3 also shows the maintenance message. This is typically a bootstrap message containing load programs in the information field. A complete treatment of bootstrap messages and start up procedures is beyond the scope of this book.

NOTE
Refer to the *DDCMP Specification Order* **(No. AA-D599A-TC) for a complete detailed description of DDCMP.**

APPENDIX E
DDCMP BLOCK CHECK COMPUTATION

E.1 DDCMP ERROR DETECTION
Error detection is provided in this protocol by block check bytes after each of the message headers and message blocks. This block check consists of computing a 16-bit cyclic redundancy check using a polynomial known as the CRC-16 polynomial and appending the check bits computed to each block. This polynomial and scheme have been widely used in BiSync and other protocols.

E.2 THE CRC-16 POLYNOMIAL
The CRC-16 polynomial $[X^{16} + X^{15} + X^2 + 1 = (X + 1) * (X^{15} + X + 1)]$ (see Section E.3) has the following error detection properties:

1. It will detect all errors that change an odd number of bits (that is, 1, 3, 5, ... bit errors).

2. It will detect all errors that change 2 bits, provided that the block length is less than 32767 bits (including the CRC bits). Thus, the maximum count (length of data field) should be 4093.

3. It will detect all errors that consist of a single burst error of 16 or fewer bits. A burst error is a group of bits in which the first bit and the last bit are in error and the intervening bits may or may not be in error. A 16-bit burst error might have as many as 16 bits in error. The partitioning of bits in error into burst errors is not unique.

4. It will detect all errors that consist of two occurrences of two adjacent bits in error, provided that the block length is less than 32767 bits including the CRC bits.

5. It will detect all except the fraction $1/2^{15}$ of errors that consist of a single burst error of 17 bits.

6. It will detect all except the fraction $1/2^{16}$ of errors that consist of a single burst error of 18 or more bits.

7. It will not detect some errors that change 4 bits. For example, it will not detect the error pattern that is identical to the CRC polynomial. Thus the minimum hamming distance between two valid messages (including the CRC bits) is 4 bits.

E.3 CRC COMPUTATION
The algorithm for computing the CRC is as follows:

1. Consider the header or data portion of the message as it appears on a serial line (LSB of the first byte first, MSB of the final byte last) and append 16 zeros after the header or data.

2. Take the string of bits constructed in 1, and treat each bit as the coefficient of a term of a polynomial with the LSB of the first byte being the coefficient of the highest order polynomial term. The highest order term is $A * X^{63}$ for a header block and $A * X^{(8 * <count> + 15)}$ for a data block where A is the least significant bit of the first byte of the header or data. The lowest order term is $0 * X^0$ for both cases.

3. Divide the polynomial constructed in 2 by the CRC-16 polynomial $X^{16} + X^{15} + X^2 + 1$, using synthetic division and module 2 arithemtic on the coefficients (that is, addition = subtraction = XOR. All carries and borrows are ignored) obtaining a quotient that is discarded and a 16-bit remainder.

   Transmit the coefficients of the remainder as the block check bytes following the original message bits, transmitting the coefficients of the highest order term (X^{15}) first. Thus, the first byte represents coefficients of the X^8 through X^{15} terms of the remainder (from left to right) and the second byte represents coefficients of the X^0 through X^7 terms of the remainder (also from left to right).

4. On reception, perform the same algorithm and compare the received block check bytes with the computed block check bytes. If the bytes are not identical, an error has occurred.

NOTE

1. On a parallel circuit, the same algorithm is used and the same block check bytes are computed, although the bytes are sent in parallel instead of serially. Notice that for the purposes of the block check byte computation, the LSB of the first byte is always treated as the highest order term (that is, the term with the largest exponent) in the message polynomial.

2. On reception, the message may be handled with the block check bytes included (two bytes longer) and the algorithm computed based on this longer message. If the remainder is not zero, an error has occurred.

Interprocessor test programs DZITA ITEP monitor and DZDMO ITEP DMC11 overlay provide the capabilities to check out the communications link (refer to Appendix G, Link Test) and to test the ability of the DMC11 to perform both Remote Load Detect and down-line load.

F.1 REMOTE LOAD DETECT

Remote Load Detect (RLD) is also referred to as unattended system control in Maintenance Operation (MOP) mode specifications (Spec. No. AA-D60ZA-TC). Unattended system control is defined as follows:

The Enter MOP Mode message is used to control an unattended system. This message, together with the appropriate hardware, enables a satellite computer to halt current operation and begin operating in either the MOP primary or secondary mode. This is accomplished by transferring control to a resident MOP program or bootstrap. The hardware is used to recognize this message and force the computer system to transfer control to the MOP program, usually residing in a read-only memory. The password in this message protects the system from being controlled and loaded by an unauthorized host. Only messages with a matching password will cause the system to enter MOP mode.

F.2 DMC11 SETUP FOR REMOTE LOAD DETECT

F.2.1 DMC11 Addressing

When using the DMC11 with a bootstrap module (M9301-YJ), the DMC must be addressed according to the rules for floating address assignment. These rules are outlined in the installation section of this manual. If the address is not set correctly, the (M9301-YJ) will not find the DMC and neither manual booting of the DMC nor an RLD works.

F.2.2 DMC11 Line Unit Setup

DMC11 line units (M8201 and M8202), switch packs No. 2 and No. 3 must be properly set when DMC11 is to be used with a bootstrap module such as the M9301-YJ.

This combination is used in applications where RLD and subsequent down-line loading are required.

Setup of switch packs No. 2 and No. 3 is only required at the end of the link (satellite station) where the M9301-YJ is installed.

Switch pack No. 2 (E87 on M8201 and E90 on M8202) is set up to contain the 8-bit password specified by the operating system.

- Switch No. 1 is the MSB, switch No. 8 is the LSB.

- Set switches off for a 1.

- All switches off (SP2 = 377) inhibits RLD operation.

Switch pack No. 3 (E88 on M8201 and E91 on M8202) is set to the low order 8 bits of the bootstrap entry point (offset).

- Switch No. 1 is the MSB, switch No. 8 is the LSB

NOTE
**Switch No. 8 represents bit 0 of the boot address and
should be set to 0.**

- Set switches off for a 1.

- Setting for current M9301-YJ code should be 356 (octal) for booting unit 0 and 374 (octal) for booting unit 1.

NOTE
**The bootstrap entry point (offset) may be different
for bootstrap ROM modules other than the M9301-
YJ.**

F.3 PROCEDURE TO TEST REMOTE LOAD DETECT UNDER ITEP

Down-line load should not be attempted unless the DMC11 link has been checked out successfully using the link test under DMC11 ITEP. The following are the switch settings required on the M9301-YJ and DMC11 line unit (M8202 or M8201) when using ITEP.

NOTE
**The M9301-YJ must have both the power-up boot
and diagnostics disabled.**

MODULE/SWITCH	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10
SP2 M8201/E87 M8202/E90	ON	ON	ON	ON	ON	ON	ON	ON		
SP3 M8201/E88 M8202/E91	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON		

In this mode, the originating station (the one running ITEP) will send an Enter MOP message to the boot station (the one with M9301-YJ) and initiate a down line load. Successfully down-line loaded, the boot station will print out a boot complete message. See events for RLD under ITEP which follow the setup requirements below.

1. Set the Enable/Halt switch on the console of the boot station to enable position. If the boot station is a PDP-11/34 or PDP-11/04, press Init (followed by CNTL HALT when using KY11-LB).

2. Under ITEP at the originating station:

    - Modify parameter No. 1 to 400

    - Modify parameter No. 2 to 0

- Deposit 1004 to console switch register

- Type (CR)

The automatic mode bootstrap test should then complete and print out end pass message.

Events for RLD Under ITEP (See Figure F-1)

1. At CPU No. 1, ITEP steps up DMC11, then assigns Enter MOP Mode (MOP 6) message.

NOTE
Scope the serial line on DMC11 No. 2 to see if there
is any message arriving every ten seconds.

2a. At CPU No. 2, DMC11 No. 2 compares MOP 6 message received to password setup in line unit switch pack No. 2.

b. If all passwords matched, DMC11 No. 2 writes 173000 plus the contents of switch pack No. 3 on line unit to location 24, clears location 26, and asserts AC LO on the UNIBUS.

NOTE
Load 125252 into locations 24 and 26. These two lo-
cations should be modified if 2.b is occurring.

Scope AC LO on CPU No. 2 to see if it is pulsing
because 2.b is occurring.

c. CPU No. 2 program control is transferred to DMC11 boot code in the ROM boot (M9301-YJ type). The correct entry into boot code must be set up in line unit switch pack #3 which contains offset added to 173000.

d. The DMC11 boot code sets up the DMC11 and sends a Request Secondary Boot (MOP 8) message.

3. At CPU No. 1, ITEP checks receipt of MOP 8 message and transmits a memory load with Transfer Address (MOP 0) message.

4a. At CPU No. 2, the ROM boot receives MOP 0 and transfers program control to location 6.

b. The down-line loaded program is then executed and a Boot Complete message is printed at the console terminal.

NOTE
1. The above procedure will set the password for
down line load to 0. This password is deter-
mined by the switch (SP2) settings on
M8201/E87 or M8202/E90 at the boot sta-
tion or remote station. When doing down-line
load with software, the password used by soft-
ware must match the password selected on the
DMC11 line unit at remote station; in this
case password is 0.

HOST	LINK ACTION	REMOTE NODE

HOST INITIATES DOWN-LINE LOAD BY SETTING DMC INTO MAINT. MODE WITH CNTRL I AND SENDS A MOP 6 MSG. THE PASSWORD IN MOP 6 MSG. MUST EQUAL THAT OF THE REMOTE NODE.

MOP 6 MESSAGE →

DMC-11 RECEIVES MOP 6 MSG. AND CHECKS PASSWORD. IF EQUAL, DMC-11 TRIES TO DO AN NPR TO LOCATION 24 WITH BOOT ADDRESS FROM THE SWITCH PACK ON THE LINE UNIT.(ADDRESS = DMC-11 CODE IN M9301-YJ)

DMC-11 ALSO CLEARS LOC. 26. NOW DMC-11 ASSERTS AC LO TO TRAP CPU TO LOC.24 TO JUMP TO M9301-YJ CODE. THE M9301-YJ INITIALIZES THE DMC TO MAINT. MODE AND ASSIGNS A RECEIVE BUFFER AT LOC.0 WITH CHARACTER COUNT EQUAL TO 7774. THE M9301-YJ THEN TRANSMITS A MOP 8 MSG. TO THE HOST. IF NPR WAS UNSUCCESSFUL, THEN WHEN AC LO WAS ASSERTED, THE CPU SHOULD HAVE TRIED TO EXECUTE WHAT-EVER WAS IN LOC.24 AND SHOULD START RUNNING. NOW A SECOND NPR TO LOC.24 & 26 OCCURS FOLLOWED BY A SECOND ASSERTION OF AC LO. THIS SECOND SEQUENCE WILL START THE CPU IF NO HARDWARE FAILURE IS AT FAULT.

← MOP 8 MESSAGE

HOST CHECKS FOR MOP 8 MSG. AND WHEN RECEIVED TRANSMITS A MOP 0 MSG. TO THE REMOTE NODE.
NOTE: MOP 0 MSG. MUST BE A SELF STARTING MSG. AT LOCATION 6 AND IF MORE THAN ONE LOAD IS REQUIRED IT MUST ALSO BE ABLE TO SEND A REQUEST FOR A TERTIARY BOOT MSG. BACK TO THE HOST CPU FOR MUTLIPLE LOADS.

MOP 0 MESSAGE →

MOP 0 MSG. RECEIVED.SAME SEQUENCE AS FOR REMOTE NODE REQUEST, SEE MOP 0 ON THE FLOW CHART (FIGURE F-2).

MOP 6 MSG.=	CODE	4 BYTES EQUAL TO SYSTEM PASSWORD(PASSWORD=0 FOR ITEP)			
	6	PASSWORD	PASSWORD	PASSWORD	PASSWORD

MOP 8 MSG=	CODE	DEVICE TYPE	MOP VERIFY	PROGRAM TYPE	
	8	DMC= 12	1	0 SECONDARY LOADER	

MOP 0 MSG=	CODE	LOAD#	LOAD ADDRESS 4 BYTES				PROGRAM IMAGE	TRANSFER ADDRESS			
	0	0	0	0	0	0	DATA	0	0	6	0
MEMORY ADRS.	0	1	2	3	4	5	6				

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Figure F-1 Down Line Load To Remote Node Using Remote Load Detect

2. For automatic boot (RLD, on successful recognition of the Enter MOP message the remote DMC11 will NPR PC and PS to locations 24 and 26 respectively and then it will assert AC LO. Switch (SP No. 3) setting in the events sequence sets the bootstrap entry point (offset) to 356 for booting DMC11 unit 0.

3. On 11/40, 45, 70, the AC LO asserted by the DMC11 will cause the CPU to assert DCLO. The setting of M9301-YJ SW2 to OFF, prevents the M9301 from attempting to take control of the address bits during the simulated power-up.

4. In order to verify switches SP2 and SP3 on the line unit, run any DMC11 diagnostics. The STAT2 under the MAP OF DMC11 STATUS will give the actual set up of the switches.

STAT2: Low byte (bits 7-0) = SP2
(PASSWORD)
High byte (bits 15-8) = SP3
(BOOT OFFSET)

F.4 PROCEDURE TO TEST DOWN-LINE LOAD UNDER ITEP
The down-line load should not be attempted unless the DMC11 link has been checked out successfully, using the link test under DMC11 ITEP.

In this mode, the operator at the boot station has to do a boot to M9301-YJ at the entry point for DMC11 boot code which sends a Request Secondary Boot message to the originating station. (See Figure F-2).

The originating station running ITEP in bootstrap mode then replies with a Memory Load with Transfer Address message.

The boot station executes that program and prints out a Boot Complete message.

Procedure:

1. Under ITEP at the originating station,

   a. Modify parameter No. 1 to 2400

   b. Modify parameter No. 2 to 0

   c. Deposit 1004 in Console Switch Register

   d. Type <CR>

HOST   LINK ACTION   REMOTE NODE

INITIATE REQUEST FOR
SECONDARY BOOT MESSAGE.
1. TYPE XM,
2. LOAD ADDRESS 773356
   or 773374 UNIT 1.
3. DEPRESS CONSOLE BOOT
   SWITCH IF M9301-YJ
   SWITCH PACK IS SET
   TO ADDRESS 773356
   OR 773374 UNIT 1.

MOP 8 MESSAGE

DMC-11 RECEIVES SECONDARY
BOOT MSG. AND INFORMS
CPU THAT A MAINT. MSG.
WAS RECEIVED. DMC MUST
NOW BE INITIALIZED AND
THE CNTRL I FORMAT MUST
SET MAINT. MODE AND
TRANSMIT THE MOP 0 MSG.
TO THE REMOTE NODE.
NOTE: MOP MSG. 0 MUST
NOTE: MOP MSG. 0 MUST BE
A SELF STARTING MSG. AT
LOCATION 6 AND IF MORE
THAN ONE LOAD IS REQUIRED
IT MUST ALSO BE ABLE TO
SEND A REQUEST FOR A
TERTIARY BOOT MSG. BACK
TO THE HOST CPU FOR
MULTIPLE LOADS.

NOTE: ADDRESSES ABOVE
SELECT DMC-11 UNIT 0 & 1
RESPECTIVELY WITHOUT
DIAGNOSTICS ENABLED. IF
ONLY DOING BOOT REQUEST
FROM THIS REMOTE NODE
THEN DIAGNOSTIC'S ENABLE
ADDRESS CAN BE USED.
(773354 & 773372 RESP).
ANY OF THE ABOVE PUTS
THE M9301-YJ CODE TO
SEND A MOP 8 MSG VIA
THE DMC-11 LINK.

M9301-YJ CHECKS FOR MOP 0
MSG. AND STARTS LOADING
AT LOCATION 0,WHEN
DONE LOADING, THE M9301-YJ TRANSFERS
STARTING ADDRESS OF 6
FROM M9301-YJ TO START
MOP 0 MSG. (SECONDARY BOOT
REQUEST MSG. COMPLETED.)
MOP 0 MSG. MUST NOW REQUEST
TERTIARY LOADER, IF
NECESSARY FOR MORE DATA
TO BE LOADED.
NOTE: MAX DATA/MSG. IS 8K
WORDS OR 16K BYTES.

MOP 0 MESSAGE

MOP 8 MSG=	CODE	DEVICE TYPE	MOP VERIFY	PROGRAM TYPE
	8	DMC= 12	1	0 SECONDARY LOADER

MOP 0 MSG.=	CODE	LOAD#	LOAD ADDRESS 4 BYTES				PROGRAM IMAGE	TRANSFER ADDRESS			
	0	0	0	0	0	0	DATA	0	0	6	0
MEMORY ADDRESS	0	1	2	3	4	5	6				

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Figure F-2 Remote Node Request for Down-Line Load Flowchart

2. At the boot station, boot the M9301-YJ via one of the following methods,

a. Type XM under the console emulator

b. Load address 773356 and start

c. On the PDP-11/04 and PDP-11/34, when switch setting on the M9301-YJ is set up to boot the DMC11, a control boot to KY11-LB initiates the boot to the DMC11. This may take two control boots to occur with KY11-LB (CNTRL BOOT/CNTRL HALT/CNTRL BOOT).

NOTE
Refer to the M9301-YJ manual for proper switch setting in each case.

Upon successful completion of a down-line load, the terminal at the boot station prints out a Boot Complete message.

G.1 ABSTRACT

ITEP (Interprocessor Test Program) is designed as a maintenance aid to verify the proper operation of a complete communication link from one PDP-11 system to another or to a communication test center (for remote applications). To run ITEP to check out a DMC11 communication link, an ITEP monitor (DZITA) and DMC11 ITEP overlay (DZDMO) are required. Under ITEP, an additional feature called Remote Load Detect (RLD) can also be checked out.

NOTE
The RLD checkout procedure is described in Appendix F.

G.2 REQUIREMENTS

- PDP-11 system with at least 4K words of memory.

- DMC11 communication interface.

- Another PDP-11 system with DMC11.

G.3 PROGRAM LOADING PROCEDURE

The DZITA monitor and DMC11 ITEP overlay (DZDMO) are in absolute format and can be loaded under an absolute loader, XXDP monitor, or can update two utility programs in the following order.

- ITEP monitor DZITA

- DMC11 ITEP overlay DZDMO

G.4 OPERATING PROCEDURES FOR LINK TEST

For detailed operating procedures, refer to the DZDMO listings. The following inputs are required to run ITEP.

ITEP Questions	Operator Reply
INTERFACE TYPE DMC?	CR carriage return
BUS ADDRESS = 160010?	DMC11 CSR Address CR
VECTOR ADDRESS = 000300?	DMC11 Vector Address CR
PRIORITY = 000240?	CR for BR5
PARAMS #1 = 000000?	CR for Link Test

PARAMS #2=000001?   {   CR for Full Duplex

                          OCR for Half Duplex

Set Switches   1.   Select mode of operation by referring to Table G-1 and set
                            up CPU Console Switch Register.

                      2.   CR to proceed.

G.4.1 MODE Selection

Three standard messages are selectable by an operator via console switches SW10 and SW9 as follows:

SW10	SW9	Data Selected
0	0	Get data from the operator.
0	1	$A THE QUICK BROWN FOX JUMPED OVER THE LAZY DOG.
1	0	$B 0123456789
1	1	$C COM-TEST MAYNARD THE QUICK BROWN FOX JUMPED OVER THE LAZY DOG 0123456789

ITEP has four modules selectable by Console Switch Register SW0-3. The overlay performs the following functions in the four modes.

Internal Loopback Mode

1. Establishes the modem connection.

2. Waits to receive a message terminated by the receive terminating character (001).

3. Verifies the data against the data selected by SW09 and SW10 (SW07=0).

4. Transmits the data selected by SW09 and SW10 (SW08=0), or transmits the received data (SW08=1).

5. Returns to monitor for END PASS (SW04=1) or goes to step 1 (SW04=0).

Example:

To select message number 3 ($C COM-TEST....) and return to the monitor for the end pass in Internal Loopback Mode, the switch setting should be 3030 or 3430.

External Loopback Mode

1. The overlay establishes the modem connection.

2. Transmits the selected data.

3. Enables the receiver.

4. Waits for the message to be received.

G-2

5. Verifies the data (SW07=0).

6. Returns to the monitor for END PASS (SW04=1) or goes to step 1 (SW04=0).

Example:

To select message number 3 ($C COM-TEST.....) and return to the monitor for the end pass in External Loopback Mode, the switch setting should be 3024.

One-Way-In Mode

1. The overlay establishes the modem connection.

2. Enables the receiver.

3. Waits for the message to be received.

4. Verifies the data (SW07=0).

5. Returns to the monitor for END PASS (SW04=1) or goes to step 1 (SW04-0).

Example:

To select message number 3 ($C COM-TEST.....) and return to the monitor for the end pass in One-Way-In mode, the switch setting should be 3022.

One-Way-Out Mode

1. The overlay establishes the modem connection.

2. Enables the transmitter.

3. Transmits the selected data.

4. Returns to monitor for END PASS (SW04=1) or goes to step 1 (SW04=0).

Example:

To select message number 3 ($C COM-TEST.....) and return to the monitor for the end pass in One-Way-Out mode, the switch setting should be 3021.

G.4.2 Starting ITEP
ITEP requires a complete communications loop. Ensure that a loop is established with compatible equipment. The variable parameters must be the same in each of the two processors. The mode must be one of the options listed in Table G-2. The system that is to receive data first should be loaded and started first. If the modem being used on this system has an automatic answer feature, it should be enabled. The system that is to transmit first should then be loaded and the connection established.

The load address is 200. Refer to the program listing for details regarding restrictions, error messages, and optional selections.

Table G-1 Operational Switch Setting

SW15=1 HALT ON ERROR
SW14=1 SINGLE PASS
    SW14 HAS NO EFFECT IF SW04=0
SW13=1 INHIBIT ERROR TYPEOUTS
SW12=1 INHIBIT ALL TYPEOUTS EXCEPT ERRORS
    IF SW12=0 AND SW04=1 END PASS IS TYPED
    AND TRANSMITTED/RECEIVED DATA IS TYPED.
SW11=1 USE PREVIOUSLY SPECIFIED DATA
SW10=1 DATA SELECT (WITH SW09)
SW09=1 DATA SELECT (WITH SW10)
    00=1 GET DATA FROM OPERATOR
    01=1 TEST MESSAGE #1 ($A QUICK BROWN FOX)
    10=1 TEST MESSAGE #2 ($B NUMERICS)
    11=1 TEST MESSAGE #3 ($C COMTEST/QUICK BROWN FOX/NUMERICS)
SW08=1 TRANSMIT RECEIVED DATA (INTERNAL LOOPBACK MODE)
SW07=1 DO NOT TEST RECEIVED DATA
SW06=1 MONITOR TRANSMITTED DATA ON CONSOLE TTY.*
SW05=1 MONITOR RECEIVED DATA ON CONSOLE TTY.*
    * IN MANY CASES, NOT ALL DATA WILL APPEAR ON THE CONSOLE
    TTY. THIS IS ESPECIALLY TRUE WHEN THE COMM INTERFACE IS
    RUNNING AT A FASTER RATE (BPS) THAN THE CONSOLE, BUT EVEN AT
    EQUAL OR SLOWER RATES, ALL CHARACTERS MAY NOT APPEAR ON THE
    CONSOLE.
SW04=1 RETURN TO MONITOR FOR END PASS
    WHEN SW04=0 PROGRAM LOOPS IN THE OVERLAY NEVER RETURNING TO
THE MONITOR.
SW03=1 INTERNAL LOOPBACK MODE
SW02=1 EXTERNAL LOOPBACK MODE
SW01=1 ONE-WAY-IN MODE
SW00=1 ONE-WAY-OUT MODE

Table G-2 Valid Mode Combinations

CPU No. 1	CPU No. 2
One-Way-Out	One-Way-In
One-Way-In	One-Way-Out
External Loopback	Internal Loopback
Internal Loopback	External Loopback
External Loopback (full-duplex)	External Loopback (full-duplex)
External Loopback (full-duplex with test connector H3251/H3250 /12-12528 connected at the end of the cable)	

H.1 OVERVIEW

The function of the DZDMH diagnostics is to verify that the DMC11 option performs according to specifications. The diagnostics verify that there are no malfunctions and that all operations of the DMC11 are correct in its environment.

Parameters must be set up to alert the diagnostics to the DMC11 configuration. These parameters are contained in the status table and are generated in two ways: (1) manual input, in which the operator answers questions, and (2) autosizing, in which the program automatically determines the parameters.

DZDMH tests the DMC11-AR and DMC11-AL microprocessors (M8200-YA and M8200-YB) or the KMC11 microprocessor (M8204). Free-running tests are performed. A line unit (M8201 or M8202) must be installed. DZDMH can be used as a heat test diagnostic by manufacturing.

Currently five off-line diagnostics must be run in sequence to detect errors at an early stage. The five diagnostics are:

1. CZDMC – basic W/R and microprocessor tests

2. CZDME – DDCMP Line Unit Test

3. DZDMF – BITSTUFF line unit tests

4. CZDMG – CROM and jump tests

5. DZDMH – free-running tests (heat test tape)

H.2 REQUIREMENTS

H.2.1 Equipment
Any PDP-11 family CPU (except an LSI-11) with a minimum 8K word memory, and console terminal.

DMC11-AR with DMC11-DA or DMC11-FA,
DMC11-AL with DMC11-MA or DMC11-MD.

H.2.2 Storage
The program uses all 8K words of memory except where the absolute loader and bootstrap loader reside. Locations 1500 through 1540 contain the status table. This contains information generated at the start of the diagnostics by manual input (questions) or automatically (autosizing). The status table is an overlay area and should not be altered by the operator.

H.3 LOADING PROCEDURE

H.3.1 Method
All programs are in absolute format and are loaded using the absolute loader.

NOTE
If the diagnostics are on a media such as disk, mag-
tape, DECtape, or cassette, follow the instructions
for the accompanying monitor.

The following table summarizes the absolute loader starting address for each memory size available.

MEMORY SIZE	STARTING ADDRESS
4K	017500
8K	037500
12K	057500
16K	077500
20K	117500
24K	137500
28K	157500

To load programs, perform the following steps:

1. For the memory size available, place the starting address of the absolute loader into the switch register and place the HALT switch in the up position.

2. Press the LOAD ADDRESS key on the console and release.

3. Press the START key on the console and release (the program loads into the CPU).

H.4 STARTING PROCEDURE
To start up the programs, perform the following steps:

1. Set the switch register to 000200.

2. Press the LOAD ADDRESS key and release.

3. Set the switch register as follows:

All bits = 0,   for autosizing

Bit 0 = 1,   for manual input (questions).

Bit 7 = 1,   for using existing parameters set up by a previous start or a previously run DC11 diagnostic.

4. Press the START key and release. The program prints Maindec Name and program nar
    (if this was the first start-up of the program) and also the following:

MAP OF DMC11 STATUS

PC	CSR	STAT1	STAT2	STAT3
001500	160010	145310	177777	000000
001510	160070	145320	177777	000000

The program prints the letter R and proceeds to run the diagnostic. The above example illustrate:
status table starting at address 1500 with information for two DMC11s.

NOTE
**The user must verify the status table if autosizing is
selected.**

Refer to Paragraph H.8.5 for a description of the status table.

If the diagnostic was started with switch zero equal to one, indicating manual parameter input, th
questions are printed requiring operator response. The following is an example of a manual parame
input dialogue. Operator responses are underlined.

HOW MANY DMC11'S TO BE TESTED?1

01
CSR ADDRESS?160010
VECTOR ADDRESS?810
BR PRIORITY LEVEL? (4,5,6,7)?5
DOES MICRO-PROCESSOR HAVE CRAM? (Y OR N)N
WHICH LINE UNIT? IF NONE TYPE "N", IF M8201 TYPE "1", IF M8202, TYPE "2"?)1
IS THE LOOP BACK CONNECTOR ON?Y
SWITCH PAC#1 (DDCMP LINE#)?377
SWITCH PAC#2 (8M873 BOOT ADD)?377

The status map is printed at the end of the dialogue and reflects the answers supplied by the operat
If autosizing is used, the status information must be verified to match the hardware. If it does i
match, the diagnostic must be restarted with switch zero equal to one and the questions answered
the operator.

H.4.1 Control Switch Settings

SW 15 Set: Halt on error

SW 14 Set: Loop On Current Test

SW 13 Set: Inhibit error printout

SW 12 Set: Inhibit type out/label on error

SW 11 Set: Inhibit iterations (quick pass)

SW 10 Set: Escape to next test on error

SW 09 Set: Loop with current data

SW 08 Set: Catch error and loop on it

SW 07 Set: Use previous status table

SW 06 Set: Halt in ROMCLK routine before clocking microprocessor

SW 05 Set: Reserved

SW 04 Set: Reserved

SW 03 Set: Reselect DMC11s desired active

SW 02 Set: Lock on selected test

SW 01 Set: Restart Program at Selected Test

SW 00 Set: Build new status table from questions. If both switches 00 and 07 equal zero, a new status table is built by autosizing.

Switches 06 and 09–15 are dynamic; they can be changed as needed while the diagnostic is running. Switches 00–03 and switch 07 are static; they are used only on starting or restarting the diagnostic.

H.4.1.1 Startup Switch Register Options

SW 01   RESTART PROGRAM AT SELECTED TEST. It is strongly suggested that at least one pass be made before trying to select a test because the program has to clear areas and set up parameters. When this switch is used, the diagnostic will ask, TEST NO.? Answer by typing the number of the test desired followed by a carriage return. This begins execution at the selected test.

SW 02   LOCK ON SELECTED TEST. This switch, when used with switch 01, causes the program to loop constantly on the selected test. Pressing any key on the console lets the program advance to the next test and loop until a key is again pressed. If switch 02 equals zero when switch 01 is used, the program begins at the selected test and continues normal operations.

SW 03   RESELECT DMC11s DESIRED ACTIVE. A message is typed out for setting the switch register equal to the active DMC11s. This means if the system has four DMC11s, bits 00, 01, 02, and 03 are set in location DMACTV from the switch register. Using switch 00 alters that location. Therefore, if four DMC11s are in the system, do not set switches greater than number 03 in the up position; this causes a fatal error. Do not select more active DMC11s than information in the status table.

The method for setting the startup switch register options follows.

1.   Load address 200.

2.   Set switch zero to one. The program types a message.

3.   Set a switch for each DMC desired active. For example, if you have four DMC11s but want to run only the first and the last, set switch register bits 00 and 03 to one. Press CONTINUE. The number (if valid) will be in the data lights (except for the PDP-11/05).

4. Make any other switch settings desired. Press CONTINUE.

H.4.1.2 Dynamic Switches

SW 12: Delete print out/bell on error.

SW 13: Delete error printout.

SW 15: Halt on the error.

SW 08: Go to the beginning of the test (on error).

SW 10: Go to the next test (on error).

The scope switches are listed below.

SW 06: Halt in ROMCLK routine before clocking microprocessor instruction. This allows the operator to scope a microprocessor instruction in the static state before it is clocked. Press CONTINUE to resume running.

SW 09: (If enabled by SCOP1) on an error. If * is printed in front of the test number (example, *TEST NO. 10), SW 09 is incorporated in that test and is therefore recommended for the scope loop (SW 11=0, SW 10=0, SW 09=1, SW 08=0). If SW 09 is not enabled and there is an error (constant), SW 08 is recommended (SW 14=0, SW 10=0, SW 09=0, SW 08=1). For intermittent errors, SW 14=1 will loop on test regardless of error or no error (SW 14=1, SW 10=0, SW 09=0, SW 08=1,0).

SW 11: Inhibit interactions.

SW 14: Loop on current test.

H.4.2 Starting Address
The starting address is at 000200. There are no other starting addresses for the DMC11 diagnostics.

<div align="center">

NOTE
**If address 000042 is nonzero, the program assumes it
is under ACT11 or XXDP control and will act ac-
cordingly after all available DMC11s are tested. The
program returns to XXDP or ACT11.**

</div>

H.5 OPERATING PROCEDURE
When the program is initially started, messages described in Paragraph H.4 are printed. The program then runs the diagnostic.

H.5.1 Program and/or Operator Action
Program and/or operator may be required by the diagnostics. Operator action should be as follows:

1. Halt on error (via SW 15=1) whenever an error occurs.

2. Clear SW 15.

3. Set SW 14 (loop on this test).

4. Set SW 13 (inhibit error printout).

<div align="center">

H-5

</div>

The test number and program counter will be displayed. Depending on the particular test, an error message may be displayed to aid the operator in determining the problem. If more information concerning the error report is necessary, look in the listing for the test number which was typed out and then note the program counter of the error report.

H.6 ERRORS
A test number and program counter are displayed at the time of an error (providing SW 13=0 and SW 12=0). In most cases, additional descriptive information is supplied in the error message.

H.6.1 Error Recovery
If the DMC11 hangs the bus (gains control of the bus so that console manual functions are inhibited), an INIT or power down/up is necessary for the operator to regain control of the CPU. When this happens, inspect location TSTNO (address 1220) for the number of the test running at the time of error.

H.7 RESTRICTIONS

H.7.1 Starting Restrictions
The status table should be verified regardless of how the program was started. It may also be used with the information printed on the console terminal to isolate problems.

H.7.2 Operating Restrictions
The status table must be set up the first time a DMC11 diagnostic is loaded into core and run. This is done by manual input (SW 00=1) or by autosizing (SW 00=0 and SW 07=0). Thereafter, the status table need not be set up by subsequent restarts or by loading the next DMC diagnostic because it is overlayed. The current parameters in the status table are used when SW 07=1 on startup.

H.7.3 Hardware Configuration Restrictions

DMC11(M8200)	Jumper W1 must be installed and switch 7 of E76 must be in the OFF position.
KMC(M8204)	Jumper W1 must be installed.
LINE UNIT(M8201)	Jumpers W1, W2, and W4 must be installed. Jumpers W3, and W5 must be removed. SW 8 of E26 must be in the ON position.
LINE UNIT(M8202)	Jumper W1 must be installed. SW 8 of E26 must be in the OFF position.

H.8 ADDITIONAL INFORMATION

H.8.1 Execution Time
All DMC11 device diagnostics display an END PASS message within four minutes providing no errors occurred; SW 12=0 and SW 11=1 (DELETE ITERATIONS) are set. Actual execution time depends on the PDP-11 CPU configuration and the type of memory in the system.

H.8.2 Pass Complete
Every time the program is started, the tests run as if SW 11 (DELETE ITERATIONS) were up (=1). This is to verify no hard errors as soon as possible. Therefore, each time the program is started, the first pass will be a quick pass until all DMC11s in the system are tested. When the diagnostic has completed a pass, a display similar to the following appears:

END PASS DZDMH CSR: 175000 VEC: 0300 PASSES: 000001
ERRORS: 000000

H.8.3   Key Locations

RETURN (1214)   Contains the address where the program returns when the iteration count is
reached or if loop on test is asserted.

NEXT (1216)   Contains the address of the next test to be performed.

TSTNO (1226)   Contains the number of the test being performed.

RUN (1316)   The bit in RUN always points to the DMC11 currently being tested. For ex-
ample,

(RUN) 1302/0000000001000000

means that DMC11 number 06 is the DMC11 now running.

DMCR00–DMCR17

DMST00–DMST17

(1500)–(1640)

These locations contain information needed to test up to 16 (decimal) DMC11s
sequentially. They contain the CSR, VECTOR, and STATUS concerning the
configuration of each DMC11.

DMACTV (1306)   Each bit set in this location indicates that the associated DMC11 will be tested in
turn. For example, (DMACTV) 1276/0000000000011111 means that DMC11
numbers 00, 01, 02, 03, 04 will be tested. As another example, (DMACTV)
1276/0000000000010001 means that DMC11 numbers 00 and 04 will be tested.

DMCSP (1401)   Contains the CSR of the current DMC11 under test.

H.8.4   Status Table
The status table starts at location 1500. It is filled by autosizing or by the manual parameter input. The
locations may also be altered by hand (toggled in) to suit the specific configuration.

The status map example shown below contains information for two DMC11s. The table can contain
up to 16 DMC11s. Following the map is a condition of the bits for each map entry.

MAP OF DMC11 STATUS

PC	CSR	STAT1	STAT2	STAT3
001500	160200	140310	177777	000000
001510	160210	016120	000000	000000

Each map entry contains four words with the status information for four DMC11s. The PC shows the core memory location of the first of the four words. In the example above, the first DMC status is in locations 1500, 1502, 1504, and 1506. The second DMC status is located at 1510, 1512, 1514, and 1516. The information contained in each four-word entry is defined as follows:

CSR: Contains DMC11 CSR address

STAT1: BITS 00–08   DMC11 vector address

BIT 15=1 Microprocessor has CRAM

BIT 15=0 Microprocessor has CROM

BIT 14=1 Turnaround connector is on

BIT 14=0 No turnaround connector

BIT 13=0 Line unit is an M8201

BIT 13=1 Line unit is an M8202

BIT 12=1 No line unit

BITS 9–11 DMC11 BR priority level

STAT2: Low byte is switch PAC#1 (DDCMP line number)
High byte is switch PAC#2 (BM873 boot address)

STAT3: BIT 0=1   perform free-running tests on KMC (must be set manually. See test 1.)

BIT 1=0   DMC11-AR (low-speed)

BIT 1=1   DMC11-AL (high-speed)

H.8.5   Method of Autosizing

H.8.5.1   Finding the Control Status Register – The autosizing routine finds a DMC11 as follows:

1. Starting at address 160000, all addresses in increments of 10 up to and including address 167760 are tested.

2. If the address does not time out, the first CROM address is written to address 125252 and then read back.

3. If the first CROM address contains -1, 125252, 626, or 16520, a DMC11 or KMC11 has been found. If not, the address is updated by 10 and the search continues. These values are interpreted as follows:

    -1   DMC11 with no CROM

    125252   KMC11 with CRAM

    626   DMC11-AL

    16520   DMC11-AR

    Further tests are performed to determine: (1) which line unit, if any, is installed; (2) if a loopback connector is installed; and (3) various switch settings on the line unit. This is why the status table must be verified by the user. If any of the information does not agree with the hardware, the diagnostic must be restarted and the questions answered. All DMC11s in the system will be found by the autosizer. If none are found, the diagnostic must be restarted and the questions answered.

H.8.5.2 Finding the Vector and BR Level – The vector area (addresses 300–776) is filled with the instruction IOT and .+2 (next address). The processor status is started at 7, and the DMC11 is programmed to interrupt. The processor status is lowered by one until the DMC11 interrupts. A delay is made and, if no interrupt occurs at processor status level three (because of a bad DMC11), the program assumes vector address 300 at bus priority level 5. The problem should be corrected in the diagnostic and the program set up again to obtain the correct vector. If an interrupt occurred, the address to which the DMC11 interrupted is reported as the vector.

NOTE
**If the vector reported is not the same as set up by the
operator, autosizing should not be done.**

H.8.6 Software Switch Register
If the diagnostic is run on a PDP-11/04 or other CPU without a hardware switch register, a software switch register is used. If the hardware switch register does not exist or it contains 177777, the software switch register is used.

To obtain control at any allowable time during execution of the diagnostic, the operator types CTRL G on the console terminal keyboard. This action causes the following to be printed:

SWR = XXXXXX NFW?

The current contents (in octal) of the software switch register appear in place of XXXXXX. The software control routine then awaits operator action. The operator must type one or more of the following legal characters: 0–7, line field, carriage return, or CTRL U. No check is made for legality. If the input character is not a line feed, carriage return, or CTRL U, an octal digit is assumed.

To change the contents of the software switch register, the operator types the new desired value in octal (leading zeroes may be omitted) and terminates the input string with a carriage return or line feed depending on the program action desired. The input value is truncated to the last six digits typed. At least one digit must be typed per input string prior to the terminator before a change to the software switch register occurs.

When the input string is terminated with a carriage return, the diagnostic continues execution from the point of interruption. If a carriage return is the only character typed, the program continues without changing the software switch register. The line feed differs from the carriage return by transferring control to address 200 and restarting the program.

If CTRL U is typed at any point in the input string, the input value is disregarded and SWR=XXXXXX NEW? displayed.

To set the software switch register for the starting switches, first load the diagnostic, type CTRL G, and then start the diagnostic.

APPENDIX I
DIFFERENCES BETWEEN DDCMP V4.0
AND DMC11 IMPLEMENTATION OF
DDCMP V3.03

This appendix summarizes the known differences between DDCMP V4.0 and DMC11 implementation of DDCMP V3.03.

A. A DMC11 receiver does not count characters in the data field of a numbered data message when the following occurs:

    a. No received buffer is available.

    b. Received message is out of sequence.

    c. Received message length (character count in valid header) is longer than the assigned received buffer.

B. The receiver is reset to resynchronize after detecting a bad header CRC. This could cause false synchronization or message framing if the data field contains SYNC characters followed by a valid header.

C. If a receiver buffer is not available when a numbered message header comes in, the header BCC is not checked. The resulting NAK, no buffer available message, is queued to the transmitter even if the header BCC is bad.

D. In DDCMP Maintenance Operation (MOP) Mode, the maintenance message headers are sent with Quick SYNCs and select bits cleared, and a number appears in the NUM field.

E. The reply timer is started at the beginning of a message transmission rather than at the end.

F. On receive, the DMC11-AL assumes the Quick SYNC bit is always set and cannot receive abutted messages. A synchronization sequence is required for each message.

G. On DMC11 start up, the START message is sent every second. In half-duplex applications this could cause line contention problems where both stations would send START at the same time, every second.

H. All NAKs received are accumulated in a cumulative counter (PDP-11 Base Address +5). There is no NAK received threshold counter.

I. The receiver ignores ACK with a response number greater than X, where X is the number of the data message that was last transmitted.

Skipping of unneeded retransmission is not possible. For example, if DMC11 sends out numbered messages 1, 2, 3, 4, 5, and 6 and there was a noise hit on message No. 3 only, DMC11 No. 2 replies with a NAK (RESP=2) and then DMC11 No. 1 has to retransmit 3, 4, 5, 6.

J. On transmit, the DMC11 always has Quick SYNC and select bits cleared in a numbered message header. The transmitter always sends out a separate control message following the numbered message with both Quick SYNC and select bits set. All unnumbered messages have both QS + SEL bits set.

K. On receive, the DMC11-AR always checks the Quick SYNC and select bits and therefore is capable of receiving abutted messages.

L. Quick SYNC and Select must never be set in a numbered message to be received by DMC11, that is, on messages from non-DMC DDCMP implementations.

<div align="center">

NOTE

If Q and S bits are set in the numbered message header, both bits will be written into memory extension bits of the Receive Buffer Address (BA/CC 0). Therefore, RCV VACC/0 will have memory extension bits set.

If the Select bit is set in a data message on HDX link, a NAK may be lost due to collision of receive data with the transmitted NAK (DMC11-AR only). This causes the Reply (REP) sequence to be initiated.

</div>

M. Synchronization sequences always consist of eight SYNC characters for DMC11-AR and ten SYNC characters for DMC11-AL.

N. The reply to a REP message is always a NAK (with implied acknowledgements).

O. NAK MSG number = last correctly received MSG number, that is, if NAK MSG number = last transmitted message number, all messages have been received correctly. (Possibly a lost ACK occurred.)

P. ACKs are sent every second for the last message. After completion of START SEQ, Idles ACKs for message number 0.

Q. In HDX – The section interval timer is the same at both ends creating a possible deadlock where both ends are in contention for the link.

APPENDIX J
PROGRAMMING PROCEDURES FOR DMC11-AR
OPTION IN AUTO DIAL/AUTO ANSWER
APPLICATION

The DMC11 AR option can be programmed to function in autodial/autoanswer applications. The autodial programming of the associated DN11 automatic calling unit interface should be ordered the same as other communication options, that is, perform the dial sequence and then start the DMC11, not the inverse. The premature abort of messages via the communication link can be detected by using dummy messages and the aborted call can be programmed as part of the driver. Details are presented in paragraphs J.1 to J.3 following.

J.1 AUTO DIAL
The DMC11 functions with the Bell 801 autodial or equivalent dialer provided the proper programming sequence and 801 options are selected.

When the DMC11 is used in conjunction with a Bell 801 autodial, the DMC11 must be halted with MASTER CLEAR or procedure error prior to asserting Call Request (CRQ).

When dialing and modem handshaking are completed, Data Set Status (DSS) in the 801 dialer is asserted. Only then should the DMC be given a Base and Control Transfer.

The recommended method of terminating calls is with the 801 dialer strapped to use the CRQ disconnect option. After CRQ is dropped (on hook), the DMC11 should be halted again by MASTER CLEAR or procedure error so the next 801 dial may take place.

An alternate route to disconnecting is via the DTR disconnect option in the 801 dialer. Disconnect in this case is caused by dropping DTR in the DMC. The DMC11 drops DTR for one second when a procedural error is asserted, and the DMC11 is then left in this state until the next 801 dial takes place.

J.2 PREMATURE LINK DISCONNECT
The DMC11 does not monitor the state of the carrier and, therefore, cannot detect line loss during message framing. This can be programmed around by periodically sending dummy messages and running a timer on messages received.

J.3 AUTO ANSWER
The DMC11 microcode does not test for a premature call abort. An abort occurs when a call is received but the caller does not enter the data mode (that is, Carrier is not asserted), thereby causing the call to disconnect.

The user may test for a premature call abort by means of a ring timer. In general, the software must clear DTR and scan RING. When RING is detected, set DTR, start the DMC11 (BASE I, CNTL I, etc.) and start the software timer. If the software timer expires before the DMC11 interrupts with DDCMP start received, then MASTER CLEAR DMC11, clear DTR, and scan RING again.

A flow chart of the auto answer sequence is presented in Figure J-1. This programming technique of loading microinstructions while the DMC11 microprocessor is running is only valid when the DMC11 microcode is in the initialized state.

	PROGRAM NOTES	COMMENTS
MASTER CLEAR DMC	MOVB # 100, DMC BSEL1;	MASTER CLEAR DMC11
CLEAR DTR	MOV # 122013 DMC SEL6; NOP (WASTE TIME) MOVB # 202, DMC BSEL1;	LOAD MICROINSTRUCTION TO CLEAR DTR SET ROM IN
RING STATE TO DMC BSEL 3 BIT 7 (EVERY 300 NS)	MOV # 21263, DMC SEL6;	LOAD MICROINSTRUCTION TO WRITE RING STATE TO BSEL 3
TEST RING ON — NO	DRIVER DOES RING SCAN	
DDCMP START REC'D TIMER ON		
MASTER CLEAR	MOVB # 100, DMC BSEL1 (ALSO SETS DTR)	
START DMC	BASE I, CONTROL I RX BUFFER	
TIME OUT — NO → DDCMP START REC'D — NO		
SERVICE DMC AS REQUIRED		

MK-0815

Figure J-1 Auto Answer Sequence

J-2

GLOSSARY

ACKNOWLEDGE (ACK):
Indicates that the previous transmission block was accepted by the receiver and it is ready to accept the next block of the transmission.

ARITHMETIC LOGIC UNIT (ALU):
Allows the microprocessor to perform arithmetic and logic operations.

A PORT:
Read/write input to the multiport RAM.

ASYNCHRONOUS TRANSMISSION:
Transmission in which time intervals between transmitted characters may be of unequal length. Transmission is controlled by start and stop elements at the beginning and end of each character. Also called Start-Stop transmission.

BUFFERED ARITHMETIC LOGIC UNIT (BALU):
Operations performed by the ALU are buffered by the BALU and directed to data memory, respective registers and the Berg Port.

BERG PORT:
An 8-bit port that allows the microprocessor to communicate with other devices without using the UNIBUS.

BIT-STUFF PROTOCOL:
Zero insertion by the transmitter after any succession of five continuous ones designed for bit-oriented protocols such as IBM's Synchronous Data Link Control (SDLC).

BITS PER SECOND (BPS):
Bit transfer rate per unit of time.

B PORT:
Read Address input of the multiport RAM (Read Only Port).

BRANCH REGISTER (BRG):
Temporary card storage register used for branch determination and shifting right.

BUFFER:
Storage device used to compensate for a difference in the rate of data flow when transmitting data from one device to another.

CCITT:
Comite Consultatif Internationale de Telegraphie et Telephonie – An international consultative committee that sets international communications usage standards.

CONTROL AND STATUS REGISTERS (CSRs):
Communication of control and status information is accomplished through these registers.

CRC (Cyclic Redundancy Check):
An error scheme in which the check character is generated by taking the remainder after dividing all the serialized bits in a block of data by a predefined number.

CROM:
Plug-in Control Read Only Memory used as the instruction memory for the processor.

CYCLIC REDUNDANCY CHECK (CRC):
An error detection scheme in which the check character is generated by taking the remainder after dividing all the serialized bits in a block of data by a predetermined binary number.

DATA LINK ESCAPE (DLE):
A control character used exclusively to provide supplementary line control signals (control character sequences or DLE sequences). These are two-character sequences where the first character is DLE. The second character varies according to the function desired and the code used.

DATA MULTIPLEXER (DMUX):
An 8-bit wide, 8-to-1 multiplexer used to select data for the B input of the ALU.

DATA-PHONE DIGITAL SERVICE (DDS):
A communications service of the Bell System in which data is transmitted in digital rather than analog form, thus eliminating the need for modems.

DESTINATION ROM (DROM):
Controls the operand as defined by the destination of the instruction in the instruction register.

DIGITAL DATA COMMUNICATIONS PROTOCOL (DDCMP):
DIGITAL's standard communications protocol for character oriented protocol.

DIRECT MEMORY ACCESS (DMA):
Permits I/O transfers directly into or out of memory without passing through the processor's general registers.

DMC:
Data Communications Controlled option designation for the ROM controlled microprocessor and line units that are run by the micro controller.

ELECTRONIC INDUSTRIES ASSOCIATION (EIA):
A standards organization specializing in the electrical and functional characteristics of interface equipment.

FROM:
Function ROM – Controls up to 16 functions performed by the ALU.

FULL-DUPLEX (FDX):
Simultaneous two-way independent transmission in both directions.

FIELD REPLACEABLE UNIT (FRU):
Refers to a faulty unit not to be repaired in the field. Unit is replaced with a good unit and faulty unit is returned to predetermined location for repair.

FIFO:
First In/First Out characteristic of the SILO hardware buffer.

HALF-DUPLEX (HDX):
An alternate, one-way-at-a-time independent transmission.

IBUS/OBUS:
Microprocessor NPR control, miscellaneous registers, and CSRs.

IBUS*/OBUS*:
Microprocessor NPR control, miscellaneous registers, and CSRs.

INSTRUCTION REGISTER (IR):
Contains the instruction that is being executed. Outputs are used to control the microprocessor.

LARS:
Field Service Labor Activity Reporting System.

LINK MANAGEMENT:
The Link Management component resolves the transmission and reception on links that are connected to two or more transmitters and/or receivers in a given direction.

LU IBUS:
The Line Unit Input data Bus provides a path to the DMUX via the Berg connector.

MEMORY ADDRESS REGISTER (MAR):
Controls the data memory for buffered arithmetic and logic operations to main memory.

MAIN MEMORY (MEM):
Data storage area for the microprocessor 4K X 8 RAM; cannot be accessed directly by the CPU.

MAINTENANCE INSTRUCTION REGISTER (MIR):
Provides a destination for an instruction that can be loaded by the CPU during maintenance.

MOP:
Maintenance Operation Protocol.

MULTIPORT RAM:
Contains all M8200 control and status registers between the microprocessor and the CPU processor.

NEGATIVE ACKNOWLEDGMENT (NAK):
Indicates that previous transmission block was in error and that receiver is ready to accept a retransmission of tde erroneous block (also a Not Ready Reply to a Station selection in multiport).

NON-PROCESSOR REQUEST (NPR):
Direct memory access type transfers, see DMA.

PROGRAM COUNTER (PC):
A 14-bit counter used to control the address of the control ROM directly.

PROGRAM COUNTER REGISTER (PCR):
Contains upper six bits to be loaded into the PC on a branch condition and provides extra field addressing with future expansion capability.

PROTOCOL:
A formal set of conventions governing the format and relative timing of message exchange between two communicating processes.

RANDOM ACCESS MEMORY (RAM)

READ ONLY MEMORY (ROM)

RS232-C:
EIA standard single-ended interface levels to modem.

RS 422:
EIA standard differential interface levels to modem.

RS 423:
EIA standard single-ended interface levels to modem.

RS 449:
EIA standard connections for RS422 and RS423 to modem interface.

SCRATCHPAD MEMORY (SP):
Read/write memory used for temporary storage of data.

SROM:
Source ROM – Defines the type of instruction to be executed and the source of the data used for the instruction.

SYNCHRONOUS TRANSMISSION:
Transmission in which the data characters and bits are transmitted at a fixed rate with the transmitter and receiver synchronized.

SYSTEM CLOCK:
Basic timing generated by a 33.33MHz crystal providing microprocessor timing functions.

UNIBUS:
A single high speed bus on which system components connect and communicate with each other. Addresses, data, and control information are transmitted via 56 available lines of the bus.

V.35:
(CCITT Standard) – Differential current mode type signal interface for high-speed modems.

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