EK-DMF32-UG-002

DMF32
USER'S GUIDE

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DMF32
USER'S GUIDE

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1 GENERAL DESCRIPTION

1.1 INTRODUCTION

The DMF32 is an intelligent VAX family DMA UNIBUS controller that supports a combination of I/O devices, including the following (see Figure 1-1):

- Eight asynchronous lines
- One synchronous line
- One DMA line printer interface or one enhanced DR11-C functional parallel I/O port

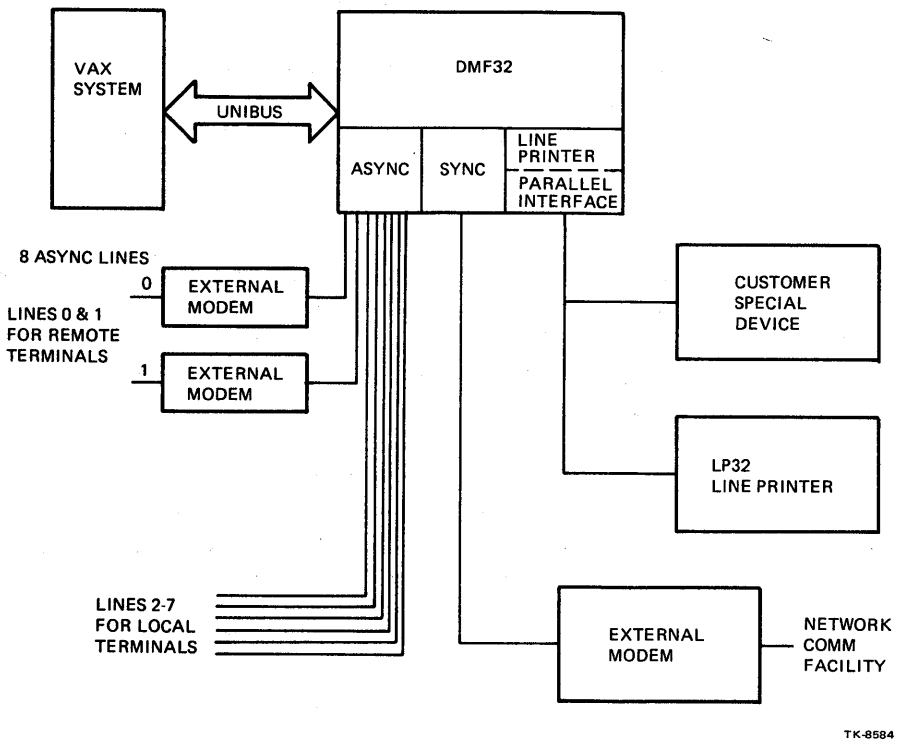


Figure 1-1 DMF32 Overview Block Diagram

1.1.1 Asynchronous Multiplexer

The asynchronous multiplexer supports eight transmit and eight receive lines. Each pair of lines (one transmit and one receive) can be programmed to operate at one of 16 baud rates ranging from 50 bps to 19.2 Kbps. Both line 0 and line 1 have split-speed capability and full modem control. The asynchronous multiplexer also supports the auto echo function.

Transmission can be selected for DMA or SILO operation. In SILO mode, each line transmits characters from its own 32-character buffer. These buffers are loaded under host software control. In DMA mode, a transmit line transmits characters from the main memory location specified by the buffer address and character count.

All eight lines share a 48-character receive silo. There is a programmable silo timeout period for the receive silo.

An interrupt can be generated under one of the following conditions:

- Sixteen characters have entered the silo
- The silo has been non-empty for a time greater than a programmable timeout period. This timeout period can be set to zero.

The asynchronous lines are connected either to data terminal equipment (DTE) or data communications equipment (DCE) via standard EIA RS-232-C 25-pin connectors. The signal levels of the asynchronous multiplexer are RS423 compatible (1μ second rise time).

1.1.2 Synchronous Interface

The synchronous interface is a single-line DMA communications device with full modem control (EIA RS-232-C/CCITT-V.28). The signal levels of the synchronous interface are RS423 compatible (1μ second rise time). The DMA transfers are double buffered; that is, both the transmitter and receiver have two sets of byte count and buffer address registers.

The synchronous interface supports various bit-oriented protocols (SDLC and HDLC) and byte-oriented protocols (DDCMP). The synchronous line can frame the messages, generate and check CRC, and DMA these messages to and from host memory. The host-level software performs all message acknowledgments and higher level network functions.

Running the GEN BYTE protocol (general byte-oriented synchronous) allows the synchronous interface to implement any byte-oriented protocol. The GEN BYTE protocol uses a straight transfer of data between main memory and the synchronous interface. The host-level software handles the protocol-specific functions.

The synchronous interface has modem control. The modem lines conform to EIA RS-232-C/CCITT-V.24 specifications for speeds up to 19,200 bits per second. The synchronous interface is connected to DTE or DCE via the standard 25-pin Cinch connector. Direct connection to another synchronous interface can be done via a null modem cable.

When using the DMF32 crystal-controlled baud rate generator, the synchronous line can transmit at one of sixteen different programmable speeds. With external clocking, any transmit or receive bit rate up to 19.2 kbps can be used. The receiver uses an external clock originating from the modem, except during maintenance testing.

1.1.3 Line Printer Interface

The DMA line printer operates with the LP32 family of printers. This interface also supports low-level formatting functions.

1.1.4 Parallel Interface

This 16-bit parallel interface is an enhanced DR11-C functional interface. It can also support SILO mode (half-duplex) or double-buffered DMA (half-duplex). Since the line printer interface and the parallel interface share hardware, both interfaces cannot be used concurrently.

1.2 PHYSICAL DESCRIPTION

The DMF32 consists of a single hex-size peripheral controller (SPC) module, an 8.25-inch × 4-inch distribution panel, and three 40-pin shielded BC06R flat cables. The three BC06R cables connect the single hex module to the distribution panel via standard Berg connectors. Refer to Figure 1-2 for the DMF32 components.

The distribution panel has eleven Cinch connectors. Eight connectors are for the eight asynchronous lines, one connector is for the synchronous line, and two connectors are for the parallel port. The distribution panel also has three 10-position DIP switch packs.

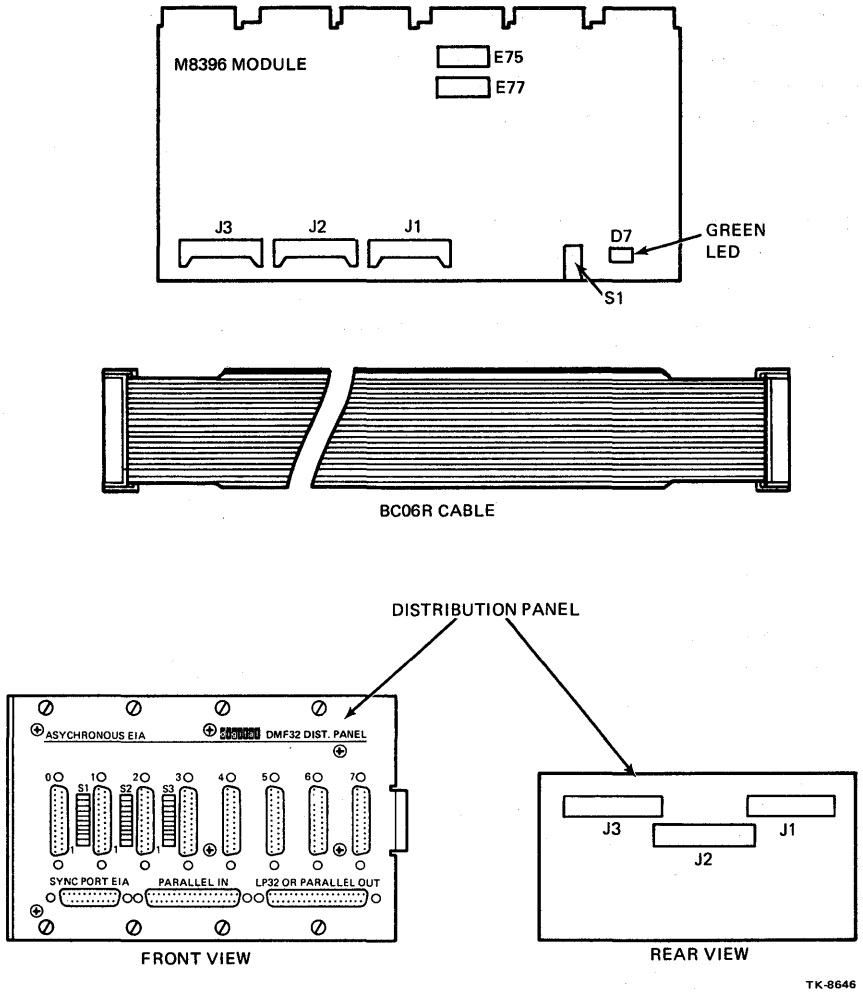


Figure 1-2 DMF32 Components

1.2.1 DMF32 Configurations

The DMF32 is available in three different options; each is designated by two letters (AA, AB, or AC). These options are defined in the following paragraphs.

1.2.1.1 DMF32-AA Option – The DMF32-AA option is used in the VAX-11/730 system packages. Table 1-1 lists the contents of this option.

Table 1-1 DMF32-AA Options

Quantity	Part Number	Description
1	M8396	Hex module
3	BC06R-7	40-conductor cable
1	70-18754-00	Distribution panel assembly
1	H3248	Single-line loopback
1	EK-DMF32-UG	*DMF32 User's Guide*
1	MP01271	*DMF32 Field Maintenance Print Set*

1.2.1.2 DMF32-AB Option – The DMF32-AB option is used in the BA11-KW expander cabinets. This option is identical to the DMF32-AA except that it has three BC06R-10 cables instead of three BC06R-7, and contains the additional items listed in Table 1-2.

Table 1-2 DMF32-AB Option Additional Contents

Quantity	Part Number	Description
1	74-27040-01	H9544-SJ frame, I/O non-shielded
4	90-09700-00	Screws, Sems Truss Phillips
4	90-06664-00	Washer, flat SST
4	90-07786-00	Nut, U-nut Retainer (.240 inside diameter)

1.2.1.3 DMF32-AC Option – This option is identical to the DMF32-AA except that it has three BC06R-12 cables instead of three BC06R-7 cables.

1.2.2 Test Connectors

The H3248 and H3249 test connectors, shown in Figure 1-3, are used with the DMF32. Only the H3248 test connector is included in the DMF32 options. The H3248 plugs into the distribution panel to loop back data and modem signals on a single line. The H3249 test connector connects to the M8396 module via the three BC06R cables. This arrangement provides staggered turnaround of the data and modem lines, testing both the M8396 module and cables.

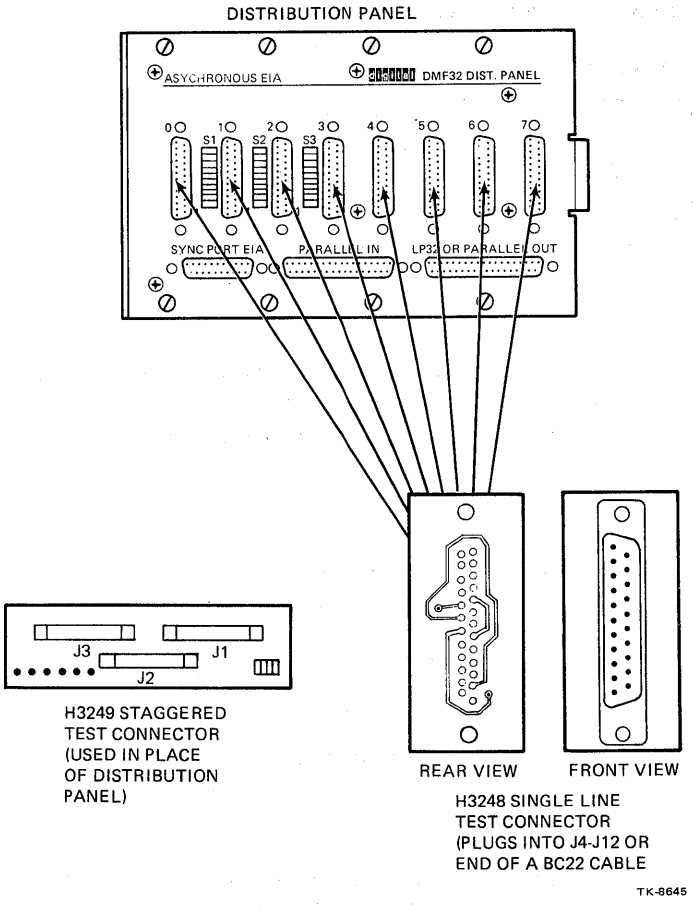


Figure 1-3 DMF32 Test Connectors

1.3 GENERAL SPECIFICATIONS

This section provides the information on the necessary environment, power specifications, device functional specifications, and performance parameters.

1.3.1 Environment

Table 1-3 lists the environment specifications for the DMF32.

Table 1-3 Environmental Specifications

Environment	Specification
Class B Environment	10C (50°F) to 40C (104°F)
Operating Temperature	Where maximum temperature is reduced 1.8°C per 1000 meters (1°F per 1000 feet) of altitude
Relative Humidity	10% to 90% with a maximum wet bulb of 28°C (82°F) and a minimum dewpoint of 2°C (36°F)
Cooling	11 cubic feet per minute
Heat Dissipation	175 BTU per hour

1.3.2 Power Specifications

The SPC slot the DMF32 is plugged into provides the power for the DMF32. The electircal requirements are as follows:

8.0 amperes @ +5 Vdc
0.5 amperes @ +15 Vdc
0.5 amperes @ −15 Vdc

1.3.3 DMF32 Functional Parameters

Tables 1-4 through 1-7 list the functional parameters for the devices of the DMF32.

Table 1-4 Synchronous Functional Parameters

Parameter	Description
DMA Transfer	Double-Buffered
Protocols Supported	DDCMP, SDLC, HDLC, GEN BYTE
Protocol Functions	Bit stuffing, bit removal, cyclic redundancy check generation and recognition, framing messages
Modem Lines	EIA RS-232-C/CCITT-V.24
Data Rates	800, 1200, 1760, 2152, 2400, 4800, 9600 and 19200 bits per second using internally genenrated transmit clock

Table 1-5 Asynchronous Functional Parameters

Parameter	Description
Operating Mode	Full-duplex or half-duplex
Data Format	Asynchronous, serial by bit, one start bit, and 1 or 2 stop bits provided by the hardware under program control.
Character Size	5, 6, 7, or 8 bits, program-selectable. (Does not include the parity bit.)
Parity	Parity is program-selectable. There can be odd, even, or no parity. If parity is selected, a parity bit is added to the character in the MSB position.
Order of Bits	Transmission/reception low-order bit first
Data Rates	50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, and 19200 bits per second
Split Speed	Line 0 and line 1 only
Full Modem Control	Line 0 and line 1 only
Asynchronous Lines	RS-232-C compatible

Table 1-6 Parallel Interface Functional Parameters

Parameter	Description
Data Input	16 bits parallel in
Data Output	16 bits parallel out
Electrical Signals	Similar to the DR11-C

Table 1-7 Printer Controller Functional Parameters

Parameter	Description
Printer Supported	LP25, LP26, LP07
Formatting Capabilities	Tab expansion, lower case to upper case conversion, line wrap, ff to lf conversion

1.3.4 DMF32 Performance Parameters

Each of the eight asynchronous lines may transmit and receive at a maximum speed of 19,200 bits per second. The synchronous line may transmit and receive at a maximum speed of 19,200 bits per second. However, all of these lines may not operate at their maximum speed concurrently.

1.3.5 Installation Distances

The recommended distance from the DMF32 to the RS-232-C/CCITT-V.24 terminal or modem is 15 meters (50 feet) at up to 9600 bps with a BC22 or similar cable. Operation which exceeds 50 feet does not meet the distances recommended in RS-232-C/CCITT-V.24. Operation is often possible at longer distances, depending on the terminal equipment, type of cable, speed of operation, and electrical environment. For these reasons, DIGITAL cannot guarantee error-free operation at distances greater than 15 meters (50 feet).

The DMF32 can be connected to local DIGITAL terminals (and most other terminals) at distances greater than 50 feet with acceptable results if the terminal and computer are in the same building, in a modern office environment. A shielded twisted pair cable (Belden 8777 or equivalent) is recommended and used in the BC22D null modem cable.

NOTE

The ground potential difference between the DMF32 and the terminal must not exceed two volts. This condition limits operation to within a single building served by one ac power service.

2 INSTALLATION

2.1 SCOPE

This chapter describes the procedures for unpacking, installing, and checking out the DMF32.

2.2 UNPACKING AND INSPECTION

The DMF32 is packed according to commercial packing practices. Remove all packing materials and check the equipment against the shipping list. Table 1-1 lists the items contained in the DMF32 options. Inspect all items and carefully check the module for cracks, loose components, and breaks in the etched paths. Report damages or missing items to the shipper immediately and inform the DIGITAL representative.

2.3 DEVICE AND VECTOR ADDRESS ASSIGNMENTS

The DMF32's device addresses are selected from the floating address space of the UNIBUS input/output (I/O) page. The E75 switch pack on the DMF32 selects the first DMF32 CSR address. The DMF32 calculates the other DMF32 CSR addresses from the first address.

When there are no floating devices before the DMF32, the first floating address space for a DMF32 is 760340 (FE0E0 hex). The second floating address space for a DMF32 is 760400 (FE100 hex). The third floating address space for a DMF32 is 760440 (FE120 hex). When operating under VMS, the actual address(es) can be determined by using the SYSGEN utility. Refer to the *VAX/VMS Guide to Writing a Device Driver* (AA-H499B-TE) for the procedure to determine CSR address assignments.

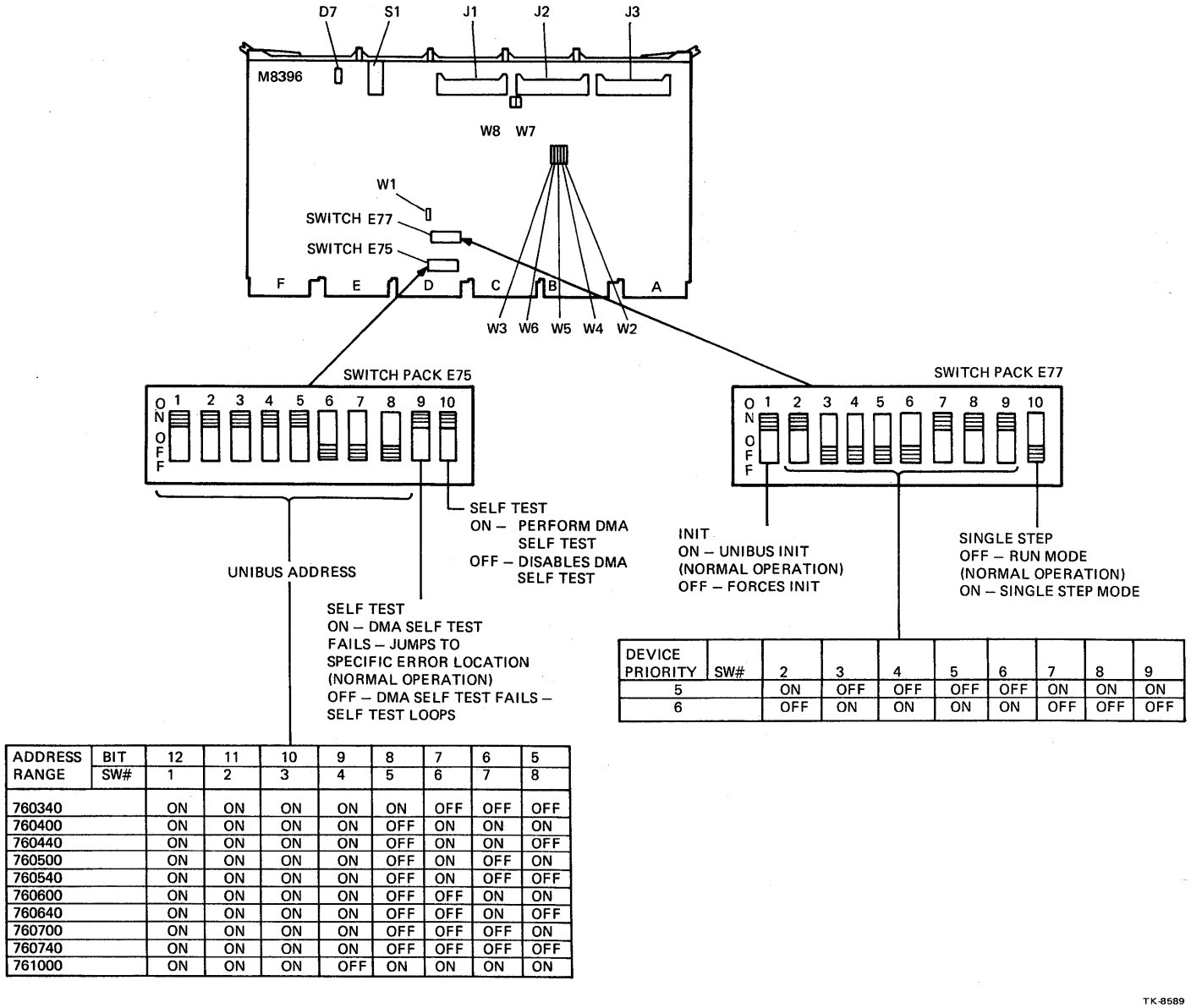
There are no switches on the DMF32 for interrupt vectors. At autoconfigure time, the operating system loads the value of the base vector into the DMF32. The DMF32 calculates the other DMF32 vectors from this base vector.

2.4 INSTALLATION PROCEDURE

2.4.1 M8396 Module Installation

To install the M8396, perform the following steps.

1. Set the switches on the E77 switch pack to the correct priority level; also set switch 1 (E77) to ON and switch 10 (E77) to OFF. Refer to Figure 2-1 for the switch settings. Also confirm that all eight jumpers are installed on the DMF32. Table 2-1 lists the DMF32 jumper functions, and Figure 2-1 shows the jumper locations.



DEVICE PRIORITY	SW#	2	3	4	5	6	7	8	9
5		ON	OFF	OFF	OFF	OFF	ON	ON	ON
6		OFF	ON	ON	ON	ON	OFF	OFF	OFF

ADDRESS RANGE	BIT SW#	12 1	11 2	10 3	9 4	8 5	7 6	6 7	5 8
760340		ON	ON	ON	ON	ON	OFF	OFF	OFF
760400		ON	ON	ON	ON	OFF	ON	ON	ON
760440		ON	ON	ON	ON	OFF	ON	ON	OFF
760500		ON	ON	ON	ON	OFF	ON	OFF	ON
760540		ON	ON	ON	ON	OFF	ON	OFF	OFF
760600		ON	ON	ON	ON	OFF	OFF	ON	ON
760640		ON	ON	ON	ON	OFF	OFF	ON	OFF
760700		ON	ON	ON	ON	OFF	OFF	OFF	ON
760740		ON	ON	ON	ON	OFF	OFF	OFF	OFF
761000		ON	ON	ON	OFF	ON	ON	ON	ON

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Figure 2-1 DMF32 Switch Settings and Jumper Locations

Table 2-1 DMF32 Jumper Functions

Jumper	Name	Function
W1	UNIBUS INIT	Out – Disables UNIBUS Init In – Enables UNIBUS Init
W2	SYNC DSR	Always installed
W3	RX D RTN	Always installed
W4	DSR RTN	Always installed
W5	DCE TX CLK RTN	Always installed
W6	DCE RX CLK RTN	Always installed
W7	ASYNC 0 DSR	Always installed
W8	ASYNC 1 DSR	Always installed

2. Set the switches on E75 for the DMF32 CSR address. Refer to Section 2.3 and Figure 2-1 for the correct E75 switch settings.

3. The DMF32 can be installed into any slot that provides 8 amperes at +5V and 0.5 amperes at +15V and −15V. Refer to the appropriate VAX-11 installation manual for the location of SPC slots into which the DMF32 can be installed. Table 2-2 lists the VAX family installation manuals.

CAUTION

Do not insert or remove the M8396 module with power ON. Insert and remove the module slowly and carefully to avoid catching components on the card guides or changing the switch settings.

Table 2-2 VAX Family Installation Manuals

VAX System Number	Title	Document
VAX-11/780	*VAX-11/780 Installation Manual*	EK-SI780-IN
VAX-11/750	*VAX-11/750 Installation and Acceptance Manual*	EK-SI750-IN
VAX-11/730	*VAX-11/730 Installation Guide*	EK-SI730-IN

2.4.2 DMF32 Distribution Panel Installation

The DMF32 distribution panel is mounted in either a H9544-SJ mounting frame or a shielded bulkhead panel. To mount the distribution panel into the frame opening, position the distribution panel at an angle so that the lip of the distribution panel is behind the frame. The distribution panel is secured to the frame by eight screws.

The BC06R-XX cables are connected from M8396 J1 to distribution panel J1, J2 to J2, and J3 to J3. To connect the cables in this way, the cables for J1 and J3 are crossed over. When connecting each cable, make sure that the cable's rib side is facing up and the red strip is on the correct side.

2.4.3 Distribution Panel Installation Procedure

1. Determine if the system/expander cabinet has a shielded bulkhead type panel included as part of the cabinet. If the system/expander cabinet DOES contain a shielded bulkhead type panel, continue with Step 2. If system/expander cabinet DOES NOT contain a shielded bulkhead type panel, proceed to Step 4.

2. Remove the four 2 inch plates from the bulkhead panel to enable mounting the DMF32 distribution panel (refer to Figure 2-2).

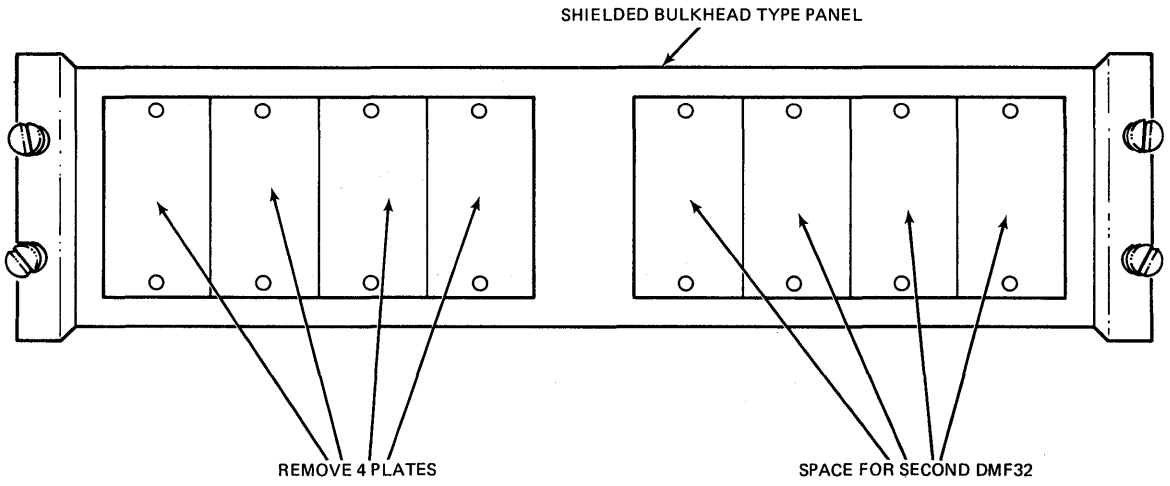


Figure 2-2 Shielded Bulkhead Type Panel

3. Discard the H9544-SJ "picture frame" (see Figure 2-3) from the DMF32-AB option package, since the frame is not used with the system/expander cabinets that contain the shielded bulkhead type frame. Now proceed to Step 7.

4. Remove the H9544-SJ picture frame from the DMF32-AB option package. Refer to Figure 2-3 to identify the frame.

5. Align the H9544-SJ frame on the cabinet vertical rails in the desired location. Mark the rail holes for reference, then install the U-nuts supplied with the option (see Figure 2-3).

6. Mount the H9544-SJ frame to the vertical rails of the cabinet with the screws and washers supplied.

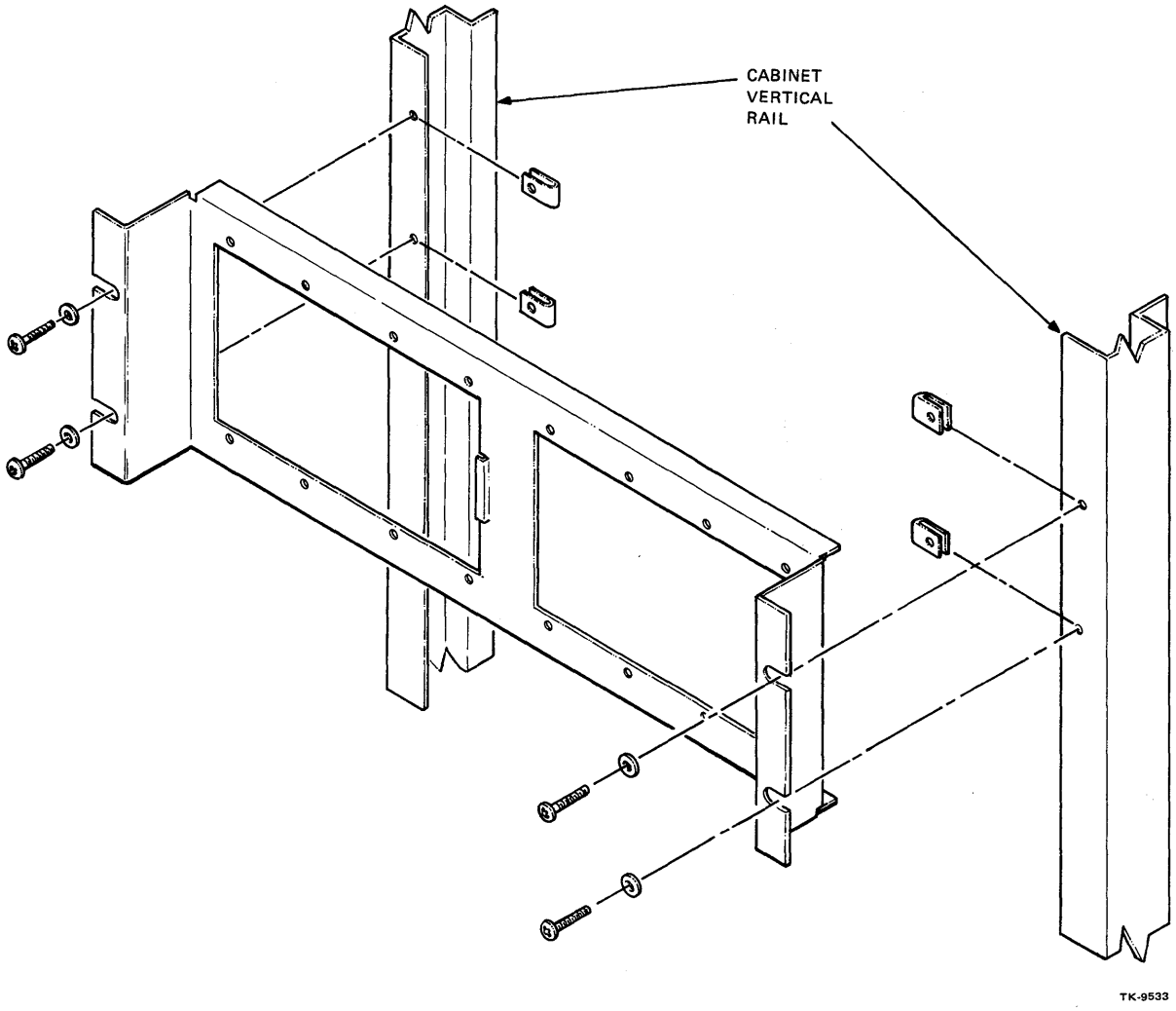


Figure 2-3 H9544-SJ Frame Installation

7. Install the BC06R-XX cables, if these cables have not yet been installed. The BC06R-XX cables are connected from the M8396 module to the DMF32 distribution panel: J1 to J1, J2 to J2, and J3 to J3. To make these connections, cables from J1 and J3 must be crossed (see Figure 2-4). Refer to the proper VAX-11 installation manual for the proper cable routing. Table 2-2 list the VAX-11 installation manuals.

8. Connect the BC06R-XX cables to J1, J2, and J3 of the M8396 module.

9. Pull the ends of the three BC06R-XX cables through the H9544-SJ/ shielded frame bulkhead opening that the DMF32 distribution panel is to be mounted in.

CAUTION

Connecting the BC06R-XX cables incorrectly can cause damage to the parallel port on the M8396.

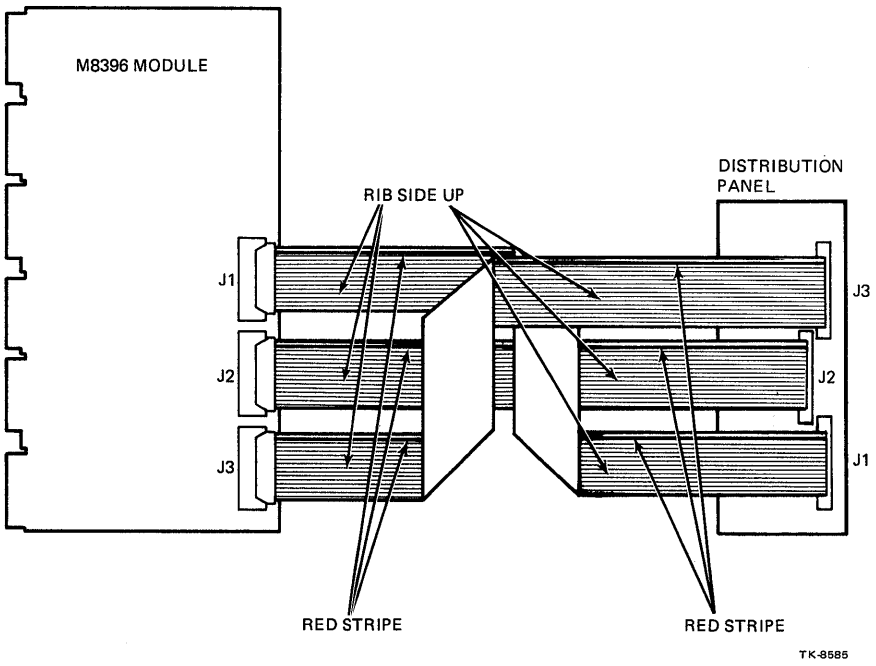


Figure 2-4 BC06R Cable Connections

10. Connect the three BC06R-XX cables to the distribution panel, making sure that the cable's rib side is up and the red strip is on the correct side (see Figure 2-4).

11. Position the distribution panel at an angle so that the lip of the distribution panel is behind the frame (see Figure 2-5).

12. Secure the distribution panel to the frame with the eight capture screws (part of the distribution panel).

2.4.4 BC06R Cable Routing

Refer to the appropriate VAX-11 installation manual for the BC06R cable routing. Table 2-2 lists the appropriate VAX family installation manuals.

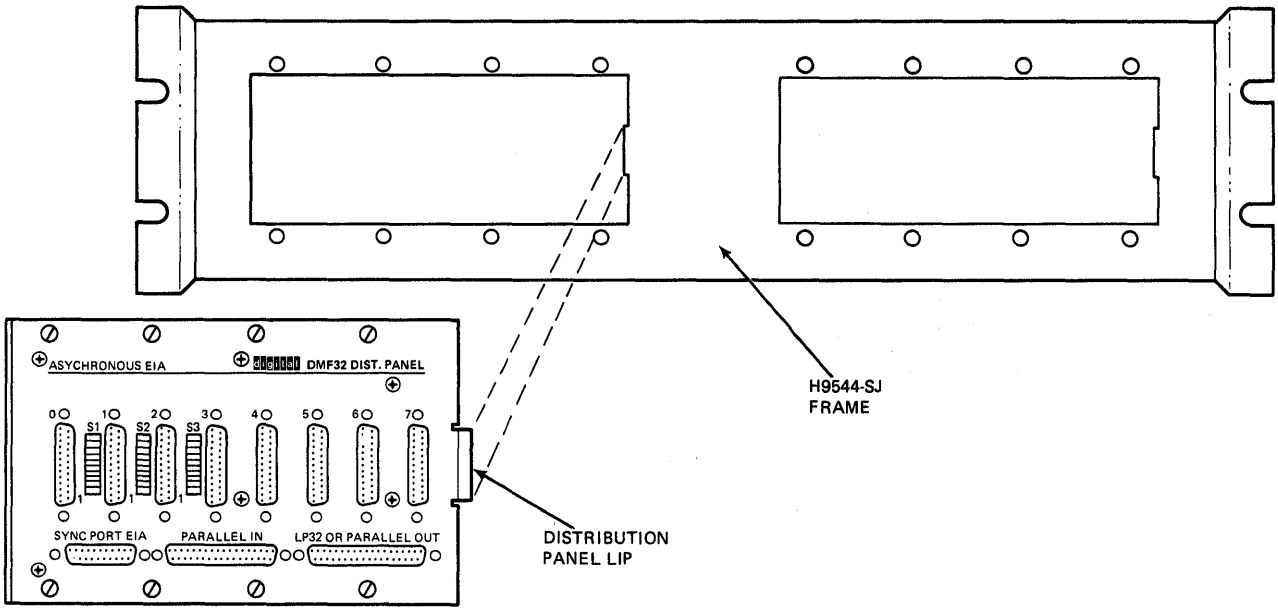


Figure 2-5 DMF32 Distribution Panel Installation

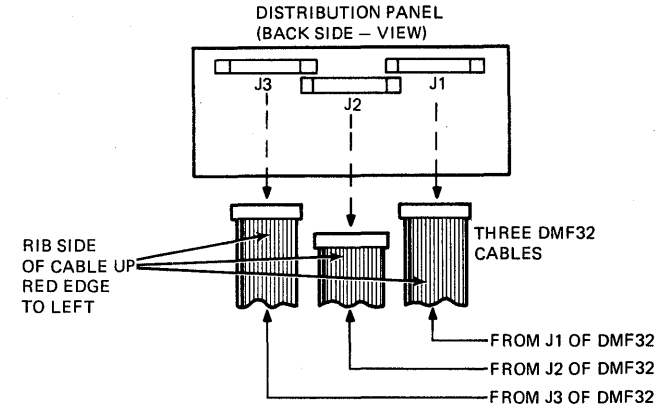
2.4.5 Verifying Standalone Operation

Run the Level 3 diagnostics with the H3249 staggered turnaround connector to verify the standalone operation of the DMF32. To verify the standalone operation, perform the following steps.

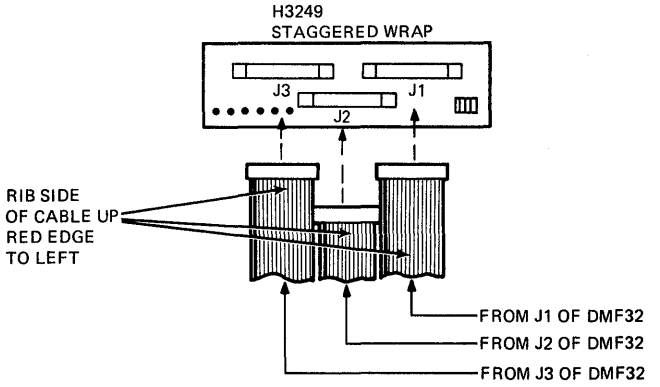
1. Connect the staggered turnaround connector (see Figure 2-6).

2. Run the Level 3 diagnostics listed in Table 2-3.

3. Disconnect the H3249 staggered turnaround connector. Connect the three BC06R cables to the distribution panel as shown in Figure 2-6.



STEP 1 – DISCONNECT THE THREE DMF32 CABLES FROM BACK SIDE OF THE DISTRIBUTION PANEL



STEP 2 – CONNECT THE THREE DMF32 CABLES TO THE STAGGERED WRAP

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Figure 2-6 Staggered Connector Installation

Table 2-3 Level 3 Diagnostics

Diagnostic	Section Tested	Operating Instruction
EVDLB	Synchronous port	Section 3.2.2
EVDLC	Asynchronous port	Section 3.2.3
EVDLD	Parallel port	Section 3.2.4

2.4.6 Communications Equipment Interface Cabling

Connect the cables from the distribution panel to the communications devices, printers, terminals, etc. Figure 2-7 shows the connectors on the distribution panel. Table 2-4 lists the recommended cables.

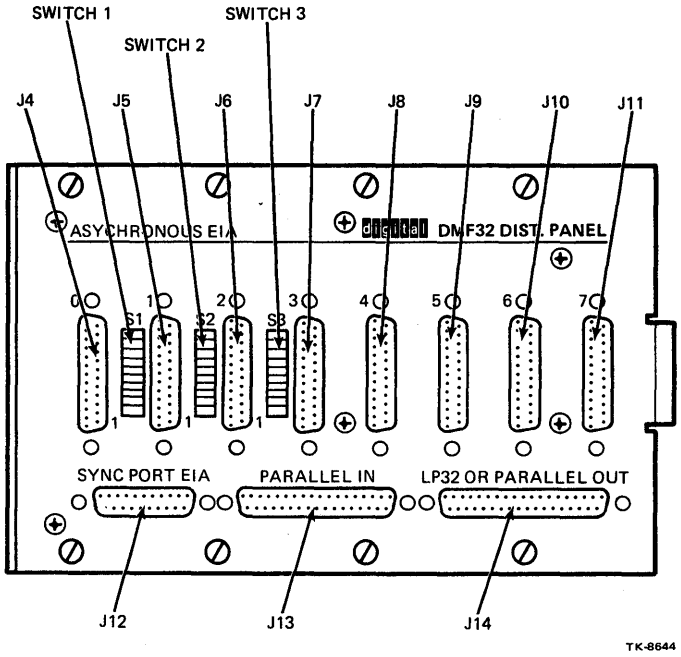

Figure 2-7 DMF32 Distribution Panel

Table 2-4 Recommended Cables

Cable	Device
BC22D	local terminals
BC22E	ASYNC modems (lines 0 and 1)
BC22F	SYNC modem
BC27A*	LP25, LP26
BC27B	LP07

* The BC27A cable or the BC27B cable is provided with the LP32 option.

2.4.7 Distribution Panel Switch Settings

Set the switches of the three switch packs on the distribution panel. Refer to Figure 2-7 for the switch pack locations. Table 2-5 lists the switch settings for the asynchronous line 0 (switch 1) and asynchronous line 1 (switch 2). Table 2-6 lists the switch settings for the synchronous line (switch 3). Table 2-7 lists the switch settings (switch 3) for the DMF32 device configurations. Table 2-8 shows the functions of jumpers W1 and W2 on the distribution panel. Both jumpers are normally installed.

Table 2-5 Common Switch Setups for Asynchronous Lines 0 and 1

Switch Packs 1 and 2	Local Terminal	Modems and H3248 Single-Line Connector
Switch 1	OFF	OFF
Switch 2	ON	ON
Switch 3	OFF	OFF
Switch 4	ON	ON
Switch 5	ON	ON
Switch 6	ON	ON
Switch 7	ON	ON
Switch 8	ON	OFF
Switch 9	ON	ON
Switch 10	ON	ON

Table 2-6 Common Switch Set-ups for the Synchronous Line

Switch Pack 3	Modems and H3248 Single Line Loopback Connector
Switch 1	ON
Switch 2	ON
Switch 3	ON
Switches 6-10	Not used

Table 2-7 DMF32 Device Configuration

Switch Pack 3		Active Device
Switch 4 ON	Switch 5 ON	Asynchronous
Switch 4 OFF	Switch 5 ON	Asynchronous, LP32
Switch 4 ON	Switch 5 OFF	Asynchronous, parallel interface, synchronous
Switch 4 OFF	Switch 5 OFF	Asynchronous, LP32, synchronous

Table 2-8 Distribution Panel EIA Selection Jumpers

Jumper W1	Jumper W2	Function
In or Out	In	Signal ground connected directly to frame ground
In	Out	Signal ground connected to frame ground through 100-ohm resistor
Out	Out	Signal ground isolated from frame ground

2.4.8 Verifying System-Integrated Operation

To verify system-integrated operation, run the DMF32 Level 2R diagnostics as follows:

1. Place all modems into loopback mode.
2. If modem loopback mode is not available, install a H3248 single-line loopback connector on one of the asynchronous connectors, and install a H3248 single-line loopback connector on the synchronous connector.
3. Run the DMF32 Level 2R diagnostics listed in Table 2-9.

Table 2-9 DMF32 Level 2R Diagnostics

Diagnostic	Section Tested	Operating Instruction
EVDLA	Synchronous port	3.3.2
EVDAC	Asynchronous port	3.3.3

4. Return all modems to the normal mode of operation.

5. Disconnect the H3248 single-line connector and reconnect any disconnected cables.

6. Set the three switch packs on the distribution panel for normal mode of operation. Refer to Tables 2-5, 2-6, and 2-7 for the switch settings.

7. The attached devices can be verified by running the following user-level diagnostics.

   EVAAA – Line Printer Diagnostic
   EVTAA – Terminal Diagnostic
   EVTBA – Terminal Exerciser
   EVDLF – Data Link Test

3 DMF32 DIAGNOSTICS

3.1 INTRODUCTION

This chapter describes using the DMF32 diagnostics. The DMF32 is supported by both Level 3 and Level 2R diagnostics. The Level 3 diagnostics are standalone diagnostics that run under the Diagnostic Supervisor using direct I/O. There are three Level 3 diagnostics: EVDLB, EVDLC, and EVDLD. These diagnostics verify the functionality of the DMF32 as follows:

EVDLB-verifies the synchronous interface
EVDLC-verifies the asynchronous multiplexer
EVDLD-verifies the parallel interface

The Level 2R diagnostics enable fault isolation to the option level while running under VMS. Various loopback methods can be used at either the distribution panel connector, modem cable, local modem, or remote modem. These various loopback methods can isolate the fault to a specific component of the network. Also, the Level 2R diagnostics can be used to provide a complete link between the DMF32 and another DMF32 or similar device for end-to-end function verification.

The Level 2R diagnostics, running under the Diagnostic Supervisor, use the QIO interface of the VMS device driver. There are two DMF32 Level 2R diagnostics: EVDAC and EVDLA. EVDAC verifies the functionality of the asynchronous multiplexer, and EVDLA verifies the functionality of the synchronous interface.

3.1.1 Diagnostic Supervisor

Both Level 3 and Level 2R diagnostics run under the Diagnostic Supervisor. Loading and using the Diagnostic Supervisor are described in both the *VAX-11/730 Diagnostic System Overview Manual* (EK-DS730-UG) and the *VAX Diagnostic System User's Guide* (EK-VX11D-UG).

3.1.2 DMF32 CSR Address and Vector Address

The DMF32 CSR address 760340 is used as an example address in the following diagnostic procedures. The actual address depends on the switch settings of E77 on the DMF32.

The vector address is used as an example address. The actual address is floating; thus the vector address depends on the UNIBUS configuration.

When running under VMS, the actual CSR address and vector address can be determined. Use the VMS utility SYSGEN to determine the actual addresses.

3.1.3 Hardware Loopback Methods

There are five loopback methods that can be used in running the DMF32 diagnostics. These loopback methods are sometimes referred to as "wraps". The five loopback methods are as follows:

- Internal wrap
- H3248 single-line loopback connector
- H3249 staggered loopback connector
- Local modem
- Programmable modem

3.1.3.1 Internal Wrap – The internal wrap enables the data to be internally looped within the DMF32. No external loopback connector is needed with the internal wrap. This wrap tests the DMF32's functionality (except the drivers, the receivers, the cables from the DMF32 to the distribution panel, and the distribution panel).

3.1.3.2 H3248 Single-Line Loopback Connector – The H3248 single-line loopback connector can be used when running the synchronous or asynchronous diagnostics. When the H3248 is used, the functionality of the drivers, receivers, cables from the DMF32 to the distribution panel, and the distribution panel are verified. The H3248 single-line loopback connector is connected to the line that is to be tested. Figure 3-1 shows how the H3248 single-line loopback connector is connected.

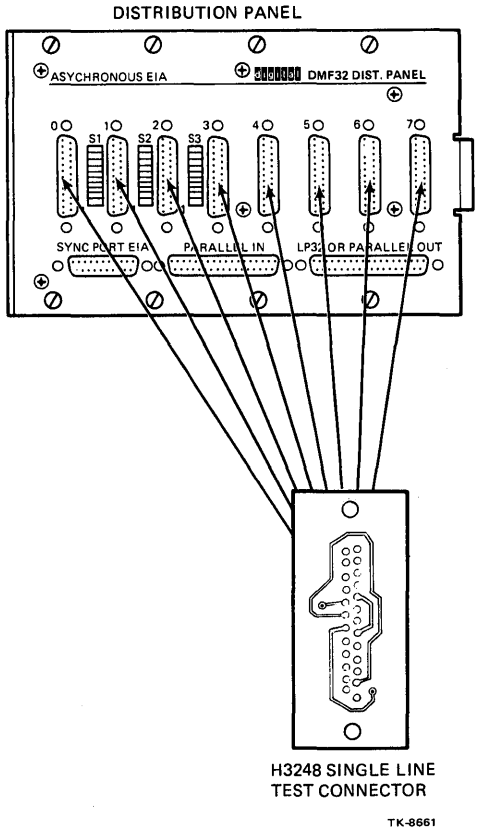

Figure 3-1 Single-Line Connector Installation

3.1.3.3 H3249 Staggered Loopback Connector – The H3249 staggered loopback connector can be used with any of the diagnostics, except EVDAC. This loopback connector is used to test the functionality of the DMF32 up to the distribution panel (exclusive of the distribution panel). The H3249 staggered loopback connector is required to test specific asynchronous multiple functions and to loop back the parallel port. Figure 3-2 shows how the H3249 staggered loopback connector is connected.

The dip switch pack on the H3249 staggered loopback connector is used for the following purpose. Switch 1 (H3249) is equivalent to switch 4 of SW-3 (distribution panel), and switch 2 (H3249) is equivalent to switch 5 of SW-3 (distribution panel). Both switches 3 and 4 (H3249) are not used. Refer to Table 2-7 for the equivalent switch positions of switches 1 and 2 (H3249).

The H3249 staggered loopback connector is part of each spares kit.

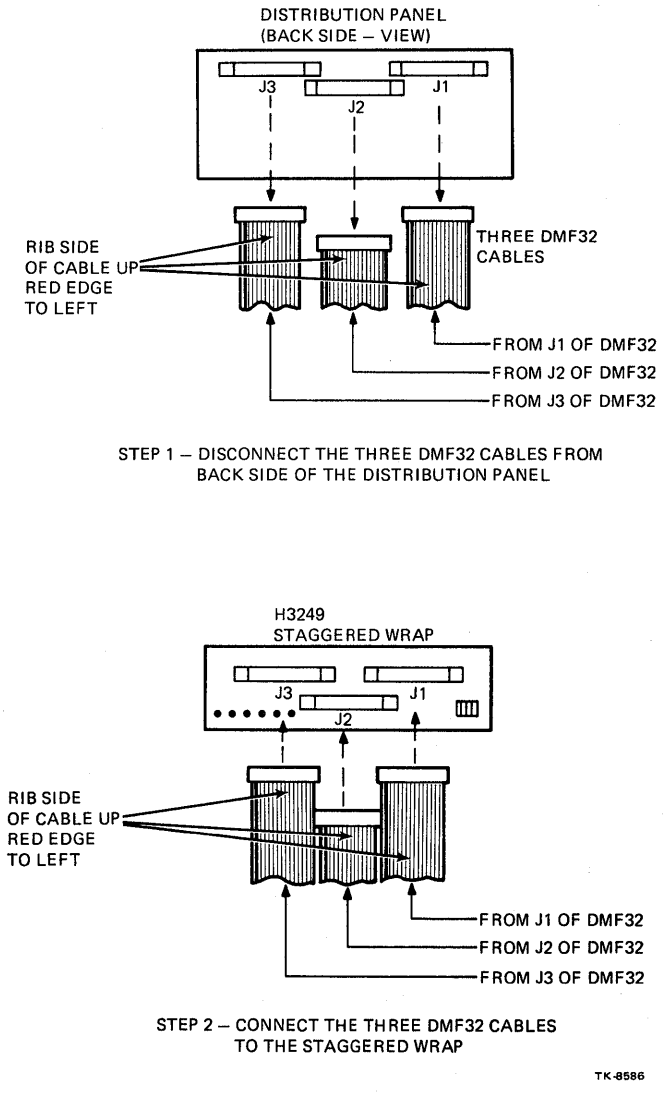

Figure 3-2 Staggered Connector Installation

3.1.3.4 Local Modem – Local modem is used when a modem is manually selected for analog (local) loopback testing. Any modem that can internally loop back data may be selected.

3.1.3.5 Programmable Modem – When a programmable modem is used, no manual intervention is required for local loopback. A programmable modem is any device that, whenever the diagnostics assert User TX (pin 18), provides a loopback path between the transmit data and the receive data.

3.1.4 Distribution Panel Switch Settings

When asynchronous or synchronous diagnostics are run with the H3248 attached, the switches on the distribution panel must be set as listed in Table 3-1.

3.1.5 Self Test

After each power-up, the DMF32 performs a self test. The first test of the EVDLB diagnostic verifies if this self test has been completed satisfactorily. The self test checks the following hardware elements:

1. 2901 ALU can perform computations correctly.
2. 2901 A and B registers can be addressed properly.
3. Condition codes can be set properly.
4. The local store RAM is operational.
5. The micro PC stack functions to four levels of the subroutine call correctly.
6. The UNIBUS slave trap hardware functions correctly.
7. The UNIBUS master I/O addressing and data transfers function correctly.

Table 3-1 Distribution Panel Switch Settings

Asynchronous Diagnostic Switches S1 and S2		Synchronous Diagnostic Switch S3	
Switch	**State**	**Switch**	**State**
1	OFF	1	ON
2	ON	2	ON
3	OFF	3	ON
4	ON	4-10	Not used
5	ON		
6	ON		
7	ON		
8	OFF		
9	ON		
10	ON		

3.2 DMF32 LEVEL 3 DIAGNOSTICS

There are three Level 3 diagnostics used to support the DMF32: EVDLB, EVDLC, and EVDLD. These diagnostics operate under the VAX Diagnostic Supervisor (DS). Table 3-2 lists some of the parameters of these diagnostics.

3.2.1 Level 3 Hardware Prerequisites

The following must be functional before the Level 3 diagnostics may be used.

- VAX-11 CPU
- Memory (256 KB minimum)
- UNIBUS adapter (DW730, DW750, or DW780, as applicable)
- Green LED on the DMF32 must be illuminated

3.2.2 EVDLB Diagnostic Description

The EVDLB diagnostic tests the synchronous port only; it ignores devices on the asynchronous and parallel ports. The default section of the EVDLB diagnostic provides internal loopback testing (no external loopback connector is required). An external connector (single-line loopback connector or the H3249 staggered loopback connector) can be used to verify the complete functionality of the synchronous interface.

The manual section of the EVDLB diagnostic provides for external loopback testing using the local modem or the remote modem as the rloopback device. Using the remote modem verifies the functionality of the communications facilities.

3.2.2.1 Loading, Attaching, and Running EVDLB – After the Diagnostic Supervisor is loaded, the operating instructions in Example 3-1 can be used for the EVDLB diagnostic. The underlined portions are what the user enters into the system.

Table 3-2 DMF32 Level 3 Diagnostic Parameters

Diagnostic	EVDLB	EVDLC	EVDLD
Section Tested	Synchronous port (DMF32S)	Asynchronous port (DMF32A)	Parallel port (DMF32P)
Generic Device	XGA0	TXA	LCA
VAX Diagnostic Supervisor Version	6.6 of later	6.6 of later	6.6 or later
Running Time	1 minute	3.00 minutes (quick flag clear)	40 seconds with H3249 or LP on port
		0.5 minutes (quick flag set)	25 seconds with nothing on the port

```
DIAGNOSTIC SUPERVISOR.  ZZ-ENSAA-6.6-xxx  dd-mm-yyyy  hh:mm:ss.ss

DS] LOAD EVDLB                    ; Loads synchronous port diagnostic

DS] ATTACH DW730 HUB DW0          ; Attaches UBA to 11/730
    or
DS] ATTACH DW750 HUB DW0          ; Attaches UBA to 11/750
    or
DS] ATTACH DW780 SBI DW0 3 4      ; Attaches UBA to 11/780

DS] ATTACH DMF32S                 ; Attaches DMF32 synchronous port

DEVICE LINK? DW0                  ; The option is linked to the UBA

DEVICE NAME? XGA0                 ; The option is named XGA0

CSR? 760340                       ; The CSR address is 760340 (range
                                  ; = 760000-777776)

VECTOR? 300                       ; Vector is 300 (range = 300-766)

BR? 5                             ; BR interrupt level is 5
                                  ; (range = 5-6)

EXTERNAL WRAP? NONE               ; NONE  -  No external loopback
                                  ;          connector is connected
                                  ; WRAP  -  H3248 or H3249 loopback
                                  ;          connector is connected
                                  ; MODEM -  External modem connected

DS] SEL XGA0                      ; Selects the synchronous port to
                                  ; be run

If UNIBUS Init jumper W1 has been removed, event flag 2 must be
set before running the EVDLB diagnostic.

DS] SET EVENT 2                   ; Sets event flag 2

                          NOTE
          To run EVDLB, the S3 switches on the
          distribution panel must be set (refer to
          Section 3.1.4).

DS] START                         ; Runs the diagnostic
```

Example 3-1 Loading, Attaching, and Running EVDLB

3.2.3 EVDLC Diagnostic Description

The EVDLC diagnostic tests the asynchronous port only; it ignores devices on the synchronous and parallel ports. This diagnostic performs both DMA and SILO mode testing with either an internal or external loopback connector connected. The EVDLC diagnostic has two sections: default and manual intervention.

The default section provides for internal loopback testing when no external loopback connector is used. Also, when an H3248 single-line loopback connector or a programmable modem is used, the default section provides an external loopback path for all the modem signals. Using the H3249 staggered loopback connector provides complete functional testing of the asynchronous device.

The default parameters are as follows:

- 8 bits per character
- 1 stop bit
- Parity disabled
- Baud rate selected from attach sequence

The manual section provides for external loopback testing when a nonprogrammable modem or a remote modem is used as the loopback device. Using the remote modem verifies the communications facilities.

3.2.3.1 Loading, Attaching, and Running EVDLC – After the Diagnostic Supervisor is loaded, the operating instructions in Example 3-2 can be used for the EVDLC diagnostic. The underlined portions are what the user enters into the system.

3.2.4 EVDLD DIAGNOSTIC DESCRIPTION

The EVDLD diagnostic tests the DMF32 parallel port only; it ignores the devices on the synchronous and asynchronous ports. This diagnostic tests both the parallel interface and line printer controller functions of the DMF32. To fully test the DMF32 line printer logic, a line printer must be attached to the line printer port. To fully test the DMF32 parallel interface logic, an H3249 loopback connector must be attached to the J2 and J3 connectors.

Testing the parallel port with the H3249 loopback connector is preferred since this is the only way that the parallel interface is completely tested. When neither a line printer or H3249 staggered loopback connector is attached to the parallel port, only the control and status register tests are performed. The diagnostic CSR low byte is used to loop the data that would normally be transferred to the printer. This tests the format functions without an attached printer.

3.2.4.1 Loading, Attaching, and Running EVDLD – After the Diagnostic Supervisor is loaded, the operating instructions in Example 3-3 can be used for the EVDLD diagnostic. The underlined portions are what the user enters into the system.

```
DIAGNOSTIC SUPERVISOR.  ZZ-ENSAA-6.6-xxx  dd-mm-yyyy  hh:mm:ss.ss

DS] LOAD EVDLC                  ; Loads asynchronous port diagnostic

DS] ATTACH DW730 HUB DW0        ; Attaches UBA to 11/730
      or
DS] ATTACH DW750 HUB DW0        ; Attaches UBA to 11/750
      or
DS] ATTACH DW780 SBI DW0 3 4    ; Attaches UBA to 11/780

DS] ATTACH DMF32A               ; Attaches the asynchronous
                                ; diagnostic

DEVICE LINK? DW0                ; Option is linked to the UBA

DEVICE NAME? TXA                ; The option is named TXA (range =
                                ; A-F)

CSR? 760340                     ; The CSR address is 760340 (range =
                                ; 760000-777776)

VECTOR? 300                     ; Vector address is 300 (range =
                                ; 300-766)

BR? 5                           ; BR interrupt level is 5 (range =
                                ; 5-6)

ACTIVE LINES? 377               ; All lines to be tested (octal bit
                                ; map of lines to be tested)
                                ; bit 0 = line 0
                                ; bit 1 = line 1, etc. (range =
                                ; 000-377)

BAUD RATE? 9600                 ; Baud rate that is to be used in
                                ; external wrap tests. This parameter
                                ; determines the line speed for the
                                ; remote loopback (manual) modem test
                                ; and the single-line loopback test.
                                ; Baud rates that can be selected are
                                ; 50, 75, 110, 135, 150, 300, 600,
                                ; 1200, 1800, 2000, 2400, 3600, 4800,
                                ; 3600, 4800, 7200, 9600, 19200

WRAP TYPE? INTERNAL             ; INTERNAL - Data loopback path is
                                ;            internal to the DMF32
                                ; H3248 - Single-line loopback
                                ;         connector is connected at
                                ;         the distribution panel
                                ; H3249 - Staggered loopback
                                ;         connector is used
                                ; LOCAL MODEM - A modem manually
                                ;         selected for analog
                                ;         (local) loopback testing
                                ; PROGRAMMABLE MODEM - A modem that
                                ;         selects analog (local)
                                ;         loopback test mode when
                                ;         EIA pin 18 is asserted

UNIBUS INIT JUMPER? YES         ; YES - Jumper W1 installed on DMF32
                                ; NO  - No jumper W1

DS] SEL TXA                     ; Select the device to run
```

NOTE

The S1 and S2 switches on the distribution panel must be set (refer to Section 3.1.4) before running EVDLC.

```
DS] START                       ; Starts running the program
```

Example 3-2 Loading, Attaching, and Running EVDLC

```
DIAGNOSTIC SUPERVISOR.  ZZ-ENSAA-6.6-xxx  dd-mm-yyyy  hh:mm:ss.ss

DS] LOAD EVDLD                          ; Loads the parallel port

DS] ATTACH DW730 HUB DW0                ; Attaches UBA to 11/730
      or
DS] ATTACH DW750 HUB DW0                ; Attaches UBA to 11/750
      or
DS] ATTACH DW780 SBI DW0 3 4            ; Attaches UBA to 11/780

DS] ATTACH DMF32P                       ; Attaches the parallel port
                                        ; diagnostic

DEVICE LINK? DW0                        ; The option is linked to
                                        ; the UBA

DEVICE NAME? LCA                        ; The option is named LCA

CSR] 760340                             ; The CSR address is 760340
                                        ; (range = 760000-777776)

VECTOR? 300                             ; Vector address is 300
                                        ; (range = 300-776)

BR? 5                                   ; BR interrupt level is 5
                                        ; (range = 5-6)

PORT DEVICE? OTHER                      ; OTHER - Other than an H3249
                                        ;         staggered loopback
                                        ;         connector or line
                                        ;         printer is
                                        ;         connected
                                        ; LP - Line printer is
                                        ;      connected
                                        ; WRAP - H3249 loopback
                                        ;        connector is
                                        ;        connected

DS] SEL LCA                             ; Select the parallel port
                                        ; to be run

DS] START                               ; Start running the program
```

Example 3-3 Loading, Attaching, and Running EVDLD

3.2.4.2 EVDLD Event Flags – The EVDLD diagnostic uses three event flags: EV3, EV4, and EV5. The EV3 flag indicates to the diagnostic whether DMF32 jumper W1 has been removed. The EV4 and EV5 flags control the buffer type error message printouts. Refer to Table 3-3 for the EVDLD event flags. Example 3-4 shows EVDLD Event Flag instructions.

3.3 DMF32 LEVEL 2R DIAGNOSTICS

There are two Level 2R diagnostics used to support the DMF32: EVDLA and EVDAC. Both operate under the VAX Diagnostic Supervisor (DS) with VMS. Table 3-4 lists some of the parameters for these diagnostics.

Table 3-3 EVDLD Event Flags

Event Flag State	EV3	EV4	EV5
Clear	UNIBUS Init will affect the DMF32 (jumper W1 installed)	Only first eight errors in a buffer are displayed	No effect
Set	UNIBUS Init will not affect the DMF32 (jumper W1 removed)	All errors in the buffer are displayed	Entire buffer is dumped regardless of whether the data is erroneous or not (EV4 need to be set when EV5 is set)

```
DS] SET EVENT 4,5          ; Sets event flags 4 and 5

DS] SHOW EVENTS            ; Shows all event flags that are
                           ; currently set

DS] CLEAR EVENTS 4,5       ; Clears event flags 4 and 5
```

Example 3-4 EVDLD Event Flag Instructions

Table 3-4 DMF32 Level 2R Diagnostic Parameters

Diagnostic	EVDLA	EVDAC
Section Tested	Synchronous port	Asynchronous port
Generic Device	XGA0	TXA
VMS Release	3A or later	3A or later
VAX Diagnostic Supervisor Version	6.6 or later	6.6 or later

3.3.1 Level 2R Hardware Prerequisites

The following must be functional before the Level 2R diagnostics may be used.

- VAX-11 CPU
- Memory (128 KB minimum)
- UNIBUS adapter (DW730, DW750, or DW780, as applicable)
- Green LED on the DMF32 must be illuminated

3.3.2 EVDLA Diagnostic Description

The EVDLA provides integrity testing and fault detection for the synchronous device while operating under VMS. The operating system (VMS) produces the error reports, which identify the failing functional area of the synchronous device, and the status reports of the synchronous device.

3.3.2.1 Loading, Attaching, and Running EVDLA – The instructions in Example 3-5 are used to load, attach, and run EVDLA. It is assumed that VMS is already loaded. Again, user input is underlined.

3.3.3 EVDAC Diagnostic Description

The EVDAC diagnostic tests the functionality of the asynchronous multiplexer while operating under VMS. This diagnostic has two selectable sections: default and link.

The default section is used for all normal testing. The link section is used for link testing. The EVDAC diagnostic exercises a DMF32 that is linked to another DMF32 (even in the same system) which is also running EVDAC.

3.3.3.1 Loading, Attaching, and Running EVDAC – The instructions in Example 3-6 are used to load, attach, and run EVDAC. It is assumed that VMS is already loaded.

```
$ RUN EVDLA                          ; Start supervisor (11/780 = ESSAA,
                                     ; 11/750 = ECSAA, 11/730 = ENSAA)

DIAGNOSTIC SUPERVISOR.  ZZ-ENSAA-6.6-xxx  8-FEB-1982  09:40:14.80

DS] ATTACH DW780 SBI DW0 3 4         ; Attaches the UBA on the SBI
    or                               ; VAX-11/780

DS] ATTACH DW750 HUB DW0             ; For VAX-11/750 testing
    or
DS] ATTACH DW730 HUB DW0             ; For VAX-11/730 testing

DS] LOAD EVDLA                       ; Loads the EVDLA program

DS] ATTACH DMF32S                    ; Attaches the synchronous
                                     ; diagnostic

DEVICE LINK? DW0                     ; The option is linked to the UBA

DEVICE NAME? XGA0                    ; The option is named XGA0 (range =
                                     ; A-F)

CSR? 760340                          ; The CSR address is 760340 (range =
                                     ; 760000-777776)

VECTOR? 300                          ; Vector address is 300 (range =
                                     ; 300-776)

BR? 5                                ; BR interrupt level is 5 (range =
                                     ; 5-6)

WRAP TYPE? NONE                      ; NONE  - No external backloop
                                     ;         connector or modem
                                     ; WRAP  - External backloop
                                     ;         connector is connected
                                     ; MODEM - External modem is
                                     ;         connected

DS] SEL XGA0                         ; Select the synchronous port

DS] START                            ; Start running EVDLA without either
    or                               ; an external loopback connector or
                                     ; a modem

DS] START/SELECTION:CABLE            ; External loopback connector is
    or                               ; connected

DS] START/SECTION:MODEM              ; External modem is connected
```

Example 3-5 Loading, Attaching, and Running EVDLA

```
$ ALLOCATE TXA(N)              ; Allocate all lines to be tested

$ RUN ENSAA                    ; Start supervisor (11/780 = ESSAA
                               ; 11/750 = ECSAA, 11/730 = ENSAA)

DIAGNOSTIC SUPERVISOR.  ZZ-ENSAA-6.6-xxx  8-FEB-1982  09:40:14.80

DS] ATTACH DW780 SBI DW0 3 4   ; Attaches the UBA on the SBI
    or                         ; VAX-11/780
DS] ATTACH DW750 HUB DW0       ; For VAX-11/750 testing
    or
DS] ATTACH DW730 HUB DW0       ; For VAX-11/730 testing

DS] LOAD EVDAC                 ; Loads the EVDAC program

DS] ATTACH DMF32A              ; Attaches the asynchronous
                               ; diagnostic

DEVICE LINK? DW0               ; The option is linked to the UBA

DEVICE NAME? TXA               ; The option is named TXA (range =
                               ; A-F)

CSR? 760340                    ; The CSR address is 760340 (range =
                               ; 760000-777776)

VECTOR? 300                    ; Vector address is 300 (range =
                               ; 300-776)

BR? 5                          ; BR interrupt level is 5 (range =
                               ; 5-6)

ACTIVE LINES? 377              ; All lines 0-7 to be tested
                               ; (octal bit map of lines to be
                               ; tested)
                               ; bit 0 = line 0,
                               ; bit 1 = line 1, etc. (range =
                               ; 000-377)

BAUD RATE? 9600                ; Baud rate that is to be used in
                               ; external wrap tests.  Baud rates
                               ; that can be selected are 50, 75,
                               ; 110, 135, 150, 300, 600, 1200, 1800
                               ; 2000, 2400, 3600, 4800, 7200, 9600,
                               ; 19200

WRAP TYPE? INTERNAL            ; INTERNAL - Wrapped internally at
                               ;            the UART
                               ; H3248 - Single-line wrap at the
                               ;         distribution panel
                               ; LOCAL MODEM - Modem with internal
                               ;               wrap
                               ; PROGRAMMABLE MODEM - A modem which
                               ;     diagnostics can set to internal
                               ;     wrap by setting the User
                               ;     Transmit Modem signals

UNIBUS INIT JUMPER? YES        ; Jumper on DMF32 module that
                               ; inhibits UNIBUS Inits

DS] SEL TXA                    ; Selects the asynchronous port to
                               ; be run

DS] START                      ; Start program running
```

Example 3-6 Loading, Attaching, and Running EVDAC

4 PROGRAMMING

4.1 INTRODUCTION

The DMF32 consists of four distinct devices. Each device is programmed independent of the other three devices, since each device contains its own set of registers. There are only two registers that are common to the DMF32: CSR 0 and CSR 1.

4.1.1 DMF32 CSR 0

The operating system uses CSR 0 at AUTOCONFIGURE time. CSR 0 contains a 4-bit code that indicates to the operating system which three of the four devices are available for operation. The parallel interface (DR) and the line printer controller (LP) cannot operate concurrently.

The DMF32 uses two dip switches to select the desired devices: switches 4 and 5 on switch pack 3 on the distribution panel. Refer to Table 2-7 for the valid switch setting combinations. These two switches, which are read by the DMF32, should be set before power up, since the microcode samples these switches only once after power up.

After power up, the program can write to CSR 0 bits ⟨15:12⟩ to change the device code to another valid combination. For example, to switch a diagnostic program from DR to LP or LP to DR without human intervention, execute a WRITE WORD (MOVW) instruction to CSR 0 bits ⟨15:0⟩. The WRITE WORD overwrites the base interrupt vector which occupies the low byte of CSR 0. To load the interrupt vector (CSR 0 high byte) without affecting the CSR 0 high byte (device available bits), execute a BYTE output instruction (MOVB). This MOVB instruction loads the low byte of CSR 0, regardless of whether the high or low byte is accessed.

Also at AUTOFIGURE time, the operating system loads the value of the first interrupt vector into CSR 0. There are no switches on the DMF32 for interrupt vectors. The DMF32 determines the value of the other seven interrupt vectors as contiguous with a greater value than the first vector in CSR 0. Table 4-1 lists the vectors.

Figure 4-1 shows the bit configurations for CSR 0; Table 4-2 defines the CSR 0 bit functions.

Table 4-1 DMF32 Floating Vectors

Vector Number	Vector	Vector Value (Octal)
0	Synchronous interface receive	Base (CSR 0 bits ⟨9:0⟩)
1	Synchronous interface transmit	Base + 4
2	Parallel interface vector A	Base + 10
3	Parallel interface vector B	Base + 14
4	Asynchronous multiplexer receive	Base + 20
5	Asynchronous multiplexer transmit	Base + 24
6	Line printer controller	Base + 30
7	Not used	Base + 34

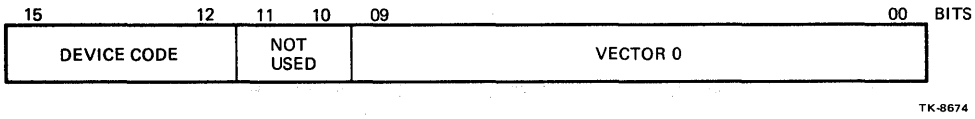

Figure 4-1 CSR0

Table 4-2 CSR 0 Bit Functions

Bit	Title	Function
⟨15:12⟩	Device code	These bits select between parallel interface or line printer operation (defined in Table 4-3).
⟨11:8⟩	Not used	Reserved for future use (always written and read as zeros).
⟨7:0⟩	Interrupt Vector	Contains the first interrupt vector (read/write).

Table 4-3 Device Selection

Device Code	Selected Device
1000	Async only
1010	Async and line printer
1101	Async, sync, and parallel interface
1110	Async, sync, and line printer

4.1.2 DMF32 CSR 1 Diagnostic Register

CSR 1 is used for diagnostic purposes. What is loaded into the high byte of CSR 1 determines the function performed. Table 4-4 lists the different functions.

Reading CSR 1 clears the low byte of CSR 1. This low byte is used in LP maintenance mode.

4.1.3 DMF32 Device Control Status Registers

The floating control status registers of the four devices (synchronous interface, asynchronous multiplexer, line print controller, and parallel interface) reside in a contiguous block of 16 words. A dip switch pack (E77) on the DMF32 determines the starting address of the block. These registers can only be accessed by word, except for the register used to access a transmit silo of an asynchronous line, and the parallel interface output buffer when in DR11-C functional mode. Access by word means that the instruction that operates on the register causes a data out (DATO) rather than a data out byte (DATOB) UNIBUS cycle. The DMF32 ignores the least significant UNIBUS address bit on registers that are word-access only, and therefore treats a DATOB as a DATO for these registers.

4.2 SYNCHRONOUS INTERFACE

The synchronous interface is a serial line that transfers data from main memory directly (DMA). Since the DMF32 stores the UNIBUS addresses and byte counts, each 16-bit transfer (two character) to and from main memory requires only one memory reference. Both the transmitter and receiver have two sets of byte count registers and buffer address registers. After one message has been transferred between the main memory and synchronous interface, the second message can start immediately even if the CPU has not been notified of completion of the first message. BR level interrupts signal the completion of transfers, modem status changes, and error conditions.

Table 4-4 CSR 1 High Byte Functions

CSR 1 High Byte (HEX) Contents	Diagnostic Function
55	Forces a parity error. A parity error causes the green LED on the DMF32 to go off, and inhibits microcode execution. In this state, DMF32 registers cannot be accessed. To restart execution, UNIBUS signals DC LO or INIT must be asserted.
AA	Starts execution at location 0000. Location 0000 is where execution begins after a UNIBUS DC LO or INIT. This feature allows program controlled initiation of the powerup self test.
2A	CSR 1 high byte contains the microcode REV level. To read the REV level number, 2A (hex) must be written to CSR 1 bits ⟨15:8⟩, then a read of CSR 1 bits ⟨15:8⟩ will obtain the REV level. The number is stored in BCD and there are two digits in the byte.
AA	The self test has successfully completed.

4.2.1 Synchronous Interface Protocol Support

The synchronous interface supports both bit-oriented protocols (SDLC and HDLC) and byte-oriented protocols (DDCMP). The synchronous interface performs bit stuffing, bit removal, and control character generation and recognition. The program loads registers in the DMF32 to specify the protocol, error control, and the number of bits per character.

Byte-oriented protocols not supported by the synchronous interface may be implemented by running the general byte-oriented synchronous (GEN BYTE) protocol. This protocol is not really a protocol, but implements a straight transfer of data between main memory and the synchronous interface. In this way, the software can perform protocol-specific functions.

4.2.2 Synchronous Interface Baud Rate

Using the crystal controlled baud rate generator, the synchronous line can be programmed to transmit at one of eight different speeds up to 19,200 bps. Any transmit or receive bit rate up to 19,200 bps can be used with external clocking. The receiver uses an external clock input from the modem, except during maintenance testing.

4.2.3 Synchronous Interface Device Registers

The synchronous interface uses four device registers and 16 indirect registers. The four device registers are as follows:

- Receive control status register
- Transmit control status register
- Miscellaneous register
- Data set change flag register

4.2.3.1 Receive Control Status Register – The receive control status register enables the following:

- The receiver
- The match character (GEN BYTE)
- The receive interrupt
- The local loop (maintenance testing)
- Strip sync

It also indicates the following:

- The selected receive buffer address register
- The receiver is active
- The received message has been transferred to the secondary receive buffer
- Residual bit count does not equal zero (HDLC, SDLC)
- If the DMF32 is either a primary or secondary station (HDLC, SDLC), or a control station, or tributary station (DDCMP)
- A receive error
- The received message has been transferred to the primary receive buffer

4.2.3.2 Transmit Control Status Register – The transmit control status register enables the following:

- NPR request (primary and secondary)
- Interrupt request when the data set change bit is set
- Interrupt request when either transmit done primary, transmit done secondary, or transmit error bit is set

It also indicates the following:

- The selected transmit buffer address register and character count registers
- The transition of any of the data set change bits
- The message from secondary data buffer has been transferred to the synchronous interface
- Transmit error
- The message from primary data buffer has been transferred to the synchronous interface

The transmit control status register controls the state of the serial line when a transmit underrun occurs and selects the transmit clock source.

4.2.3.3 Miscellaneous Register – The miscellaneous register performs the following:

- Selects one of the 16 indirect registers
- Initiates a Master Reset

4.2.3.4 Data Set Change Flag Register – The data set change flag register indicates which of the following receive modem signals have changed:

- Carrier detect
- Ring indicator
- Data set ready
- Clear to send
- User receive

4.3 SYNCHRONOUS OPERATION

The synchronous interface is ready for operation after the following is performed. The program loads the interrupt vectors into the first CSR of the DMF32. Next, the powerup Master Reset is performed. After a Master Reset (or DC LO or INIT), the transmitter and receiver are disabled and the transmitter is held marking. The protocol parameter register (indirect register [0] bits ⟨7:0⟩) and transmit/receive BPC (bits per character) registers (indirect register [0] bits ⟨15:8⟩) should now be loaded by the program; the Master Reset should also be set. After the Master Reset bit clears, the program should load any parameter(s) and enables the transmitter and receiver.

4.3.1 Synchronous Transmit Operation

For byte-oriented protocols, the program should load both the sync register (indirect register [3] bits ⟨15:8⟩) and the number-of-syncs register (indirect register [3] bits ⟨7:0⟩). The sync register contains the character used for the transmit and receive synchronization. The number-of-syncs register contains the number of sync characters to be transmitted prior to the message. For bit-oriented protocols, the standard "flag" character is used for transmit and receive synchronization.

4.3.1.1 Pretransmission Considerations – Before data is transmitted from a buffer, the following is performed. The program sets the primary/secondary bit (transmit CSR bit ⟨2⟩) to indicate whether the primary buffer address register (indirect register [10]) or secondary buffer address register (indirect register [12]), and the character count register (indirect register [11] or [13]) are to be used. Next, the program loads the appropriate buffer address and character count registers. If there is more than one message to be transmitted, both the primary and secondary registers are loaded. A buffer transfer can start and finish on any byte boundary. A pair of word aligned bytes are direct memory accessed two bytes at a time via the UNIBUS.

4.3.1.2 Initiating Transmission – Assume the primary character count and buffer address registers are active. After loading these registers, the transmit enable bit should be set to start the DMA transfer of characters from main memory to the synchronous interface. Setting the transmit enable bit clears all transmit error bits. Loading the primary or secondary character count register clears the transmit done primary bit or the transmit done secondary bit respectively.

4.3.1.3 Synchronous Interface Data Transmission – The synchronous interface acts on the bytes to be transmitted according to the specific protocol used. After a successful DMA transfer and message transmission, the transmit done primary bit is set. If the transmit interrupt enable bit is active, setting the transmit done primary bit causes an interrupt to the transmit vector.

If the message is aborted due to an error condition, the transmit error bit is set, while the transmit enable bit is cleared. The transmit primary/secondary bit always changes to one state. The transmit primary/secondary bit is changed to one state to indicate that the secondary character count and buffer address registers are now active.

If transmit done secondary bit is set, then the synchronous interface becomes idle (transmit enable bit does not clear) and waits for transmit done secondary bit to be cleared by the software loading the secondary character count register. If the transmit done secondary bit is clear, the secondary buffer processing begins.

While the secondary buffer data is being transferred to the synchronous interface to be transmitted, the program should service the transmit done primary interrupt. If there is another message to be transmitted, the primary buffer address should be loaded with the address of the message buffer; then the primary character count register should be loaded with the message size in bytes. Loading the primary character count register clears the transmit done primary bit. This double buffering scheme results in high message throughput without any stringent requirements on interrupt latency. The CPU has a full message transmission time to service an interrupt.

4.3.1.4 Synchronous Interface Transmission Errors – Transmit error conditions abort the transmitted message. Aborting the transmitted message sets the done bit pointed to by the transmit primary/secondary bit. The transmit error bit is set and the transmit enable bit is cleared.

The transmit error bits ⟨2:0⟩ (indirect register [2]) indicate the cause of the transmitted error. The following are transmit errors:

- Transmit underrun error. The synchronous interface could not get and process characters fast enough to sustain the baud rate.

- DMA error. The synchronous interface UNIBUS controller either did not receive a SSYN at least 32 μs after issuing a MSYN, or the controller could not become bus master for at least 32 μs after having asserted BUS NPR.

- Transmit message length error. The character count indicates a buffer length too small for the message of the particular protocol. This error may be detected before transmission begins (for example, SDLC frame under four characters).

4.3.2 Synchronous Receiver Operation

After a Master Reset or INIT, the synchronous receiver is disabled. To receive messages, the program sets the receive primary/secondary bit (receive CSR bit ⟨2⟩) to indicate whether the primary or secondary buffer address register (indirect register [6] or [8]), primary or secondary count register (indirect register [7] or [9]) are to be used. The program loads the appropriate receive buffer address and receive character count register (both primary and secondary registers can be loaded). Loading the primary or secondary character count registers clears the primary or secondary done bit, respectively. A receive buffer can start and finish on any byte boundary. A pair of word-aligned bytes are transferred two at a time.

4.3.2.1 Synchronous Receiver Synchronization – Assume the primary character count and buffer address registers are active. After loading these registers, the receiver enable bit should be set to search for character synchronization. For byte-oriented protocols, receiving two successive sync characters (the character programmed in sync register bits ⟨7:0⟩) causes synchronization. Bit-oriented protocols are synchronized when a "flag" character signals the beginning of a frame. Setting receiver enable bits clears all the receive error bits.

4.3.2.2 Synchronous Interface Data Reception – The way the synchronous interface acts upon the received bytes depends upon the specific protocol used. After a successful DMA transfer and message reception, the receive done bit is set. If the receive interrupt enable bit is active, setting the receive done primary bit causes an interrupt to the receive vector. If the message is aborted due to an error condition, the receive error bit is set, and the receive enable bit is cleared.

After the receive done primary bit or error bit are set, the receive primary/secondary bit changes to a one to indicate that the secondary character count and buffer address registers are now active. If the receive done secondary bit is set, the synchronous interface becomes idle (receive enable bit remains set) and no more messages are received. When the receive done secondary bit and receive error bit are both clear, the received message is loaded into the secondary buffer.

While the receive data is being transferred to the synchronous interface and then to the secondary buffer in main memory, the program should service the receive done primary interrupt. As part of this service, the primary buffer address register should be loaded with the buffer address of the message, and the primary character count register should be loaded (clearing the receive done primary bit) with the maximum possible message size in bytes.

4.3.2.3 Synchronous Interface Receiver Errors – Receive error conditions abort received messages. An aborted receive message sets the receive error bit. Receive error bits ⟨7:0⟩ indicate the cause of the receive error. The possible receive error conditions are as follows:

- Receive overrun error (The synchronous interface could not process and transfer the received characters to main memory fast enough. This would result if the synchronous interface was operating at too high a baud rate.)
- DMA error (The synchronous interface UNIBUS controller did not receive SSYN at least 32 μs after issuing a MSYN, or the controller could not become bus master for at least 32 μs after having asserted BUS NPR.)
- Receive block check error
- Receive VRC error
- Receive abort character
- Receive overflow (The received message is too big for the buffer space allocated to it.)

An error condition that aborts a receive message changes the state of the receive primary/secondary bit and clears the receive enable bit.

4.4 SYNCHRONOUS INTERFACE DEVICE REGISTERS

The synchronous interface uses four device registers and 16 indirect registers. The four device registers are as follows:

- Receive control status register
- Transmit control status register
- Miscellaneous register
- Data set change flag register

4.4.1 Receive Control Status Register

The receive control status register has an address of base +4. Read/modify/write UNIBUS cycles are allowed. Access is by word only.

Figure 4-2 shows the bit format of the receive control status register. Table 4-5 describes the functions of the receive control status register.

4.4.2 Transmit Control Status Register

The transmit control status register has an address of base +6. Read/modify/write UNIBUS cycles are allowed. Access is by word only.

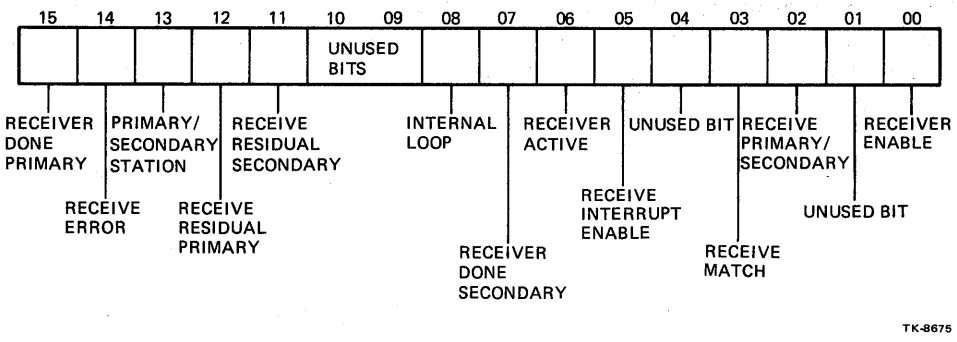

Figure 4-2 Synchronous Receive CSR

Table 4-5 Synchronous Receive Control Status Register Functions

Bits	Title	Function
⟨0⟩	Receiver Enable	When set, this bit enables processing of the receiver serial input data. When the receiver enable bit becomes asserted, the receiver is enabled to search for synchronization provided that the done bit pointed to by the transmit primary/secondary bit is clear. When the receiver enable bit is cleared, the receiver logic is disabled. The transition of the receiver enable bit from a zero to a one state clears the receive error bits. Only the program can change the state of the receiver enable bit from a zero to a one. The receiver enable bit is read/write and is cleared by: • Master Reset or INIT. • setting either receiver abort, receiver DMA error, receiver overrun, receiver VRC, receiver overflow, or receiver BCC error.
⟨1⟩	Unused Bit	
⟨2⟩	Receive Primary/ Secondary	This bit indicates which receive buffer address register is being used (primary receive buffer address register bits ⟨17:0⟩ or secondary receive buffer address register bits ⟨17:0⟩). It also indicates which receive character count register (primary receive character count register bits ⟨13:0⟩ or secondary receive character count register bits ⟨13:0⟩) will be used.

Table 4-5 Synchronous Receive Control Status Register Functions (Cont)

Bits	Title	Function
		A zero state indicates that the primary registers are active; a one state indicates that the secondary registers are active. When the NPR transfer of received data is terminated (successfully or unsuccessfully), the receive primary/secondary bit changes state to indicate the new active receive buffer. However, if the new buffer's receiver done bit is not clear, the receiver becomes idle until the done bit is cleared. If the new buffer's done bit is not clear, it means the CPU has not yet processed the previous message in this new buffer. The done bit is cleared by software loading the character count register. This bit is read/write and is cleared by a Master Reset or INIT.
⟨3⟩	Receive Match Character	This bit is used only when running the GEN BYTE protocol. When this bit is set, the character stored in the match character register bits ⟨7:0⟩ is used as the match character for generating an interrupt. All received characters in the message are compared with the characters stored in the match character register bits ⟨7:0⟩. If a match is found, a receive interrupt is posted informing the driver that the special character has arrived. Finding a match only causes an interrupt. After the match, characters continue to be received and direct memory accessed. There may be multiple matches and corresponding interrupts in a message. This bit is read/write, and is cleared by a Master Reset or INIT. This bit is always read as zero.
⟨4⟩	Unused Bit	
⟨5⟩	Receiver Interrupt Enable	When set, bit ⟨5⟩ enables interrupt requests to the receive vector if the receive done primary bit (receive CSR bit ⟨15⟩), receive done secondary bit (receive CSR bit ⟨7⟩, or receive error bit (receive CSR bit ⟨14⟩) is set. This bit is read/write and is cleared by a Master Reset or INIT.
⟨6⟩	Receiver Active	When set, this bit indicates that the synchronous interface is processing a message. The synchronous interface clears this bit upon completion of the message transfer. This bit is read-only and is cleared by a Master Reset, an INIT, or the negation of the receive enable bit (receive CSR bit ⟨0⟩).

Table 4-5 Synchronous Receive Control Status Register Functions (Cont)

Bits	Title	Function
⟨7⟩	Receiver Done Secondary	This bit is set after the synchronous interface has received a message. Since the DMF32 has some on-board buffering, the receiver done secondary bit may be set while the DMF32 still contains characters to be direct memory accessed. However, if the receiver interrupt enable bit is set, an interrupt to the receive vector is posted only after all the characters have been direct memory accessed to main memory. This bit is read-only and is cleared by loading the secondary receive character count register bits ⟨13:0⟩. A Master Reset or INIT sets this bit.
⟨8⟩	Internal Loop	Bit ⟨8⟩ generates a local loop for use in maintenance testing (refer to Table 4-6).

Table 4-6 Internal Loop

Bit ⟨8⟩	State	Definition
	0	No internal loop. The transmitter serial output is connected to EIA RS-232-C circuit BA, Transmitted Data. The receiver serial input is connected to EIA RA-232-C circuit BB, Received Data.
	1	Use internal loop. The transmitter serial output is connected to the receiver serial input. EIA RS-232-C circuit BA, Transmitted Data is held marking, while EIA RA-232-C circuit BB, Received Data, is ignored. The receiver uses the selected transmit clock. This bit is read/write and is cleared by a Master Reset or INIT.
⟨10:9⟩	Unused Bits	These two bits are always read as zeroes.
⟨11⟩	Receive Residual Secondary	This bit is used for bit-oriented protocols only. The receive residual secondary bit is set whenever the residual bit count (secondary bits ⟨2:0⟩) does not equal zero. After the receiver done secondary bit is set, the receiver residual secondary bit should be inspected. If the receiver residual secondary bit is clear, then all of the bits in the last character are part of the message. However, if the receiver residual secondary bit is set, then only some of the bits in the last character are part of the message. The residual bit count bits ⟨2:0⟩ needs to be inspected to determine how many bits are part of the message.

Table 4-6 Internal Loop (Cont)

Bit ⟨8⟩	State	Definition
		Receive residual secondary bit is read only, and is cleared by either a Master Reset, INIT, or by writing to the secondary receive character count register.
⟨12⟩	Receive Residual Primary	This bit is used for bit-oriented protocol only. The receive residual primary bit is set whenever the residual bit count (bits ⟨2:0⟩) does not equal zero. After the done primary bit is set, the receive residual primary bit should be inspected. If the receive residual primary bit is clear, then all of the bits in the last character are part of the message. However, if receive residual primary bit is set, only some of the bits in the last character are part of the message. The residual bit (bits ⟨2:0⟩) needs to be inspected to determine how many bits are part of the message. The receive residual primary bit is read only and is cleared by either a Master Reset, INIT, or by writing to the primary receive character count register.
⟨13⟩	Primary/ Secondary Station	For SDLC and HDLC protocol: When bit ⟨13⟩ is clear, the synchronous interface acts as primary station. If this bit is set, the synchronous interface acts as a secondary station. For DDCMP protocol: When bit ⟨13⟩ is clear, the synchronous interface acts as a control station. If this bit is set, the synchronous interface acts as a tributary station. This bit is read/write and is cleared by a Master Reset or INIT.
⟨14⟩	Receive Error	Bit ⟨14⟩ is the inclusive OR of all the error bits in the receiver error register. Setting the receive error bit clears the receive enable bit, and also causes an interrupt to the receive vector if the receive interrupt enable bit is set. This bit is read-only and is cleared by a Master Reset, an INIT, or by reading receiver error register (indirect register [1] bits ⟨7:0⟩).

Table 4-6 Internal Loop (Cont)

Bit ⟨8⟩	State	Definition
⟨15⟩	Receiver Done Primary	This bit is set after the synchronous interface has received a message. Since the DMF32 has some on-board buffering, the receiver done primary bit may be set while the DMF32 still contains characters to be direct memory accessed. However, if the receiver interrupt enable bit is set, an interrupt to the receive vector is posted only after all the characters have been direct memory accessed to main memory. This bit is read-only and is cleared by loading the primary receive character count register (primary receive character count bits ⟨13:0⟩). A Master Reset or INIT sets this bit.

Figure 4-3 shows the bit format of the transmit control status register. Table 4-7 describes the functions of the transmit control status register.

4.4.3 Miscellaneous Register

The miscellaneous register performs the following:

- Selects one of the 16 indirect registers
- Initiates Master Reset

The miscellaneous register has an address of base +8. Read/modify/write UNIBUS cycles are allowed. Access is by word only.

Figure 4-4 shows the bit format of the miscellaneous register. Table 4-9 describes the functions of the miscellaneous register.

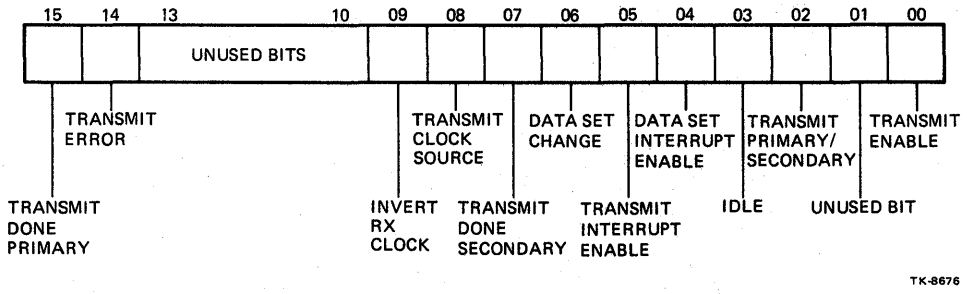

Figure 4-3 Synchronous Transmit CSR

Table 4-7 Synchronous Transmit Control Status Register Functions

Bits	Title	Function
⟨0⟩	Transmit Enable	When set, this bit enables character transmission if the done bit pointed to by the transmit primary/secondary is clear. The primary or secondary done bit is automatically cleared when the software loads the primary or secondary character count register, respectively. The transition of transmit NPR enable bit from zero to one clears the transmit error bits. For any protocol, if the the software clears the transmit enable bit in the middle of message transmission, the following happens: • The transmit error bit sets • The active done bit sets • An interrupt is generated (if the transmit interrupt enable bit is set) • None of the bits in the transmit error register bits ⟨7:0⟩ are set The transmit NPR enable bit is read/write and is cleared by the following: • Performing a Master Reset or INIT. • Setting transmitter DMA error bit, transmit underrun bit, or transmit character length bit.
⟨1⟩	Unused Bit	This bit is always read as a zero.
⟨2⟩	Transmit Primary/ Secondary	This bit indicates which of the transmit buffer address registers (indirect register [10] or indirect register [12]) and transmit character count registers (indirect register [11] or indirect register [13]) are being used or are to be used. A zero bit indicates that the primary registers are active; a one bit indicates that the secondary registers are active. When the NPR transfer of transmitted data is terminated (successfully or unsuccessfully), then the transmit primary/secondary bit changes state, which indicates the new active transmit buffer. Bit ⟨2⟩ is read/write and is cleared (indicating primary registers active) by a Master Reset or INIT.

Table 4-7 Synchronous Transmit Control Status Register Functions (Cont)

Bits	Title	Function
⟨3⟩	Idle	Bit ⟨3⟩ controls the state of the serial line between messages. For byte-oriented protocols, the serial line sends sync characters, or marks, depending on whether the idle bit equals 0 or 1, respectively. For bit-oriented protocols, the serial line marks or transmits flag characters, depending on whether the idle bit equals 0 or 1, respectively. If the transmit enable bit (synchronous CSR bit ⟨0⟩) is cleared by software immediately after a message has been successfully transmitted, the line may mark until the transmit bit is set again, independent of the idle bit. This bit is read/write and is cleared by a Master Reset or INIT.
⟨4⟩	Data Set Interrupt Enable	When set, this bit enables interrupt requests to be made to the transmit vector if the data set change bit (synchronous transmit CSR bit ⟨6⟩) is set. The data set interrupt enable bit is read/write and is cleared by a Master Reset or INIT.
⟨5⟩	Transmit Interrupt Enable	When set, this bit enables the interrupt requests to the transmit vector if either the transmit done primary bit (transmit CSR bit ⟨15⟩), transmit done secondary bit (transmit CSR bit ⟨7⟩) or transmit error bit (transmit CSR bit ⟨14⟩) becomes set. Bit ⟨5⟩ is read/write and is cleared by a Master Reset or INIT.
⟨6⟩	Data Set Change	Bit ⟨6⟩ is set by the ON-to-OFF or OFF-to-ON transition of any of the following bits: • Ring indicator • Carrier detect • Data set ready • Clear to send • User receive If the data set interrupt enable bit (transmit CSR bit ⟨4⟩) is set, setting data set change bit (transmit CSR bit ⟨6⟩) causes an interrupt request to the transmit vector. The program may read the data set change flag register to determine which modem lines have changed. Bit ⟨6⟩ is read-only; it is cleared by reading the modem receive register (indirect register [4]) and by a Master Reset or an INIT.

Table 4-7 Synchronous Transmit Control Status Register Functions (Cont)

Bits	Title	Function
⟨7⟩	Transmit Done Secondary	This bit is set after a message has been transferred from the secondary data buffer in main memory to the synchronous interface. Setting this bit causes an interrupt to the transmit vector if the transmit interrupt enable bit (transmit CSR bit ⟨5⟩) is set. Bit ⟨7⟩ is read/write and is cleared by writing to the secondary transmit character count register (indirect register [13] bits ⟨13:0⟩). This bit is set by either Master Reset or INIT.
⟨8⟩	Transmit Clock Source	Bit ⟨8⟩ selects the clock source for the transmitter. Refer to Table 4-8 for definitions.

Table 4-8 Transmit Clock Source Definitions

Bits	Bit ⟨8⟩ State	Definition
	0	Uses the clock from the modem. This is an EIA RS-232-C circuit DB, Transmission Signal Element Timing (DCE Source). EIA RS-232C circuit DA, Transmit Signal Element Timing (DTE Source) is held marking.
	1	Uses the internal transmit baud rate generator, with the baud rate specified in transmit baud rate generator register (indirect register [2] bits ⟨11:8⟩). The output of the baud rate generator is connected to EIA RS-232C circuit DA, Transmit Signal Element Timing (DTE Source). This read/write bit is cleared by a Master Reset or INIT.
⟨9⟩	Invert Receive Clock	If this bit is set, the receiver clock signal (when not in internal loop mode) is inverted. This function is used for testing. This bit is read/write and is cleared by a Master Reset or INIT.
⟨13:10⟩	Unused Bits	These bits are always read as zeroes.

Table 4-8 Transmit Clock Source Definitions (Cont)

Bits	Bit ⟨8⟩ State	Definition
⟨14⟩	Transmit Error	This bit is the 'inclusive OR' of all error bits in the transmit error register (indirect register [2] bits ⟨7:0⟩). As the transmit error bit (transmit CSR bit ⟨14⟩) is set, an interrupt to the transmit vector is requested, if transmit interrupt enable bit (transmit CSR bit ⟨5⟩) is set. Transmit error bit (transmit CSR bit ⟨14⟩) is the logical 'inclusive OR' of the following signals: • Transmit DMA error • Transmit underrun error • Transmit message length The transmit error bit is read-only; it is cleared by reading the transmit error register (indirect register [2] bit ⟨7:0⟩), by a Master Reset, or by an INIT.
⟨15⟩	Transmit Done Primary	Bit ⟨15⟩ is set after a message is transferred from the primary data buffer in main memory to the synchronous interface. Setting this bit causes an interrupt to the transmit vector if the transmit interrupt enable bit (transmit CSR bit ⟨5⟩) is set. This bit is read only and is cleared by writing to the primary transmitter character count register (indirect register [11] bits ⟨13:0⟩). This bit is set by either a Master Reset or INIT.

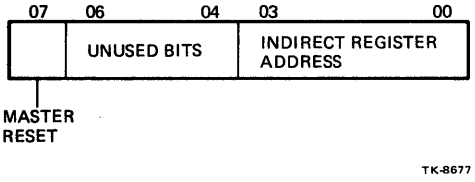

Figure 4-4 Miscellaneous Register

Table 4-9 Miscellaneous Register Functions

Bits	Title	Function
⟨3:0⟩	Indirect Register Address	These read/write bits point to one of 16 indirect registers. These registers are accessible by word only, and are accessed through address base + A. A write to an indirect register causes indirect register address field (miscellaneous register bits ⟨3:0⟩) to increment by one. Successive indirect registers may be loaded by successive UNIBUS writes or read/modify/write cycles. The indirect register is cached when the indirect register address is written to or changed. Therefore, the indirect register address should always be written to prior to a read from the indirect register. Not writing to the indirect register address causes multiple reads of the same clock in the indirect register. Writing to the indirect register causes the indirect register address to increment. The data pointed to by the incremented indirect register address is automatically cached in the indirect register. Table 4-11 lists the indirect registers. Bits ⟨3:0⟩ are not necessarily affected by a Master Reset or INIT.
⟨6:4⟩	Unused Bits	
⟨7⟩	Master Reset	When the program sets this bit, a Master Reset is initiated. This bit remains set while the reset is in progress and clears automatically after the reset has completed. The program should not access synchronous device registers except for the miscellaneous register, while the reset is in progress. The program can write a one to the Master Reset bit while the reset is in progress, but the DMF32 ignores it because the reset is already in progress. A Master Reset initializes various CSR bits as specified in the bit descriptions. The transmitter is held marking, the receiver is disabled, and the interface is set up to emulate the protocol specified in protocol parameter register (indirect register [0] bits ⟨7:0⟩). Character count and buffer address registers are not affected by a Master Reset.

4.4.4 Data Set Change Flag Register

Figure 4-5 shows the data set change flag register bit format.

This register indicates which receive modem signals the DMF32 detects as having made a transition. This register can be used to identify a modem line that has experienced a rapid sequence of two transitions. For example, if the carrier is lost for a short period, the carrier detect will go off and then go on again. However, by the time the program reads the respective modem receiver register, carrier detect may have returned to its original state. Without further information, the program could not identify which modem receive signal experienced this momentary transition. The data set change flag register provides this additional information by flagging the modem receive signal that changed.

The data set change flag register is read-only and is automatically cleared by a program read of the modem receive register (indirect register [4] bits ⟨7:0⟩). It is also cleared by a Master Reset or an INIT. Table 4-10 lists the receive modem signals.

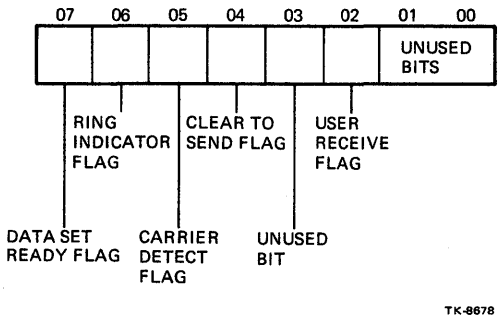

Figure 4-5 Data Set Change Flag Register

Table 4-10 Receive Modem Signals

Data Set Change Flag Register Bit	Modem Signal
7	Data set ready flag
6	Ring indicator flag
5	Carrier detect flag
4	Clear to send flag
3	Unused bit
2	User receive flag
⟨1:0⟩	Unused bits

4.5 SYNCHRONOUS INDIRECT REGISTERS

Bits ⟨3:0⟩ of the miscellaneous register addresses one of the 16 indirect registers. A write to one of these indirect registers increases the address of the indirect registers by one. Table 4-11 lists the indirect registers.

An indirect register is cached whenever the indirect register address register is written to or changed. Therefore, the indirect register address register should be always written to, before doing a read from an indirect register. If the indirect register address register is not written to before the read, then multiple reads of the same data will result. Writing to an indirect register increments the indirect register address. This automatically caches the data pointed to by the incremented indirect register address.

Table 4-11 Synchronous Indirect Registers

Indirect Register	Bits	Title
0	⟨7:0⟩	Protocol parameter register
0	⟨15:8⟩	Transmit BPC/receive BPC
1	⟨7:0⟩	Receive error
1	⟨15:8⟩	Residual bit counts
2	⟨7:0⟩	Transmit error
2	⟨11:8⟩	Transmit baud rate generator
3	⟨4:0⟩	Number of syncs
3	⟨15:8⟩	Sync register
4	⟨7:0⟩	Modem receive
4	⟨15:8⟩	Modem transmit
5	⟨15:0⟩	Secondary station address
6	⟨15:0⟩	Primary receive buffer address
7	⟨13:0⟩	Primary receive character count
8	⟨15:0⟩	Secondary receive buffer address
9	⟨13:0⟩	Secondary receive character count
10	⟨15:0⟩	Primary transmit buffer address
11	⟨13:0⟩	Primary transmit character count
12	⟨15:0⟩	Secondary transmit buffer address
13	⟨13:0⟩	Secondary transmit character count
14	⟨7:0⟩	Match character
14	⟨15:8⟩	Unused bits
15	⟨15:0⟩	Unused bits

Only the following indirect registers are cleared by both a Master Reset and an INIT.

- Indirect register [0] bits ⟨7:0⟩ (receive error register)
- Indirect register [2] bits ⟨15:0⟩ (transmit error register and transmit BRG register)

Only indirect register [4] bits ⟨15:0⟩ is cleared by an INIT but is not affected by Master Reset. All other indirect registers are not affected by a Master Reset and are of unpredictable value after an INIT. It is the responsibility of the program to initialize these registers properly.

All of the indirect registers are read/write except for indirect register [4] bits ⟨7:0⟩ (receive modem register). The receive modem register is read-only. Read/modify/write UNIBUS cycles may be performed to all of the indirect registers.

4.5.1 Indirect Register [0]

The indirect register [0] consists of two registers: protocol parameter register and transmit BPC/receive BPC register. The protocol parameter register (indirect register [0] bits ⟨7:0⟩) determines the protocol and the error control. The transmit BPC/receive BPC register determines the bits-per-character for the synchronous transmit and the receive operation.

Figure 4-6 shows the bit format of indirect register [0]. Table 4-12 describes the functions for indirect register [0].

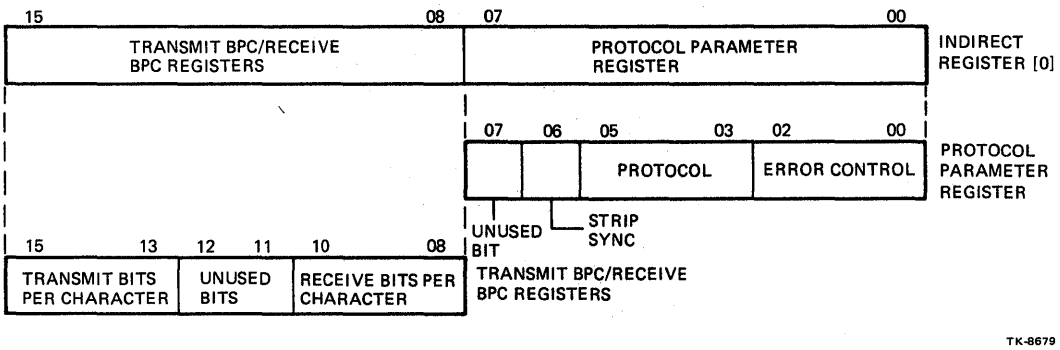

Figure 4-6 Synchronous Indirect Register [0]

Table 4-12 Indirect Register [0] Functions

Bits	Title	Function
⟨2:0⟩	Error Control	Bits ⟨2:0⟩ determine the error control (shown in Table 4-13). Table 4-14 lists valid error control, bits per character, and protocol combinations.
⟨5:3⟩	Protocol	Bits ⟨5:3⟩ determine the protocol to be performed (shown in Table 4-15).
⟨6⟩	Strip Sync	STRIP SYNC is used only for the GEN BYTE protocol. If this bit is set, then any characters contiguous to the sync characters that cause synchronization are automatically stripped off from the serial input data. Other protocols automatically strip sync.
⟨7⟩	Unused Bit	
⟨10:8⟩	Receive Bits Per Character	Bits ⟨10:8⟩ determine the number of bits per character for the synchronous receive operation (shown in Table 4-16).
⟨12:11⟩	Used Bits	
⟨15:13⟩	Transmit Bits Per Character	Bits ⟨15:13⟩ determine the number of bits per character for the synchronous transmit operation (shown in Table 4-17).

Table 4-13 Error Control Codes

Protocol Parameter Register	
Bits ⟨2:0⟩	**Error Control**
000	CRC-CCITT preset to 1s
001	CRC-CCITT preset to 0s
010	LRC/VRC odd
011	CRC-16
100	LRC odd
101	LRC even
110	LRC/VRC even
111	No error control

Table 4-14 Valid Error Control, Bits Per Character, and Protocol Combinations

Protocol	Bits/ Character	Error Control
SDLC	8	CRC-CCITT preset to 1s
SDLC	7	CRC-CCITT preset to 1s
SDLC	6	CRC-CCITT preset to 1s
SDLC	5	CRC-CCITT preset to 1s
HDLC	8	CRC-CCITT preset to 1s
HDLC	7	CRC-CCITT preset to 1s
HDLC	6	CRC-CCITT preset to 1s
HDLC	5	CRC-CCITT preset to 1s
DDCMP	8	CRC-16
GEN BYTE	8	CRC-16
GEN BYTE	8	No error control
GEN BYTE	7	VRC even
GEN BYTE	7	VRC odd
GEN BYTE	7	VRC/LRC even
GEN BYTE	7	VRC/LRC odd
GEN BYTE	7	No error control
GEN BYTE	6	VRC even
GEN BYTE	6	VRC odd
GEN BYTE	6	VRC/LRC even
GEN BYTE	6	VRC/LRC odd
GEN BYTE	6	No error control
GEN BYTE	5	VRC even
GEN BYTE	5	VRC odd
GEN BYTE	5	VRC/LRC even
GEN BYTE	5	VRC/LRC odd
GEN BYTE	5	No error control
SDLC	8	No error control
SDLC	7	No error control

Table 4-14 Valid Error Control, Bits Per Character, and Protocol Combinations (Cont)

Protocol	Bits/ Character	Error Control
SDLC	6	No error control
SDLC	5	No error control
HDLC	8	No error control
HDLC	7	No error control
HDLC	6	No error control
HDLC	5	No error control

Table 4-15 Protocol Selection

Protocol Parameter Register Bits ⟨5:3⟩	Protocol
000	DDCMP
001	SDLC
010	HDLC
011	Spare
100	Spare
101	Spare
110	Spare
111	GEN BYTE

Table 4-16 Receive Bits Per Character Selection

Bits ⟨10:8⟩	Receive Bits Per Character
000	8
001	1
010	2
011	3
100	4
101	5
110	6
111	7

Table 4-17 Transmit Bits Per Character

Bits ⟨15:13⟩	Transmit Bits Per Character
000	8
001	1
010	2
011	3
100	4
101	5
110	6
111	7

4.5.2 Indirect Register [1]

Indirect register [1] consists of two registers: receive error register and residual bit count register. The receive error register contains the errors for the synchronous receive operation. The residual bit count register specifies how many bits of the last character transferred to main memory are part of the message for bit-oriented protocols.

Figure 4-7 shows the bit format for indirect register [1]. Table 4-18 describes the functions for indirect register [1].

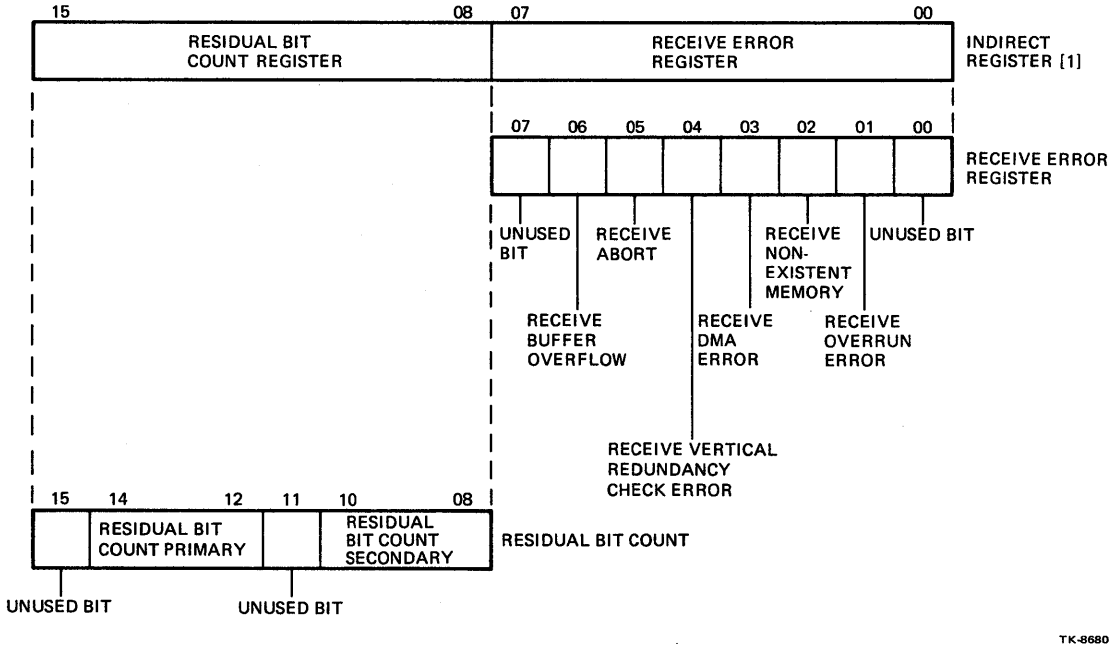

Figure 4-7 Synchronous Indirect Register [1]

Table 4-18 Indirect Register [1] Functions

Bits	Title	Function
⟨0⟩	Unused Bit	
⟨1⟩	Receive Overrun Error	This bit is set if a receive overrun condition is detected. This would occur if the synchronous interface could not process and direct memory access the received characters fast enough (because the synchronous interface was operating at too high a baud rate). The receive overrun bit is cleared by a Master Reset, INIT or by reading receiver error register bits ⟨7:0⟩.
⟨2⟩	Receive DMA Error	This bit is set if the DMF32 UNIBUS controller either did not receive a SSYN at least 32 μs after issuing a MSYN, or the controller could not become bus master for at least 32 μs after having asserted BUS NPR. Setting this bit clears the receiver enable bit. This bit is cleared by a Master Reset or INIT, or by reading receiver error register bits ⟨7:0⟩.
⟨3⟩	Receive Block Check Character Error	Bit ⟨3⟩ is asserted if the received message generates a block check error. This bit is cleared by a Master Reset, INIT, or by reading the receiver error register.
⟨4⟩	Receive Vertical Redundancy Check Error	Bit ⟨4⟩ is used for byte-oriented protocols only. This bit is asserted when the most recent character received has incorrect character parity. This bit is cleared by a Master Reset, INIT, or by reading the receiver error register.
⟨5⟩	Receive Abort	Bit ⟨5⟩ is used only for bit-oriented protocols. The receive abort bit is set if an abort sequence (i.e., seven consecutive one bits) is received while receiver active bit (receives CSR bit ⟨6⟩) is set. This bit is cleared by a Master Reset, INIT, or by reading receiver error register.

Table 4-18 Indirect Register [1] Functions (Cont)

Bits	Title	Function
⟨6⟩	Receive Buffer Overflow	This bit is set when the receive character count register counts to zero and the synchronous interface knows that there are still more bytes of the message to be received. For the DDCMP, SDLC, and HDLC protocols, the synchronous interface knows when the message is finished. For the GEN BYTE protocol, the synchronous interface does not know when the message is finished, except by examining the character count register. The GEN BYTE protocol is a byte-oriented synchronous transfer, in which the synchronous interface does not know what the specific protocol is. The receiver overflow bit is never set in the GEN BYTE mode. This bit is cleared by either a Master Reset, INIT, or by reading the receiver error register bits ⟨7:0⟩.
⟨7⟩	Unused Bit	
⟨10:8⟩	Residual Bit Count Secondary	These bits are used for bit-oriented protocols only. Bit-oriented messages can be any length. The residual bit count secondary bit field specifies how many bits of the last character transferred to main memory are part of the message. These bits should only be examined after the receiver done secondary bit is set. The receiver residual secondary bit (receiver CSR bit ⟨11⟩) is set when the residual bit count secondary bit field does not equal zero; thus implying that the residual bit count secondary bit field should be examined. The residual bits are right-justified within the last byte.
⟨11⟩	Unused Bit	This bit should be ignored by the program.
⟨14:12⟩	Residual Bit Count Primary	These bits are used for bit-oriented protocols only. Bit-oriented messages can be any length. The residual bit count primary bit field specifies how many bits of the last character transferred to main memory are part of the message. These bits should only be examined after the receiver done primary bit is set. The receiver residual primary bit (receiver CSR bit ⟨12⟩) is set when the residual bit count primary bit field does not equal zero; thus implying that the residual bit count primary bit field should be examined. The residual bits are right-justified within the last byte.
⟨15⟩	Unused Bit	This bit should be ignored by the program.

4.5.3 Indirect Register [2]

Indirect register [2] consists of two registers: transmit error register and transmit baud rate generator register. The transmit error register contains the transmit underrun error, transmit DMA memory error, and the transmit message length error. The transmit baud rate generator contains the code that determines the synchronous transmit baud rate when using the on board baud rate generator.

Figure 4-8 shows the bit format for indirect register [2]. Table 4-19 describes the functions for indirect register [2].

4.5.4 Indirect Register [3]

Indirect register [3] contains the sync character used for transmit idle fill for a transmit underrun and receive synchronization. This register also contains the specified number of sync characters to be transmitted prior to a message.

Figure 4-9 shows the bit format for indirect register [3]. Table 4-21 describes the functions of indirect register [3].

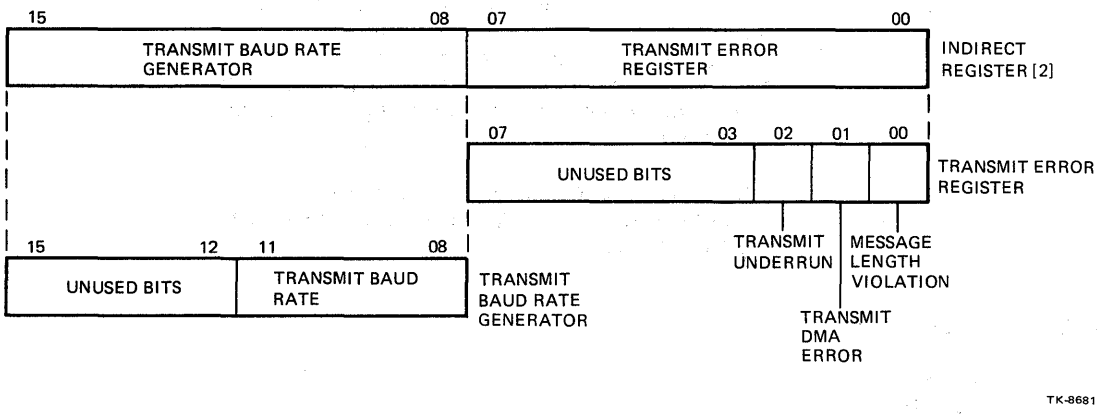

Figure 4-8 Synchronous Indirect Register [2]

Table 4-19 Indirect Register [2] Functions

Bits	Title	Function
⟨0⟩	Message Length Violation	Bit ⟨0⟩ is set by the synchronous interface if the character count indicates a buffer length too small for the message of the specific protocol. This error can be detected before transmission is begun (SDLC frame under four characters). This bit is cleared by a Master Reset or by reading the transmit error register.
⟨1⟩	Transmit DMA Error	This bit is set if the synchronous interface UNIBUS controller either did not receive a SSYN at least 32 μs after issuing a MSYN, or the controller could not become bus master for at least 32 μs after having asserted BUS NPR. This bit is cleared by a Master Reset, INIT, or by the reading of transmit error register bits ⟨7:0⟩.
⟨2⟩	Transmit Underrun Error	This bit is set if a transmit underrun condition is detected. This would occur if the synchronous interface could not process and direct memory access the transmitted characters fast enough (because the synchronous interface was operating at too high a baud rate). The transmit underrun error bit is cleared by a Master Reset, INIT, or by reading the transmit error register bits ⟨7:0⟩.
⟨7:3⟩	Unused Bits	
⟨11:8⟩	Transmit Baud Rate Generator	Bits ⟨11:8⟩ specify the baud rate for the internal baud rate generator. Table 4-20 lists the transmit baud rates.
⟨15:12⟩	Unused Bits	These bits are cleared by a Master Reset or an INIT.

Table 4-20 Transmit Baud Rates

Bits ⟨11:8⟩	Bits Per Second
0000	800.000
0001	1,200.000
0010	1,760.000
0011	2,152.357
0100	2,400.000
0101	4,800.000
0110	9,600.000
0111	19,200.000
1000	28,800.000
1001	32,081.013
1010	38,400.000
1011	57,600.000
1100	76,800.000
1101	115,200.000
1110	153,600.000
1111	316,800.000

CAUTION

Operation at speeds greater than 19,200 bps is not recommended due to bandwidth limitations.

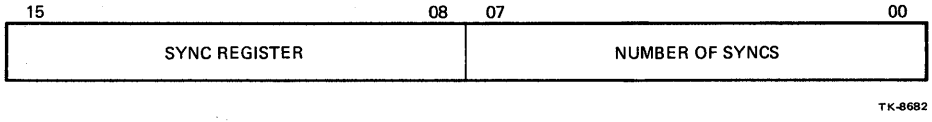

Figure 4-9 Synchronous Indirect Register [3]

Table 4-21 Indirect Register [3] Functions

Bits	Title	Function
⟨7:0⟩	Number of Syncs	Bits ⟨7:0⟩ specifies the number of sync characters specified in sync register (indirect register [3] bits ⟨15:8⟩) to be transmitted prior to a message.
⟨15:8⟩	Sync Register	This register is used only for byte-oriented protocols, and has the following functions: • It contains the sync character transmitted between messages when the IDLE bit is clear. Thus, this register is used as an idle fill. Also, the contents of this register is transmitted before a transmit message is direct-memory accessed. The number of sync characters transmitted should be specified in the number of sync register bits ⟨7:0⟩. • The character in the sync register is used for receive synchronization.

4.5.5 Indirect Register [4]

Indirect register [4] consists of two registers: receive modem register and transmit modem register. The receive modem register contains all the modem signals that originate from the DCE. The transmit modem register contains the modem signals to be transmitted to the DCE.

Figure 4-10 shows the bit format for indirect register [4]. Table 4-22 describes the functions of indirect register [4].

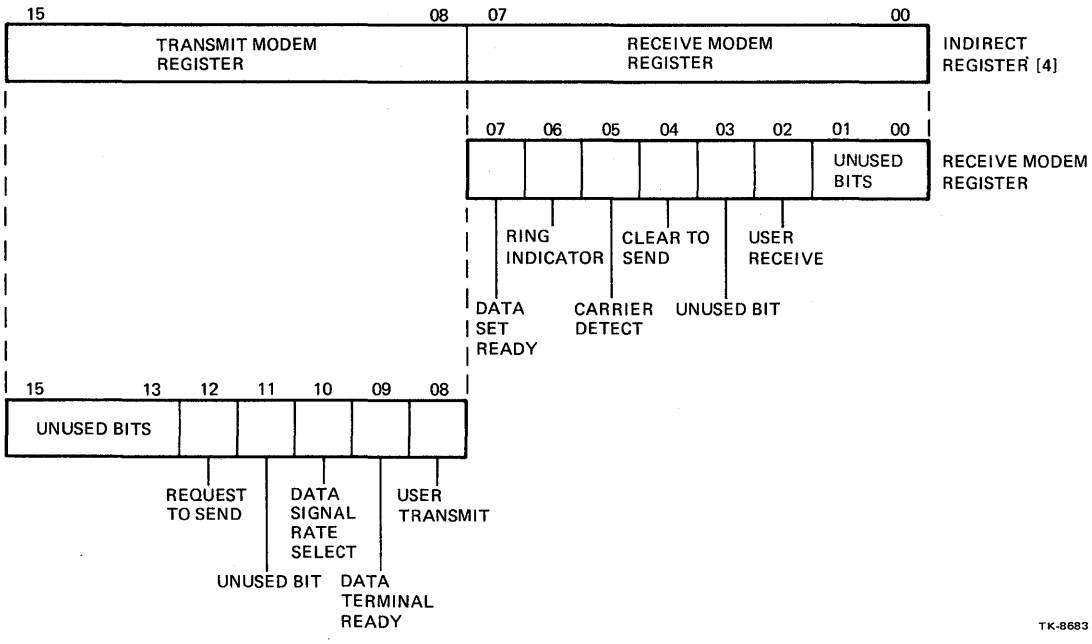

Figure 4-10 Synchronous Indirect Register [4]

Table 4-22 Indirect Register [4] Functions

Bits	Title	Function
⟨1:0⟩	Unused Bits	
⟨2⟩	User Receive	Bit ⟨2⟩ is connected (via a jumper) to pin 25 of the 25-pin Cinch connector on the distribution panel. The user receive bit can be used for whatever purpose the user desires. The ON-to-OFF or OFF-to-ON transition of this signal causes the data set change bit (transmit CSR bit ⟨6⟩) to set.
⟨3⟩	Unused Bit	
⟨4⟩	Clear To Send	Bit ⟨4⟩ reflects the state of the Clear to Send line (RS-232C circuit CB) originating from the modem. Any ON-to-OFF or OFF-to-ON transition of this line asserts the data set change bit (transmit CSR bit ⟨6⟩).
⟨5⟩	Carrier Detect	This bit reflects the state of the Received Line Signal Detector line (RS-232C circuit CF) originating from the modem. Any ON-to-OFF or OFF-to-ON transition of this line asserts the data set change bit (transmit CSR bit ⟨6⟩).
⟨6⟩	Ring Indicator	This bit reflects the state of the Ring Indicator line (RS-232C circuit CE) originating from the modem. Any ON-to-OFF or OFF-to-ON transition of this line asserts the data set change bit (transmit CSR bit ⟨6⟩).
⟨7⟩	Data Set Ready	Bit ⟨7⟩ reflects the state of the Data Set Ready line (RS-232C circuit CC) originating from the modem. Any ON-to-OFF or OFF-to-ON transition of this bit asserts the data set change bit.
⟨8⟩	User Transmit	This line is connected (via a jumper) to pin 18 of the 25-pin Cinch connector on the distribution panel. This pin is an EIA RS-232C unassigned pin, and can be used for whatever purpose the user desires.
⟨9⟩	Data Terminal Ready	Bit ⟨9⟩ controls the Data Terminal Ready line (EIA RS-232C circuit CD) connected to the modem. When bit ⟨9⟩ is set, the Data Terminal Ready line is in the ON state. If this bit is clear, the Data Terminal Ready line is in the OFF state.

Table 4-22 Indirect Register [4] Functions (Cont)

Bits	Title	Function
⟨10⟩	Data Signal Rate Selector	Bit ⟨10⟩ controls the Data Signal Rate Selector line (EIA RS-232C circuit CH) connected to the modem. When this bit is set, the Data Signal Rate Selector line is in the ON state. If this bit is clear, the Data Signal Rate Selector line is in the OFF state.
⟨11⟩	Unused Bit	
⟨12⟩	Request to Send	Bit ⟨12⟩ controls the Request to Send line (EIA RS-232C circuit CA) connected to the modem. When this bit is set, the Request to Send line is in the ON state. If this bit is clear, the Request to Send line is in the OFF state.
⟨15:13⟩	Unused Bits	

4.5.6 Indirect Register [5]

Indirect register [5] bits ⟨15:0⟩ contains either the secondary station address or the tributary station address. For bit-oriented protocols, this register contains the secondary station address. For DDCMP, this register contains the tributary station address. The synchronous interface compares this address with the address of an incoming receive message to determine whether the message is destined for this node. If the station has a one-byte address, then only the low byte is used and the upper byte is ignored.

Figure 4-11 shows the bit format for indirect register [5].

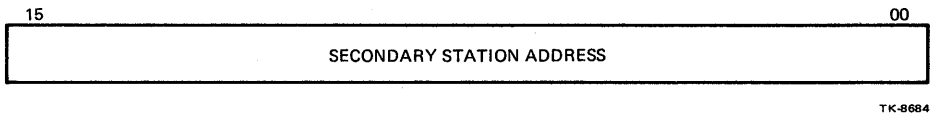

Figure 4-11 Synchronous Indirect Register [5]

4.5.7 Indirect Registers [6] and [7]

Figure 4-12 shows the bit format for both indirect registers [6] and [7].

Indirect register [6] bits ⟨15:0⟩ and indirect register [7] bits ⟨15:14⟩ together contain the 18-bit primary receive buffer address. Indirect register [7] bits ⟨15:14⟩ contains the two most significant address bits. This address points to a receive data buffer in main memory. A received message is transferred into this buffer via nonprocessor request (DMA).

Indirect register [7] bits ⟨13:0⟩ is the primary receive character count register. This register is loaded with the size (in bytes) of the receive data buffer (the buffer pointed to by the primary receive character count buffer address). This character count register is decremented by the synchronous interface each time data is transferred to main memory. The program may read this register to calculate the length of the received message. If the message size is larger than the buffer space allotted to the message, then part of the message is lost. This condition is flagged by the receive overflow bit. Loading this register clears the receiver done primary bit.

4.5.8 Indirect Registers [8] and [9]

Figure 4-13 shows the bit format for both indirect registers [8] and [9].

Indirect register [8] bits ⟨15:0⟩ and indirect register [9] bits ⟨15:14⟩ together contain the 18-bit secondary receive buffer address. Indirect register [9] bits ⟨15:14⟩ contains the most significant address bits. This address points to a receive data buffer in main memory. A received message is transferred into this buffer via nonprocessor request (DMA).

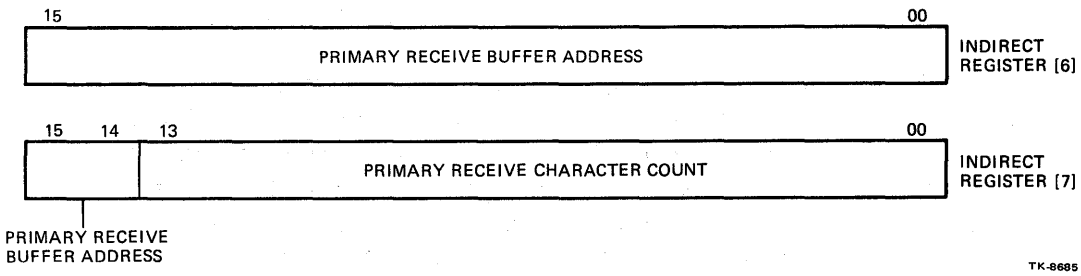

Figure 4-12 Synchronous Indirect Register [6] and [7]

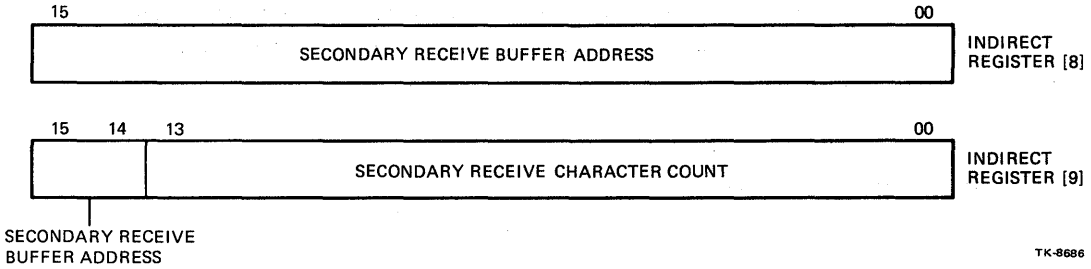

Figure 4-13 Synchronous Indirect Register [8] and [9]

Indirect register [9] bits ⟨13:0⟩ is the secondary receive character count register. This register is loaded with the size (in bytes) of the receive data buffer (the buffer pointed to by the secondary receive character count buffer address). This character count register is decremented by the synchronous interface each time data is transferred to main memory. The program may read this register to calculate the length of the received message. If the message size is larger than the buffer space allotted to the message, then part of the message is lost. This condition is flagged by the receive overflow bit. Loading this register clears the receiver done secondary bit.

4.5.9 Indirect Registers [10] and [11]

Figure 4-14 shows the bit format for both indirect registers [10] and [11].

Indirect register [10] bits ⟨15:0⟩ and indirect register [11] bits ⟨15:14⟩ together contain the 18-bit primary transmit buffer address. Indirect register [11] bits ⟨15:14⟩ contains the two most significant address bits. This address points to a transmit data buffer in main memory. A message to be transmitted is transferred from this buffer to the synchronous interface via nonprocessor request (DMA). The primary transmit character count register (primary transmit character count) contains the size (in bytes) of the message.

Indirect register [11] bits ⟨13:0⟩ is the primary transmit character count register. This register is loaded with the size (in bytes) of the transmit data buffer (the buffer pointed to by the primary transmit character buffer address). This character count register is decremented each time data is transferred from the synchronous interface to main memory. Loading this register clears the transmit done primary bit.

4.5.10 Indirect Registers [12] and [13]

Figure 4-15 shows the bit format for both indirect registers [12] and [13].

Indirect register [12] bits ⟨15:0⟩ and indirect register [13] bits ⟨15:14⟩ together contain the 18-bit secondary transmit buffer address. Indirect register [13] bits ⟨15:14⟩ contains the two most significant address bits. This address points to a transmit data buffer in main memory. A message to be transmitted is transferred from this buffer to the synchronous interface via nonprocessor request (DMA). The secondary transmit character count register (secondary transmit character count) contains the size (in bytes) of the message.

Indirect register [13] bits ⟨13:0⟩ is the secondary transmit character count register. This register is loaded with the size (in bytes) of the transmit data buffer (the buffer pointed to by the secondary transmit character buffer address). This character count register is decremented each time data is transferred from the synchronous interface to main memory. Loading this register clears the transmit done secondary bit.

4.5.11 Indirect Register [14]

Figure 4-16 shows the bit format for indirect register [14].

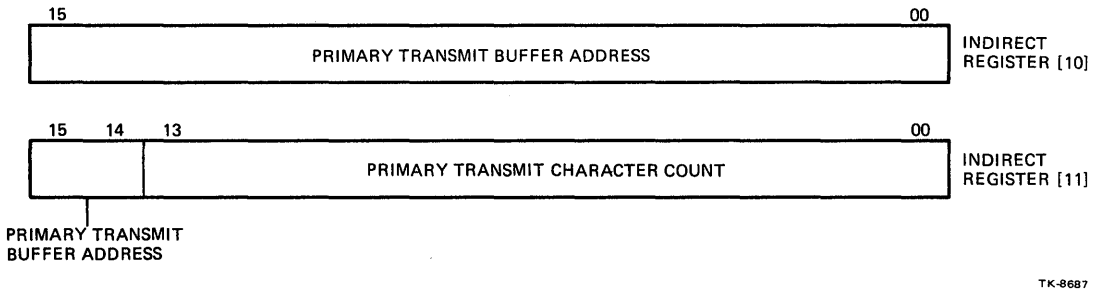

Figure 4-14 Synchronous Indirect Registers [10] and [11]

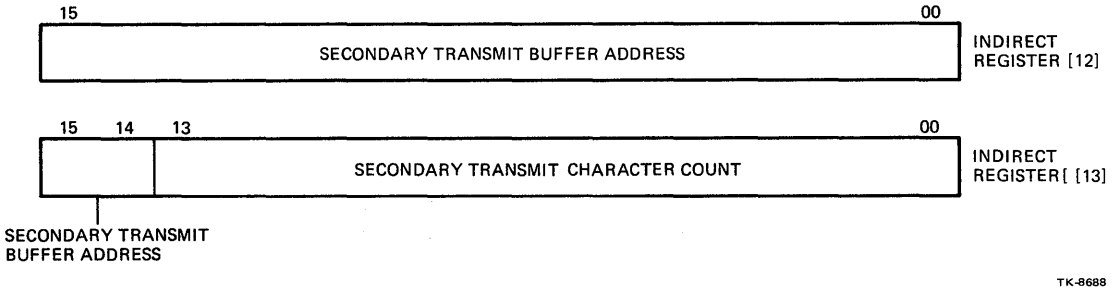

Figure 4-15 Synchronous Indirect Registers [12] and [13]

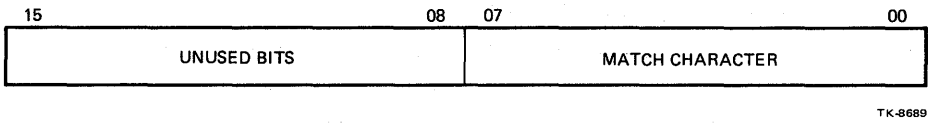

Figure 4-16 Synchronous Indirect Register [14]

Indirect register [14] bits ⟨7:0⟩ contains the match character. This termination character is used only when operating in GEN BYTE mode. If receive match bit (receive CSR bit ⟨3⟩) is set, receiving a character that matches the character stored in this register causes an interrupt.

Indirect register [14] bits ⟨15:8⟩ are not used.

4.5.12 Indirect Register [15]

This indirect register is not used.

4.6 SYNCHRONOUS INTERFACE PROTOCOLS

The synchronous interface supports the following bit-oriented protocols:

- SDLC-Synchronous Data Link Control (IBM)
- HDLC-High Level Data Link Control (ISO)

The synchronous interface supports bit-oriented protocols by performing the following:

- Bit stuffing and bit removal
- Flag character (01111110) recognition for receive message framing
- Flag character generation for transmit message framing
- Abort character (01111111) recognition in a receive message
- Abort character (11111111) generation in a transmit message
- Secondary station address recognition in a receive message (maximum address length dependent upon protocol) when operating as a secondary station
- CRC check on a receive message
- CRC generation on a transmit message

4.6.1 Bit-Oriented Protocol – Transmit Operation

A message is preceded with an opening flag and is terminated with a closing flag (01111110). Between transmitted messages, the synchronous interface either sends ones or flag characters on the synchronous line, depending on whether the idle bit (transmit CSR bit ⟨3⟩) is a zero or a one.

4.6.1.1 Bit Stuffing – Bit stuffing prevents a flag character within the message from being transmitted as a flag sequence. The synchronous interface performs bit stuffing by inserting a 0 after any sequence of five ones within the message. When CRC is specified, the CRC calculations include all bits within the message, except for the stuffed zeros. The opening and closing flags are not included in the CRC calculations.

4.6.1.2 Bit-Oriented Protocol Transmit Errors – A DMA memory error (indirect register [2] bit ⟨1⟩) or a transmit underrun error (indirect register [2] bit ⟨2⟩) causes the transmission to abort. When the transmission is aborted, the synchronous interface automatically transmits an abort character (11111111).

The synchronous interface detects a transmit length violation error prior to message transmission. This error indicates that the message length is less than four bytes.

The transmit error bit (transmit CSR bit ⟨14⟩) is an inclusive OR of all error bits in the transmit error register (indirect register [2] bits ⟨7:0⟩). Asserting the transmit error bit causes the transmit enable bit (transmit CSR bit ⟨0⟩) to clear. With the transmit enable bit cleared, subsequent messages are not transmitted until the program acknowledges the error condition.

The message in the transmit buffer should contain the complete SDLC or HDLC frame, starting with the address field and terminating with the final data character. The synchronous interface inserts the CRC characters prior to the closing flag. If CRC is not specifed, the message should contain the CRC check as the final 16 bits.

The transmitter operates the same for both SDLC and HDLC. However, the receiver operates differently due to different interpretation of the address field bits.

4.6.2 Bit-Oriented Protocol – Receive Operation

The beginning of a frame is recognized by receiving a nonflag character after a flag character. When operating as a secondary station, the synchronous interface compares the secondary station address field in the received frame with the programmed secondary station address. If the two secondary station address fields are identical, the synchronous interface initiates the NPR transfer to the receive buffer in main memory. If the addresses are not identical, the message is ignored and the synchronous interface searches for the next message. Regardless of the programmed secondary station address, the "all parties" address (11111111) is always recognized as a valid address.

4.6.2.1 Bit-Oriented Protocol Secondary Station Address – SDLC specifies a secondary station address of one byte. The program loads the secondary station address into the low byte of the secondary station address register (indirect register [5] bits ⟨7:0⟩).

HDLC specifies a secondary station address of either one or two bytes. If the least-significant bit of the first byte is zero, the second byte is the address extension. The first secondary station address byte could be loaded by the program into the secondary station address bits ⟨7:0⟩ (indirect register [5] bits ⟨7:0⟩). The optional second byte should be loaded into the secondary station address bits ⟨15:8⟩ (indirect register [5] bits ⟨15:8⟩).

4.6.2.2 ADCCP Protocol – The Advanced Data Communication Control Procedure (ADCCP) protocol is implemented by running the synchronous interface in HDLC or SDLC mode. ADCCP specifies any number of bytes for the secondary station address. If the least-significant bit of the first byte is zero, then the second byte is also part of the address. If the least-significant bit of the second byte is also zero, then the third byte is part of the address. The final byte of the address has a 1 in the least-significant bit position of the address.

In HDLC mode, the synchronous interface only compares the first two bytes of a multi-byte address. If the two addresses are identical, the synchronous interface initiates an NPR transfer of the message from the buffer to the main memory. Thus, to receive an ADCCP message in HDLC mode, the program must verify that any remaining address bytes of the transferred message are destined for the respective node.

4.6.2.3 Bit-Oriented Protocol CRC – All bits in the received message (a frame) are included in the CRC, except for the stuffed bits. The synchronous interface removes the stuffed bits prior to the CRC calculation. The stuffed bits are always removed, even if CRC is not specified.

The received CRC is compared to the CRC generated by the synchronous interface. If the two CRCs are not identical, the receive BCC error bit (indirect register [1] bit ⟨3⟩) is set. The received CRC is not transferred to the buffer in main memory if CRC checking is specified.

4.6.2.4 Bit-Oriented Protocol Receive Errors – If receive overrun error (indirect register [1] bit ⟨1⟩), receive DMA error (indirect register [1] bit ⟨2⟩), receive buffer overflow error (indirect error [1] bit ⟨6⟩), or receive abort error (indirect register [1] bit ⟨5⟩) is set when a message is received, the synchronous interface clears the receive enable bit (receive CSR bit ⟨0⟩). Clearing the receive enable bit disables the receiver, thus inhibiting any further message reception.

4.6.3 DDCMP – Receive Operation

The synchronous interface supports DDCMP by:

- Checking CRC on a receive message
- Generating CRC on a transmit message
- Recognizing a tributary address
- Checking quick sync bit for subsequent resynchronization
- Checking byte count to determine message length

The synchronous interface can be operated as a control station (primary/secondary station bit is clear) or a tributary station (primary/secondary station bit is set). When operating as a tributary station, the program should load both the secondary station address (indirect register [5] bit ⟨7:0⟩) with the tributary address. The synchronous interface uses the secondary station address to check the address of a receive message. If operating as a control station, the synchronous interface does not check the receive address field.

4.6.3.1 DDCMP Received Message – A receive message is transferred with header and possible data to the receive buffer in main memory. The CRC checks, header CRC, and data CRC are removed from the transferred message. All sync characters that cause byte synchronization are stripped. Trailing pad characters are removed.

4.6.3.2 DDCMP Data Streams – For data messages and maintenance messages, the synchronous interface reads the character count information in the header, and thus knows where the data stream ends. For data messages, the character count begins after the first start of heading (SOH) character; for maintenance messages, the character count begins after the first data link escape (DLE) character. The receive DMA character count register must contain a length at least as long as the header and the data. Control messages have no data field and are of a fixed length of eight bytes. The receive DMA character count register must be loaded with a value of at least six. The two CRC bytes are not direct memory accessed.

4.6.3.3 DDCMP Receive Synchronization – The synchronous interface checks the quick sync bit in the receive message. When the quick sync bit is set, the synchronous interface resynchronizes at the end of the message. If the quick sync bit is not set, the synchronous interface checks the byte immediately following the end of the message. If this byte is an SOH, enquing (ENQ), or DLE, the synchronous interface recognizes this byte as the beginning of an abutting message. The receiver resynchronizes if the byte is not an SOH, ENQ, or DLE. The receiver always resynchronizes after receiving a message with a CRC error.

4.6.4 DDCMP – Transmit Operation

The transmit buffer should not include any CRCs, either header or data. The synchronous interface generates the CRCs and inserts them at the correct points (for both header and data) in the transmit message stream. The synchronous interface inserts at least two pad characters (eight consecutive 1s) at the end of each message.

For data messages and maintenance messages, the synchronous interface reads the character count information in the header, and thus knows where the data stream ends. For data messages, the character count begins after the first SOH character; for maintenance messages, the character count begins after the first DLE character. The transmit DMA character count register must contain a length at least as long as the header and the data, otherwise, the transmit message length error bit becomes asserted. Control messages have no data field, and are of a fixed length of eight bytes. The transmit DMA character count register must be loaded with a value of at least six. The synchronous interface generates the two CRC bytes.

4.6.4.1 DDCMP Transmit Errors – Asserting either the transmit DMA memory error bit (indirect register [2] bits ⟨1⟩) or transmit underrun error bit (indirect register [2] bit ⟨2⟩) terminates the transmission. Termination causes the line to either idle sync characters or to mark, depending on the state of the idle bit (transmit CSR bit ⟨3⟩).

Setting the transmit error bit (transmit CSR bit ⟨14⟩), which is the inclusive OR of all the transmit error bits, clears the transmit enable bit (transmit CSR bit ⟨0⟩). Clearing the transmit enable bit terminates the message transmission until the program acknowledges the error condition.

4.6.5 General Byte-Oriented (GEN BYTE) Protocol

The GEN BYTE protocol transfers character-oriented transmit or receive data. Any byte-oriented protocol may be implemented by having software perform the protocol-specific functions. An optional programmable receive match character specifies that, when a match character is received, the synchronous interface should generate a receive interrupt. The receive match character bit (receive CSR bit ⟨3⟩) determines if the optional programmable match character is to be used. The programmable match character should be loaded into the match character register bits ⟨7:0⟩. Also, block check or parity generation and detection may be performed.

4.6.5.1 GEN BYTE Protocol – The character used for receive synchronization is stored in sync register bits ⟨7:0⟩. Receiving two successive sync characters signals synchronization. If the strip sync bit is set, all sync characters contiguous to the initial two sync characters that caused synchronization are not transferred to the receive buffer in main memory. This buffer is loaded with receive data until the character count register counts to zero.

4.6.5.2 GEN BYTE CRC – If CRC is specified, the synchronous interface checks the receive CRC and indicates an error condition by setting receive BCC error bit (indirect register [1] bit ⟨3⟩). If vertical redundancy check (VRC) or VRC and longitudinal redundancy check (VRC/LRC) are specified, the first detection of a VRC error sets the receive VRC error bit (indirect register [1] bit ⟨4⟩). If VRC/LRC is specified and only an LRC error is detected, the receive BCC error bit (indirect register [1] bit ⟨3⟩) is set.

4.6.5.3 Transmit Operation – Characters are direct memory accessed from the buffer in main memory until the character count register counts to zero. If CRC is specified, the synchronous interface generates the block check and appends the block check to the end of the message. If the VRC is specified, the synchronous interface attaches a parity bit to each character. If the VRC/LRC are specified, the synchronous interface attaches a parity bit to each character, and appends the LRC to the end of the message.

4.7 ASYNCHRONOUS INTERFACE

The asynchronous multiplexer contains eight transmit and eight receive lines. Each of the asynchronous lines may be programmed to operate at one of 16 baud rates, ranging from 50 bps to l9,200 bps. Although the lines can be programmed to run at 19,200 bps, this should be done with caution, for the clock error at 19,200 bps is 3.125%. The actual frequency is 19,800 bps. Two of the eight lines have both split speed capability and modem control. Received characters, with their respective line numbers and status information are stored in a 48-word silo. Interrupts may be generated if more than 16 characters are in the silo or after the silo has been non-empty for a time exceeding the programmable timeout period since the last silo read.

In SILO mode, each transmit line has its own 32-character silo for storing data to be transmitted. Characters may be loaded into a silo one or two at a time. In DMA mode, characters transmit from main memory via DMA, as specified by the transmit line's buffer address register and character count register. Once DMA is initiated, the transmit silo is automatically filled with characters and transmission may begin if the transmitter is enabled. After the silo fills, DMA stops. When the silo count drops below two characters, DMA is restarted and the silo is refilled. This cycle continues until the DMA byte count is equal to zero. When the DMA byte count is zero and the last character has been removed from the transmit silo, an interrupt will be requested if enabled.

The auto XON/XOFF mode is selectable on a per line basis and may be used in DMA or silo transmit mode. When auto XON/XOFF is selected, the DMF32 automatically disables the transmitter for a line receiving an XOFF. The XOFF is still entered in the receive silo, so the operating system may disable its timeout function. Receiving an XON reenables the transmitter for that line. The XON is also put into the receive silo to inform the operating system that transmissions have restarted. This mode allows relatively long silo timeouts as the time-critical XOFF instantly disables the transmitter.

4.7.1 Asynchronous Device Registers

The asynchronous interface uses four device registers and 32 indirect registers. The device registers are as follows:

- Control status register
- Line parameter register
- Receiver buffer
- Receive silo parameter register

4.7.1.1 Control Status Register – The control status register performs the following:

- Points to one of 32 indirect registers.
- Initiates Master Reset.
- Enables the receive interrupt.
- Indicates when data becomes available in the receive silo.
- Contains the transmit line number.
- Indicates DMA error.
- Enables transmit interrupt.
- Indicates transmit ready.

4.7.1.2 Line Parameter Register – The line parameter register indicates the following:

- The line selected
- The character length
- Parity enabled
- Even/odd parity
- The stop code
- Baud rates

4.7.1.3 Receive Buffer Register – The receive buffer register performs the following:

- Stores the receive character with line number and error status.
- Indicates when there has been a data set change and on which line.
- Indicates parity, framing, and overrun errors.
- Indicates when data is valid in the receive buffer.

4.7.1.4 Receive Silo Parameter Register – The receive silo parameter register contains the receive silo alarm timeout.

4.7.2 Asynchronous Device Operation

After an INIT or a Master Reset, the transmit and receive buffers are empty, and all lines are disabled. The program must load the line parameter register bits ⟨15:0⟩ with the desired parameters for specific lines before enabling these lines, even if all parameters are zero. Line select (line parameter register bits ⟨2:0⟩) should contain the line number whose parameters are to be loaded. The program should also set the appropriate interrupt enable bits in the control status register. The program is now ready to enable the desired transmit and receive lines. The modem control signals emanating from the asynchronous multiplexer can be set or cleared at any time. A Master Reset or INIT clears the bits in the CSR representing the transmit modem bits. However, the actual transmit modem signals are cleared only after an INIT, and are not affected by a Master Reset.

4.7.2.1 Asynchronous Transmit Operation – A line must be enabled to transmit data. Setting the appropriate bits in the line parameter register enables a transmit line. A disabled line is held marking unless the line is programmed for auto echo or remote loopback.

When the transmit ready bit is set, the transmitter is available for loading. The transmit ready bit is set under the following conditions:

- In silo mode, when a transmit silo becomes empty due to a character leaving the silo.

- In DMA mode, when a DMA transfer for a particular line has completed, and the last character has been removed from the silo.

The transmit interrupt enable bit enables and disables the transmit ready bit to generate interrupts.

If the transmit interrupt enable bit is active when the transmit ready bit becomes set, an interrupt to the transmit vector is posted. The program should read the asynchronous CSR to determine the cause of the interrupt. If the transmit ready bit is set, the transmit line number (asynchronous CSR bits ⟨10:8⟩) contains the line number of the empty silo. If transmission stops due to an aborted DMA transfer, the transmit DMA error bit is set. Reading the asynchronous CSR clears the transmit ready bit. The transmit ready bit must be cleared before the asynchronous interface can reset it for another line.

To minimize interrupt overhead, the program should try to keep the silos filled. If the program intends to fill the silo, it may examine the transmit silo count register for the particular line to determine how many characters have been transmitted from the silo while being filled.

The silo count indicates how many full positions there are in the silo. Thus a silo count of zero indicates an empty silo, while a silo count of 32 indicates a full silo. The transmit silo count registers may be examined at any time. A transmit silo of a particular line may be loaded or flushed regardless of whether the respective transmit line is enabled.

If a line is disabled while its silo is being emptied, transmission stops after the current character has been transmitted. The silo contents will remain valid. Transmission from the silo resumes upon enabling the line.

4.7.2.2 Asynchronous Receiver Operation – A receive line is enabled by setting the appropriate bit in the line parameter register. A line must be enabled to receive data. All lines share a 48-character receive silo. There is no DMA mode for the receiver.

The receive silo is accessed via the receive buffer. Every time the receive buffer is read, data words in the silo are shifted down one position. Successive read cycles access successive silo entries. The receive silo contains receive characters and associated status information, and also data set change information.

4.8 ASYNCHRONOUS DEVICE REGISTERS

The asynchronous interface uses four device registers and 32 indirect registers. The device registers are as follows:

- Control status register
- Line parameter register
- Receiver buffer register
- Receive silo parameter register

4.8.1 Control Status Register

Asynchronous Control Status Register has an address of base +C. Read/modify/write UNIBUS cycles are not allowed. This register can be accessed by word only.

Figure 4-17 shows the bit format for the asynchronous control status register. Table 4-23 describes the functions for the asynchronous control status register.

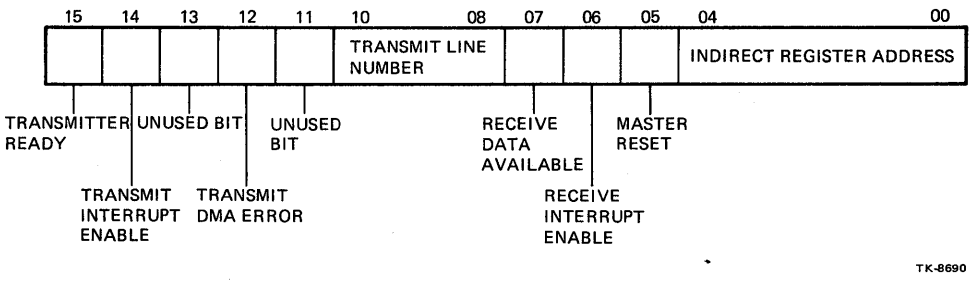

Figure 4-17 Asynchronous CSR

Table 4-23 Asynchronous Control Status Register Functions

Bits	Title	Function
⟨4:0⟩	Indirect Address Register	These read/write bits point to one of thirty-two indirect registers. A Master Reset or INIT clears bits⟨4:0⟩.
⟨5⟩	Master Reset	When the program sets this read/write bit, a Master Reset is initiated. This bit remains set while the reset is in progress, and clears automatically after the reset has completed. The program should not access the asynchronous device registers, except for the asynchronous control status register, during the reset. The program can write a one to the Master Reset bit during a reset, but the DMF32 will ignore it. A Master Reset initializes various CSR bits as specified in the bit descriptions.
⟨6⟩	Receive Interrupt Vector	When set, this bit allows interrupt requests to be made to the receive vector when: • Receiver data available bit has been set for longer that the timeout period. • More than 16 characters have entered the receive silo. A Master Reset or INIT clears this read/write bit.
⟨7⟩	Receive Data Available	The DMF32 sets this bit when data becomes available in the receive silo. The DMF32 automatically clears this bit when the receive silo becomes empty. This bit is read-only, and is cleared by a Master Reset or INIT.

Table 4-23 Asynchronous Control Status Register Functions (Cont)

Bits	Title	Function
⟨10:8⟩	Transmit Line Number	DMA Mode: If the transmit ready bit (asynchronous CSR bit ⟨15⟩) is set, bits ⟨10:8⟩ contain the line number of the transmit DMA transfer that has completed (successfully or unsuccessfully). Silo Mode: If the transmit ready bit (asynchronous CSR bit ⟨15⟩) is set, bits ⟨10:8⟩ contain the line number of the silo that has emptied. These read-only bits are cleared by either a Master Reset, INIT, or reading the asynchronous control status register.
⟨11⟩	Unused	
⟨12⟩	Transmit DMA Error	This bit is used only when the respective line is in DMA mode. This bit is set for the indicated line if the DMF32 UNIBUS controller either did not receive a SSYN at least 32 μs after issuing a MSYN, or the controller could not become bus master for at least 32 μs after having asserted BUS NPR. Bits ⟨10:8⟩ of the asynchronous control status register point to the line in error. This read-only bit is cleared by a Master Reset, INIT, or by reading this register.
⟨13⟩	Unused Bit	
⟨14⟩	Transmit Interrupt Enable	When set, this bit allows an interrupt request to be made to the transmit vector when the transmit ready bit (asynchronous CSR bit ⟨15⟩) becomes set. A Master Reset or INIT clears this read/write bit.
⟨15⟩	Transmitter Ready	Silo Mode: The DMF32 sets this bit when an enabled line (pointed to by bits ⟨10:8⟩) has loaded the last character from the silo into the respective UART's holding register. DMA Mode: The DMF32 sets this bit when an enabled line (pointed to by bits ⟨10:8⟩) has terminated a DMA transfer either successfully or unsuccessfully. A successful DMA termination means that all the data has been transferred from main memory to the DMF32 and that the last character in the silo has been loaded into the respective UART's holding register. An unsuccessful DMA transfer sets the transmit DMA memory error bit (asynchronous CSR bit ⟨12⟩). This read-only bit is cleared when the program reads the asynchronous CSR, or when a Master Reset or INIT is performed.

4.8.2 Line Parameter Register

The line parameter register has an address of base +E. Read/modify/write UNIBUS cycles are allowed. Access is by word only.

A Master Reset or INIT causes the bits in the line parameter register to clear to zero. The parameters for the line are only updated into the UARTs after this register has been written to. Therefore, the line parameter register should always be loaded with the parameters for the particular line before the line is enabled (even if the parameters are all zero).

This location, contains the line parameter for the line selected by indirect address register bits ⟨2:0⟩.

Figure 4-18 shows the bit format for the line parameter register. Table 4-24 describes the functions for the line parameter register.

4.8.3 Receiver Buffer Register

The receiver buffer has an address of base +10. This register is read-only.

The program accesses the receive silo through the receiver buffer. Every time this register is read, data words in the silo shift down one position. Successive read cycles access successive silo entries. This receive silo contains receive characters and associated status information, as well as data set change information.

Either a Master Reset or INIT can flush this silo.

Figure 4-19 shows the bit format for the receiver buffer register. Table 4-27 describes the functions for the receive buffer register.

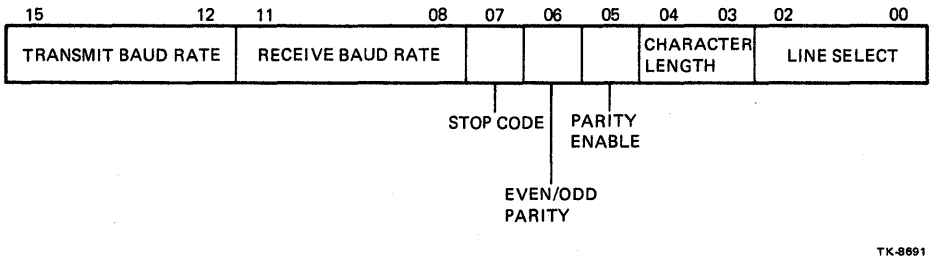

Figure 4-18 Line Parameter Register

Table 4-24 Line Parameter Register Functions

Bits	Title	Function
⟨2:0⟩	Line Select	Bits ⟨2:0⟩ contain the binary number of the line to be loaded with parameters.
⟨4:3⟩	Character Length	These two bits specify the character length (not counting the start bits, stop bits, and the parity bit, if enabled) for the selected line. Table 4-25 shows the bit codes for the characters.
⟨5⟩	Parity Enable	When set, bit ⟨5⟩ causes a parity bit to be generated on transmission. The parity bit is checked and stripped on reception for the selected line.
⟨6⟩	Parity (even odd)	When the parity enable bit is set, or bit ⟨6⟩ specifies whether even or odd parity is generated and checked for the selected line. Parity is indicated as follows: • Bit ⟨6⟩ is clear, odd character parity • Bit ⟨6⟩ is set, even character parity
⟨7⟩	Stop Code	This bit specifies the number of stop bits for the selected line, as follows: • Bit ⟨7⟩ is clear, one stop bit • Bit ⟨7⟩ is set, two stop bits
⟨11:8⟩	Receiver Baud Rate	Split baud rate capability is supported for lines zero and one. If line zero or line one is selected, the line parameter register specifies the selected baud rate of the receiver, while line parameter register bits ⟨15:12⟩ specify the selected transmitter baud rate. However, if any of lines two through seven are selected, then bits ⟨15:12⟩ specify both the receive and transmit baud rates for the selected line. Bits ⟨11:8⟩ are ignored when any of the lines two through seven are selected. Table 4-26 lists the receiver baud rates.
⟨15:12⟩	Transmit Baud Rate	Bits ⟨15:12⟩ specify one of 15 transmit baud rates. Table 4-26 lists the bit codes for the transmit baud rates.

Table 4-25 Character Length Bit Codes

Bit Code	Bits Per Character
00	5
01	6
10	7
11	8

Table 4-26 Receiver and Transmit Baud Rates

Bit Code	Desired Baud Rate	Actual Baud Rate	Deviation (Per Cent)
0000	50	50	0.0%
0001	75	75	0.0%
0010	110	110	0.0%
0011	134.50	134.52	0.0166%
0100	150	150	0.0%
0101	300	300	0.0%
0110	600	600	0.0%
0111	1200	1200	0.0%
1000	1800	1800	0.0%
1001	2000	2005.06	0.253%
1010	2400	2400	0.0%
1011	3600	3600	0.0%
1100	4800	4800	0.0%
1101	7200	7200	0.0%
1110	9600	9600	0.0%
1111	19200	19800	3.125%

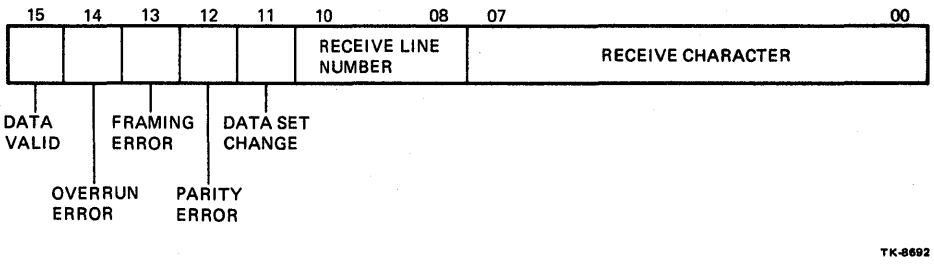

Figure 4-19 Receive Buffer

Table 4-27 Receiver Buffer Register Functions

Bits	Title	Function
⟨7:0⟩	Receive Character	If data set change bit (receiver buffer bit ⟨11⟩) is clear, then the receiver buffer bits ⟨7:0⟩ contain the received character. Bits are received least-significant bit (LSB) first. If parity is enabled, the parity bit is stripped off. Characters less than eight bits long are right-justified with the high order bits set to zero. If data set change bit (receiver buffer bit ⟨11⟩) is set, then the receiver buffer bits ⟨7:0⟩ will be zero; the program should read the receive modem signals to determine which signals changed.
⟨10:8⟩	Receive Line Number	These three bits contain the binary number of the line on which a character was received or a data set change was detected.
⟨11⟩	Data Set Change	When this bit is set, the receiver buffer bits ⟨7:0⟩ are zero, and the receiver line number (receiver buffer bits ⟨10:8⟩) contains the line number whose modem signals changed state.
⟨12⟩	Parity Error	This bit is used only if the data set change bit is clear. Bit ⟨12⟩ is set if parity is enabled for the line on which the character is received, and the character is received with incorrect parity.
⟨13⟩	Framing Error	This bit is used only if data set change bit (receiver buffer bit ⟨11⟩) is clear. This bit is set if the line on which the character was received was in the spacing (zero) state at the time the first stop bit was sampled.
⟨14⟩	Overrun Error	This bit is used only if the data set change bit is clear. Bit ⟨14⟩ is set if one or more previous characters were lost on the line on which the character was received due to a full silo. The received character is valid.
⟨15⟩	Data Valid	When bit ⟨15⟩ is set, the remaining bits in the receiver buffer are valid. This bit is set when data is loaded into the receiver buffer, and remains set as long as there is data in the buffer. This bit is cleared by Master Reset, INIT, or when the receiver buffer becomes empty.

4.8.4 Receive Silo Parameter Register

The receive silo parameter register has an address of base +10. This register is write-only and is accessed by a word. The receive silo parameter register contains the receive silo alarm timeout.

Figure 4-20 shows the bit format for the receive silo parameter register. Table 4-28 describes the functions of the receive silo parameter register.

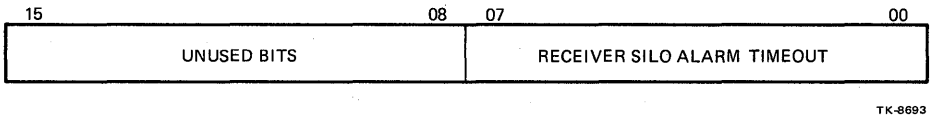

Figure 4-20 Receive Silo Parameter Register

Table 4-28 Receive Silo Parameter Register Functions

Bits	Title	Function
⟨7:0⟩	Receiver Silo Alarm Timeout	These eight bits specify the silo alarm timeout period. An interrupt is generated if data is in the silo for a time equal to or larger than the timeout period. Every time the receive silo is read, a Master Reset or INIT occurs, the internal timer is initialized to zeros. The timeout period can range from approximately 0 to 300 μs. 00000000 = infinite 00000001 = no timeout to 11111111 = maximum timeout This interval timer is based on microcode loops and thus is not very accurate. After a Master Reset or an INIT, the timeout value is set to one.

4.9 ASYNCHRONOUS INDIRECT REGISTERS

The indirect registers have an address of base +12. A 5-bit address (asynchronous control status register bits ⟨4:0⟩) addresses the indirect registers. The low three bits of the address indicate the line number being referenced. The upper two bits select which indirect register of that line is being accessed.

4.9.1 Indirect Registers [0] Through [7]

Each indirect register [0] through [7] consists of a 16-bit write-only register: transmit character line [0] through [7]. Each indirect register [0] through [7] also consists of two read-only registers: transmit silo count register and receive modem register. The transmit character register is used only in silo mode to load one or two characters into the 32-character transmit silo for the respective line. The transmit silo count register is used only in silo mode to contain the number of entries in the 32-character silo for the respective line. The receive modem register contains all modem signals received from the DCE. Since lines 2 through 7 have no modem control signals, receive modem registers 2 through 7 are always read as all zeros.

Figure 4-21 shows the bit format for indirect registers [0] through [7]. Table 4-29 describes the functions of indirect registers [0] through [7].

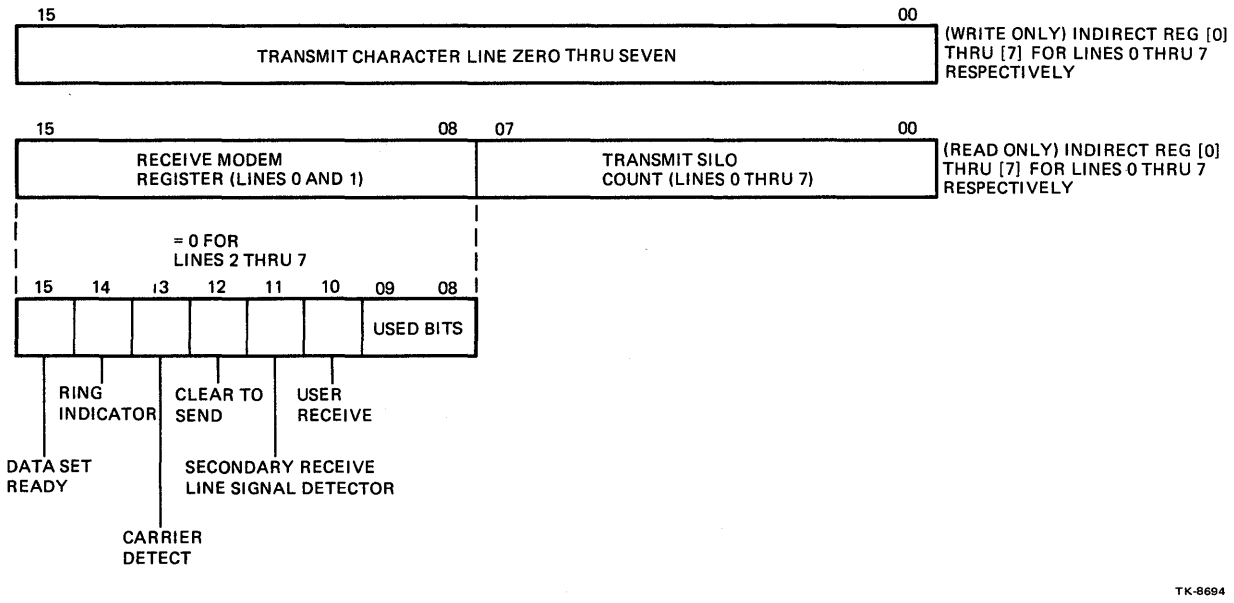

Figure 4-21 Asynchronous Indirect Registers [0] Through [7]

Table 4-29 Indirect Registers [0] Through [7] Functions

Bits	Title	Function
⟨15:0⟩	Transmit Character	This write-only register should be written only in SILO mode. Writing to this register in DMA mode has unpredictable results. Writing to this register, one or two characters are entered into the 32 character transmit silo for the selected line. When the write to this register is a WORD (UNIBUS DATO), two characters are loaded into the silo, the low-order character first. If the write to this register is a BYTE (UNIBUS DATOB), only the low-order character is loaded into the silo; the high-order character is ignored. If the silo is full, a write to this register has no effect on the silo. *WARNING* *The program must wait eight μs after writing to this register before accessing this register again or accessing any other register on the DMF32. If this time period is not respected, a SSYN timeout may occur on the subsequent DMF32 register access.*
⟨7:0⟩	Transmit Silo Count	This read-only register is used only in silo mode. The transmit silo count register contains the number of entries in the 32 character transmit silo for the specific line. A Master Reset or INIT clears this register.
⟨15:8⟩	Receive Modem Status	The receive modem status register (indirect registers [0] through [7] bits ⟨15:8⟩) is cleared during a Master Reset or INIT, but is updated if the following conditions are met: • Data set change flag clear. • Data set change flag is set and there is room in the receive silo for a data set change entry. After a Master Reset, the data set change flag is cleared. If the receive silo is full, the data set change is enabled; the data set change is flagged when the silo is no longer full. Thus, data set changes are not lost when the receive silo is full. When read, bits ⟨15:8⟩ of this read-only register contain the receive modem status for the selected line. This register is valid only for lines 0 and 1. Lines 2 through 7 return all zeroes in these bits. All modem signals represented in this register emanate from the DCE.
⟨9:8⟩	Unused Bits	

Table 4-29 Indirect Registers [0] Through [7] Functions (Cont)

Bits	Title	Function
⟨10⟩	User Receive	Bit ⟨10⟩ is connected (via a jumper) to pin 25 of the 25-pin Cinch connector on the distribution panel. The user receive bit can be used for whatever purpose the user desires.
⟨11⟩	Secondary Receive Line Signal Detector	This bit reflects the state of the secondary received line signal detector (RS-232-C circuit SCF) received from the modem.
⟨12⟩	Clear To Send	Bit ⟨12⟩ reflects the state of the Clear to Send line (RS-232-C circuit CB) received from the modem.
⟨13⟩	Carrier Detect	Bit ⟨13⟩ reflects the state of the Received Line Signal Detector line (RS-232-C circuit CF) received from the modem. If jumpered (on the distribution panel), this bit can represent the Secondary Receive Line Signal Detector.
⟨14⟩	Ring Indicator	Bit ⟨14⟩ reflects the state of the Ring Indicator line (RS-232-C circuit CE) which is received from the modem.
⟨15⟩	Data Set Ready	This bit reflects the state of the Data Set Ready line (RS-232-C circuit CC) which is received from the modem.

4.9.2 Indirect Registers [8] Through [15]

Indirect registers [8] through [15] have an address of base +12. Read/modify/write UNIBUS cycles are allowed and all of the bits within these registers may be read or written. These registers are accessed by word only.

Each indirect register [8] through [15] consists of two registers: a line control register and a transmit modem register. Each line control register controls various functions for each respective line (indirect register [8] controls line 0, indirect register [9] controls line 1). Figure 4-22 shows the bit format for the line control registers of indirect registers [8] through [15]. Table 4-30 describes the functions of the line control registers. This register is cleared by a Master Reset or INIT. However, this register must be loaded with the appropriate information prior to using a line after a Master Reset.

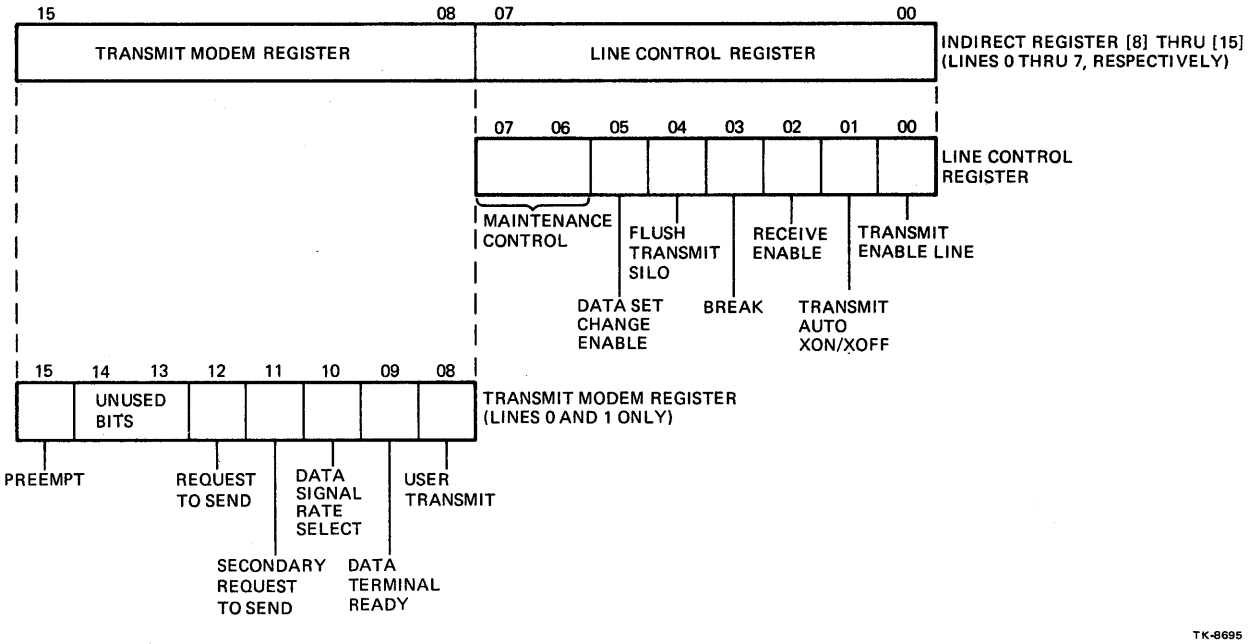

Figure 4-22 Asynchronous Indirect Registers [8] Through [15]

Table 4-30 Indirect Registers [8] Through [15] Functions

Bits	Title	Function
⟨0⟩	Transmit Enable Line	When this bit is set, the transmitter for the selected line is enabled. If this bit is clear, the transmitter for the selected line is disabled. If the transmit enable bit is cleared while a character is being transmitted, the transmitter is disabled after the complete character has been transmitted.
⟨1⟩	Transmit Auto XON/XOF	When this bit is set, XOFF disables the transmitter for the respective line. The XOFF is still loaded into the receive silo. Receiving XON reenables that line. XON is also loaded into the receive silo.
⟨2⟩	Receive Enable	When this bit is set, the receiver for the respective line is enabled. If the bit is clear, the receiver for the respective line is disabled. If the receive enable bit is set to zero while a character is being assembled, the character is lost.
⟨3⟩	Break	When this bit is set, the EIA Transmitted Data line is held spacing after the current character is serialized. Transmission resumes after the break is cleared.

Table 4-30 Indirect Registers [8] Through [15] Functions (Cont)

Bits	Title	Function
⟨4⟩	Flush Transmit Silo Line	Setting this bit flushes the transmit silo for the selected line and terminates the DMA in progress. The contents of the transmit silo are invalidated. Disabling the transmitter does not flush the silo, it just inhibits character transmission. After the silo has been flushed, this bit is automatically cleared and a transmit interrupt is generated.
⟨5⟩	Data Set Change Enable	When set, this bit enables the DMF32 to search for a transition in the modem receive signals for the selected line. Finding a change results in an entry into the receive silo with the data change bit set. If the data set change enable bit is clear, transitions on the receive modem lines for the selected line are ignored.
⟨7:6⟩	Maintenance Control Function Line	Table 4-31 defines the maintenance control function bits.
⟨8⟩	User Transmit	This line is connected (via a jumper) to pin 18 of the respective line's 25-pin Cinch connector on the distribution panel. This pin is an EIA RS232-C unassigned pin that can be used for any purpose.
⟨9⟩	Data Terminal Ready	This bit controls the Data Terminal Ready line (EIA RS-232-C circuit CD) connected to the modem. When bit⟨9⟩ is set, the Data Terminal Ready line is in the ON state. If this bit is clear, the line is in the OFF state.
⟨10⟩	Data Signal Rate Select	Bit ⟨10⟩ controls the Data Signal Rate Select line (EIA RS-232-C circuit CH) connected to the modem. When this bit is set, the data signal rate select line is in the ON state. If the bit is clear, the line is in the OFF state. Data signal rate select is a read/write bit that is cleared by INIT, but is not affected by a Master Reset.
⟨11⟩	Secondary Request To Send	This bit controls the Secondary Request to Send line (EIA RS-232-C circuit SCA) connected to the modem. When this bit is set, the Secondary Request to Send line is in the ON state; if the bit is clear, the line is in the OFF state.

Table 4-30 Indirect Registers [8] Through [15] Functions (Cont)

Bits	Title	Function
⟨12⟩	Request To Send	Bit ⟨12⟩ controls the Request to Send line (EIA RS-232-C circuit CA) connected to the modem. When this bit is set, the Request to Send line is in the ON state; if the bit is clear, the line is in the OFF state.
⟨14:13⟩	Unused Bits	
⟨15⟩	PREEMPT	This bit may be set by the program to preempt silo output. When set, transmisssion is halted. The user may then load the transmit character indirect register. The low byte loaded is transmitted and the silo is reenabled. This allows the program to interrupt a silo or DMA transmission, send a character (presumably an XON or XOFF), then continue silo or DMA transmission. No characters are lost; the preempt character is merely inserted into the effective transmit output stream. Loading the character into the indirect register clears this bit.

Table 4-31 Maintenance Control Function Bits

Bits ⟨7:6⟩	Definition
00	Normal operation.
01	Automatic echo mode. The received data is retransmitted at the same baud rate as the receiver, regardless of the state of the transmit enable bit. The receive enable bit must be set for this mode to work.
10	Local loopback. The transmitter output is internally connected via DMF32 to the receiver input. The EIA Transmitted Data line is held marking, while the EIA Received Data is ignored. Various other conditions must be satisfied to operate in local loopback mode. Also, various modem receive signals are ignored when operating in this mode. Refer to Section 4.10 for a description of these conditions.
11	Remote Loopback. The received data is not loaded into the receive silo, but is automatically retransmitted. The receive clock clocks the transmitter. The transmit enable bit is ignored.

The transmit modem registers contain the modem signals applied to the DCE. Each transmit modem register controls a respective line (transmit modem register of indirect register [8] controls line 0, indirect register [9] controls line 1). The transmit modem registers for indirect registers [10] through [15] are not used. Figure 4-22 shows the bit format for the transmit modem registers. Table 4-30 describes the functions of the transmit modem registers.

Although this register may be read and written for all lines, only lines 0 and 1 actually have modem connections. A Master Reset does not clear the actual transmit modem lines even though the bits in this register are zero. The actual signals are updated after the transmit modem register is loaded. An INIT clears the actual modem signals.

4.9.3 Indirect Registers [16] Through [23] (Read/Write)

Indirect registers [16] through [23] have an address of base +12. Read/modify/write UNIBUS cycles are allowed. These registers are accessed by word only.

Each buffer address register is used only if the respective line is in DMA mode. This register should be loaded with the low 16-bits of the DMA buffer address for the respective line.

This register is read/write, and is not necessarily cleared by Master Reset or INIT. After a read or write of the DMA buffer address register, subsequent reads or writes of the indirect register will access the DMA character count register. This permits two writes of the indirect register to load first the DMA buffer address register and then the DMA character count register without an intervening write to the indirect address register (asynchronous CSR bits ⟨4:0⟩). However, the indirect address register remains pointing to the DMA buffer address register because only a working copy of the indirect address register used by DMF32 microcode is auto-incremented. To access any other indirect register, including the DMA buffer address register, the indirect register must be reloaded. Reloading the indirect register updates the working copy of the indirect register with the appropriate address.

The appropriate register is loaded with the low 16-bits of the DMA buffer address for the respective line (indirect register [16] is used for line 0, indirect register [17] is used for line 1).

Figure 4-23 shows the bit format for indirect registers [16] through [23].

These registers are read/write and are not always cleared by a Master Reset or an INIT.

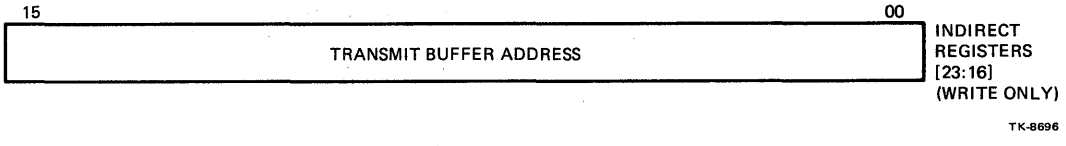

Figure 4-23 Asynchronous Indirect Registers [16] Through [23]

4.9.4 Indirect Registers [24] Through [31]

Each indirect register [24] through [31] contains two registers: DMA character count register and the upper two bits of the transmit buffer address. Bits ⟨13:00⟩ of indirect registers [24] through [31] contain the 14-bit character counts for the respective lines (indirect register [24] is used for line 0, indirect register [25] is used for line 1).

Bits ⟨15:14⟩ contain the two most significant bits of the 18-bit UNIBUS buffer address for the transmit lines.

Figure 4-24 shows the bit format for indirect registers [24] through [31].

Indirect registers [24] through [31] are read/write registers that are used only in DMA mode. Read/modify/write UNIBUS cycles are allowed. Writing to these registers initiates a DMA transfer. These registers are not always cleared by a Master Reset or INIT.

4.10 RELATIONSHIP BETWEEN MAINTENANCE MODES AND MODEM SIGNALS

Table 4-32 lists the relationship between maintenance modes and modem signals.

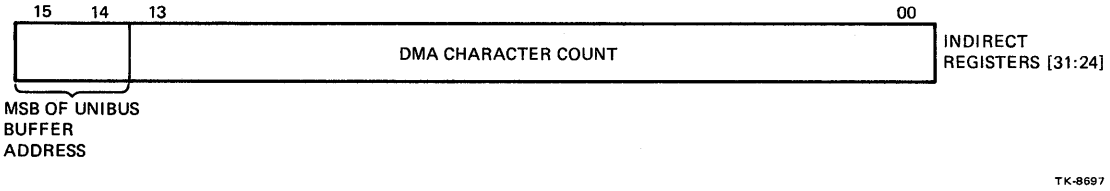

Figure 4-24 Asynchronous Indirect Registers [24] Through [31]

Table 4-32 Relationship Between Maintenance Modes and Modem Signals

Async Line	Mode	Description
0	Normal operation, auto echo, and remote loopback	Async line zero Carrier Detect modem signal must be ON for the receiver to operate.
0	Local loopback	Async line zero Data Terminal Ready modem signal is OFF. Async line zero Request to Send modem signal is OFF. The programmable bit Data Terminal Ready 0 must be ON, even though the actual Data Terminal Ready modem signal for async line zero is OFF. Carrier Detect 0 follows the state of Data Terminal Ready 0. The Carrier Detect modem signal for async line zero is ignored. The programmable bit Request to Send 0 must be ON, even though the actual Request to Send modem signal for async line zero is OFF.

Table 4-32 Relationship Between Maintenance Modes and Modem Signals (Cont)

Async Line	Mode	Description
1	Normal operation, auto echo, and remote loopback	Async line one Carrier Detect modem signal must be ON for the receiver to operate.
1	Local loopback	Async line one Data Terminal Ready modem signal is OFF. Async line one Request to Send modem signal is OFF. The programmable bit Data Terminal Ready 1 must be ON, even though the actual Data Terminal Ready modem signal for async line one is OFF. Carrier Detect 1 follows the state of Data Terminal Ready 1. The Carrier Detect modem signal for async line one is ignored. The programmable bit Request to Send 1 must be ON, even though the actual Request to Send modem signal for async line one is OFF.
2	Normal operation, auto echo, and remote loopback	Operation is independent of any modem signals.
2	Local loopback	User Transmit modem signal for async line zero is OFF. The Secondary Request to Send modem signal for async line zero is OFF. The programmable bit USER TX 0 must be ON, even though the actual User Transmit modem signal for async line zero is OFF. The programmable bit Secondary Request to Send 0 must be ON, even though the actual Secondary Request to Send modem signal for async line zero is OFF.
3	Normal operation, auto echo, and remote loopback	Operation is independent of any modem signals.
3	Local loopback	User Transmit modem signal for async line one is OFF. The Secondary Request to Send modem signal for async line one is OFF. The programmable bit USER TX 1 must be ON, even though the actual User Transmit modem signal for async line one is OFF. The programmable bit Secondary Request to Send 1 must be ON, even though the actual Secondary Request to Send modem signal for async line one is OFF.

Table 4-32 Relationship Between Maintenance Modes and Modem Signals (Cont)

Async Line	Mode	Description
4	Normal operation, auto echo, and remote loopback	Operation is independent of any modem signals.
4	Local loopback	The Data Signal Rate Select modem signals for async lines zero and one are OFF. The programmable bit Data Signal Rate Select 0 must be ON, even though the actual Data Signal Rate Select modem signal for async line zero is OFF. The programmable bit Data Signal Rate Select 1 must be ON, even though the actual Data Signal Rate Select modem signal for asynchronous line one is OFF.
5	Normal operation, auto echo, and remote loopback	Operation is independent of any modem signals.
5	Local loopback	The Request to Send modem signal for the synchronous line is OFF. The Data Terminal Ready modem signal for the synchronus line is OFF. The programmable bit Data Terminal Ready in the sync line must be ON, even though the actual Data Terminal Ready modem signal for the sync line is OFF. The programmable bit Request to Send in the sync line must be ON, even though the actual Request to Send modem signal for the sync line is OFF.
6	Normal operation, auto echo, and remote loopback	Operation is independent of any modem signals.
6	Local loopback	The User Transmit modem signal for the synchronous line is OFF. The Data Signal Rate Select modem signal for the synchronous line is OFF. The programmable bit USER TX in the sync line must be ON, even though the actual User Transmit modem signal for the sync line is OFF. The programmable bit Data Signal Rate Select in the sync line must be ON; even though the actual Data Signal Rate Select modem signal for the sync line is OFF.
7	Normal operation, auto echo, and remote loopback	Operation is independent of any modem signals.
7	Local loopback	Operation is independent of any modem signals.

4.11 LINE PRINTER CONTROLLER

The line printer controller interfaces with LP model printers. Optionally, this DMA device can perform the following low level formatting functions:

- Tab expansion
- Automatic carriage return insertion
- Automatic line wrap
- Form feed to multiple line feed conversion

The line printer controller uses two UNIBUS addresses. The first address accesses the line printer CSR, while the second address accesses one of eight indirect registers. The indirect address field (line printer CSR bits ⟨10:8⟩) determines which one of the eight indirect registers is to be accessed.

The printer CSR performs enables:

- The printer controller
- Formatting
- Printer interrupt
- Master reset

The printer CSR points to one of eight indirect addresses. It also indicates:

- Connect verify
- Print done
- Line printer error
- DMA error
- DAVFU ready

4.11.1 Line Printer Controller Operation

After power up or an INIT, the line printer controller is in the idle state. Next the program should set the appropriate bits in the line printer CSR bits.

4.11.1.1 Loading Line Printer CSR and Indirect Registers – The line printer CSR and indirect registers should be loaded as follows.

1. If formatting is desired, the format control (line printer CSR bit ⟨2⟩) is set to one; the indirect register address field (line printer CSR bits ⟨10:8⟩) is set to two. Setting the interrupt enable bit (line printer CSR bit ⟨6⟩) enables the interrupts.

2. The program loads indirect register [2] bits ⟨15:0⟩ with the prefix character (indirect register [2] bits ⟨15:8⟩) and the prefix character count (indirect register [2] bits ⟨7:0⟩). The prefix character count specifies the number of prefix characters inserted at the beginning of the message. Accessing the indirect register, increments the indirect address field (line printer CSR bits ⟨10:8⟩) by one.

3. The program then loads indirect register [3] bits ⟨15:0⟩ with the suffix character (indirect register [3] bits ⟨15:8⟩) and the suffix character count (indirect register [3] bits ⟨7:0⟩). The suffix character count specifies the number of suffix characters to be appended at the end of the message.

4. The program loads the low order 16 bits of the DMA buffer address into the indirect register [4] bits ⟨15:0⟩. The program then loads the DMA character count into indirect register [5] bits ⟨15:0⟩. The next word loaded should contain the two high order bits of the UNIBUS DMA buffer address, and certain format control.

5. The last word loaded should contain the number of lines on a page (indirect register [7] bits ⟨7:0⟩) and the carriage width (indirect register [7] bits ⟨15:8⟩) for the particular line printer used.

6. If formatting is not desired, then the format control (line printer CSR bit ⟨2⟩) is cleared to zero. The indirect register address field (line printer CSR bits ⟨10:8⟩) is set to 4. Three writes to the indirect register load the DMA character count and buffer address.

At this point, all the appropriate indirect registers have been loaded. Table 4-33 list the indirect registers.

4.11.1.2 Line Printing Cycle – To initiate printing, the program sets the print enable bit (line printer CSR bit ⟨0⟩). After the device successfully transfers the last character to the line printer, the print done bit (line printer CSR bit ⟨7⟩) is set. The print enable bit automatically clears when the print done bit becomes set. If the interrupt enable bit (line printer CSR bit ⟨6⟩) is set, an interrupt request is posted. The interrupt service routine should read the line printer CSR. If the service routine finds the print done bit (line printer CSR bit ⟨7⟩) set and the line printer error bit (line printer CSR bit ⟨14⟩) clear, this indicates a successful print cycle.

The indirect register auto-increment feature reduces the number of device register accesses the interrupt service routine must make. Either a read or write to an indirect register increments the address field by one.

After a successful print cycle, if formatting is enabled, the program should read the indirect register twice to retrieve two words of status. The indirect address field is equal to zero at this time. The first word (indirect register [0]) is a count of the number of bytes transferred to the line printer. The second word (indirect register [1]) contains a 16-bit count of the number of lines the paper has moved from the last print cycle.

After having read the status of the previous print cycle, the indirect register address field points to indirect register [2]. To initiate a new DMA cycle, successive writes to the indirect register are executed to load the desired parameters and then the print enable bit (line printer CSR bit ⟨0⟩) is set.

Table 4-33 Line Printer Indirect Registers

Indirect Register	Name
[0] - bits ⟨15:0⟩	Bytes transmitted
[1] - bits ⟨15:0⟩	Line count
[2] - bits ⟨15:8⟩	Prefix character
[2] - bits ⟨7:0⟩	Prefix character count
[3] - bits ⟨15:8⟩	Suffix character
[3] - bits ⟨7:0⟩	Suffix character count
[4] - bits ⟨15:0⟩	DMA buffer address ⟨15:0⟩
[5] - bits ⟨15:0⟩	DMA character count
[6] - bits ⟨1:0⟩	DMA buffer address ⟨17:16⟩
[6] - bits ⟨7:2⟩	Unused bits
[6] - bit ⟨8⟩	Auto carriage return insert
[6] - bit ⟨9⟩	Form feed to line feed convert
[6] - bit ⟨10⟩	Nonprintable character accept
[6] - bit ⟨11⟩	DAVFU
[6] - bit ⟨12⟩	Line wrap
[6] - bits ⟨14:13⟩	Unused bits
[6] - bits ⟨15⟩	Lower case to upper case convert
[7] - bits ⟨15:8⟩	Line printer carriage width
[7] - bits ⟨7:0⟩	Lines per page

4.12 LINE PRINTER CSR REGISTER

The line printer control status register has an address of base +14. Read/modify/write UNIBUS cycles are allowed. This register is accessed by word only.

Figure 4-25 shows the bit format for the line printer CSR. Table 4-34 describes the functions for the line printer CSR.

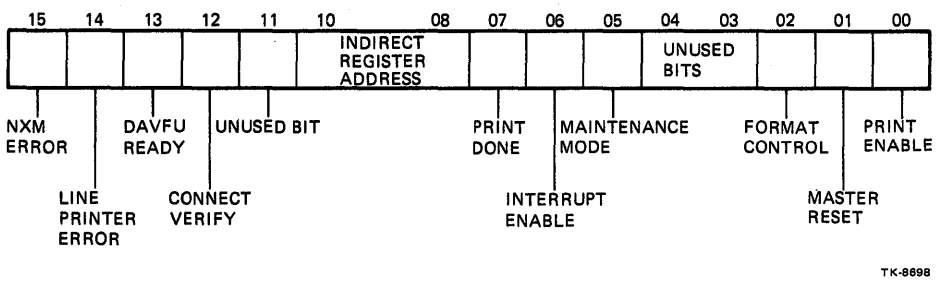

Figure 4-25 Line Printer CSR

Table 4-34 Line Printer Control Status Register Functions

Bits	Title	Function
⟨0⟩	Print Enable	This bit is used to initiate, suspend, or continue line printer output. When this bit is set, the line printer controller is enabled. When enabled, characters are transferred from the controller to the line printer, provided there are characters to send. If this bit is clear, no characters are transferred from the controller to the line printer. If the print done bit (line printer CSR bit ⟨7⟩) is set, writing a one to set the print enable bit (line printer CSR bit ⟨0⟩) clears the following: • DMA error (line printer CSR bit ⟨15⟩ • Print done (line printer CSR bit ⟨7⟩ • Indirect register [0] (bytes transmitted) • Indirect register [1] (line count) This bit is read/write and is cleared by either a Master Reset or INIT. This bit is automatically cleared when the print done bit (line printer CSR bit ⟨7⟩) or DMA error bit (line printer CSR bit ⟨15⟩) becomes set.
⟨1⟩	Master Reset	The program can read Master Reset, but write ones only. When the program sets this bit, a Master Reset is initiated. The Master Reset bit remains set while the reset is in progress, and clears automatically after the reset has finished. The program should not access the line printer device registers, other than line printer CSR, while the reset is in progress. The program may write a one to the Master Reset while the reset is in progress, but the DMF32 ignores such action. Master Reset or an INIT clears lines per page ⟨7:0⟩. All other indirect registers are indeterminate after a Master Reset or INIT. The device driver ensures that the indirect registers contain valid data. The Master Reset may be used to abort the output.
⟨2⟩	Format Control	When the format control field is clear, formatting is disabled. Characters from main memory are direct memory accessed directly to the line printer. When the format control field contains 1, formatting is enabled.

Table 4-34 Line Printer Control Status Register Functions (Cont)

Bits	Title	Function
		If the format control field contains 1, and DAVFU bit is set, all direct memory accessed characters with MSB set are discarded by DMF32, unless the character is a "paper instruction channel select" code (#200:#213), or a "paper instruction, lines to be stepped" code (#200:#237) in which case, the character is passed on to the printer. However, if the format control field contains 1 and DAVFU bit is clear, all direct memory accessed characters with MSB set are discarded by DMF32. If the format control field contains 0, all characters, regardless of their MSB, are transmitted to the line printer. The format control field is read/write, and is cleared by a Master Reset or an INIT.
⟨4:3⟩	Unused Bits	These bits are always read as zeros.
⟨5⟩	Maintenance Mode	When this bit is set, data is not sent to the line printer, but written into the DMF32 diagnostic register. The diagnostic register is the second word of the 16 words DMF32 responds to. After setting the print enable bit (line printer CSR bit ⟨0⟩), the software should wait at least 500 μs before reading the looped back data. It should also wait 500 μs between subsequent reads. If the register is read sooner, it may contain zeros until the character is loaded in by microcode. This bit is read/write and cleared by a Master Reset or INIT.
⟨6⟩	Interrupt Enable	If the interrupt enable bit is set, interrupt requests are posted when the error rbit (line printer CSR bit ⟨15⟩) or the print done bit (line printer CSR bit ⟨7⟩) becomes set. The interrupt enable bit is read/write, and is cleared by a Master Reset or an INIT.
⟨7⟩	Print Done	If the format control field contains 0, the print done bit (line printer CSR bit ⟨7⟩) is set after the DMA transfer is complete and all characters are transferred to the line printer. If the format control field contains 1, the print done bit (line printer CSR bit ⟨7⟩) is set after the DMA transfer is complete and all characters, including extra formatting characters (suffix characters), are transferred to the line printer. Setting bit ⟨7⟩ causes an interrupt request to be posted, if the interrupt enable bit (line printer CSR bit ⟨6⟩) is set. Bit ⟨7⟩ is set when bit ⟨15⟩ (DMA error) is set. The print done bit is read-only, and is cleared by setting the print enable bit. It is set by either a Master Reset or by an INIT.

Table 4-34 Line Printer Control Status Register Functions (Cont)

Bits	Title	Function
⟨10:8⟩	Indirect Address Field	Bits ⟨10:8⟩ point to one of eight word registers. After an access (read or write) to an indirect register, the indirect address field is automatically incremented by one. When the print done bit (line printer CSR bit ⟨7⟩) or error bit (line printer CSR bit ⟨15⟩) is set, the indirect address field is automatically cleared to zero. This automatic increment feature may be used in the following way. After an interrupt is posted due to the print done bit (line printer CSR bit ⟨7⟩) becoming set, the program reads the line printer CSR register. The program finds, for example, that the print done bit is set and the error bit is clear. The program reads from address Base + 16. Since the indirect register address field points to zero, the first three words should be read to get the status of the previous DMA transfer. The program now sets up parameters for the next DMA transfer. This is done by writing a word of prefix information to the address Base + 16, then writing again with a word of suffix information. The next word loaded contains the DMA buffer address, and the word loaded after that is the DMA character count. Assuming that the other indirect registers already contain valid data, the program sets the print enable bit to initiate printing. The indirect register address field is read/write and cleared by a Master Reset or an INIT. Table 4-35 lists the line printer indirect registers.
⟨11⟩	Unused Bit	This bit is always read as a zero.
⟨12⟩	Connect Verify	This read/only bit reflects the state of a signal from the DMF32, that goes to the line printer where it is looped around and then read back by the DMF32. If this bit is clear, the line printer is connected to the DMF32 distribution panel. If this bit is set, the line printer is not connected.
⟨13⟩	DAVFU Ready	This bit reflects the state of the DAVFU ready line from the line printer. This bit is not affected by a Master Reset or an INIT.
⟨14⟩	Line Printer Error	This bit reflects the state of the OFFLINE signal from the line printer. When this bit is set, the line printer is offline. The zero to one transition of this bit posts an interrupt if the interrupt enable bit (line printer CSR bit⟨6⟩) is set. This bit is read-only.

Table 4-34 Line Printer Control Status Register Functions (Cont)

Bits	Title	Function
⟨15⟩	DMA Error	This bit is set if the DMF32 UNIBUS controller either did not receive SSYN at least 32 μs after issuing a MSYN, or the controller could not become bus master for at least 32 μs after having asserted BUS NPR. This bit is read-only and is cleared by a Master Reset, or INIT, or writing a 1 to the print enable bit.

4.13 LINE PRINTER INDIRECT REGISTERS

The line printer controller uses eight read/write indirect registers. These registers are addressed by the line printer CSR bits ⟨10:8⟩. Read/modify/write UNIBUS cycles are not allowed to the indirect registers. Table 4-35 describes the functions of the line printer indirect registers. Figure 4-26 shows the bit configuration of Indirect Register [6].

Table 4-35 Line Printer Indirect Registers Functions

Register/Bits	Title	Function
Indirect Register [0] Bits ⟨15:0⟩	Bytes Transmitted	This register contains the number of bytes transferred from the line printer controller to the line printer. If format control (line printer CSR bit ⟨2⟩ equals one, the prefix characters, formatted data, and suffix characters are included in the count. When the format control (line printer CSR bit ⟨2⟩) equals zero, the bytes transmitted (indirect register [0] bits ⟨15:0⟩) indicate the actual number of characters direct memory accessed. If the print done bit is set, writing a 1 to the print enable bit clears the bytes transmitted register (indirect register [0] bits ⟨15:0⟩).
Indirect Register [1] Bits ⟨15:0⟩	Line Count	Line count register bits ⟨15:0⟩ is used only if DAVFU is clear. This register contains a count of the number of lines the paper on the line printer has moved from printing the latest buffer. If print done bit is set, writing a 1 to the print enable bit clears this register.

Table 4-35 Line Printer Indirect Registers Functions (Cont)

Register/Bits	Title	Function
Indirect Register [2] Bits ⟨15:8⟩	Prefix Character	Indirect register [2] bits ⟨15:8⟩ is loaded with the type of prefix character to be inserted at the beginning of the buffer. A zero value for this prefix character is interpreted as a "new line" command. A "new line" command is a carriage return followed by a line feed that is sent to the line printer. The carriage return preceeds the line feed only if the automatic carriage insert bit (indirect register [6] bit ⟨8⟩) is not active, that is, equal to one. If the prefix character count (indirect register [2] bits ⟨7:0⟩) equals zero, then no prefix characters are sent.
Indirect Register [2] Bits ⟨7:0⟩	Prefix Character Count	The prefix character count register (indirect register [2] bits ⟨7:0⟩) is loaded with the number of prefix characters to be inserted at the beginning of the buffer.
Indirect Register [3] Bits ⟨15:8⟩	Suffix Character	Indirect register [3] bits ⟨15:8⟩ is loaded with the type of suffix character to be appended at the end of the buffer. A zero value for this suffix character is interpreted as a "new line" command. A "new line" command is a carriage return followed by a line feed that is sent to the line printer. The carriage return preceeds the line feed only if the automatic carriage insert bit (indirect register [6] bit ⟨8⟩) is not active, that is, equal to one. If the suffix character count (indirect register [3] bits ⟨7:0⟩) equals zero, then no suffix characters are sent.
Indirect Register [3] Bits ⟨7:0⟩	Suffix Character Count	The suffix character count register (indirect register [3] bits ⟨7:0⟩) is loaded with the number of suffix characters to be appended at the end of the buffer.

Table 4-35 Line Printer Indirect Registers Functions (Cont)

Register/Bits	Title	Function
Indirect Register [4] Bits ⟨15:0⟩	DMA Buffer Address	This register contains the low-order bits of the UNIBUS DM buffer address. The two high-order bits reside in the indirect register [6] bits ⟨1:0⟩.
Indirect Register [5] Bits ⟨15:0⟩	DMA Character Count	This register is loaded with the 16 bit DMA character count.
Indirect Register [6] Bits ⟨1:0⟩	DMA Buffer Address (two most significant bits)	Indirect register [6] bits ⟨1:0⟩ are loaded with the two most significant bits of the UNIBUS DMA buffer address.
Indirect Register [6] Bits ⟨7:2⟩	Unused Bits	
Indirect Register [6] Bit ⟨8⟩	Automatic Carriage	If the format control (line printer CSR bit ⟨2⟩) equals one, and the automatic carriage insert bit is clear, the line printer automatically inserts a carriage return before a line feed or form feed. Carriage returns in the data stream preceeding a line feed or form feed are stripped out if automatic carriage insert bit is active.
Indirect Register [6] Bit ⟨9⟩	Form Feed/ Line Feed Convert	If format control (line printer CSR bit ⟨2⟩) equals one, and the form feed/line feed convert is clear, a form feed is translated into multiple line feeds to reach the next top of form.

Table 4-35 Line Printer Indirect Registers Functions (Cont)

Register/Bits	Title	Function
Indirect Register [6] Bit ⟨10⟩	Nonprintable Character Accept	If format control (line printer CSR bit ⟨2⟩) equals one, this bit specifies that nonprintable, non control characters are sent to the line printer, assuming that such a character causes a space to be printed. Characters with the MSB set are considered nonprintable characters. If this bit is set, all characters with the MSB set are transferred to the line printer, regardless of the setting of DAVFU bit. If format control (line printer CSR bit ⟨2⟩) equals one and this bit is clear, then the DMF32 discards nonprintable characters.
Indirect Register [6] Bit ⟨11⟩	Direct Access Vertical Format Unit (DAVFU)	The program sets this bit if the line printer is a DAVFU. When DAVFU bit is set, special vertical format control codes are allowed to be direct memory accessed to the line printer.
Indirect Register [6] Bit ⟨12⟩	Line Wrap	If format control (line printer CSR bit ⟨2⟩) equals one and this bit is set, a carriage return and line feed are inserted into the character stream prior to the current character if the horizontal position of the current character is past the value stored in the line printer carriage width (indirect register [7] bits ⟨15:8⟩). If the automatic carriage insert bit is set, only the line feed is sent to the printer.
Indirect Register [6] Bits ⟨14:13⟩	Unused Bits	
Indirect Register [6] Bit ⟨15⟩	Lower Case to Upper Case Convert	If format control (line printer CSR bit ⟨2⟩) equals one and the lower case to upper case conversion bit is clear, this specifies lower case character to upper case character conversion.

Table 4-35 Line Printer Indirect Registers Functions (Cont)

Register/Bits	Title	Function
Indirect Register [7] Bits ⟨7:0⟩	Lines Per Page	If format control (line printer CSR bit ⟨2⟩) equals one, and the DAVFU bit is clear, then the indirect register [7] bits ⟨7:0⟩ (lines per page) is loaded with the number of lines on a page for the attached line printer.
Indirect Register [7] Bits ⟨15:8⟩	Line Printer Carriage Width	If format control (line printer CSR bit ⟨2⟩) equals one, the line carriage width (indirect register [7] bits ⟨15:8⟩) is loaded with the width of the carriage of the attached line printer.

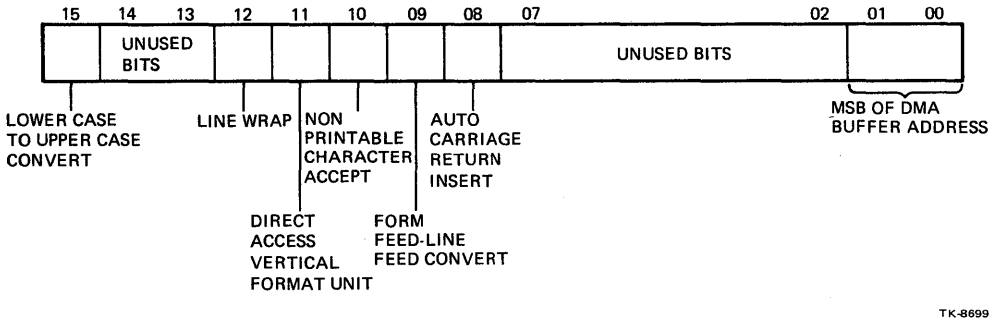

Figure 4-26 Line Printer Indirect Registers [6]

4.14 PARALLEL INTERFACE (DR)

The parallel interface (DR) is not only functionally a DR-11-C, but also supports silo data transfers or double buffered DMA transfers in one direction. The parallel interface can operate in three modes: DR-11-C functional mode, silo mode and DMA mode. When the device is not in the DR-11-C mode, an enhanced transfer protocol is emulated. This enhanced transfer protocol causes a transfer or interrupt request to occur whenever a zero-to-one or a one-to-zero transition of either User Request A or User Request B line occurs.

4.14.1 DR-11-C Functional Mode

In this mode, the program reads the parallel interface input buffer to read data from the user device. After the data has been read, the DMF32 pulses the Data Transmitted line to inform the user device that the data has been read and that the data hold time has been satisfied. The parallel interface buffer bits ⟨15:0⟩ reflects the state of the 16 input line wires at the time the parallel interface input buffer bits ⟨15:0⟩ is read.

The program writes to the parallel interface output buffer bits ⟨15:0⟩ to write data to the user device. The 16 output lines to the user device reflect the state of the parallel interface output buffer bits ⟨15:0⟩. After the program writes to the parallel interface buffer, the DMF32 pulses the New Data Ready line.

4.14.1.1 DR-11-C User Request A and B – The user device controls both the User Request A and B lines. User Request A is reflected in the parallel interface CSR bit ⟨7⟩; User Request B line is reflected in the parallel interface CSR bit⟨15⟩.

When the Interrupt Enable A bit (parallel interface CSR bit ⟨6⟩) is set, a zero-to-one transition of User Request A line causes an interrupt request to Vector A. Similarly, if the Interrupt Enable B bit is set, a zero-to-one transition of User Request B causes an interrupt request to vector B.

4.14.2 Silo Mode

In silo mode, the 32-word silo can be used as either a transmit silo or as a receive silo, depending on the mode selected. Both User Request A and B lines are activated by either a zero-to-one or one-to-zero transition. One of the user request lines must be dedicated to operate as a transfer request line so that the user device can access the silo without program intervention.

4.14.2.1 Writing To and Reading From Silo – If the silo is being used for receive, the program reads the silo via the parallel interface input buffer. Each read of the parallel interface input buffer causes the silo entries to shift down by one word. However, if the silo is being used for transmit, the program loads a data word into the silo by writing to the parallel interface output buffer. The contents of the silo (either transmit or receive) can be flushed by the program writing a one to the flush buffer bit (parallel interface bit ⟨11⟩).

4.14.2.2 Silo Request A and B – The following explanation assumes that the User Request A is programmed for use as the transfer request line, and the silo is used to receive words (mode = 0111).

After the user device changes the state of the User Request A line, the parallel interface reads the data, pulses the Data Transmitted signal, and loads the data word into the silo. After a word is loaded into the silo, the parallel interface sets Request A (parallel interface CSR bit ⟨7⟩).

If the Interrupt Enable A bit (parallel interface CSR bit ⟨6⟩) is set when Request A changes state, an interrupt request is posted for vector A. However, the User Request A line can be used to load up to 32 words into the silo before the interrupt service routine empties the silo. After 32 words are loaded into the silo, the parallel interface does not accept any more characters until the program reads from the silo. The parallel interface indicates to the user device that the silo is full (cannot accept any more characters) by not pulsing the Data Transmitted signal in response to User Request A line. In this example, the operation of User Request B is the same as in DR11-C functional mode; that is, asserting User Request B causes an interrupt request to vector B if the interrupt enable B bit (parallel interface CSR bit ⟨5⟩) is set.

4.14.3 DMA Mode

DMA mode is activated by setting the mode bits (miscellaneous register bits ⟨3:0⟩) appropriately. Either User Request A or Request B is selected for use as a transfer request line. Both Request A and Request B are activated by a transition on the respective line. DMA operation is double buffered, so that the program has a full buffer time to respond to an interrupt.

4.14.3.1 DMA Transfer – The following explanation assumes that User Request A is selected as the transfer line, and the DMA is a receive operation (mode = 1011). Also the NPR primary/secondary bit (parallel interface CSR bit ⟨2⟩) is clear, indicating that the primary buffer is active.

The transition (zero-to-one or one-to-zero) of User Request A indicates to the parallel interface that the user device wants to transfer data to memory. Next, the parallel interface reads the data on the 16 input lines, pulses the Data Transmitted signal, and transfers data to the on-board silo. Data in the silo is subsequently direct memory accessed to the main memory buffer. After successfully filling the buffer in main memory, the NPR primary/secondary bit (parallel interface CSR bit ⟨2⟩) and the done primary bit (parallel interface CSR bit ⟨8⟩) are both set. An interrupt request is posted to vector A provided that the Interrupt Enable A bit (parallel interface CSR bit ⟨6⟩) is set.

The DMA transfers continue into the secondary buffer, unless the done secondary (parallel interface CSR bit ⟨9⟩) is set. If the done secondary bit is set, DMA transfers are inhibited until the program writes to the secondary word count register, which clears the done secondary bit.

An error condition aborts an NPR transfer. When an error occurs, the DMA memory error (parallel interface CSR bit ⟨13⟩) is set instead of the done bit. Setting the DMA memory error bit terminates the DMA transfer. An interrupt request is posted to vector A if the interrupt enable bit (parallel interface CSR bit ⟨6⟩) is set. DMA transfers continue after a Master Reset or INIT clears the error bits.

When receive DMA is used, the program may read the parallel interface input buffer to read the previous word that was direct memory accessed to memory. If transmit DMA is used, a program write to the parallel interface output buffer causes the written data to be applied to the output lines as the next transfer to the user device, after which DMA transmissions are resumed.

Request A bit (parallel interface CSR bit ⟨7⟩) reflects the state of the User Request A line, but does not post an interrupt request. User Request B functions as a general purpose interrupt request line.

The DMA buffer address register is 17 bits long. The least significant bit is assumed to be zero (the address is on a word boundary). The word count register specifies the number of words to be direct memory accessed.

4.14.4 Parallel Interface Device Registers

The parallel interface uses four device registers and four indirect registers. The registers are as follows:

- Parallel interface control status register
- Output buffer
- Input buffer/miscellaneous register
- Indirect registers

4.14.4.1 Parallel Interface Control Status Register – The read/write parallel interface control status register has an address of base +1E. Read/modify/write UNIBUS cycles are not allowed. This register is accessed by word only.

The parallel interface control status register enables the following:

- Control zero line
- Control one line
- Interrupt enable B
- Interrupt enable A
- Buffer flush
- Master reset

This register also points to one of four indirect registers, and indicates the following:

- Primary or secondary buffer in use
- Primary or secondary count register in use
- Request A state
- Request B state
- Successful transfer to primary buffer (DMA mode)
- Successful transfer to secondary buffer (DMA mode)
- DMA error

Figure 4-27 shows the bit format for the parallel interface CSR. Table 4-36 describes the functions of the parallel interface CSR.

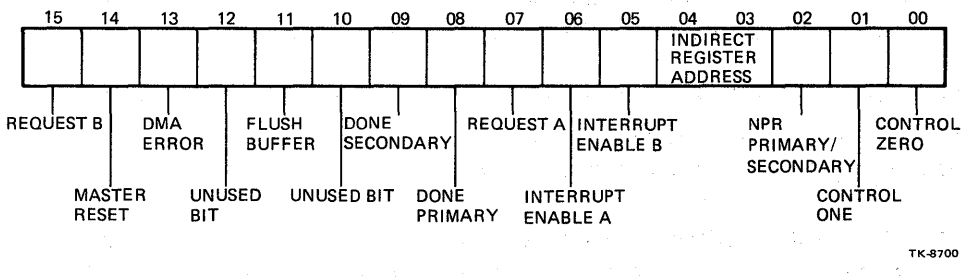

Figure 4-27 Parallel Interface CSR

Table 4-36 Parallel Interface Control Status Register Functions

Bits	Title	Function
⟨0⟩	Control Zero	Bit ⟨0⟩ controls the state of the control zero line originating from the parallel interface. When bit ⟨0⟩ is set, control zero is high. When bit ⟨0⟩ is clear, control zero is low. This bit can be used for any user-defined function. Bit ⟨0⟩ is cleared by a Master Reset or INIT.
⟨1⟩	Control One	Bit ⟨1⟩ controls the state of the control one line originating from the parallel interface. When bit⟨1⟩ is set, control one is high. When bit ⟨1⟩ is clear, control one is low. This bit may be used for any user-defined function. Bit ⟨1⟩ is cleared by a Master Reset or INIT.
⟨2⟩	NPR Primary/ Secondary	Bit ⟨2⟩ indicates which of the buffer address registers (primary or secondary) and word count registers (primary word count or secondary word count) are being used or are to be used. A zero indicates that the primary registers are active; a one indicates that the secondary registers are active. After a buffer (primary or secondary) has successfully or unsuccessfully been filled with data via DMA, NPR primary/secondary bit changes state, and thus points to the other buffer. When NPR primary/secondary bit changes state, the appropriate done bit or error bit is set, and an interrupt request is posted. If User Request A requests a DMA transfer (MODE = '1001 or '1011), then the interrupt is posted to Vector A, provided that interrupt enable A bit (DR CSR bit ⟨6⟩) is set. If User Request B requests a DMA transfer (MODE = '1010 or '1000), then the interrupt is posted to Vector B, if interrupt enable B bit (DR CSR bit ⟨5⟩) is set. After NPR primary/secondary bit changes state, data is direct memory accessed to the new buffer provided that the new buffer's done bit is not set. If the new buffer's done bit is set, then DMA is inhibited until the done bit is cleared. An error condition (DMA memory error being set) aborts the NPR transfer and causes an interrupt request to be posted. This interrupt request is posted to the same vector that would have been chosen had the buffer been filled successfully. After an error condition, operation continues only after the error bits are cleared, either by a Master Reset or INIT. NPR primary/secondary bit is read-only, and is cleared by a Master Reset or INIT.
⟨4:3⟩	Indirect Register Address	Bits ⟨4:3⟩ point to one of four indirect registers. The indirect register address is read/write, and is cleared by a Master Reset or INIT.

Table 4-36 Parallel Interface Control Status Register Functions (Cont)

Bits	Title	Function
⟨5⟩	Interrupt Enable B	When set, bit ⟨5⟩ enables interrupt request to vector B. Bit ⟨5⟩ is read/write, and is cleared by a Master Reset or INIT.
⟨6⟩	Interrupt Enable A	When set, bit ⟨6⟩ enables interrupt requests to vector A. Bit ⟨6⟩ is read/write, and is cleared by a Master Reset or INIT.
⟨7⟩	Request A	The state of bit ⟨7⟩ follows that of the input signal USER REQUEST A. In DR11-C functional mode (Mode ⟨3:0⟩ = '0000), the zero to one transition of user REQUEST A causes an interrupt request to be posted to Vector A if the Interrupt Enable A bit is set. In silo mode with the User Request A line requesting a data transfer (miscellaneous register bits ⟨3:0⟩ equals either 0101 or 0111), any transition (zero-to-one or one-to-zero) causes either data to enter the silo from the user device (receive) or leave the silo to be transferred to the user device (transmit). After the data has entered or left the silo, an interrupt request is posted to Vector A provided that the interrupt enable A bit is set. The receive buffer cannot overflow; after 32 words are entered into the silo, the DMF32 will not accept any more characters until the program reads from the silo to provide room for more characters. The DMF32 informs the user device that it will not accept any more characters by not pulsing the Data Transmitted line in response to the User Request line, thus not completing the handshaking protocol. Also, the silo cannot underrun in SILO transmit mode. If the silo is empty and the user device requests new data by changing the state of the User Request line, the DMF32 does not apply new data to the output lines or pulse the New Data Ready signals until the program has entered new data into the silo. In DMA mode (receive or transmit), if User Request A requests a data transfer (Mode ⟨3:0⟩ = '1001 or '1011), the zero-to-one or one-to-zero transition of Request A does not cause an interrupt request to be posted, but is used by the user device to transfer data.
⟨8⟩	Done Primary	Bit ⟨8⟩ is used only in DMA mode. This bit is set if a DMA transfer to or from the primary buffer has completed successfully. If a DMA transfer aborts due to an error condition, the DMA error bit is set instead of the done primary bit. Bit ⟨8⟩ is read-only, and is cleared by writing to the primary word count register. It is set by a Master Reset or an INIT.

Table 4-36 Parallel Interface Control Status Register Functions (Cont)

Bits	Title	Function
⟨9⟩	Done Secondary	Bit ⟨9⟩ is used only in DMA mode. This bit is set if a DMA transfer to or from the secondary buffer has completed successfully. If a DMA transfer aborts due to an error condition, the DMA error bit is set instead of the done secondary bit. This bit is read-only, and is cleared by writing to the secondary word count register. It is set by a Master Reset or an INIT.
⟨10⟩	Unused Bit	
⟨11⟩	Flush Buffer	Bit ⟨11⟩ is used only in silo mode. Writing a one to the flush buffer causes the contents of the buffer to be invalidated. This bit is cleared by either a Master Reset or INIT.
⟨12⟩	Unused Bit	
⟨13⟩	DMA Error	This bit is used only in DMA mode. It is set when the DMF32 UNIBUS controller either did not receive a BUS SSYN at least 32 μs after issuing a BUS MSYN, or the controller could not become bus master for at least 32 μs after having asserted BUS NPR. Setting the DMA error bit causes an interrupt to Vector A or B, depending on whether User Request A or User Request B is used to request the data transfer, respectively. The respective interrupt bit must be set to post an interrupt request. This bit is read-only, and can only be cleared by a Master Reset or INIT.
⟨14⟩	Master Reset	When the program sets this bit, a Master Reset is initiated. This bit remains set while the reset is in progress and clears automatically after the reset is completed. While the Master Reset is occurring, the program should not access the DMF32 parallel interface device registers, except for the parallel interface CSR. The program may write an one to the Master Reset bit while a reset is occurring, but such action is ignored. The Master Reset bit is high when the reset is occurring. A Master Reset initializes various CSR bits as specified in the bit descriptions.

Table 4-36 Parallel Interface Control Status Register Functions (Cont)

Bits	Title	Function
⟨15⟩	Request B	The state of bit ⟨15⟩ follows the state of the input signal user Request B. In DR11-C functional mode (Mode ⟨3:0⟩ = '0000), the zero-to-one transition causes an interrupt request to be posted to Vector B provided that Interrupt Enable B bit (parallel interface CSR bit ⟨5⟩) is set. In SILO mode, with the User Request B line requesting a data transfer (miscellaneous register bits ⟨3:0⟩ equals either 0110 or 0100), any transition (zero-to-one or one-to-zero) causes either data to enter the silo from the user device (receive) or leave the silo to be transferred to the user device (transmit). After the data has entered or left the silo, an interrupt request is posted to Vector B provided that the interrupt enable B bit is set. The miscellaneous register has an address of base +1C. This write-only register is accessed by word only. When in DMA mode (receive or transmit), if User Request B requests a data transfer (Mode ⟨3:0⟩ = '1010 or '1000), the zero-to-one or one-to-zero transition of Request B does not cause an interrupt request to be posted, but is used by the user device to transfer data.

4.14.4.2 Parallel Interface Output Buffer – The parallel interface output buffer has an address of base +1A. Read/modify/write UNIBUS cycles are not allowed. In the DR11-C functional mode, this register can be accessed by either high or low byte. In DMA and silo modes, this register is accessed by word only.

In DR11-C functionality mode, silo receive mode, or DMA receive mode, the program uses this register to output data onto the 16 output lines. In functionality mode, this register may be accessed by a high or low byte. If only the high byte is accessed, the clock signals NEW DATA READY and NEW DATA READY HIGH are pulsed for one microsecond after the data has been put on the output lines. If only the low byte is written to, NEW DATA READY and NEW DATA READY LOW are pulsed for one microsecond after the data has been put on the output lines. If this register is written to as a word, NEW DATA READY, NEW DATA READY HIGH, and NEW DATA READY LOW are all pulsed for one microsecond after the data has been put on the output lines.

In SILO transmit mode, the program uses this register to enter data into the 32-word silo one word at a time. The silo word count register may be accessed to determine the number of words in the silo. In SILO transmit mode, this register must be accessed as a word, entering two bytes into the silo at a time. When the device asserts the user request line to get a word from the silo, the DMF32 pulses NEW DATA READY, NEW DATA READY HIGH, and NEW DATA READY LOW for one microsecond after the data has been put onto the output lines.

In DMA transmit mode, the program uses this register to insert a word onto the output lines between DMA transfers. The program inserting a word onto the output lines between words that have been direct memory accessed is transparent to the user device. It is transparent because the user device does its normal handshake protocol to obtain the data regardless of whether the data has been direct memory accessed from main memory or inserted between direct memory accesses by the program writing to this register. The normal handshake protocol is used when the user device toggles the request line, then the DMF32 applies the data onto the lines and pulses the New Data Ready lines.

The parallel interface output buffer is cleared by either a Master Reset or INIT.

4.14.4.3 Parallel Interface Input Buffer

The parallel interface input buffer has an address of base +1C. This register is read-only.

In either DR11-C functionality mode, SILO transmit mode, or DMA transmit mode, this register reflects the state of the 16 input lines from the user device. The user data should be stable on the input lines before the program reads the parallel interface input buffer. After the program reads the parallel interface input buffer, the DMF32 pulses the Data Transmitted line to inform the user device that the data has been read.

In SILO receive mode, this register is used to access the receive silo. Reading the parallel interface input buffer causes the silo entries to shift down by one word position. The word count register should be read to determine the number of entries remaining in the silo.

In DMA receive mode, this register contains the previous word direct memory accessed to main memory.

A Master Reset or INIT clears the parallel interface input buffer bits ⟨15:0⟩.

4.14.4.4 Miscellaneous Register – The miscellaneous register has an address of base +1C. This write-only register is accessed by word only.

The miscellaneous register indicates the following:

- Specific mode of operation
- Most significant UNIBUS primary buffer address bit (DMA)
- Most significant UNIBUS secondary buffer address bit (DMA)

The miscellaneous register is cleared by a Master Reset or INIT.

Figure 4-28 shows the bit format for the miscellaneous register. Table 4-37 describes the functions for the miscellaneous register.

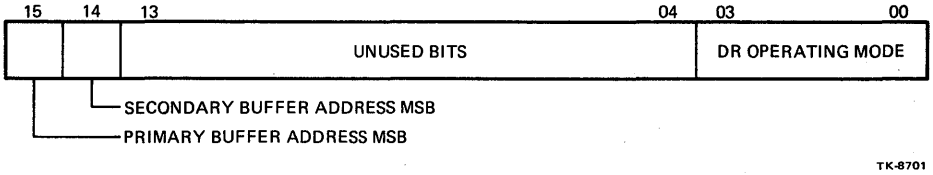

Figure 4-28 Miscellaneous Register

Table 4-37 Parallel Interface Miscellaneous Register Functions

Bits	Title	Function
⟨3:0⟩	DR Operating Mode	Bits ⟨3:0⟩ contain the parallel interface operating mode. The program should write the desired DMF32 parallel interface operating mode to the miscellaneous register bits ⟨3:0⟩. A write to the miscellaneous register should be preceeded by a Master Reset if the operating mode specified in the miscellaneous register bits ⟨3:0⟩ is being changed. After a Master Reset or INIT, the parallel interface is initialized to the DR11-C functional mode (Table 4-38 lists the modes).
⟨13:4⟩	Unused Bits	
⟨14⟩	Secondary Buffer Address MSB	Bit ⟨14⟩ is the most significant UNIBUS secondary buffer address bit, used in the DMA mode.
⟨15⟩	Primary Buffer Address MSB	Bit ⟨15⟩ is the most significant UNIBUS primary buffer address bit, used in the DMA mode.

Table 4-38 Parallel Interface Operating Modes

Bits	⟨3:0⟩	Mode
	0000	DR11-C functional mode
	0101	Silo/transmit, User Request A requests data transfer
	0100	Silo transmit, User Request B requests data transfer
	0111	Silo receive, User Request A requests data transfer
	0110	Silo receive, User Request B requests data transfer
	1001	DMA transmit, User Request A requests data transfer
	1000	DMA transmit, User Request B requests data transfer
	1011	DMA receive, User Request A requests data transfer
	1010	DMA receive, User Request B requests data transfer

4.14.5 Parallel Interface Indirect Registers – The parallel interface indirect registers have an address of base +1E. Read/modify/write UNIBUS cycles are not allowed. This register is accessed by word only.

The parallel interface uses four indirect registers. These registers are addressed by the parallel interface CSR bits ⟨4:3⟩. Table 4-39 describes the functions for the parallel interface indirect registers.

Table 4-39 Parallel Interface Indirect Registers Functions

Indirect Register/Bits	Title	Function
Indirect Register [0] Bits ⟨15:0⟩	Primary Buffer Address Register	This read/write register stores the primary buffer address (UNIBUS address) of the transmit or receive buffer for DMA transfers. The most significant UNIBUS address bit (the seventeenth bit counting from zero) is the primary buffer address bit ⟨17⟩ (miscellaneous register bit ⟨15⟩). Bits ⟨16:1⟩ are stored in the primary buffer address register. Since only word-aligned transfers are permitted, the least significant UNIBUS address bit is assumed to be zero. The primary buffer address register is cleared by a Master Reset or INIT.
Indirect Register [1] Bits ⟨15:0⟩	Primary Word Count Register	In DMA mode, this read/write register is loaded with the primary buffer size in words (receive or transmit). Writing tro this register clears the done primary bit (parallel interface CSR bit ⟨8⟩). In silo mode, (transmit or receive), this read/write register contains the number of word entries in the silo. This register is cleared by a Master Reset or INIT.

Table 4-39 Parallel Interface Indirect Registers Functions (Cont)

Indirect Register/Bits	Title	Function
Indirect Register [2] Bits ⟨15:0⟩	Secondary Buffer Address	This read/write register stores the secondary buffer address (UNIBUS address) of the transmit or receive buffer for DMA transfers. The most significant UNIBUS address bit (the seventeenth bit counting from zero) is secondary buffer address bit ⟨17⟩ (miscellaneous register bit ⟨14⟩). Bits ⟨16:1⟩ are stored in the secondary buffer address register. Since only word-aligned transfers are permitted, the least significant UNIBUS address bit is assumed to be zero. The secondary buffer address register is cleared by a Master Reset or INIT.
Indirect Register [3] Bits ⟨15:0⟩	Secondary Word Count	In DMA mode, this read/write register is loaded with the secondary buffer size in words (receive or transmit). Writing to this register clears the done secondary bit (parallel interface CSR bit ⟨9⟩). This register is cleared by a Master Reset or INIT.

4.15 DIFFERENCES BETWEEN DMF32 AND THE DR11-C

The DMF32 parallel interface is a microcoded implementation; the DR11-C is a hardwired implementation. These two devices are functionally similar, but are not identical. Different implementations result in different signal timings, different register access times, and different data transfer rates. The bandwidth of the DMF32 parallel interface depends upon many factors, such as latency time and the extent to which that other devices on the DMF32 (synchronous interface and asynchronous multiplexer) are used. The more other devices are used, the less the bandwidth of the parallel interface.

The following list specifies the major differences between the DMF32 running in the DR11-C functional mode and the DR11-C.

1. DMF32: The timing of NEW DATA READY, NEW DATA READY HIGH, NEW DATA READY LOW, and DATA TRANSMITTED signals are fixed. These signals are fixed as one microsecond active high pulses. The width of these pulses CANNOT be changed. If a longer pulse is required, then the user's device needs to contain the appropriate circuitry to change the characteristics of the signal. A monostable multivibrator may be used to lengthen the pulse.

   DR11-C: The timing of these signals may be varied by changing a capacitor on the DR11-C module.

2. The DMF32 uses bits in the control and status registers that are not used by the DR11-C. These bits must not be set by software when running in DR11-C functional mode.

3. DMF32: Read/modify/write UNIBUS cycles to any of the parallel interface control and status registers are not permitted. These cycles are not permitted because there is no interlock by the DMF32 in between the read and write part of the cycle. This means that macro instructions such as "bit set" and "bit test" are not permitted. Move instructions are recommended.

   DR11-C: Can perform read/modify/write UNIBUS cycles to some registers.

4. DMF32: Data out byte (DATOB) UNIBUS cycles should not be used to write to a control and status register in any mode, except for the output buffer when in the DR11-C functional mode. Except for the above noted special case, the DMF32 treats a DATOB cycle as DATO cycle and ignores the least significant UNIBUS address bit.

   DR11-C: No restrictions.

5. The DMF32 and DR11-C have the same electrical signals that interface to the user device, but the CONNECTORS AND CONNECTOR PINOUTS ARE DIFFERENT. The DMF32 distribution panel has two 37 pin D type connectors to which the user can connect user supplied cables to connect to the user device.

6. The DMF32 and DR11-C both have TTL compatible logic for the interfacing signals. However, these devices use DIFFERENT types of drivers and receivers. Table 4-40 lists the drivers and receivers that the DMF32 uses.

4.16 DMF32 DRIVERS AND RECEIVERS

Table 4-40 lists the DMF32 drivers/receivers and associated signals. Figure 4-29 shows the drivers and receivers.

Table 4-40 DMF32 Drivers/Receivers and Associated Signals

Driver/Receiver	Associated Signals
7437 driver with 1 kohm pullup resistor to +5 volts on output	New Data Ready New Data Ready High New Data Ready Low Data Transmitted INIT
74S240 driver with 1 kohm pullup resistor to +5 volts on output	Sixteen data output lines
74LS240 driver with 1 kohm pullup resistor to +5 volts on output	Control Zero Control One
74LS240 receiver with 1 kohm pullup resistor to +5 volts on pullup	Sixteen data input lines User Request A User Request B

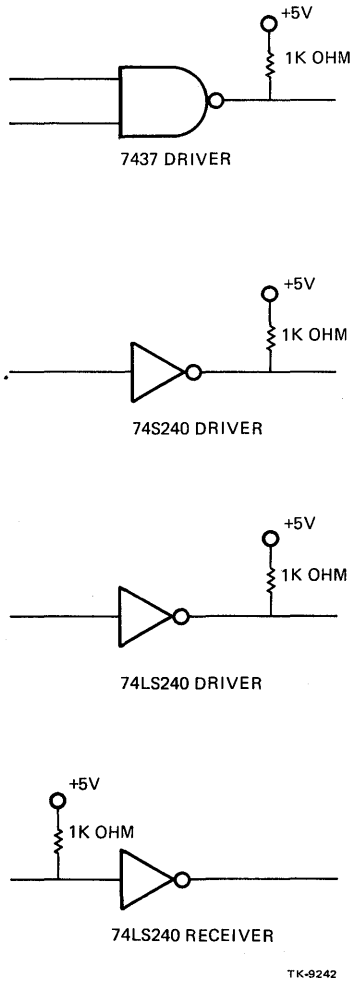

Figure 4-29 DMF32 Drivers and Receivers

Synchronous 25-Pin Cinch Connector

A

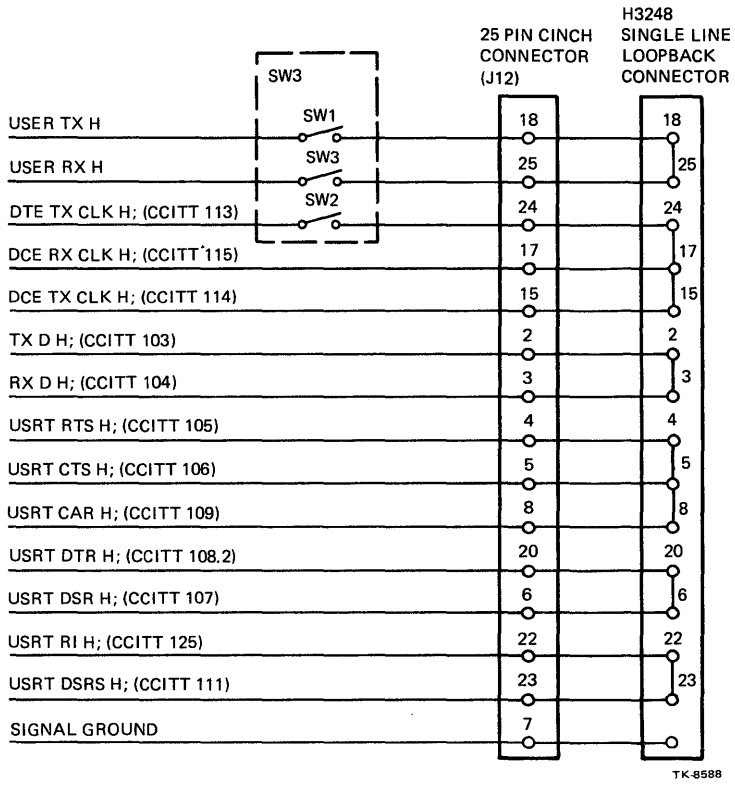

Figure A-1 Synchronous 25 Pin Cinch Connector

Asynchronous 25-Pin Cinch Connector

B

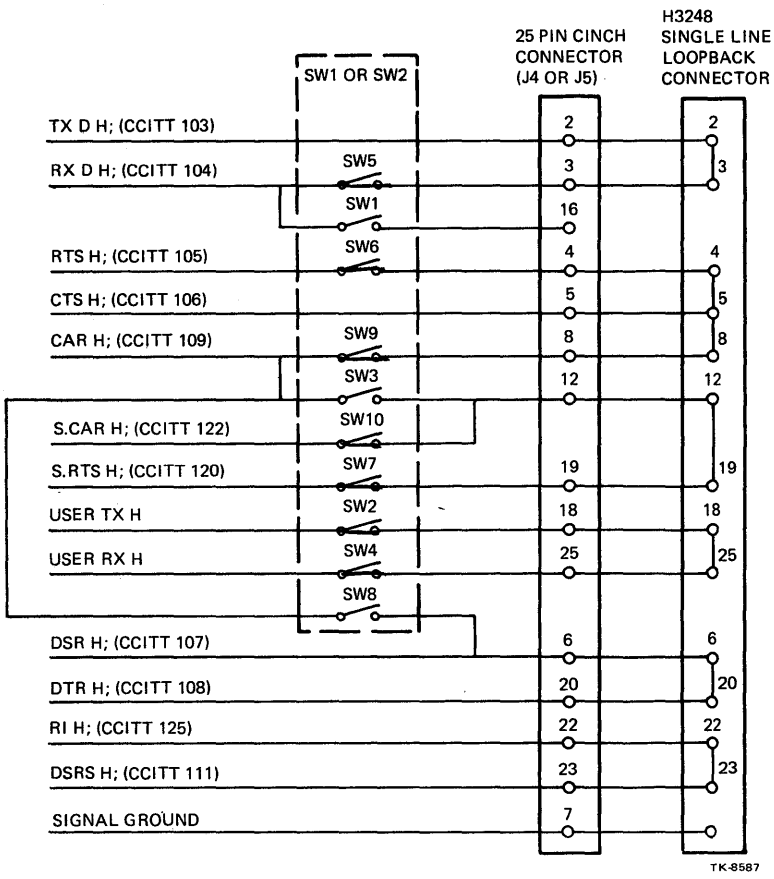

Figure B-1 Asynchronous 25 Pin Cinch Connector

Parallel Interface/Line Printer Signals

C

Table C-1 Parallel Interface/Line Printer Signals

Signal Name Number	Connector/Pin
J3 TX DR/LP⟨0⟩ L (printer data ⟨1⟩)	J14-26
J3 TX DR/LP⟨1⟩ L (printer data ⟨2⟩)	J14-20
J3 TX DR/LP⟨2⟩ L (printer data ⟨3⟩)	J14-22
J3 TX DR/LP⟨3⟩ L (printer data ⟨4⟩)	J14-1
J3 TX DR/LP⟨4⟩ L (printer data ⟨5⟩)	J14-24
J3 TX DR/LP⟨5⟩ L (printer data ⟨6⟩)	J14-23
J3 TX DR/LP⟨6⟩ L (printer data ⟨7⟩)	J14-5
J3 TX DR/LP⟨7⟩ L (printer data ⟨8⟩)	J14-6
J3 TX DR/LP⟨8⟩ L (printer spare)	J14-3
J3 TX DR/LP⟨9⟩ L (printer spare)	J14-21
J3 TX DR/LP⟨10⟩ L (printer spare)	J14-25
J3 TX DR/LP⟨11⟩ L (printer spare)	J14-7
J3 TX DR/LP⟨12⟩ L (printer spare)	J14-36
J3 TX DR/LP⟨13⟩ L (printer spare)	J14-2
J3 TX DR/LP⟨14⟩ L (printer strobe)	J14-37
J3 TX DR/LP⟨15⟩ L	J14-8
J3 RX DR REQ A H	J14-13
J3 TX DR N.D.R. LO H	J14-10
J3 TX DR N.D.R. HI H	J14-9
J3 TX DR N.D.R. H	J14-4
J3 TX DR REQ B H	J13-22
J3 TX DR DATA XMTD H	J13-13
J3 RX DR/LP⟨15⟩ H	J13-20
J3 RX DR/LP⟨14⟩ H (printer on-line)	J13-9/J14-12
J3 RX DR/LP⟨13⟩ H	J13-1
J3 RX DR/LP⟨12⟩ H	J13-21
J3 RX DR/LP⟨11⟩ H	J13-4
J3 RX DR/LP⟨10⟩ H	J13-2
J3 RX DR/LP⟨9⟩ H	J13-6
J3 RX DR/LP⟨8⟩ H	J13-3
J3 RX DR/LP⟨7⟩ H (printer demand)	J13-16/J14-18
J3 RX DR/LP⟨6⟩ H (printer DAVFU RDY)	J13-14/J14-17
J3 RX DR/LP⟨5⟩ H	J13-8
J3 RX DR/LP⟨4⟩ H (printer conn VFY)	J13-18/J14-14
J3 RX DR/LP⟨3⟩ H	J13-10
J3 RX DR/LP⟨2⟩ H	J13-11
J3 RX DR/LP⟨1⟩ H (printer spare)	J13-5/J14-11
J3 RX DR/LP⟨0⟩ H (printer spare)	J13-17/J14-19
J2 TX DR CTRL ZERO L	J13-7
J2 TX DR INIT L	J13-19/J14-15
J2 TX DR CTRL ONE L	J14-16

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