VAX 9000 Family
Clock Subsystem Technical Description

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DIGITAL INTERNAL USE ONLY

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About This Manual

This manual describes clock generation and distribution for the VAX 9000 family processors. It supplies technical information to support clock subsystem maintenance and maintenance training.

This manual is a reference manual for Customer Services personnel as well as a training resource for Educational Services.

Intended Audience

The content, scope, and level of detail in this manual assumes that the reader:

- Is familiar with the VAX architecture and VMS operating system at the user level
- Has experience maintaining midrange and large VAX systems

Manual Structure

This manual has four chapters and an index.

- Chapter 1, Overview, describes the clock signals and timing.
- Chapter 2, MCM Functional Description, describes the master clock module, clock generation, distribution, and control.
- Chapter 3, CDXX Description, describes clock distribution and regeneration in the MCUs.
- Chapter 4, Clock Subsystem Physical Description, describes the physical characteristics of the clock subsystem components.

Manual Conventions

This manual uses the following signal name and state conventions.

Signal Name Word Separators

Underscores (_) are used as word separators in multiword signal names in most engineering prints and in command line arguments, for example: CLK_CNTL_CPU0.

For clarity and easier reading, spaces are used as word separators in this manual, for example: CLK CNTL CPU0.

Signal State Indicators

In most cases, functional descriptions that require the high or low state of a signal be specified are beyond the scope of this manual. Therefore, H and L state indicators are omitted, except where necessary for clarity.

1
Overview

This chapter describes the major clock signals, distribution, and timing. Figure 1–1 shows the master clock module (MCM) assembly. Figure 1–2 shows the major signals and components of the clock subsystem. Figure 1–3 shows clock signal distribution in a CPU. Figures 1–4 and 1–5 show clock timing.

1.1 Clock Signal Overview

The master clock module (Figure 1–1) generates and distributes clock and clock control signals to the rest of the system (Figure 1–2). Sections 1.1.1 through 1.1.7 describe the seven major clock signals. Of these, the three primary signals are the master clock, reference clock, and clock control. All other clocks, except the service processor unit (SPU) clocks, are derived from these three signals.

1.1.1 Master Clock

The master clock (MCLK) is sinusoidal and its frequency is programmable between 340 MHz and 580 MHz. All system timing is referenced to the rising edge of the master clock.

1.1.2 Reference Clock

The reference clock (RCLK) is a square wave and its frequency is one-eighth of the master clock frequency. The reference clock defines a *machine cycle;* that is, each cycle of the reference clock is a machine cycle.

1.1.3 Clock Control

The clock control signal (CLK CNTL) enables or disables clocks continuously in bursts or at intervals.

1.1.4 XJA Clocks

The MCM also generates phase-shifted reference clocks to compensate for data and clock transmission time differences between the system control unit (SCU) and JXDI bus to the XJA (Section 1.3.7).

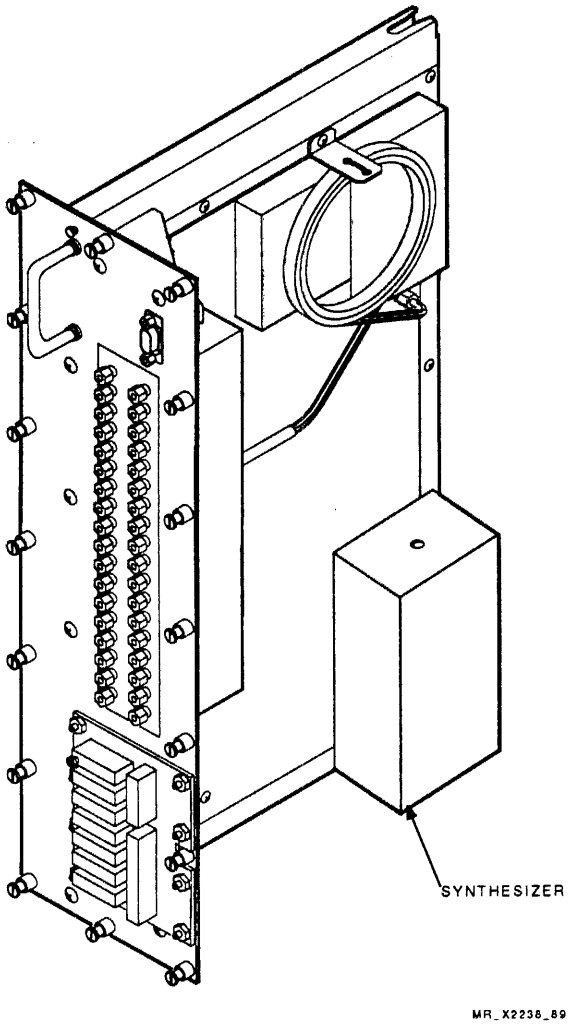


Figure 1–1 MCM Assembly

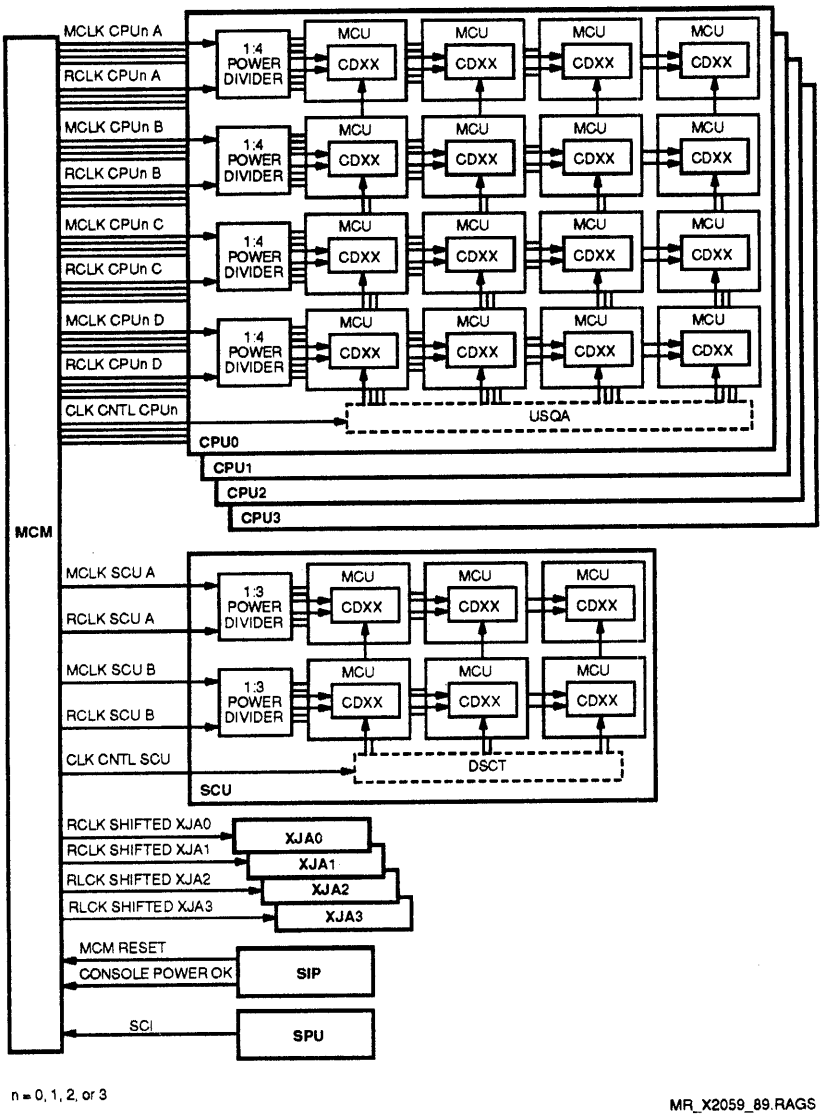


Figure 1–2 Clock Subsystem

1.1.5 STRAM Clocks

A clock distribution chip (CDXX, Chapter 3) in every multichip unit (MCU) uses master and reference clocks to generate programmable, eight-phase clocks for timing self-timed RAMs (STRAMs) on the MCUs (Figure 1–3).

NOTE
The CDXX also provides the interface between the macrocell arrays (MCAs) on a high density signal carrier (HDSC) and the scan control module (SCM) in the service processor unit (SPU). See Chapter 3 for a description of the CDXX scan functions.

1.1.6 Phase A and B Clocks

In all the gate arrays, master and reference clocks conditioned by the CDXX are used to form two-phase, nonoverlapping A and B clocks. The timing of these clocks is designed to prevent race conditions when data is transferred between latches in A and B latch pairs.

1.1.7 SPU Clocks

The SPU clocks are exceptions because these clocks are not derived from MCM clocks. The SPU generates its own clocks. Synchronization between SPU and MCM timing is performed in the clock control interface (CCI, Section 2.1).

NOTE
Many of the clock subsystem signals are distributed as differential pairs (that is, complementary high and low signals) to improve transmission characteristics.

1.2 Clock Signal Distribution

Figure 1–2 shows clock signal distribution in a quad CPU system. Note that any VAX 9000 configuration includes only one MCM.

The MCM distributes copies of the master clock, reference clock, and clock control as follows:

Clock	Number of Copies
MCLK	Four to each CPU Two to SCU
RCLK	Four to each CPU Two to SCU
RCLK SHIFTED XJA	One to each XJA (differential)
CLK CNTL	One to each CPU (differential) One to SCU (differential)

1.2.1 CPU and SCU Clocks

The master and reference clocks in a CPU and the SCU are fanned out through 1:4 and 1:3 power dividers to a CDXX in every MCU (Figure 1–2).

NOTE
The 1:3 power dividers are 1:4 power dividers with one output terminated in the power divider assembly.

In a CPU, clock control fans out to a maximum of 16 CDXXs through the USQA MCA in the INT MCU; and in the SCU, clock control fans out to four or six CDXXs through the DSCT MCA in the CCU MCU.

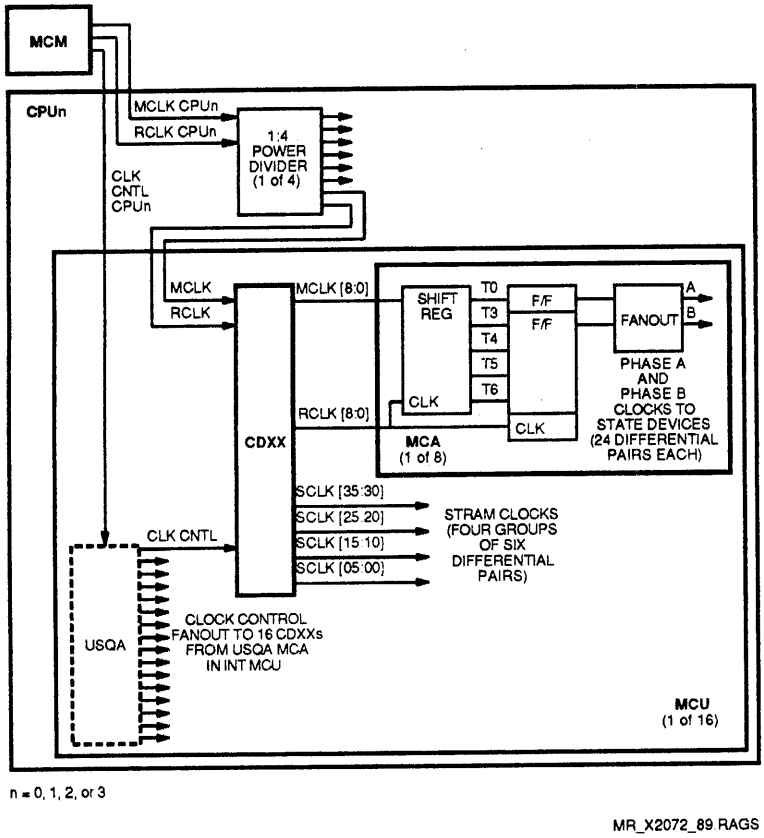


Figure 1–3 Clock Distribution in a CPU

Each CDXX (Figure 1–3) generates nine copies of the master and reference clocks (MCLK8 through MCLK0 and RCLK8 through RCLK0). MCLK0 and RCLK0 are test copies; the other copies of each clock are sent to the eight MCAs on the HDSC. Additionally, the CDXX uses the master and reference clocks to generate 24 copies of the STRAM clocks (SCLK35 through SCLK30, SCLK25 through SCLK20, SCLK15 through SCLK10, and SCLK05 through SCLK00).

On every MCA, the master and reference clocks are used to generate the nonoverlapping phase A and B clocks (also called on-gate-array clocks). Each MCA generates 24 copies of the phase A and B clocks for the state devices in the MCA.

Unlike CPU and SCU clocks, the phase-shifted XJA reference clocks are not conditioned or regenerated by a clock distribution gate array.

Figure 1–4 shows the relationship between these clock signals.

1.3 Timing Overview

A machine cycle is defined as the period from one rising edge of RCLK to the next rising edge of RCLK. In other words, a machine cycle consists of eight rising edges of the master clock. Figure 1–4 shows basic system timing.

NOTE
Unless stated differently, waveforms are shown only to clarify descriptions and do not represent measured waveforms.

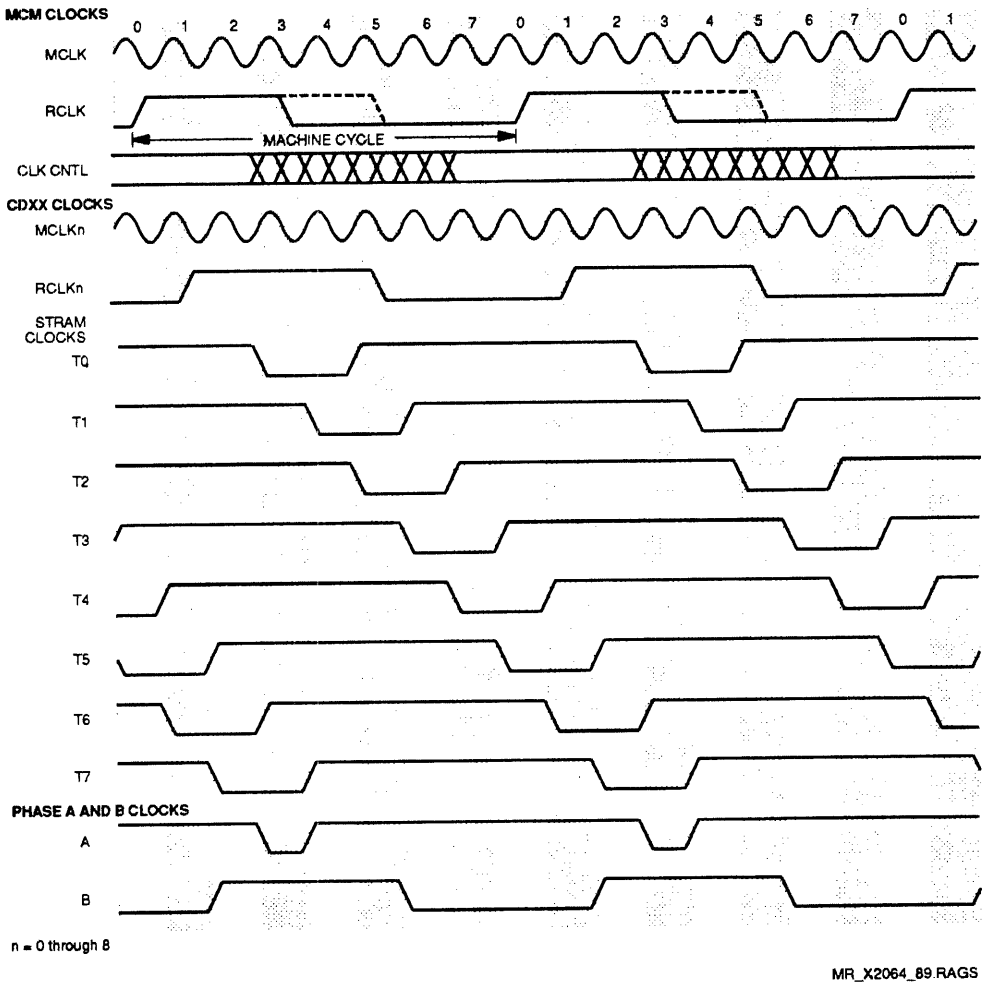


Figure 1–4 Basic Clock Relationships

1.3.1 Master Clock

The sinusoidal master clock is generated by a phase-locked, voltage-controlled oscillator in the MCM (Section 2.2.1). Its frequency can be varied in 4-MHz increments from 340 MHz (2.941 ns period) to 580 MHz (1.724 ns period). It runs continuously after the system is powered up.

1.3.2 Reference Clock

In the MCM, the master clock is divided by eight to produce the square-wave reference clock. The reference clock frequency range is from 42.5 MHz (23.529 ns period) to 72.5 MHz (13.793 ns period). The reference clock pulse is asserted for three-eighths to five-eighths of a machine cycle; that is, for three to five master clock cycles. It runs continuously after the system is powered up.

1.3.3 Clock Control

Clock control signals are generated by the clock control interface (CCI) in the MCM (Section 2.1). Separate clock control signals are sent to each CPU and the SCU. Each clock control signal independently enables and disables clocks during the current machine cycle to perform the following functions:

- Stop clocks.
- Run clocks on every machine cycle (normal operation).
- Run clocks for a burst of machine cycles.
- Run clocks for a burst of machine cycles at intervals.
- Run clocks at intervals.

1.3.4 Gated Reference Clock

The CDXX uses the master clock to change the reference clock's duty cycle to 50%; that is, this gated reference clock is asserted for one-half of a machine cycle (unlike the ungated reference clock that is asserted for three-eighths to five-eighths of a machine cycle). Clock control enables/disables the gated reference clock for the current machine cycle, which controls generation of phase A and B clocks in the MCAs (Figure 1–3).

1.3.5 STRAM Clocks

The CDXX generates selectable, eight-phase STRAM clocks for every MCA on the HDSC. Each STRAM clock phase starts on a different eighth of a machine cycle. One phase is selected, multiplexed, and fanned out into 24 copies of the STRAM clock. All STRAM clocks are asserted for one-fourth of a machine cycle.

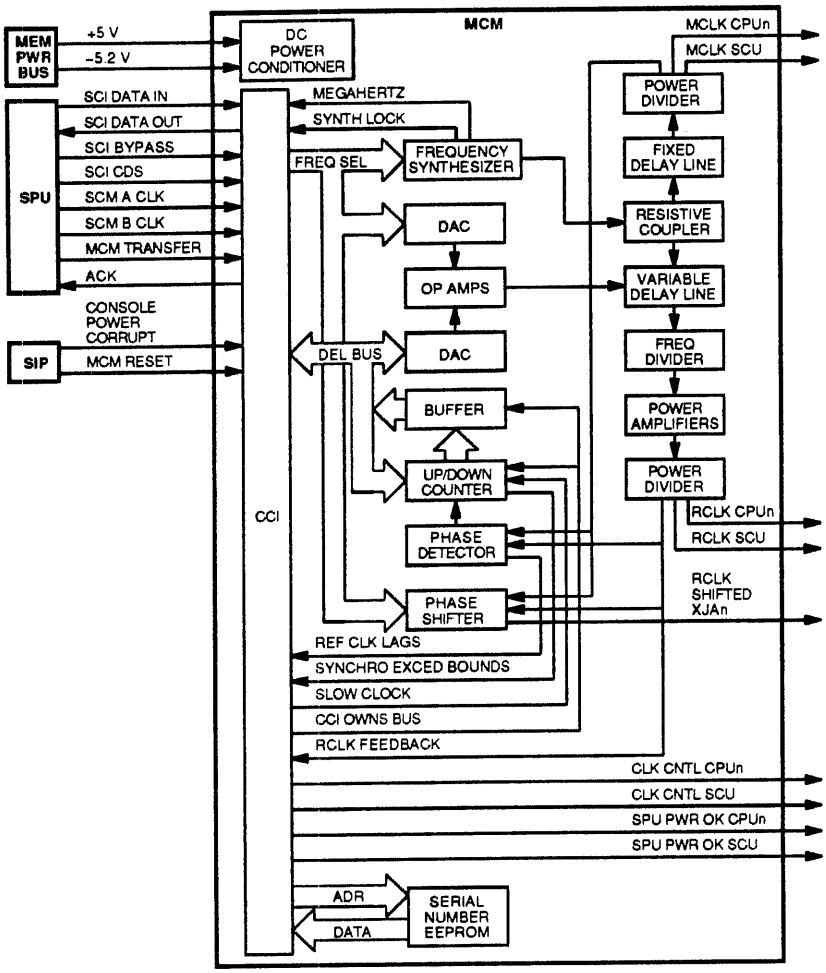
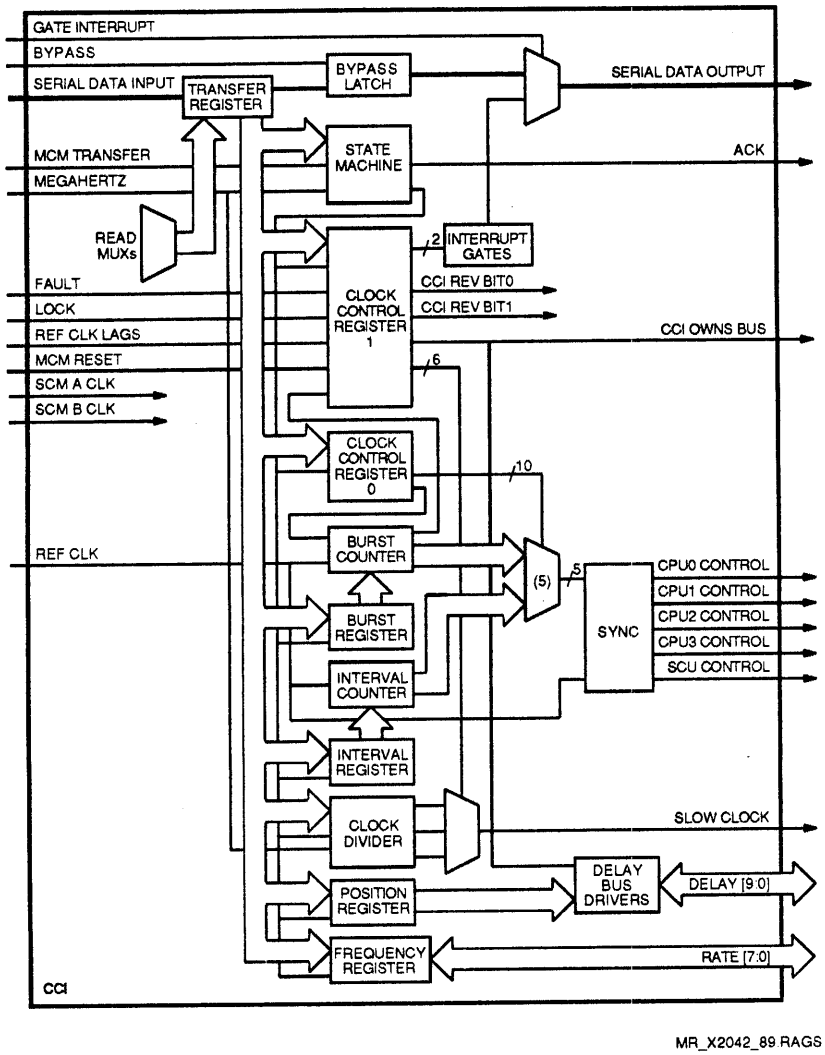


Figure 2–1 MCM Block Diagram



MR_X2042_89.RAGS

Figure 2–2 CCI Block Diagram

2.1.1 Transfer Register

Data is transferred between the console and MCM through the 20-bit transfer register in the CCI (Figure 2–3 and Table 2–1).

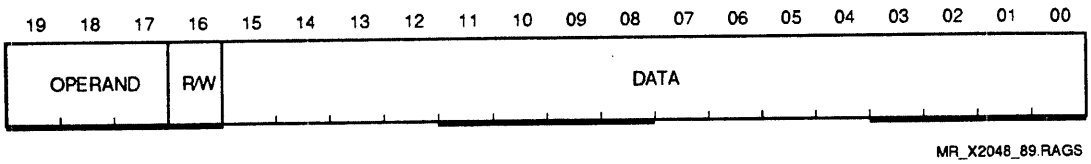


Figure 2–3 CCI Transfer Register Format

Table 2–1 CCI Transfer Register Bit Description

Bits	Name	Description
19:17	Operand	Contains the address of one of the following CCI locations: **Value** **Location** 000 MCM0 — Clock control register 0 001 MCM1 — Frequency register 010 MCM2 — Burst register 011 MCM3 — Interval register 100 MCM4 — Clock control register 1 101 MCM5 — Position register 110 MCM6 — EEPROM 111 MCM7 — Clock divider/external position
16	R/W	Read or write selected location, as follows: **Value** **Operation** 0 Read 1 Write
15:00	Data	Addressed location's read or write data. All 16 bits are not used in all locations, but the transfer register must be fully loaded for a successful data transfer.

2.1.1.1 Transfer Register Write and Read Data Paths

Figures 2–4 and 2–5 show simplified CCI location write and read data paths. Console serial data is loaded into the transfer register through bit [19]. When the register is full, the CCI transfers data in parallel between the transfer register's 16-bit data field (bits [15:00]) and one of eight CCI locations. The transfer register's 3-bit operand field (bits [19:17]) contains the CCI location address; the read or write bit (bit [16]) determines the transfer direction. Serial read data returns to the console through transfer register bit [00].

Note that:

- Not all locations accessed through the transfer register are registers.
- Not all bits of all registers allow full read and write access.
- The format of read data is not the same as the format of write data.

For write operations, the state machine converts the values of the operand and read/write (R/W) fields into a load signal for the specified location, except a write to EEPROM is a "no-op" (location MCM6, Section 2.1.10).

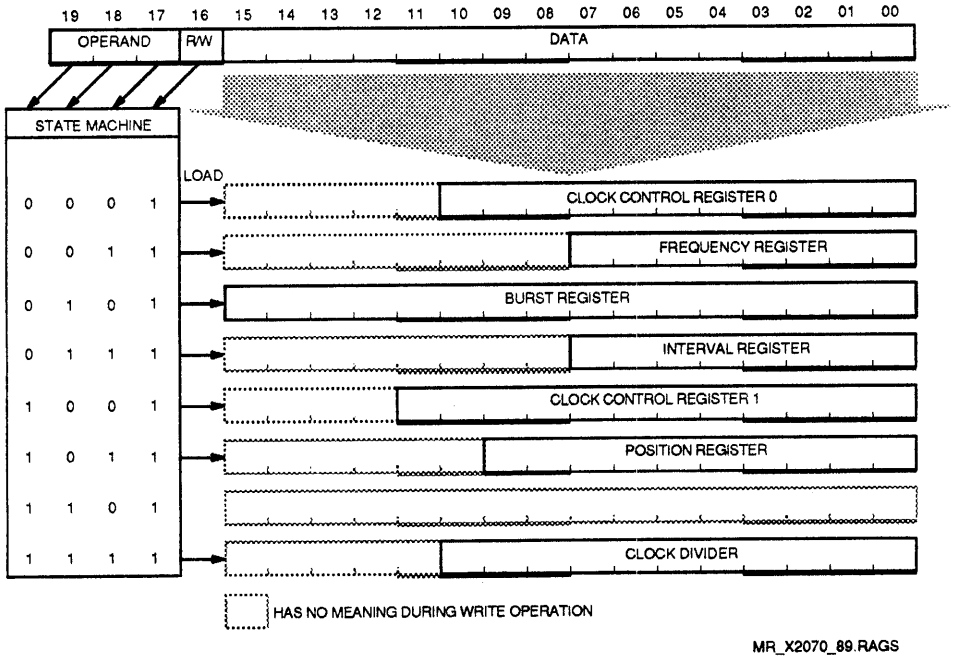


Figure 2–4 CCI Transfer Register Write Data Format

For read operations, the state machine converts the value of the operand field into read multiplexer select signals and the value of the read/write field into a parallel load signal for the transfer register.

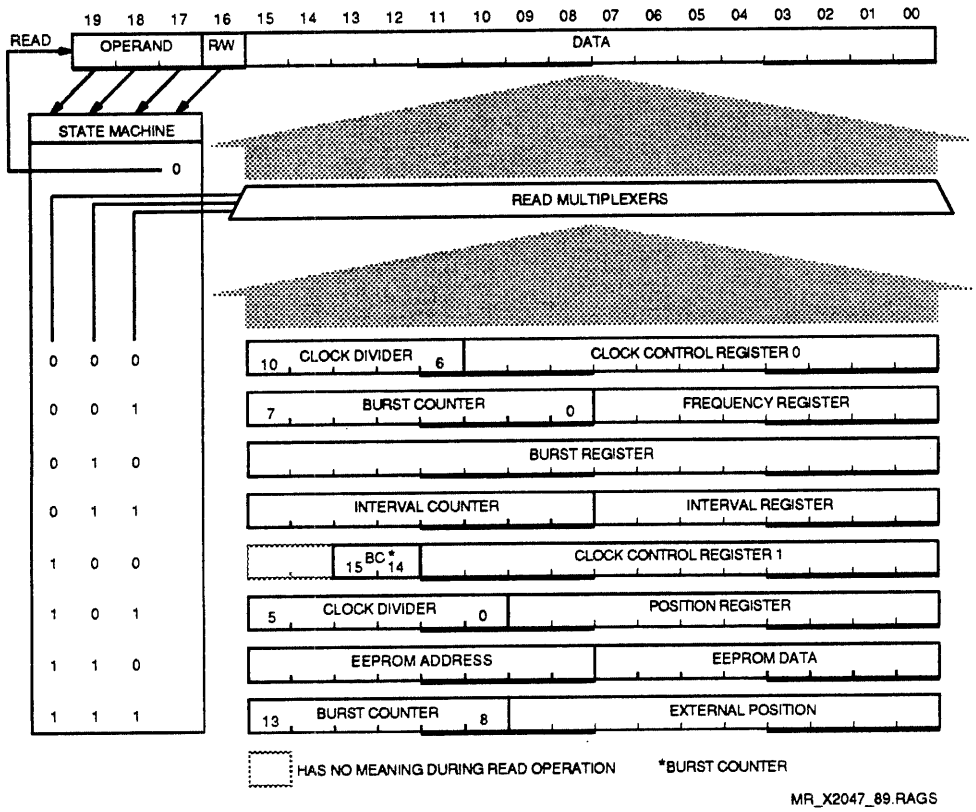


Figure 2–5 CCI Transfer Register Read Data Format

2.1.1.2 Console to MCM Data Transfer Protocol

Data is transferred between the MCM and console through the CCI transfer register, according to the following protocol (see Figure 2–7 for timing):

1. The console loads transfer register [19:00] and asserts MCM TRANSFER.
2. When MCM TRANSFER is asserted, the CCI writes or reads according to transfer register bit [16], the location coded in transfer register bits [19:17].
3. After the operation is completed, the CCI asserts ACKNOWLEDGE.
4. When ACKNOWLEDGE is asserted, the console deasserts MCM TRANSFER.
5. When MCM TRANSFER is deasserted, the CCI deasserts ACKNOWLEDGE. The CCI is now ready for another console command.

2.1.1.3 Transfer Register Operation

Figure 2–6 shows the logic for several transfer register bits. Each bit is implemented with a multiplexer and A and B latches, and transfers data in serial or parallel modes. (This is essentially the same implementation used for the scan rings described in Section 3.2.3.)

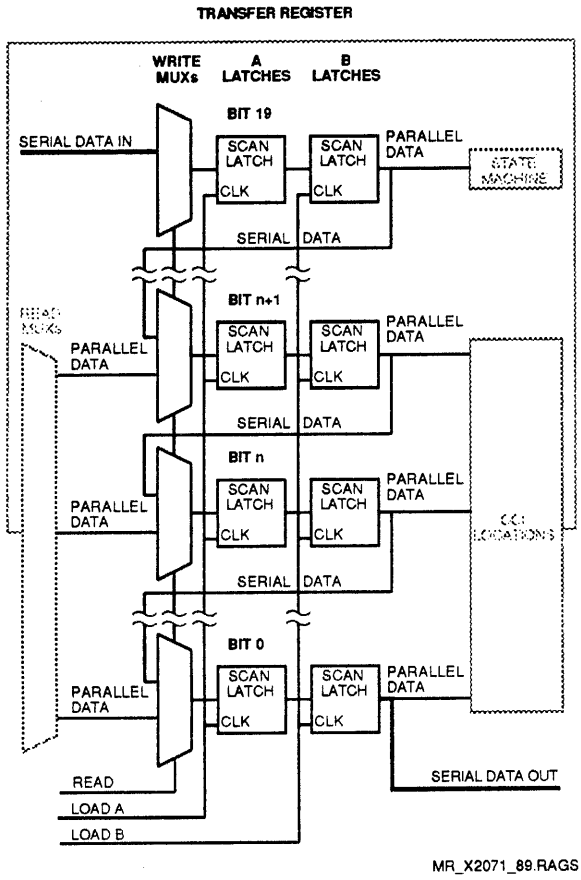


Figure 2–6 CCI Transfer Register Implementation

When transferring data to or from the console, the transfer register is in serial mode, and the serial data multiplexer input is selected (READ is not asserted). Serial data is clocked through the register by LOAD A and LOAD B clocks. At this time the LOAD A and LOAD B clocks are derived from the nonoverlapping, 1-MHz scan clocks from the SPU, SCM A CLK, and SCM B CLK.

When the transfer is complete, the console asserts MCM TRANSFER. MCM TRANSFER is synchronized with the 1-MHz clock (MEGAHERTZ) from the frequency synthesizer to form SYNCHED XFER (Figure 2–7). During the time that SYNCHED XFER is asserted, SCM A CLK and SCM B CLK are disabled and the console cannot change the contents of the transfer register. The CCI is ready to perform the operation indicated in transfer register bits [19:16].

When transferring data to or from a CCI location, the transfer register is in parallel mode. For write operations, the state machine decodes transfer register bits [19:17] and [16] into a specific CCI location load signal, and the location is written from transfer register bits [15:00]. For read operations, the state machine decodes transfer register bits [19:17] and [16] into a read multiplexer select signal and asserts READ. The selected location's data is clocked into the transfer register, in parallel, by the LOAD A and LOAD B clocks. At this time, the LOAD A clock is derived from the READ signal while the 1-MHz clock (MEGAHERTZ) is deasserted. Shortly after the A latch is loaded, the CCI asserts ACKNOWLEDGE. The LOAD B clock is derived from ACKNOWLEDGE while the 1-MHz clock is deasserted.

When ACKNOWLEDGE is asserted, the console deasserts MCM TRANSFER. The CCI then deasserts ACKNOWLEDGE. SCM A CLK and SCM B CLK are enabled, and the CCI is ready for the next transfer from the console.

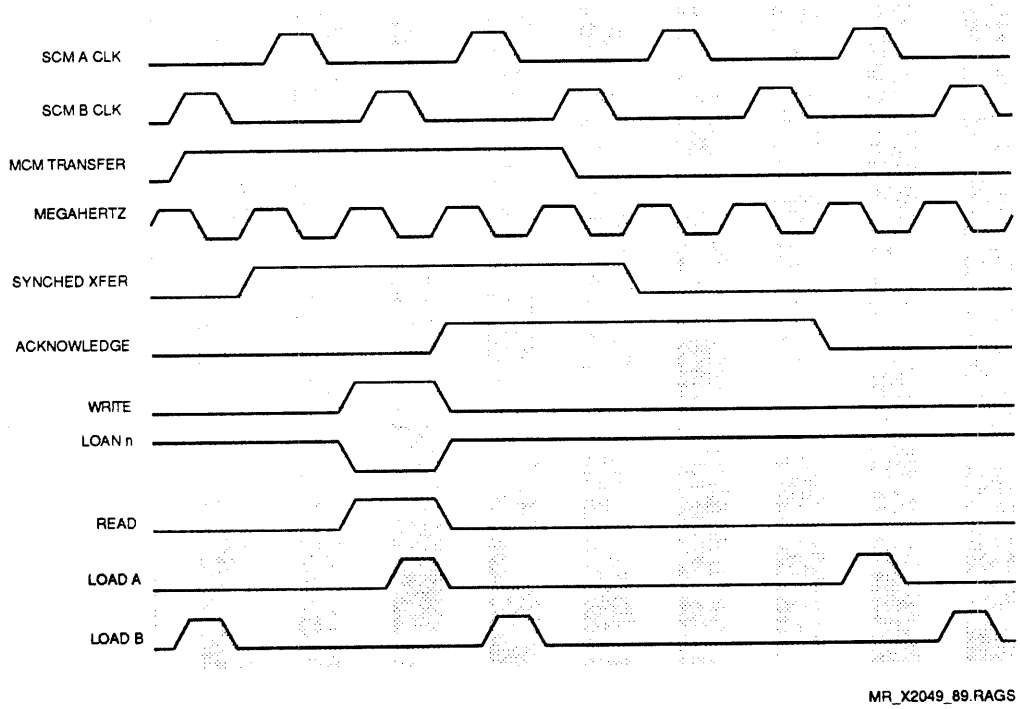


Figure 2–7 CCI Transfer Register Timing

2.1.2 Clock Control Register 0 (MCM0)

Clock control register 0 (CCR0) is an 11-bit register (Figure 2–8 and Table 2–2). Bits [09:00] make up five 2-bit fields that select the CPU and SPU clock modes, and bit [10] enables burst counter loading.

To ensure system-wide clock control signal synchronization, CCR0 is loaded in synchronization with the reference clock. (Other CCI locations are loaded in synchronization with the 1-MHz clock.)

The console can read and write all clock control register 0 bits. When CCR0 is read, five bits of the clock divider value are also read into transfer register (Figure 2–5), as follows:

Transfer register bits [15:11] = Clock divider bits [10:06]
Transfer register bits [10:00] = CCR0 bits [10:00]

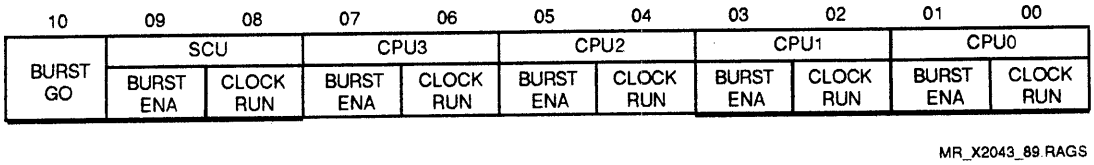


Figure 2–8 CCI Clock Control Register 0 Format

Table 2–2 CCI Clock Control Register 0 Bit Description

Bits	Name	Description
10	Burst go	Enables burst counter parallel load. When this bit is asserted and the value of the burst counter is zero, the contents of the burst register are transferred to the burst counter. As soon as the burst counter is loaded, this bit is cleared. This bit is cleared at power-up.
09:08	SCU burst enable SCU clock run	Each of these five 2-bit burst enable/clock run fields determines clock mode for the CPUs and SCU as follows: **Value** **Mode** 00 Stop clocks (the value at power-up). 01 Run clocks (normal operation). 10 Burst clocks. Burst clocks on intervals. 11 Run clocks on intervals. See Section 2.1.12 for more information on clock modes.
07:06	CPU3 burst enable CPU3 clock run	
05:04	CPU2 burst enable CPU2 clock run	
03:02	CPU1 burst enable CPU1 clock run	
01:00	CPU0 burst enable CPU0 clock run	

2.1.3 Frequency Register (MCM1)

The 8-bit frequency register controls the frequency select lines to the frequency synthesizer and phase shifter (Figure 2–9 and Table 2–3).

The master clock frequency is set to four times the value of this register. Incrementing or decrementing the value changes the master clock frequency in 4-MHz steps. The range of register values is from 85_{10} (53_{16}) to 145_{10} (91_{16}) and is equivalent to a frequency range from 340 MHz to 580 MHz. The register's power-up value is 88_{10} (58_{16}), making the master clock frequency 352 MHz at power-up.

The console can read and write all frequency register bits. When the frequency register is read, eight bits of the burst counter value are also read into the transfer register (Figure 2–5), as follows:

Transfer register bits [15:08] = Burst counter bits [07:00]
Transfer register bits [07:00] = Frequency register bits [07:00]

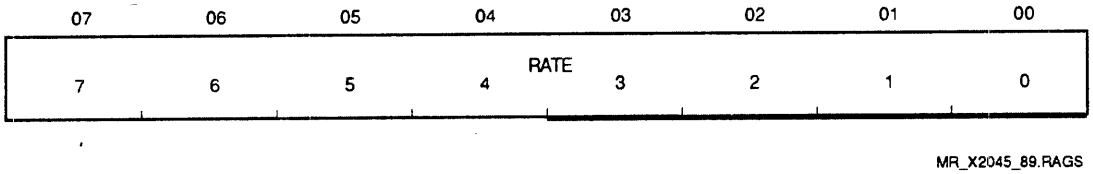


Figure 2–9 CCI Frequency Register Format

Table 2–3 CCI Frequency Register Bit Description

Bits	Name	Description
07:00	Rate [7:0]	One-fourth the decimal value of the master clock frequency.

2.1.4 Burst Register (MCM2)

The 16-bit burst register value is loaded into the burst counter (Figure 2–10, Table 2–4, and Section 2.1.5). The register value is unchanged until the register is reloaded. The register is not automatically cleared at power-up; a known value must be loaded into the register.

The console can read and write all burst register bits.

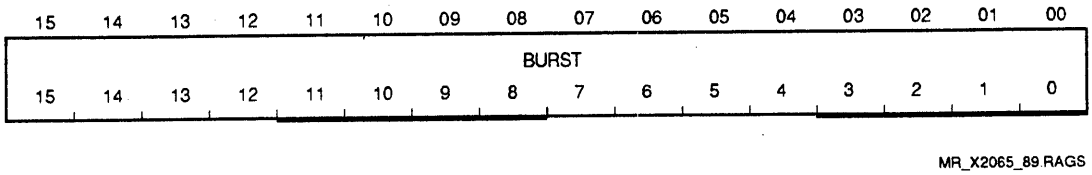


Figure 2–10 CCI Burst Register Format

Table 2–4 CCI Burst Register Bit Description

Bits	Name	Description
15:00	Burst register [15:0]	Specifies the number of machine cycles for which a CPU or the SCU runs. It is loaded into the burst counter.

2.1.5 Burst Counter

The 16-bit burst counter counts down the number of machine cycles for which clocks are enabled. The counter is loaded from the burst register (Section 2.1.4) when the count is zero and burst go (CCR0 bit [10]) is asserted.

The count is decremented every machine cycle when the value of the interval counter is zero. When the burst count reaches zero, the burst halt interrupt is set (CCR1 bit [05]). Section 2.1.12 describes clock modes, including burst clocks and burst clocks on interval.

The counter is reset at power-up by MCM RESET. The console cannot write to the burst counter and cannot read it directly. When the following three locations are read, the contents of the burst counter are also read into the transfer register (Figure 2–5):

Read frequency register (MCM1)

Transfer register bits [15:08] = Burst counter bits [07:00]
Transfer register bits [07:00] = Frequency register bits [07:00]

Read clock control register 1 (MCM4)

Transfer register bits [15:14] are unused
Transfer register bits [13:12] = Burst counter bits [15:14]
Transfer register bits [11:00] = CCR1 bits [11:00]

Read external position (MCM7)

Transfer register bits [15:10] = Burst counter bits [13:08]
Transfer register bits [09:00] = External position bits [09:00]

2.1.6 Interval Register (MCM3)

The 8-bit interval register value is loaded into the interval counter (Figure 2–11, Table 2–5, and Section 2.1.7). The register value is unchanged until the register is reloaded. The register is not automatically cleared at power-up; a known value must be loaded into the register.

The console can read and write all interval register bits. When the interval register is read, the interval counter value is also read into the transfer register (Figure 2–5), as follows:

Transfer register bits [15:08] = Interval counter bits [07:00]
Transfer register bits [07:00] = Interval register bits [07:00]

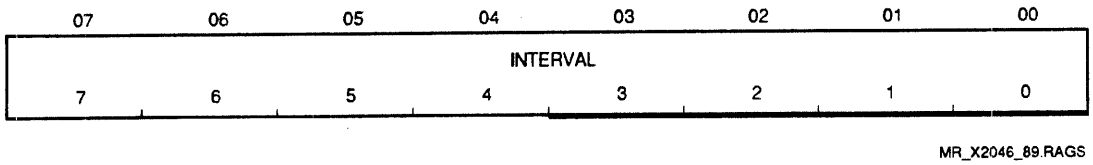


Figure 2–11 CCI Interval Register Format

Table 2–5 CCI Interval Register Bit Description

Bits	Name	Description
07:00	Interval register [7:0]	Specifies the number of machine cycles for which a CPU or the SCU does *not* run. It is loaded into the interval counter.

2.1.7 Interval Counter

The 8-bit interval counter counts down the number of machine cycles for which clocks are disabled. When the count reaches zero, the counter is reloaded from the interval register (Section 2.1.6).

The count is decremented every machine cycle. When the count reaches zero, the burst counter is enabled to count down, clocks are enabled for one machine cycle, and the interval counter is reloaded from the interval counter. Section 2.1.12 describes clock modes, including clock on interval and burst clocks on interval.

The counter is reset at power-up by MCM RESET. The console cannot write to the interval counter and cannot read it directly. When the console reads the interval register, the interval counter value is also read into the transfer register (Figure 2–5), as follows:

Transfer register bits [15:08] = Interval counter bits [07:00]
Transfer register bits [07:00] = Interval register bits [07:00]

2.1.8 Clock Control Register 1 (MCM4)

Clock control register 1 (CCR1) is a 12-bit multipurpose control and status register (Figure 2–12). As noted in Table 2–6, the console has the following access to the register's bits:

Read/write: Bits [09:07, 04, 02, 00]
Read/clear: Bits [05, 03, 01]
Read-only: bits [11:10, 06]

When the console reads CCR1, two bits of the burst counter value are also read into the transfer register (Figure 2–5), as follows:

Transfer register bits [13:12] = Burst counter bits [15:14]
Transfer register bits [11:00] = CCR1 bits [11:00]

Transfer register bits [15:14] are unused.

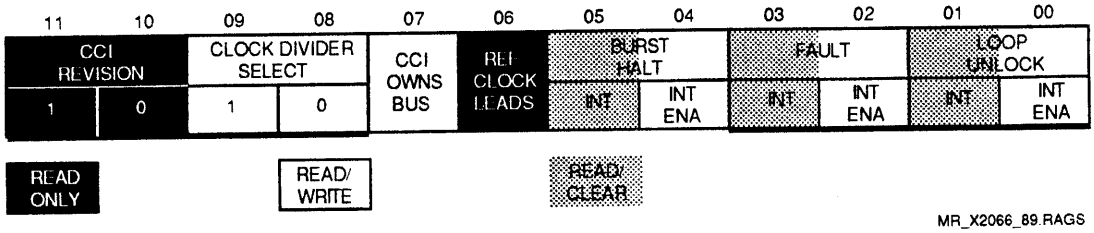


Figure 2–12 CCI Clock Control Register 1 Format

Table 2–6 CCI Clock Control Register 1 Bit Description

Bits	Name	Description
11:10	CCI revision [1:0]	Read-only. The binary revision number of the CCI gate array, where 00 = pass 1 of the gate array, 01 = pass 2, and so on.
09:08	Clock divider select [1:0]	Controls a multiplexer to select inputs from the clock divider register and control the slow clock, as follows: **Value** **Action** 00 Stop slow clock (power-up value). 01 Divide 1 MHz by 2048 (488 Hz). 10 Divide 1 MHz by 1024 (976 Hz). 11 Divide 1 MHz by 512 (1095 Hz).
07	CCI owns bus	Determines whether the delay bus is written or read, as follows: **Value** **Operation** 0 The value in the position register is written to the delay bus. 1 The value on the delay bus is input to the CCI read multiplexers. This bit is set at power-up.

Table 2–6 (Cont.) CCI Clock Control Register 1 Bit Description

Bits	Name	Description
06	Reference clock leads	Indicates the position of the rising edge of the reference clock with respect to the rising edge of the master clock, as follows: **Value** **Position** 0 Reference clock rising edge occurs before master clock rising edge (RCLK leads MCLK). 1 Reference clock rising edge occurs after master clock rising edge (RCLK lags MCLK).
05	Burst halt interrupt	When set, indicates that the burst counter has counted down to zero. This bit is cleared at power-up. The console can read and clear, but not write, this bit.
04	Burst halt interrupt enable	When set, enables burst halt interrupts to the gated interrupt logic.[1] At power-up, this bit is cleared, disabling the interrupt.
03	Fault interrupt	The MCM sets this bit to indicate that the time between the leading edges of the master and reference clocks is out of bounds; that is, the up/down counter has detected a synchronization error condition and asserts SYNCHRO EXCED BOUNDS. When the two clocks are within synchronization limits, this bit is zero. The console can read and clear, but not write, this bit.
02	Fault interrupt enable	When set, enables fault interrupts to the gated interrupt logic.[1] At power-up, this bit is cleared, disabling the interrupt.
01	Loop unlocked interrupt	The MCM sets this bit to indicate that the frequency synthesizer's programmable phase-locked loop is unlocked (the likely power-up condition). When the phase-locked loop is locked, this bit is zero. The console can read and clear, but not write, this bit.
00	Loop unlocked interrupt enable	When set, enables loop unlocked interrupts to the gated interrupt logic.[1] At power-up, this bit is cleared, disabling the interrupt.

[1]The console receives enabled interrupts only when GATE INTERRUPT is asserted.

2.1.9 Position Register (MCM5)

The 10-bit position register (Figure 2–13 and Table 2–7) value drives the delay bus to control the variable delay line in the MCM. The variable delay line determines the position of the positive transition of the reference clock with respect to the positive transition of the master clock, over the frequency range of the master clock.

The console can read and write all position register bits. The register value is not loaded on the delay bus until CCI OWNS BUS is asserted (CCR1 bit [07] is cleared).

When the console reads this location, the state of CCI OWNS BUS determines what value is read into the transfer register:

- If CCI OWNS BUS is asserted (CCR1 bit [07] is cleared) the position register value is input to the read multiplexers.
- If CCI OWNS BUS is deasserted (CCR1 bit [07] is set) the delay bus value (called external position) is input to the read multiplexers. Note that the external position value is also input to the read multiplexers when location MCM7 is read (Section 2.1.11).

Synchronization loop operation (Section 2.4.3) causes the register and bus values to differ.

The register is not automatically cleared at power-up; a known value must be loaded into the register.

When this location is read, six bits of the clock divider value are also read into the transfer register (Figure 2–5), as follows:

Transfer register bits [15:10] = Clock divider bits [05:00]
Transfer register bits [09:00] = External position bits [09:00]

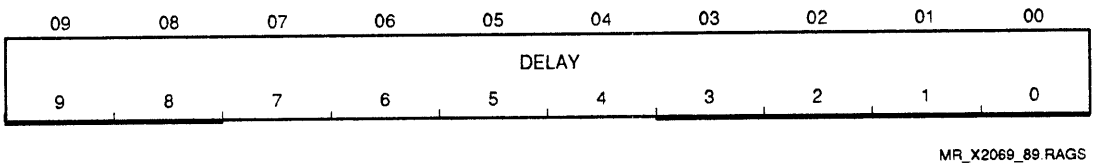


Figure 2–13 CCI Position Register Format

Table 2–7 CCI Position Register Bit Description

Bits	Name	Description
10:00	Delay [10:0]	When CCI owns bus is asserted (clock control register 1 bit [07] is cleared), this value is written to the delay bus.

2.1.10 EEPROM Read (MCM6)

This location provides the means to read information, such as serial or revision numbers, from the MCM's 2-Kbyte EEPROM. Note that only 256 bytes of the 2-Kbyte EEPROM are used.

The EEPROM's address lines are connected to the CCI's BIT15 READ through BIT8 READ output pins, and the EEPROM's data lines are connected to the CCI's BIT7 through BIT0 input pins (Figure 2–14). A read request to this location, with transfer register bits [15:08] set to the EEPROM address, returns the 8-bit EEPROM data in transfer register bits [07:00] (Figure 2–5). If the console writes to this location, the CCI returns an ACKNOWLEDGE; however, this is a no-op and the CCI does not perform any other operations on this request.

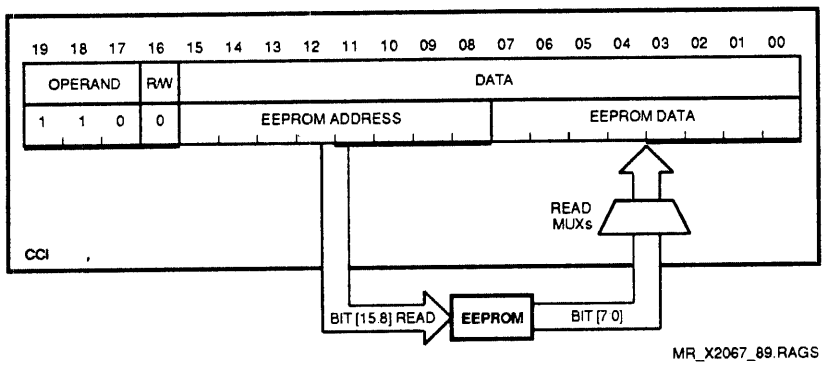


Figure 2–14 CCI EEPROM Read

2.1.11 Clock Divider (MCM7)

The 11-bit clock divider is a resettable, count-up counter, clocked by the 1-MHz clock (MEGAHERTZ) from the frequency synthesizer. The three most significant bits of the clock divider are inputs to the SLOW CLOCK multiplexer (Figure 2–15). The multiplexer inputs are selected by signals CDIVS1 and CDIVS0 from CCR1 bits [09:08] (Section 2.1.8), as follows (Table 2–8):

Table 2–8 CCI Slow Clock Frequency Select

CCR1 [09:08] Value	Slow Clock Frequency
00	Stop slow clock (power-up value).
01	488 Hz (Divide 1 MHz by 2048).
10	976 Hz (Divide 1 MHz by 1024).
11	1095 Hz (Divide 1 MHz by 512).

The console can read and write all bits of this location. Writing to MCM7 loads data into the clock divider. When this location is read, burst counter and external position values are read into the transfer register (Figure 2–5), as follows:

Transfer register bits [15:10] = Burst counter bits [13:08]
Transfer register bits [09:00] = External position bits [09:00]

Note that the external position value can also be input to the read multiplexers when location MCM5 is read (Section 2.1.9).

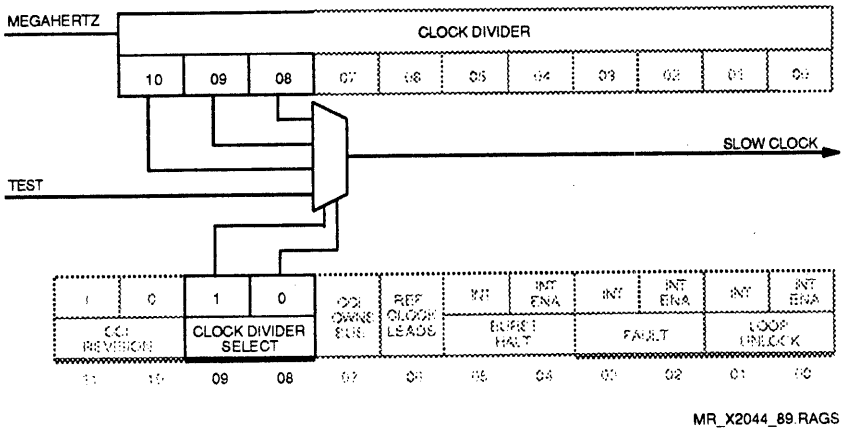


Figure 2–15 CCI Clock Divider

2.1.12 Clock Modes

Figure 2–16 is a simplified diagram of the clock control logic. Each multiplexer is controlled by one of five 2-bit burst enable and clock run fields in clock control register 0 (Section 2.1.2). Each multiplexer output is fed through a synchronization circuit where the clock control signals are synchronized with the reference clock. The synchronizer output signals are the clock control signals to the CPUs and SCU. The following sections describe the clock modes.

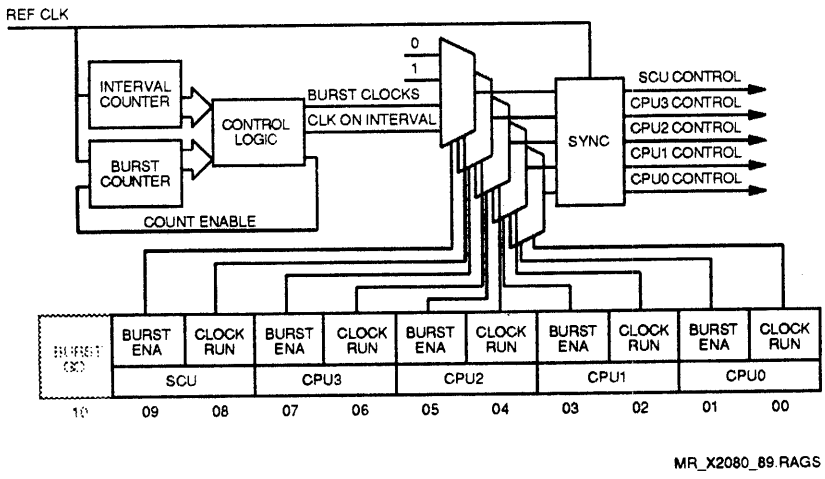


Figure 2–16 CCI Clock Control Implementation

2.1.12.1 Stop Clocks Mode

Burst Enable	Clock Run	Multiplexer Input
0	0	Logical 0

The logical-zero multiplexer input causes the clock control signal to be deasserted. This is the power-up condition.

2.1.12.2 Run Clocks Mode

Burst Enable	Clock Run	Multiplexer Input
0	1	Logical 1

Clocks are enabled for every machine cycle. The logical-one multiplexer input causes the clock control signal to be constantly asserted. The burst and interval counters are ignored. This is the normal operating condition.

2.1.12.3 Burst Clocks Mode

Burst Enable	Clock Run	Multiplexer Input
1	0	BURST CLOCKS

The BURST CLOCKS signal is asserted only when the burst counter count is greater than zero and the interval counter count is zero. This results in two submodes: burst clocks and burst clocks on interval. (The burst and interval counters are described in Sections 2.1.5 and 2.1.7.)

When the interval register value is zero, the interval counter value is also zero and doesn't change until the interval register is reloaded. Therefore, the BURST CLOCKS and clock control signals depend only on the burst counter value. The clock control signal is asserted and enables clocks for the number of machine cycles specified by the burst counter value.

2.1.12.4 Burst Clocks on Interval Mode

Burst Enable	Clock Run	Multiplexer Input
1	0	BURST CLOCKS

As stated in the preceding section, the BURST CLOCKS signal is asserted only when the burst counter value is greater than zero and the interval counter value is zero.

When the interval register value is greater than zero, that value is loaded into the interval counter each time it counts down to zero. When the interval counter value is greater than zero, the burst counter clock and BURST ENABLE are disabled. Therefore, for the number of machine cycles equal to the interval counter value, the burst counter value does not decrement, and clock control deasserts.

When the interval counter value decrements to zero, the burst counter value decrements by one, and clock control asserts for one machine cycle.

For example: If the interval register value = 5, and the burst counter value = 10, clocks are disabled for five machine cycles, enabled for one machine cycle, disabled for five machine cycles, enabled for one machine cycle, and so on, until the burst counter decrements to zero at the end of 50 machine cycles.

2.1.12.5 Clock on Interval Mode

Burst Enable	Clock Run	Multiplexer Input
1	1	CLK ON INTERVAL

Run clocks at intervals specified by the interval counter value. Clock control and CLOCK ON INTERVAL are deasserted if the interval counter value is greater than zero.

When the interval counter value decrements to zero, clock control is asserted for one machine cycle and the interval counter is reloaded from the interval register.

For example: If the interval register value = 2, clocks are disabled for two machine cycles, enabled for one machine cycle, disabled for two machine cycles, enabled for one machine cycle, and so on, until the interval register value is changed.

2.1.13 Interrupts and Serial Data Output

CCI interrupts are transferred to the console over the serial data output path, as shown in Figure 2–17. The CCI generates three different interrupts:

- Burst halt
- Fault (excessive time between MCLK and RCLK leading edges)
- Loop unlocked

When one of these interrupts occurs, it sets a bit in CCR1. If the interrupt is enabled, it is passed through the interrupt gates to the input of the serial data output multiplexer. The other input to the multiplexer is the transfer register (through the bypass latch). The console selects the multiplexer input with the GATE INTERRUPT signal. If the console asserts GATE INTERRUPT, interrupts are transferred over the SERIAL DATA OUTPUT line; otherwise, transfer register data is transferred.

2.1.13.1 Bypass Latch

The bypass latch is an additional two-phase latch in the serial data output path. By asserting BYPASS, the console can bypass this latch. BYPASS asserts the clock inputs to both halves of the latch, and transfer register data is gated through to the serial data output multiplexer. When BYPASS is not asserted, the latch is clocked normally by nonoverlapping phase A and B clocks, and transfer register data is clocked through to the serial data output multiplexer.

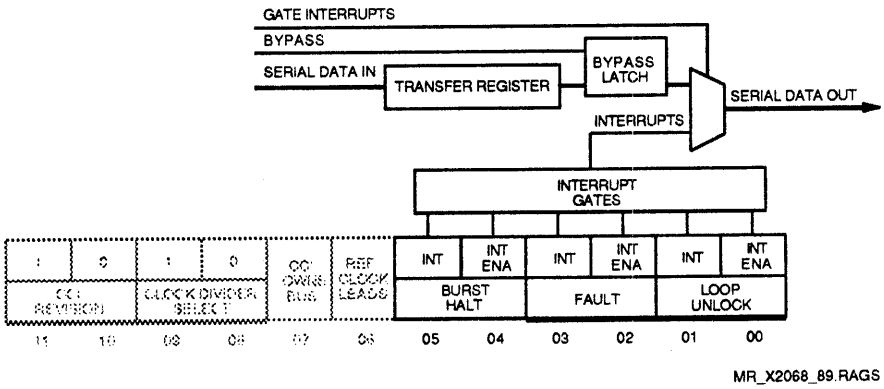


Figure 2–17 CCI Interrupts

2.1.14 SPU Power OK

The CCI converts the SPU power signal from TTL to ECL, and distributes one copy to each CPU and the SCU. This signal is normally asserted.

If power to the SPU fails or is not in specification, the SPU PWR OK signals are deasserted; the CPUs and SCU ignore any subsequent console commands. In the CCI, the state machine enters and remains in the reset state, and any data in the transfer register is ignored.

2.1.15 Initialization and Reset

With the exception of the interval, position, and burst registers, all CCI registers and counters are initialized by MCM RESET at power-up. Coming from the signal interface panel (SIP), MCM RESET is not asserted until all the required power supplies have reached their specified outputs.

2.2 MCLK Channel

The MCLK channel generates and distributes the master clock signal, generates a 1-MHz clock, and provides frequency synthesizer status. It includes the frequency synthesizer, resistive coupler, fixed delay line, and power divider (Figure 2–18).

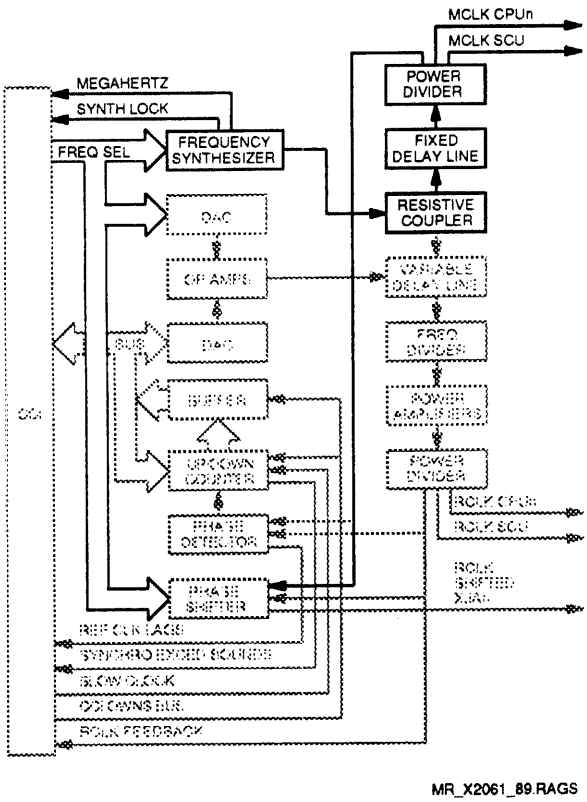


Figure 2–18 MCM MCLK Channel

2.2.1 Frequency Synthesizer

The frequency synthesizer is a phase-locked, voltage controlled oscillator (VCO) contained in a separate subassembly on the MCM (Figure 1–1).

The frequency select bus (FREQ SEL7 through FREQ SEL0) from the CCI and power are the only inputs to the synthesizer. The CCI frequency register (Section 2.1.3) drives the frequency select bus, which controls the synthesizer's VCO.

Synthesizer outputs are SYNTH MCLK to the MCLK channel fixed delay line, RCLK channel variable delay line, and LOCK and MEGAHERTZ to the CCI.

The master clock output signal, SYNTH MCLK, is a sinusoidal signal in the frequency range from 340 MHz to 580 MHz. Its RF power level is approximately 0.5 W.

The SYNTH LOCK signal is normally asserted. If a synchronizer fault occurs, SYNTH LOCK is deasserted, setting the loop unlocked interrupt bit in CCR1 (Section 2.1.8). Possible synchronizer faults are loss of the reference oscillator, off frequency, or locked on the wrong phase.

The free running 1-MHz clock output, MEGAHERTZ, provides timing for many CCI functions and is the source of the slow clock (Section 2.1.11).

2.2.2 Fixed Delay Line

The fixed delay line in the MCLK channel is an exact length of coaxial cable that compensates for delays in the RCLK channel.

2.2.3 Power Dividers

The MCLK and RCLK power dividers are identical. Depending on system configuration, these microwave dividers provide a 1:20 (up to four CPUs) or 1:12 (up to two CPUs) split. The dividers provide transformer-coupled balanced dual outputs for each output port, with up to 30 db of isolation between ports. The MCM's power divider inputs and outputs are coupled to coaxial cables.

2.3 RCLK Channel

The RCLK channel divides the master clock frequency by eight to produce the reference clock, increases signal power, and distributes it to the rest of the system. It includes the frequency divider, power amplifiers, and power divider (Figure 2–19). The power dividers are identical to the MCLK channel power dividers (Section 2.2.3).

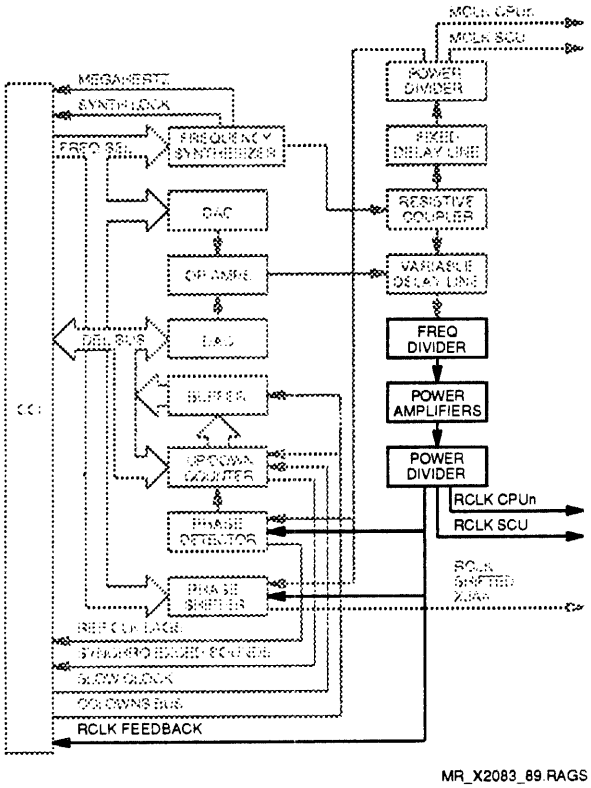


Figure 2–19 MCM RCLK Channel

2.3.1 Frequency Divider

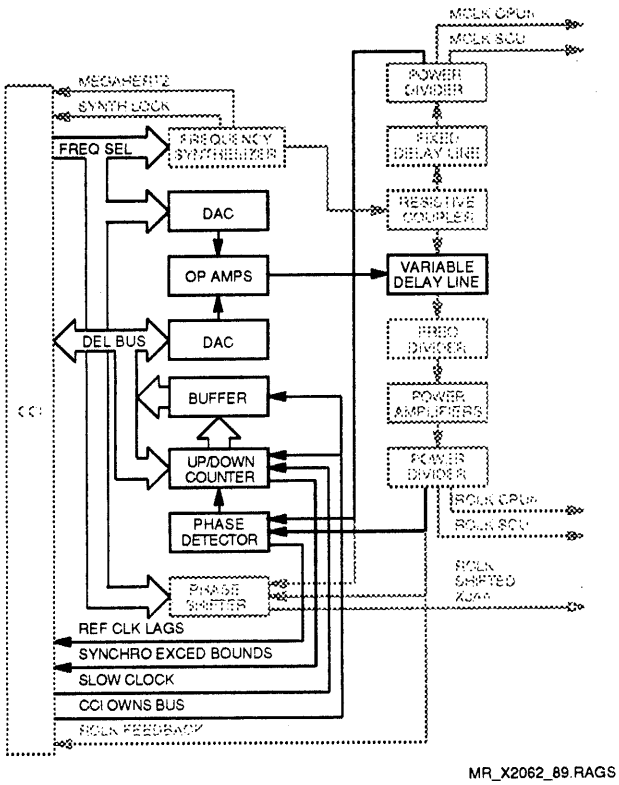
A sample of the master clock is taken from the resistive coupler and fed through the variable delay line to the divide-by-eight frequency divider. The divider output is the low-power reference clock at one-eighth the frequency of the master clock.

2.3.2 Power Amplifiers

The low-power reference clock from the frequency divider is input to two cascaded RF power amplifiers. The amplifiers have a combined total gain of approximately 25 db and the output signal is approximately 9 V peak-to-peak. Frequency response of the amplifiers falls off below 50 MHz, causing some degradation of the RCLK square wave at those frequencies. The output of the amplifiers is fed to the power divider through a coaxial cable.

2.4 Synchronizer

The synchronizer maintains the alignment between the rising edges of the master and reference clocks. It also reports the relative position of the two clocks in terms of lead/lag and whether the relative position is in specified limits. The synchronizer includes the phase detector, up/down counter, digital-to-analog converters (DACs), op amps (operational amplifiers), and variable delay line (Figure 2–20). Note that the up/down counter, DACs, and op amps are also called the "synchronization loop."



MR_X2062_89.RAGS

Figure 2–20 MCM Synchronizer

2.4.1 Variable Delay Line

The variable delay line consists of eight varactor diodes that simulate the capacitance of a transmission line. The synchronizer loop (Section 2.4.3) controls the bias on the diodes to vary the delay.

2.4.2 Phase Detector

The phase detector is a high-speed flip-flop, clocked by the reference clock with the master clock as the data input. If the master clock positive transition occurs before the reference clock's (reference clock lags), the detector output, REF CLK LAGS, is low; if the reference clock leads, the output is high. Detector output determines the count direction of the up/down counter.

When REF CLK LAGS is low, CCR1 bit [06] is set (Section 2.1.8).

2.4.3 Synchronization Loop

The synchronization loop consists of the phase detector, up/down counter, DACs, and op amps. It varies the bias applied to the variable delay line varactor diodes.

One DAC gets its input from the frequency select bus (through the XJA clock phase shifter PROM, Section 2.5). It provides a component of varactor bias to adjust the delay as a function of frequency.

The other DAC gets its input from the delay bus. The value on the bus depends on the CCI OWNS BUS signal, as follows:

- When CCI OWNS BUS is asserted (CCR1 bit [07] is cleared), the value in the position register (Section 2.1.9) is placed on the delay bus.
- When CCI OWNS BUS is deasserted, the value on the delay bus is loaded into the up/down counter and input to the DAC. At the same time, the buffered counter output is placed on the bus. Therefore, DAC output is now proportional to the counter value and direction.

The output of each DAC goes to an operational amplifier. The outputs of both operational amplifiers are summed and applied to the input of a third operational amplifier. The output of the third operational amplifier is the source for varactor bias.

Ultimately, the relative position of the master and reference clocks determine the amount of variable delay line delay, as follows:

- Reference clock leads

  When the reference clock leads the master clock, the phase detector output is high, causing the following:

  1. The up/down counter counts down.
  2. Delay bus DAC output voltage decreases.
  3. Delay line varactor bias decreases.
  4. Delay line capacitance increases.
  5. Delay line delay increases.

- Reference clock lags

  When the reference clock lags the master clock, the phase detector output is low, causing the following:

  1. The up/down counter counts up.
  2. Delay bus DAC output voltage increases.
  3. Delay line varactor bias increases.
  4. Delay line capacitance decreases.
  5. Delay line delay decreases.

If the value in the up/down counter exceeds the range from 0 to 255 (that is, underflow or overflow occurs), SYNCHRO EXCED BOUNDS is asserted, setting CCR1 [03], the fault interrupt bit.

2.5 XJA Clock Channel

The phase shifter (Figure 2–21) adjusts the position of the reference clock in one-eighth machine cycle increments to compensate for differences in data and timing delays to the XJAs.

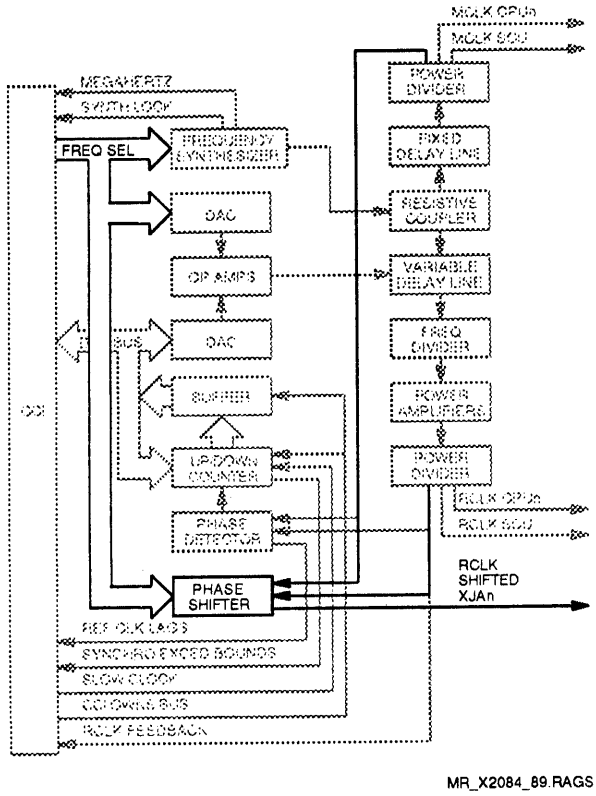


Figure 2–21 MCM XJA Clock Channel

2.5.1 Phase Shifter

Figure 2–22 is a detailed block diagram of the phase shifter. The PROM, addressed by FREQ SEL7 through FREQ SEL0, is a lookup table that provides a frequency-dependent value to the shift register.

The four least significant bits of the PROM are input to a TTL-to-ECL level converter/inverter. From the converter/inverter, the value and its complement are loaded into the 8-bit shift register with every RCLK. The shift register is clocked by MCLK and the output of its sixth bit is fanned out as RCLK SHIFTED XJAn.

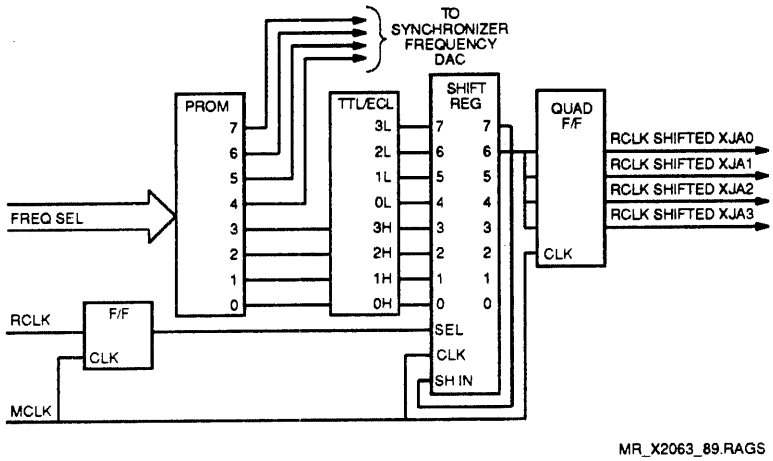


Figure 2–22 MCM XJA Clock Phase Shifter

The values in the PROM lookup table are such that the XJA clock is shifted in one-eighth machine cycle increments, or 45 degrees, according to the frequency of MCLK. The frequency/phase relationship is shown in Figure 2–23. Note that this same PROM provides a frequency compensation value to the synchronization loop (Section 2.4.3).

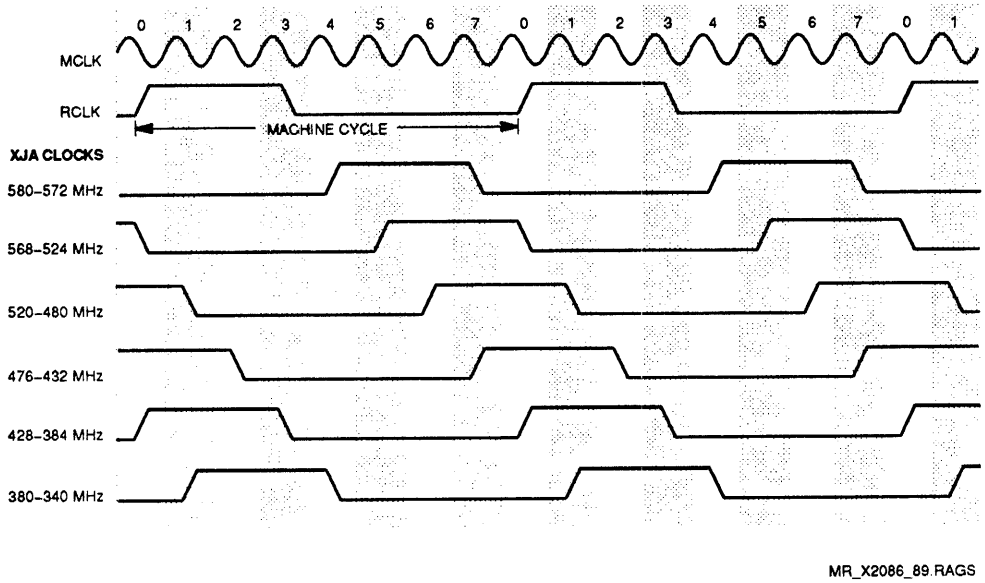


Figure 2–23 XJA Clock Timing

3
CDXX Description

This chapter describes the functions of the clock distribution gate array, or CDXX.

3.1 Introduction

A CDXX is mounted in the center of every HDSC. Its two major functions are to provide the scan function interface to the other MCAs on the HDSC and distribute clocks. (For more information on scan system operation, see *VAX 9000 Family SPU Technical Description.*) More specifically, the CDXX does the following:

- Buffers and distributes MCLK to the gate arrays.
- Buffers, reshapes, and distributes RCLK to the gate arrays.
- Generates and distributes STRAM clocks to the gate arrays.
- Provides the interface between the HDSC and the SPU scan control module (SCM).
- Detects clock synchronization errors.
- Detects HDSC overtemperature.
- Reports exception conditions to the SCM.
- Reports the HDSC serial number to the SCM.

Figure 3–1 is a simplified block diagram of the CDXX.

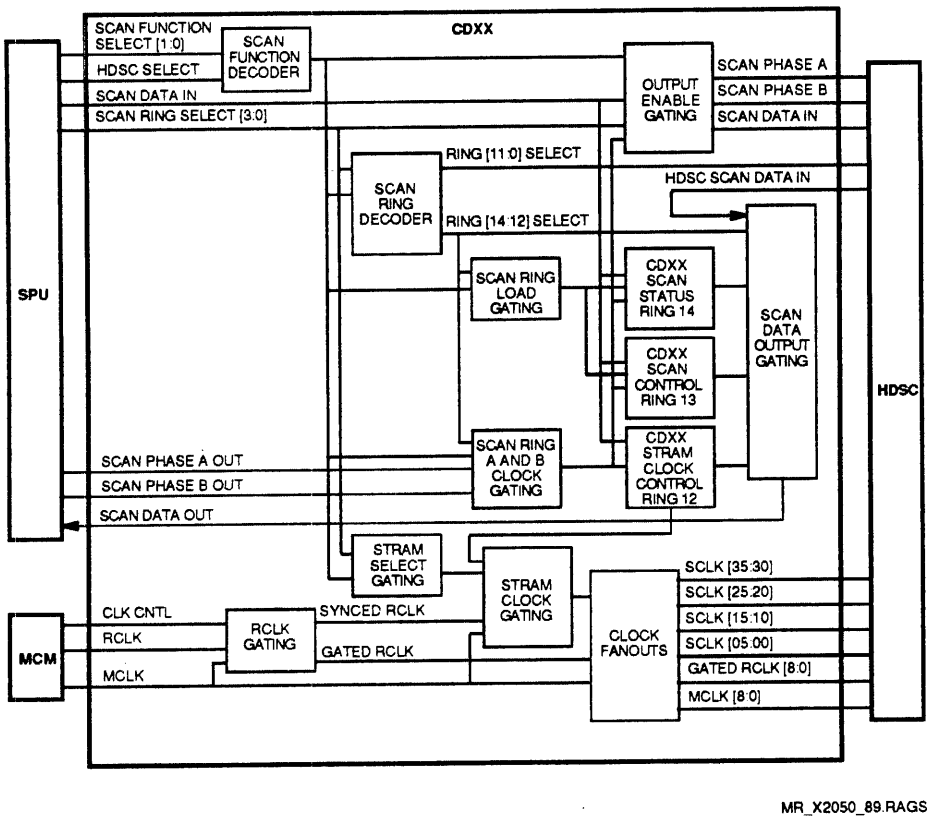


Figure 3–1 CDXX Block Diagram

3.2 Scan Functions

With the exception of MCLK and RCLK functions, all CDXX functions, including STRAM clock generation, depend on scan control signals from the SPU. These signals are shown in Figures 3–2 and 3–3 and are described in Table 3–1.

Table 3–1 Scan Control Signal Description

Signal	Description
HDSC SELECT	Selects this HDSC and enables the scan function decoder.
SCAN FUNCTION SELECT 1 SCAN FUNCTION SELECT 0	Select the scan function decoder output as shown in Table 3–2.
SCAN RING SELECT 3 through SCAN RING SELECT 0	Select the scan rings or the STRAM clocks, depending on the scan function, as shown in Table 3–2.
SCAN PHASE A OUT SCAN PHASE B OUT	Phase A and B scan clocks.

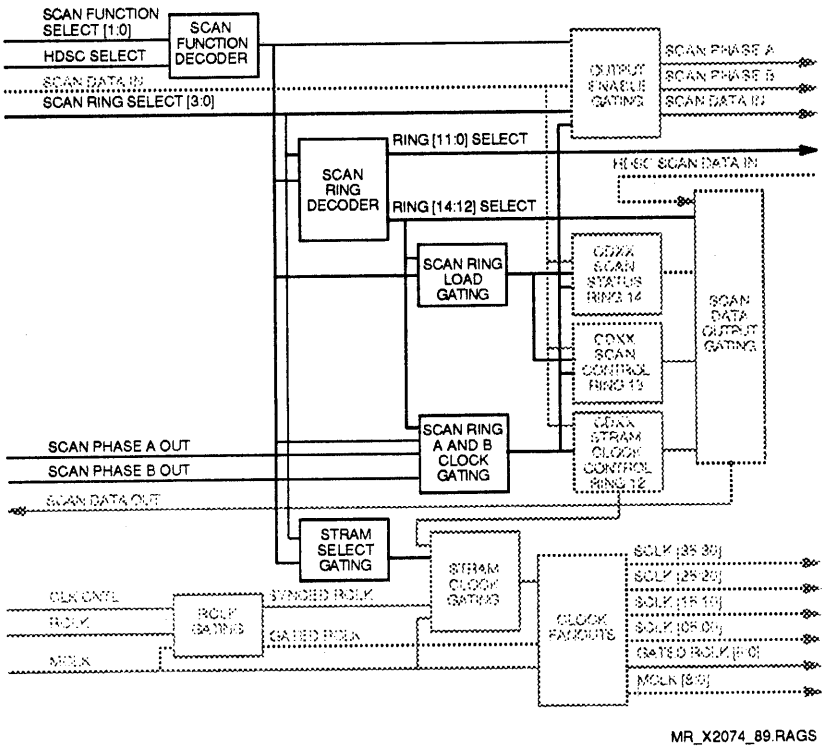


Figure 3–2 CDXX Decoder Functions

Each CDXX receives the scan control signals from the previous CDXX and sends them to the next CDXX, but the first CDXX on the scan bus (SBUS) receives scan signals from the SCM. The last CDXX on the scan bus sends scan signals to the SCM.

When a CDXX is not selected, it passes data from the SCAN DATA IN line to the SCAN DATA OUT line. When a CDXX is selected and the scan bus is not in the no-op state (Section 3.2.1), data moves from the SCAN DATA IN line to the selected scan ring to the SCAN DATA OUT line.

3.2.1 Scan Bus States

The scan bus states correspond to the functions encoded in SCAN FUNCTION SELECT 1 and 0 (Table 3–2).

Normally, the scan bus is in the no-op (no operation in progress) state. In this state, a nonselected CDXX can report *enabled* exception conditions onto the SCAN DATA OUT line. See Section 3.2.6 for more information on exception conditions.

If the scan bus is in the no-op or STRAM LOAD state and the CDXX is selected, then the CDXX is in the LOOPBACK mode. In this mode, scan data in, scan ring select, and scan clock signals are NORed (ORed and inverted) onto the SCAN DATA OUT line for fault isolation purposes (Figure 3–9).

If the scan bus is in the SCAN LOAD or SCAN SHIFT state and the CDXX is selected, SCAN RING SELECT 3 through 0 select one of 16 scan rings. (See Sections 3.2.3 through 3.2.3.4 for a description of the scan rings.)

If the scan bus is in the STRAM LOAD state and the CDXX is selected, SCAN RING SELECT 3 through 0 select the STRAM group(s).

Table 3–2 Scan Ring/STRAM Clock Select Decoding

SCAN FUNCTION SELECT 1 0	Function[1]	SCAN RING SELECT 3 2 1 0	Select
0 0	No-op	–	–
0 1	SCAN SHIFT	0 0 0 0	RING 0 SELECT (HDSC ring)
		0 0 0 1	RING 1 SELECT (HDSC ring)
		0 0 1 0	RING 2 SELECT (HDSC ring)
		0 0 1 1	RING 3 SELECT (HDSC ring)
		0 1 0 0	RING 4 SELECT (HDSC ring)
		0 1 0 1	RING 5 SELECT (HDSC ring)
		0 1 1 0	RING 6 SELECT (HDSC ring)
		0 1 1 1	RING 7 SELECT (HDSC ring)
		1 0 0 0	RING 8 SELECT (HDSC spare ring)
		1 0 0 1	RING 9 SELECT (HDSC spare ring)
		1 0 1 0	RING 10 SELECT (HDSC spare ring)
		1 0 1 1	RING 11 SELECT (HDSC spare ring)
		1 1 0 0	RING 12 SELECT (CDXX ring)
		1 1 0 1	RING 13 SELECT (CDXX ring)
		1 1 1 0	RING 14 SELECT (CDXX ring)
		1 1 1 1	RING 15 SELECT (Broadcast — HDSC rings 7 through 0)

[1]These functions correspond to scan bus states.

Table 3–2 (Cont.) Scan Ring/STRAM Clock Select Decoding

SCAN FUNCTION SELECT 1 0	Function[1]	SCAN RING SELECT 3 2 1 0	Select
1 0	SCAN LOAD	0 0 0 0	RING 0 SELECT (HDSC ring)
		0 0 0 1	RING 1 SELECT (HDSC ring)
		0 0 1 0	RING 2 SELECT (HDSC ring)
		0 0 1 1	RING 3 SELECT (HDSC ring)
		0 1 0 0	RING 4 SELECT (HDSC ring)
		0 1 0 1	RING 5 SELECT (HDSC ring)
		0 1 1 0	RING 6 SELECT (HDSC ring)
		0 1 1 1	RING 7 SELECT (HDSC ring)
		1 0 0 0	RING 8 SELECT (HDSC spare ring)
		1 0 0 1	RING 9 SELECT (HDSC spare ring)
		1 0 1 0	RING 10 SELECT (HDSC spare ring)
		1 0 1 1	RING 11 SELECT (HDSC spare ring)
		1 1 0 0	RING 12 SELECT (CDXX ring)
		1 1 0 1	RING 13 SELECT (CDXX ring)
		1 1 1 0	RING 14 SELECT (CDXX ring)
		1 1 1 1	RING 15 SELECT (Broadcast — HDSC rings 7 through 0)
1 1	STRAM LOAD	0 0 0 1	STRAM GROUP 0 LOAD SELECT
		0 0 1 0	STRAM GROUP 1 LOAD SELECT
		0 0 1 1	STRAM GROUP 1, 0 LOAD SELECT
		0 1 0 0	STRAM GROUP 2 LOAD SELECT
		0 1 0 1	STRAM GROUP 2, 0 LOAD SELECT
		0 1 1 0	STRAM GROUP 2, 1 LOAD SELECT
		0 1 1 1	STRAM GROUP 2, 1, 0 LOAD SELECT
		1 0 0 0	STRAM GROUP 3 LOAD SELECT
		1 0 0 1	STRAM GROUP 3, 0 LOAD SELECT
		1 0 1 0	STRAM GROUP 3, 1 LOAD SELECT
		1 0 1 1	STRAM GROUP 3, 1, 0 LOAD SELECT
		1 1 0 0	STRAM GROUP 3, 2 LOAD SELECT
		1 1 0 1	STRAM GROUP 3, 2, 0 LOAD SELECT
		1 1 1 0	STRAM GROUP 3, 2, 1 LOAD SELECT
		1 1 1 1	STRAM GROUP 3, 2, 1, 0 LOAD SELECT

[1]These functions correspond to scan bus states.

3.2.2 Scan Function Decoding

Figure 3–3 is a detailed picture of scan control signal decoding.

The HDSC SELECT signal enables the scan function decoder. The decoder and its associated gating:

- Enable scan ring selection and scan clock generation for scan ring load and shift operations.
- For STRAM clock generation, assert the STRAM group load signal according to the scan ring select control signal.

  For STRAM load and no-op operations, scan clocks to the scan rings are disabled.

The scan ring decoder and its associated gating:

- Select 1 of 12 HDSC scan rings, where rings 0 through 7 are the primary rings and rings 8 through 11 are spare rings.
- Simultaneously select HDSC scan rings 0 through 7 by selecting ring 15.
- Select either CDXX scan ring 12, 13, or 14 and enable scan clocks to the selected ring to shift data through it.
- Parallel load either CDXX scan ring 13 or 14 by enabling SCAN LOAD from the scan function decoder to the selected ring.

See Sections 3.2.3 through 3.2.3.4 for a description of the scan rings.

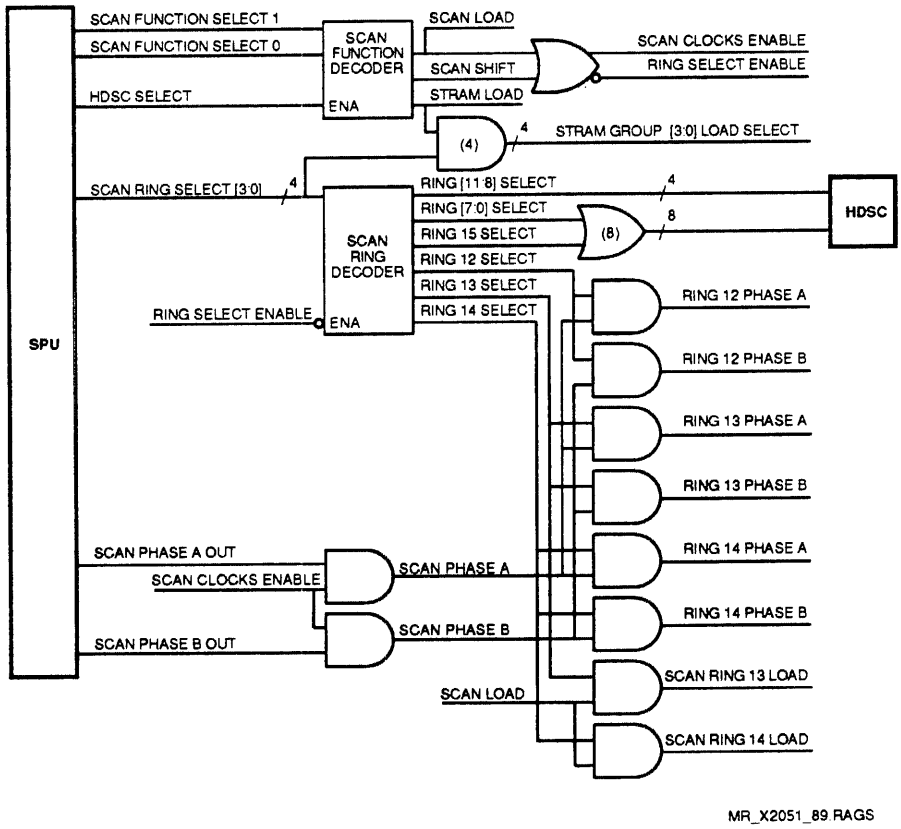


Figure 3–3 CDXX Decoder Details

3.2.3 Scan Ring Overview

The CDXX scan rings are implemented with a set of serially-connected scan latch pairs (Figure 3–4). The first latch in every pair is clocked by the phase A scan clock and the other latch is clocked by the phase B scan clock.

Rings 13 and 14 are special rings in that ring 13 can be loaded and ring 14 can be read while system clocks are running. Because system and scan clocks are ORed together on the MCAs, system clocks are stopped for normal scan operations to prevent disruption of the system state. Together, rings 13 and 14 enable detection and report the occurrence of exception conditions. When an exception condition occurs, the SPU can scan ring 14 on all CDXXs to determine the location and cause of the exception while the system is running. See Section 3.2.6 for more information on exception conditions.

As Figure 3–4 shows, a multiplexer is included at the input to each latch pair in rings 13 and 14. The multiplexer allows these rings to operate in serial or parallel mode. Normally, the rings are in serial mode, and the serial data input is passed through the multiplexers. In parallel mode, a load signal is asserted to select the parallel data input to the multiplexers. (The CCI transfer register (Section 2.1.1.3) is implemented similarly to rings 13 and 14.)

Serial data (scan data) is shifted in through the LSB and out through the MSB of all three CDXX scan rings.

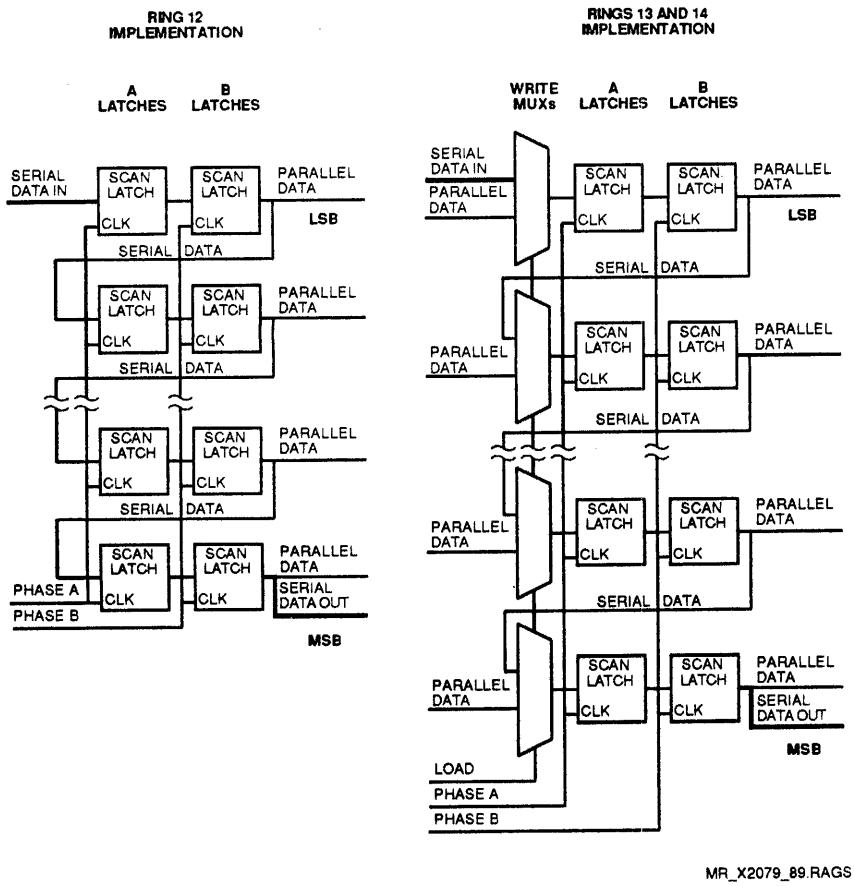


Figure 3–4 CDXX Scan Ring Implementation

Figure 3–5 highlights the scan ring functions in the CDXX. Sections 3.2.3.1 through 3.2.3.4 describe the 16 scan rings selected by the CDXX.

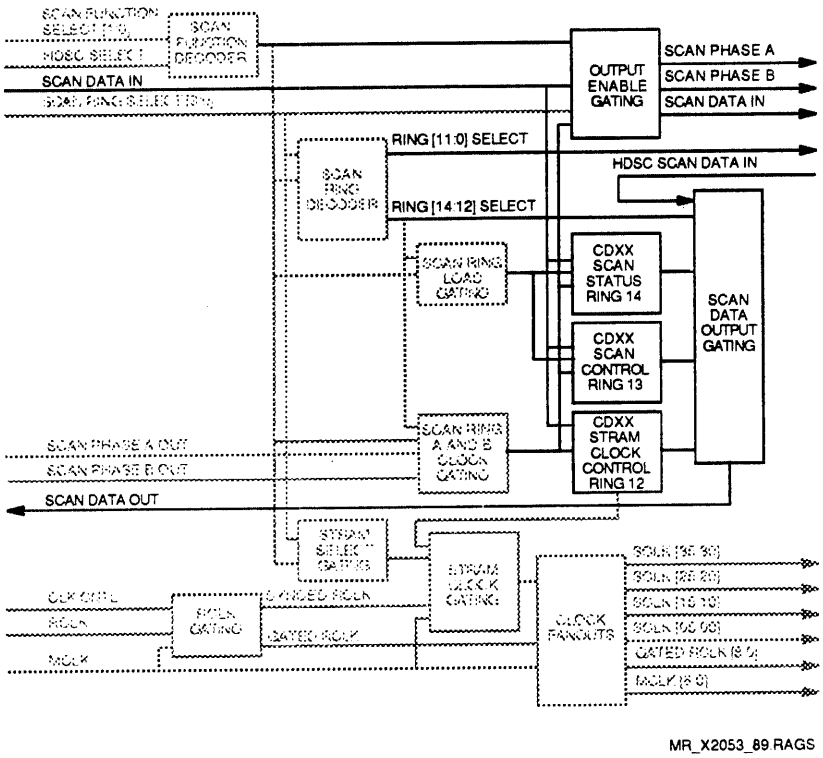


Figure 3–5 CDXX Scan Ring Functions

3.2.3.1 HDSC Scan Rings

Scan rings 0 through 7 are reserved for the eight gate arrays on the HDSC. Scan rings 8 through 11 are spare rings reserved for the gate arrays on the HDSC. Scan ring 15 is the broadcast ring. It selects HDSC rings 7 through 0 to save or restore machine state quickly.

3.2.3.2 CDXX Scan Ring 12

Scan ring 12 (Figure 3–6 and Table 3–3) is the CDXX STRAM clock control ring. This 16-bit ring cannot be parallel loaded. Data in this ring controls the STRAM clock phase-select multiplexers. See Section 3.3.3 for more information on STRAM clock generation.

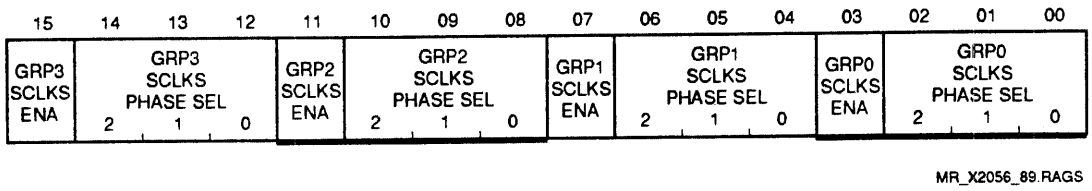


Figure 3–6 CDXX Scan Ring 12 Format

Table 3–3 CDXX Scan Ring 12 Bit Description

Bits	Mnemonic	Description
15	GRP3 SCLKS ENA	When set, enables generation of group 3 STRAM clocks (SCLK35 through SCLK30).
14:12	GRP3 SCLKS PHASE SEL [2:0]	This binary-encoded field selects the phase for the group 3 STRAM clocks (SCLK35 through SCLK30), as follows: 0 0 0 Phase 0 0 0 1 Phase 1 0 1 0 Phase 2 0 1 1 Phase 3 1 0 0 Phase 4 1 0 1 Phase 5 1 1 0 Phase 6 1 1 1 Phase 7
11	GRP2 SCLKS ENA	When set, enables generation of group 2 STRAM clocks (SCLK25 through SCLK20).
10:08	GRP2 SCLKS PHASE SEL [2:0]	This binary-encoded field selects the phase for the group 2 STRAM clocks (SCLK25 through SCLK20), as follows: 0 0 0 Phase 0 0 0 1 Phase 1 0 1 0 Phase 2 0 1 1 Phase 3 1 0 0 Phase 4 1 0 1 Phase 5 1 1 0 Phase 6 1 1 1 Phase 7
07	GRP1 SCLKS ENA	When set, enables generation of group 1 STRAM clocks (SCLK15 through SCLK10).
06:04	GRP1 SCLKS PHASE SEL [2:0]	This binary-encoded field selects the phase for the group 1 STRAM clocks (SCLK15 through SCLK10), as follows: 0 0 0 Phase 0 0 0 1 Phase 1 0 1 0 Phase 2 0 1 1 Phase 3 1 0 0 Phase 4 1 0 1 Phase 5 1 1 0 Phase 6 1 1 1 Phase 7
03	GRP0 SCLKS ENA	When set, enables generation of group 0 STRAM clocks (SCLK05 through SCLK00).
02:00	GRP0 SCLKS PHASE SEL [2:0]	This binary-encoded field selects the phase for the group 0 STRAM clocks (SCLK05 through SCLK00), as follows: 0 0 0 Phase 0 0 0 1 Phase 1 0 1 0 Phase 2 0 1 1 Phase 3 1 0 0 Phase 4 1 0 1 Phase 5 1 1 0 Phase 6 1 1 1 Phase 7

3.2.3.3 CDXX Scan Ring 13

Scan ring 13 (Figure 3–7 and Table 3–4) is the CDXX scan control ring. This 14-bit ring is parallel cleared (loaded with zeros) and cannot be read. Data is shifted into this ring, then loaded into the three CDXX control registers:

HOT (HDSC overtemperature) control register
Clock check control register
Exception control register

After the registers are loaded, this ring is cleared. Exception conditions are described in Section 3.2.6.

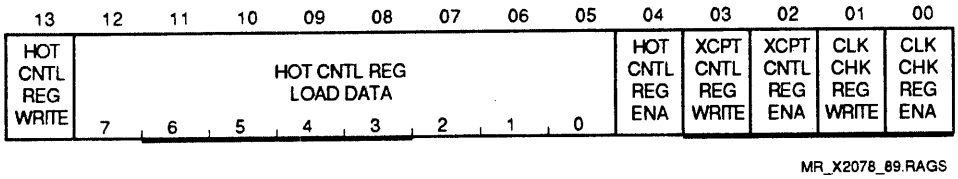


Figure 3–7 CDXX Scan Ring 13 Format

Table 3–4 CDXX Scan Ring 13 Bit Description

Bits	Mnemonic	Description
13	HOT CNTL REG WRITE	When set, write enables the HOT control register and the data in bits [12:05] are loaded into that register.
12:05	HOT CNTL REG LOAD DATA [7:0]	The new encoded HDSC overtemperature trip point setting. When bit 13 is set, the value in these bits is loaded into HOT control register [08:01]. (**Note**: Scan ring 14 [13:06] contains the currently loaded value.)
04	HOT CNTL REG ENA	When this bit and bit 13 are set, HOT control register bit 0 is set, enabling HOT (overtemperature) exception condition reporting.
03	XCPT CNTL REG WRITE	When set, write enables the exception control register and the value in bit 2 is loaded into that register.
02	XCPT CNTL REG ENA	When this bit and bit 3 are set, exception control register bit 0 is set, enabling exception condition reporting.
01	CLK CHK REG WRITE	When set, write enables the clock check control register and the value in bit 0 is loaded into that register.
00	CLK CHK REG ENA	When this bit and bit 1 are set, clock check control register bit 0 is set, enabling clock synchronization failure exception condition reporting.

3.2.3.4 CDXX Scan Ring 14

Scan ring 14 (Figure 3–8 and Table 3–5) is the CDXX information scan ring. This 47-bit ring is parallel loaded. Data is loaded into this ring, then shifted out to the SCM. In addition to control register data, this ring contains the CDXX revision number and the HDSC type, revision number, and serial number. This ring has no effect on any registers or latches, with the exception of the clock system failure and latched exception latches. These two latches store any exceptions that occurred after this ring was last loaded. Exception conditions are described in Section 3.2.6.

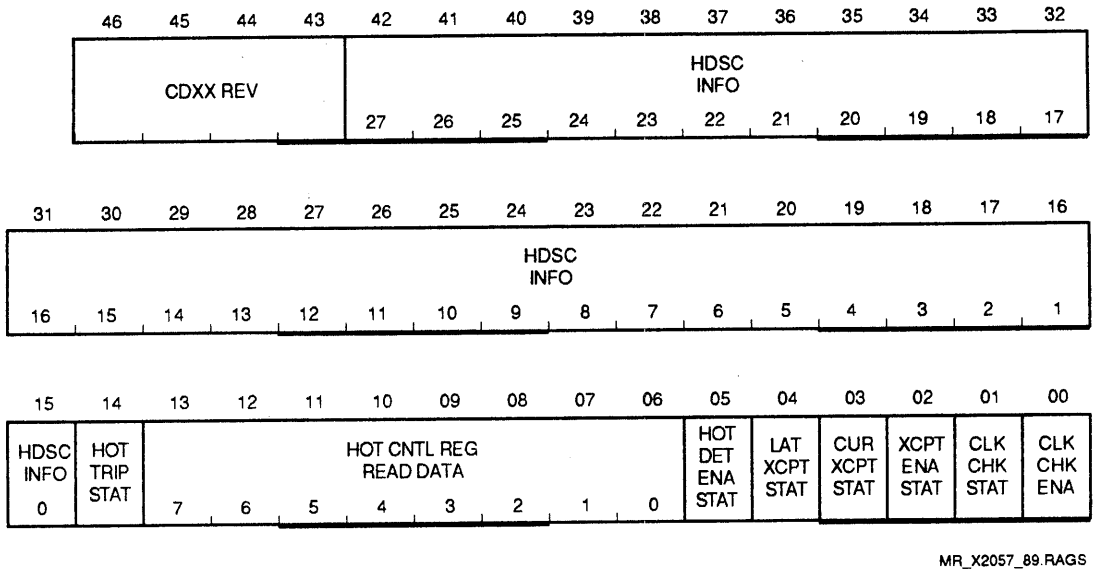


Figure 3–8 CDXX Scan Ring 14 Format

Table 3–5 CDXX Scan Ring 14 Bit Description

Bits	Mnemonic	Description
46:43	CDXX REV	The 4-bit CDXX revision number. Bit 46 is the most significant bit of the revision number.
42:15	HDSC INFO	HDSC information. The 28-bit HDSC type, revision number, and serial number.
14	HOT TRIP STAT	HOT tripped status. When set, indicates that the HDSC temperature exceeded the programmed HOT value. An exception is reported to the console on the SCAN DATA OUTPUT line if: • The programmed HOT value is exceeded. • HOT exception condition reporting is enabled (HOT control register bit 00 is set). • The scan system is idle.
13:06	HOT CNTL REG READ DATA [7:0]	HOT control register read data. This value is a copy of the current encoded HDSC overtemperature trip point setting from HOT control register [08:01]. (**Note**: Scan ring 13 [12:05] contains a new encoded value to be loaded.)

Table 3–5 (Cont.) CDXX Scan Ring 14 Bit Description

Bits	Mnemonic	Description
05	HOT DET ENA STAT	HOT detection enable status. The value in this bit is a copy of the value in HOT control register bit 0. When set, indicates that HOT exception condition reporting is enabled. An exception is reported to the console on the SCAN DATA OUTPUT line if: • HOT exception condition reporting is enabled. • The HDSC temperature exceeded the programmed HOT value. • The scan system is idle.
04	LAT XCPT STAT	Latched exception status. This bit indicates that an HDSC exception occurred since the bit was last read.
03	CUR XCPT STAT	Current exception status. When set, indicates that an HDSC exception is currently occurring.
02	XCPT ENA STAT	Exception enable status. The value in this bit is a copy of the value in exception control register bit 0. When set, indicates that exception condition reporting is enabled. An exception is reported to the console on the SCAN DATA OUTPUT line if: • Exception condition reporting is enabled. • A latched exception condition has occurred. • The scan system is idle.
01	CLK CHK STAT	Clock check status. When set, indicates that a clock system failure has occurred.
00	CLK CHK ENA	Clock check enable status. The value in this bit is a copy of the value in clock check control register bit 0. When set, indicates that clock check exception condition reporting is enabled. An exception is reported to the console on the SCAN DATA OUTPUT line if: • Clock check exception condition reporting is enabled. • A clock system failure has occurred. • The scan system is idle.

3.2.4 Scan Data Flow

Figure 3–9 shows the CDXX scan data in and out paths through the CDXX and Figure 3–10 shows the CDXX to HDSC scan signals.

SCAN DATA OUT to the SPU has several possible sources (Figure 3–9), as follows:

- At the top of the figure, the source of SCAN DATA OUT is either the HDSC scan rings or any one of the CDXX scan rings if:

  This HDSC is selected.
  The scan function is SCAN SHIFT or SCAN LOAD (Table 3–2).

- The NORed combination of SCAN DATA IN and CDXX internal scan ring select and scan clock signals is the source of SCAN DATA OUT if:

  This HDSC is selected.
  The scan function is no-op or STRAM LOAD (Table 3–2).

- Exception conditions (Section 3.2.6) are the source of SCAN DATA OUT if:

  This HDSC is not selected.
  The scan bus is in the no-op state (Table 3–2).

- SCAN DATA IN is the source of SCAN DATA OUT if this HDSC is not selected. In other words, scan data is passed to the next CDXX (or SPU, if this is the last CDXX).

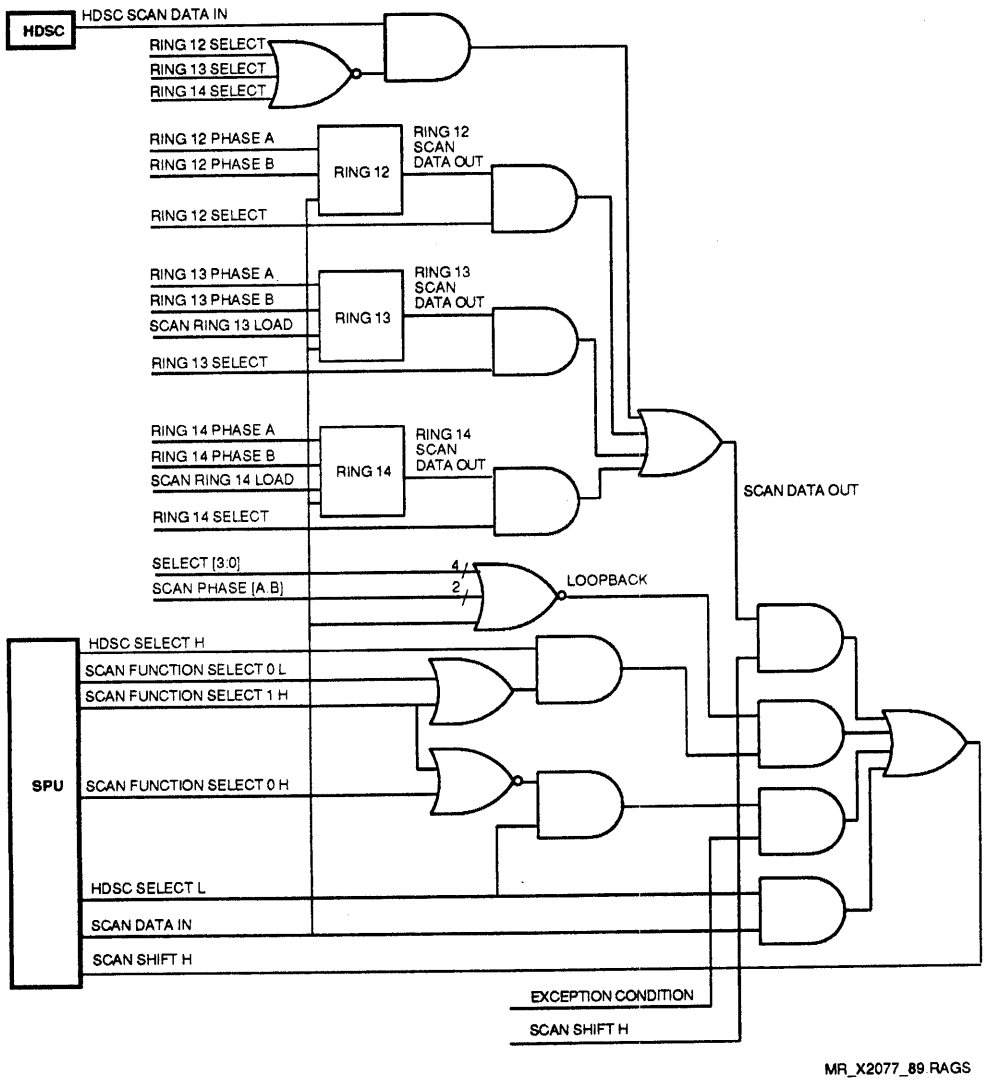


Figure 3–9 CDXX Scan Data Out

As Figure 3–10 shows, scan data in, scan clocks, and scan load signals are not gated to the HDSC unless SCAN OUTPUT ENABLE is asserted. SCAN OUTPUT ENABLE is deasserted only if HDSC scan ring 13 or 14 is selected.

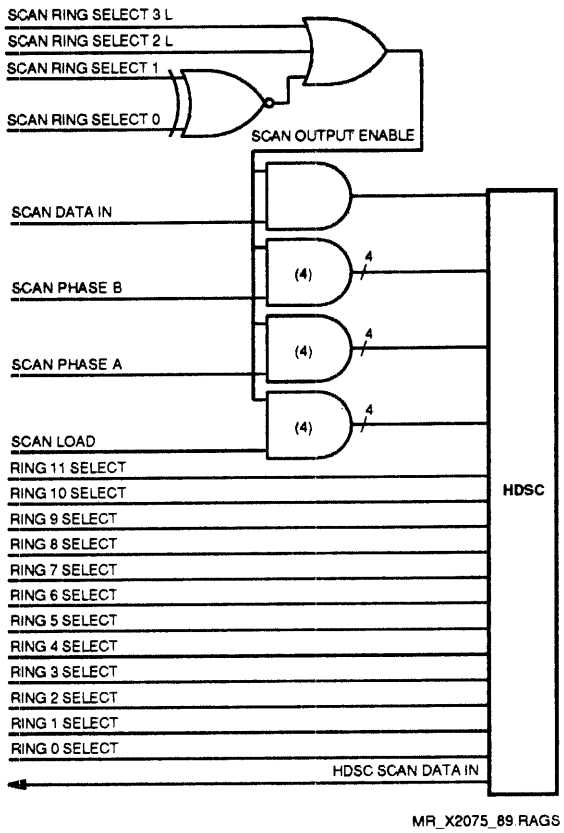


Figure 3–10 CDXX-to-HDSC Scan Signals

3.2.5 CDXX Control Registers

The CDXX contains three control registers:

HOT control register
Exception control register
Clock check control register

Each of these registers is loaded from scan ring 13 and read through scan ring 14. Each register includes a write-enable bit. To load the registers, the data and write-enable bits are set in scan ring 13, shifted in, and scan ring 13 is loaded. The combination of the write enable and scan ring 13 load signal, enables the register data to be loaded. As soon as the transfer is complete, and the scan ring 13 load signal is deasserted, write enable is deasserted. This prevents any change in register data until scan ring 13 is again loaded with the appropriate write bit(s) set.

The registers are described in Sections 3.2.5.2 through 3.2.5.3.

3.2.5.1 CDXX Exception Control Register

This 2-bit register (Figure 3–11 and Table 3–6) enables HDSC exception condition reporting. Section 3.2.6.1 describes exception condition reporting.

The register is loaded from scan ring 13, and its status is reported through scan ring 14.

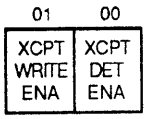


Figure 3–11 CDXX Exception Control Register Format

Table 3–6 CDXX Exception Control Register Bit Description

Bits	Mnemonic	Description
01	XCPT WRITE ENA	This is scan ring 13 bit 3. When set, it write-enables bit 0.
00	XCPT DET ENA	When set, enables latched exception condition reporting. This bit is loaded from scan ring 13 bit 2 when bit 1 is set, and is read through scan ring 14 bit 2.

3.2.5.2 CDXX HOT Control Register

This 10-bit register (Figure 3–12 and Table 3–7) enables HDSC overtemperature condition reporting and sets the overtemperature trip temperature, that is, the HDSC temperature that is above normal. Section 3.2.6.2 describes exception condition reporting.

The register is loaded from scan ring 13, and its status is reported through scan ring 14.

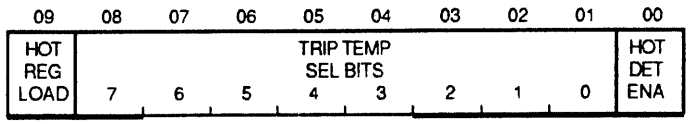


Figure 3–12 CDXX HOT Control Register Format

Table 3–7 CDXX HOT Control Register Bit Description

Bits	Mnemonic	Description
09	HOT REG LOAD	This is scan ring 13 bit 13. When set, it write-enables bits [08:00].
08:01	TRIP TEMP SEL BITS [7:0]	The coded value in these bits sets the bias voltage on the overtemperature detector. These bits are loaded from scan ring 13 [12:05] when bit 9 is set. These bits are read through scan ring 14 [13:06].
00	HOT DET ENA	When set, enables HOT exception condition reporting. This bit is loaded from scan ring 13 bit 4 when bit 9 is set, and is read through scan ring 14 bit 5.

3.2.5.3 CDXX Clock Check Control Register

This 2-bit register (Figure 3–13 and Table 3–8) enables clock synchronization error reporting. The clock check logic is described in Section 3.2.6.3.

The register is loaded from scan ring 13, and its status is reported through scan ring 14.

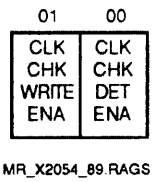


Figure 3–13 CDXX Clock Check Control Register Format

Table 3–8 CDXX Clock Check Control Register Bit Description

Bits	Mnemonic	Description
01	CLK CHK WRITE ENA	When set, write-enables bit 0. This bit is loaded from scan ring 13 bit 1.
00	CLK CHK DET ENA	When set, enables clock system failure exception condition reporting. This bit is loaded from scan ring 13 bit 0 when bit 1 is set. This bit is read through scan ring 14 bit 0.

3.2.6 Exception Condition Reporting

The CDXX reports three types of errors, or exception conditions:

HDSC errors (latched)
HDSC overtemperature (HOT)
Clock synchronization (clock check)

As Figure 3–14 shows, each condition must be enabled to be reported.

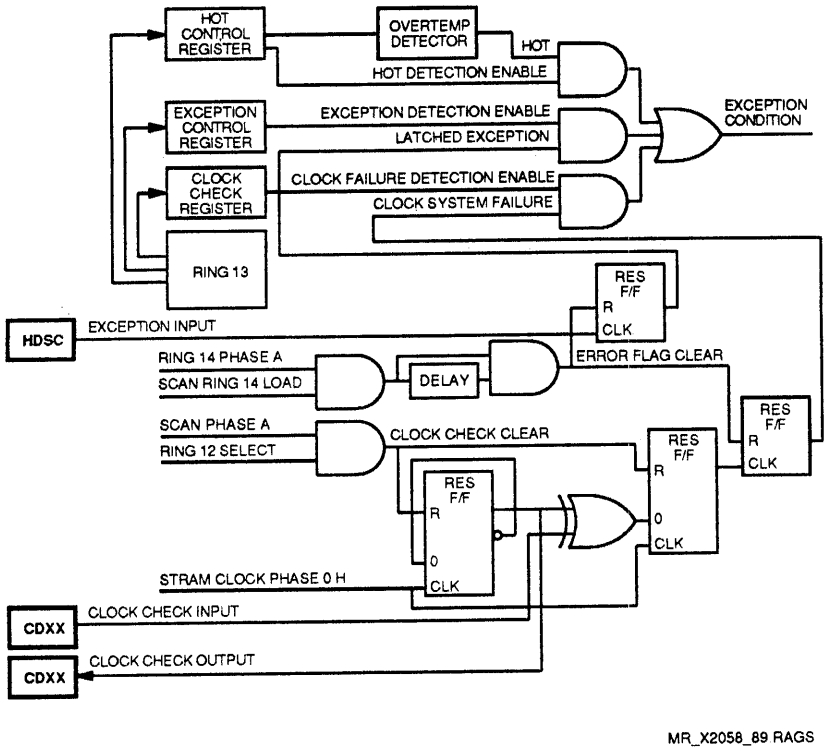


Figure 3–14 CDXX Exception Condition Logic

3.2.6.1 HDSC Errors (Latched Exceptions)

HDSC errors assert EXCEPTION INPUT and are enabled by the exception control register (Section 3.2.5.1). When an error occurs, it is latched and asserts LATCHED EXCEPTION. The error status is reported in scan ring 14, and if enabled, the exception condition is reported when the scan bus is in the no-op state (Section 3.2.4). The latched exception condition is cleared when scan ring 14 is read.

3.2.6.2 HDSC Overtemperature Errors

HDSC overtemperature, or HOT, errors are detected in the CDXX by the overtemperature detector. The detector includes a programmable DAC for setting the temperature at which an overtemperature condition is detected. This detection, or trip temperature, is determined by the value in HOT control register bits [07:00], which controls the bias on the DAC.

If an overtemperature condition occurs, the error status is reported in scan ring 14, and if enabled, the exception condition is reported when the scan bus is in the no-op state (Section 3.2.4).

4
Clock Subsystem Physical Description

This chapter describes the physical characteristics of the clock subsystem components.

4.1 MCM Physical Description

The MCM (Figure 1–1) is a self-contained, air-cooled assembly mounted in the SCU cabinet. The frequency synthesizer and MCLK and RCLK power dividers are contained in separate subassemblies. The module's overall dimensions are as follows:

Height	47.00 cm (18.50 in)
Width	13.21 cm (5.20 in)
Depth	26.94 cm (10.60 in)

Two versions of the MCM assembly are shown in Figures 4–1 and 4–2. The major differences are the front panel connectors and the power dividers. The quad CPU version (Figure 4–1) uses 1:20 power dividers, while the dual CPU version (Figure 4–2) uses 1:12 power dividers.

4.2 Clock Subsystem Cables

All external signals are connected to the MCM on the front connector panel (Figures 4–1 and 4–2). Table 4–1 lists connectors and signals.

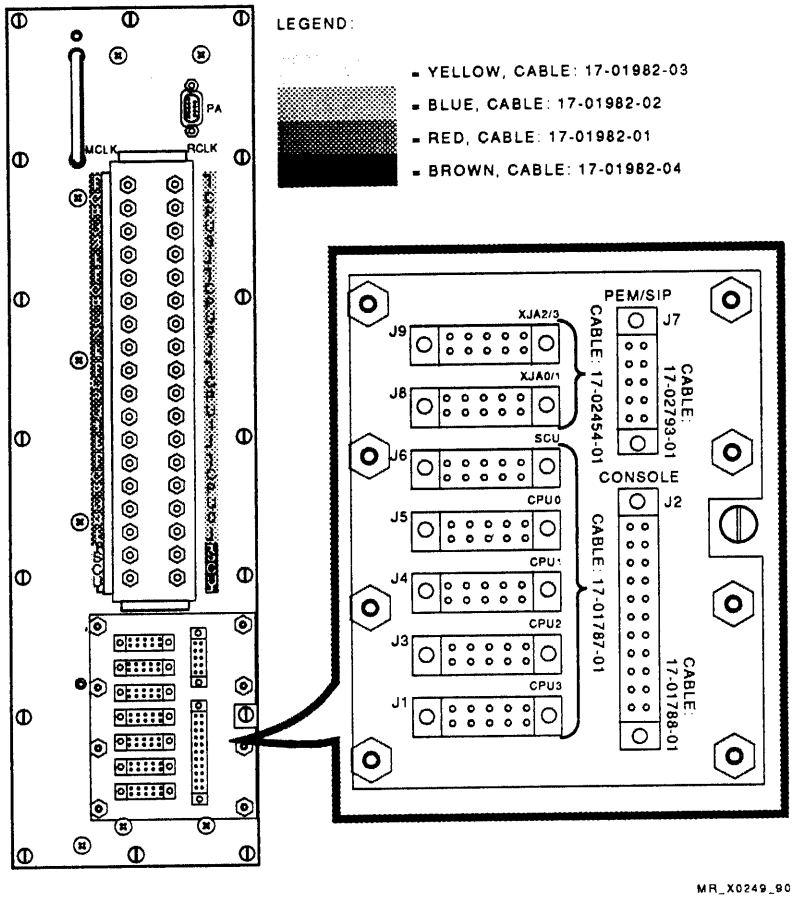


Figure 4–1 MCM Quad CPU Front Panel

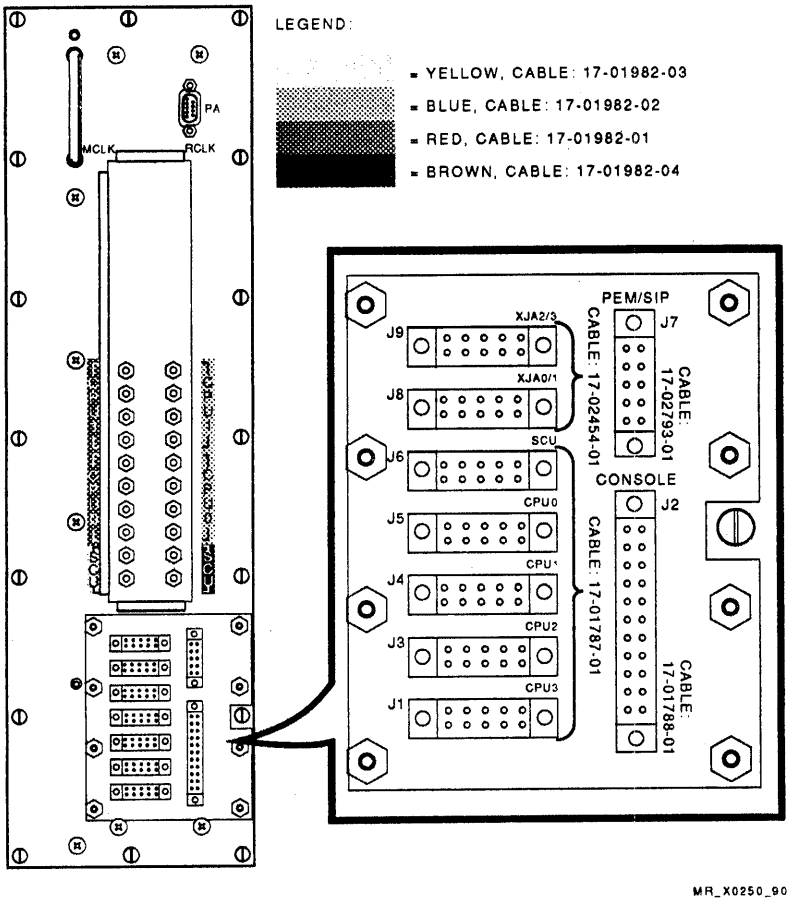


Figure 4–2 MCM Dual CPU Front Panel

Table 4–1 Clock Subsystem Cables

Connector	To/From	Signal
J1	CPU3	Clock control lines A through D
J2	SPU	SPU-to-MCM data and data transfer control signals
J3	CPU2	Clock control lines A through D
J4	CPU1	Clock control lines A through D
J5	CPU0	Clock control lines A through D
J6	SCU	Clock control lines
J7	SIP	Clock control lines A through D
J8	XJA1	RCLK shifted
J9	XJA0	RCLK shifted
J12	SCU	MCLK
J13		RCLK
J14		MCLK
J15		RCLK
J16	CPU0	MCLK
J17		RCLK
J18		MCLK
J19		RCLK
J20		MCLK
J21		RCLK
J22		MCLK
J23		RCLK
J24	CPU1	MCLK
J25		RCLK
J26		MCLK
J27		RCLK
J28		MCLK
J29		RCLK
J30		MCLK
J31		RCLK
J32	CPU2	MCLK
J33		RCLK
J34		MCLK
J35		RCLK
J36		MCLK
J37		RCLK
J38		MCLK
J39		RCLK
J40	CPU3	MCLK
J41		RCLK
J42		MCLK
J43		RCLK
J44		MCLK
J45		RCLK
J46		MCLK
J47		RCLK

4.3 Clock Subsystem FRUs

The clock subsystem field replaceable units (FRUs) are listed in Table 4–2.

Table 4–2 Clock Subsystem FRUs

Part Number	Description
70-25847-01	Master clock module with 1:20 power dividers
70-25847-02	Master clock module with 1:12 power dividers
17-01982-01	CPU clock cable, flexible coax, MCLK (red)
17-01982-02	CPU clock cable, flexible coax, RCLK (blue)
17-01982-03	SCU clock cable, flexible coax, MCLK (yellow)
17-01982-04	SCU clock cable, flexible coax, RCLK (brown)
17-01787-01	CPU/SCU clock control cable
17-01788-01	SPU data/control cable
17-02454-01	XJA clock cable
17-02793-01	SIP clock control cable
12-31516-01	SMA 50-Ohm terminator

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