DataGeneral

TECHNICAL STATEMENT

TEXT LISTING

068-000269-03

PROGRAM

ECLIPSE MAP DIAGNOSTIC, PART B

TEXT TAPE

097-000269-03

ABSTRACT

THIS IS THE SECOND OF 2 PROGRAMS (EMAPA,EMAPB) DESIGNED TO VERIFY THE OPERATION OF THE MEMORY ALLOCATION AND PROTECTION (MAP) FEATURE.

```
 0001 EMAPB    MACRO REV 06.30          14:32:24 02/14/79
01
02
03
04
05                      ;*************************************************************
06                      ;
07                      ; NAME: EMAPB.TX                      PART NUMBER: 097-000269
08                      ;
09                      ;
10                      ; DESCRIPTION: ECLIPSE MAP DIAGNOSTIC, PART B
11                      ;
12                      ;
13                      ; REVISION HISTORY:
14                      ;
15                      ;       REV.            DATE
16                      ;
17                      ;       00              04/11/75
18                      ;       01              11/07/75
19                      ;       02              08/06/76
20                      ;       03              12/31/76
21                      ;
22                      ; COPYRIGHT (C) DATA GENERAL CORPORATION, 1975, 1976
23                      ; ALL RIGHTS RESERVED.
24                      ;*************************************************************
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!0002 EMAPB
01                  ;
                            .TITLE  EMAPB
03                  ;
04                  ; ECLIPSE MEMORY PROTECTION AND MANAGMENT TEST
05                  ;       PART    2
```

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01
02              ;EMAPB
03              ;MAP DIAGNOSTIC- 2 OF 2
04              ;
05              ;THIS DIAGNOSTIC IS DESIGNED TO RUN IN AN
06              ;AUTO-LOAD AUTO-RUN ENVIRONMENT.
07              ;
08              ;1.0    ABSTRACT
09              ;
10              ;               THIS IS THE SECOND OF 2 PROGRAMS (EMAPA,EMAPB)
11              ;               DESIGNED TO VERIFY THE OPERATION OF THE MEMORY
12              ;               ALLOCATION AND PROTECTION (MAP) FEATURE.THIS
13              ;               PROGRAM WHICH TESTS MMPU SHOULD ONLY BE RUN AFTER
14              ;               SUCCESSFUL EXECUTION OF THE FIRST MAP DIAGNOSTIC.BOTH
15              ;               OF THESE PROGRAMS ARE PREREQUSITES TO THE
16              ;               MULTIPROGRAMMING AND  RELIABILITY TEST PROGRAM.
17              ;
18              ;
19              ;               A COMPLETE TEST REQUIRES THAT AN I/O TESTER
20              ;               AND A FPU BE PRESENT IN THE SYSTEM.
21              ;
22              ;
23              ;
24              ;2.0    MACHINE REQUIREMENTS
25              ;       2.1     ECLIPSE PROCESSOR WITH MAP OPTION.
26              ;       2.2     8K OF READ/WRITE MEMORY.
27              ;       2.3     TTY
28              ;       2.4     RTC (OPTIONAL)
29              ;       2.5     I/O TESTER (OPTIONAL)
30              ;       2.6     FPU (OPTIONAL
31              ;
32              ;
33              ;3.0    OPERATING PROCEDURE
34              ;       3.1     LOADING
35              ;               LOAD PROGRAM VIA THE BINARY LOADER.
36              ;       3.2     START ADDRESS
37              ;               SET SWITCHES TO 200 OCTAL.
38              ;               PRESS START.
39              ;               THE PROGRAM STARTS BY PRINTING OUT THE
40              ;               PROGRAM NAME AND REVISION NUMBER.  IF
41              ;               MAP FEATURE MMPU DOES NOT EXIST AND THE
42              ;               PROGRAM IS RUN IN AUTO MODE IT PRINTS
43              ;               A MESSAGE AND EXITS TO DTOS. IT
44              ;               THEN INFORMS THE OPERATOR OF THE EXISTENCE
45              ;               OF THE I/O TESTER AND THE FLOATING POINT
46              ;               UNIT. THIS IS FOLLOWED BY THE PHYSICAL
47              ;               NUMBER OF 1K MEMORY BLOCKS IN THE SYSTEM.
48              ;
49
50              ;       3.3     SWITCH SETTINGS
51              ;               SWITCH 0 (0) = USE CONTENTS OF "SWREG"
52              ;               SWITCH 0 (1) = USE DATA SWITCHES
53              ;               SWITCH 1 (1) = PROCEED FROM ERROR
54              ;               SWITCH 2 (1) = INHIBIT PRINTOUT TO TTO
55              ;               SWITCH 3 (1) = PRINT FAILURE RATE
56              ;               SWITCH 4 (1) = INHIBIT PRINTING PASS COUNT
57              ;               SWITCH 5 (1) = ENABLE PRINTOUT TO LPT
58              ;
59              ;               PLEASE NOTE THAT THE SELECTION TO USE THE
60              ;               DATA SWITCHES OR THE CONTENTS OF
```



```
01              ;               "SWREG" MAY BE MADE ONLY AT THE BEGINNING OF
02              ;               THE PROGRAM OR FOLLOWING AN ERROR HALT.
03              ;
04              ;       3.4     NORMAL OPERATION
05              ;               PROGRAM WILL EXECUTE ALL TESTS IN SEQUENCE
06              ;               AND AUTOMATICALLY LOOP.  IF SWITCH 4 IS CLEAR,
07              ;               A MESSAGE "PASS"  WILL BE PRINTED AT THE
08              ;               END OF EACH PASS ALONG WITH THE
09              ;               PASS COUNT IN DECIMAL.  IF SWITCH 4 IS SET,
10              ;               THE PASS COUNT WILL BE ACCUMULATED, BUT NOT
11              ;               PRINTED.
12              ;
13              ;
14              ;
15              ;4.0    ERROR DESCRIPTION
16              ;       4.1     NORMAL
17              ;               UPON THE DETECTION OF AN ERROR, THE PROGRAM
18              ;               WILL PRINT THE C/PC AND AC'S AND THEN LOOP.
19              ;               CONSULT THE LISTING FOR A TEST DESCRIPTION.
20              ;               SET THE SWITCHES TO CONTINUE.
21              ;
22              ;       4.2     ABNORMAL
23              ;               THERE ARE SEVERAL TYPES OF UNEXPECTED FAILURES
24              ;               WHICH WILL CAUSE A PROGRAM HALT.  THEY ARE AS
25              ;               FOLLOWS:
26              ;                       UNEXPECTED INTERRUPT
27              ;                       STACK OVERFLOW OR UNDERFLOW
28              ;               THE CAUSE OF ANY OF THESE FAILURES SHOULD BE
29              ;               CORRECTED BEFORE RESUMING TESTING.
30              ;
31              ;       4.3     MAP DATA
32              ;               THE CONTENTS OF THE USER AND DCH MAPS
33              ;               MAY BE PRINTED ON THE TTY/CRT FOR
34              ;               VISUAL ANALYSIS BY SETTING THE
35              ;               SWITCHES TO OCTAL 206 AND PRESSING START.
36              ;
37              ;
38              ;5.0    PROGRAM DESCRIPTION
39              ;       5.1     COMMON SUBROUTINE CALLS
40              ;               THE DIAGNOSTIC IS COMPRISED OF A SERIES OF
41              ;               SHORT TESTS.  BASICALLY, EACH TEST CONSISTS
42              ;               OF A SETUP PROCEDURE, ONE OR MORE EVALUATING
43              ;               CASES WITH ERROR CALLS, AND A LOOP CAPABILITY.
44              ;               EACH PARTICULAR TEST CASE IS DESCRIBED IN THE
45              ;               LISTING.  THE COMMON ROUTINES FOR SETUP (SETUP),
46              ;               ERROR CALLS (EHALT), AND LOOP (LOOP) ARE
47              ;               DESCRIBED HERE,ALONG WITH OTHER COMMONLY
48              ;               CALLED ROUTINES.
49              ;
50              ;
51              ;               SETUP
52              ;               EACH TEST BEGINS WITH A CALL TO SETUP.  THIS
53              ;               ROUTINE ISSUES AN IORST, SETS UP THE LOOP ADDRESS,
54              ;               RESETS CERTAIN ERROR SWITCHES AND ITERATION
55              ;               COUNTS.  IT ALSO STORES AN ADDRESS OF 60 INTO
56              ;               LOCATIONS 0,1,2,3 AND 45.  LOC 60 IS SET AS A
57              ;               JMP INDIRECT TO LOC 61.  LOC 61 CONTAINS AN
58              ;               ADDRESS WITHIN THE TEST WHICH POINTS TO SETUP+1.
59              ;               THE USER STACK AND VECTOR STACKS ARE ALSO
60              ;               INITIALIZED.
```

```
01                ;
```



```
01                ;
02                ;       EHALT
03                ;       THIS ROUTINE IS CALLED WHEN AN ERROR IS
04                ;       DETECTED.  SOMETIMES AN ERROR MIGHT OCCUR
05                ;       WITH USER MODE ENABLED.  FOR THIS REASON,
06                ;       UPON ENTRY INTO EHALT, AN SCL IS EXECUTED
07                ;       TO REMOVE USER MODE.  THE ROUTINE WILL THEN
08                ;       PROCEED TO HALT.  THIS ROUTINE WILL ALSO
09                ;       INTERROGATE ERROR SWITCHES AND PRINT ERROR DATA.
10                ;
11                ;       LOOP
12                ;       THIS ROUTINE IS CALLED AT THE END OF EACH TEST
13                ;       SEQUENCE.  IT IS USED TO ITERATE THE SEQUENCE
14                ;       100 TIMES IF NO ERROR HAS BEEN DETECTED.
15                ;       IF AN ERROR HAS BEEN DETECTED, IT IS USED TO
16                ;       MAINTAIN THE SCOPE LOOP AND INTERROGATE THE
17                ;       SWITCHES, ETC. THE USER STACK AND VECTOR STACK
18                ;       ARE ALSO INITIALIZED.
19                ;
20                ;
21                ;       LEPAB
22                ;       MAP ALL OF MEMORY TO
23                ;       LOGICAL = PHYSICAL
24                ;
25                ;       SULMP
26                ;       SET UP THE AC'S FOR A LMP INSTRUCTION
27                ;       AS PER THE WORDS FOLLOWING THE CALL.
28                ;       WORD 1 = AC0     WORD 2 = AC1
29                ;       WORD 3 = AC2     WORD 4 = AC3
30                ;
31                ;       SETDONE
32                ;       THE DONE FLOP IS SET IN ONE OF
33                ;       THE FOLLOWING DEVICES:
34                ;       RTC, I/O TESTER OR TTY/CRT.
35                ;
36                ;       SUMAP
37                ;       A BLOCK OF MEMORY IS SET UP TO DO A BLOCK
38                ;       LOAD OF THE MAP VIA A LMP.  THE CALL
39                ;       IS FOLLOWED BY 3 PAIRS OF TWO WORDS.  THE
40                ;       FIRST WORD IN EACH PAIR IDENTIFIES WHICH
41                ;       MAP:
42                ;       400 = OCH, 1000 = USER A, 1400 = USER B
43                ;       THE SECOND WORD IN EACH PAIR DENOTES
44                ;       HOW THAT MAP IS TO BE LOADED:
45                ;       0 = 0'S, 1 = 1'S, 2 = ADDRESS
46                ;
47                ;       RCBLK
48                ;       THIS ROUTINE IS USED FOLLOWING A BLOCK
49                ;       LOAD OF THE MAP BY A LMP TO READ
50                ;       BACK AND CHECK THE LOADED MAPS.
51                ;       AS DESCRIBED ABOVE FOR THE "SUMAP" ROUTINE,
52                ;       THE CALL IS FOLLOWED BY A USER SELECTION
53                ;       WORD AND A LOAD SPECIFIER.
54                ;
55                ;       SUIOMAP
56                ;       A BLOCK OF MEMORY IS SET UP FOR
57                ;       A LMP TO PERFORM A BLOCK LOAD
58                ;       OF DEVICE PROTECTION.  THE CALL IS
59                ;       FOLLOWED BY 2 FIVE WORD BLOCKS.
60                ;       THE FIRST WORD OF EACH 5 WORD BLOCK
```

```
0007 EMAPB
01              ;               SPECIFIES THE USER: 0 = USER A, 20000 = USER B.
02              ;               THE NEXT 4 WORDS IN EACH BLOCK SPECIFY
03              ;               THE DEVICE PROTECTION WHICH IS TO BE
04              ;               LOADED FOR THE SELECTED USER.
05              ;
06              ;
07              ;               IOCHK
08              ;               THIS ROUTINE IS USED FOLLOWING A
09              ;               BLOCK LOAD OF DEVICE PROTECTION IN
10              ;               THE MAP VIA LMP.  IT CREATES
11              ;               A 4 WORD BY 16 BIT MATRIX OF
12              ;               THE DEVICE PROTECTION IN THE MAP
13              ;               AND COMPARES THIS TO THE MATRIX
14              ;               OF THE ORIGINAL LOADED DEVICE PROTECTION
15              ;               WHICH HAS BEEN PREVIOUSLY SAVED.
16              ;               THE CALL IS FOLLOWED BY A ONE
17              ;               WORD USER IDENTIFICATION SPECIFIER:
18              ;               0 = USER A, 20000 = USER B.
19              ;
20              ;               TRAN
21              ;               IF NO ERROR EXISTS, A NEW
22              ;               RANDOM # IS RETURNED IN AC0.
23              ;               IF AN ERROR EXISTS, THE OLD
24              ;               # IS RE-CIRCULATED.
25              ;
26              ;               SPA1
27              ;               SET ALL DEVICE PROTECTION BITS
28              ;               FOR USER A = 1.
29              ;
30              ;               SPA0
31              ;               SET ALL DEVICE PROTECTION BITS
32              ;               FOR USER A = 0.
33              ;
34              ;               SPB1
35              ;               SET ALL DEVICE PROTECTION BITS
36              ;               FOR USER B = 1.
37              ;
38              ;               SPB0
39              ;               SET ALL DEVICE PROTECTION BITS
40              ;               FOR USER B = 0.
41              ;
42              ;               IOMAP
43              ;               THE DEVICE PROTECTION MAP FOR A
44              ;               SELECTED USER IS SET AS SPECIFIED
45              ;               BY THE 5 WORD INFORMATION BLOCK
46              ;               FOLLOWING THE CALL.
47              ;               WORD 1 = USER, 0 = USER A, 20000 = USER B.
48              ;               THE NEXT 4 WORDS SPECIFY THE CONTENTS
49              ;               OF THE DEVICE PROTECTION MAP FOR THAT USER.
50              ;
```

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0008 EMAPB
01              ;
02              ;       5.2     MONITOR LOCATIONS
03              ;
04              ;
05              ;               THE FOLLOWING LOCATIONS IN PAGE 0 MAY BE
06              ;               MONITORED/EXAMINED TO PROVIDE ADDITIONAL
07              ;               INFORMATION.
08              ;
09              ;               LOC 200         USED BY DTOS
10              ;               LOC 201         CURRENT TEST ADDRESS LOCATION
11              ;               LOC 202         STARTING ADDRESS FOR  PROGRAM
12              ;               LOC 203         PROGRAM PASS COUNT
13              ;               LOC 204         TEST ITERATION COUNT
14              ;
15              ;
16              ;       5.3     MEMORY MAP
17              ;
18              ;               UNLESS OTHERWISE SPECIFIED,MEMORY
19              ;               IS ALWAYS MAPPED TO ITSELF.THAT IS
20              ;               LOGICAL=PHYSICAL FOR USER A AND USER B.
21              ;
22              ;
23              ;
24              ;6.0    SEQUENCE OF TESTING
25              ;
26              ;               THE TESTING SEQUENCE FOR
27              ;               PROGRAM MAPB IS AS FOLLOWS:
28              ;
29              ;
30              ;               LEF TESTS
31              ;
32              ;               PC IS DEFINED/UNDEFINED TESTS
33              ;
34              ;               LMP TESTS
35              ;
36              ;               LOGICAL BLOCK SWITCHING
37              ;
38              ;               DATA CHANNEL
39              ;
40              ;               FLOATING POINT
41              ;
42              ;               MISCELLANEOUS TESTS
43              ;
44              ;
45              ;
46              ;
47              ;
48              ;
49              ;7.0    PROGRAMMING DESCRIPTION FOR MAP FEATURE
50              ;
51              ;               THE INSTRUCTIONS WHICH MAY BE
52              ;               USED TO SETUP AND INTERROGATE
53              ;               THE MAP FEATURE ARE BRIEFLY
54              ;               DESCRIBED HERE.
55              ;
56              ;               7.1     DOA INSTRUCTION
57              ;
58              ;                       THE DOA INSTRUCTION WITH THE FOLLOWING
59              ;                       FORMAT WILL DEFINE THE MAP FOR A
60              ;                       SINGLE 1K WORD BLOCK OF LOGICAL MEMORY.
```

BIT	CONTENTS
0	UNUSED
1-5	LOGICAL BLOCK NUMBER
6-7	MAP TYPE 01=DATA CHANNEL 10=USER A 11=USER B
8	WRITE PROTECT
9-15	PHYSICAL BLOCK NUMBER

THE DUA INSTRUCTION WITH THE FOLLOWING FORMAT WILL DEFINE THE I/O DEVICES WHICH ARE INACCESSIBLE TO THE USER.

BIT	CONTENTS
0	UNUSED
1	MUST BE 1
2	USER SELECTION 0=A, 1=B
3-5	DEVICE CLASS
6-7	MUST BE 00
8-15	DEVICE PROTECT BITS

THE DOA INSTRUCTION WITH THE FOLLOWING FORMAT DEFINES THE PROTECTION FEATURES THAT ARE TO BE ENABLED FOR A USER.

BIT	CONTENTS
0	UNUSED
1	MUST BE 0
2	USER SELECTION 0=A, 1=B
3-5	UNUSED
6-7	MUST BE 00
8	UNUSED
9	LEF MODE
10	I/O PROTECT
11	WRITE PROTECT
12	INDIRECT PROTECT
13	DATA CHANNEL PROTECT
14	DATA CHANNEL MAP ENABLE
15	USER MAP ENABLE

7.2 DOB INSTRUCTION

THE DOB INSTRUCTION MAY BE USED TO MAP SUPERVISOR BLOCK 31. BITS 9-15 OF THE SPECIFIED AC DENOTE A PHYSICAL BLOCK NUMBER TO WHICH LOGICAL 31 WILL BE MAPPED WHEN IN THE SUPERVISOR MODE.

7.3 DIA INSTRUCTION

THE DIA INSTRUCTION MAY BE USED TO READ INTO THE SPECIFIED AC THE STATUS OF THE LAST ENABLED USER.

BIT	CONTENTS
0-1	UNUSED
2	USER 0=A, 1=B
3-8	UNUSED
9	LEF
10	IO PROTECT
11	WRITE PROTECT
12	INDIRECT PROTECT
13	DATA CHANNEL PROTECT
14	DATA CHANNEL MAP ENABLE
15	USER MODE INTERRUPT

7.4 DIC INSTRUCTION

THE DIC INSTRUCTION MAY BE USED TO READ INTO THE SPECIFIED AC THE CONTENTS OF THE MAP STATUS REGISTER.

BIT CONTENTS

```
;                       0       DATA CHANNEL PROTECT ERROR
;                       1       ERROR  DURING MAP SINGLE CYCLE
;                       2       WRITE PROTECT ERROR
;                       3       VALIDITY PROTECT ERROR
;                       4       INDIRECT PROTECT ERROR
;                       5       I/O PROTECTION ERROR
;                       6       USER LAST ENABLED, 0=A, 1=B
;                       7       PC ON  STACK IS UNDEFINED
;                       8       WRITE PROTECT
;                       9-15    PHYSICAL BLOCK NUMBER WHICH
;                               CORRESPONDS TO THE
;                               LOGICAL PAGE NUMBER GIVEN IN THE
;                               LAST TRANSLATE BLOCK INSTRUCTION.
;
;
;
;               7.5     DOC INSTRUCTION
;
;                       THE DOC INSTRUCTION MAY BE USED TO
;                       TRANSLATE A LOGICAL BLOCK NUMBER TO
;                       ITS CORRESPONDING PHYSICAL BLOCK NUMBER.
;                       THE RESULT IS PLACED IN BITS 9-15 OF
;                       THE MAP STATUS REGISTER.
;
;                       BIT     CONTENTS
;
;                       0       UNUSED
;                       1-5     LOGICAL BLOCK NUMBER TO
;                               BE TRANSLATED
;                       6-7     00=NO TRANSLATION
;                               01=DCH MAP
;                               10=USER A
;                               11=USER B
;
;               7.6     MAP SINGLE CYCLE
;
;                       AN IO PULSE ISSUED TO THE MAP
;                       ALLOWS THE LAST USER MAP ENABLED
;                       TO BE MAPPED FOR ONE MEMORY REFERENCE.
;                       THE FIRST MEMORY REFERENCE AFTER
;                       THE NEXT LOAD OR STORE INSTRUCTION
;                       IS MAPPED.  AFTER THE MEMORY CYCLE
;                       IS MAPPED, THE USER MAP IS AGAIN
;                       DISABLED.
;
;
;
```



```
;
;               7.7     LEF INSTRUCTION
;
;                       IF THE LEF MODE BIT IN THE USER STATUS
;                       IS 1 FOR A USER, THEN ALL I/O
;                       INSTRUCTIONS ISSUED BY THAT USER
;                       WILL BE INTERPRETED AS LEF INSTRUCTIONS.
;                       THE LOGICAL EFFECTIVE ADDRESS IS
;                       COMPUTED FROM BITS 5-15 OF
;                       THE INSTRUCTION AND PLACED IN THE
;                       SPECIFIED AC.
;
;               7.8     LMP
;
;                       A BLOCK ADD AND MOVE  IS PERFORMED.
;                       THE RESULT IS LOADED INTO THE MAP
;                       FEATURE.  THE ACCUMULATORS ARE SET UP
;                       IN THE SAME MANNER AS THE BAM
;                       INSTRUCTION.  THE ONLY EXCEPTION IS THAT
;                       DATA IS NOT TRANSFERED TO THE
;                       DESTINATION ADDRESS AND AC3 IS
;                       UNUSED.
;
;                       ACCUMULATORS
;
;                       AC0 = ADDEND
;                       AC1 = NUMBER OF WORDS TO BE MOVED
;                       AC2 = SOURCE ADDRESS
;                       AC3 = DESTINATION ADDRESS (UNUSED)
;
;                       THE INFORMATION TO BE LOADED INTO
;                       THE MAP IS IN THREE FORMATS
;                       AS DESCRIBED IN SECTION 7.1,
;                       FOR THE DUA INSTRUCTION.
;
;
;
;
;8.0    I/O TESTER HARDWARE DESCRIPTION
;
;       8.1     TEST BOARD COMMANDS
;
;               IORST  -  CLEAR THE TESTER
;               NIOC 0 -  CLEAR THE TESTER (IF  NEW MODE)
;               INTA   -  READ THE DATA BUFFER (NOT NEW MODE)
;               DATIC  -  READ THE PULSE DETECTORS
;               DATIB  -  READ THE DATA BUFFER
;               DATIA  -  READ THE DCH ADDRESS BUFFER (NEW MODE)
;               DATOA  -  LOAD THE DATA BUFFER
;               DATOB  -  LOAD THE FUNCTION BUFFER
;               DATOC  -  LOAD THE DATA AND DCH ADDRESS BUFFERS
;
;       8.2     FUNCTION REGISTER BIT ASSIGNMENTS
;
;               BIT 0     SET DCH SYNC
;               BIT 1     SET DCH MODE0
;               BIT 2     SET DCH MODE1
;               BIT 3     SET PI SYNC
;               BIT 4     BUSY (IF NOT IN NEW MODE)
;               BIT 5     DONE (IF NOT IN NEW MODE)
```

```
01                ;               BIT 6     NEW MODE
02                ;               BITS 7-9  AN OCTAL # WHICH SPECIFIES THE
03                ;                         # OF RQENB PULSES BETWEEN
04                ;                         SUCCESSIVE DCH CYCLES. (NEW MODE ONLY)
05                ;                         NOTE THAT 0 SPECIFIES 1 RQENB PULSE.
06                ;               BITS 10-15  # OF DCH CYCLES TO BE RUN.
07                ;                         (NEW MODE ONLY)
08                ;                         NOTE THAT 0 SPECIFIES 1 DCH CYCLE.
09                ;
10                ;
11                ;
12                ;       8.3     PULSE DETECTOR BIT ASSIGNMENTS
13                ;
14                ;               BIT 0     IOPLS
15                ;               BIT 1     INTA (INTA AND DCHP)
16                ;               BIT 2     MSKO
17                ;               BIT 3     DCHI
18                ;               BIT 4     OVFLO
19                ;               BIT 5     DCHO
20                ;               BIT 6     DCHA
21                ;               BIT 7     RQENB (COMPLEMENTS WITH EACH PULSE)
22                ;               BIT 8     DATOA
23                ;               BIT 9     DATOB
24                ;               BIT 10    DATOC
25                ;               BIT 11    DATIA
26                ;               BIT 12    DATIB
27                ;               BIT 13    DATIC (NOT SET IF DEV CODE = 0)
28                ;               BIT 14    STRT
29                ;               BIT 15    CLR
30                ;
31                ;       8.4     TEST BOARD LOGIC
32                ;
33                ;               THE TEST BOARD CONTAINS 16 PULSE
34                ;               DETECTOR FLIP FLOPS.  THESE FF'S MAY
35                ;               BE READ BY A "DIC" WITH A DEVICE
36                ;               CODE OF 0.  THEY MAY BE CLEARED BY
37                ;               IORST OR NIOC 0 (IF IN NEW MODE).
38                ;               A PARTICULAR FF SETS WHENEVER
39                ;               A PULSE OCCURS ON THE LINE TO
40                ;               WHICH IT IS CONNECTED.
41                ;
42                ;               THE TEST BOARD ALSO CONTAINS
43                ;               A 16 BIT DATA BUFFER.  THIS
44                ;               BUFFER MAY BE LOADED/READ ETC.
45                ;               UNDER PROGRAM CONTROL.  THIS
46                ;               BUFFER IS ALSO USED FOR DCH
47                ;               OPERATIONS.  IT SHOULD BE NOTED THAT
48                ;               IN NEW MODE, ANY LOAD DATA BUFFER
49                ;               PROCEDURE, ACTUALLY LOADS THE
50                ;               EXCLUSIVE OR OF THE OUTPUT DATA
51                ;               AND THE DATA PREVIOUSLY STORED IN THE BUFFER.
52                ;
53                ;
54                ;               A 15 BIT DCH ADDRESS BUFFER
55                ;               IS USED TO DIRECT DCH REQUESTS
56                ;               TO ANY LOCATION IN/OUT OF MEMORY.
57                ;
58                ;
59
60                      .EOT
```



```
**00000 TOTAL ERRORS, 00000 PASS 1 ERRORS
```