DataGeneral

TECHNICAL STATEMENT

TEXT LISTING

068-000310-04

PROGRAM

WRITABLE CONTROL STORE
DIAGNOSTIC, PART C

TEXT TAPE

097-000310-04

ABSTRACT

THIS PROGRAM IS 3 OF 4 DESIGNED TO VERIFY THE OPERATION OF THE WRITABLE CONTROL STORE OPTION (WCS).

THIS PROGRAM SHOULD NOT BE RUN UNTIL ALL THE C.P. AND I/O TEST PROGRAMS HAVE BEEN SUCCESSFULLY EXECUTED.

```
 0001 WCSC  MACRO REV 06.20              14:32:26 08/30/77
01
02
03
04
05
06
07              ;*****************************************************************
08              ;
09              ; NAME: WCSC.TX                          PART NUMBER: 097-000310
10              ;
11              ;
12              ; DESCRIPTION: WRITABLE CONTROL STORE DIAGNOSTIC, PART C
13              ;
14              ;
15              ; REVISION HISTORY:
16              ;
17              ;       REV.            DATE
18              ;
19              ;       00              06/06/75
20              ;       01              12/19/75
21              ;       02              04/02/76
22              ;       03              08/06/76
23              ;       04              09/02/77
24              ;
25              ;
26              ; COPYRIGHT (C) DATA GENERAL CORPORATION, 1975, 1976, 1977
27              ; ALL RIGHTS RESERVED.
28              ;*****************************************************************
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!0002 WCSC
01              ;
                        .TITLE  WCSC
03              ;
04              ; ECLIPSE WRITABLE CONTROL STORE TEST
05              ;       PART    3
```

```
10003 WCSC
01
02                ;
03                ;EWCS
04                ;
05                ;
06                ;THIS DIAGNOSTIC IS DESIGNED TO RUN IN AN
07                ;AUTO-LOAD AUTO-RUN ENVIRONMENT.
08                ;
09                ;
10                ;1.0     ABSTRACT
11                ;
12                ;
13                ;
14                ;        THIS PROGRAM IS 1 OF 4  DESIGNED TO VERIFY THE
15                ;        OPERATION OF THE WRITABLE CONTROL STORE OPTION (WCS).
16                ;
17                ;
18                ;        THIS PROGRAM SHOULD NOT BE RUN UNTIL ALL THE C.P.
19                ;        AND I/O TEST PROGRAMS HAVE BEEN SUCCESSFULLY EXECUTED.
20                ;
21                ;
22                ;        THE LAST STEP IN THE TEST PROCEDURE SHOULD BE THE
23                ;        EXECUTION OF ALL THE WCS TEST PROGRAMS WITH THE
24                ;        CAT/KITTEN RUNNING IN THE BACKGROUND.
25                ;
26                ;
27                ;
28                ;
29                ;
```

```
10004 WCSC
01
02                ;
03                ;2.0     MACHINE REQUIREMENTS
04                ;
05                ;        2.1      ECLIPSE PROCESSOR ( WILL NOT RUN ON S130 )
06                ;        2.2      8K OF READ/WRITE MEMORY
07                ;        2.3      TTY OR CRT
08                ;        2.4      WCS OPTION IN PAGE 2
09                ;        2.5      I-O TESTER (OPTIONAL)
10                ;        2.6      FLOATING POINT UNIT (OPTIONAL)
11                ;
12                ;                 PLEASE NOTE THAT FOR A COMPLETE TEST,SUCH
13                ;                 AS IN FACTORY TEST,THE I-O TESTER AND THE
14                ;                 FLOATING POINT UNIT MUST BE IN THE SYSTEM.
15                ;
16                ;
17                ;
18                ;3.0     OPERATING PROCEDURE
19                ;
20                ;        3.1      LOADING
21                ;                 LOAD PROGRAM VIA THE BINARY LOADER.
22                ;        3.2      START ADDRESS
23                ;                 SET SWITCHES TO 200 OCTAL.
24                ;                 PRESS START.
25                ;                 THE PROGRAM STARTS OUT BY PRINTING THE
26                ;                 PROGRAM NAME AND REVISION NUMBER ALONG
27                ;                 WITH THE EXISTENCE OF THE I/O TESTER
28                ;                 AND/OR THE FLOATING POINT UNIT.
29                ;        3.3      SWITCH SETTINGS
30                ;                 SWITCH 0 (0) = USE CONTENTS OF SWREG"
31                ;                 SWITCH 0 (1) = USE DATA SWITCHES
32                ;                 SWITCH 1 (1) = PROCEED FROM ERROR
33                ;                 SWITCH 2 (1) = INHIBIT PRINTOUT TO TTY
34                ;                 SWITCH 3 (1) = PRINT FAILURE RATE,ALSO THE #
35                ;                                OF ITERATIONS FOR CURRENT TEST.
36                ;                 SWITCH 4 (1) = DO NOT PRINT PASS MESSAGE AT
37                ;                                 END OF TEST.
38                ;                 SWITCH 5 (1) = ENABLE PRINTOUT TO LPT
39                ;
40                ;                 PLEASE NOTE THAT THE OPTION TO USE THE
41                ;                 DATA SWITCHES OR THE CONTENTS OF "SWREG"
42                ;                 MAY ONLY BE EXERCISED AT THE BEGINNING OF
43                ;                 THE PROGRAM OR FOLLOWING AN ERROR HALT.
44                ;
45                ;        3.4      NORMAL OPERATION
46                ;                 PROGRAM WILL EXECUTE ALL TESTS IN SEQUENCE
47                ;                 AND AUTOMATICALLY LOOP.  IF SWITCH 4 IS RESET,
48                ;                 A MESSAGE "PASS XXXX" WILL BE PRINTED AT THE
49                ;                 END OF EACH PASS.  XXXX IS THE PASS COUNT
50                ;                 IN DECIMAL.  IF SWITCH 4 IS SET, THE
51                ;                 PASS COUNT WILL BE ACCUMULATED, BUT NOT
52                ;                 PRINTED.
53                ;
54                ;
55                ;
```

```
10005 WCSC
01
02              ;
03              ;4.0    ERROR DESCRIPTION
04              ;       4.1     NORMAL
05              ;               UPON THE DETECTION OF AN ERROR,THE CARRY,
06              ;               PC AND THE AC'S WILL BE PRINTED AND THEN
07              ;               THE PROGRAM WILL LOOP ON THE FAILING TEST.
08              ;               THE ADDRESS OF THE TEST FAILING IS
09              ;               CONTAINED IN LOCATION 201. CONSULT THE
10              ;               LISTING FOR A DETAILED TEST DESCRIPTION.
11              ;               AND SET THE DATA SWITCHES AS DESIRED.
12              ;       4.2     ABNORMAL
13              ;               THERE ARE SEVERAL TYPES OF UNEXPECTED FAILURES
14              ;               WHICH WILL CAUSE A PROGRAM HALT.  THEY ARE AS
15              ;               FOLLOWS:
16              ;                       UNEXPECTED INTERRUPT
17              ;                       STACK OVERFLOW OR UNDERFLOW
18              ;               THE CAUSE OF ANY OF THESE FAILURES SHOULD BE
19              ;               CORRECTED BEFORE RESUMING TESTING.
20              ;
21              ;5.0    PROGRAM DESCRIPTION
22              ;               5.1 COMMON SUBROUTINE CALLS
23              ;               THE DIAGNOSTIC IS COMPRISED OF A SERIES OF
24              ;               SHORT TESTS.  BASICALLY, EACH TEST CONSISTS
25              ;               OF A SETUP PROCEDURE, ONE OR MORE EVALUATING
26              ;               CASES WITH ERROR CALLS, AND A LOOP CAPABILITY.
27              ;               EACH PARTICULAR TEST CASE IS DESCRIBED IN THE
28              ;               LISTING.  THE COMMON ROUTINES FOR SETUP (SETUP),
29              ;               ERROR CALLS (EHALT), AND LOOP (LOOP) ARE
30              ;               DESCRIBED HERE ALONG WITH OTHER COMMONLY
31              ;               USED ROUTINES.
32              ;
33              ;
34              ;               SETUP
35              ;               EACH TEST BEGINS WITH A CALL TO SETUP.  THIS
36              ;               ROUTINE  SETS  THE LOOP ADDRESS,
37              ;               RESETS CERTAIN ERROR SWITCHES AND ITERATION
38              ;               COUNTS,AND INITIALIZES THE USER STACK.IT ALSO
39              ;               LOADS ALL OF WCS RAM WITH A ONE WORD MICRO
40              ;               ROUTINE WHICH  SIMPLY RETURNS TO XOP1+1.
41              ;
42              ;               EHALT
43              ;               THIS ROUTINE IS CALLED WHEN AN ERROR
44              ;               IS DETECTED.INITIALLY IT WILL CAUSE
45              ;               A PROGRAM HALT.IT WILL THEN PERFORM
46              ;               SPECIFIC FUNCTIONS AS SELECTED VIA
47              ;               THE SWITCH REGISTER.
48              ;
49              ;
50              ;               LOOP
51              ;               THIS ROUTINE IS CALLED AT THE END OF EACH TEST
52              ;               SEQUENCE.  IT IS USED TO ITERATE THE SEQUENCE
53              ;               10  TIMES IF NO ERROR HAS BEEN DETECTED.
54              ;               IF AN ERROR HAS BEEN DETECTED, IT IS USED TO
55              ;               MAINTAIN THE SCOPE LOOP AND INTERROGATE THE
56              ;               SWITCHES, ETC.  THE USER STACK
57              ;               IS   ALSO INITIALIZED.
58              ;
```

```
10006 WCSC
01              ;
02              ;
03              ;
04              ;       ARL
05              ;       LOAD EVERY LOCATION IN THE WCS RAM WITH THE
06              ;       MICRO-WORD THAT FOLLOWS THE CALL.
07              ;
08              ;       SRL
09              ;       LOAD ONE LOCATION IN THE WCS RAM WITH THE MICRO-WORD
10              ;       WHICH FOLLOWS THE CALL.THE LAST ENTRY IN THE
11              ;       MICRO-ORDER STRING DENOTES THE ADDRESS INTO WHICH
12              ;       THE MICRO-WORD WILL BE LOADED.
13              ;
14              ;E.G.   SRL AR PC ACS A1 F0 L N S N N N JUMP 0 10 0 377
15              ;
16              ;       THE SPECIFIED MICRO-WORD FOLLOWING THE SRL CALL
17              ;       WOULD BE LOADED INTO LOCATION 377 OCTAL IN  THE
18              ;       WCS RAM.
19              ;
20              ;
21              ;       DC1A0
22              ;       LOAD ALL DECODE 1 ADDRESSES=000.
23              ;
24              ;       DC1A1
25              ;       LOAD ALL DECODE 1 ADDRESSES=377.
26              ;
27              ;       DC2A0
28              ;       LOAD ALL DECODE 2 ADDRESSES=000.
29              ;
30              ;       DC2A1
31              ;       LOAD ALL DECODE 2 ADDRESSES=377.
32              ;
33              ;       LSDC1
34              ;       LOAD A SINGLE DEC1 RAM WITH A SPECIFIC ADDRESS.
35              ;       WORD1=WHICH DEC1 RAM LOCATION (0-17)
36              ;       WORD2=WHAT ADDRESS (0-377)
37              ;
38              ;
39              ;       LSDC2
40              ;       LOAD A SINGLE DEC2 RAM WITH A   SPECIFIC ADDRESS.
41              ;       WORD1=WHICH DEC2 RAM LOCATION (0-17).
42              ;       WORD2=WHAT ADDRESS (0-377)
43              ;
44              ;
45              ;       5.2 TEST DESCRIPTION
46              ;
47              ;       EACH TEST STARTS VIA A CALL SETUP TO INITIALIZE
48              ;       THE STATE OF THE C.P. AND TO LOAD ALL OF THE WCS RAM
49              ;       WITH A COMMON MICRO-WORD WHICH IF EXECUTED WOULD SIMPLY
50              ;       RETURN TO THE MAIN PROGRAM AT THE LOCATION SPECIFIED BY
51              ;       THE PC.THE AC'S ARE SET UP TO THEIR TEST VALUES,THE DEC1
52              ;       AND DEC2 ADDRESSES ARE LOADED  AS REQUIRED,AND A "TEST"
53              ;       MICRO-ROUTINE IS LOADED INTO THE WCS RAM.IN MOST CASES
54              ;       THIS "TEST" MICRO-ROUTINE STARTS AT LOCATION 0.AN XOP1
55              ;       IS THEN EXECUTED TO ENTER WCS.THE "TEST" MICRO-ROUTINE
56              ;       IS EXECUTED AND WCS IS EXITED.THE PROGRAM THEN CHECKS
57              ;       FOR EXPECTED RESULTS.
58              ;
59              ;       5.3 ERROR ANALYSIS
60              ;
```

```
                ;       WCS ENTRY ERROR
                ;
                ;       IF A DEC1 ADDRESSING ERROR OCCURS WHILE ATTEMPTING TO
                ;       ENTER WCS VIA AN XOP1 INSTRUCTION,THE PROGRAM WILL
                ;       PROBABLY EXECUTE ONE MICRO-INSTRUCTION IN WCS RAM
                ;       AND RETURN TO THE LOCATION OF THE XOP1+1.THE PROGRAM
                ;       MUST BE MICRO-INSTRUCTED STARTING AT THE XOP1
                ;       INSTRUCTION TO TRACE THE FAILING FLOW.
                ;
                ;       WCS EXIT ERROR
                ;
                ;       IF AN ERROR OCCURS IN AN ATTEMPT TO EXIT WCS,THE TEST
                ;       WOULD RETURN TO THE LOCATION SPECIFIED BY THE PC.
                ;
                ;
                ;
                ;       EXPECTED RESULTS INCORRECT
                ;
                ;
                ;       IF THE "TEST" MICRO-ROUTINE CAN BE EXECUTED IN WCS
                ;       AND A SUCCESSFUL EXIT IS MADE BACK TO THE TEST PROGRAM,
                ;       BUT THE  RESULTS ARE INCORRECT,THE "TEST"  MICRO-ROUTINE
                ;       MUST BE CAREFULLY EXAMINED TO DETERMINE
                ;       ITS PROPER EXECUTION.
                ;
                ;       THE FAILING SEQUENCE MAY BE SINGLE INSTRUCTED STARTING
                ;       AT THE POINT PRECEEDING THE XOP1 INSTRUCTION WHERE
                ;       THE AC'S ETC. ARE INITIALIZED UP TO BUT NOT INCLUDING
                ;       THE XOP1 INSTRUCTION.AT THE XOP1 INSTRUCTION,ONE MAY
                ;       MICRO INSTRUCT THROUGH THE XOP1,AND INTO WCS.NOTE THAT
                ;       THE PAGE BITS ON THE ROM ADDRESS LIGHTS WILL EQUAL 10
                ;       WHEN ENTRY TO PAGE 2 WCS IS MADE.THE TEST MICRO-ROUTINE
                ;       MAY THEN BE MICRO-INSTRUCTED.
                ;
                ;
                ;
                ;       5.4 MONITOR LOCATIONS
                ;
                ;       THE FOLLOWING LOCATIONS IN PAGE 0
                ;       MAY BE MONITORED/EXAMINED TO PROVIDE
                ;       ADDITIONAL INFORMATION.
                ;
                ;               LOC 200     USED BY DTOS
                ;       LOOPR   LOC 201     ADDRESS OF SETUP +1 OF
                ;                           LAST TEST ENTERED
                ;       ISTART  LOC 202     PROGRAM STARTING ADDRESS
                ;       PCNTR   LOC 203     PROGRAM PASS COUNT
                ;       ITRCT   LOC 204     ITERATION COUNT
                ;       IOTS    LOC 205     I/O TESTER SWITCH,0=NO
                ;       FPUS    LOC 206     FPU SWITCH,0=NO
                ;
                ;
                ;
                ;
000001          .DUSR   WCS=1
                ;
                ;6.0    PROGRAMMING DESCRIPTION FOR WCS FEATURE
                ;
                ;
                ;
```



```
                ;
                ;
                ;
                ;       6.1 XOP1 INSTRUCTION
                ;
                ;       XOP1 ACS,ACD,ENTRY NUMBER
                ;
                ;       WHEN AN XOP1 INSTRUCTION IS LOADED INTO THE IR BY
                ;       A LDIR OR NILDIR MICRO-ORDER, THE SUBSEQUENT
                ;       PHANTOM MICROINSTRUCTION HAS A DEC1 MICRO-ORDER
                ;       IN ITS STATE CHANGE FIELD, AND SPECIAL HARDWARE
                ;       FORCES THE SUCCEEDING MICROINSTRUCTION TO BE READ
                ;       FROM PAGE 2 (THE CONTROL STORE RAM).  SINCE DEC1
                ;       MAY YIELD A UNIQUE ADDRESS FOR EACH OF THE SIXTEEN
                ;       POTENTIAL ENTRY NUMBERS IN AN XOP1 INSTRUCTION,
                ;       EACH ENTRY NUMBER MAY SELECT THE BEGINNING OF A
                ;       DIFFERENT MICROROUTINE IN THE CONTROL STORE RAM.
                ;
                ;       INFORMATION IS LOADED INTO WCS BY THREE I/O IN-
                ;       STRUCTIONS.  THESE I/O INSTRUCTIONS MUST BE EX-
                ;       ECUTED IN PAIRS.  THE FIRST SPECIFIES WHERE INFORMA-
                ;       TION IS TO BE STORED IN WCS.  THE SECOND SENDS THE
                ;       INFORMATION (A DECODE ADDRESS OR A PART OF A MICRO-
                ;       INSTRUCTION) TO  WCS.
                ;
                ;       6.2 SPECIFY ADDRESS
                ;
                ;       DOA AC,WCS
                ;
                ;       THE CONTENTS OF THE SPECIFIED AC ARE TRANSFERRED
                ;       TO THE WCS ADDRESS REGISTER.  THE FORMAT OF THE
                ;       INFORMATION IN THE SPECIFIED AC IS DEPENDENT UPON
                ;       WHETHER THE USER IS TRANSFERRING DECODE ADDRESSES
                ;       OR MICROINSTRUCTIONS INTO WCS.  IF THIS SPECIFY
                ;       ADDRESS INSTRUCTION IS TO BE FOLLOWED BY A LOAD
                ;       MICROCODE INSTRUCTION, THE CONTENTS OF THE SPECI-
                ;       FIED AC ARE INTERPRETED AS FOLLOWS:
                ;
                ;       BITS CONTENTS
                ;
                ;       0-5     UNUSED
                ;       6-13    EIGHT-BIT ADDRESS SPECIFYING A
                ;               LOCATION IN PAGE 2 OF THE CONTROL
                ;               STORE TO BE LOADED BY THE FOLLOWING
                ;               LOAD MICROCODE INSTRUCION.
                ;       14-15   TWO-BIT SUBWORD SELECTOR SPECIFYING
                ;               WHICH OF THE 56 BITS IN THE
                ;               SPECIFIED LOCATION WILL BE LOADED
                ;               BY  THE FOLLOWING LOAD MICRO-CODE
                ;               INSTRUCTION.  SUBWORDS IN
                ;               A MICROINSTRUCTION ARE NUMBERED
                ;               AS FOLLOWS:  SUBWORD 0 IS BITS
                ;               0-15; SUBWORD 1 IS BITS 16-31;
                ;               SUBWORD 2 IS BITS 32-47; SUBWORD
                ;               3 IS BITS 48-55.
                ;
                ;       IF THE SPECIFY ADDRESS INSTRUCTION IS TO BE FOLLOWED
                ;       BY A LOAD DECODE ADDRESS INSTRUCTION,
                ;       THE CONTENTS OF THE SPECIFIED AC ARE INTERPRETED AS
                ;       FOLLOWS:
```

```
 0009 WCSC
01                ;
02                ;       BIT(S) CONTENTS
03                ;
04                ;       0-10    UNSUED
05                ;       11-14   ENTRY NUMBER = FROM BITS 6-9 OF
06                ;               THE CORRESPONDING XOP1 INSTRUCTION.
07                ;       15      DECODE NUMBER = 0 IF THE FOLLOWING
08                ;               LOAD DECODE ADDRESS
09                ;               INSTRUCTION SPECIFIES A
10                ;               DECODE 1 ADDRESS, 1 IF THE FOLLOWING
11                ;               LOAD DECODE ADDRESS
12                ;               INSTRUCTION SPECIFIES A
13                ;               DECODE 2 ADDRESS.
14                ;
15                ;       A SPECIFY ADDRESS INSTRUCTION STORES THE CONTENTS
16                ;       OF THE SPECIFIED AC IN THE WCS RAM-ADDRESS
17                ;       REGISTER UNTIL A SUBSEQUENT LOAD MICROCODE OR
18                ;       LOAD DECODE ADDRESS IS EXECUTED.  THE CON-
19                ;       TENTS OF THE AC REMAIN UNCHANGED.
20                ;
21                ;       6.3 LOAD MICROCODE
22                ;
23                ;       DOB AC,WCS
24                ;
25                ;       THE CONTENTS OF THE SPECIFIED AC ARE PLACED IN THE
26                ;       SUBWORD OF THE WCS CONTROL STORE RAM LOCATION SELECTED
27                ;       BY THE PREVIOUS SPECIFY ADDRESS INSTRUCION.
28                ;       IF THE SPECIFY ADDRESS INSTRUCTION HAS
29                ;       SELECTED SUBWORD 3 (BITS 48-55) OF THE CONTROL STORE
30                ;       LOCATION, ONLY BITS 0-7 OF THE AC ARE STORED.  THE
31                ;       CONTENTS OF THE AC REMAIN UNCHANGED.
32                ;
33                ;       6.4 LOAD DECODE ADDRESS
34                ;
35                ;       DOC AC,WCS
36                ;
37                ;       BITS 8-15 OF THE SPECIFIED AC ARE PLACED IN THE
38                ;       DECODE RAM IN THE WORD SPECIFIED BY THE PREVIOUS
39                ;       SPECIFY ADDRESS INSTRUCTION.  THE CONTENTS OF
40                ;       THE AC REMAIN UNCHANGED.
41                ;
42                ;       IT IS IMPORTANT TO REMEMBER THAT WCS SOMETIMES
43                ;       FUNCTIONS AS AN I/O DEVICE AND SOMETIMES FUNCTIONS
44                ;       AS A PART OF THE CPU.  FOR PURPOSES OF LOADING
45                ;       DECODE ADDRESSES AND MICROINSTRUCTIONS INTO WCS.
46                ;       IT IS AN I/O DEVICE (DEVICE SELECT CODE 01).  WHEN
47                ;       CPU OPERATION IS DETERMINED BY DECODE ADDRESSES
48                ;       AND MICROINSTRUCTIONS ALREADY STORED IN WCS, IT
49                ;       IS AN INTEGRAL PART OF THE CPU'S CONTROL LOGIC.
```

```
 0010 WCSC
01
02
03
04                ;7.0    ROM CONTROL WORD
05                ;
06                ;
07                ;
08                ;
09                ;       THE 56 BIT ROM CONTROL WORD IS DIVIDED
10                ;       INTO THE FOLLOWING FIELDS.
11                ;
12                ;       DESCRIPTION             BITS
13                ;
14                ;       A INPUT                 0-3
15                ;       A REG                   4-7
16                ;       B REG                   8-11
17                ;       ALU                     12-15
18                ;       SHIFT                   16-19
19                ;       LOAD                    20
20                ;       CRY                     21-22
21                ;       MA                      23
22                ;       MBUS                    24-25
23                ;       RAND1                   26-28
24                ;       RAND2                   29-31
25                ;       STATE CHANGE            32-37
26                ;       PAGE                    38-39
27                ;       TRUE ADDR.              40-47
28                ;       FALSE ADDRS.            48-55
29                ;
30                ;
31                ;
32                ;
33                ;
34                ;
35                ;
36                ;
37                ;8.0    MICRO-ORDERS
38                ;
39                ;
40                ;       THE VARIOUS MICRO-ORDERS IN EACH CONTROL FIELD ARE
41                ;       DESCRIBED HERE.
42                ;
43                ;
44                ;
45                ;
46                ;
47                ;       A INPUT FIELD OF ROM WORD
48
49        000000 .DUSR    AR=0    ;AREG<0-15> = A<0-15>
50        000001 .DUSR    IRD=1   ;IR<3-4> = A<14-15>,0'S = A<0-13>
51        000002 .DUSR    BIT=2   ;2(15-COUNT) = A<0-15>
52        000003 .DUSR    TRP=3   ;IR10 = A10,IR<5-9> = A<11-15>,0'S = A<0-9> (1)
53        000005 .DUSR    PL=5    ;PL ROM WORD ADDR. BY BREG<11-15> = A<0-15>
54        000010 .DUSR    LBY=10  ;AREG<8-15> = A<8-15>,0'S = A<0-7>
55        000011 .DUSR    IRS=11  ;IR<1-2> = A<14-15>,0'S = A<0-13>
56        000012 .DUSR    Z=12    ;0'S = A<0-15>
57        000013 .DUSR    CON=13  ;RBUF<40-47> = A<8-15>,0'S = A<0-7>
58        000014 .DUSR    SEX=14  ;AREG<8-15> = A<8-15>,IR8'S = A<0-7>
59        000016 .DUSR    CCN=16  ;RBUF<40-47> = A<8-15>,1'S = A<0-7>
60        000017 .DUSR    UBY=17  ;AREG<0-7> = A<0-7>,0'S = A<8-15>
```

```
0011 WCSC
01
02                ;       A REG/B REG FIELD OF ROM WORD
03
04        000000 .DUSR    ACS=0    ;ACS
05        000001 .DUSR    AD1=1    ;SELECT AC=ACD+1
06        000002 .DUSR    ACD=2    ;ACD
07        000004 .DUSR    GRS=4    ;GR SPECIFIED BY IR BITS 1-2.
08        000005 .DUSR    GD1=5    ;GR SPECIFIED BY IR BITS 3-4,+1.
09        000006 .DUSR    GRD=6    ;GR SPECIFIED BY IR BITS 3-4.
10        000010 .DUSR    AC0=10   ;AC0
11        000011 .DUSR    AC1=11   ;AC1
12        000012 .DUSR    AC2=12   ;AC2
13        000013 .DUSR    AC3=13   ;AC3
14        000014 .DUSR    GR0=14   ;GR 0
15        000015 .DUSR    GR1=15   ;GR 1
16        000016 .DUSR    GR2=16   ;GR 2
17        000017 .DUSR    GR3=17   ;(PC) GR 3
18        000017 .DUSR    PC=17    ;(GR3)
19
20
21
22
23
24                ;       ALU FIELD OF ROM WORD (2)
25                ;
26                ;
27                ;CIN=CARRY IN
28                ;C=COMPLEMENT
29                ;
30                ;
31
32        000000 .DUSR    A=0      ;A+CIN
33        000001 .DUSR    APB=1    ;A+B+CIN
34        000002 .DUSR    A1=2     ;A+1
35        000003 .DUSR    APCB=3   ;A+CB+CIN
36        000004 .DUSR    AM1=4    ;A-1+CIN
37        000005 .DUSR    APA=5    ;A+A+CIN
38        000006 .DUSR    APA1=6   ;A+A+1
39        000007 .DUSR    APB1=7   ;A+B+1
40        000010 .DUSR    AMB=10   ;A-B
41        000011 .DUSR    CA=11    ;CA
42        000012 .DUSR    AOB=12   ;A OR B
43        000013 .DUSR    AXB=13   ;A XOR B
44        000014 .DUSR    ANB=14   ;A AND B
45        000015 .DUSR    ANCB=15  ;A AND CB
46        000016 .DUSR    CANB=16  ;CA AND B
47        000017 .DUSR    ANBC=17  ;(A AND B)C
48
49                ;       SHIFT FIELD OF ROM WORD (3)
50
51        000000 .DUSR    F0=0     ;STRAIGHT,0-SHIFT0
52        000001 .DUSR    FC=1     ;STRAIGHT,CARRY-SHIFT0
53        000002 .DUSR    FI=2     ;STRAIGHT,ION-SHIFT0
54        000003 .DUSR    FA=3     ;STRAIGHT,ALL 16 BITS
55        000004 .DUSR    L0=4     ;LEFT,0-SHIFT15
56        000005 .DUSR    LL=5     ;LEFT,LINK-SHIFT15
57        000006 .DUSR    LQ=6     ;LEFT,QBIT-SHIFT15
58        000007 .DUSR    LC=7     ;LEFT,CRY ENAB-SHIFT15
59        000010 .DUSR    R0=10    ;RIGHT,0-SHIFT0
60        000011 .DUSR    RL=11    ;RIGHT,LINK-SHIFT0
```

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0012 WCSC
01        000012 .DUSR    RM=12    ;RIGHT,MULS CRY-SHIFT0
02        000013 .DUSR    RC=13    ;RIGHT,CRY ENAB-SHIFT0
03        000014 .DUSR    SW=14    ;SWAP BYTES
04
05
06                ;       LOAD FIELD OF ROM WORD
07
08        000001 .DUSR    L=1      ;SHIFT<0-15> - AREG<0-15> (4)
09
10
11                ;       CARRY FIELD OF ROM  WORD
12
13        000000 .DUSR    N=0      ;NO EFFECT
14        000001 .DUSR    SET=1    ;1 - CARRY
15        000002 .DUSR    CLR=2    ;0 - CARRY
16        000003 .DUSR    ALC=3    ;ENABLE ALC LOGIC
17
18
19                ;       MA FIELD OF ROM WORD
20
21        000001 .DUSR    S=1      ;ALU<1-15> - LA<1-15>,START MEMORY (5)
22
23                ;       MBUS FIELD OF ROM WORD
24
25
26        000001 .DUSR    RMOD=1   ;READ,NO RELEASE (6)
27        000002 .DUSR    WRIT=2   ;WRITE AND RELEASE
28        000003 .DUSR    READ=3   ;READ AND RELEASE
29
30                ;       RAND1 FIELD OF ROM WORD
31
32
33        000001 .DUSR    DCH=1    ;ALLOW DATA CHANNEL BREAK
34        000002 .DUSR    SCND=2   ;(QBIT XOR ALU0 SAVE XOR CRY0)C - QBIT,
35                                 ;ALU0 - ALU0 SAVE (7)
36        000003 .DUSR    IOTR=3   ;IO TRANSFER (6)
37        000004 .DUSR    IOPS=4   ;I/O PULSE (6)
38        000005 .DUSR    FPDA=5   ;FLOATING POINT DATA
39        000006 .DUSR    CNDA=6   ;CONSOLE DATA SWITCHES - MEM<0-15>
40        000007 .DUSR    STIR=7   ;MEM<0-15> - IR<0-15> (7)(8)
41
42
43
44
45
46                ;       RAND2 FIELD OF ROM WORD
47
48        000001 .DUSR    BMEM=1   ;BREG<0-15> - MEM<0-15>
49        000002 .DUSR    DECL=2   ;CARRY - CIN;SHIFT<12-15> - AREG<12-15>
50        000003 .DUSR    LCNT=3   ;ALU<12-15> - COUNT<12-15>
51        000004 .DUSR    PFL=4    ;SYSRST IF PWR FF=1
52        000005 .DUSR    IOFF=5   ;0 - ION
53        000006 .DUSR    CNIN=6   ;CONSOLE FUNCTION CODE - MEM<1-4> (6)
54        000007 .DUSR    LPST=7   ;LOAD PROCESSOR STATE
55
56
57                ;       STATE CHANGE FIELD OF ROM  WORD (9)
58
59        000000 .DUSR    LDIR=0           ;PHANTOM;MEM-IR,17-COUNT,1-QBIT,
60                                         ;0-ALU0 SAVE,0 - ION PEND (6)(10)
```

```
0013 WCSC
01        000001 .DUSR   DEC1=1          ;DECODE 1
02        000002 .DUSR   DEC2=2          ;DECODE 2
03        000003 .DUSR   JUMPSR=3        ;T;F=RREG SELECTED BY RBUF<27-28> (11)
04        000004 .DUSR   RTRN=4          ;RREG SELECTED BY RBUF <38-39>
05        000005 .DUSR   JUMP=5          ;T
06        000006 .DUSR   RTRNSR=6        ;RREG SELECTED BY RBUF<38-39>
07                                       ;F=RREG SEL. BY RBUF<27-28> (11)(12)
08        000007 .DUSR   NILDIR=7        ;PHANTOM;MEM=IR,17=COUNT,1=QBIT,
09                                       ;0=ALU0 SAVE,0=ION PEND (6)(13)
10        000010 .DUSR   ALU15=10        ;T IF ALU15=1,ELSE F
11        000011 .DUSR   ALU14=11        ;T  IF ALU14=1,ELSE F
12        000012 .DUSR   ALU12=12        ;T IF ALU12=1,ELSE FALSE
13        000013 .DUSR   ALU0=13         ;T IF ALU0=1,ELSE F
14        000014 .DUSR   CRY12B=14       ;F IF CRY12=1,ELSE T
15        000015 .DUSR   SCRY=15         ;T IF A0 XOR B0 XOR CRY0=1,ELSE F
16        000016 .DUSR   DCRY=16         ;T IF CRY12=1 OR ALU<12-15> >9,ELSE F
17        000017 .DUSR   CRY0B=17        ;F IF CRY0=1,ELSE T
18        000020 .DUSR   AUTIX=20        ;T IF 20 OCTAL < OR EQUAL ALU<1-15> OR
19                                       ;37 OCTAL < OR EQUAL,ELSE F
20        000021 .DUSR   IR5B01=21       ;F IF IR5=1,ELSE DECODE 1
21        000022 .DUSR   A0B01=22        ;F IF A0=1,ELSE DECODE1
22        000023 .DUSR   ACEQI=23        ;F IF IR<1-2>=IR<3-4>,ELSE T;
23                                       ;INCREMENT IR<1-2> (14)
24        000024 .DUSR   ACEQD=24        ;F IF IR<1-2>=IR<3-4>,ELSE T;
25                                       ;DECREMENT IR<1-2> (14)
26        000025 .DUSR   CNTND=25        ;T IF COUNT NOT = 0,ELSE F;DEC. COUNT
27        000026 .DUSR   LINK=26         ;T IF LINK = 1,ELSE F
28        000027 .DUSR   NC=27           ;F
29        000030 .DUSR   INTR=30         ;T IF INTERRUPT WAITING,ELSE F
30        000031 .DUSR   IOSKPB=31       ;F IF I/O SKIP TEST TRUE,ELSE T
31        000032 .DUSR   CONRQ=32        ;T IF CONSOLE SWITCH PRESSED,ELSE F
32        000033 .DUSR   LOCKB=33        ;F IF POWER SWITCH IN LOCK POS.,ELSE T
33        000034 .DUSR   QBIT=34         ;T IF QBIT = 1,ELSE F
34        000035 .DUSR   CARRY=35        ;T IF CARRY = 1,ELSE F
35        000036 .DUSR   A0=36           ;T IF A0=1,ELSE F
36        000037 .DUSR   ALUZ=37         ;T IF ALU<0-15> = 0,ELSE F
37        000040 .DUSR   FPTB=40         ;T IF FPP TRAP OR BUSY,ELSE F
38        000041 .DUSR   FPB=41          ;T IF FPP BUSY,ELSE F
39        000042 .DUSR   FPT=42          ;T IF FPP TRAP,ELSE F
40        000043 .DUSR   FPSK=43         ;T IF FPP SKIP,ELSE F
41        000044 .DUSR   EXC4=44
42        000045 .DUSR   EXC5=45
43        000046 .DUSR   EXC6=46
44        000047 .DUSR   EXC7=47
45                ;
46                ;
47                ;
48                ;       NOTES PERTAINING TO MICRO-ORDERS ABOVE.
49                ;
50                ;       1.COUNT MUST BE > 7
51                ;       2.CIN=(DECL AND CARRY)OR(ALC AND IR7)
52                ;       3.LINK MODIFIED BY LEFT AND RIGHT SHIFTS
53                ;       4.UNLESS ALC WITH IR12=1
54                ;       5.ALLOWS DCH BREAK UNLESS STIR OR SCND
55                ;       6.DO NOT ALLOW DCH BREAK
56                ;       7.DISABLE DCH BREAK
57                ;       8.DO NOT CODE WITH ACEQI OR ACEQD
58                ;       9.FALSE ADDRESS IS IN CURRENT PAGE,TRUE ADDRESS
59                ;         MAY CHANGE CURRENT PAGE
60                ;       10.INHIBITED BY HALT/STOP(IF RBUF55=0),INTERRUPT WAITING,
```

```
0014 WCSC
01                ;         OR REXAM
02                ;       11.CURRENT PAGE SAVED IN RETURN REGISTER (RREG)
03                ;         WITH FALSE ADDRESS
04                ;       12.DO NOT CODE RBUF<27-28> = RBUF <38-39>
05                ;       13.INHIBITED BY HALT/STOP (IF RBUF55=0)
06                ;         OR REXAM
07                ;       14.DO NOT CODE WITH STIR
08                ;
09                ;       FOR A COMPLETE DESCRIPTION OF THE MICRO-ORDERS,
10                ;       PLEASE CONSULT THE DATA GENERAL TECHNICAL
11                ;       REFERENCE ENTITLED "MICROPROGRAMMING WITH THE
12                ;       ECLIPSE COMPUTER WCS-FEATURE".(014-50-XX)
13                ;
14                ;
15                ;
16                ;
17                ;
18                ;
19
```

```
10015 WCSC
01                ;
02                ;
03                ;
04                ;9.0    I-O TESTER DESCRIPTION .
05                ;
06                ;
07                ;       9.1 TEST BOARD COMMANDS
08                ;
09                ;       IORST  - CLEAR THE TESTER
10                ;       NIOC 0 - CLEAR THE TESTER(NEW MODE)
11                ;       INTA   - READ THE DATA BUFFER (NOT NEW MODE)
12                ;       DIC    - READ THE PULSE DETECTORS
13                ;       DIB    - READ THE DATA BUFFER
14                ;       DIA    - READ THE DCH ADDRESS BUFFER (NEW MODE)
15                ;       DOA    - LOAD THE DATA BUFFER
16                ;       DOB    - LOAD THE FUNCTION BUFFER
17                ;       DOC    - LOAD THE DATA AND DCH ADDRESS BUFFERS
18                ;
19                ;
20                ;       9.2 FUNCTION REGISTER BIT ASSIGNMENTS
21                ;
22                ;       BIT 0           SET DCH SYNC
23                ;       BIT 1           SET DCH MODE0
24                ;       BIT 2           SET DCH MODE1
25                ;       BIT 3           SET P1 SYNC
26                ;       BIT 4           BUSY (IF NOT NEW MODE)
27                ;       BIT 5           DONE (IF NOT NEW MODE)
28                ;       BIT 6           NEW MODE
29                ;       BITS 7-9        THE # OF RQENB PULSES BETWEEN
30                ;                       SUCCESSIVE DCH CYCLES.
31                ;       BITS 10-15      # OF DCH CYCLES
32                ;
33                ;
34                ;       9.3 PULSE DETECTOR BIT ASSIGNMENTS
35                ;
36                ;
37                ;       BIT 0   IOPLS
38                ;       BIT 1   INTA (INTA + DCHP)
39                ;       BIT 2   MSKO
40                ;       BIT 3   DCHI
41                ;       BIT 4   OVFLO-NOT USED ON ECLIPSE
42                ;       BIT 5   DCHO
43                ;       BIT 6   DCHA
44                ;       BIT 7   RQENB
45                ;       BIT 8   DOA
46                ;       BIT 9   DOB
47                ;       BIT 10  DOC
48                ;       BIT 11  DIA
49                ;       BIT 12  DIB
50                ;       BIT 13  DIC (NOT SET IF DEV. CODE=0)
51                ;       BIT 14  STRT
52                ;       BIT 15  CLR
53                ;
54                ;
55                ;
56                ;       PLEASE NOTE THAT DCH PRIORITY MUST BE WIRED
57                ;       TO THE SLOT IN WHICH THE I-O TESTER IS RESIDENT.
58                ;       FAILURE TO DO THIS WILL CAUSE ERRORS WITH ANY
59                ;       TESTS WHICH ARE TESTING THE INTA PULSE DETECTOR
60                ;       AND/OR DATA CHANNEL.
```

```
 0016 WCSC
01                ;
02                ;
03                ;
04                ;
05                ;
06                ;
07                ;10.0   SOFTWARE DEBUGGING AIDS
08                ;
09                ;       DUE TO THE DIFFICULTY IN DYNAMICALLY CHECKING
10                ;       THE OUTPUTS OF THE RAMS,A SERIES OF SHORT
11                ;       DEBUGGING ROUTINES HAVE BEEN INCLUDED AT THE
12                ;       END OF THE TEST PROGRAM STARTING AT THE
13                ;       LOCATION TAGGED "AIDS".THESE ROUTINES MAY BE
14                ;       USED ALONG WITH THE MICRO-INSTRUCT
15                ;       CAPABILITY TO STATICALLY CHECK THE OUTPUT
16                ;       OF ANY RAM.
17                ;
18                ;
19                ;11.0   RUNNING WITH CAT/KITTEN
20                ;
21                ;       THE PROGRAM MAY BE EXECUTED WITH THE CAT/KITTEN IN THE
22                ;       BACKGROUND VIA PRECEEDING THE EDTOS COMMAND WITH THE
23                ;       LETTER "C",SUCH AS "CLOAD".
24                ;
25                ;       THE DEVICE CODE FOR WCS MAY BE ADDED TO THE EDTOS
26                ;       EQUIPMENT TABLE VIA AN  "ADD  -,1"  COMMAND.
27                ;
28                ;
29                ;
30                ;       IF THE CAT/KITTEN IS SELECTED,THE FIRST PASS WILL BE A
31                ;       NORMAL RUN,AND SUBSEQUENT PASSES WILL BE WITH THE
32                ;       CAT/KITTEN IN THE BACKGROUND.
33                ;
34                ;       IF AN ERROR OCCURS AFTER THE FIRST PASS,THE NORMAL
35                ;       ERROR INFORMATION WILL BE PRINTED,BUT NO HALT WILL
36                ;       OCCUR.THE PROGRAM WILL CONTINUE TESTING AS DIRECTED
37                ;       BY THE SETTING OF THE SWITCHES.
38                ;
39                ;       IF RESTART IS REQUIRED USE THE FOLLOWING
40                ;       SPECIAL RESTART LOCATIONS:
41                ;
42                ;       170     START WITHOUT CAT/KITTEN
43                ;       171     START WITH CAT/KITTEN
44                ;
45                ;       IN ALL CASES, A CAT/KITTEN RUN SHOULD NOT BE ATTEMPTED
46                ;       UNTIL THE PROGRAM EXECUTES SUCCESSFULLY IN
47                ;       NORMAL MODE.
48                ;
49                ;       WHEN RUNNING WITH THE  CAT/KITTEN , THE PROGRAM WILL
50                ;       PRINT IT'S NORMAL PASS MESSAGE AND THE
51                ;       CAT/KITTEN WILL PRINT THE LETTER "P" AS IT'S
52                ;       PASS MESSAGE.
53                ;
54                ;
55                ;       PLEASE NOTE THAT CERTAIN TESTS CANNOT BE EXECUTED WITH
56                ;       THE CAT/KITTEN SO THAT THESE TESTS WOULD BE EXECUTED
57                ;       DURING THE FIRST PASS AND BYPASSED DURING THE SECOND
58                ;       AND SUBSEQUENT PASSES.
59                ;
```

```
!0017 WCSC
01                ;
02                ; ************ MACRO DEFINITIONS ***************
03
04        000012 C=10.
05        000013 D=11.
06        000014 E=12.
07        000015 F=13.
08        000016 G=14.
09        000017 H=15.
10        000020 I=16.
11        000021 J=17.
12        000022 K=18.
13
14                .MACRO  MIUSTK
15                        IUSTK           ;INITIALIZE USER STACK
16                        ^1              ;FAULT ADDRESS TO ^1.
17                %
18                ;
19                ;
20                ;
21                ;
22                ;
23                .MACRO CLRA0            ;CLEAR AC'S,CRY=0
24                        SUB 0,0
25                        SUB 1,1
26                        SUB 2,2
27                        SUBO 3,3
28                %
29                .MACRO CLRA1            ;CLEAR AC'S,CRY=1'S
30                        ADC 0,0
31                        ADC 1,1
32                        ADC 2,2
33                        ADCO 3,3
34                %
35                ;
36                ;
37                ;
38                ;
39                ;
40                .MACRO ARL
41                **      GARL
42                **      (^1)B3+(^2)B7+(^3)B11+(^4)B15
43                **      (^5)B3+(^6)B4+(^7)B6+(^8)B7+(^9)B9+(^C)B12+(^D)B15
44                **      (^E)B5+(^F)B7+(^G)B15
45                **      (^H)B7
46                %
47                ;
48                ;
49                .MACRO SRL
50                **      GSRL
51                **      (^1)B3+(^2)B7+(^3)B11+(^4)B15
52                **      (^5)B3+(^6)B4+(^7)B6+(^8)B7+(^9)B9+(^C)B12+(^D)B15
53                **      (^E)B5+(^F)B7+(^G)B15
54                **      (^H)B7+(^I)B15
55                %
56                ;
57                .EOT
```

```
 0018 WCSC

**00000 TOTAL ERRORS, 00000 PASS 1 ERRORS
```

0019 WCSC

ARL	000024	MC	17/40
C	000012		17/04
CLRA0	000010	MC	17/23
CLRA1	000016	MC	17/29
D	000013		17/05
E	000014		17/06
F	000015		17/07
G	000016		17/08
H	000017		17/09
I	000020		17/10
J	000021		17/11
K	000022		17/12
MIUST	000000	MC	17/14
SRL	000043	MC	17/49