

**DataGeneral**

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**TECHNICAL  
STATEMENT**

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TEXT LISTING

068-001066-01

PROGRAM

ARRAY PROCESSOR EXERCISER-B

TAPE

097-001066-01

ABSTRACT

THIS PROGRAM IS A FUNCTIONAL TEST FOR THE ARRAY PROCESSOR (AP).  
IT IS EXECUTED BY A CENTRAL PROCESSOR (OR IOP) CONTROLLING THE  
AP AND TESTS SPECIFIC AP INSTRUCTIONS.

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0001 APB.T      MACRO REV 06.30      09:35:56 09/19/79
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NAME: APB.TX      PART NUMBER 097-1066
DESCRIPTION: ARRAY PROCESSOR EXERCISER-8.
REVISION HISTORY:
REV.      DATE
00      03/29/78
01      12/29/78
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APB.TX      PART NUMBER: 097-1066

PROGRAM NAME
SOURCE FILE:  APB.SR
DIOS FILE:   APB.EXER

REVISION HISTORY
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XX/XX/78    00

MACHINE REQUIREMENTS
1. ECLIPSE FAMILY CENTRAL PROCESSOR (HOST OR IOP)
   WITH AT LEAST 16-K READ/WRITE MEMORY
2. ARRAY PROCESSOR BOARDS AP1, AP2, AP3
3. BASIC I/O TELETYPE INTERFACE AND CONTROL

TEST REQUIREMENTS
1. SAME AS MACHINE REQUIREMENTS
2. I/O TESTER OR DISC
3. MMPU1

SUMMARY
THIS PROGRAM IS A FUNCTIONAL TEST FOR
THE ARRAY PROCESSOR (AP). IT IS EXECUTED BY
A CENTRAL PROCESSOR (OR IOP) CONTROLLING THE AP
AND TESTS SPECIFIC AP INSTRUCTIONS.

RESTRICTIONS
THE PROGRAM ASSUMES
- THE SYSTEM EXCLUDING THE AP IS ERROR FREE
- THE HOST COMPUTER AND MEMORY/MAP SYSTEMS ARE
  WORKING PROPERLY.
- THE 2-AP MAINTENANCE DIAGNOSTICS USING
  THE MAINTENANCE INSTRUCTION SET (MIS) HAVE
  SUCCESSFULLY RUN.

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01 PROGRAM DESCRIPTION/THEORY OF OPERATION
02 APXB TEST
03 INSTRUCTIONS TESTED:
04
05 ARS -- ADD REAL SCALAR TO REAL ARRAY
06 SRS -- SUBTRACT REAL SCALAR FROM REAL ARRAY
07 CMS -- COMPARE REAL SCALAR TO REAL ARRAY
08 MRS -- MULTIPLY REAL ARRAY BY REAL SCALAR
09 MCS -- MULTIPLY COMPLEX ARRAY BY COMPLEX SCALAR
10 SRW -- STORE REAL SCALAR FROM W-REG.
11 SCW -- STORE COMPLEX SCALAR FROM W-REG.
12
13 TEST DESCRIPTION
14
15 THE ARS AND SRS INSTRUCTIONS ARE TESTED USING THE
16 IDEA THAT WHEN A SCALAR WITH NO FRACTIONAL PART
17 IS ADDED TO A SEQUENTIAL ARRAY THE RESULT IS AN-
18 OTHER SEQUENTIAL ARRAY. THUS IF WE ADD 1.0 TO
19 A SEQUENTIAL ARRAY OF SA X, THEN THE RESULT WOULD
20 BE THE SEQUENTIAL ARRAY OF STARTING ADDRESS X + 2.
21 IN MAIN MEMORY, THIS CONCEPT IS USED SO THAT SIM-
22 ULATION CAN BE AVOIDED.
23
24 IN ARS AND SRS TESTS:
25 A) N IS VARIED => 20, 60, 200, 700, 1777
26 INDEX VALUE = 1.0
27 A => SCALAR = 1.0
28 THE DATA BASE IS SEQUENTIAL AT FDATA.
29 THE RESULT IN RAM IS COMPARED TO ARRAY
30 STARTING AT FDATA*2
31 B) THE SEQUENTIAL DATA, WHICH IS ALWAYS
32 LOADED TO RAM, IS RANDOMLY SLICED IN LOWER
33 RAM 1/2 AND THE OUTPUT DATA IS ALSO SENT
34 TO A RANDOM SLICE IN TOP HALF OF RAM. THIS
35 WILL TEST VARIOUS RANDOM INPUT/OUTPUT STARTING
36 ADDRESSES AND RANDOM N'S. THE RESULT IS COM-
37 PARED TO THE START ADDR*2 OF SOME RANDOM SLICE
38 OF FDATA ARRAY.
39
40 C) USING SAME DATA N IS SET AT 101.
41 IJ = 10, IK = 1.
42 THEN INDEXING IS REVERSED N=101
43 IK = 10, IJ = 1.
44 RESULTS ARE CHECKED AS IN PREVIOUS MANNER
45 D) FINALLY N, IJ, IK ARE VARIED RANDOMLY.
46 N RANGE IS 1-77, IJ => 1-17, IK=> 1-17.
47 RESULTS ARE CHECKED AS IN PREVIOUS MANNER.
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7.2.2 CMS IS TESTED USING SIMULATION OF INSTRUCTION, DO INSTRUCTION AND THEN COMPARE RESULTS METHOD. IN THIS SET OF TESTS EACH CMS OPERATOR GOES THROUGH THE SAME TEST. A DATA BASE OF SEQUENTIAL FLOATING POINT #'S IS GENERATED AT FDATA.

A) IN THIS TEST N IS VARIED FROM 2-2000 BY 2. THE SCALAR USED IS 100.0. THE SIMULATED OUTPUT ARRAY IS AT HDATA. THE AP RESULT GOES TO IDATA. THESE ARE COMPARED. NOTE THAT INDEX 0 OF THESE ARRAYS IS THE # OF ELEMENTS IN THE INPUT ARRAY THAT MET THE OP CODE REQUIREMENTS WITH THE GIVEN SCALAR. EACH CMS OP CODE IS TESTED IN THIS WAY, SU THAT NOT ONLY IS N SENSITIVITY TESTED BUT BASIC FUNCTIONALITY IS TESTED.

H) IN THE SECOND SET OF CMS TESTS. THE INPUT DATA, WHICH IS ALWAYS RELOADED TO AP RAM, IS SLICED RANDOMLY. THIS IS SENT THROUGH THE SIMULATOR AND THEN CHECKED AGAINST AP RESULTS. OUTPUTS ARE IN THE SAME PLACE AS IN PREVIOUS TEST. ALL OP CODES GO THROUGH THIS TEST.

ALSO "N" = 400.0

C) IN THIS SET OF TESTS N = 100, A = 400.0 BUT INDEX IS VARIED FROM 1 - 10. PROCEDURE, OTHERWISE, IS SAME AS ABOVE TESTS.

D) IN LAST TEST THE N IS VARIED RANDOMLY FROM 1-77, THE INDEX VARIES RANDOMLY FROM 1-17, AND THE OPERATION IS VARIED RANDOMLY. THE SCALAR IS 400.0 ALL RANDOM #'S ARE GENERATED, THE INSTRUCTION SIMULATED AND THEN THE AP IS EXERCISED. RESULTS ARE COMPARED IN THE STANDARD MANNER.

7.2.3 THE MRS INSTRUCTION IS TESTED BY FIRST CREATING BOTH INPUT AND OUTPUT DATA. THEN THE INSTRUCTION IS DONE. RESULTS ARE COMPARED

A DATA BASE OF SEQUENTIAL #'S IS GENERATED AT IDATA AND MULTIPLIED BY 2.5. THIS NEW ARRAY IS LOADED AT FDATA.

A) TEST #1 VARIES N FROM 2-1024. THE SCALAR A = 2.5. THE INPUT DATA IS LOADED AT LOC 0 IN AP RAM. OUTPUT DATA IS LOADED TO LOC 2000 AP RAM. THIS OUTPUT DATA IS COMPARED TO FDATA.

B) TEST #2 IS SIMILAR TO PREVIOUS RANDOM SLICE TEST. LOWER RAM WHERE INPUT DATA IS, IS SLICED RANDOMLY (I.E. RANDOM SA, RANDOM N) THE UPPER RAM, WHERE OUTPUT DATA IS, IS ALSO SLICED RANDOMLY. THIS RANDOM SLICE IS COMPARED TO THE CORRESPONDING CHECK DATA AT FDATA IN MM.

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C) TEST #3, #4 HAVE N=101, IJ=10, IK=1, OR IK=10 IJ=1. ALL OTHER ASPECTS OF TESTS ARE IDENTICAL TO PREVIOUS ONES.

D) FINAL TESTS VARIES N, IJ, IK RANDOMLY. INPUT DATA AT IJ=10 IS ONCE AGAIN LOADED TO RAM SA=0 OUTPUT IS ALWAYS TO SA=2000 IN AP RAM. N RANGE 1-77(8) IJ, IK 1-17(8) "A" = 2.5

MCS IS TEST IN SAME MANNER AS MRS EXCEPT ALL #'S ARE COMPLEX. THE SCALAR USED IS (2.5 + 1.0 I). SRW, SCW ARE TESTED USING OTHER AP INSTRUCTIONS IN APX8 TEST. THE SRW, SCW INSTRUCTIONS READ THE WREG AND STORE TO NM.

A) SRW TEST FIRST AN ARRAY OF RANDOM #'S IS BUILT AT FDATA. EACH OF THESE #'S IS USED AS THE SCALAR TO BE LOADED TO WREG VIA THE ARA INSTRUCTION. SRW IS THEN EXECUTED. THESE RESULTING # READ FROM WREG IS COMPARED TO THE ORIGINAL VIA RNCMP.

B) SCW TEST IS SIMILAR TO THE ABOVE TEST EXCEPT MSC IS USED TO LOAD A COMPLEX (64 BIT) # TO WREG. CNCMP IS USED FOR COMPARISON.

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S?MPD 8

SWITCH SETTINGS

8.1

LOCATION "SWREG" IS USED TO SELECT THE PROGRAM OPTIONS (NOT SYSTEM CONFIGURATION). WHILE RUNNING UNDER DTOS, THIS LOCATION WILL BE LOADED BY THE MONITOR. HOWEVER UNDER STAND ALONE AND PROGRAM LOAD MODES THIS LOCATION WILL BE SET ACCORDING TO THE ANSWERS SUPPLIED BY THE OPERATOR. IN ANY CASE THE OPTIONS CAN BE CHANGED OR VERIFIED BY USING ONE OF THE COMMANDS GIVEN IN SEC. 8.2

SWITCH OPTIONS DIFFERENT BITS AND THEIR INTERPRETATION AT LOCATION "SWREG" IS AS FOLLOWS:

BIT	OCTAL VALUE	BINARY VALUE	INTERPRETATION
1	40000	1	LOOP ON ERROR
2	20000	0	SKIP LOOPING ON ERROR
3	10000	1	PRINT TO CONSOLE
4	04000	1	ABORT PRINT OUT TO CONSOLE
5	02000	0	DO NOT PRINT % FAILURE
6	01000	1	PRINT % FAILURE
7	00400	1	ALLOW END OF PASS PRINT OUT
8	00200	1	SUPPRESS END OF PASS PRINT OUT

SWITCH COMMANDS

8.2

ONCE THE PROGRAM STARTS EXECUTING THE STATE OF ANY OF THE BITS CAN BE CHANGED BY HITTING KEYS 1-9, A-F. THE PROGRAM WILL CONTINUE RUNNING AFTER UPDATING THE OPTIONS. EACH KEY WILL COMPLETE THE STATE OF THE BIT AFFILIATED WITH IT, THUS BIT 4 CAN BE ALTERED BY HITTING KEY 4. SETTING OF ANY BIT OF LOCATION "SWREG" WILL SET BIT 0. (DEFAULT MODE IS DEFINED AS ALL BITS OF SWREG SET TO 0) THE PROGRAM CAN BE LOCKED INTO SWITCH MODIFICATION MODE BY TYPING A 0, IN WHICH CASE MORE THAN ONE BIT CAN BE CHANGED BEFORE CONTROL IS ALLOWED TO RETURN TO THE MAIN PROGRAM.

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? 8.2.1 OTHER COMMANDS  
"CR" A "RETURN" CAN BE TYPED TO CONTINUE THE PROGRAM  
AFTER ITS LOCKED IN A SWITCH MODIFICATION MODE  
"D THIS COMMAND GIVEN AT ANY TIME WILL RESET "SWREG"  
TO DEFAULT MODE AND RESTART THE PROGRAM.  
"R THIS COMMAND GIVEN AT ANY TIME WILL RESTART THE  
PROGRAM. SWITCHES ARE LEFT WITH THE VALUES THEY  
HAD BEFORE THE COMMAND WAS ISSUED.  
"O THIS COMMAND GIVEN AT ANY TIME WILL CAUSE THE  
PROGRAM CONTROL TO GO TO OOT (NOTE: THIS IS AN  
OPTIONAL COMMAND AND IS AVAILBLE ONLY IF  
OOTPK IS PRESENT)  
M THIS COMMAND GIVEN AT ANY TIME WILL PRINT THE  
CURRENT OPERATING MODES.

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? 9.0 OPERATING PROCEDURE/OPERATOR INPUT  
9.1 OPERATING PROCEDURE  
1. LOAD THE PROGRAM IN THE COMPUTER  
USING THE BINARY LOADER OR DTOS TAPE.  
2. SET SWITCHES TO ONE OF THE FOLLOWING:  
500,200 - RUN ALL TESTS  
501 - ARA,SRS INSTRUCTION TESTS  
502 - CMS INSTRUCTION TESTS  
503 - MRS,MCS INSTRUCTION TESTS  
504 - SRW,SCW INSTRUCTION TESTS  
3. PRESS START.  
4. THE PROGRAM PRINTS "PASS" FOLLOWING  
THE SUCCESSFUL COMPLETION OF THE TEST.

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110. ;  
; WHEN AN ERROR IS DETECTED A VALUE FOR AN  
; ERROR PC WILL BE PRINTED ALONG WITH AC'S 0,1 AND 2  
; OF THE HOST COMPUTER.  
; THE PC VALUE PRINTED MAY POINT TO ONE OF THE  
; FOLLOWING:  
; 1. A CALL TO EHALT  
; 2. A CALL TO THE ROUTINE WHICH DETECTED  
; THE ERROR AND SUBSEQUENTLY EXITED  
; TO EHALT SUCH AS THE VECTOR COMPARE  
; ROUTINES TCOMP,CCOMP,RCOMP, AND RCCMP.  
; SUBROUTINES OF THIS TYPE HAVE SPECIAL ERROR PRINTOUTS  
; CALLED IN THE ERROR ROUTINE. IN THE CASE OF THE REAL  
; VECTOR COMPARE ROUTINES, TCOMP AND RCCMP, UP TO 3  
; PAIRS OF GOOD/BAD DATA IS PRINTED IN 2-16, BIT HEX  
; OR OCTAL FORMAT (SEE SW10), ALONG WITH THE MM ADDRESS  
; OF THE DATA AND THE RELATIVE INDEX WITHIN THE VECTOR.  
; A TOTAL ERROR COUNT IS PRINTED ALONG WITH  
; THE VECTOR/VECTOR N,I,J,K DATA. IN THE CASE OF THE  
; COMPLEX VECTOR COMPARE ROUTINES, CCOMP AND RCCMP, THE  
; GOOD/BAD DATA IS PRINTED IN 4-16, BIT HEX OR OCTAL  
; FORMAT.  
; THE SIGNIFICANCE OF ERROR PRINTOUTS IS EXPLAINED IN THE  
; LISTING AT THE SOURCE OF THE ERROR. IN GENERAL  
; AC0 CONTAINS THE CHECKWORD AND AC1 THE DATA IN  
; QUESTION.  
; AFTER PRINTING THE ABOVE THE PROGRAM HALTS ALLOWING  
; THE OPERATOR TO SET THE SWITCHES. UPON PRESSING  
; CONTINUE THE PROGRAM MAY EITHER GO ON TO THE NEXT  
; TEST OR GO INTO A SCOPE LOOP BETWEEN THE APPROPRIATE  
; CALLS TO .SETUP AND .LOOP (SEE 6.0 SWITCH SETTINGS)

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11.0 ;  
; DEBUS HELP  
; 11.1 ; MONITOR LOCATIONS  
; ; LABEL  
; ; LOCATION  
; ; 200  
; ; 201  
; ; 202  
; ; 203  
; ; 204  
; ; MEANING  
; ; DTOS START  
; ; FIRST LOCATION OF CURRENT TEST  
; ; START ADDRESS  
; ; XXXX  
; ; PASS COUNT  
; ;  
; 11.2 ; PROGRAMMING DESCRIPTION  
; ; SEE PROGRAMMERS REFERENCE  
; ; FOR ARRAY PROCESSOR.

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11.3 COMMON SUBROUTINES
A) ADDSET,SETP,LOOP =
THESE ALL WORK IN CONJUNCTION TO
SET UP THE TEST LOOP.
ADDSET TELLS SETP WHERE THE LOOP ENDS.
SETP MARKS THE END OF THE TEST LOOP.
LOOP MARKS THE END OF THE TEST LOOP.
THE AP INSTRUCTION IS EXECUTED AND THE RESULTS ARE
CHECKED FOR ERROR WITHIN THIS TEST LOOP. IF AN ERROR
OCCURS, THEN THE PROGRAM CAN LOOP INDEFINITELY BETWEEN
THE SETP AND THE LOOP. (SEE SECTION 8 ON VARIOUS SWITCH
SETTINGS).
NORMALLY, WITH NO ERRORS, THE PROGRAM WILL GO THROUGH
THIS LOOP ONCE ON THE FIRST PASS OF THE PROGRAM. ON
SUBSEQUENT PASSES THE PROGRAM WILL STAY IN THE LOOP
FOR 5 LOOPS. (OR 100, DEPENDING ON THE PROGRAM).
B) PARAMETER BLOCK LOADER ROUTINES =
THESE CALLS ALL HAVE DIFFERENT NAMES DEPENDING ON THE
INSTRUCTION. HOWEVER THEY OPERATE IN THE SAME MANNER.
THE COMMENT FIELD ON THE CALL WILL ALWAYS INDICATE
THAT THIS IS A PARAMETER BLOCK LOAD ROUTINE AND WILL
NAME THE AP INSTRUCTION THAT THE LOAD IS COMPATIBLE WITH.
THE ARGUMENTS OF THE CALL ARE THE PARAMETERS OF THE AP
INSTRUCTION. THESE PARAMETERS ARE TO BE LOADED
BY THESE ROUTINES INTO MAIN MEMORY AT A LOCATION POINTED
TO BY AC2. AC2 MUST ALWAYS POINT TO THE PARAMETER BLOCK
DURING AP INSTRUCTION EXECUTION.
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C) SLICING ROUTINES =
THESE TYPES OF ROUTINES EXIST IN SEVERAL DIFFERENT FORMS.
THEY ALL HAVE VERY SIMILAR NAMES. FOR EXAMPLE - SLICE,
SLICC,SLICA,SLICR. THESE ARE ALL JSR'S TO SOME SLICING
ROUTINE.
THE SLICING ROUTINES WILL SET UP VARIOUS RANDOM
SLICES IN AP RAM FOR THE VARIOUS INPUT AND OUTPUT
ARRAYS USED IN THE AP INSTRUCTIONS.
TO CREATE THESE SLICES, RANDOM N AND STARTING ADDRESS
ARE CREATED. THE COMMENTS ON THE CALL WILL INDICATE
THE DESTINATION OF THESE RANDOM PARAMETERS WITHIN THE
TEST CODE. THE ROUTINES ALL SLICE DIFFERENTLY.
ONE WILL DIVIDE THE RAM IN HALF AND THEN FIND
A RANDOM SLICE WITHIN EACH HALF. ANOTHER MIGHT
FIND A RANDOM SLICE FOR EACH THIRD OF RAM.
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11.4 SEQUENCE OF TESTING
IT IS IMPORTANT THAT THE PROGRAMS BE
EXECUTED IN A SPECIFIC SEQUENCE:

APIS DIAG (FOR CPU/AP ONLY)
APP EXER
APB EXER
APC EXER
APD EXER
APE EXER
APF EXER
APG EXER
APH EXER
API EXER
APJ EXER
APK EXER

12. OCTAL DEBUG TOOL (ODT)
THE DIAGNOSTIC IS EQUIPPED WITH A BUILT IN ODT WHICH CAN
BE ACCESSED BY HITTING CONTROL 0 ("0") AT ANY TIME DURING
THE EXECUTION OF THE PROGRAM (AFTER SETTING THE PARA-
METERS).
ON ENTERING ODT THE ADDRESS OF THE LOCATION HAVING THE
NEXT INSTRUCTION TO BE EXECUTED WILL BE TYPED-OUT.

CONVENTIONS AND SYMBOLS
THE FOLLOWING CONVENTIONS ARE USED BY THE ODT:
? PRESSING ANY ILLEGAL KEY CAUSES THE ODT TO RES-
POND WITH A "?".
@ ODT IS READY AND AT YOUR SERVICE.

12.1 COMMAND STRUCTURE
AN ODT COMMAND HAS THE FOLLOWING FORMAT:
[ARGUMENT] [COMMAND]
AN ARGUMENT MAY BE ONE OF THE FOLLOWING:
"EXP" AN OCTAL EXPRESSION CONSISTING OF OCTAL NUMBERS
SEPARATED BY PLUS (+) OR MINUS (-) SIGNS. LEAD-
ING ZEROS NEED NOT BE TYPED.
"ADR" AN ADDRESS IS THE SAME AS AN EXPRESSION EXCEPT
THAT BIT 0 IS NEGLECTED.
A COMMAND IS A SINGLE TELETYPE CHARACTER

12.2 ODT COMMANDS
THE LOCATIONS THAT CAN BE EXAMINED AND MODIFIED BY THE
USER ARE CALLED CELLS. THESE CELLS ARE OF TWO TYPES:
INTERNAL CPU CELLS AND MEMORY LOCATIONS.

12.3 OPENING INTERNAL CELLS
THE COMMAND TO OPEN ONE OF THE INTERNAL REGISTERS IS OF
THE FORM "NA" WHERE N IS ANY OCTAL EXPRESSION BETWEEN
0 AND 7
0-3 FOR ACCUMULATORS 0-3
4 FOR PC OF THE NEXT INSTRUCTION TO BE EXECUTED IN
THE EVENT OF A "P" COMMAND.
5 CPU AND TIO STATUS
BIT INTERPRETATION
15 STATUS OF TIO DONE FLAG
14 STATUS OF INTERRUPTS (ION FLAG)
13 STATUS OF CARRY BIT
6 ADDRESS OF THE LOCATION HAVING THE BREAK POINT (IF
ANY)
7 INSTRUCTION AT THE BREAK POINT LOCATION

OTHER COMMANDS TO OPEN CELLS ARE:
"ADR"/ OPEN THE CELL AND PRINT ITS CONTENTS
./ OPEN THE CELL CURRENTLY POINTED TO BY THE POINTER
AND PRINT ITS CONTENTS.
.+ "ADR"/ ADD "ADR" TO THE POINTER, OPEN THE CELL
AND PRINT ITS CONTENTS.
.- "ADR"/ SUBTRACT "ADR" FROM THE POINTER, OPEN
THE CELL AND PRINT ITS CONTENTS.
"CR" THE RETURN KEY IS USED TO CLOSE THE OPEN CELL
WITH OR WITHOUT MODIFICATION.

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!0017 APB.T

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03 14.1 PASS 1  
04 ;  
05 ; 14.2 SUBSEQUENT PASSES  
06 ;  
08 .TITL APB.TX  
.END

\*\*00000 TOTAL ERRORS, 00000 PASS 1 ERRORS

0018 APB.T

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S2MPD 001075 MC 6/02