

DataGeneral

**TECHNICAL
STATEMENT**

TEXT LISTING

068-001068-01

PROGRAM

ARRAY PROCESSOR EXERCISER-D

TEXT TAPE

097-001068-01

ABSTRACT

THIS PROGRAM IS A COMBINATION DIAGNOSTIC AND EXERCISER FOR THE ARRAY PROCESSOR. THE PROGRAM IS EXECUTED BY A CENTRAL PROCESSOR (OR IOP) CONTROLLING THE ARRAY PROCESSOR (AP).

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7.0 PROGRAM DESCRIPTION/THEORY OF OPERATION

7.1 APXD TEST

INSTRUCTIONS TESTED:

LDR= LOAD A VECTOR TO RAM
MVR= FIND MAX VECTOR ELEMENT
MNR= FIND MIN VECTOR ELEMENT
SMA= COMPLEX MAGNITUDE SQAURED
SER= REAL SUM OF ELEMENTS
PER= REAL PRODUCT OF ELEMENTS
PEC= COMPLEX PRODUCT OF ELEMENTS

7.2 TEST DESCRIPTION

MVR = MNR
A REAL VECTOR WITH A KNOWN MAXIMUM VALUE IS LOADED INTO AP-RAM WITH AN LDR INSTRUCTION. THE MAXIMUM VALUE WHICH THE MVR CALCULATES IS THEN COMPARED WITH THE KNOWN MAX VALUE. THE VECTOR IS THEN REVERSED IN ORDER AND MVR IS RE-EXECUTED. SIMILAR TESTS ARE PERFORMED WITH DIFFERENT WORD COUNTS, STEP INDICES, AND RANDOM ADDRESSES IN RAM.

THE MNR TESTS DIFFER ONLY IN THAT THEY SEEK MINIMUM NUMBERS RATHER THAN MAXIMUM.

7.2.2

SMA = SER
THE SMA INSTRUCTION IS TESTED BY FIRST LOADING AP-RAM (VIA LDR) WITH THE COMPLEX NUMBERS TO BE SQAURED AND SUMMED. THE SMA IS THEN EXECUTED AND THE RESULTANT VECTOR IS COMPARED WITH THE PREVIOUSLY CALCULATED ANSWERS WHICH HAVE BEEN SET UP IN MAIN MEMORY. WORD COUNT VARIES FROM 1-25 IN THE FIRST TEST, BUT OTHER TESTS USE RANDOM INDICES AND WORD COUNTS.

SER IS TESTED SIMILARLY EXCEPT THAT THE REAL VECTOR IS MERELY SUMMED.

7.2.3

PER = PEC
THESE INSTRUCTIONS ARE TESTED BY SIMULATION ROUTINES WHICH PRODUCT REAL AND COMPLEX VECTORS RESPECTIVELY. THIS IS DONE FOR A WORD COUNT OF 26 AND UNIT INDICES, INITIALLY, AND THEN RANDOM INDICES AND WORD COUNTS AND VECTOR ELEMENTS (WITH EXPONENT LIMITED +/- 7)

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S:WPD 8

SWITCH SETTINGS

LOCATION "SWREG" IS USED TO SELECT THE PROGRAM OPTIONS (NOT SYSTEM CONFIGURATION). WHILE RUNNING UNDER DTOS, THIS LOCATION WILL BE LOADED BY THE MONITOR. HOWEVER UNDER STAND ALONE AND PROGRAM LOAD MODES THIS LOCATION WILL BE SET ACCORDING TO THE ANSWERS SUPPLIED BY THE OPERATOR. IN ANY CASE THE OPTIONS CAN BE CHANGED OR VERIFIED BY USING ONE OF THE COMMANDS GIVEN IN SEC. 8.2

SWITCH OPTIONS

DIFFERENT BITS AND THEIR INTERPRETATION AT LOCATION "SWREG" IS AS FOLLOWS:

Table with 5 columns: BIT, OCTAL VALUE, BINARY VALUE, INTERPRETATION. Rows 1-8 detailing switch settings like LOOP ON ERROR, PRINT TO CONSOLE, etc.

SWITCH COMMANDS

ONCE THE PROGRAM STARTS EXECUTING THE STATE OF ANY OF THE BITS CAN BE CHANGED BY HITTING KEYS 1-9, A-F. THE PROGRAM WILL CONTINUE RUNNING AFTER UPDATING THE OPTIONS. EACH KEY WILL COMPLETE THE STATE OF THE BIT AFFILIATED WITH IT, THUS BIT 4 CAN BE ALTERED BY HITTING KEY 4. SETTING OF ANY BIT OF LOCATION "SWREG" WILL SET BIT 0. (DEFAULT MODE IS DEFINED AS ALL BITS OF SWREG SET TO 0) THE PROGRAM CAN BE LOCKED INTO SWITCH MODIFICATION MODE BY TYPING A 0, IN WHICH CASE MORE THAN ONE BIT CAN BE CHANGED BEFORE CONTROL IS ALLOWED TO RETURN TO THE MAIN PROGRAM.

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13.0 SPECIAL NOTES/SPECIAL FEATURES

13.1 FOR A COMPLETE TEST ALL PROGRAMS SHOULD BE EXECUTED WITH CAT/KITTEN.

13.2 A NOTE ABOUT AP ADDRESSING

ADDRESSES IN THE AP CAN BE OF SEVERAL MODES:

- 1) ONE WORD MODE (1E) SAME AS STANDARD ADDRESSING
- 2) TWO WORD MODE (2MM) - EACH 32 BITS IS NOW ONE ADDRESS SPACE. THIS IS USED IN THE AP TO SIMPLIFY REAL NUMBER ADDRESSING.
- 3) FOUR WORD MODE (4MM) - EACH 64 BITS IS NOW ONE ADDRESS SPACE. THIS IS USED IN THE AP TO SIMPLIFY COMPLEX NUMBER ADDRESSING.

THE AP ACCESSES AN ADDRESS RELATIVE TO THE START OF THE AP RAM. THUS AP RAM LOC 0 WOULD BE THE FIRST LOCATION THAT IS IN THE AP. HOWEVER, AS FAR AS THE ECLIPSE CPU IS CONCERNED, AP LOC 0 IS CONTAINED AT LOCATION LABEL "RAMPT". (IN PAGE ZERO. SO, IF RAMPT CONTAINS 64000, THEN 2000 2MM (AP RAM) IS REALLY 64000+2000=70000.

NOTE: "STOP ON STORE" OR "STOP ON ADDRESS" IN AP RAM SPACE WILL NOT WORK IF THE AP IS USING THE INTERNAL AP ADDRESS LINES TO ACCESS AP RAM.

14.0 RUN TIME

14.1 PASS 1 30 SEC

14.2 SUBSEQUENT PASSES 50 SEC

**00000 TOTAL ERRORS, 00000 PASS 1 ERRORS