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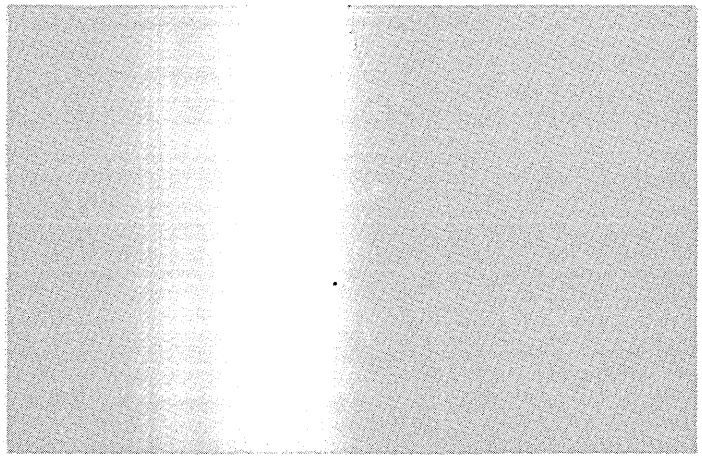

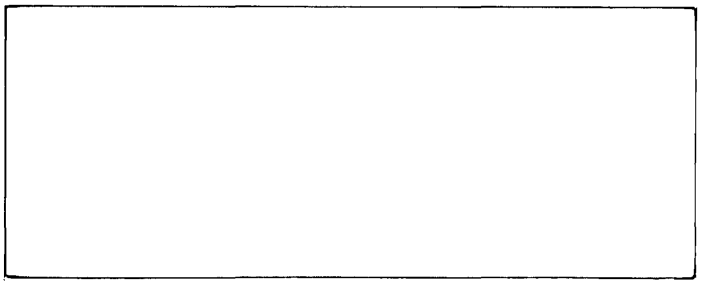

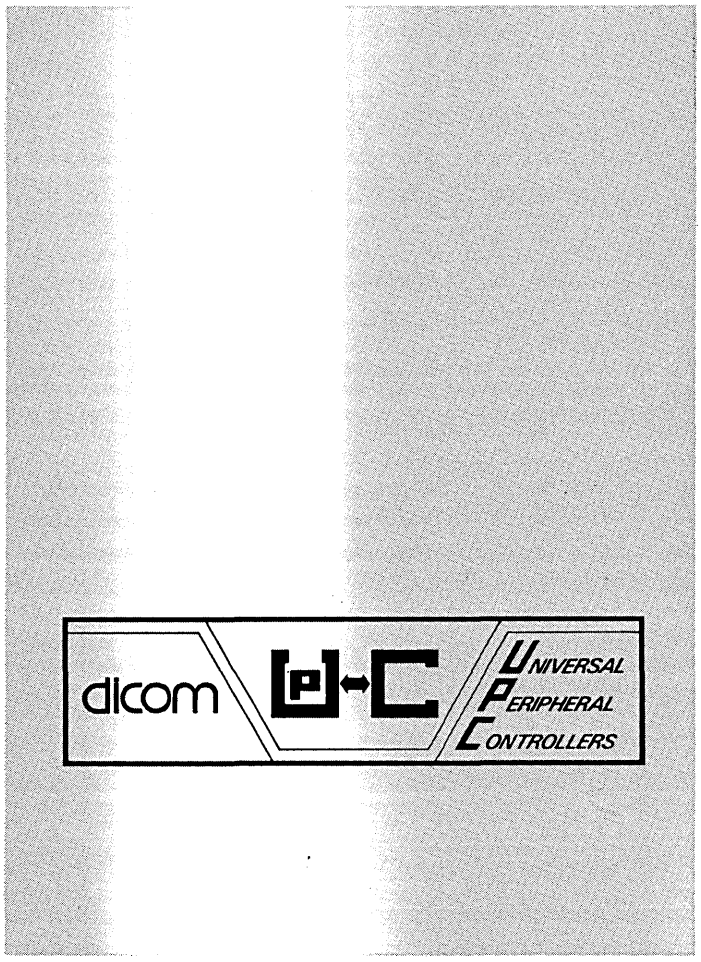

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MODEL 422
FLOPPY DISK SYSTEM
OPERATION
AND
MAINTENANCE MANUAL
PART I

dicom INDUSTRIES

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(408) 732-1060 • TWX 910-339-9285

P/N 505-01521-01 Rev. A
Revised: February 1976

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Dicom Industries certifies that this product was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory. Dicom Industries further certifies that its calibration measurements are traceable to the U.S. National Bureau of Standards to the extent allowed by the Bureau's Calibration facility.

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THE FOREGOING WARRANTY IS EXCLUSIVE OF ALL OTHER WARRANTIES, EXPRESS OR IMPLIED INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR PURPOSE.

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SECTION I

General Information

I.I INTRODUCTION

This section contains a simplified operational description, a description of the physical properties and performance characteristics, model description and option description of the Dicom Model 422 Floppy Disk System (FDS).

1.2 PURPOSE

The Dicom FDS is a multi-purpose multi-drive functionally complete low cost random access mass storage devices. The Model 422 FDS is a complete system including rack mountable enclosure, power supply, disk drives and Controller with card cage.

1.3 DESCRIPTION

The Model 422 FDS contains all the logic required for formatting and controlling hard sectored floppy disk drives. This includes the functions of data formatting, sector addressing, error detection, and data encoding and decoding. Moreover, the controller contains the timing logic for stepping the selected drive, raising and lowering the heads and remembering the track and sector position for each individual drive. This significantly reduces the average positioning time.

The basic controller consists of three modular electronic cards plus a motherboard. The first card, the Computer I/O, contains the data, command, and status registers which connect to the host processor or the Paddleboard Assembly for special interface logic. The second, the Read/Write Card, provides all the logic for timing, Read/Write, and formatting the phase-encoded data and 16 bit cyclic redundancy check (CRC) code. The third card, the Disk Interface, holds the logic for controlling and positioning the first two drives. Optionally, a fourth card, the Expansion Disk Interface Card may be installed for controlling the third and fourth drives. Likewise, a status panel display card may be connected to the motherboard to allow the user to monitor command and status of the selected drive and formatter.

Refer to 1.3.1 for Description and Specifications for Model 422 FDS.

1.3.1 MODEL 422 FLOPPY DISK SYSTEM

Part No.	Description
500-01525-01	Model 422-1: Single drive floppy disk system; includes one disk drive, controller, power supply and enclosure (for three drives).
500-01525-02	Model 422-2: Same as Model 422-1, except includes two drives.
500-01525-03	Model 422-3: Same as Model 422-1, except includes option 09 with three drives.
515-01525-SP	Option SP: Front status panel for display of disk controller commands and status.
515-01525-SK	Option SK: Slide Kit; includes quick-disconnect 20" slides and miscellaneous hardware for mounting in standard RETMA rack.
515-01525-09	Option 09: Expansion disk interface card, used for field expansion of 422 for third and fourth drive.
515-01525-10	Option 10: Expansion disk drive and required cables for use in field expansion (Specify if for use in expansion enclosure).
422 EXPANSION ENCLOSURES (422-3 or Option 09 prerequisites)	
510-01524-01	Model 422-11: Expansion enclosure; includes one disk drive, enclosure (for two disk drives) and required cables for connection to 422 mainframe.
510-01524-02	Model 422-12: Same as 422-11, except includes two drives.
505-01521-01	422 Interface and Maintenance Manual,Part I: One included with each 422 system.
505-01522-01	422 Maintenance Manual,Part II: One included with each 422 system.
520-50109-01	Model 422: Extender Board.

DISK CARTRIDGES-HARD SECTORED

Part No.	Description
024-00402-01	Disk Cartridges: Inside sector holes (for use with IBM compatible media drives).

MODEL 422
Specification

DATA STORAGE	
Disk Capacity	157,696 words/disk
Expansion	Four drives per controller/ interface = 630,784 words
Data Tracks	77 per disk
Sector per track	16
Words per sector	128
Bits per word	16
DATA ACCESS/WORDS	
Track Movement	10 msec track to track
Head Settle Delay	50 msec
Latency	167 msec (one revolution) maximum 83 msec (one half revolution) average
Transfer Rate	15,700 16-bit words/second Data words are transferred one sector (128 words) at a time.
POWER REQUIREMENTS	
Line Voltage	115VAC ($\pm$10%), single phase 230VAC ($\pm$10%), single phase
Line Frequency	60/50Hz $\pm$1Hz
PHYSICAL	
Dimensions	19" w, 10.5" h, 21" d (1 to 3 drives)
Expansion Enclosure	Same
Weight - 1 Drive	54 lbs.
2 Drives	64 lbs.
3 Drives	76 lbs.
Expansion Enclosure	
1 Drive	31 lbs.
2 Drives	42 lbs.

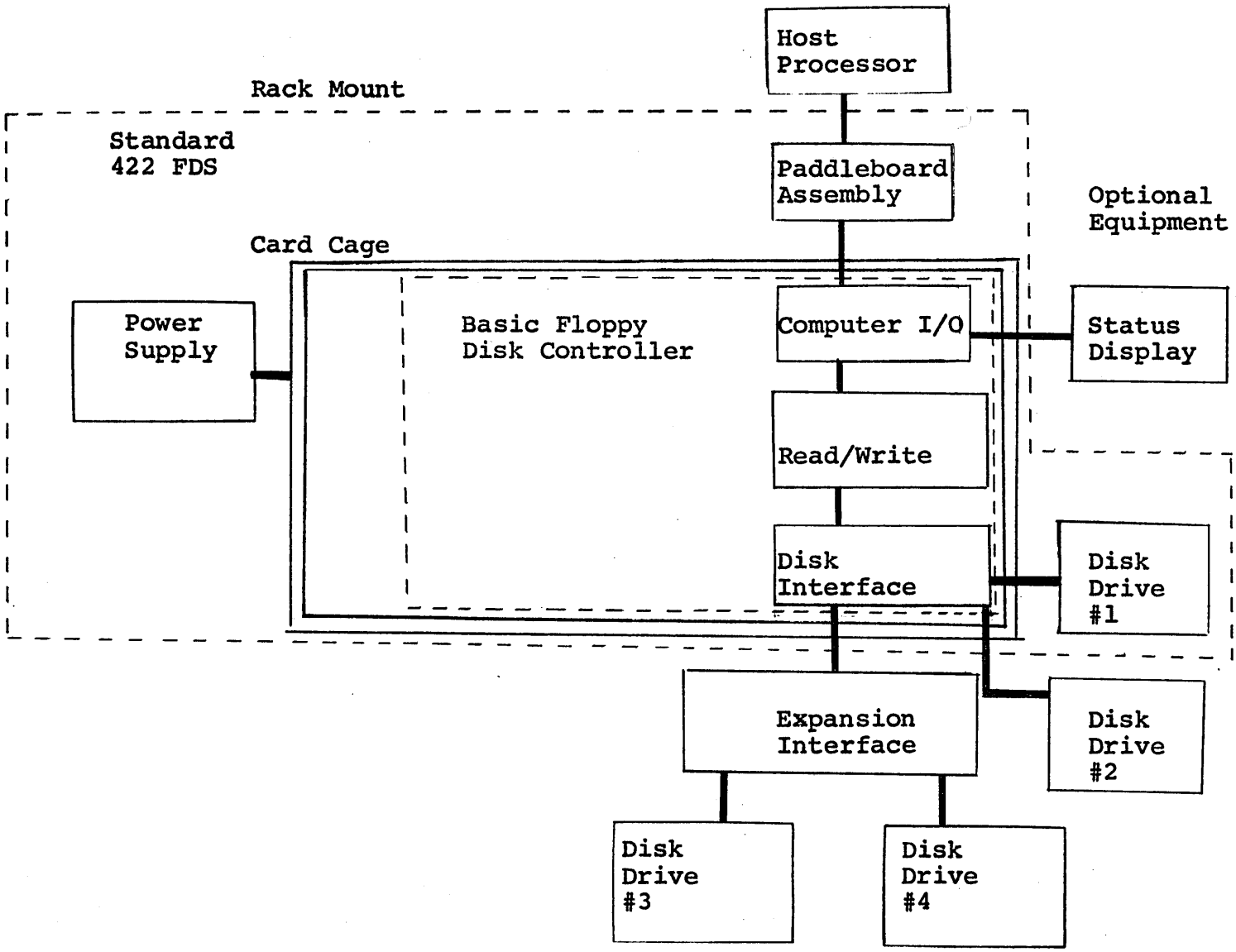
Specification (con't)

ENVIRONMENTAL

Disk Drive & Electronics	+10 to +45 C 15-95% humidity (no condensation)
Media	+10 to +45 C 20-80% humidity

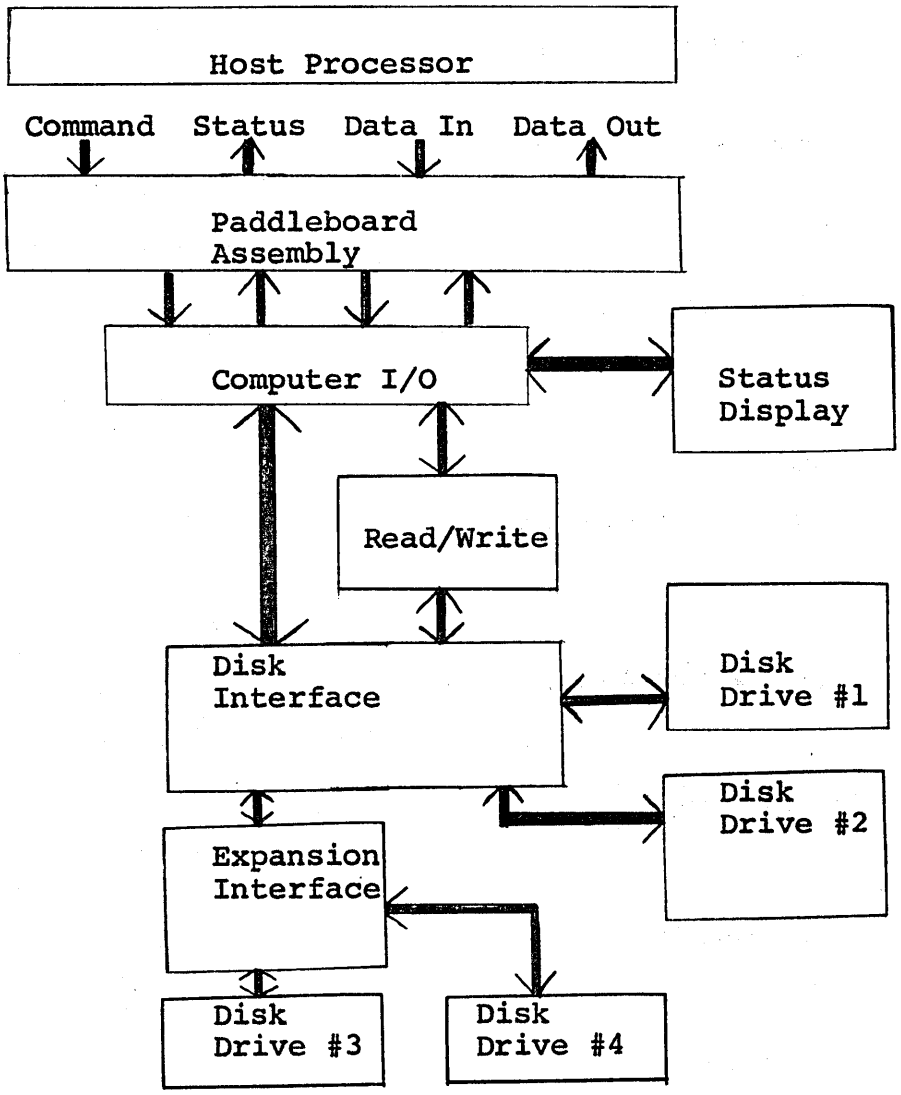
1.4 Simplified Block Diagram

Figure 1.1 depicts a block diagram of the basic configurations.



1.5 Simplified Flow Diagram

Figure 1.2 depicts a simple flow diagram for the floppy disk controller.



1.6 ELECTRICAL INTERFACE SIGNALS TO HOST EQUIPMENT

1.6.1 DATA

Input Data Lines	16-bit parallel input data lines
Output Data Lines	16-bit parallel output data lines
Data Strobe	1 line to signal FDC data is available. When writing, or acknowledge that data was taken in read by host.
Data Flag	1 line to signal host that data was taken in write, or request data to be taken in read.

1.6.2 STATUS

Selected Drive Ready	1 line to signal host that the selected drive is rotating and a cartridge is in place.
Write Protected	1 line to signal host that the selected drive has been writed protected.
Track Zero	1 line to signal host that the selected drive has reset to track position zero.
Data Error	1 line to signal host that a data error was found when reading the last sector.
Rate Error	1 line to signal host that the host processor did not answer a data flag within the time allowed after a request was made by the FDC.
Formatter Ready	1 line to signal host that the controller is not busy performing a previous command. The formatter will become READY after completing a sector read, write, or track seek command.

1.6.3 COMMAND

Initialize	1 line to FDC to reset all drives to track zero.
Function	2 lines to FDC
00	Status of selected drive
01	Read
10	Write
11	Seek
Drive Select	2 lines to FDC
00	Drive #1
01	Drive #2
10	Drive #3
11	Drive #4
Track	7 lines to FDC to address up to 77 tracks.
Sector	4 lines to FDC to address up to 16 sectors.
Command Strobe	1 line to FDC to store above command word.

1.7 ELECTRICAL INTERFACE SIGNAL PROPERTIES

All signals are TTL Compatible, low true.

High = 2.4 volts minimum
Low = 0.4 volts maximum

Signal input load equals one TTL load, output signals are from open collector 7438 or equivalent with 680 ohms pull-up. These signals are with respect to the Computer I/O motherboard connector J5A and J5B.

Any desired signal conditioning, matching or level shifting can be provided for with a user designed Paddle-board Assembly Card which plugs into J3.

SECTION II

Controller Logic Description

2.1 INTRODUCTION

This section describes the disk controller cards and their major logic funtions. A detailed theory of operation will be found in the units Operation and Maintenance Manual.

2.2 THE DISK CONTROLLER

The disk controller consists of three basic logic cards and up to three option cards (see figure 2.1), plus a motherboard. The motherboard consists of eight connectors in two rows (A and B), arranged in six columns or slots. The numbering scheme (i.e., J1A thru J8) is used throughout the logic diagrams. Three of the six slots (J3A/B, J4A, and J5A/B) are used for the controller logic cards. Connectors J1A and J1B are used for the Disk Interface cable (drawing 036-00442), which routes the signal lines and power to the first two disk drives. Connectors J1C and J1D are used to route signal lines and power to the third and fourth drives when the Expansion Disk Interface is installed in connector J2. Connector J8 is used for the interface cable(s) to the computer interface card(s). J6 is used by the Status Panel. The disk controller can be divided into three major parts; the Computer I/O card the Disk Interface card, and disk formatter. The disk formatter logic is contained primarily on the Read/Write Logic card, with some of the logic on the other two cards in the controller.

Signal mnemonics appear in quotes in the following description of the controller, i.e., "SRDY" is the Selected Drive Ready signal in the Disk Interface card.

2.3 DISK INTERFACE CARD

The Disk Interface card in slot J3A/B (drawing 520-50103) contains the conditioning logic for the signals to and from the disk drives. It contains:

Track Zero "STRØØ" Multiplexer

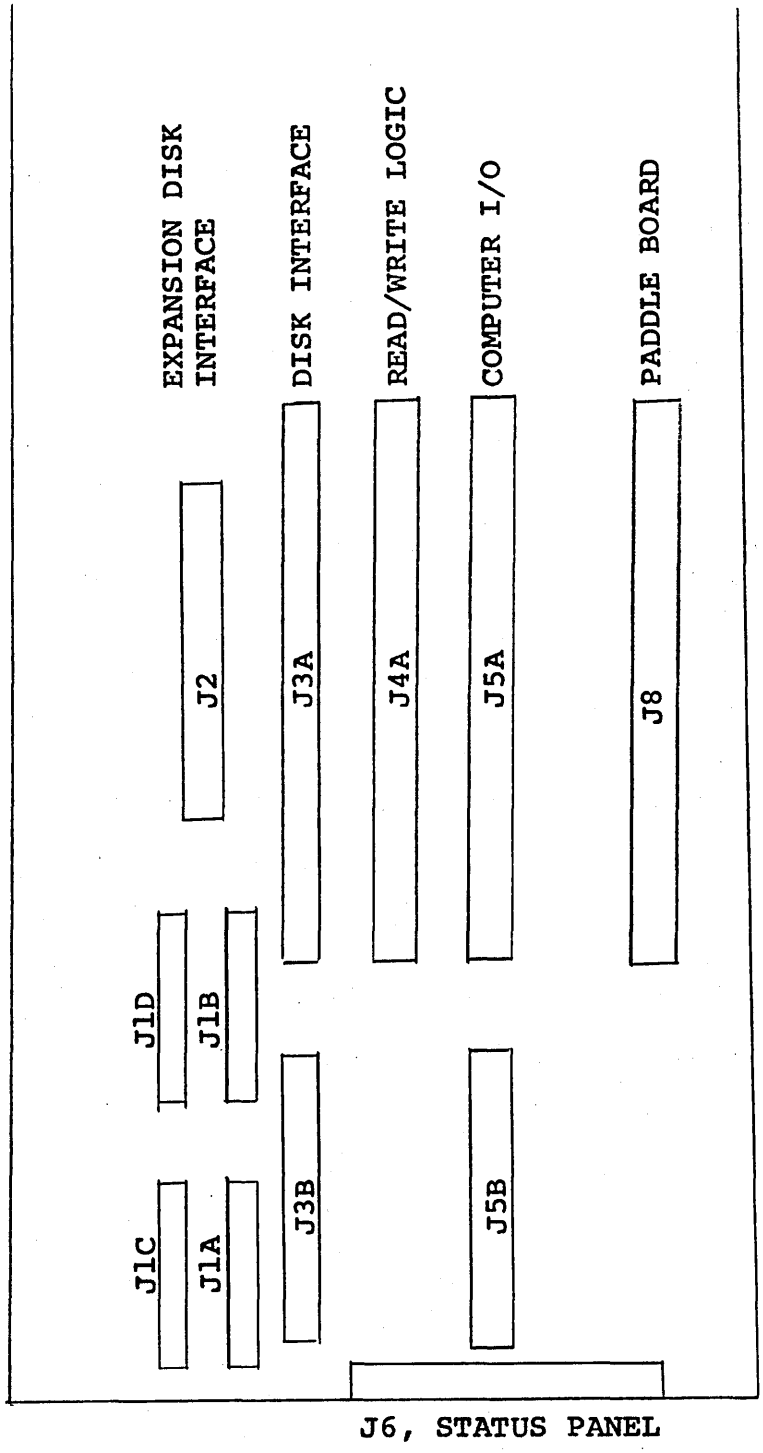
Write Protect "SWRP" Multiplexer

Separated Clock "SCLK" Multiplexer

Separated Data "SDT" Multiplexer

Sector Equal "SEQL" Multiplexer

Track Equal "TEQL" Multiplexer



NOTE: J1A and J1B are located at the top of the Disk Interface Card (520-50103); J1C and J1D are located at the top of the Expansion Box Interface Card (520-50102)

Disk Controller Layout
Figure 2.1

Sector Synchronization "SYNC" Multiplexer

File Unsafe "UNSF" Multiplexer

Ready "SRDY" Multiplexer

Track and Sector Address Counters

Track and Sector Addressing Comparators

Beginning of Sector Synchronization "SYNC" logic

Track Access and Step-In/Step-Out Signals "STPIn" and "STPOn"

Head Load "LHF" and Head Settle "50MSC" logic

Head Unload Revolution Counter "RLHF"

Drive Ready "RDYn" logic

Advance State "STAF" Flip Flop

The Three Clock Signals; 500 KHz Formatter Clock "FCLK"

250 KHz Data Strobe "WØCLK", and 250 KHz Write Clock "WCLK"

2.4 READ/WRITE LOGIC CARD

The Read/Write Logic card in slot J4A (drawing 520-50104) performs the majority of "disk formatting" functions; it handles the input and output data transfers between the computer and the disk via the Shift Register. The Shift Register performs the serial-to-parallel and parallel-to-serial conversions when reading and writing data.

The signal "ØCF" is the serial read data (SEP DATA) from the disk; "SHBØ" provides serial write data to the disk write data line "WDT" during write. Additional logic on this card includes:

The CRC Register

Bit and Word Counters for Controlling the Read/Write Sequencing

Formatter State Control "SCØØ", "SCØ1", "SCØ2", and "SCØ3" logic

Write Enable "WENF" logic

Read Enable "REDF" logic

Read and Write Sequencing to Provide Formatting by Controlling Data In/Out of the Shift Register

Data transfer request logic to the Computer I/O card

2.5 COMPUTER I/O CARD

The Computer I/O Card in slot J5A/B (drawing 520-50105) gates all signals to and from the computer interface card(s). "RBØØ-I" thru "Rl5-I" are the read data lines from the Shift Register via the Read Register. "WBØØ-I" are the read data lines from the Shift Register via the Read Register. "WBØØ-I" thru "WBl5-I" are the write data lines to the Shift Register via the Write Register. "CBØØ-I" thru "CBl5-I" are the command signals from the computer interface card(s). Command decode logic and disk controller status logic is included on this card.

2.6 EXPANSION DRIVE INTERFACE CARD

The Expansion Box Interface Card is an optional card used when the system is expanded to three or four drives. This card (drawing 520-50102) when installed in slot J2A contains logic to support the independent sector and track positioning of the drives, and some conditioning logic which is multiplexed with signals on the Disk Interface Card.

Track Zero "TRØØn"
Write Protect "WRPn"
Separate Clock "SCLKn"
Sector Equal "SEQLn"
Sector Synchronization "SYNCn"
File Unsafe "UNSFn"
Ready "RDYn"
Track and Sector Address Counters
Track and Sector Addressing Comparators
Beginning of Sector Synchronization "SYNC" logic
Track Access and Step-In/Step-Out Signals
"STPIn" and "STPOn"
Drive Ready "RDYn" logic

2.7 STATUS PANEL CARD

The Status Panel card in slot J6 (drawing 520-50106) displays the status of the Disk System. The status displayed is of two types: drive related and system related. Drive related indications display status of the currently selected drive, while system related indications pertain to conditions of the disk controller. The Light Emitting Diodes (LED) used for the display are lit when the condition is TRUE, (both lights out under DRIVE indicate drive Ø is selected).

Status which is drive related is:

Selected Drive "DADBØ1" and "DADB1"
Drive Ready "SRDY"
Write Protect "SDWPT"
Track Zero "SDTØØ"

Status which is controller related is:

Read Mode, "READ"
Write Mode, "WRIT"
Track Address bits, "TADBØ" thru "TADB6"
Sector Address bits, "SADBØ" thru "SADB3"
Formatter Ready, "FNBSY" (not busy)
Data Error, "DERR"
Rate Error, "RERR"

Write Protect switches are also provided so that Drives Ø and 1 may be protected via the Status Panel.

2.8 DISK CONTROLLER INTERFACE LINES

The disk controller interface lines consist of sixteen read data lines, sixteen write data lines, a data strobe, sixteen command lines, a command strobe, an initialize (reset) line, and seven disk controller status lines. All interface lines are negative true (Øvdc is a logic "1"). Disk controller line receivers present one TTL/DTL load; line drivers are high-voltage, open-collector outputs (7416 or 7438). The signal mnemonics and descriptions are as follows:

"WBØØ-I" thru "WB15-I": 16-bit input data word (write data) to the disk system. These lines must be stable during the data transfer strobe "DSTRB-I" time.

"RBØØ-I" thru "RB15-I": 16-bit output data word (read data) from the disk system. These lines stable prior to the data transfer request "XFREQ-I" status line going true.

"XFREQ-I": data transfer request. This status line is set true each time the disk system is ready to transfer a word. In the Write mode, "XFREQ-I" is set true each time the disk system is ready to accept a word for recording on the disk. "XFREQ-I" is set false when the disk system receives the data transfer strobe "DSTRB-I" (when the requested word is sent to the disk system). In the READ mode, "XFREQ-I" is set true each time the disk system has a word available for transfer to the computer. "XFREQ-I" is set false when the disk system receives the data transfer strobe "DSTRB-I" (when the word

is transferred from the disk system to the computer). When in the Read or Write mode, the disk system must receive a data transfer strobe within sixty microseconds of the data transfer request, or the Rate Error "RERR-I" status line will be set true (see "RERR-I" description).

"DSTRB-I": data transfer strobe. In the Write mode, "DSTRB-I" strobes the word on the write data lines into the disk system. In the Read mode, "DSTRB-I" informs the disk system that the word was accepted by the computer. In the Write mode, the leading edge of "DSTRB-I" (negative going) actually loads the input word into the disk system; the trailing edge (positive going) informs the disk controller that a word was transferred, thus satisfying the Rate Error logic. In the Read mode, only the trailing edge of "DSTRB-I" is used; this transition informs the disk controller that the word was accepted by the computer, thus satisfying the Rate Error logic. The optimum duration of "DSTRB-I" is between 500 nanoseconds and two microseconds.

"CBØØ-I" thru "CBØ3-I": sector address command bits. These four bits define which of the sixteen sectors of a track is to be accessed; "CBØØ-I" is the least significant bit.

"CBØ4-I" thru "CB1Ø-I": track address command bits. These seven bits define which of the seventy-seventy (77) tracks of a disk is to be accessed; "CBØ4-I" is the least significant bit.

"CB11-I" and "CB12-I": disk drive address command bits. These two bits define which of the four (possible) drives is to be accessed. They are decoded as follows:

"CB12-I"	"CB11-I"	
Ø	Ø	Disk Drive #1
Ø	1	Disk Drive #2
1	Ø	Disk Drive #3
1	1	Disk Drive #4

"CB13-I" and "CB14-I": mode command bits. These two bits define which of the four actual commands are to be executed by the disk system. The modes are:

"CB14-I"	"CB13-I"	
Ø	Ø	Select
Ø	1	Read
1	Ø	Write
1	1	Seek

Select - "CB13-I" and "CB14-I" at logic zero causes the disk system to select the drive defined by "CB11-I" and "CB12-I", and present the status of that drive on the status lines. The sector and track address command bits are ignored; no head motion occurs, nor are data transfer requests issued.

Read - "CB13-I" at logic one and "CB14-I" at logic zero causes the disk system to enter a read sequence, reading one sector (128 words) from disk and presenting these words to the computer. The head is first positioned to the track specified by the track address command bits; when the sector specified by the sector address command bits is under the head, data are recovered from this sector and presented on the read data lines one word at a time.

Write - "CB13-I" at logic zero and "CB14-I" at logic one causes the disk system to enter a write sequence, accepting one sector (128 words) from the write data lines and writing these words in a specified sector. The head is first positioned to the track specified by the sector address command bits; when the sector specified by the sector address command bits is under the head, data are requested from the computer and written in this sector. If data transfer requests are not honored (by a data transfer strobe), zeros are written.

Seek - "CB13-I" and "CB14-I" at logic one causes the disk system to select the drive defined by "CB11-I" and "CB12-I", and to commence track positioning. The head is positioned to the track specified by the track address command bits. No data transfer requests are issued. When the track specified is under the head, the system becomes ready to accept a new command, (not busy).

"CB15-I": initialize disk system. A logic one on this command line will cause the disk system to abort any command currently in process, retract the heads, move the heads to track zero, and enter the quiescent state (not busy).

"CSTRB-I": command strobe. A pulse on this line causes the disk system to execute the command (at the specified address) defined on the above discussed command lines. The address portion of the command word is stored by the disk system on the leading edge (negative going) of "CSTRB-I"; the command is executed on the trailing edge (positive going) of "CSTRB-I". The optimum duration of "CSTRB-I" is 500 nanoseconds to two microseconds.

"INTLZ-I": initialize disk system. A logic one on this line will cause the disk system to abort any command currently in progress, retract the heads move the heads to track zero, and enter the quiescent state (not busy). This line is indentical in operation as "CB15-I" above except it does not require a command strobe.

"SDRDY+I": selected disk drive ready. A logic zero on this status line indicates that the selected disk drive has a cartridge installed and that the drive is up to speed.

"FNBSY-I": disk formatter not busy. A logic one on this status line indicates that the disk controller (formatter) is not currently executing a read, write, or seek sequence.

"SDTØØ-I: track zero. A logic one on this status line indicates that the head on the selected drive is positioned at track zero. When the formatter is busy, this status bit is masked off (always a logic zero when the formatter is busy).

"SDWPT-I": write protected. A logic one on this status line indicates that the cartridge in the selected drive is write-protected, or that the Write Protect Switch for that drive (on the Status Panel) is in the PROTECT position. If a write command is issued when this bit is true, the track access portion of the write sequence will be accomplished, but no data will be written on disk. In the read mode, this status bit is masked off (always a logic zero when in the read mode).

"DERR-I": data error. A logic one on this status line indicates that a "parity error" was detected by the disk system hardware in reading a sector; this results from the CRC read from disk not comparing with the CRC that was computed during the reading of the data portion of the sector. The "DERR-I" bit remains set until the disk system receives another command strobe. The "DERR-I" bit may also

be set if the system has not completed its read or write sequence by the beginning of the next sector time.

"RERR-I": rate error. A logic one on this status line indicates that a data transfer request was not acknowledged by a data transfer strobe within the allowable sixty microsecond window. The "RERR-I" bit remains set until the disk system receives another command strobe. Since the disk system is a block-synchronous device, once a read or write operation is initiated the computer must transfer data at the demand rate of the disk system; if this does not occur, the Rate Error status bit is set. The disk system utilizes an input and output word buffer; thus, the computer does have up to sixty microseconds to respond to a data transfer request. During write operations, data may be transferred to a specified sector, but the amount of data may be less than 128 words. In this case, the disk system will automatically fill the remaining portion of the sector with zeros. The "RERR-I" bit will be set, as will the "Rate Error" status light; however this may be a proper indication (software dependent).

SECTION III

Interface Signal Connections

3.1 INTRODUCTION

This section specifies the connector pins for interfacing signals from the host processor either directly through connector XJ8 on the motherboard or via the Paddleboard Assembly. Also included is the wiring diagram for signal connections of the Cable Assembly from the Disk Interface Card to the Disk Drive.

3.2 CONNECTOR ASSIGNMENTS

Refer to the Motherboard Schematic Diagram for direct connection through X58 of host interface signals. Refer to the Paddleboard Schematic for interface cable pin assignments.

3.3 INTERFACE SIGNAL TIMING

The disk controller has been designed to minimize difficult system timing considerations. All data lines are static levels which are at a steady state prior to issueing the Data Strobe or Data Flag. Likewise, all command lines should be at the desired level prior to the host processor issueing the Command Strobe. Status lines are dynamic level changes, subject to the respective disk operation. Only four signal lines bear special attention. These are the Data and Command Strobes, Data Flag and Formatter Ready.

Both strobe signals should be a pulse of 1 usec $\pm$0.5 usec. The controller responds to the negative going leading edge to load the data or command registers. Furthermore, the trailing edge (positive going) of the Command Strobe signals the controller to execute the command. The negative going leading edge of the Data Flag and Formatter Ready lines may be used to signal the host processor that the last data or command has been executed.

Figures 3.1 depicts the typical read or write function timing sequence. Table 3.1 indicates the relative timing and associated action.

READ/WRITE

Controller Timing

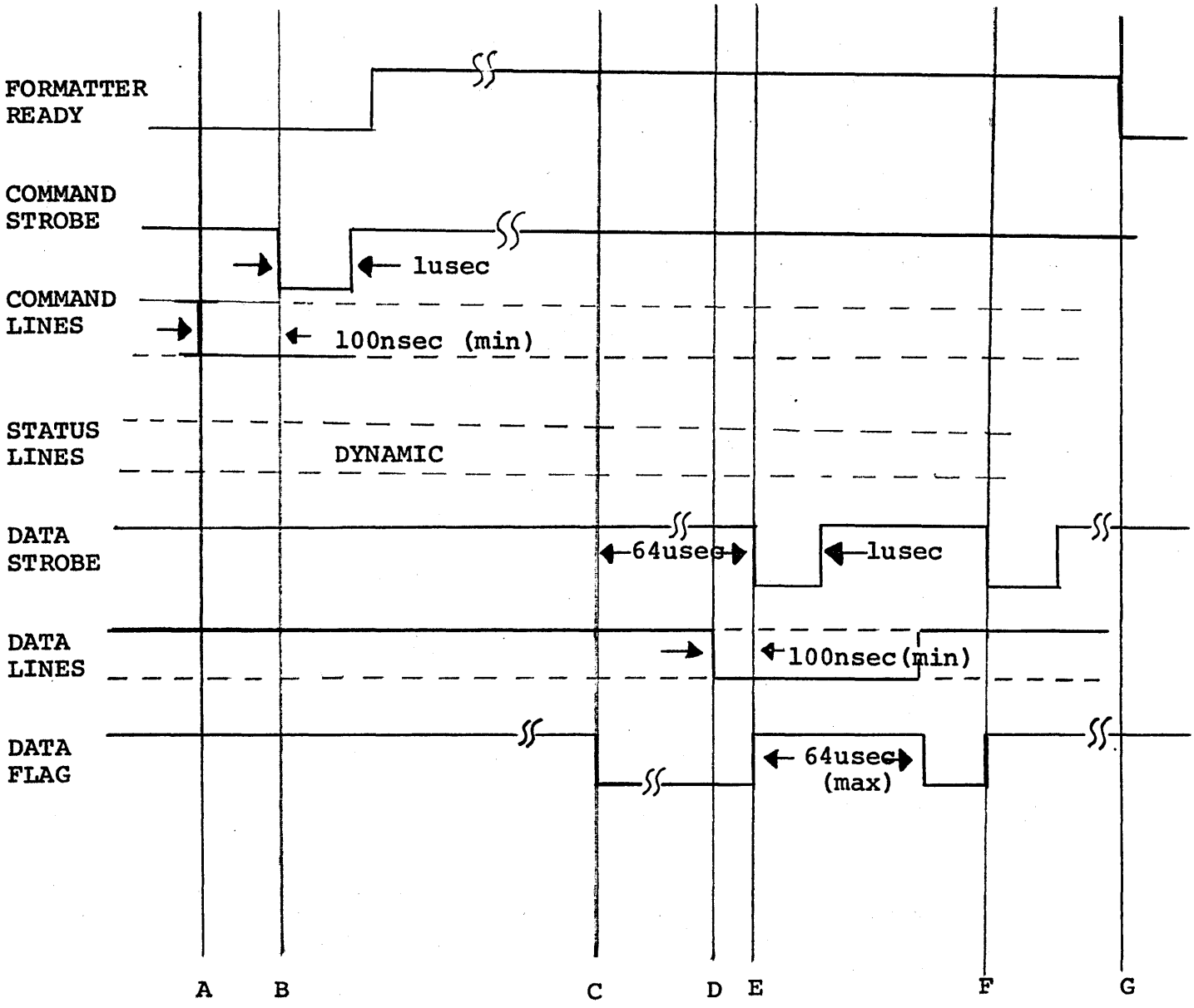


Figure 3.1

Timing Table 3.1

FROM	TO	TIME	ACTION
A	B	100nsec	Allows for command lines to settle.
B	B+	1usec ±0.5usec	Duration of Command Strobe Pulse.
B+	B++	20nsec	Formatter Ready will go false.
A	C	1msec (min)	First data request. Time will vary dependent on access time to correct track and sector.
C	D	64usec (max)	Data strobe sent to Controller. Data must be given within 64msec.
E	F	64usec (max)	128 words will be requested. Each data flag must be answered within 64msec or Rate Error will be set and the Controller will automatically zero fill the remaining portion of the sector.
B	C	10msec	When the sector write has been completed, the Formatter Ready line will set true, ready to accept the next command.

NOTE: Timing signals are not critical except for answering a data request. With proper signal line conditioning, strobe pulse width may be varied considerably. Contact the factory for any special considerations.

IV. INSTALLATION

4.1 INTRODUCTION

This section contains information on unpacking, inspection, installation, and operational checks.

4.2 UNPACKING AND INSPECTION

If the shipping carton is damaged on arrival, ask that the carrier's agent be present when the unit is unpacked. Carefully unpack the unit and inspect it for damages (scratches, dents, etc.). If the unit is damaged or fails to meet the operational checkout, in the "Operational Check Section", notify the carrier and the nearest Dicom representative immediately. Retain the shipping carton and padding material for carrier's inspection.

4.3 CONTROLS AND CONNECTORS (REAR)

a. AC line voltage SELECTOR jumper. Selects power transformer primary winding for operation either on 115 Vac or 230 Vac. For 230 Vac operation the jumper on the transformer must be changed. See Power Supply Schematic. For 5ØHz operation, the drive pully on the drive must be installed. See instructions in Appendix under Pertec Maintenance Manual.

b. LINE connector. Accepts the power cord to provide AC power to unit.

c. Fuse F1. Protects the unit from power overloads. Use 6.25 -ampere, slow blow fuse for 115 Vac: 3 -ampere, slow blow fuse for 230 Vac.

d. 115 Vac Line Output. Supplies power to Expansion Box drives when this option installed.

NOTE: The 115 Vac Output Connector should only be used for Expansion Box AC power.

4-4 CONNECTORS (REAR) EXPANSION BOX

AC LINE Connector. Accepts the power cord for 115 Vac operation which is supplied by the 422 mainframe.

This power is supplied by the 422 mainframe power supply secondary winding.

4-5 INPUT/OUTPUT CONNECTIONS - 422

Input and output signals are routed through the Computer Interface Cable Paddleboard (drawing 520-50108). Provisions have been made to allow use of flat cables or bundled cables. When the cables are installed, they are routed through the connector clamp assembly at the rear of the unit which provides for clamping the cables. When the Expansion Box is installed, the interface cables interconnecting the Expansion Box to the 422 main frame are also routed through the cable assembly.

Unless the unit is supplied complete with interface to a specified computer, cables to the interface are not provided.

4-6 INPUT/OUTPUT CABLES-EXPANSION BOX

When the Expansion Box option is installed, cables are supplied attached to the Expansion Box. One cable if a single drive; two cables if a dual drive option is installed.

The cables are connected to the 422 mainframe as follows:

a. Set the Power ON/OFF switch to OFF, and unplug the AC.

b. Open the 422 mainframe by removing the top cover.

c. Disconnect the rear cable clamp assembly on the 422 mainframe. Route the flat cables from the Expansion Box through the slotted assembly, then re-install assembly. Connect the cables to the connectors provided at the top of the Expansion Box Interface card installed in J2.

If the 422 is being expanded in the field, install the Expansion Box Interface card (520-50102) into J2. The interface cable for drive three should be connected to JI-C, the connector toward the front of the card. The second cable connects to JI-D, the connector toward the top rear of the card.

d. Replace the cover on the 422 and plug in the AC power.

4-7 JUMPER STRAP OPTIONS

The 422 utilizes jumper straps which depend on the number of drives installed in the system. These straps are installed on the Disk Interface Card and if installed, the Expansion Box Interface Card. These straps should be verified for proper installation whenever drives are added or removed from the system. They are:

CONFIGURATION	CARD	INSTALLATION
Single Drive	Disk Interface	Jumper E1 to E2 located near U1 Jumper E7 to E8 Jumper E9 to E10 located near U3
Dual Drive	Disk Interface	Remove E1 to E2
Three Drive	Disk Interface	Remove E1 to E2 Remove E7 to E8
	Expansion Box Interface	Jumper E1 to E2 located at upper middle of card
Four Drive	Disk Interface and Expansion Box Interface	Remove all jumpers

4-8 INITIAL TURN-ON

If the Dicom 422 is provided as part of a system including interface to a specified computer, refer to the System Operating and Software Manual; if an operational checkout is to be performed, the checkout procedure will be specified in that manual. Otherwise proceed as follows:

a. With no interface cable installed, apply power.

b. The front status panel should indicate the following:

Drive Ø selected; both UNIT lights off.
Neither Read nor Write Mode lights on
Track Address Zero; all lights off
Sector Address Zero; all lights off
Selected Drive Not Ready (No Diskette Loaded)
Formatter Ready lit.
Track Zero lit.

4-9 OPERATIONAL CHECK

After the initial turn-on, the unit is ready to begin operational test. Before installation and integration of a specific interface, a few additional checks may be made as follows:

a. Install a Diskette into Drive Ø.

b. The "Drive Ready" light should turn on.

c. Place the "WRITE PROTECT" switch in the "PROTECT" position.

d. The "WRITE PROTECT" light should turn on.

The unit is now ready for interface integration. Refer to the Disk Controller Interface Lines (section 1-8) for interface line definitions, or to the Software Manual if the unit was supplied with an interface.

V OPERATING INSTRUCTIONS

5-1 INTRODUCTION

The basic Dicom 422 Floppy Disk System consists of a mainframe assembly housing a card cage, power supply, control panel, and one, two or three drives. The system may be expanded to four drives by use of an Expansion Box option. The system functions as a mass storage device through cables which supply command and data information. There are no controls on the unit except for "WRITE PROTECT" switches for write protecting the Diskettes in Drives Ø and 1. The system displays to the operator the current status of the system through a front Status Panel.

5-2 STATUS PANEL

The Status Panel displays the current operation of the system. Refer to section 1-7 for a description of each indicator.

When power is first applied to the system, all drives are reset to track zero, and the Read, Write, Data Error, Rate Error, Track Address, Sector Address, and Unit indicators should turn off.

The Formatter Ready and Track Zero indicators should turn on. If a Diskette is installed in Drive Ø, the "Drive Ready" light should come on. If the Diskette is write protected with a "Write Protect" tab, then the "WRITE PROTECT" indicator should turn on.

During operation, the Status Panel will display the current drive selected, the mode of operation if reading or writing, the last track and sector address issued to the selected drive, and the status of the selected drive and of the controller.

If an error is made during operation, the following status lights will indicate the error or the correct operation:

INDICATOR	STATUS
DRIVE READY	Selected drive has a Diskette installed and drive is ready.
FMTR READY	Formatter is ready to accept a new command.
DATA ERROR	An error was made while reading the addressed data; the CRC was incorrect or a new sector was encountered while the system was still in the Read or Write Mode.
WRITE PROTECT	The selected drive is write protected.
RATE ERROR	The system was not serviced by the host computer within the proper time of a data transfer request. When in the Write Mode, if the system does not receive data after Write Mode has been commenced, the addressed sector will have zeros written into it starting with the first data request which was not answered. Note: This zero fill capability allows smaller amounts of data to be transferred to a sector then the required 128 words, while still generating the proper CRC check.
TRACK ZERO	The selected drive is positioned to track zero, and the system is not busy.

5-3 WRITE PROTECT SWITCHES

The Status Panel has two "WRITE PROTECT" switches which allow the operator to write protect the Diskettes installed in drives Ø or 1. If the Diskette has a "WRITE PROTECT" tab on the Diskette, then the Diskette will be protected regardless of the switch position. However, if the Diskette is not protected, then placing the associated switch in the "PROTECT" position will inhibit the system from writting on the protected drive, and will turn on the "WRITE PROTECT" indicator when the associated drive is selected.

During a Read operation, the "WRITE PROTECT" indicator will be turned off by the system.

VI PRINCIPLES OF OPERATION

6-1 INTRODUCTION

This section discusses the basic principles of operation of the Dicom 422 Floppy Disk System.

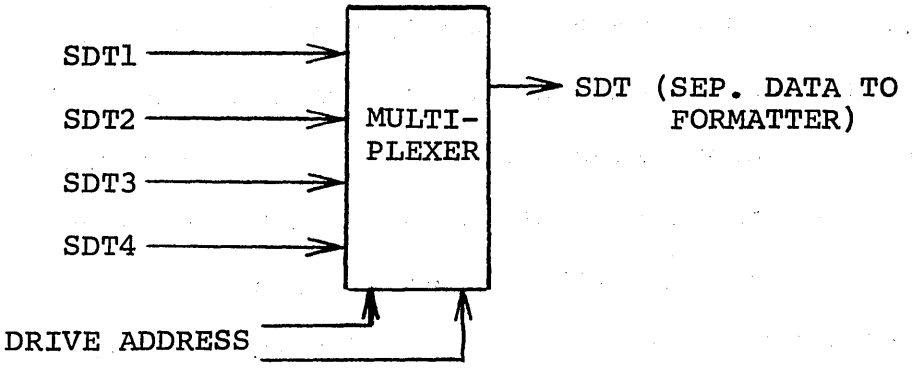
6-2 DISK INTERFACE

The Disk Interface logic on card 3A/B is shown on logic drawing 520-50103 in the appendicies. There are thirteen signal lines required to exchange data, control, and status information between the controller and each of the four possible disk drives. A detailed description of these lines is contained in an appendix of this manual. Briefly, these lines are:

STEP IN	Move head towards center of disk
STEP OUT	Move head towards circumference of disk
LOAD HEAD	Engages R/W head with disk media
FILE UNSAFE RESET	Reset for disk drive control logic
WRITE ENABLE	Enables writing of data
SECTOR	Indicates sector location on disk
INDEX	Indicates index location on disk
TRACK ØØ	Indicates when head is positioned on track ØØ
FILE UNSAFE	Indicates disk drive malfunction
WRITE PROTECT	Indicates disk is write protected
SEP DATA	Read data from disk drive
SEP CLOCK	Read clock from disk drive
WRITE DATA	Write data and clock to disk drive

Conceptually, all of the above lines are controlled in the same manner. However, because of differing requirements for WRITE DATA and WRITE ENABLE, this control is implemented differently.

The above signal lines must be multiplexed by the controller to allow for the selection of one of the four possible disk drives which can be used during a read or write operation. The multiplexers are controlled by the disk drive address supplied as part of the disk address. A typical configuration is shown below for the Separate Data lines.



The Selected Drive Ready signal is derived from the sector pulses from each drive. The READY DELAY for each drive times out at a predetermined time; if a sector pulse is not received from each drive within this time period, the drive is not ready. If no cartridge is installed, or if the cartridge is not up to speed, the READY DELAY will time out.

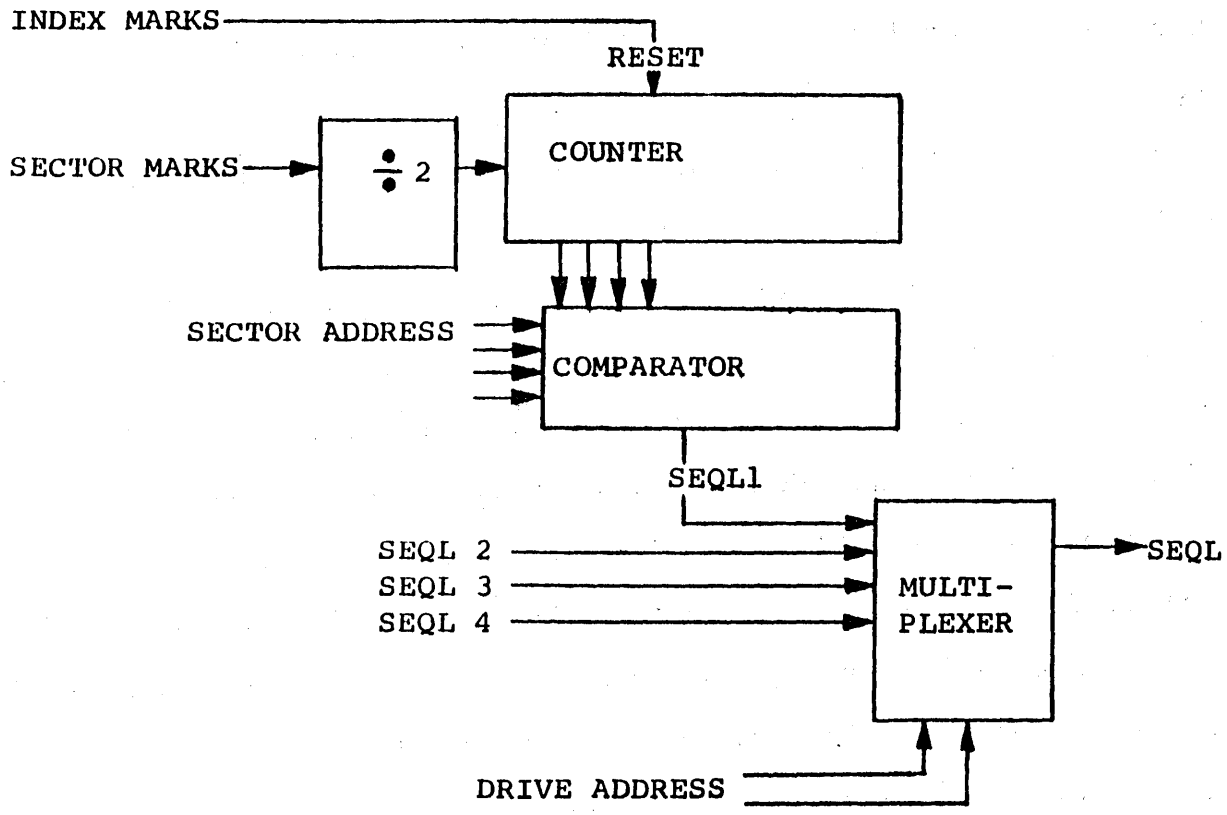
The STEP IN, STEP OUT, and LOAD HEAD signals are used to control track positioning and loading of the read/write heads. Since the heads on all disk drives move independently, the STEP IN and STEP OUT signal lines are controlled on an individual basis. However, the LOAD HEAD signal is presented to all disk drives simultaneously. During State Ø (power up) the heads are retracted to the home position (track zero)simultaneously, but the heads are not loaded. During normal sequences, a single control circuit is used to generate the head step and settling time, which is directed to the selected drive.

As STEP IN and STEP OUT signals are sent to the disk drives to increment the track positioning motor, the Track Counter for that drive is incremented or decremented to record track location. During a read/write sequence this counter is compared to the track address portion of the Disk Address Register. When an address comparison is achieved (Track Equal "TEQL" goes true), the formatter enters the actual read/write state; this occurs when the ADVANCE STATE Flip Flop is set.

When the first read/write command is issued after power up, the heads are not loaded. When the track access portion of the read/write sequence is accomplished ("TEQL" is true), the heads are loaded and the HEAD SETTLE delay is initiated. When this delay times out, the ADVANCE STATE Flip Flop is set and the actual read/write state is entered. The heads will remain loaded after the read/write sequence is completed; if another read/write sequence is not initiated within 800 milliseconds (five revolutions of the disk), the heads will be unloaded.

The SECTOR and INDEX signals are derived from the thirty-two sector marks and the index mark which result from a single revolution of the disk cartridge. These marks, which are derived from the sensing holes located on the circumference of the cartridge, provide for disk sector addressing.

Each disk drive uses separate and independent sector addressing circuits. The sector marks from the disk drive are counted and compared to the sector address portion of the Disk Address Register. The equal output of the Sector Comparator is then multiplexed with the other sector addressing circuits so that the formatter can select the proper addressing logic according to the drive select portion of the Disk Address Register.



The "SYNC" logic is used to define (to the disk formatter) the actual beginning of a sector.

6-3 COMPUTER I/O

The Computer I/O logic on card 5A/B is shown on logic drawing 520-50105 in the appendicies. Two separate "channels" in the disk controller are used to exchange data, status, and command information with the computer. The command and status lines are handled in one channel, and the input data and output data lines in the other channel.

Two data I/O buffer registers, the WRITE REGISTER and the READ REGISTER, are implemented on the READ/WRITE LOGIC card. Data are steered to/from these registers via the data channel of the Computer I/O card. During a write operation, the "WBnn-I" lines are steered to the WRITE REGISTER; during a read operation, the READ REGISTER outputs are gated onto the "RBnn-I" lines.

A DISK ADDRESS REGISTER is implemented on the Computer I/O card; the disk address bits are loaded into this register by the control channel of the Computer I/O card. The DISK ADDRESS REGISTER is actually loaded on the leading edge of the command strobe "CSTRB-I".

Command decode logic and the mode Flip Flops are contained on this card. On the trailing edge of the command strobe "CSTRB-I" the appropriate mode Flip Flops are set along with the FORMATTER BUSY Flip Flop; the setting of this busy Flip Flop actually initiates the track accessing, and subsequently the entering of the read/write sequence. "CSTRB-I" also causes the RATE ERROR Flip Flop of this card and the DATA ERROR Flip Flop of the READ/WRITE LOGIC card to be reset (if they were set by the previous operation).

The Computer I/O card generates the data transfer request "XFREQ-I" as a result of the read data transfer request "RST" or write data transfer request "WDR" being sent from the Read/ Write Logic card.

"FNBSY-I": The "FNBSY-I" FORMATTER BUSY FLIP FLOP is contained on the Computer I/O Card. This FLIP FLOP is set by "CSTRB-I" for each new command, and is cleared by the completion of the commanded sequence.

The Computer I/O card also contains the rate error "RERR-I" logic. The RATE ERROR Flip Flop is set if a data transfer strobe "DSTRB-I" is not received in response to each data transfer request "XFREQ-I".

The four remaining status lines (DERR-I, SDRDY+I", "SDTØØ-I" and "SDWPT-I") are gated by the control channel, but are generated on the Disk Interface card or the Read/Write Logic card.

6-4 READ/WRITE LOGIC

As previously discussed, when a read/write command is received the FORMATTER BUSY Flip Flop is set, and the track access portion of the sequence is initiated. When the access is completed ("TEQL" goes true) and the heads have settled out ("50MSC" goes false), the ADVANCE STATE Flip Flop "STAF" is set; it is the generation of "STAF" which causes the formatter to enter the actual read/ write state ("SCØ3" or "SCØ2").

The two STATE COUNT Flip Flops on the Read/Write Logic card (520-50104) provide for four states of the formatter:

"SCØØ"; power-up and reset.

"SCØ1"; idle/track access/seek.

"SCØ2"; write.

"SCØ3"; read.

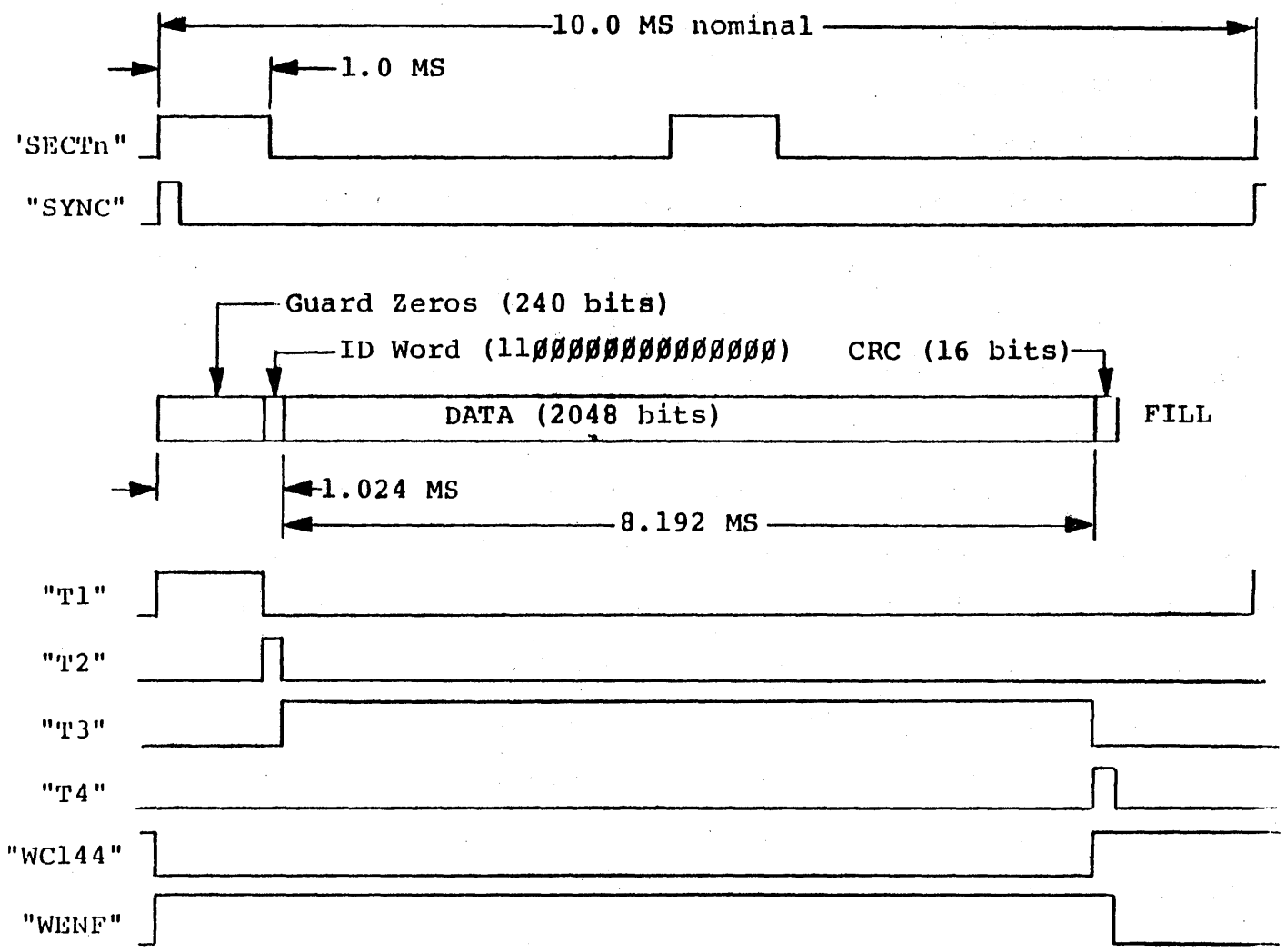
Upon completion of a read/write sequence, the formatter reverts to the idle state "SCØ1". This is accomplished by "END" going true; "END" is generated as a result of End-Read "ENDR", End-Write "ENDW", or "ABORT" going true.

6-4-1 FORMAT OF A SECTOR

Although there are thirty-two physical sector marks on a disk, these are divided by two on the Disk Interface card, and a sector of data is written on two physical sectors. A sector consists of fifteen Guard Zero words (240 bits), one 16-bit ID (synchronization) word, 128 16-bit Data words, a 16-bit CRC word, and the remainder of the sector is filled with zeros.

The function of Guard Zero words is to allow for the physical displacement between the read and write gaps on the head. At "SYNC" time in the write mode the write gap begins writing the Guard Zeros; however, at "SYNC" time in the read mode the read gap is already thru part of the Guard Zero portion of the sector.

The function of the ID word is to define (synchronize) to the read logic the beginning of valid data. The CRC word serves to perform a hardware parity check, thus verifying that the data portion of the sector was recovered correctly.



6-4-2 WRITE SEQUENCE

When "STAF" goes true, if the WRITE MODE Flip Flop is set the write state "SCØ2" is entered. This causes the WRITE ENABLE Flip Flop to set as soon as "SEQL" and "SYNC" go true. At this point (time "T1") the WRITE ID & DATA and the ENABLE CRC Flip Flops are reset, but the "WENn" line to the disk on the Disk Interface card has turned on the write current. Since the SHIFT

REG is cleared (by "ROW") "SHBØ" is zero; thus, only clock (zeros) will be sent to the disk via the "WDTn" line until "TAF" goes true.

When the R/W WORD COUNTER counts fifteen words, time "T2" is entered; this forces data bits 15 and 14 to true and the ID word is loaded into the SHIFT REG, along with the WRITE ID & DATA Flip Flop being set. Now the ID word (along with clock) is sent to the disk on "WDTn". When "TAF" went true the WRITE TRANSFER REQUEST Flip Flop "WDE" was also set; when the computer responds with a word, "WST" is generated, loading the word into the WRITE REG.

The next significant event is the WRITE BIT COUNTER counting sixteen bits having been sent to the disk; this is the beginning of time "T3". The contents of the WRITE REG are transferred to the SHIFT REG by "LOAD", and this data word is shifted to the disk. Another "WDE" is generated, and the computer responds with another word. When the WRITE BIT COUNTER has determined that the previous word has been shifted out, the next word is loaded into the SHIFT REG, and sent to the disk. This sequence continues until 144 words (fifteen Guard Zero words, the ID word, plus the 128 data words) have been sent to the disk.

When "WC144" goes true, time "T4" is entered. At this point the computed CRC contained in the CRC SHIFT REG is shifted to the disk. The next time the WRITE BIT COUNTER reaches a count of sixteen, End-Write "ENDW" is generated. This clears the WRITE ENABLE Flip Flop, returns the formatter to the idle state ("SCØ1"), and clears the WRITE MODE and FORMATTER BUSY Flip Flops on the Computer I/O.

6-4-3 READ SEQUENCE

When "STAF" goes true, if the READ MODE Flip Flop is set, the read state "SCØ3" is entered. This causes the READ ENABLE Flip Flop to set as soon as "SEQL" and "SYNC" go true. At this point, the read gap on the head is in the Guard Zero portion of the sector; the SERIAL DATA Flip Flop is thus supplying zeros to the SHIFT REG on the "OCF" line. The first ones seen will be those in the ID (synchronization) word.

The first time both "SHB14" and "SHB15" are true the ID WORD READ Flip Flop is set. Serial data continues to be supplied to the SHIFT REG, and is also routed to the CRC SHIFT REG at this time to commence the CRC computation. When "RTAF" went true, this caused the READ BIT COUNTER to start counting; when it reaches a count of sixteen, this indicates that the first data word has been recovered from disk and is in the SHIFT REG.

At this point the VALID READ DATA Flip Flop is set, the word is transferred to the READ REG, and a data transfer request is sent to the computer via the "RST" line.

Before the next word is completely assembled in the SHIFT REG, the computer will have accepted the word in the READ REG (if not, Rate Error will be set - see "RERR-I" description, page 1-11). When the READ BIT COUNTER again reaches a count of sixteen, the word will be transferred from the SHIFT REG to the READ REG, and another data transfer request is generated via "RST". This sequence continues until the R/W WORD COUNTER has reached a count of 128 ("WBC7" goes true).

At this point the 128 data words have been transferred, and the END OF DATA Flip Flop is set; now the CRC will be verified. When the eighth bit of the CRC word has been shifted into the CRC SHIFT REG (the "RBC3" signal from the READ BIT COUNTER goes true), "PTMP" is generated. If the computed CRC and the CRC read do not verify, the DATA ERROR Flip Flop is set by "PERL"; this informs the computer that an error was detected by the disk system while reading the sector.

The "PTM" signal also generates End-Read "ENDR". This resets the READ ENABLE Flip Flop, and also resets the FORMATTER BUSY Flip Flop on the Computer I/O card.

6-5 Expansion Box Interface

The Expansion Box Interface logic on Card J2 is shown on logic drawing 520-50102 in the appendicies. This card supports the individual lines required for the third and fourth drives; these lines are:

STEP IN
STEP OUT
LOAD HEAD
FILE UNSAFE RESET
WRITE ENABLE
SECTOR
INDEX
TRACK ØØ
FILE UNSAFE
WRITE PROTECT
SEP DATA
SEP CLOCK
WRITE DATA

The above lines are controlled and multiplexed similar to the manner as described in the Disk Interface section. The cable, which connects the drive in the Expansion Box,(through the JI C/D connector on the Expansion Box Interface)carries the same signal and power lines as the cables used on the Disk Interface Card.

VII MAINTENANCE

7-1 INTRODUCTION

This section contains maintenance and service information for the Dicom 422 Floppy Disk System. This includes recommended calibration and periodic test procedures, as well as periodic maintenance procedures.

7-2 POWER SUPPLY

The power supply module has been designed such that there are no adjustments required. However, the supply voltages should be checked at six month intervals to verify their correct output values: these are:

+5VDC	±0.2V	
+24VDC	(unregulated)	-2.0VDC, +4.0VDC
-12VDC	1.0VDC	-4.0VDC

7-3 DISK DRIVES

Refer to the sections in the Appendicies for periodic test and maintenance procedures. Dicom stronly recommends that for long, reliable life these procedures be followed at the specified time intervals. Further, to assure optimum performance the following performance and wear checks be performed at three to six months intervals.

7-3-1 DRIVE PRESSURE PAD

The pressure pad should be visually inspected at regular intervals, based on the number of hours that the pressure pad is in contact with the disk. Dicom recommends that every six months or 100 hrs. of head loaded operation, the pressure pad should be checked. Refer to the Flexible Disk File Maintenance Manual.

The pressure pad should be centered on it's mounting holder and should still have a felt touch. If off center or appears to be polished, the pad should be removed by pulling it off, and a new pad applied with its adhesive backing. These pads are available directly from the drive manufacturer.

7-3-2 DRIVE HEAD/WRITE HEAD

The Read/Write Head should be visually inspected while examining the pressure pad. Any excessive build up of oxide should be cleaned using a cleaning solution. Dicom recommends that the user performs the Head Read/Write Check, every six months or 1,000 hrs., which ever occurs first.

7-3-3 DRIVE BELT

Dicom recommends that the belt be wiped down with a cleaning solvent such as ISOPROPYL ALCOHOL every six months. When installing the belt after cleaning, turning the belt inside out, will yield more even wear. Cleaning the belt is recommended to clean off any dust particles that may be adhering to the belt, thus causing the belt to slip under insertion loads of a diskette.

7-4 DISK CONTROLLER

The 422 Disk Controller has been carefully designed to eliminate any required adjustments. However, due to component value changes there are a few timing circuits which should be checked at six month intervals to assure continous reliable system operation. These circuits, located on the Disk Interface logic card (520-50103), are:

SIGNAL	NAME	LOCATION	TIME AND TOLERANCE
STEP PULSE	1MSC*	U27-pin4	1msec -.5msec, +1.0msec
STEP DELAY	1ØMSC*	U27-pin12	10.5msec ±0.5msec +5.0msec
HEAD SETTLE	5ØMSC*	U49-pin4	50msec -10.0msec,+20.0msec
RDY1 DELAY	ROS1	U48-6	7.5msec ±2.0msec
RDY2 DELAY	ROS2	U48-14	7.5msec ±2.0msec

* NOTE: TO TEST "RDYn" DELAY, a Diskette must be installed so that sector timing pulses will be generated. The signal at pins 6 and 14 will be of the capacitor discharge cycle, which will retrigger at 5msec intervals. Since the circuit is always being retriggered before it times out, the output of U48 pins 5 and 13 respectively will always be positive if a diskette is installed, and low if a diskette is removed, or not rotating. To verify the timers, disconnect AC power to the drive in question and rotate it slowly by hand.

These same equivalent circuits are located on the Expansion Box Interface card if an Expansion Box is installed.

7-5 DISK DRIVE P-ADAPTOR (520-50113)

The Disk Drive P-Adaptor is designed to facilitate the use of the Pertec Disk Drive with the Disk Controller. The adapter performs the separation of data and clock pulses, as well as index and sector pulses. There are three primary timing circuits on the Adaptor card which is mounted to the rear connector of each drive.

Two of the timing circuits use fix timing components, while one circuit, the separate data/clock, requires adjustment of a variable re sistor.

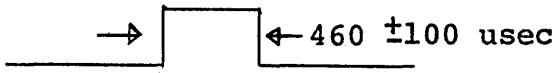
The following procedure should be used to verify and adjust these circuits.

7-5-1 INDEX AND SECTOR PULSE WIDTH

(a) Install a hard sectored diskette.

(b) With the door closed, and diskette rotating verify that the pulse at U-11 pin #6 is 460 usec ±100 usec 7412

Index/Sector Pulse Width (U11 - pin 6)



7-5-2 INDEX TIME OUT

(a) With the diskette rotating as per 5-5-1, verify the delay time between sector pulses which allows the index timer to time out.

(b) Verify that the pulse width at U9 - pin 4 is 3.9msec ±.5msec

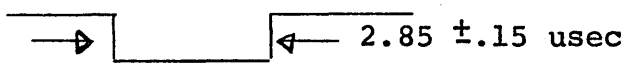
Index - Time Out (U9 - pin #4)

7-5-3 CLOCK/DATA SEPARATOR

(a) With a previously written diskette installed as per 5-5-1, monitor U9 - pin 12.

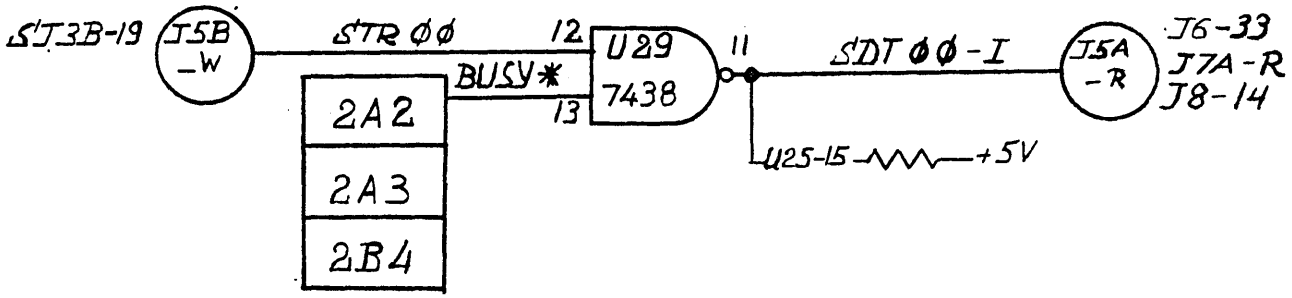
(b) Adjust the variable resistor located adjacent to U9 for a pulse width of 2.85 ±.15 usec

Clock/Data Separator (U9 - pin 12)



7-6 LOGIC DIAGRAM CONVENTIONS

As an example of the conventions used in the logic diagrams, consider the following excerpt from the COMPUTER I/O Card, drawing 520-50105, sheet 2 of 3, zone A4.



The circle indicates a connection to the Motherboard Connector. The designation in front of the circle indicates were the signal is coming from. An S in front of the designator indicates that it is the source of the signal. The designator(s) to the right of the circle on output, indicate to which connector(s) the signal is sent.

The rectangular boxes indicate a connection somewhere else on this card, but the connection is shown at another place or sheet of this logic diagram. The coordinates inside the box define the sheet and zone. In this case, "BUSY*" originates on sheet 2, zones A2, A3, and B4.

The 2-NAND gate shown is located at U29 on the card. The gate is a 7438 type with input pins 12 and 13, and output on pin 11. The output signal SDTØØ-I exits the card at connector J5A pin R, which has mother board connections to J6-33, J7A-R, and J8-14. The signal is also connected to U25 pin 15 on the card. U25 is a resistor pack which is a 680-ohm pull-up; it is contained in a 16-pin DIP pack.

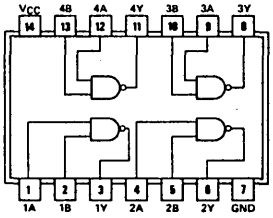
54/74 Family
SSI Circuits
MSI/LSI Circuits

ACTIVE COMPONENTS, MODEL 422 FDS CONTROLLER
(with one or two drives implemented)

ITEM	DICOM Part No.	QTY	DESCRIPTION
7400	100-02428	7	Quad 2-NAND
7402	100-02430	2	Quad 2-NOR
7404	100-02431	12	Hex Inverter
7408	100-02433	16	Quad 2-AND
7410	100-02435	3	Triple 3-NAND
7411	100-02846	2	Triple 3-AND
7416	100-02790	4	Hex Inverter, Open Collector
7417	100-02891	2	Hex Buffer, Open Collector
7420	100-02436	1	Dual 4-NAND
7425	100-02849	1	Dual 4-NOR
7432	100-02836	6	Quad 2-OR
7433	100-02909	1	Quad 2-NOR
7438	100-02851	17	Quad 2-NAND, Open Collector
7474	100-02440	9	Dual D-Type Flip-Flop
7476	100-02443	1	Dual J-K Flip-Flop
7485	100-02853	10	4-bit Magnitude Comparator
7486	100-02442	1	Quad 2-EX-OR
74H11	100-02847	3	Triple 3-AND
74H21	100-02848	1	Dual 4-AND
74107	100-02860	6	Dual J-K Master/Slave Flip-Flop
74123	100-02461	4	Dual One-Shots
74153	100-02861	6	Dual 4-to-1 Multiplexer
74162	100-02854	1	Synchronous 4-bit Counter
74164	100-02855	2	8-bit Parallel/Serial Shift Register
74174	100-02857	6	Hex D-Type Flip-Flop
74175	100-02858	2	Quad D-Type Flip-Flop
74193	100-02859	10	4-bit Up/Down Counter
74199	100-02856	2	Broadside-load 8-bit Shift Register
1N4005	112-02382	5	Diode
M5060	115-02413	1	SCR
- - -	165-02684	15	LED (Red; HP-5082-4850)
- - -	165-02878	3	LED (Green; HP-5082-4984)
- - -	165-02879	3	LED (Yellow; HP-5082-4550

00
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

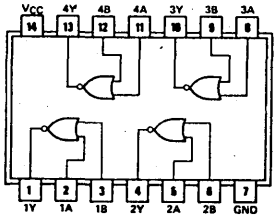
positive logic:
$Y = \overline{AB}$



SN5400/SN7400(J N)

02
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

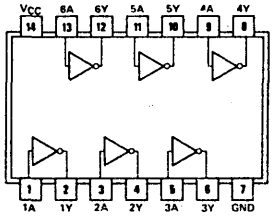
positive logic:
$Y = \overline{A+B}$



SN5402/SN7402(J, N)

04
HEX INVERTERS

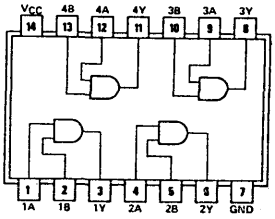
positive logic:
$Y = \overline{A}$



SN5404/SN7404(J, N)

08
QUADRUPLE 2-INPUT POSITIVE-AND GATES

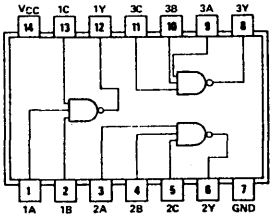
positive logic:
Y = AB



SN5408/SN7408(J, N, W)

10
TRIPLE 3-INPUT POSITIVE-NAND GATES

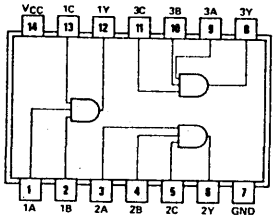
positive logic:
$Y = \overline{ABC}$



SN5410/SN7410(J, N)

11
TRIPLE 3-INPUT POSITIVE-AND GATES

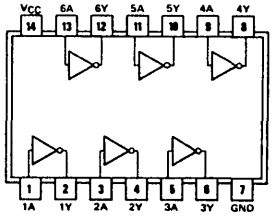
positive logic:
Y = ABC



SN54H11/SN74H11(J, N)

16
HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTCR HIGH-VOLTAGE OUTPUTS

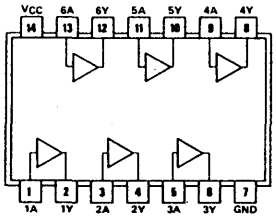
positive logic:
$Y = \overline{A}$



SN5416/SN7416(J, N, W)

17
HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

positive logic:
Y = A

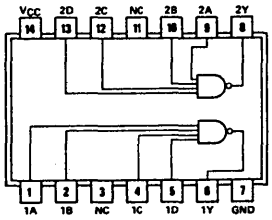


SN5417/SN7417(J, N, W)

20

DUAL 4-INPUT POSITIVE-NAND GATES

positive logic:
$Y = \overline{ABCD}$

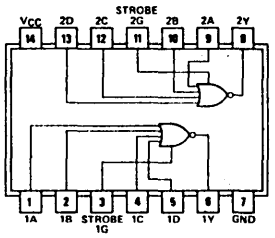


SN5420/SN7420(J, N)

25

DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE

positive logic:
$Y = \overline{G(A+B+C+D)}$

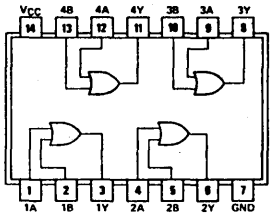


SN5425/SN7425 (J, N, W)

32

QUADRUPLE 2-INPUT POSITIVE-OR GATES

positive logic:
Y = A+B

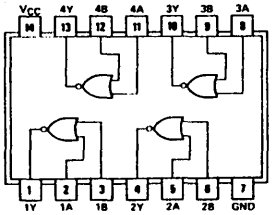


SN5432/SN7432(J, N, W)

33

QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS WITH OPEN-COLLECTOR OUTPUTS

positive logic:
$Y = \overline{A+B}$

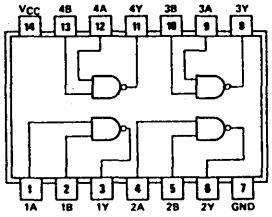


SN5433/SN7433(J, N, W)
SN54LS33/SN74LS33(J, N, W)

38

QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

positive logic:
$Y = \overline{AB}$



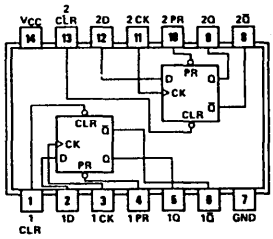
SN5438/SN7438(J, N, W)

74

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$



SN5474/SN7474(J, N)

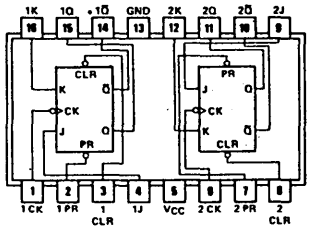
H = high level (steady state), L = low level (steady state), X = irrelevant
⎍ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.
↑ = transition from low to high level, ↓ = transition from high to low level
Q_0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

76

DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR

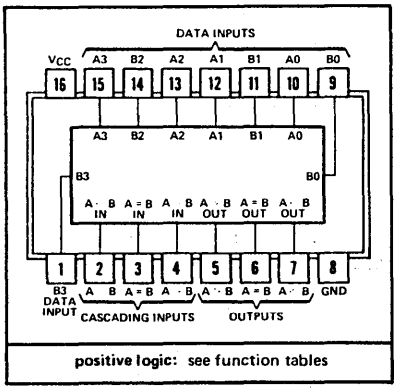
'76, 'H76
FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\overline{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

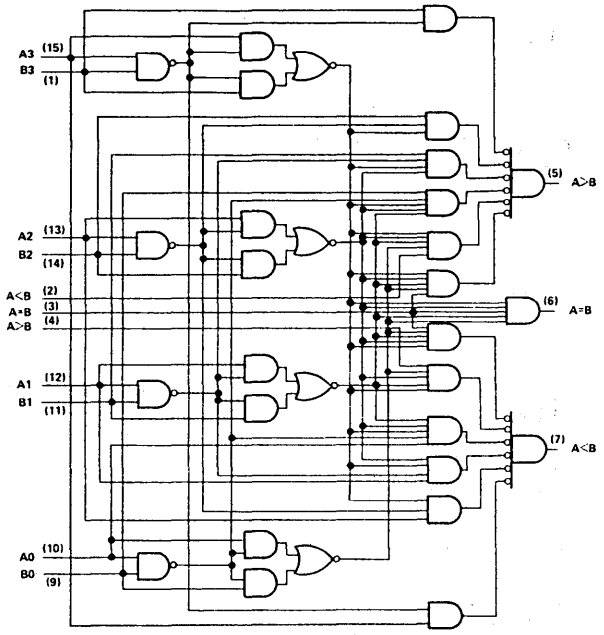


SN5476/SN7476(J, N, W)

SN7485
4-BIT MAGNITUDE COMPARATORS



positive logic: see function tables



description

These four-bit magnitude comparators perform comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding A > B, A < B, and A = B inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A = B input and additionally for the 'L85, low-level voltages applied to the A > B and A < B inputs. The cascading paths of the '85 and 'S85 are implemented with only a two-gate-level delay to reduce overall comparison times for long words. An alternate method of cascading which further reduces the comparison time is shown in the typical application data.

FUNCTION TABLES

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

'85, 'S85

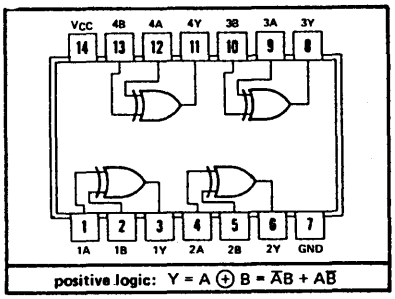
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

SN7486
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level



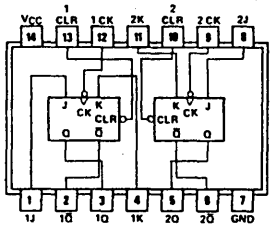
positive logic: $Y = A \oplus B = \overline{A}B + A\overline{B}$

107

DUAL J-K MASTER-SLAVE FLIP-FLOPS WITH CLEAR

FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	⎍	L	L	Q_0	$\bar{Q}_0$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	TOGGLE	



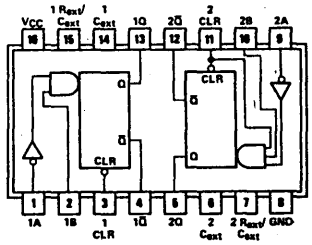
SN54107/SN74107(J, N)

123

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎



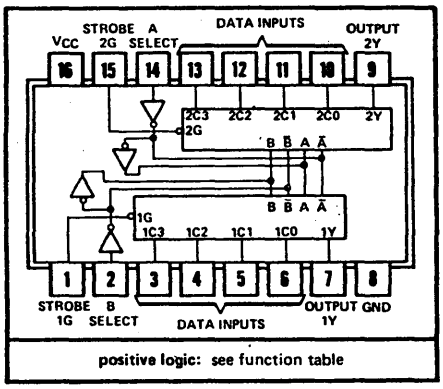
SN54123/SN74123(J, N, W)

H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎎ = one low-level pulse, X = irrelevant (any input, including transitions).
To use the internal timing resistor of '121, 'L121, '122, or 'L122, connect R_{int} to V_{CC}.
An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
For accurate repeatable pulse widths, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.
To obtain variable pulse widths, connect external variable resistance between R_{int} or R_{ext}/C_{ext} and V_{CC}.

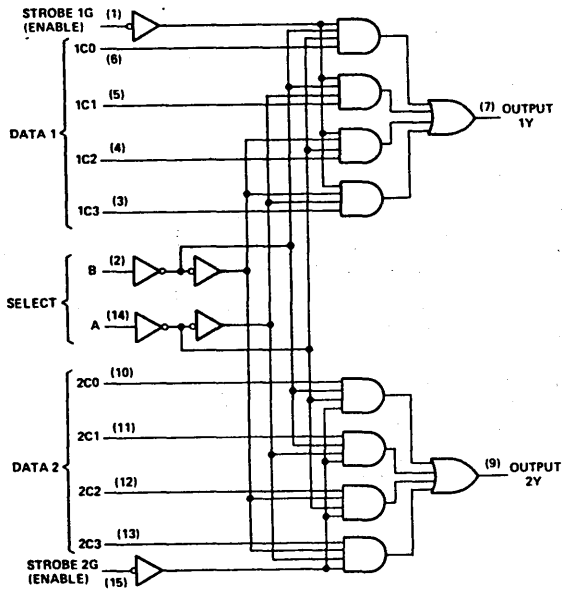
SN74153
DUAL 4-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

description

Each of these monolithic, data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.



positive logic: see function table

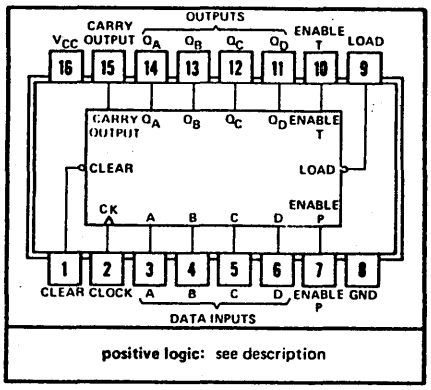


FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

SN54162
SYNCHRONOUS 4-BIT COUNTER



positive logic: see description

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting schemes. The '160 and '162 are decade counters and the '161 and '163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four J-K master-slave flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input should be avoided when the clock is low if the enable inputs are high at or before the transition. The clear function for the '160 and '161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load, or enable inputs. The clear function for the '162 and '163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

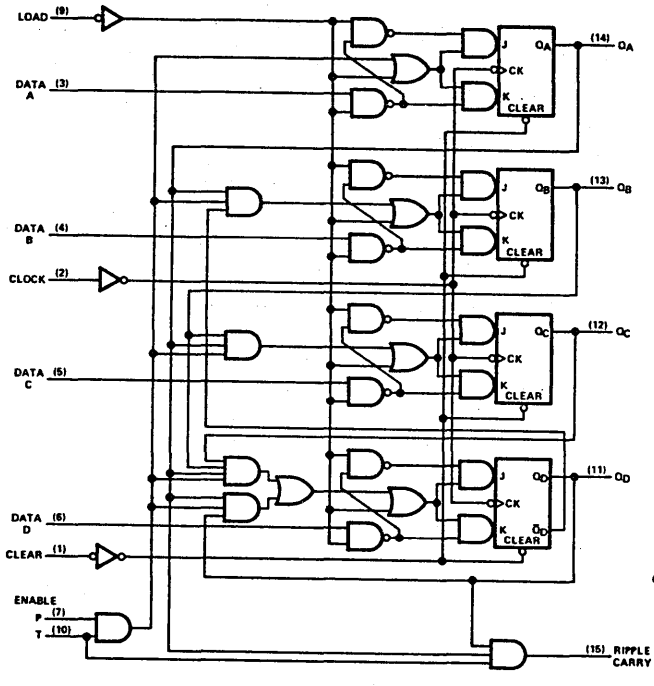
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the carry output. The carry output thus enabled will produce a positive output pulse with a duration approximately equal to the positive portion of the Q_A output. This positive overflow carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs should occur only when the clock input is high.

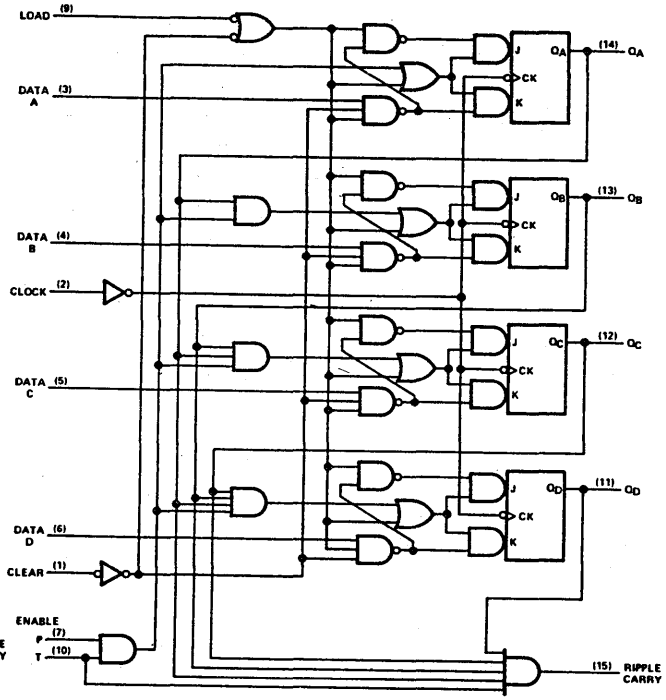
SN54160, SN74160 SYNCHRONOUS DECADE COUNTERS

SN54162, SN74162 synchronous decade counters are similar; however the clear is synchronous as shown for the SN54163, SN74163 binary counters at right.

SN54163, SN74163 SYNCHRONOUS BINARY COUNTERS

SN54161, SN74161 synchronous binary counters are similar; however, the clear is asynchronous as shown for the SN54160, SN74160 decade counters at left.

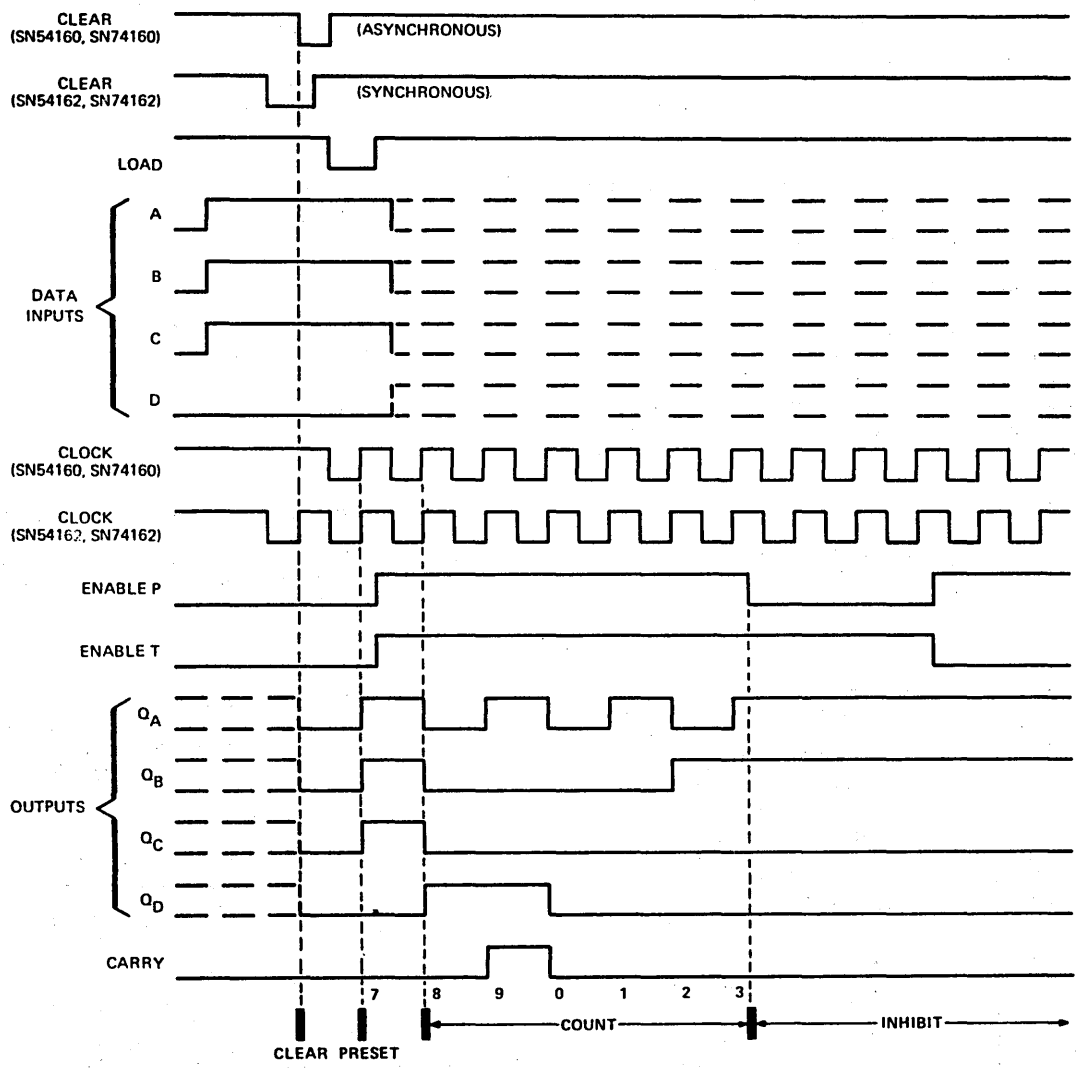




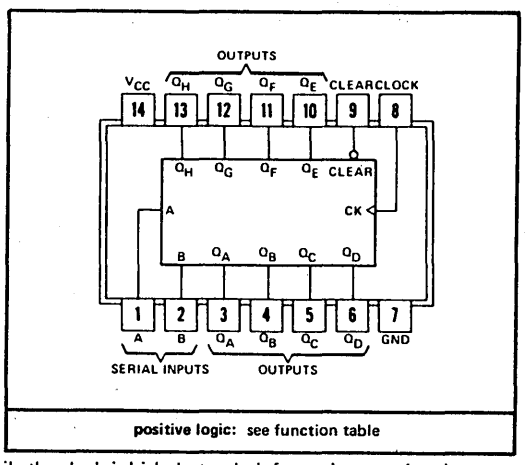
typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit



SN74164
8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS



positive logic: see function table

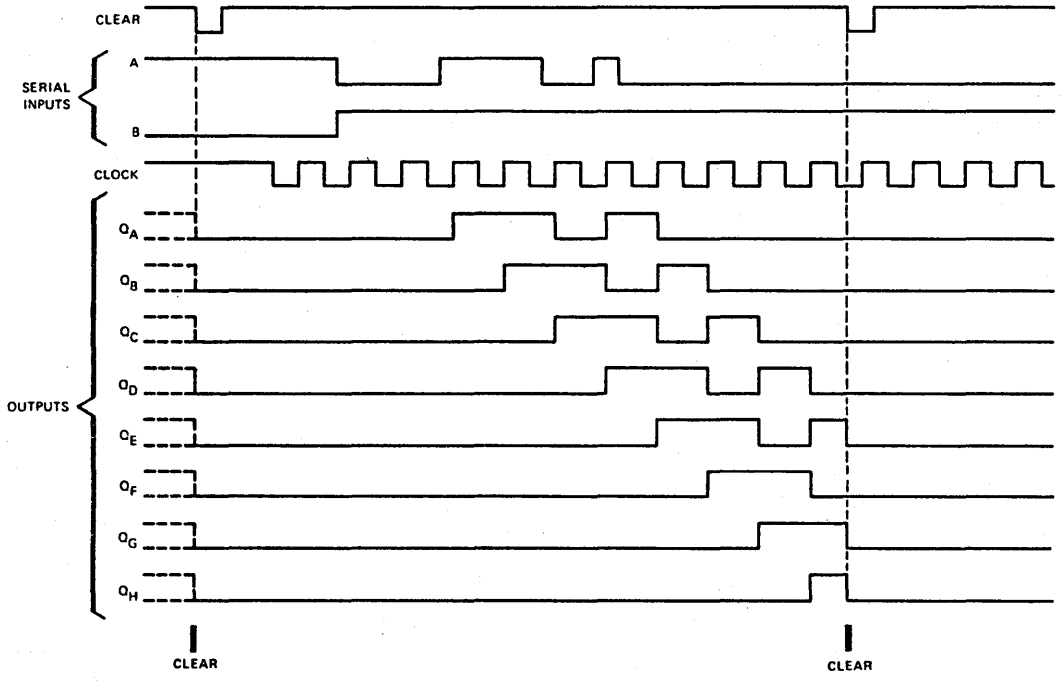
description

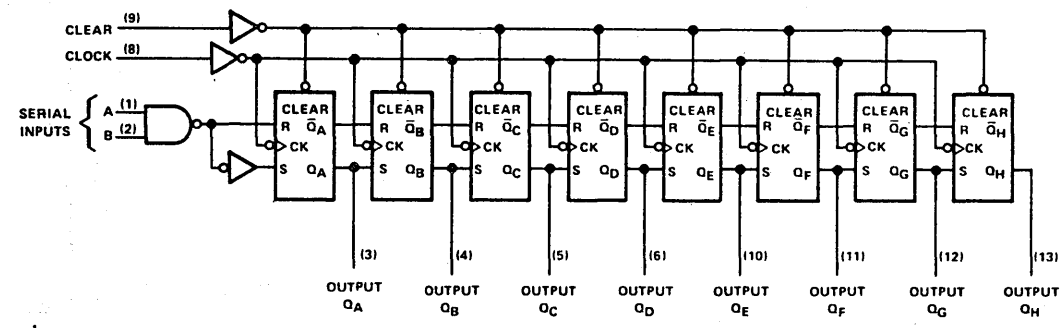
These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input.

INPUTS				OUTPUTS			
CLEAR	CLOCK	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L		L
H	L	X	X	Q_{A0}	Q_{B0}		Q_{H0}
H	↑	H	H	H	Q_{An}		Q_{Gn}
H	↑	L	X	L	Q_{An}		Q_{Gn}
H	↑	X	L	L	Q_{An}		Q_{Gn}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level.
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.

typical clear, shift, and clear sequences

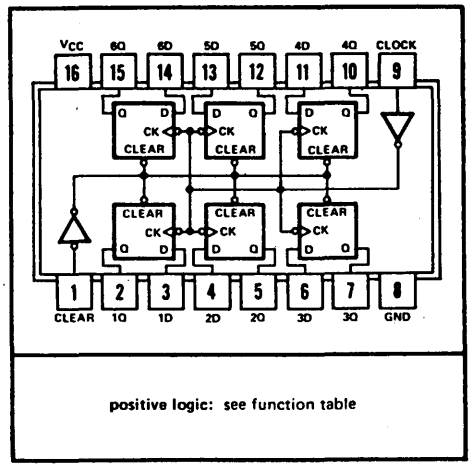




⊣◇ . . . . dynamic input activated by transition from a high level to a low level

SN74S174, SN74S175
HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

SN54S174 . . . J OR W PACKAGE
'174, 'LS174, SN74S174 . . . J, N, OR W PACKAGE
(TOP VIEW)



positive logic: see function table

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the '175, 'LS175, and 'S175 feature complementary outputs from each flip-flops.

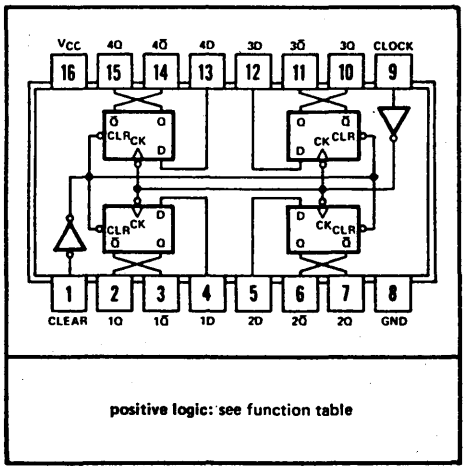
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

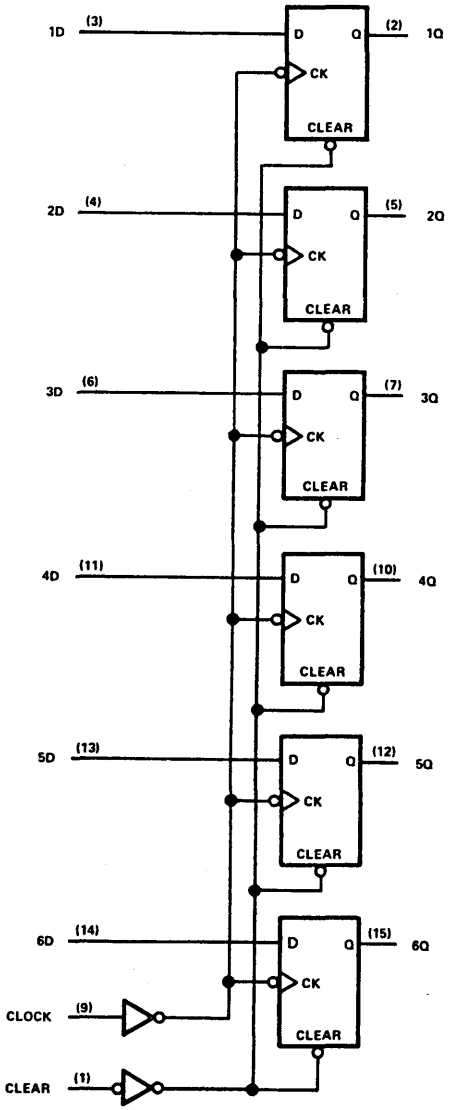
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
† = '175, 'LS175, and 'S175 only

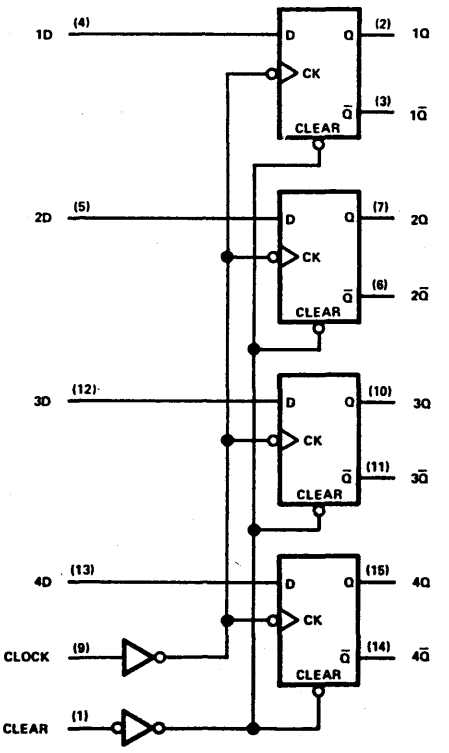
'175, 'LS175, 'S175 . . . J, N, OR W PACKAGE
(TOP VIEW)



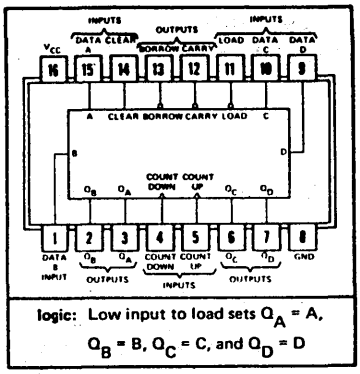
positive logic: see function table

dynamic input activated by transition from a high level to a low level.





SN74193
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)



logic: Low input to load sets Q_A = A, Q_B = B, Q_C = C, and Q_D = D

description

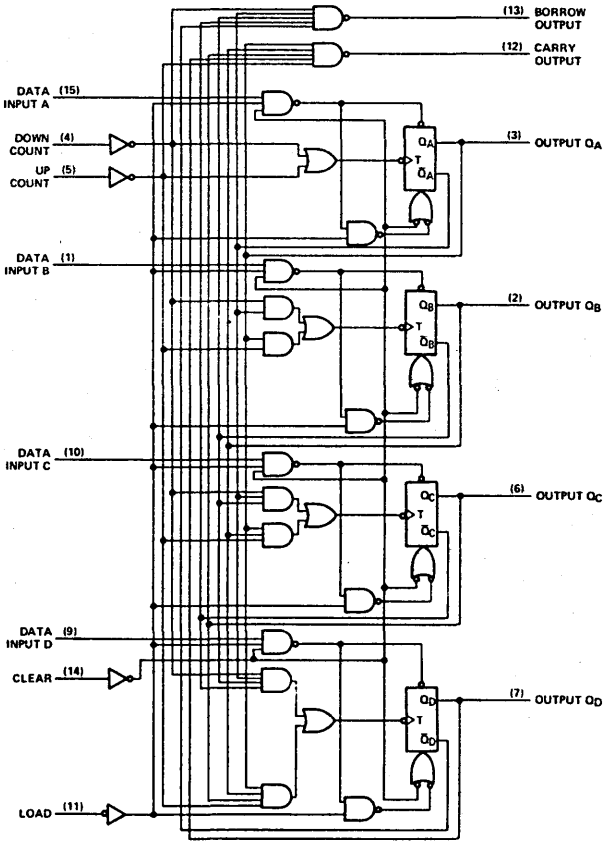
These monolithic circuits are synchronous reversible (up/down) counters having a complexity of 55 equivalent gates. The '192, 'L192, and 'LS192 circuits are BCD counters and the '193, 'L193 and 'LS193 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count inputs is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

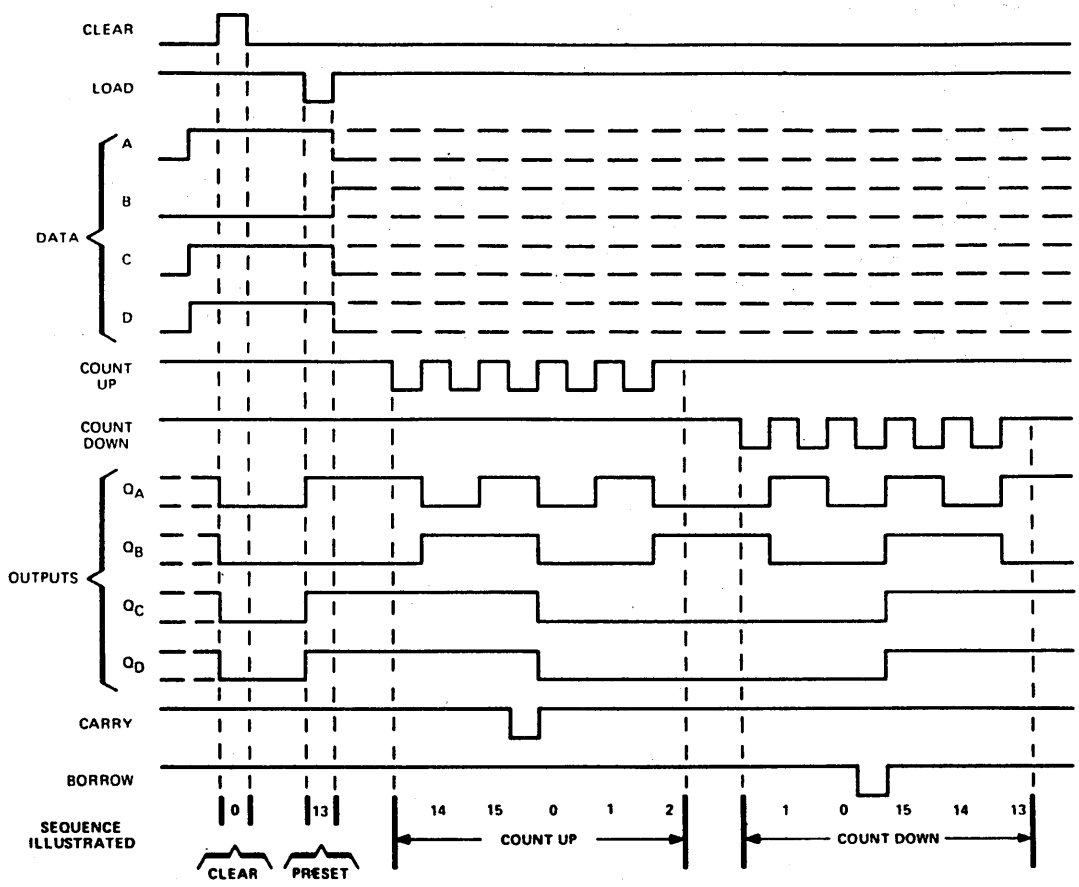


SN74193
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



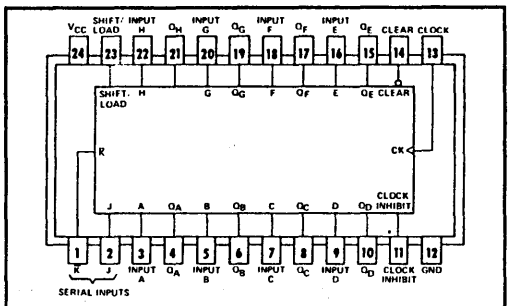
NOTES: A. Clear overrides load, data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.

These registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, a direct overriding clear line, and gated clock inputs. The register has three modes of operation:

Parallel (Broadside) Load
Shift (In the direction Q_A toward Q_H)
Inhibit Clock (Do nothing)

Parallel loading is accomplished by applying the eight bits of data and taking the shift/load control input low when the clock input is not inhibited. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.



positive logic: see function table

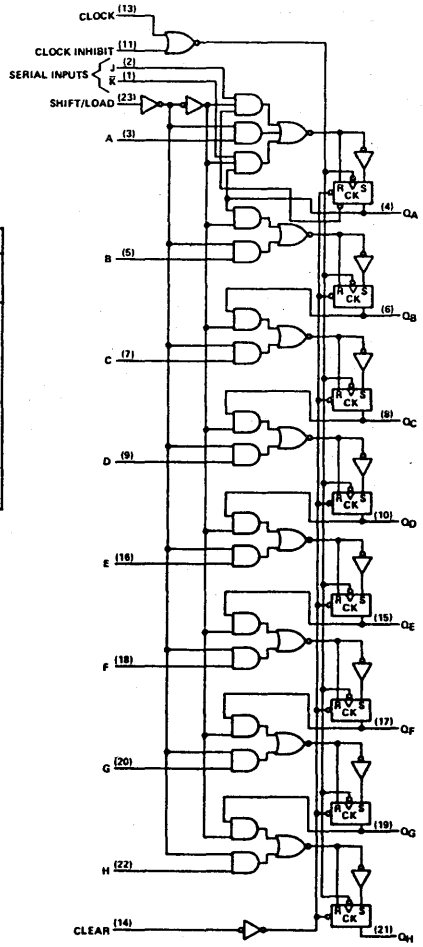
Shifting is accomplished synchronously when shift/load is high and the clock input is not inhibited. Serial data for this mode is entered at the J-$\overline{K}$ inputs. See the function table for levels required to enter serial data into the first flip-flop.

Both of the clock inputs are identical in function and may be used interchangeably to serve as clock or clock-inhibit inputs. Holding either high inhibits clocking, but when one is held low, a clock input applied to the other input is passed to the eight flip-flops of the register. The clock-inhibit input should be changed to the high level only while the clock input is high.

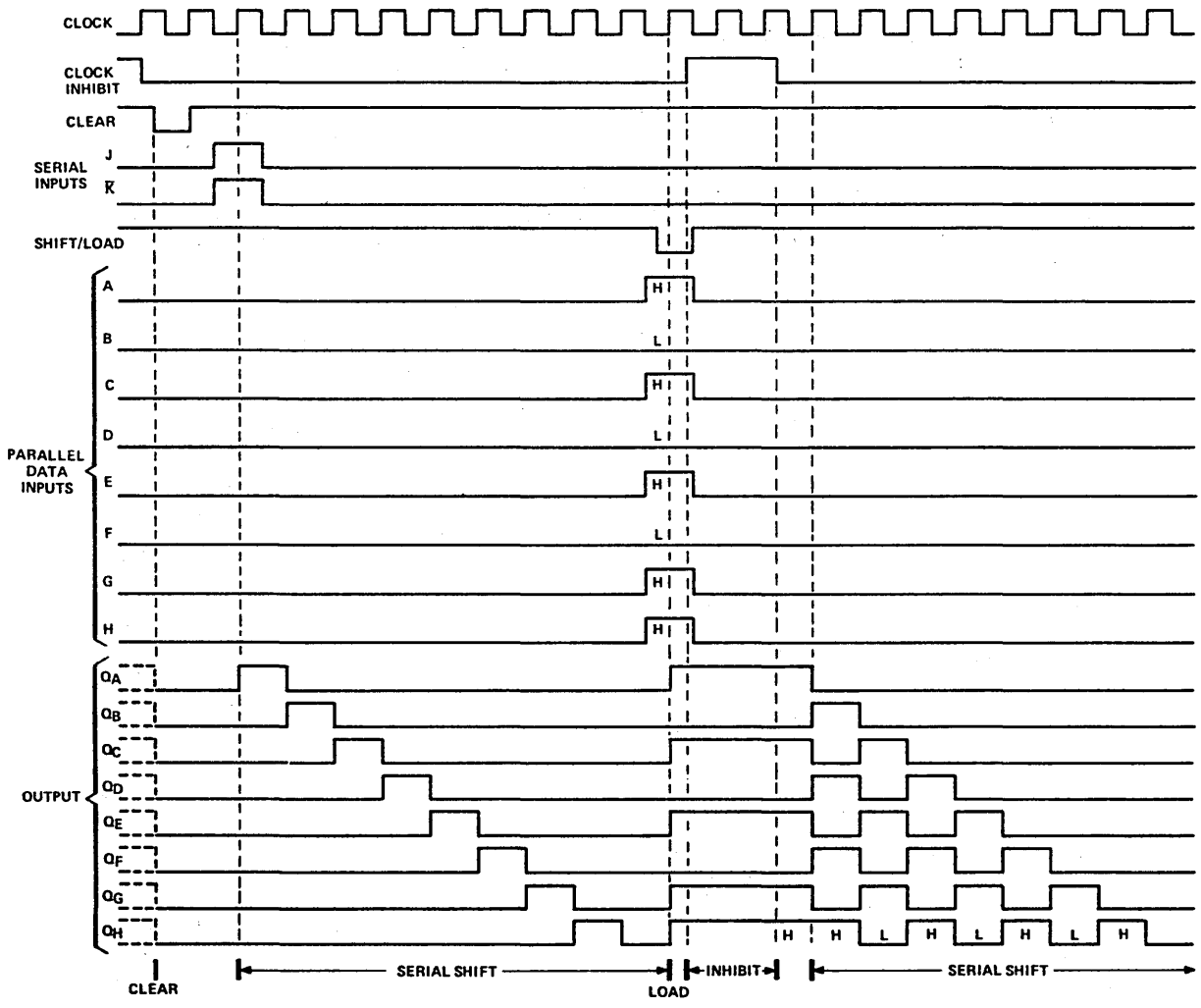
FUNCTION TABLE

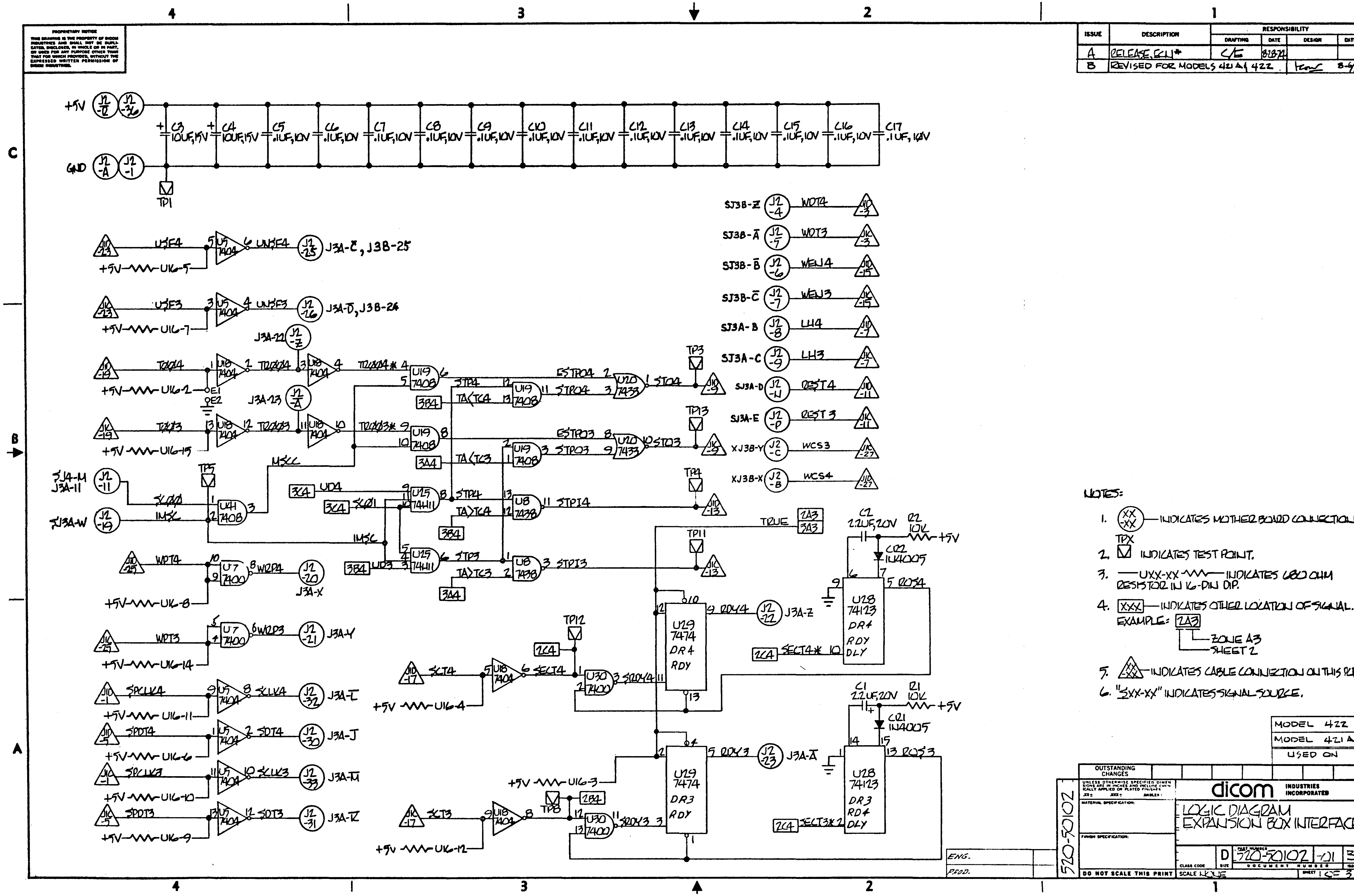
INPUTS							OUTPUTS			
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL J	SERIAL $\overline{K}$	PARALLEL A . . . H	Q_A	Q_B	Q_C . . .	Q_H
L	X	X	X	X	X	X	L	L	L	L
H	X	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{H0}
H	L	L	↑	X	X	a . . . h	a	b	c	h
H	H	L	↑	L	H	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Gn}
H	H	L	↑	L	L	X	L	Q_{An}	Q_{Bn}	Q_{Gn}
H	H	L	↑	H	H	X	H	Q_{An}	Q_{Bn}	Q_{Gn}
H	H	L	↑	H	L	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Gn}
H	X	H	↑	X	X	X	Q_{A0}	Q_{B0}	Q_{B0}	Q_{H0}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a . . . h = the level of steady-state input at inputs A thru H, respectively.
Q_{A0}, Q_{B0}, Q_{C0} . . . Q_{H0} = the level of Q_A, Q_B, or Q_C thru Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn} . . . Q_{Gn} = the level of Q_A or Q_B thru Q_G, respectively, before the most-recent ↑ transition of the clock.



typical clear, shift, load, and inhibit sequences

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ISSUE | DESCRIPTION | RESPONSIBILITY | DRAFTING | DATE | DESIGN | DATE
A | RELEASE, ECN# | C/E | 8/28/74
B | REVISED FOR MODELS 421A & 422
NOTES:
1. (XX -XX) INDICATES MOTHER BOARD CONNECTION
2. TPX INDICATES TEST POINT.
3. —UXX-XX-WW— INDICATES 680 OHM RESISTOR IN 16-PIN DIP.
4. XXX —INDICATES OTHER LOCATION OF SIGNAL. EXAMPLE: 2A3 —ZONE A3 —SHEET 2
5. INDICATES CABLE CONNECTION ON THIS P.C.B.
6. "SXX-XX" INDICATES SIGNAL SOURCE.
MODEL 422
MODEL 421A
USED ON
OUTSTANDING CHANGES
dicom INDUSTRIES INCORPORATED
LOGIC DIAGRAM
EXPANSION BOX INTERFACE
D 520-50102 -01 3
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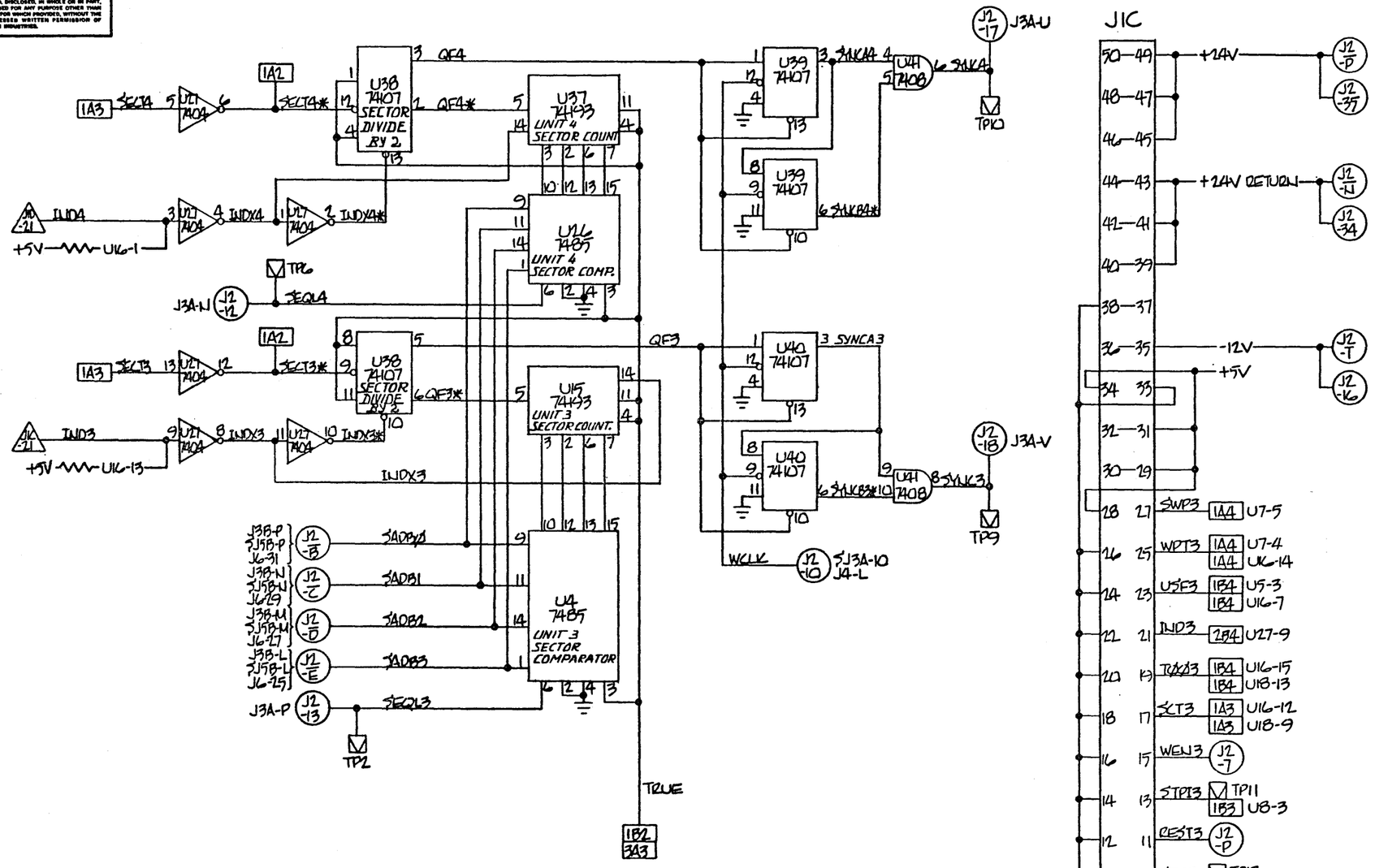
SHEET 1 OF 3
520-50102
ENG.
PROD.

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE



JIC

50–49	+24V		J2 -D, J2 -35
48–47			
46–45			
44–43	+24V RETURN		J2 -N, J2 -34
42–41			
40–39			
38–37			
36–35	-12V		J2 -T
34–33	+5V		J2 -K
32–31			
30–29			
28–27	SWP3	1A4	U7-5
26–25	WPT3	1A4	U7-4
		1A4	U16-14
24–23	USF3	1B4	U5-3
		1B4	U16-7
22–21	IND3	2B4	U27-9
20–19	TDX03	1B4	U16-15
		1B4	U18-13
18–17	SCT3	1A3	U16-12
		1A3	U18-9
16–15	WEN3	J2 -7	
14–13	STPI3	TP11	
		1B3	U8-3
12–11	RESI3	J2 -P	
10–9	STO3	TP13	
		1B3	U20-10
8–7	LH3	J2 -9	
6–5	SPDT3	1A4	U5-13
		1A4	U16-9
4–3	WDT3	J2 -5	
2–1	SPCLK3	1A4	U5-11
		1A4	U16-10

NOTES (REF):

1. (XX -XX) — INDICATES MOTHER BOARD CONNECTION TPX
2. TPX — INDICATES TEST POINT.
3. —UXX-XX— INDICATES 680 OHM RESISTOR IN 16-PIN DIP.
4. XXX — INDICATES OTHER LOCATION OF SIGNAL. EXAMPLE: 2A3 — ZONE A3, SHEET 2
5. (XX -XX) — INDICATES CABLE CONNECTION ON THIS PCB
6. "XX-XX" INDICATES SIGNAL SOURCE.

OUTSTANDING CHANGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES. .XX ± .005 ANGLES ±

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LOGIC DIAGRAM EXPANSION BOX INTERFACE

CLASS CODE D | SIZE | CAGE NUMBER 520-50102 | DOCUMENT NUMBER -01 | ISSUE B

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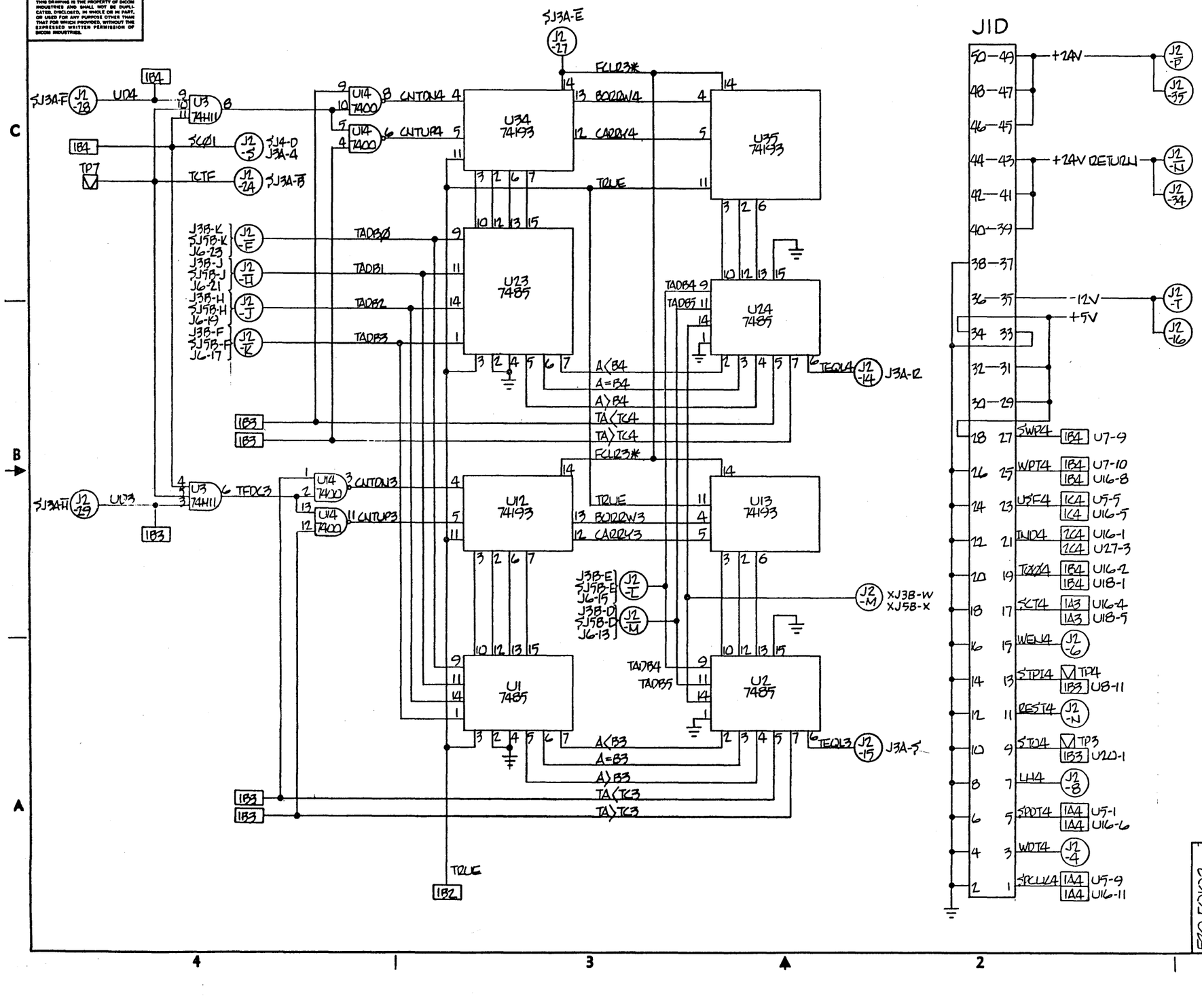
520-50102

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE



NOTES (REF):

1. (XX / -XX) — INDICATES MOTHER BOARD CONNECTION. TPX
2. ☑ INDICATES TEST POINT.
3. —UXX-XX— INDICATES 680 OHM RESISTOR IN 16-PIN DIP.
4. [XXX] — INDICATES OTHER LOCATION OF SIGNAL. EXAMPLE: [2A3] — ZONE A3, SHEET 2
5. ⚠ XX / XXX — INDICATES CABLE CONNECTION ON THIS PCB.
6. "XX-XX" INDICATES SIGNAL SOURCE.

OUTSTANDING CHANGES

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.XX ± .XXX ± ANGLES ±
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LOGIC DIAGRAM EXPANSION BOX INTERFACE

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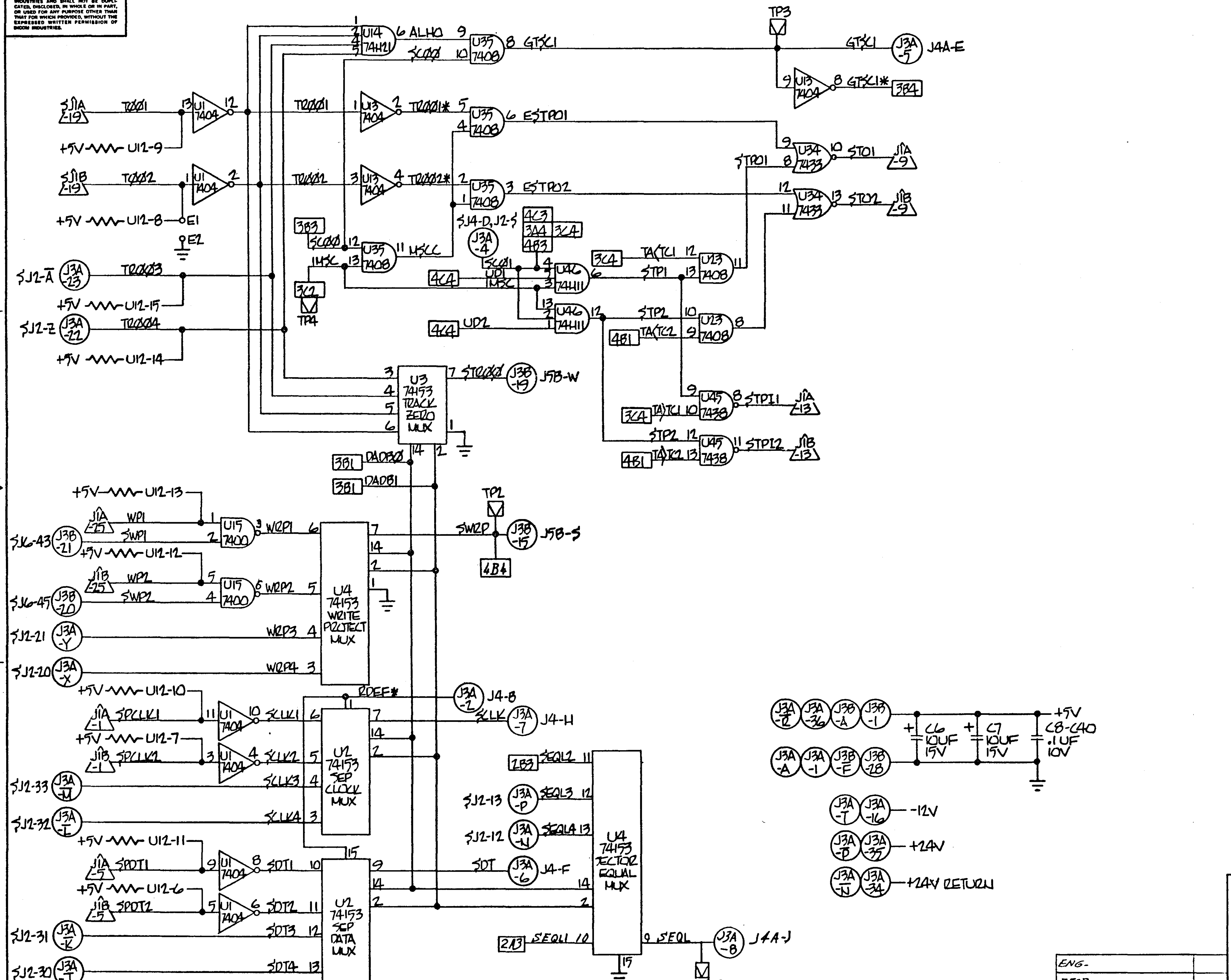
520-50102

ISSUE	DESCRIPTION	DRAFTING	DATE	DESIGN	DATE
A	RELEASE, ECN #	C/E	8/28/74		
B	REVISED FOR MODELS 421A/422				3-5/76



NOTES:

1. (XX -XX) —INDICATES MOTHER BOARD CONNECTION.
2. TPX [ ] INDICATES TEST POINT.
3. —UXX-XX-/\/\/\— INDICATES 680 OHM RESISTOR IN 16 PIN DIP.
4. [XXX]—INDICATES OTHER LOCATION OF SIGNAL. EXAMPLE: [2A3] —ZONE A3 —SHEET 2
5. (triangle) INDICATES CABLE CONNECTION ON THIS PCB.
6. "SXX-XX" INDICATES SIGNAL SOURCE.

MODEL 421A
MODEL 422
USED ON

OUTSTANDING CHANGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES

MATERIAL SPECIFICATION:

FINISH SPECIFICATION:

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LOGIC DIAGRAM DISK INTERFACE

D 520-50103-01 3

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520-50103

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE

NOTES (REF):
1. (XX / -XX) — INDICATES MOTHER BOARD CONNECTION.
2. TPX — INDICATES TEST POINT.
3. —UXX-XX-/\/\/\— INDICATES 680 OHM RESISTOR IN 16-PIN DIP.
4. XXX — INDICATES OTHER LOCATION OF SIGNAL. EXAMPLE: 2A3 — ZONE A3, SHEET 2
5. (XXX) — INDICATES CABLE CONNECTION ON THIS PCB.
6. "3XX-XX" INDICATES SIGNAL SOURCE.

OUTSTANDING CHANGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES AS FOLLOWS: .XX ± .XXX ± ANGLES ±
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LOGIC DIAGRAM
DISK INTERFACE

CLASS CODE D | SIZE | PART NUMBER 520-5103 -01 | DOCUMENT NUMBER | 3 ISSUE

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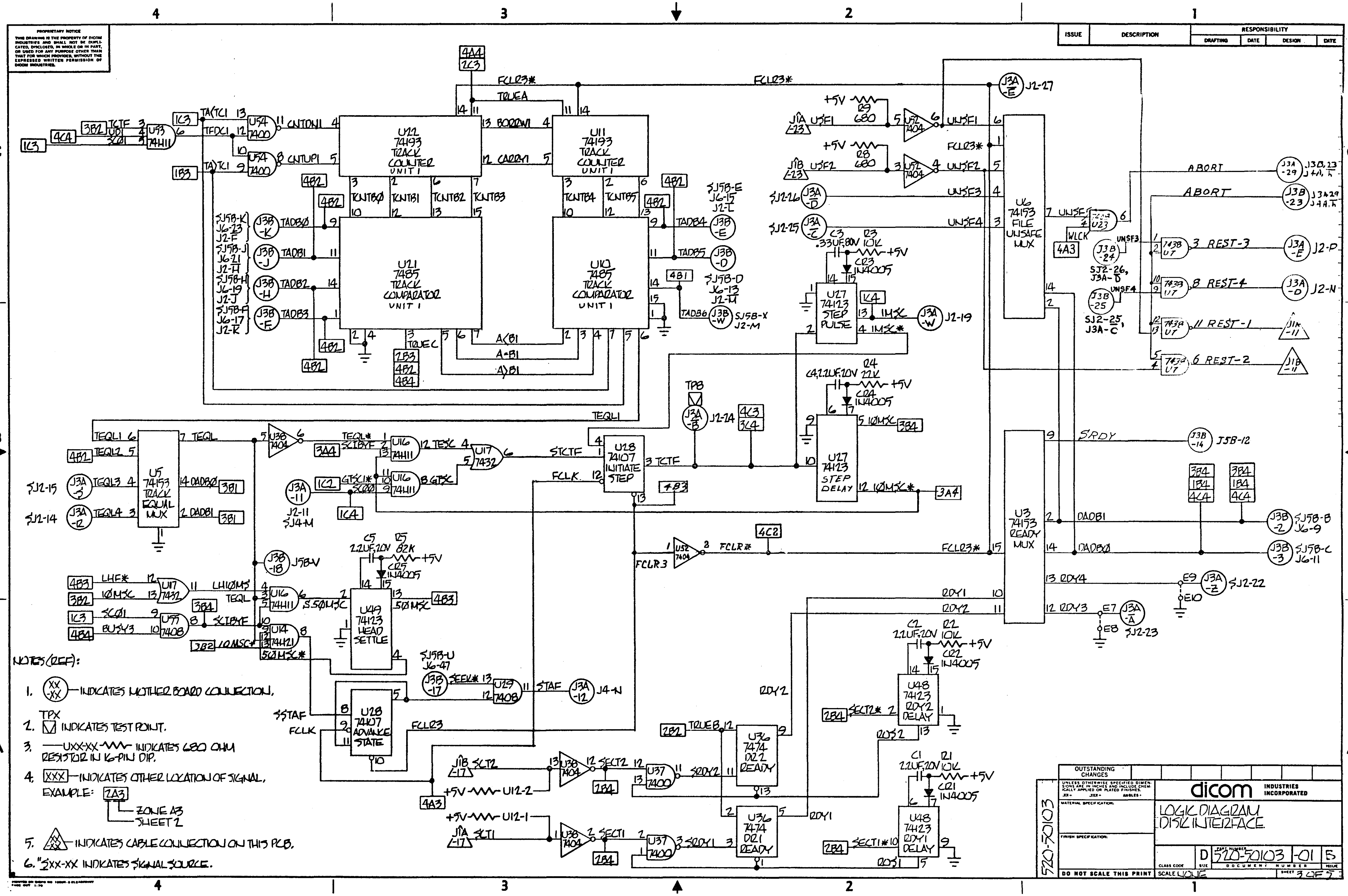
520-5103



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ISSUE
DESCRIPTION
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DATE
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DATE
U12 74193 TRACK COUNTER UNIT 1
U11 74193 TRACK COUNTER UNIT 1
U21 7485 TRACK COMPARATOR UNIT 1
U10 7485 TRACK COMPARATOR UNIT 1
U6 74153 FILE UNSAFE MUX
U27 74123 STEP PULSE
U27 74123 STEP DELAY
U28 74107 INITIATE STEP
U5 74153 TRACK EQUAL MUX
U3 74153 READY MUX
U49 74123 HEAD SETTLE
U28 74107 ADVANCE STATE
U36 7474 DR2 READY
U36 7474 DR1 READY
U48 74123 RDY2 DELAY
U48 74123 RDY1 DELAY
FCLR3*
TRUEA
BORROW1
CARRY1
ABORT
REST-3
REST-4
REST-1
REST-2
SRDY
NOTES (REF):
1. (XX -XX) — INDICATES MOTHER BOARD CONNECTION.
2. TPX INDICATES TEST POINT.
3. —UXX-XX-ᴧᴧᴧ— INDICATES 680 OHM RESISTOR IN 16-PIN DIP.
4. [XXX] — INDICATES OTHER LOCATION OF SIGNAL.
EXAMPLE: [2A3] ZONE A3, SHEET 2
5. INDICATES CABLE CONNECTION ON THIS PCB.
6. "$XX-XX INDICATES SIGNAL SOURCE.
OUTSTANDING CHANGES
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MATERIAL SPECIFICATION:
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LOGIC DIAGRAM DISK INTERFACE
D 520-50103 -01 5
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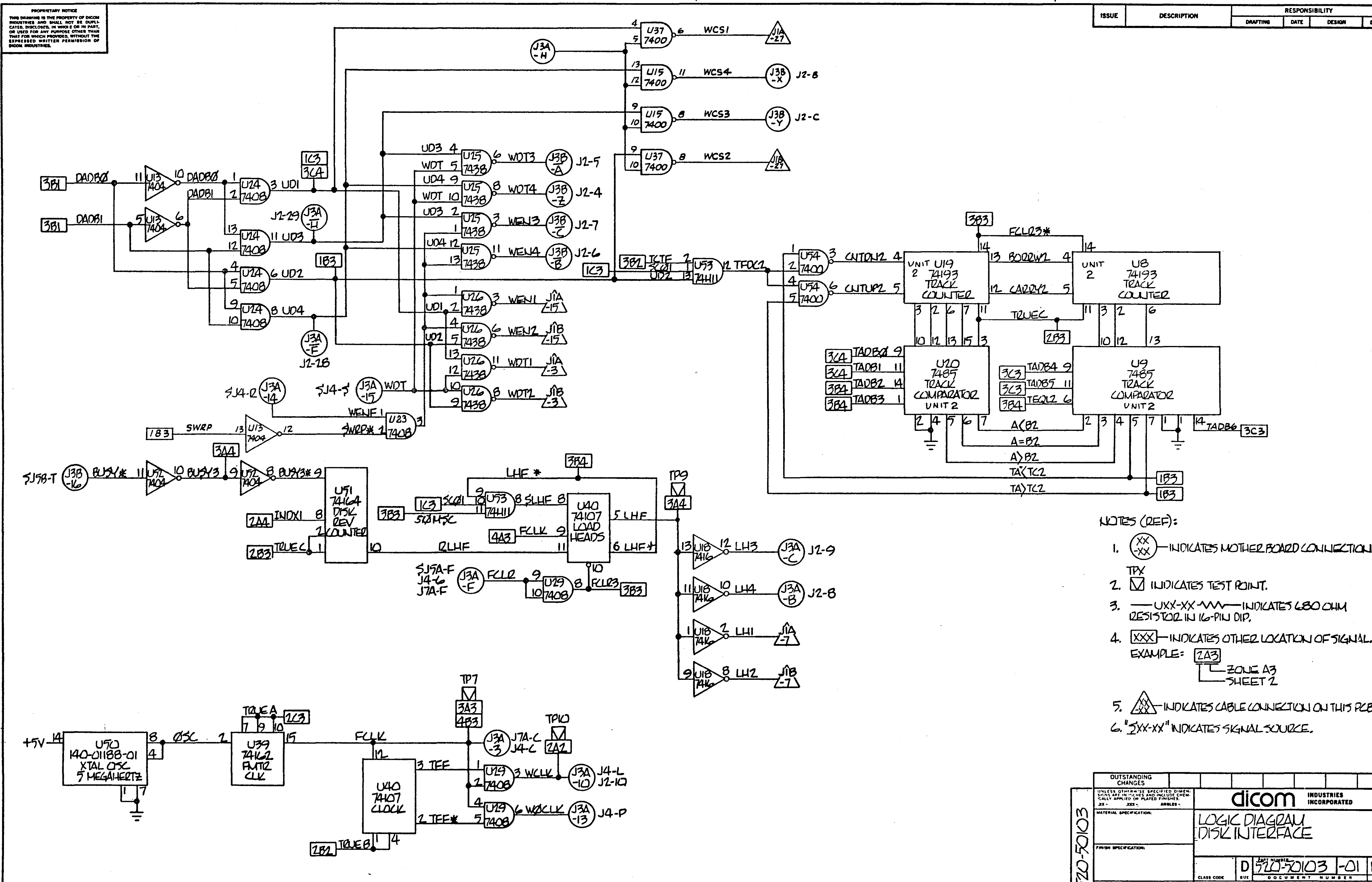
SHEET 3 OF 7
520-50103

ISSUE	DESCRIPTION	DRAFTING	DATE	DESIGN	DATE



NOTES (REF):

1. (XX/-XX) — INDICATES MOTHER BOARD CONNECTION.
2. TPX ☒ INDICATES TEST POINT.
3. —UXX-XX-ᐱᐯᐱ— INDICATES 680 OHM RESISTOR IN 16-PIN DIP.
4. [XXX] — INDICATES OTHER LOCATION OF SIGNAL.
   EXAMPLE: [2A3] — ZONE A3, SHEET 2
5. △ (XX/-XX) — INDICATES CABLE CONNECTION ON THIS PCB.
6. "ŹXX-XX" INDICATES SIGNAL SOURCE.

OUTSTANDING CHANGES

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LOGIC DIAGRAM DISK INTERFACE

CLASS CODE | SIZE D | DOCUMENT NUMBER 520-50103 -01 | ISSUE B

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520-50103

ISSUE	DESCRIPTION	RESPONSIBILITY			
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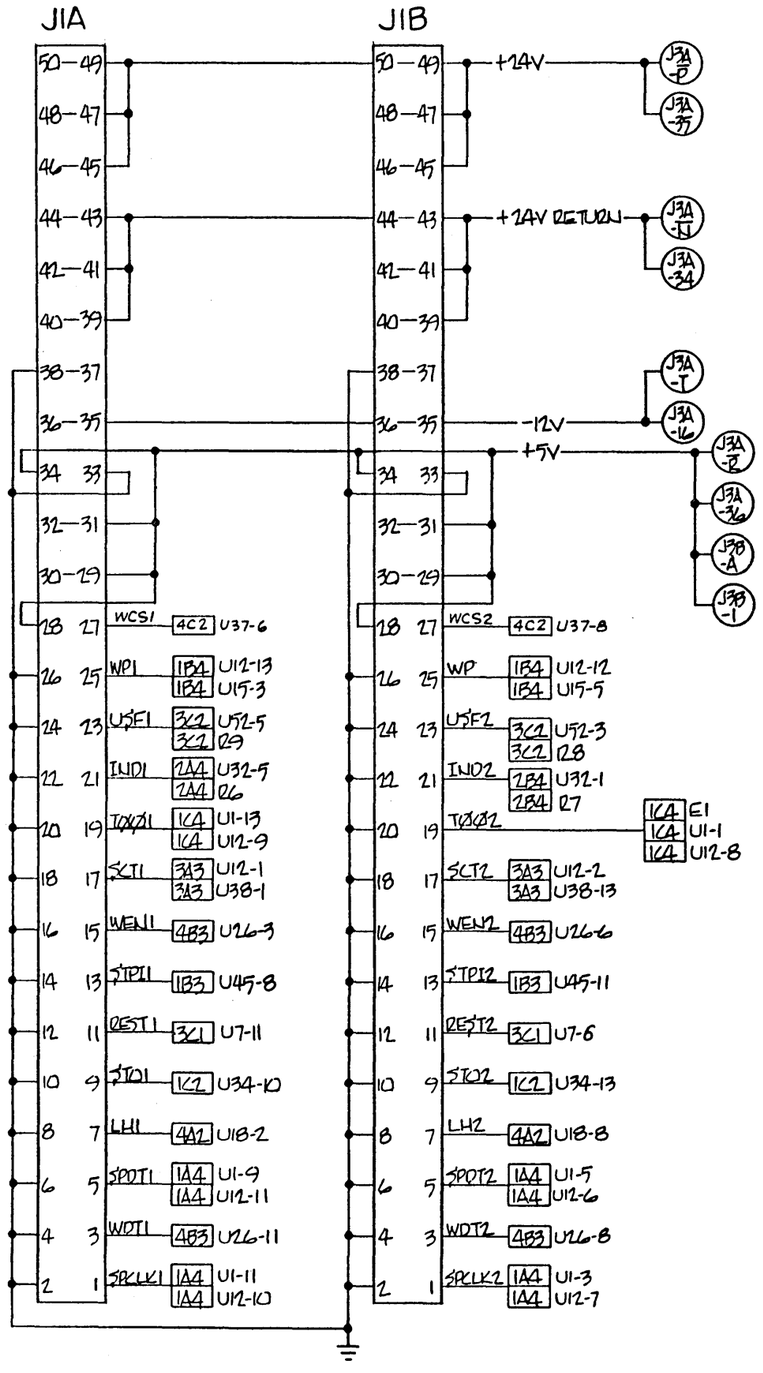

OUTSTANDING CHANGES

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.XX ± .XXX ± ANGLES ±

MATERIAL SPECIFICATION

FINISH SPECIFICATION

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LOGIC DIAGRAM
DISK INTERFACE

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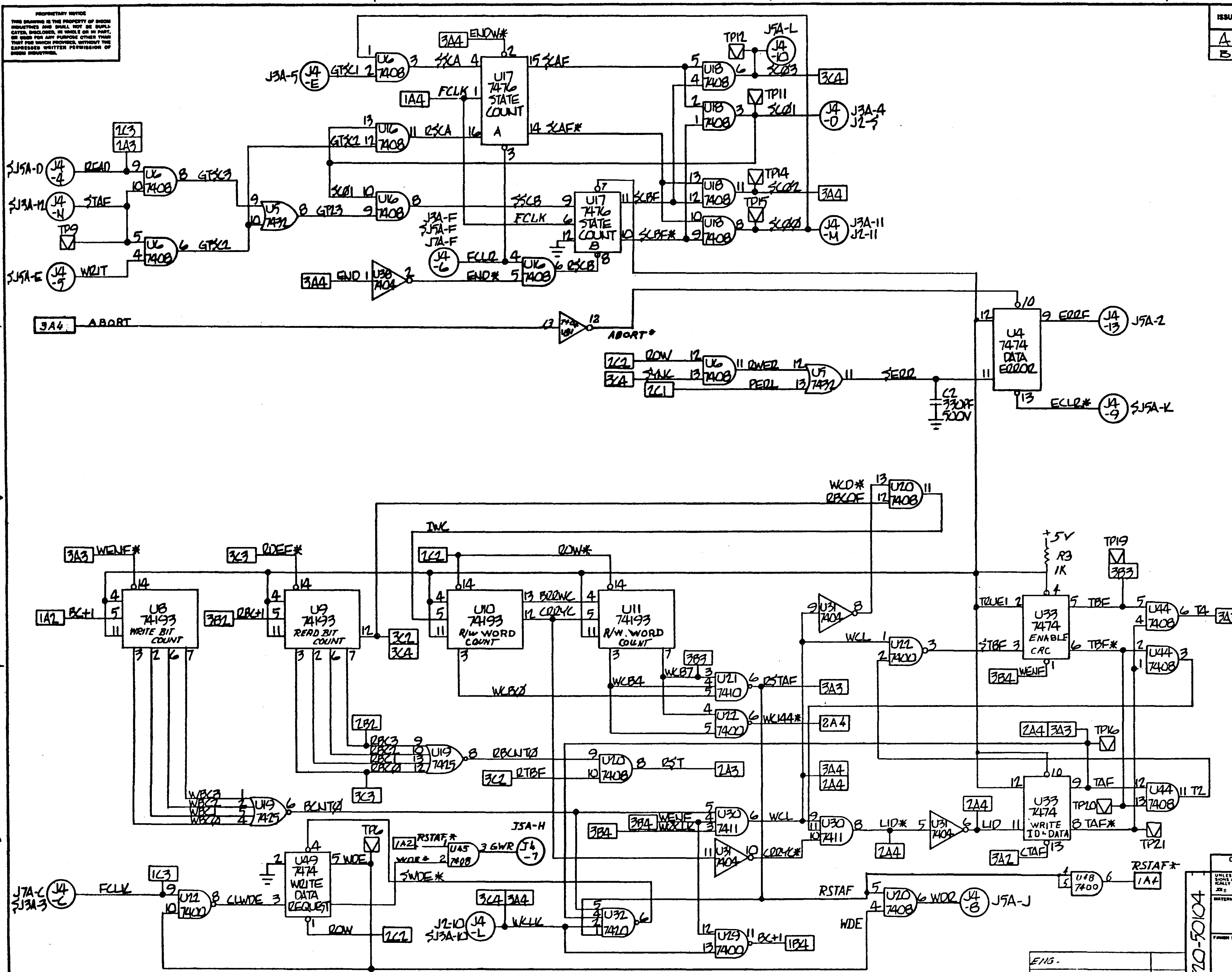
SCALE NONE | SHEET 5 OF 5

520-50103

ISSUE	DESCRIPTION	DRAFTING	DATE	DESIGN	DATE
A	RELEASE, ECN	C/E	8/28/74		
B	REVISED FOR MODELS 421A & 422				8-6/76



NOTES:

1. (XX-XX) INDICATES MOTHER BOARD CONNECTION.
2. TPX INDICATES TEST POINT.
3. [XXX] INDICATES OTHER LOCATION OF SIGNAL. EXAMPLE: [2A3] ZONE A3, SHEET 2
4. "SXX-XX INDICATES SIGNAL SOURCE.

MODEL 422
MODEL 421A
USED ON

520-50104

dicom INDUSTRIES INCORPORATED

LOGIC DIAGRAM
READ/WRITE LOGIC

D 520-50104-01 3

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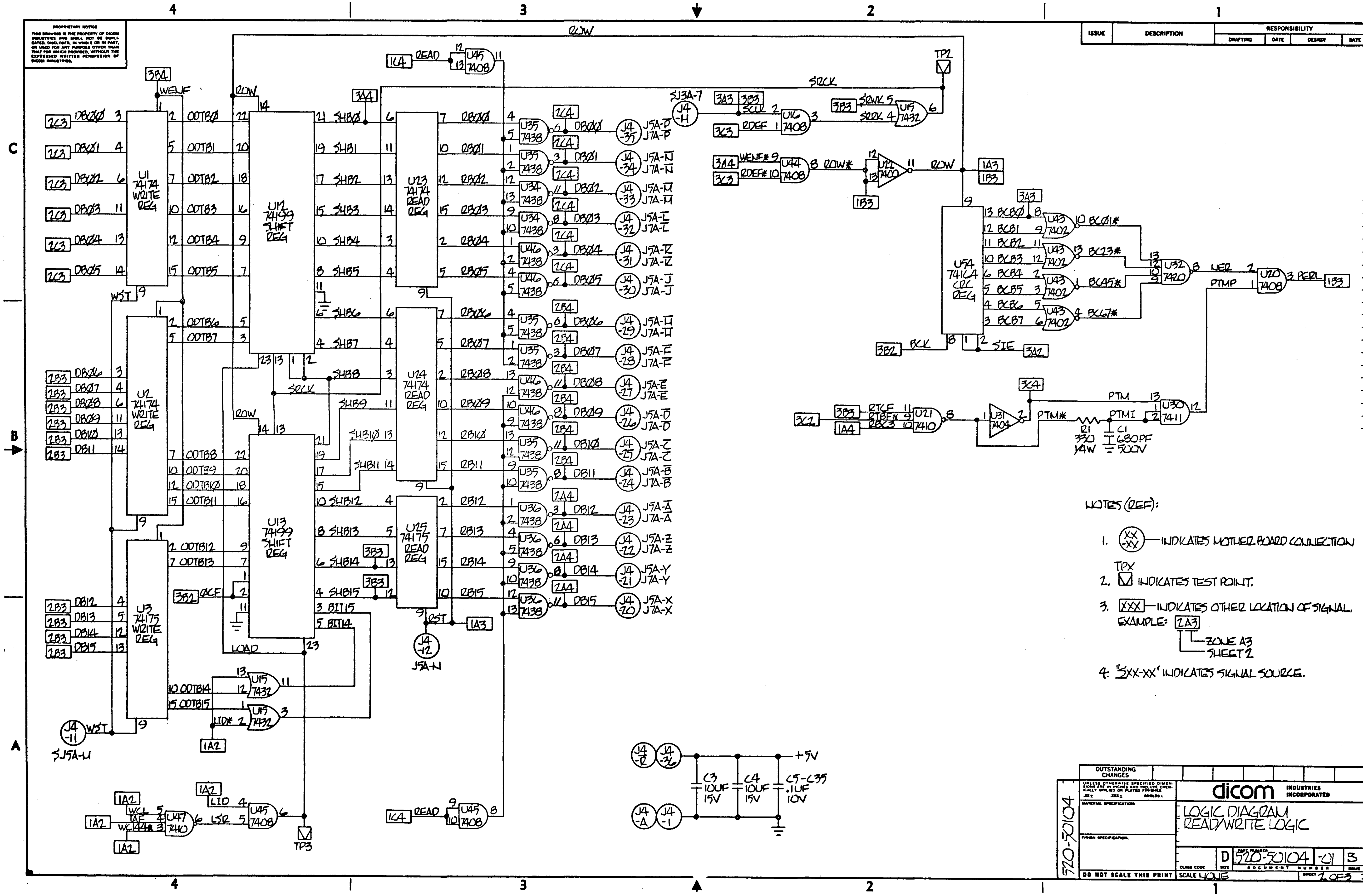
SCALE NONE SHEET 1 OF 3



PROPRIETARY NOTICE
ROW
SRCK
TP2
TP3
NOTES (REF):
1. (XX -XX) —INDICATES MOTHER BOARD CONNECTION
2. TPX INDICATES TEST POINT.
3. XXX —INDICATES OTHER LOCATION OF SIGNAL. EXAMPLE: 2A3 —ZONE A3 —SHEET 2
4. "SXX-XX" INDICATES SIGNAL SOURCE.
U1 74174 WRITE REG
U2 74174 WRITE REG
U3 74175 WRITE REG
U12 74199 SHIFT REG
U13 74199 SHIFT REG
U23 74174 READ REG
U24 74174 READ REG
U25 74175 READ REG
U54 74164 CRC REG
+5V
C3 10UF 15V
C4 10UF 15V
C5-C35 .1UF 10V
R1 330 1/4W
C1 680PF 500V
ISSUE
DESCRIPTION
RESPONSIBILITY
DRAFTING
DATE
DESIGN
DATE
OUTSTANDING CHANGES
dicom INDUSTRIES INCORPORATED
LOGIC DIAGRAM
READ/WRITE LOGIC
D
520-50104 -01
B
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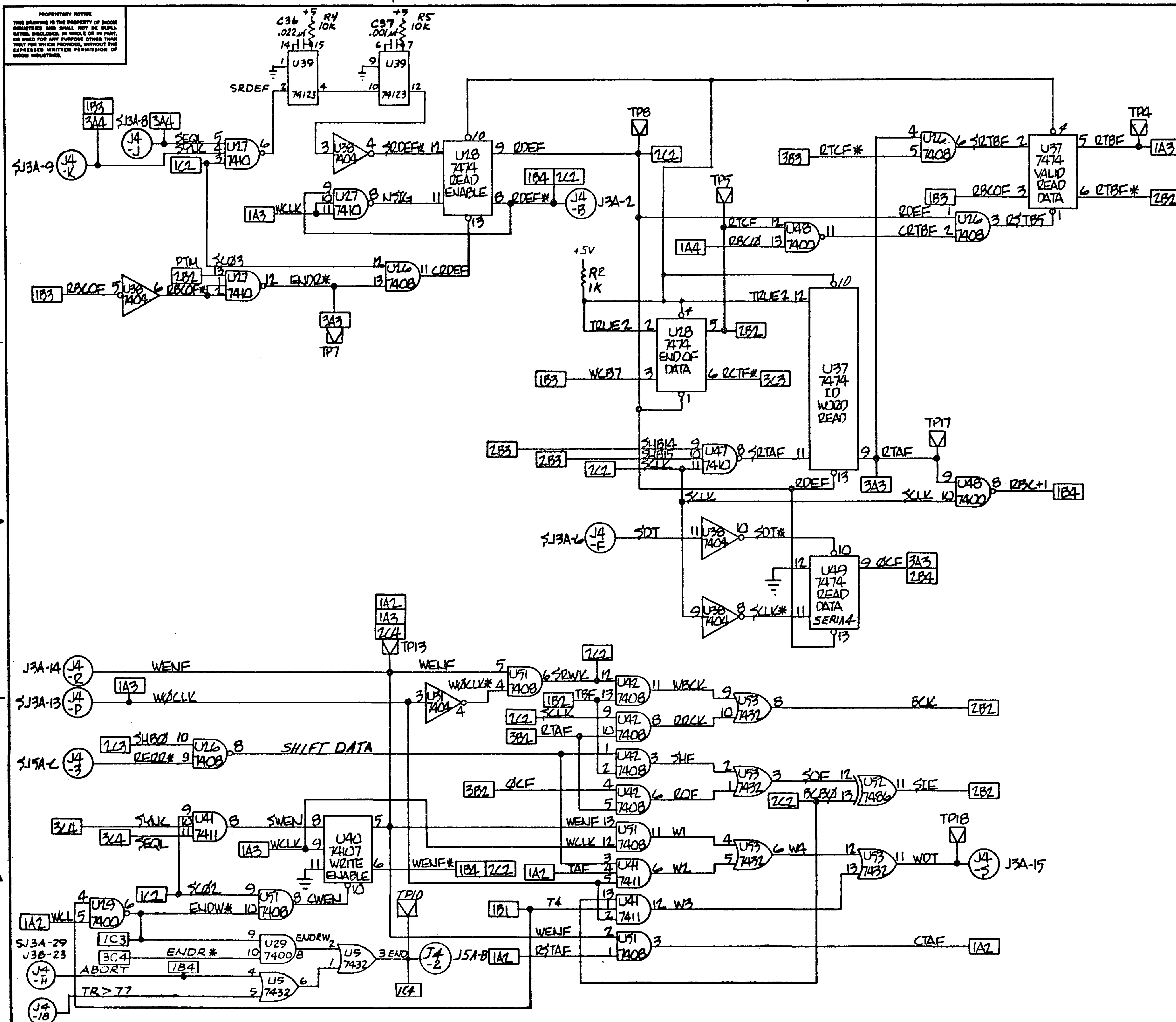
SCALE NONE
1 OF 3
520-50104



NOTES (REF):

1. (XX -XX) — INDICATES MOTHER BOARD CONNECTION.
2. TPX INDICATES TEST POINT.
3. [XXX] — INDICATES OTHER LOCATION OF SIGNAL.
   EXAMPLE= [2A3] — ZONE A3, SHEET 2
4. $XX-XX INDICATES SIGNAL SOURCE.

ISSUE	DESCRIPTION	RESPONSIBILITY: DRAFTING	DATE	DESIGN	DATE

OUTSTANDING CHANGES

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MATERIAL SPECIFICATION:

FINISH SPECIFICATION:

dicom INDUSTRIES INCORPORATED

LOGIC DIAGRAM READ/WRITE LOGIC

CLASS CODE | SIZE D | DOCUMENT NUMBER 520-50104-01 | ISSUE 3

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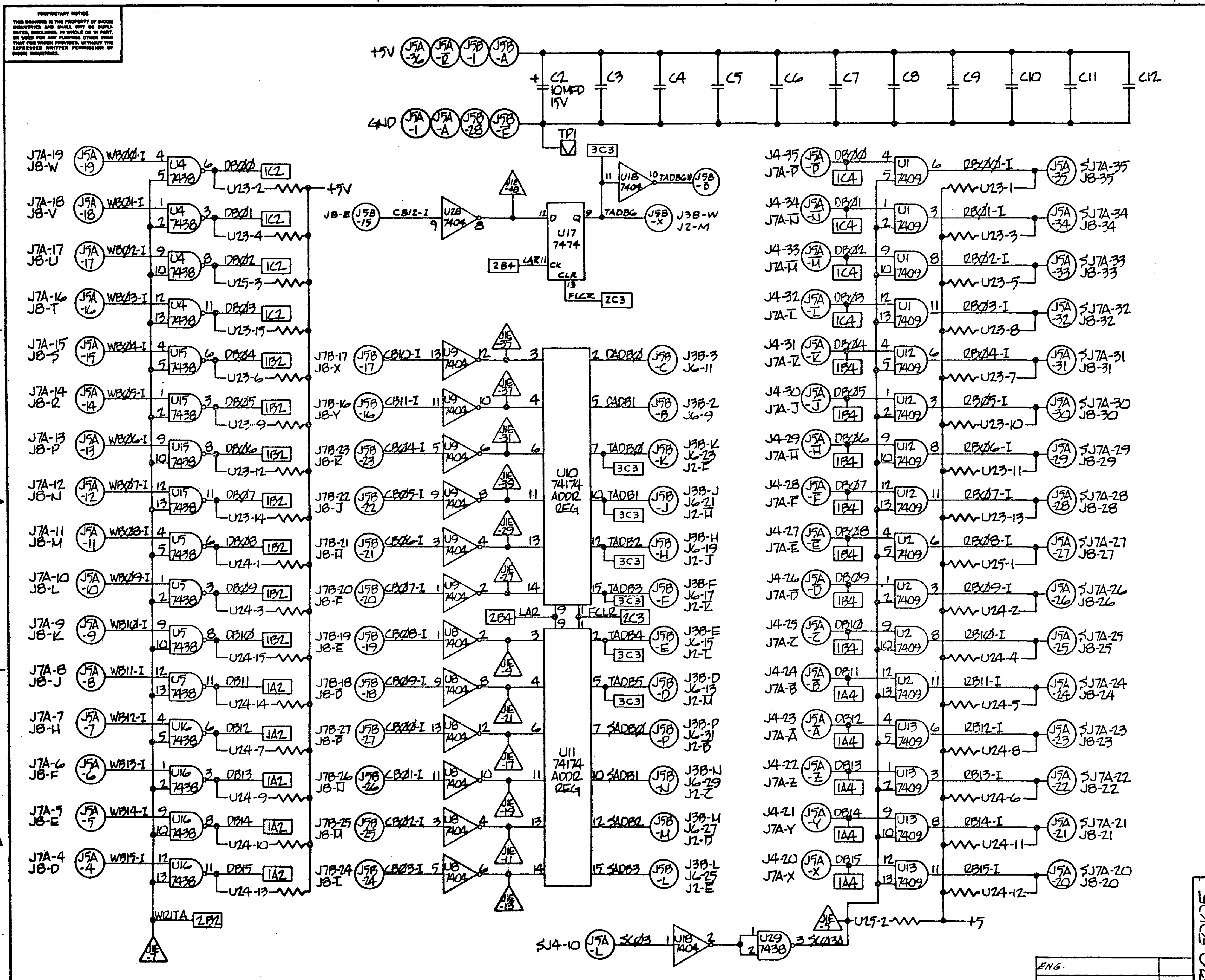
520-50104

ISSUE	DESCRIPTION	DRAFTING	DATE	DESIGN	DATE
A	RELEASE, ECN#	C/E	8-18-74		
B	REVISED FOR MODELS 421 A & 422				8-6/76



NOTES:

1. (XX -XX) — INDICATES MOTHER BOARD CONNECTION.
2. TPX ☒ INDICATES TEST POINT.
3. —UXX-XX-/\/\/\— INDICATES 680 OHM RESISTOR IN 16-PIN DIP.
4. [XXX] — INDICATES OTHER LOCATION OF SIGNAL. EXAMPLE: [2A3] — ZONE A3, SHEET 2
5. (triangle) INDICATES CABLE CONNECTION ON THIS PCB.
6. "$XX-XX" INDICATES SIGNAL SOURCE.
7. UNLESS OTHERWISE SPECIFIED, ALL CAPACITORS ARE .1 MFD., /OV.

MODEL	422
MODEL	421A
USED ON	

dicom INDUSTRIES INCORPORATED

LOGIC DIAGRAM, COMPUTER I/O,

D 520-50105 -01 B

ENG.
PROD.

DO NOT SCALE THIS PRINT — SCALE NONE — SHEET 1 OF 3

520-50105

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE

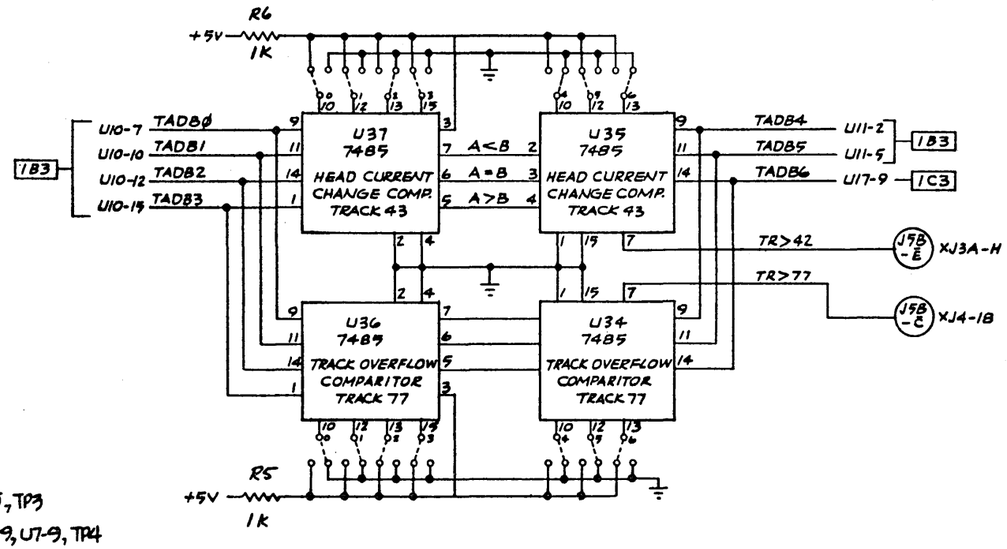
NOTES (REF):

1. (XX-XX) — INDICATES MOTHER BOARD CONNECTION.
2. TPX — INDICATES TEST POINT.
3. —UXX-XX— INDICATES 680 OHM RESISTOR IN 16-PIN DIP.
4. XXX — INDICATES OTHER LOCATION OF SIGNAL. EXAMPLE: 2A3 — ZONE A3, SHEET 2
5. INDICATES CABLE CONNECTION ON THIS PCB.
6. "SXX-XX" INDICATES SIGNAL SOURCE.

OUTSTANDING CHANGES	dicom INDUSTRIES INCORPORATED
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUSIVE ONLY APPLIED ON PLATED FINISHES.	LOGIC DIAGRAM COMPUTER I/O
MATERIAL SPECIFICATION	SIZE D — PART NUMBER 510-50105-01 — ISSUE B
FINISH SPECIFICATION	CLASS CODE — DWG NO. — DOCUMENT NUMBER — SHEET 2 OF 3
DO NOT SCALE THIS PRINT	SCALE NONE

510-50105

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE



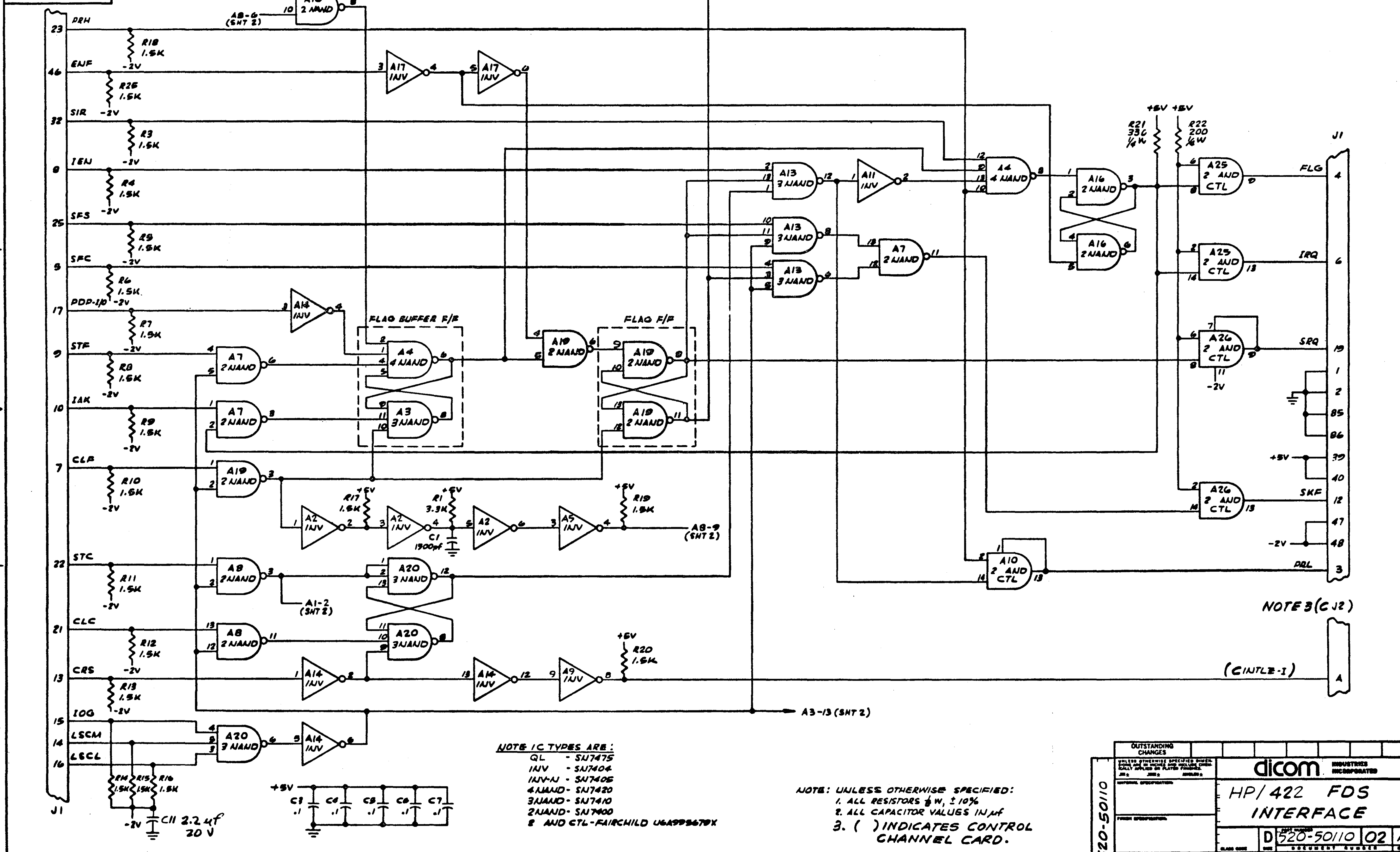
JIE

	2 1	U3-3, U17-5, TP3
	4 3	U3-13, U6-9, U7-9, TP4
	6 5	U1-2,-5,-10 ϕ-13, U2-2,-5,-10 ϕ-13, U12-2,-5,-10 ϕ-13, U13-2,-5,-10 ϕ-13, U25-2, U29-3
	8 7	U4-2,-5,-10 ϕ-13, U5-2,-5,-10 ϕ-13, U15-2,-5,-10 ϕ-13, U16-2,-5,-10 ϕ-13, U25-10, U29-8
	10 9	U8-2, U11-3
	12 11	U8-4, U11-13
	14 13	U8-6, U11-14
	16 15	U30-9, J5A-D
	18 17	U8-12, U11-6
	20 19	U8-10, U11-11
	22 21	U8-8, U11-4
	24 23	U20-9, U21-6, U31-5 ϕ-10
	26 25	U20-11, U21-4, U31-4 ϕ-12
	28 27	U9-2, U10-14
	30 29	U9-4, U10-13
	32 31	U9-6, U10-6
	34 33	U3-11, U19-2 ϕ-6, U29-13, U32-13, J5B-T
	36 35	U9-12, U10-3
	38 37	U9-10, U10-4
	40 39	U9-8, U10-11
	42 41	J5B-15
	44 43	U20-12, U32-2, U33-13
	46 45	U3-9, U21-2, J5B-9
U28-8	48 47	U21-12, U32-9
U9-5, TP2, J5A-2	50 49	U21-10, U32-10 ϕ-12, U33-12

OUTSTANDING CHANGES											
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES. .XX ± .XXX ± ANGLES ±	dicom INDUSTRIES INCORPORATED										
MATERIAL SPECIFICATION	LOGIC DIAGRAM, COMPUTER I/O,										
FINISH SPECIFICATION											
DO NOT SCALE THIS PRINT	CLASS CODE	DATE	D	520-50105 DOCUMENT NUMBER	-21	3 ISSUE
	SCALE NONE					SHEET 3 OF 3

520-50105

ISSUE	DESCRIPTION	DRAFTING	DATE	DESIGN	DATE
A	RE-RELEASE FROM 520-50052D	T.C./P.M.	9-76		



NOTE IC TYPES ARE:
- QL - SN7475
- INV - SN7404
- INV-N - SN7406
- 4NAND - SN7420
- 3NAND - SN7410
- 2NAND - SN7400
- 2 AND CTL - FAIRCHILD U6A9956X

NOTE: UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS ¼W, ± 10%
2. ALL CAPACITOR VALUES IN µf
3. ( ) INDICATES CONTROL CHANNEL CARD.

dicom INDUSTRIES INCORPORATED

HP/422 FDS INTERFACE

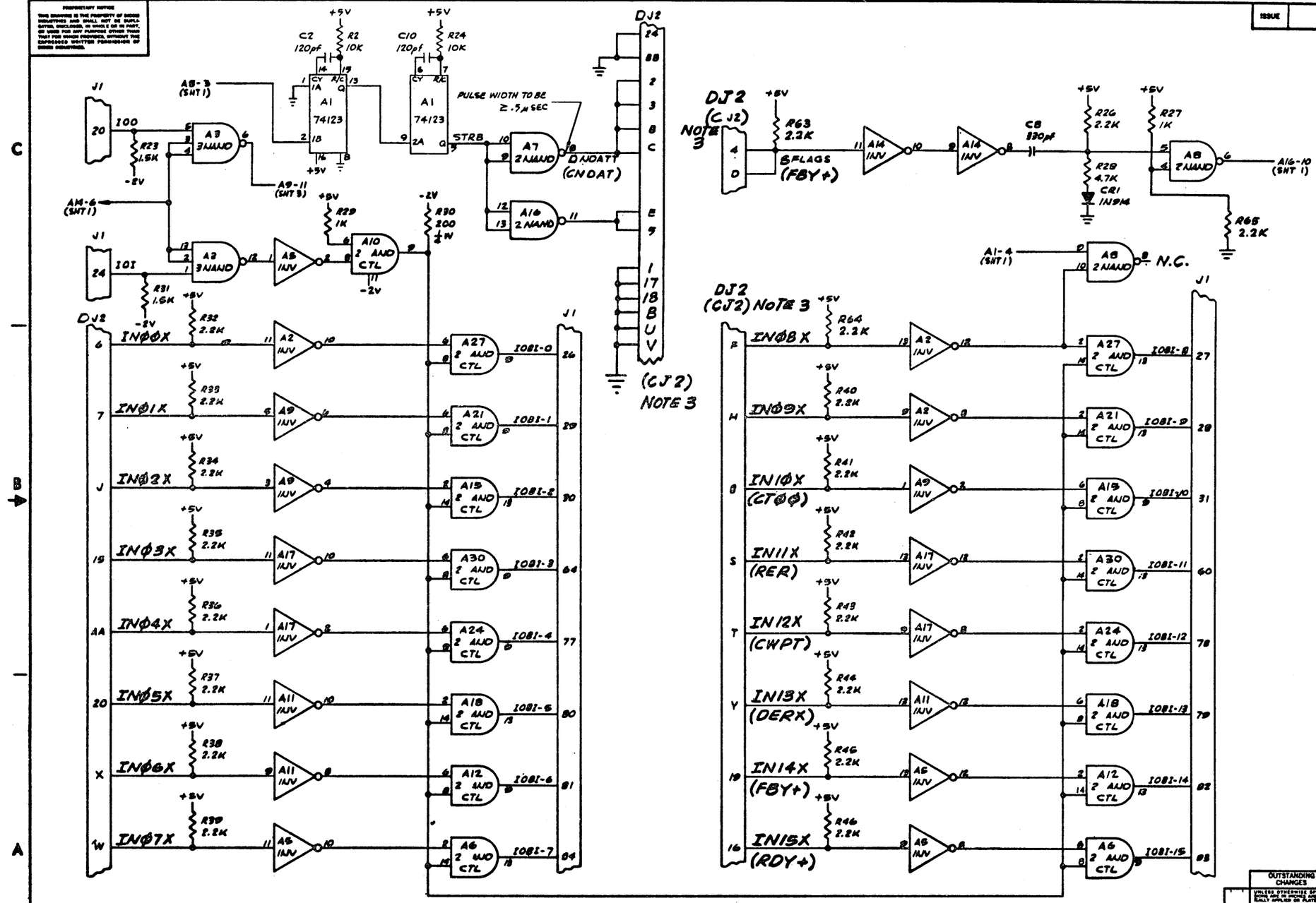
D 520-50110 02 A

520-50110

DO NOT SCALE THIS PRINT

SHEET 1 OF 2

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE



OUTSTANDING CHANGES

dicom INDUSTRIES INCORPORATED

520-50110

HP/422 FDS INTERFACE

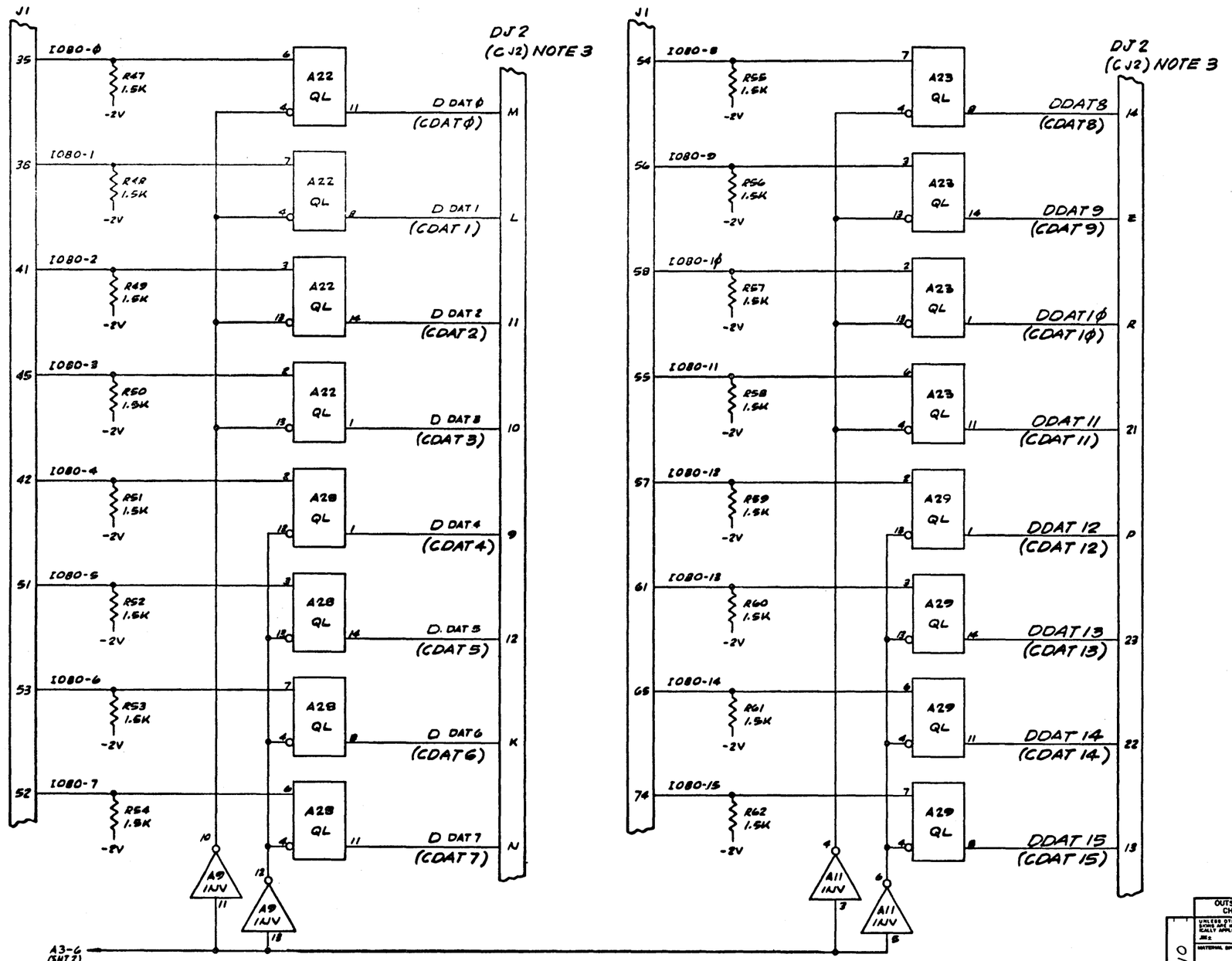
D 520-50110 02 A

DO NOT SCALE THIS PRINT

SCALE

SHEET 2 OF 3

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE



OUTSTANDING CHANGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE: .XX ± .Ø1, .XXX ± .ØØ5, ANGULAR ± 1°. MATERIAL SPECIFICATION. FINISH SPECIFICATION. DO NOT SCALE THIS PRINT

dicom INDUSTRIES INCORPORATED

H-P/422 FDS INTERFACE

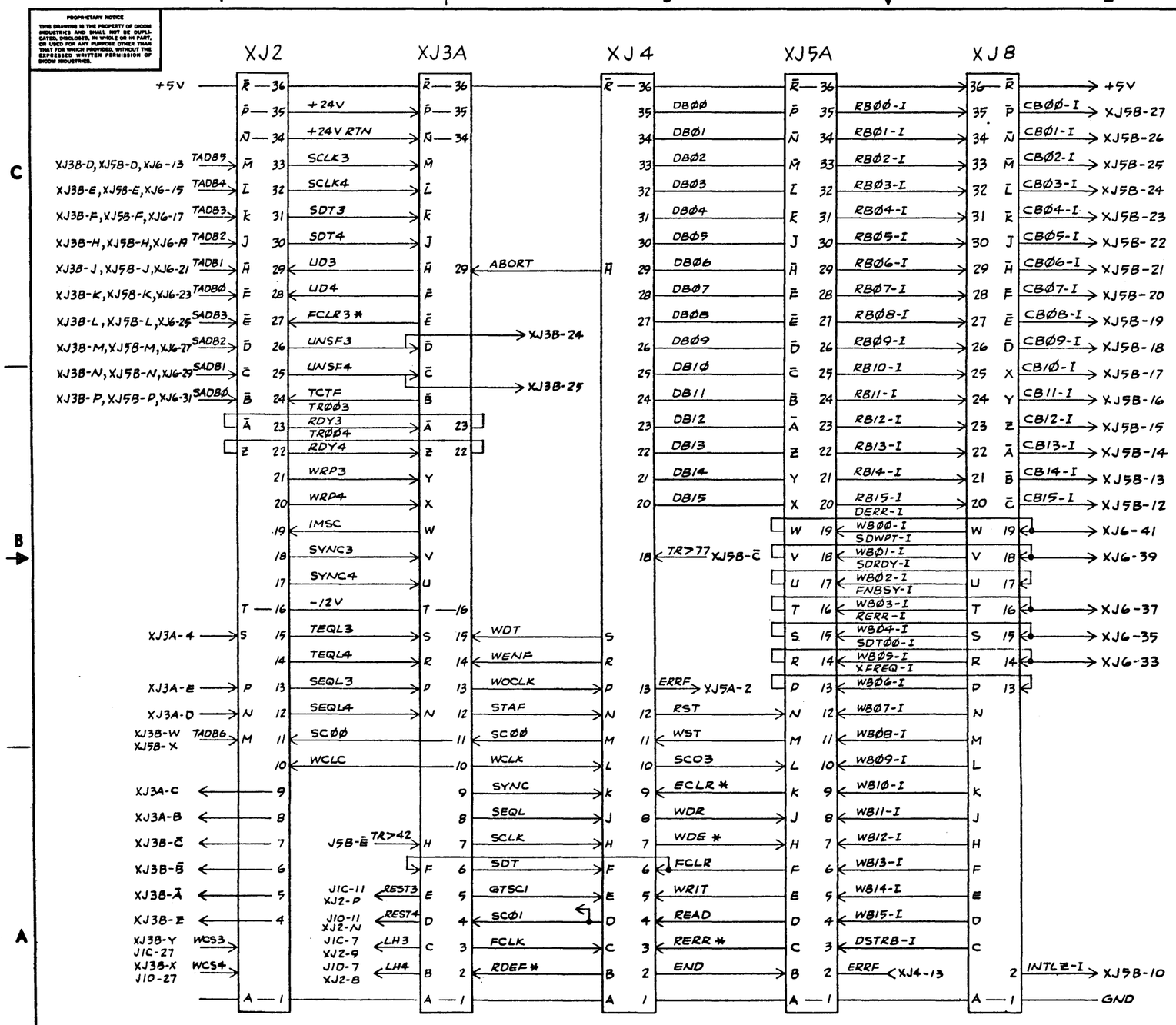
520-50110

CLASS CODE D | PART NUMBER 520-50110 | 02 | A

DATE | DOCUMENT NUMBER | ISSUE

SCALE | SHEET 3 OF 3

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE
A	PRODUCTION REL.			tms	5/6-76



MODEL 4:2
MODEL 4:1A
USED ON

OUTSTANDING CHANGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
.XX ± .XXX ± ANGLES ±

MATERIAL SPECIFICATION

FINISH SPECIFICATION

DO NOT SCALE THIS PRINT

dicom INDUSTRIES INCORPORATED

SCHEMATIC DIAGRAM, MOTHER BOARD

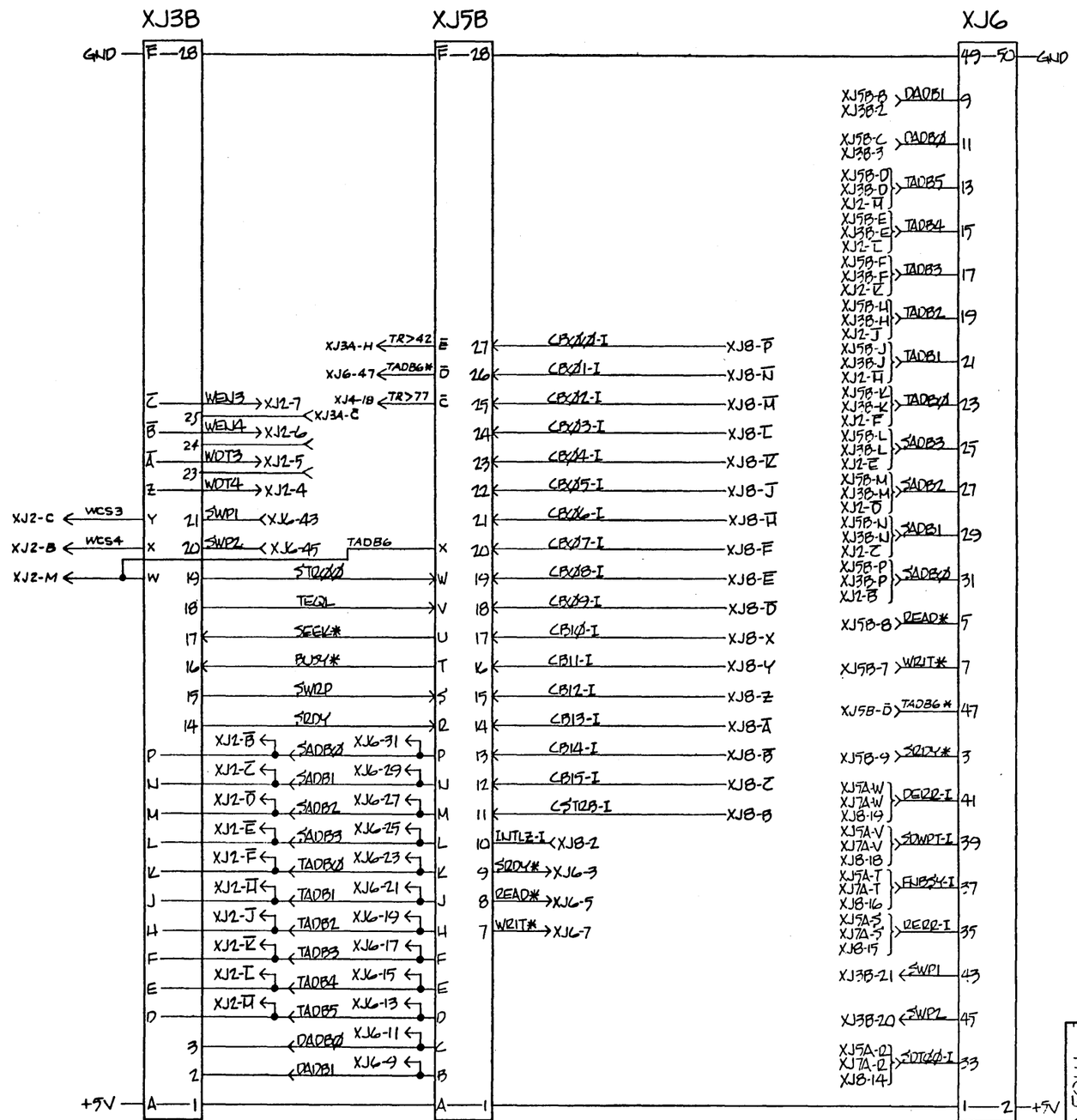
CLASS CODE D | SIZE | PART NUMBER 520-50111 | DOCUMENT NUMBER -01 | ISSUE A

SCALE | SHEET 1 OF 2

ENG
PROD

111505-025

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE



OUTSTANDING CHANGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
XX ± .01 XXX ± .005 ANGLES ±

MATERIAL SPECIFICATION:

FINISH SPECIFICATION:

DO NOT SCALE THIS PRINT

dicom INDUSTRIES INCORPORATED

SCHEMATIC DIAGRAM MOTHER BOARD

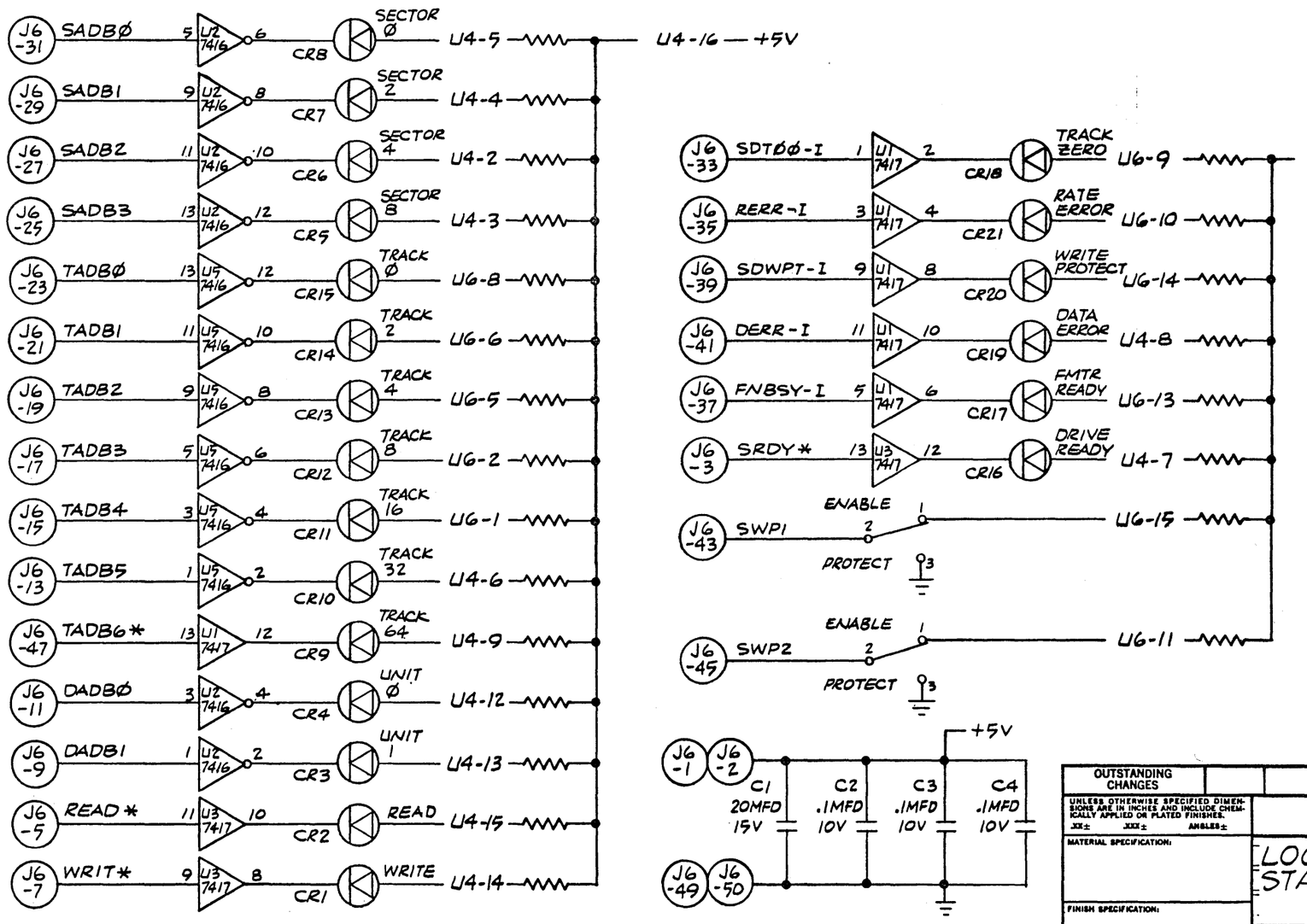
520-50111

CLASS CODE: D | SIZE | PART NUMBER / DOCUMENT NUMBER: 520-50111-01 | ISSUE: A

SCALE: NONE | SHEET 1 OF 2

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE
A	PRODUCTION REL			[illegible]	8-4/76

NOTES:
1. (XX / -XX) — INDICATES MOTHERBOARD CONNECTION
2. ALL RESISTORS ARE 100 Ω, 1/4 WATT
3. CR1 - CR15 & CR19 ARE RED LED'S
4. CR16 & CR17 ARE GREEN LED'S
5. CR18, CR20 & CR21 ARE AMBER LED'S
6. S1 & S2 ARE SPST
7. LED'S ——— FRONT OF BOARD
   ALL OTHER COMPONENTS BACK OF BOARD



520-50112

MODEL 422
MODEL 421A
USED ON

OUTSTANDING CHANGES									

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
XX± XXX± ANGLES±

MATERIAL SPECIFICATION:

FINISH SPECIFICATION:

dicom INDUSTRIES INCORPORATED

LOGIC DIAGRAM, STATUS PANEL

ENG		
PROD		

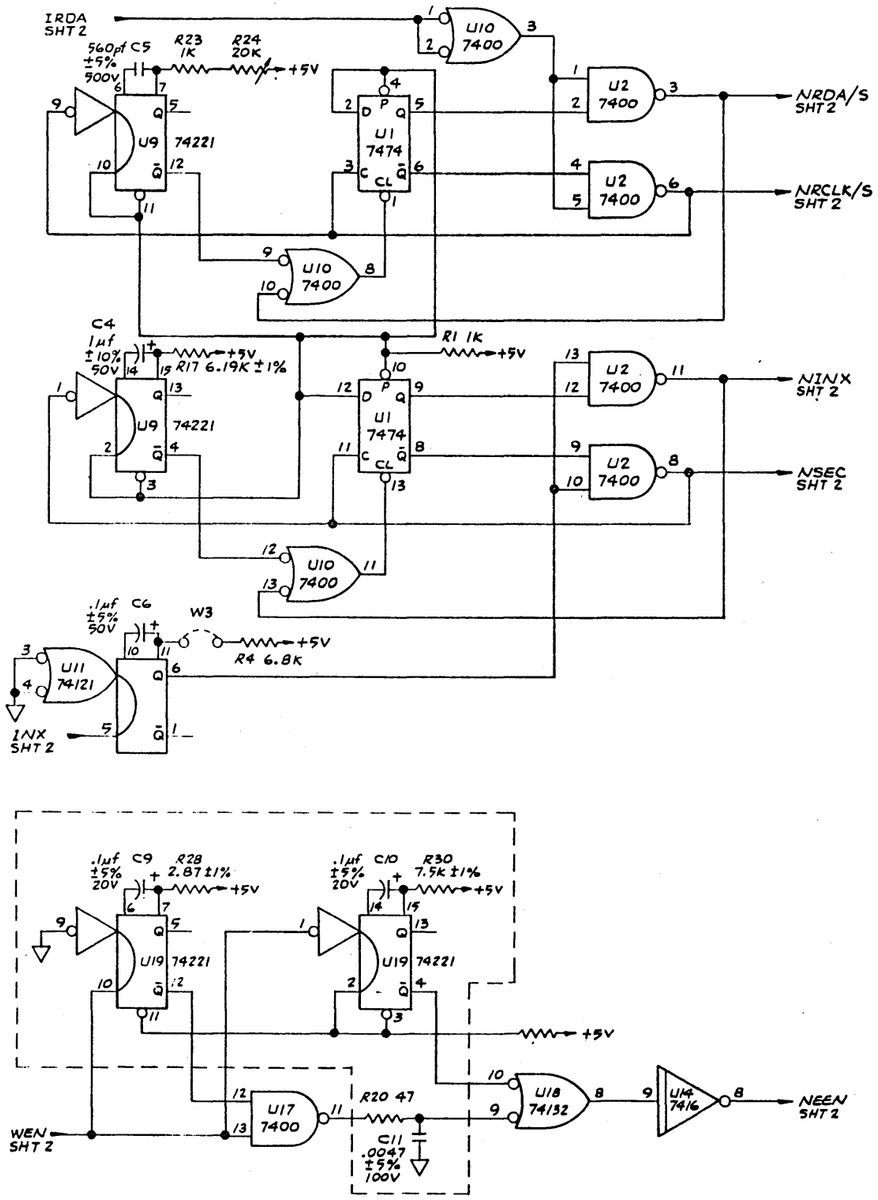
DO NOT SCALE THIS PRINT

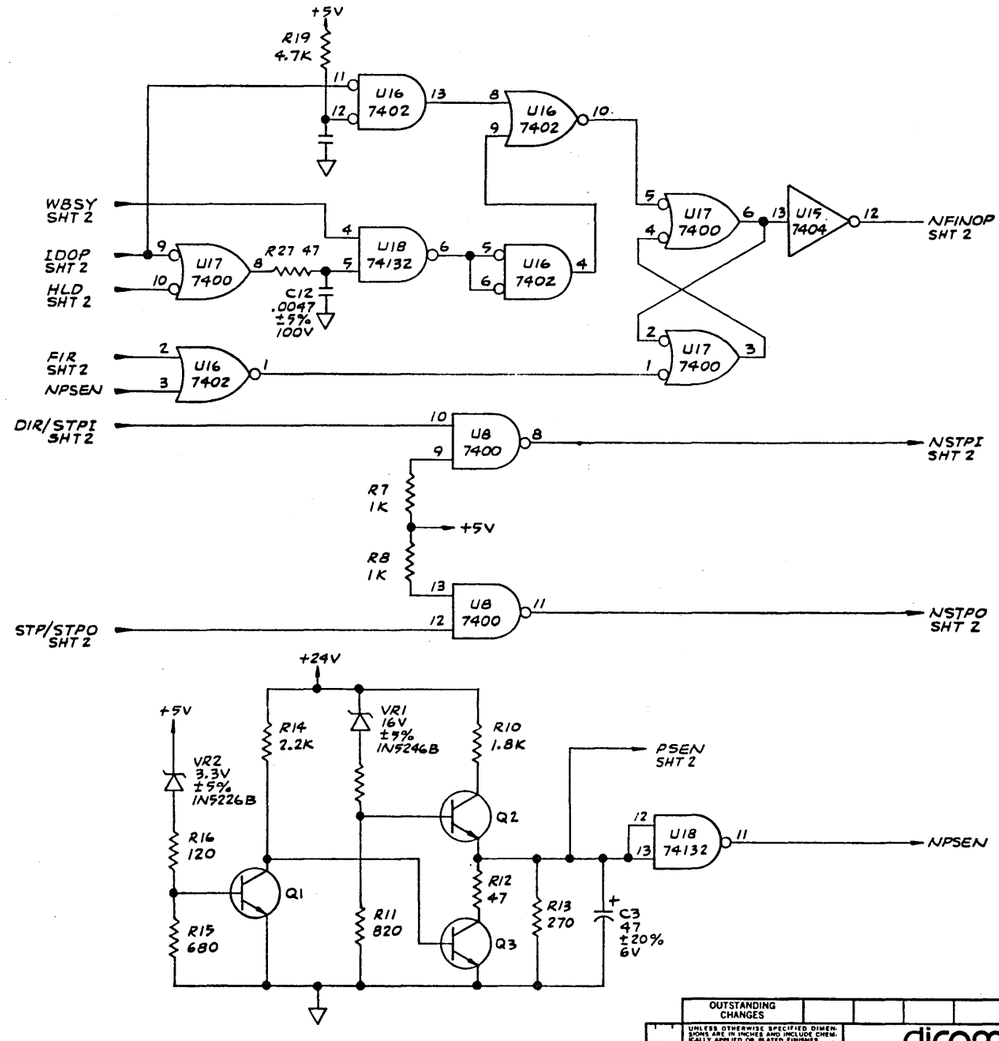
CLASS CODE	SIZE	PART NUMBER / DOCUMENT NUMBER		ISSUE
	C	520-50112	-01	A

SCALE — SHEET 1 OF 1

PRINTED ON DIEPO NO. 10000H-8 CLEARPRINT FADE-OUT 1-76

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE
B	REDRAWN	T.C./P.M.	9/76		





OUTSTANDING CHANGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE BEFORE PLATING AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES. .XX ± .XXX ± ANGLES ±

MATERIAL SPECIFICATION:

FINISH SPECIFICATION:

DO NOT SCALE THIS PRINT

dicom INDUSTRIES INCORPORATED

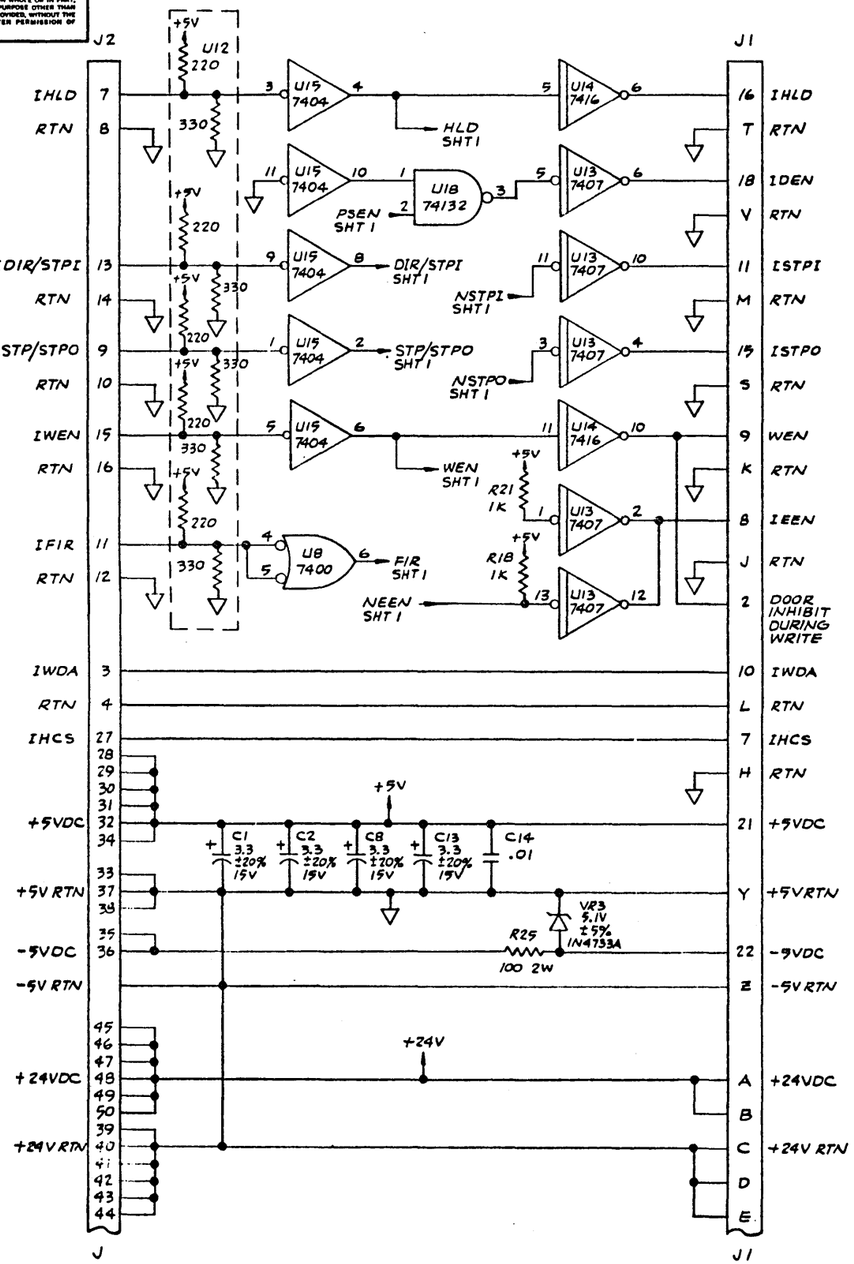
422 "P" ADAPTER

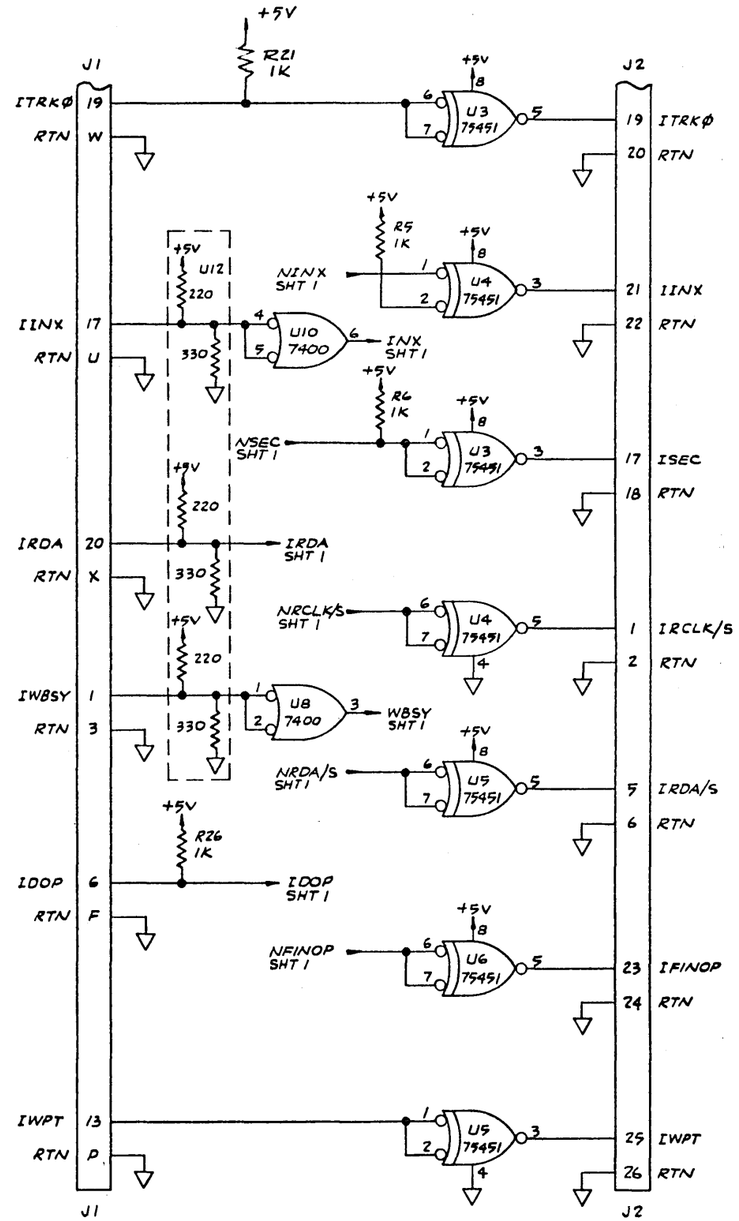
520-50113-01

CLASS CODE D SIZE | PART NUMBER / DOCUMENT NUMBER 520-50113 01 | ISSUE B

SCALE | SHEET 1 OF 2

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE





OUTSTANDING CHANGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES. XX ± XXX ± ANGLES ±

MATERIAL SPECIFICATION

FINISH SPECIFICATION

DO NOT SCALE THIS PRINT

dicom INDUSTRIES INCORPORATED

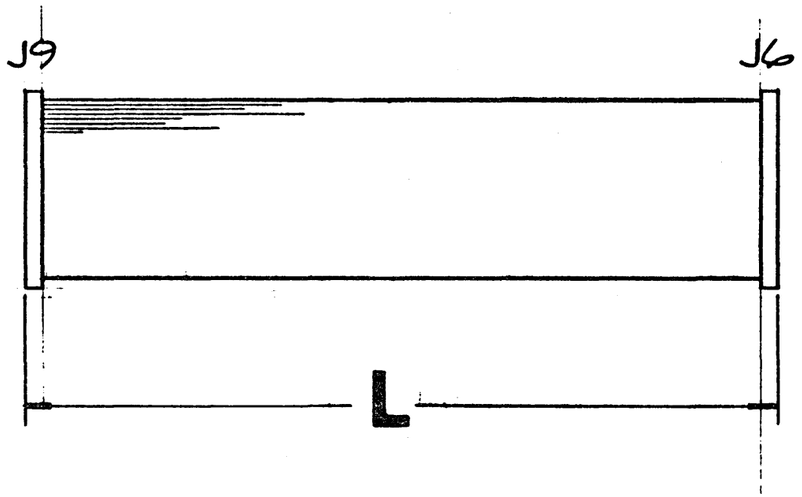
422 "P" ADAPTER

520-50113-01

CLASS CODE D SIZE PART NUMBER 520-50113 DOCUMENT NUMBER 01 ISSUE B

SCALE SHEET 2 OF 2

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE
A	RELEASE, ECN#	J. TINKEN	10-8-74	CE	10-8-74
B	ADDED -02 & -03			tcm	8-6/76



DASH NO	DIM L ± 1"	USED ON
-01	8 INCH	421A/422
-02	24 INCH	422
-03	8 FEET	421A/422

NOTES:

1. INSTALL CONNECTORS:

PIN 1 TO PIN 1
PIN 2 TO PIN 2
PIN 50 TO PIN 50

ENG.		11-21-74
PROD		

036-70104

OUTSTANDING CHANGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
.XX± .XXX± ANGLES±

MATERIAL SPECIFICATION:
REF
IMPL 036-70104

FINISH SPECIFICATION:

DO NOT SCALE THIS PRINT

dicom INDUSTRIES INCORPORATED

CABLE ASSY, STATUS PANEL, MODEL 421

CLASS CODE	SIZE	PART NUMBER / DOCUMENT NUMBER	ISSUE
	B	036-70104	B

SCALE 1/2

SHEET 1 OF 2

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE

P2 3M			P1 3M
1	SPCLK(n)	-SEP CLOCK	1
2		RETURN	2
3	WDT(n)	-WRITE DATA	3
4		RETURN	4
5	SPDT(n)	-SEP DATA	5
6		RETURN	6
7	LH(n)	-LOAD HEAD	7
8		RETURN	8
9	STO(n)	-STEP OUT	9
10		RETURN	10
11	REST(n)	-FILE UNSAFE RESET	11
12		RETURN	12
13	STPI(n)	-STEP IN	13
14		RETURN	14
15	WEN(n)	-WRITE ENABLE	15
16		RETURN	16
17	SCT(n)	-SECTOR	17
18		RETURN	18
19	TØØ(n)	-TRACK ØØ	19
20		RETURN	20
21	IND(n)	-INDEX	21
22		RETURN	22
23	USF(n)	-FILE UNSAFE	23
24		RETURN	24
25	WP(n)	-WRITE PROTECT	25
26		RETURN	26
27	WCS(n)	WRITE CURRENT SWITCH	27
28		+5V	28
29		+5V	29
30		+5V	30
31		+5V	31
32		+5V	32
33		RETURN	33
34		+5V	34
35		-12V	35
36		-12V	36
37		RETURN	37
38		RETURN	38
39		+24V RETURN	39
40		+24V RETURN	40
41		+24V RETURN	41
42		+24V RETURN	42
43		+24V RETURN	43
44		+24V RETURN	44
45		+24V	45
46		+24V	46
47		+24V	47
48		+24V	48
49		+24V	49
50		+24V	50

XJ1A — — — — — — DRIVE 1 — — — — — — — XJ1Ø
XJ1B — — — — — — DRIVE 2 — — — — — — — XJ11
XJ1C — — — — — — DRIVE 3 — — — — — — — XJ12
XJ1D — — — — — — DRIVE 4 — — — — — — — XJ13

036-70104

OUTSTANDING CHANGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
.XX ± .XXX ± ANGLES ±

MATERIAL SPECIFICATION:

FINISH SPECIFICATION:

DO NOT SCALE THIS PRINT

dicom INDUSTRIES INCORPORATED

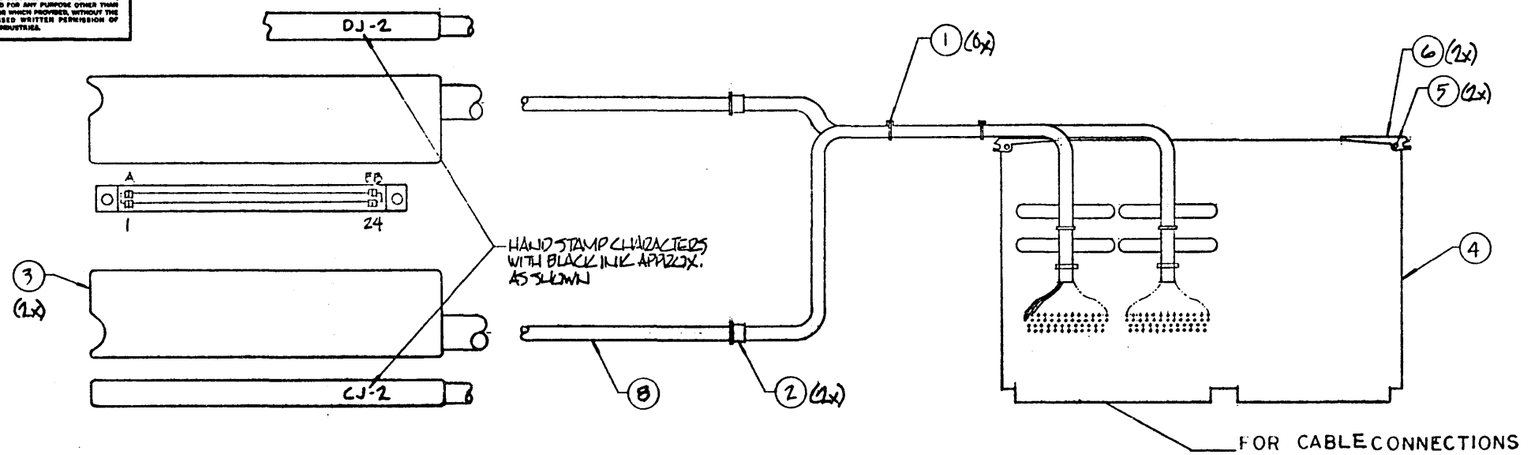
CABLE ASSY, PERTEC "P" DISK INTERFACE

CLASS CODE	SIZE	PART NUMBER / DOCUMENT NUMBER		ISSUE
	C	036-70104	02 03	A

SCALE NONE

SHEET 2 OF 2

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE
D	REVISED FOR MODELS 421A & 422			8-6/70 tmr	



DJ2

PADDLEBOARD

C	WHT/RED/GRN	DISTRB-I	C
4	WHT/GRY/BRN	VEREQ-I	13
6	WHT/BRN/VIO	RB00-I	35
7	WHT/RED/BRN	RB01-I	34
J	WHT/BLK/GRY	RB02-I	33
15	WHT/BLK/VIO	RB03-I	32
AA	WHT/RED/YEL	RB04-I	31
20	WHT/RED/GRN	RB05-I	30
X	WHT/BLU/BRN	RB06-I	29
W	WHT/GRN/BRN	RB07-I	28
F	WHT/BRN/YEL	RB08-I	27
H	WHT/BRN/ORN	RB09-I	26
8	WHT/BLU/BLK	RB10-I	25
S	WHT/GRN/YEL	RB11-I	24
T	WHT/ORN/VIO	RB12-I	23
Y	WHT/ORN/GRY	RB13-I	22
19	WHT/BLK/GRN	RB14-I	21
16	WHT/RED/BLU	RB15-I	20
N	WHT/BLU/ORN	WB01-I	W
L	WHT/VIO	WB01-I	V
11	WHT/BLK/YEL	WB02-I	U
10	WHT/BRN/BLK	WB03-I	T
9	WHT/BLK/RED	WB04-I	S
12	WHT/ORN/BLK	WB05-I	R
K	WHT/GRY	WB06-I	P
N	WHT/RED/GRY	WB07-I	N
14	WHT/BLU	WB08-I	M
Z	WHT/ORN/GRN	WB09-I	L
R	WHT/GRN/YEL	WB10-I	K
21	WHT/RED/VIO	WB11-I	J
P	WHT/BRN	WB12-I	H
23	WHT/ORN	WB13-I	F
22	WHT/YEL	WB14-I	E
13	WHT/GRN	WB15-I	D
24			3
18			THRU
17			12
1			

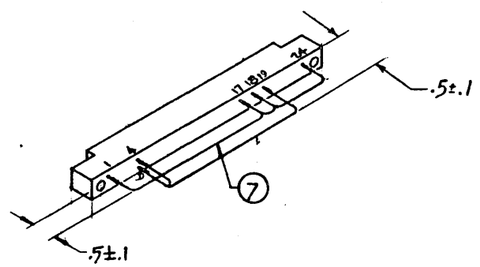
CJ2

PADDLEBOARD

M	WHT/BLK/RED	CB00-I	P
L	WHT/BRN/BLK	CB01-I	N
11	WHT/BRN/VIO	CB02-I	M
10	WHT/RED/ORN	CB03-I	L
9	WHT/ORN/VIO	CB04-I	K
12	WHT/BRN/GRN	CB05-I	J
K	WHT/ORN/YEL	CB06-I	H
N	WHT/RED/GRY	CB07-I	F
14	WHT/BLK/GRY	CB08-I	E
Z	WHT/BLU/RED	CB09-I	D
21	WHT/VIO	CB10-I	X
P	WHT/BLU/BLK	CB11-I	Y
R	WHT/BLU/YEL	CB12-I	Z
23	WHT/RED/BRN	CB13-I	A
22	WHT/BRN/GRY	CB14-I	B
13	WHT/RED/GRN	CB15-I	C
6	WHT/BLU/VIO	SDDRV-I	17
19	WHT/BLU/BRN	ENBSY-I	16
Y	WHT/RED/VIO	DEDD-I	19
8	WHT/ORN/BLK	SDTXD-I	14
T	WHT/BLU	SDWPT-I	18
S	WHT/GRY	DEDD-I	15
A	WHT/ORN/BLU	INTLZ-I	2
C	WHT/ORN/GRN	GSTDB-I	B
24			1
18			A
17			
1			
4			
D			

THESE CONNECTIONS FOR MODEL 421A ONLY

DASH NO.	ITEM LENGTH
-01	6'
-02	15'



MODEL 422
MODEL 421A
USED ON

OUTSTANDING CHANGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
XX ± .03 XXX ± .010 ANGLES ± 1°

MATERIAL SPECIFICATION: DEF MIL-C-00443

FINISH SPECIFICATION: /

DO NOT SCALE THIS PRINT

ENG. [illegible] PROD.

dicom INDUSTRIES INCORPORATED

CABLE ASSY, FLOPPY DISK INTERFACE

CLASS CODE D SIZE | PART NUMBER 036-00443 DOCUMENT NUMBER | ISSUE 3

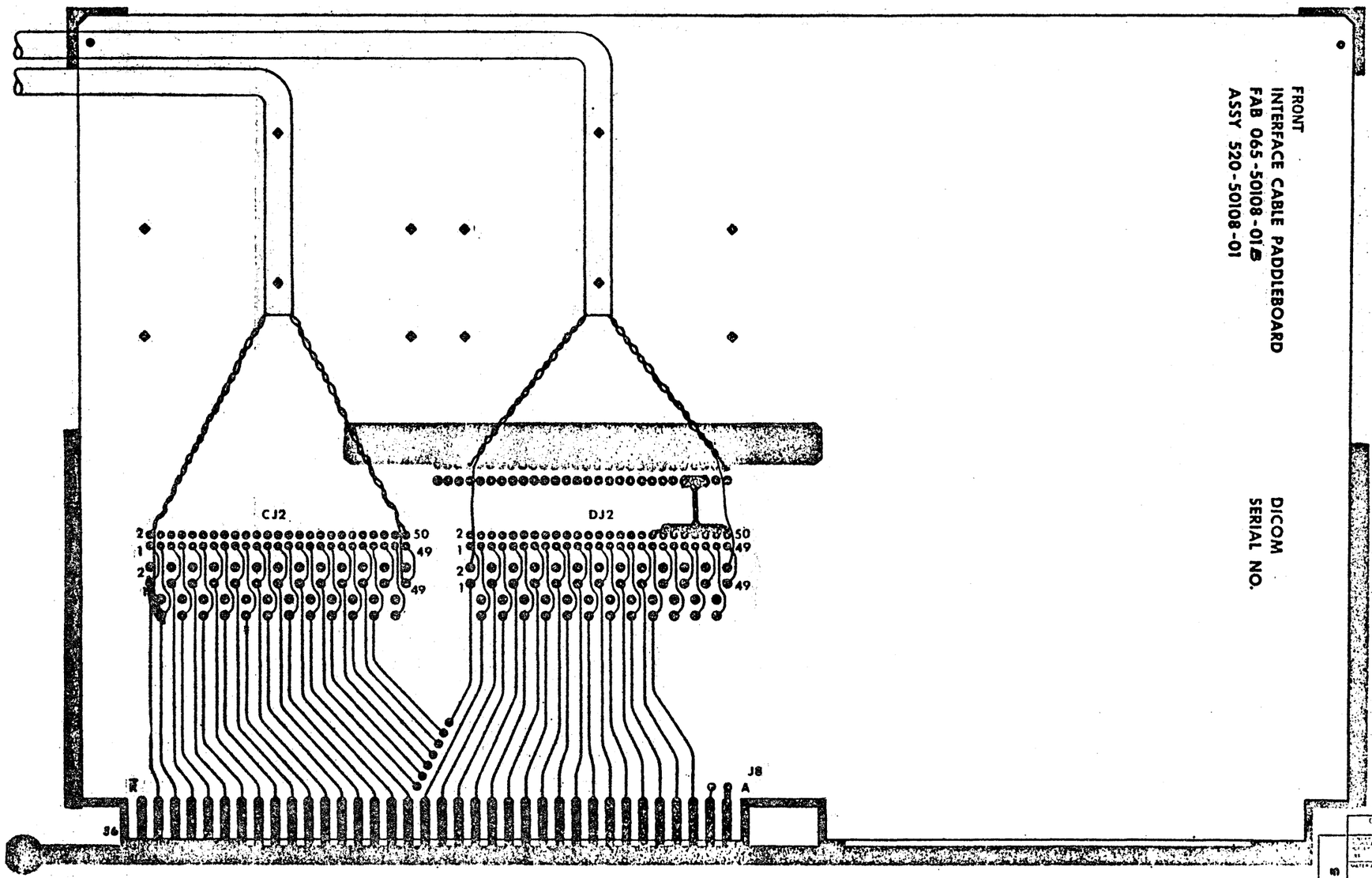
SCALE NONE | SHEET 1 OF 2

036-00443

ISSUE	DESCRIPTION	APPROVED	DATE	DRAWN	DATE
B					

REDUCE TO 14.000 ± .005

FRONT



FRONT
INTERFACE CABLE PADDLEBOARD
FAB 065-50108-01B
ASSY 520-50108-01

DICOM
SERIAL NO.

REDUCE TO 9.500 ± .005

B

A

DATE

ENG.

PROD.

036-00445

OUTSTANDING CHANGES

SEE SHT 1

dicom INTEGRATION INCORPORATED

CABLE ASSY. -
HP42IA, 422 FLOPPY DISK
INTERFACE

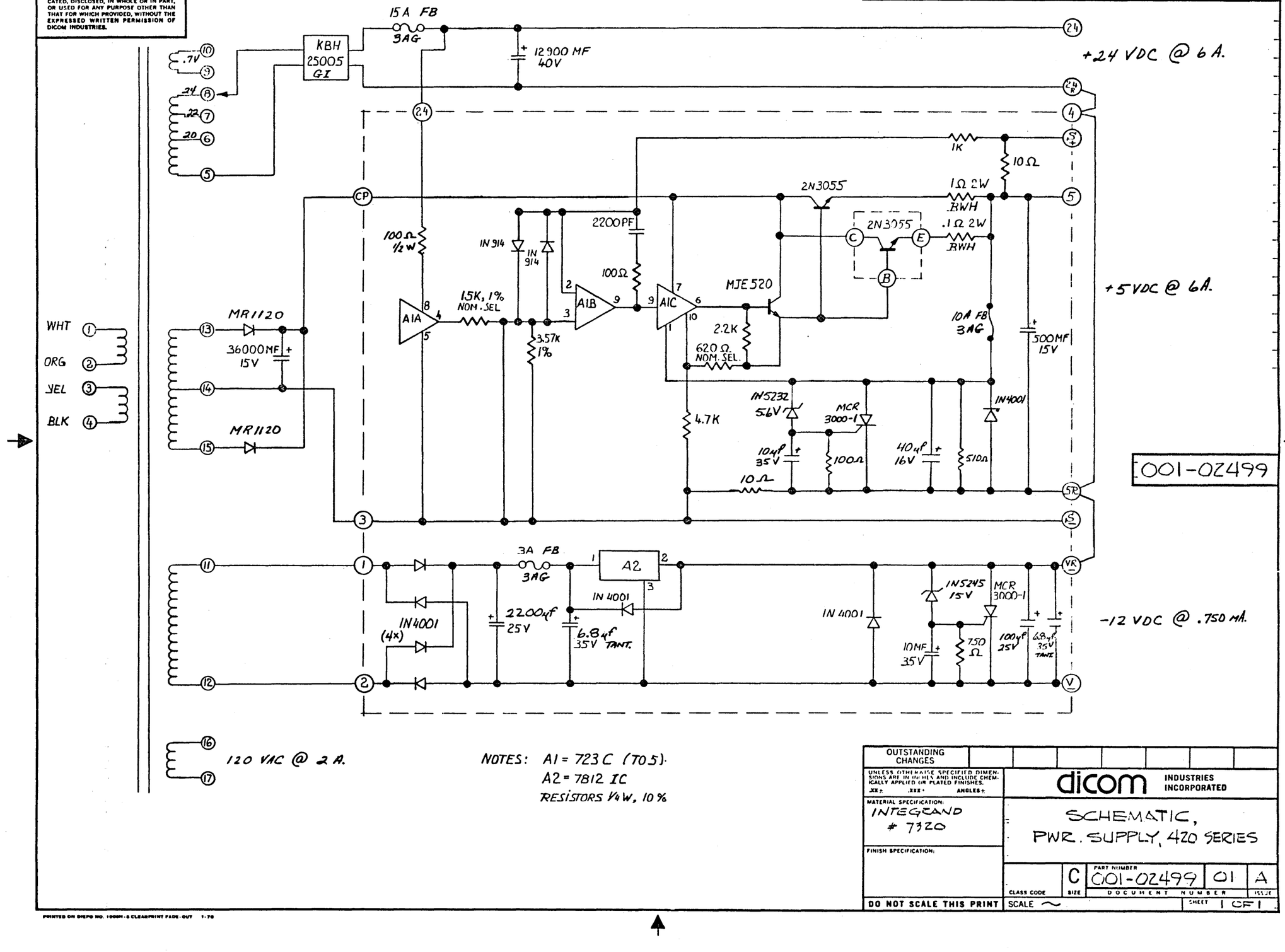
—

D | 036-00443 | B

DO NOT SCALE THIS PRINT

SHT 1 OF 2

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE



NOTES: A1 = 723C (TO5).
A2 = 7812 IC
RESISTORS 1/4W, 10%

OUTSTANDING CHANGES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
.XX ± .XXX ± ANGLES ±

MATERIAL SPECIFICATION: INTEGRAND # 7320

FINISH SPECIFICATION:

DO NOT SCALE THIS PRINT

dicom INDUSTRIES INCORPORATED

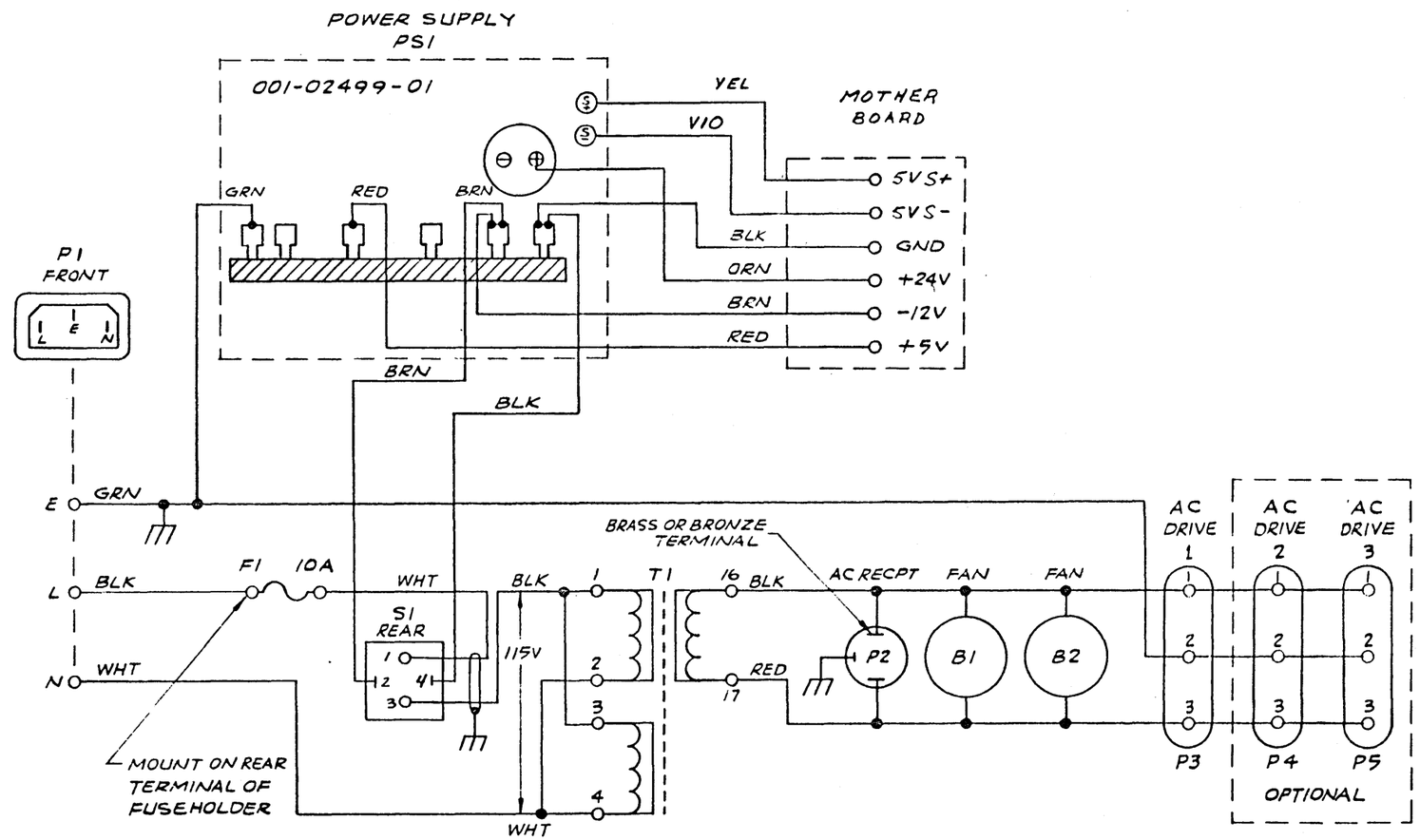
SCHEMATIC, PWR. SUPPLY, 420 SERIES

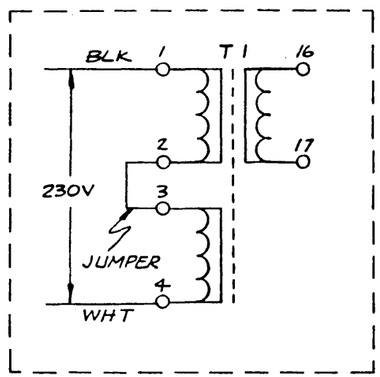
CLASS CODE	SIZE	PART NUMBER / DOCUMENT NUMBER		ISSUE
	C	001-02499	01	A

SCALE ~ SHEET 1 OF 1

PRINTED ON DIEPO NO. 1000H-5 CLEARPRINT FADE-OUT 1-76

ISSUE	DESCRIPTION	RESPONSIBILITY			
		DRAFTING	DATE	DESIGN	DATE
A				SILVIA	5/96





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