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DTC-1Ø-1 HOST ADAPTER* FOR THE IEEE 696.1 (S-1ØØ) BUS

PRELIMINARY SPECIFICATION
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*THE DTC-1Ø-1 HAS DMA CAPABILITY

WARRANTY DISCLAIMER:

ANY MODIFICATION OR ALTERATION TO THIS BOARD AUTOMATICALLY NULLIFIES ANY WARRANTY OFFERED BY DTC OR ITS DISTRIBUTORS.

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1.0 INTRODUCTION

The DTC-10-1 Host Adapter is a single board interface card for the IEEE 696.1 S-100 Bus. This host adapter may be utilized with any of the Data Technology Corporation 1KA Series Disk Drive Controllers. This specification provides the programming mechanism and command block format utilized by the DTC-10-1 Host Adapter. The detailed specifications for the DTC controllers can be found in the respective controller documentation.

The DTC-10-1 Host Adapter fits into a single S-100 Bus slot and presents one unit load to the bus.

Commands are issued to the controller through the Host Adapter in the host computer. The controller accepts data from the Host Adapter and transfers the data to the correct location on the disk. In addition, the controller will detect/correct burst errors from the fixed disk drive (4 bits in length) before data is transferred to the host computer (on hard disk and non-IBM format floppies only).

1.1 Sample Disk Subsystems

The DTC-10-1 Host Adapter will operate with any DTC controller with the standard DTC-1KA host interface. All of the DTC-1KA controllers have the identical host bus protocol, so that software developed for one controller can be easily modified for use with other DTC-1KA controllers. Each of the DTC controllers complies with the interface requirements for the particular disk drive; installation is therefore fairly simple.

A list of available DTC-1KA controllers and their respective disk drives follows. Because new, and sometimes plug-compatible, drives are constantly being introduced this list is only representative.

CONTROLLER	DISK AND CAPACITY
DTC 510	Seagate Technogy ST506 or equivalent (Olivetti, RMS, and Tandon Magnetics) 1 or 2 ST506 drives; 3 or 6M-bytes each
DTC 520	ST506 (1 to 2) and mini-floppy (1 to 3)
SA1410	Shugart Associates SA600

SA142Ø	Shugart Associates SA6ØØ with 96 TPI; mini-floppy
SA14Ø1	2 Shugart Associates SA1ØØØ (5 or 1ØM-bytes)
SA14Ø3	4 SA1ØØ's with non-IBM (ECC format) floppies
SA14Ø3D	SA1ØØØ with integral IBM-compatible single/double-density 8-inch flexible disk drive backup
SA1404	Shugart Associates SA4ØØØ (14 to 58M-bytes)
SA1404D	SA4ØØØ with SA8ØØ/85Ø integral IBM-compatible single/double-density flexible disk drive backup
SA14Ø6	SA1ØØØ with Data Electronics Streaker streaming tape backup (1Ø to 2ØM-bytes)
SA14Ø7	SA4ØØØ with DEI Streaker backup
DTC1Ø1	Memorex 1Ø1 (11 to 22M-bytes) Fujitsu 2321/2 (11 to 22M-bytes)
DTC1Ø1D	Memorex 1Ø1, Fujitsu 2321/2 and integral IBM single/double-density backup
DTC9ØØ/91Ø	Data Peripherals DP1ØØ (1ØM-bytes) 8-inch hard disk cartridge with SA1ØØØ fixed disk
DTC6ØØ/61Ø	CDC Finch (24M-bytes) with optional IBM single/double-density floppy backup

2.Ø DTC-1Ø-1 BASIC FEATURES

The DTC-1Ø-1 has a full set of features that enable it to be an integral part of an S-1ØØ system. Included in the circuitry are:

* Processor I/O and/or DMA data transfer logic
* DMA capable of operation to 3ØØK-bytes/sec
* Interrupt or tie-in to off-board vectored interrupt generator
* Phantom Boot capability
* 6 Mhz operation

2.1 Theory of Operation

Upon Reset the Phantom EPROM is enabled (removing a jumper can disable this function). The EPROM looks like a repeating sequence of 512 Bytes from address Ø to FFFFFF. The board will pull the Phantom line (67) only when a sMEMR cycle is initiated. Therefore, the CPU can read the boot program, tranfer it to regular memory, jump to it and disable the Phantom circuit, and then load a CP/M boot program from disk.

Disk commands are issued to the DTC controller via commands stored in the main memory (the command structure is described in section 4.Ø of each of the DTC controller specifications). Depending on the type of command, the controller will request up to 1Ø command bytes. Upon receipt of the last command byte, the controller will begin execution of the command.

For the data transfer commands, a check is performed on the disk address and status is flagged if it exceeds the drive limits. The data is stored in a sector buffer on the controller before it is transferred to the host or disk drive. This buffer eliminates any possibility of data overruns between the host and the disk.

Upon completion of the command, the controller will output the completion status to the data register in the host adapter. (Further delineation of the completion status may be requested by issuing the appropriate sense commands).

2.2 1KA Host Interface

The electrical interface to the DTC disk drive controllers are all based on a common bus structure. The DTC-1Ø-1 will work with any of these hard disk controllers as outlined in section 1.1 and Appendix B.

2.3 IEEE 696.1 Bus Interface

The ITC-1Ø-1 Host Adapter is designed to operate in S-1ØØ systems based upon the IEEE standard 696.1. It features 16-bit I/O addressing, 24-bit memory addressing and 8-bit data paths. The DMA arbitration operates according to the scheme described in the IEEE 696.1 publication. The IEEE 696 standard pin description is outlined in Appendix C.

3.0 DTC-10-1 HARDWARE AND OPERATION

3.1 Interface Register Definition

The interface registers for the DTC-10-1 Host Adapter are listed below. B represents the 6 most significant bits of the I/O address (or the 14 most significant bits in a 16-bit I/O address.)

BIX Address	Register	
b0	Data in/out Register	DAR
b1	Control Register (write only)	CNR
b1	Completion Status Register (read)	CSTAT
b2	Status Register (read only)	PSTAT
b2	Clear DMA Address (write pulse)	CLRDMA
b3	DMA Address (write only)	DMADD
b3	Clear Phantom Status (read pulse)	CLRPHANT

3.1.1 Register Definition

DATA INPUT REGISTER - Disk read data, completion status, and controller sense bytes are passed through this register. The data is held for each handshake cycle.

DATA OUPUT REGISTER - Command bytes and disk data are passed through this register to the controller. Data is latched and held until updated by the host.

CONTROL REGISTER - Provides control over the controller select process and host adapter operations.

COMPLETION STATUS REGISTER - Stores the controller completion status during both DMA and non-DMA command cycles.

STATUS REGISTER - Enables the host to read the status of the host bus and monitor the host adapter opertation.

CLEAR DMA ADDRESS - A write to this port produces a pulse that resets the internal DMA address counter to zero

CLEAR PHANTOM STATUS - A read to this port disables the on board Phantom boot PROM, so the host can resume normal operation.

DMA ADDRESS REGISTER - DMA address bytes are sent to this register in the following order: Byte address 16 to 23, 8 to 15, 0 to 7. If only 16-bit addresses are used in the host computer, two bytes must be sent.

3.1.2 Bit Definition For Unique Registers

Control Register (CNR)	Output Address MN1
Bit 7	Not used
Bit 6	Assert select and Data bit Ø - used to access a controller.
Bit 5	Not used
Bit 4	Interrupt Enable - enables the interrupt channel, must be set prior to Bit 3.
Bit 3	Request Interrupt Enable - the interrupt will activate if REQ is present.
Bit 2	Not used
Bit 1	Enable data, after the selection process.
Bit Ø	DMA Enable - the DMA channel will activate when REQ and DATA are present.

BUS STATUS - processor can read status of host bus

Bus Status (BSTAT)	Input Address MN3
Bit 7	REQ - indicates the controller either requests data or has data for the host adapter.
Bit 6	IN/OUT* (reference to controller) - low indicates data to host adapter, high indicates data to controller.
Bit 5	MSG - indicates last byte in data or command string.
Bit 4	COM/DTA* - a command to the controller will have a high, data will be low.
Bit 3	BUSY - indicates the status of the busy signal; high means controller is busy.
Bit 2	PERR - received parity error. This bit set indicates that the data from the controller had a parity error. This bit is reset by outputting a COMMAND (b01)
Bit 1	IINT - Interrupt has been activated. This bit is reset by reading BSTAT.
Bit Ø	DONE - this bit is set when the DMA is not enabled or if a DMA has completed. It is reset when the DMA is enabled.

3.2 Normal Command Sequence Operation

The method by which a command is executed is as follows:

1 - Device driver builds a Command Descriptor Block (CDB) in system memory (see section 4.0 of the appropriate DTC controller specification).

2 - The driver then writes the address of the first byte of the CDB into the Command I/O Pointer Block (CIOPB) of the command driver routine.

3 - The DATA ADDRESS (DAD) is also set up if a data transfer is required. Commands requiring data transfers are READ, WRITE, READ ID, REQUEST SENSE, REQUEST SYNDROME, and WRITE ECC. If the DMA channel is to be used, the DAD is written into the DMADD register in the following order: most significant byte, middle byte and least significant byte.

4 - The driver now performs a GETCON routine which determines if the controller is busy. When it is not busy, the GETCON routine will assert the SELECT line until the controller responds with a BUSY.

5 - When the controller responds to the host adapter by asserting BUSY, the driver shifts to the OUTCOM routine. In response to the REQuest bit in the BSTAT, the driver passes the command one byte at a time to the controller.

6 - The controller verifies that the command is correct and begins the command execution phase. At this time the data is transferred to or from the host adapter and into or out of the S-100 memory. If the DMA is activated, the rest of the command cycle will proceed automatically.

7 - After the data transfer is completed, the controller enters the command completion phase. The controller sends a one-byte completion status to the host adapter indicating whether or not an error occurred during command execution. This is handled by the CMPSTAT routine in the programmed I/O mode or automaticaly in the DMA mode. Finally, the controller sends the message byte (of zeroes), and the operation is complete. The DONE bit will be set if in DMA mode.

8 - At this time the controller enters the idle (non-BUSY) mode awaiting another command. If an error was encountered by the controller, the CMSTAT routine will return with it in the C register. It is the responsibility of the device driver to issue a REQUEST SENSE command to request any detailed information about the error.

3.3 Hardward Theory Of Operation

The DTC-10-1 Host Adapter serves as a data channel for the controller. Commands and data are fetched/stored to the system memory as a function of REQ. The host adapter consists of Command and Status Registers, a DMA channel, and an interrupt latch. The registers are addressed as I/O ports. Commands and data are passed through these registers as a function of the I/O driver routine and the controller status lines. The host adapter will return an ACK after each DATA or COMMAND cycle has been completed.

Each memory cycle is initiated when the controller asserts REQ. The driver will respond by reading/writing the data register.

When data is transferred to the host adapter, the data on the host bus is held until the memory write is completed. When data is transferred to the controller, the data is latched into a holding register, then sent to the controller.

3.3.1 I/O Logic Operation (Bus Slave)

The host adapter responds to commands from the CPU processor to either read a particular register or write to a register. The 14-bit address selection (4 I/O locations = 2 Bits) is set with the dipswitches at location 12D (Address bits 15 to 8) and 7D (Address bits 7 to 2). The dipswitch selects a block of four I/O addresses. A read is selected when lines DBIN, PR/W*, and SINP are asserted with the appropriate I/O address. A write is performed when SOUT is high and PR/W* is low along with the I/O address. Because low power Schottky logic is used, the I/O logic will perform at the highest speed clocks now currently in use.

3.3.2 I/O Logic DMA Channel

The DMA channel is activated when the DMA enable bit is set and REQ and DATA are passed from the controller. The DMA begins the IEEE 696 arbitration process by pulling down the HOLD line and asserting the DMA arbitration bits DMA0* through DMA3*. The DMA priority is set by the 8-pin DIP switch below 4B. When the the CPU responds with HOLDA the arbitration process is complete. If the arbitration is unsuccessful for the DTC-10-1 it will try again as soon as HOLDA goes low. After a successful arbitration, the DMA will begin transferring data under the command of the controller. Once the host adapter has the bus the entire data move can proceed without dropping the bus, or the host adapter can be set to drop the bus after each cycle. This function is set by a jumper at location TP2 (near 3B). It is recommended that dynamic memories be self-refreshing as a Z-80 based refresh will be inhibited by the DMA cycle. The DMA logic will respond to a memory that is not ready (pREADY or XREADY) by stretching the read and/or write pulses. If the controller asserts IN, then the DMA will read data from memory. If IN is deasserted, then the DMA will write to memory. When COMMAND is asserted the DMA will drop the bus and input the completion status to the CSTAT register. Upon receipt of the MSG bit, the DONE bit will be set. If the Interrupt enable is set, the MSG bit will cause an interrupt.

3.3.3 Interrupt Logic

The DTC-10-1 can cause an interrupt in two ways. If INTEN is set, then RINTF is set (on succeeding writes to the BCCN port). The interrupt will activate when, and if, a REQ is present. This can be used in a read operation when the command string is passed to the controller, but there is a time lag before a seek and read operation is complete. The controller sector buffer must be full before the read data is passed to the host adapter. If DMA is active, the interrupt can be set to operate when the command cycle is complete. When the interrupt is active, the INT line, the NMI line or one of the vectored interrupt lines will be pulled down (i.e., set by jumpers E1 thru E11). The interrupt is cleared by a read to the bus status register (BSTAT).

4.0 ELECTRICAL/MECHANICAL SPECIFICATIONS

HOST ADAPTER PHYSICAL PARAMETERS

(The DTC-10-1 Host Adapter fits into a single S-100 slot).

Width	10.0	inches
Length	5.125	inches
Height	0.75	inch
Weight	0.7	lbs.

ENVIRONMENTAL PARAMETERS

	Operating:	Storage:
Temperature (degrees F/C)	32/0 to 131/55	-40/-10 to 167/75
Relative Humidity (@ 40 degrees F, wet bulb temp, no condensation)	10% to 95%	10% to 95%
Altitude	sea level to 10K feet	sea level to 15K feet

POWER REQUIREMENTS

Voltage @ current(host adapter) +8 VDC @ 1.5A(max)

Note: For the physical parameters of the controller, refer to its DTC controller specification.

5.0 INSTALLATION

5.1 Inspection

Inspect all shipping containers for damage. If a container is damaged, the contents should be checked and the DTC-10-1 Host Adapter verified electrically. If the host adapter is damaged, call Data Technology Corporation Customer Service for Return Material Authorization number. Please retain all shipping labels and documentation.

5.2 Preparation For Use

Before the DTC-10-1 Host Adapter can be used, initial setup may be required. Be sure the power requirements for the Host Adapter are met (section 4.0). The host adapter is installed in a vacant slot in the S-100 backplane.

A 50-pin, mass-terminated cable connects the host adapter to location J6 on the DTC controller board (pin 1 is marked on the host adapter connector as a triangle or dot and on the controller silkscreen). Refer to the interconnection diagram in the appropriate controller specification for connection of the controller to the disk drives. Note that all cables, including drive cables, are of the mass-terminated type, so no inadvertant signal swapping can occur.

Be sure the controller has adequate DC power (refer to the controller specification; the controller maintains the same power connector pinouts as the disk drive). To set up the controller, refer to the switch setting instructions found in the controller specification.

The following sections describe in detail the proper jumper settings on the host adapter.

5.2.1 Address Switches

The address switches are located in positions 12D and 7D.

Note: If the switch is on, the logic compares for zero (ØV to Ø.8V) on the S-1ØØ bus. Bit assignment is as follows:

12D Position	Address	Label
1	A15	F
2	A14	E
3	A13	D
4	A12	C
5	A11	B
6	A1Ø	A
7	A9	9
8	A8	8

7D Position	Address	Label
1	BOOT A9	U
2	BOOT A1Ø	T
3	A7	7
4	A6	6
5	A5	5
6	A4	4
7	A3	3
8	A2	2

5.2.2 DMA Priority Switch

The DMA priority is set by an 8 pin DIP Switch below 4B.

Position	Function	Label
1	DMA3	3
2	DMA2	2
3	DMA1	1
4	DMAØ	Ø

If an external vectored interrupt controller is being used the INT line may be jumpered to the vectored interrupt lines VIØ through VI7 (4 to 11) instead of pin 73.

5.2.3 Parity

The ITC-10-1 generates odd parity with the standard parity jumper at TP1 (near 12A). On outputs from the controller the odd parity is checked and the PERR bit is set if bad parity is found.

5.2.4 Phantom EPROM

The ITC-10-1 has a socket for a BOOT PROM (at 7A) that can be accessed in the Phantom mode. There is also a Phantom state generator circuit that is set by RESET* or PCR* and reset by a read to b3. If the Phantom feature is not wanted, jumpers TP3 and TP5 should be disconnected. If the Phantom state generator is to be on an another board, but the on board phantom PROM is to be read, then jumpers TP3 should be disconnected and jumper TP5 sould be connected. The 2716 used as the BOOT PROM is switch-selectable by Dipswitch 5D, positions 1 and 2, to determine which 512-byte segment (out of 2048 bytes) is to be read in the Phantom mode.

5.2.5 Jumper Summary

Jumper	Postion	Function	Description
TP1	12A	Host Data Parity	Preset for odd parity
TP2	3B	DMA Control	c-h DMA will hold for duration of data transfer
			c-d DMA will drop after each cycle
TP3	13B	Phantom Control	Connects on-board Phantom generator to S-100 bus
TP4	9D	Extend I/O Address	c-ext enables extended I/O address to 16 bits; 65,536 addresses
			c-gnd enables 8-bit I/O address range; 256 addresses
TP5	14D	PROM Read	Enables PROM to be read in Phantom mode

5.3 Initial Checkout

The initial verification of the disk subsystem can be done via an appropriate monitor PROM, or through a debugging utility such as DDT under CP/M*.

First, verify that all the interface registers are accessible through the correct addresses and that the registers can be read/ written with the expected results. Install driver routines by reading Appendix A or the ITC S-100 Driver BIOS Diskette. Next, attempt to issue a few commands to the disk subsystem, again via the console.

A recommended approach is to first issue a RECALIBRATE command. After verifying that it executed correctly, issue a SEEK command to verify that the logical Address calculation has been performed correctly. Then, issue a FORMAT DRIVE command; the recommended interleave for the S-100 system running at 2MHz is 4. Finally, data transfer commands should be issued to verify the data. All commands can be issued via the console programmer's interface.

6.0 REFERENCE DOCUMENTATION

This section provides information regarding the documentation available for using the DTC-10-1 Host Adapter.

6.1 DTC-Supplied Documentation

6.1.1 DTC Controller Specifications

Each controller that is manufactured by DTC is described by its own specification. Refer to the appropriate controller document when attempting to program the disk subsystem.

6.1.2 DTC Software Manual

This manual explains how to install CP/M onto your system using the DTC-1403D Controller and the DTC-10-1 Host Adapter. Also available is a DTCPICS diskette.

6.2 Other Documentation

6.2.1 IEEE S-100

a. IEEE 696.1 Standard Specifications for S-100 Bus Interface Devices.

b. S-100 CPU/ System Manual - use the version appropriate for your system.

6.2.2 Disk Drive Documentation

Use the appropriate drive manufacturer's manual for your disk drive.

APPENDIX A COMMANDS/PROGRAMMING

An I/O request to the DTC controller is performed by passing a command descriptor block (CDB) to the controller. The first byte of a CDB is the command class and opcode. The remaining bytes specify the drive logical unit number (LUN), block address, control bytes, and number of blocks to transfer. The controller performs an implied seek and verify when commanded to access a block.

Due to the different types of commands each controller recognizes, the command format for the DTC-10-1 Host Adapter will only indicate the skeletal representation of the command. The reader is directed to section 4.0 of the appropriate DTC controller specification for more detailed command information.

A.1 Command Format

A.1.1 Commands Requiring 6 Bytes

7 6 5 4 3 2 1 0	
Command Byte 0	XXXX
Command Byte 1	XXXX + 1
Command Byte 2	XXXX + 2
Command Byte 3	XXXX + 3
Command Byte 4	XXXX + 4
Command Byte 5	XXXX + 5
7 6 5 4 3 2 1 0	

XXXX is the HEX address that is loaded into the CIOPB location

A.1.2 Commands Requiring 10 Bytes

7 6 5 4 3 2 1 0	
Command Byte 0	XXXX
Command Byte 1	XXXX + 1
Command Byte 2	XXXX + 2
Command Byte 3	XXXX + 3
Command Byte 4	XXXX + 4
Command Byte 5	XXXX + 5
Command Byte 6	XXXX + 6
Command Byte 7	XXXX + 7
Command Byte 8	XXXX + 8
Command Byte 9	XXXX + 9
7 6 5 4 3 2 1 0	

XXXX is the HEX address that is loaded into the CIOPB location

A.2 Request Syndrome Command

The REQUEST SYNDROME Command returns 2 bytes of information. The data returned for the REQUEST SYNDROME Command is listed as follows:

7 6 5 4 3 2 1 0	
Data Byte 0	XXXX
Data Byte 1	XXXX + 1

XXXX is the HEX address that is loaded into the DMA location

A.3 Drive and Controller Sense Information

Upon execution of the REQUEST SENSE command, the controller returns four bytes of information in the following format. (Refer to Drive and Controller Sense in section 4.0 of the DTC controller specifications for a detailed interpretation of these bytes).

7 6 5 4 3 2 1 0	
Data Byte 0	XXXX
Data Byte 1	XXXX + 1
Data Byte 2	XXXX + 2
Data Byte 3	XXXX + 3

XXXX is the HEX address that is loaded into the DMA location

Note: Data that is received from the controller as well as data that is sent to the controller will be transferred in the above order.

APPENDIX E HOST BUS PIN ASSIGNMENT

The host I/O bus uses a 50-pin connector (AMP 2-87227-5 or equivalent). The unused pins are spares for future use. The pin assigments are as follows:

Signal	Pin Number	
DATA0	2	
DATA1	4	
DATA2	6	
DATA3	8	
DATA4	10	
DATA5	12	
DATA6	14	
DATA7	16	
PARITY	18	
--	20	Future Usage
--	22	
--	24	
--	26	
--	28	
--	30	
--	32	
--	34	
BUSY	36	
ACK	38	
RST	40	
MSG	42	
SEL	44	
C/D	46	
REQ	48	
I/O	50	

Note: All signals are negative true and all odd pins are connected to ground. The signal lines are terminated with 220 ohms to 5V and 330 ohms to ground.

APPENDIX C IEEE S-100 SYSTEM BUS SIGNAL DEFINITION

IEEE S-100 Bus
Component Side Pins

Pin	Signal	Description
1	+8 volts	Logic power - unregulated, max < 11.5v
2	+16 volts	Aux power - unregulated, max < 21.5v
3	XRDY	Act H, one of two bus ready signals
4	VI1*	Vectored interrupt line 0, active low, open collector; used with a vectored interrupt circuit to speed interrupt handling.
5	VI1*	See pin 4
6	VI2*	" " "
7	VI3*	" " "
8	VI4*	" " "
9	VI5*	" " "
10	VI6*	" " "
11	VI7*	" " "
12	NMI*	Non-maskable interrupt; active low, open collector.
13	PWRFAIL*	Power failure signal, active low
14	DMA3*	DMA request; active low, open collector
15	A18	Extended address bit 18
16	A16	Extended address bit 16
17	A17	Extended address bit 17
18	SIXB*	Disable the 8 status signals; active low, open collector
19	CDSB*	Disable the 5 control output signals; active low, open collector
20	GND	Extra ground
21	NDEF	Not defined
22	AIXB*	Disable the address lines (first 16); active low, open collector
23	DCISB*	Disable data output lines; active low, open collector
24	Phi Clk	Phase 1 master timing for the bus
25	PSTVAL	Status valid strobe; active low, at PSYNC time indicates that stable address and status are on the bus.
26	PHLDA	Hold acknowledge signal, active high
27	RFU	Reserved for future use
28	RFU	
29	A5	Address bit 5
30	A4	Address bit 4
31	A3	Address bit 3
32	A15	Address bit 15

33	A12	Address bit 12
34	A9	Address bit 9
35	DO1	Data out bit 1, bidirectional data 1
36	DO0	Data out bit 0, bidirectional data 0
37	A10	Address bit n10
38	DO4	Data out bit 4, bidirectional data 4
39	DO5	Data out bit 5, bidirectional data 5
40	DO6	Data out bit 6, bidirectional data 6
41	DI2	Data in bit 2, bidirectional data 10
42	DI3	Data in bit 3, bidirectional data 11
43	DI7	Data in bit 7, bidirectional data 15
44	SM1	Status indicating machine code fetch
45	SOUT	Status indicating I/O output cycle
46	SINP	Status indicating I/O input cycle
47	SMEMR	Status indicating memory read - not an interrupt instruction fetch
48	SHLTA	Status indicating halt instruction is being acknowledged
49	CLOCK	A 2MHz clock - not required to be synchronous with other events
50	GND	Main ground

S-100 Circuit Side Pins

51	+8 volts	See pin 1
52	-16 volts	Negative aux power, unregulated, max <21.5v
53	GND	Extra ground
54	Slave CLR*	Resets bus slaves, is active with POC
55	DMA0*	DMA arbitration line, active low, open collector
56	DMA1*	same as DMA0*
57	DMA2*	same as DMA0*
58	SXTRQ*	Status signal which requests that 16-bit slaves assert SIXTN*
59	A19	Extended address bit 19
60	SIXTN*	An active low signal asserted by 16-bit bus slaves in response to SXTRQ*
61	A20	Extended address bit 20
62	A21	Extended address bit 21
63	A22	Extended address bit 22
64	A23	Extended address bit 23
65	NDEF	Not defined
66	NDEF	same as above
67	PHANTOM*	Creates an alternate bank of memory, usually after PCR* or RESET*
68	MWRT	Status indicated memory write

69	RFU	
70	GND	Extra ground
71	RFU	
72	RDY	Ready, indicates memory or I/O is ready; active high, open collector
73	INT*	The primary interrupt request signal is low true, open collector.
74	HOLD*	Request processor stop for DMA purposes; active low, open collector
75	RESET*	Master reset signal; active low, open collector
76	PSYNC	Control signal indicating beginning of new bus cycle
77	PR/W*	Read high, write low with data from CPU valid during low phase.
78	PDBIN	Control signal requesting input data
79	A0	Address bit 0
80	A1	Address bit 1
81	A2	Address bit 2
82	A6	Address bit 6
83	A7	Address bit 7
84	A8	Address bit 8
85	A13	Address bit 13
86	A14	Address bit 14
87	A11	Address bit 11
88	DO2	Data out bit 2, bidirectional data 2
89	DO3	Data out bit 3, bidirectional data 3
90	DO7	Data out bit 7, bidirectional data 7
91	DI4	Data in bit 4, bidirectional data 12
92	DI5	Data in bit 5, bidirectional data 13
93	DI6	Data in bit 6, bidirectional data 14
94	DI1	Data in bit 1, bidirectional data 9
95	DI0	Data in bit 0, bidirectional data 8
96	SINTA	Status indicating fetch of interrupt instruction
97	SWO*	Status indicating transfer of data from bus master to bus slave
98	ERROR*	Status indicating error condition during the present bus cycle
99	POC*	Power on clear, must remain low for 10ms
100	GND	Main ground

APPENDIX D SAMPLE PROGRAM FOR THE DTC-10-1 (PROGRAMMED I/O)

The DTC-10-1 Host Adapter uses programmed I/O, taking advantage of the fact that the DTC controllers have a built-in sector buffer. The control lines of the host bus are available to the CPU through the Bus Status Register. Data and commmands are transmitted through the host bus by a simple handshake procedure as outlined in the DTC controller specifications. The types of commands available to the user are as follows:

STATUS Sends drive status to host adapter

- TEST DRIVE READY
- REQUEST SENSE
- CHECK TRACK FORMAT
- REQUEST SYNDROME

MOTION CONTROL Moves heads without R/W operation

- SEEK
- RECALIBRATE

R/W Read Write Operations

- READ
- WRITE
- COPY

FORMAT Formats drive or tracks with specified standard format

- FORMAT TRACK
- FORMAT BAD TRACK
- FORMAT DRIVE

DIAGNOSTICS Runs controller microdiagnostics

- RAM DIAGNOSTIC
- WRITE ECC
- READ ID
- DRIVE DIAGNOSTIC

Flow Diagrams

Status commands:

GET CONTROLLER
SEND COMMANDS to controller
READ STATUS DATA
COMPIETICN STATUS

Motion Control:

GET CONTROLLER
SEND COMMANDS to controller
COMPIETION STATUS

Write Sector(s):

GET CONTROLLER
SEND COMMANDS
LOAD DATA
COMPIETION STATUS

Read Sector(s):

GET CONTROLLER
SEND COMMANDS
WAIT FOR REQ
READ DATA
COMPIETION STATUS

Copy:

GET CONTROLLER
SEND COMMANDS
COMPIETION STATUS

Diagnostics:

GET CONTROLLER
SEND COMMANDS
COMPIETION STATUS

PROGRAMMMING:

```
BASE equals Base I/O Address
DATAIN equals BASE
DATAOUT equals BASE
BCON equals BASE+1 ;Buss Control
BSTAT equals BASE+2 ; Bus Status
DMAOUT equals Base+3 ; DMA control bytes
DMAIN equals BASE+3  ; DMA status information
CIOPB ; Command Address
DMA   ; Data Address bits 0 to 7
DMA+1 ; DMA bits 8 to 15
DMA+2 ; DMA bits 16 to 23
PIC equ true ; Processor I/O data transfer
DMAT equ not PIC ;DMA data transfer
```

Sample program to GET CONTROLLER:

```
GETCON: IN BSTAT            ;input from status port
        ANI 08H             ;select bit 3 (busy)
        JNZ GETCON          ;if busy wait in getcon loop
        MVI A,40H           ;get ready to assert SEL and DATA0
        OUT BCON            ;to get attention of controller
CBUSY:  IN BSTAT            ;input from bus status
        ANI 08H             ;again look at BUSY
        JZ CBUSY            ;we have controller attention else loop
        MVI A,02H           ;get ready to allow data enable
        OUT BCON            ;done
        RET                 ;return from get controller routine
```

Sample program to OUTPUT COMMANDS:

```
OUTCOM: LHLD CIOPB          ;load pointer to command queue
COMREQ: IN BSTAT            ;input from bus status
        MOV C,A             ;store in C
        ORA A               ;set flags
        JP COMREQ           ;wait for REQ
        ANI 10H             ;check for command/ data
        RZ                  ;return when data is requested
        MOV A,C             ;also see if controller switched direction
        ANI 40H
        RZ                  ;if it wants to send data, return
        MOV A,M             ;move commands from queue to accumulator
        OUT DATAOUT         ;write comands to controller
        INX H               ;increment pointer
```

```
        JMP COMREQ          ;loop as long as commands are requested
```

Sample program to SEND DATA TO CONTROLLER (a WRITE operation):

```
        LHLD DMA            ;load pointer to data (16 bit address)
DAREQ:  IN BSTAT            ;input from bus status
        MOV C,A             ;store
        ANI 80H             ;set flags
        JZ DAREQ            ;wait for REQ
        ANI 10H             ;check for COM
        JNZ CMPSTAT         ;on receipt of command completion status is
                             present
        MOV A,M             ;move data into accumulator
        OUT DATAOUT         ;output to controller
        INX H               ;increment pointer
        JMP DAREQ           ;go back for another byte
CMPSTAT:IN DATAIN           ;input completion status
        MOV C,A             ;place in C for futher use
IREQ:   IN BSTAT            ;looking for last REQ
        MOV B,A             ;save for checking
        ANI 80H             ;check for REQ
        JZ IREQ             ;loop untill found
        IN DATAIN           ;input last byte
        ORA A               ;see if last byte is non-zero
        JNZ BADBYTE         ;if last byte is non zero
        MOV A,C             ;now check completion status
        ORA A               ;to see if it is zero
        JNZ BADSTAT         ;if not zero
        MOV A,B             ;Now check last bus status
        ANI 01H             ;for parity error
        JNZ BADPAR          ;high is bad parity
        XRA A               ;zero accumulator
        RET                 ;GREAT! everything is OK
```

For information on how to decode errors generated, refer to the appropriate DTC controller specification.

Sample program to READ DATA FROM CONTROLLER:

```
READ:   LHLD DMA            ;load data pointer
RDREQ:  IN BSTAT            ;input bus status
        MOV C,A             ;store for further checking
        ANI 80H             ;look for REQ
        JZ RDREQ            ;else loop
        MOV A,C
        ANI 10H             ;check for COM
        JNZ CMPSTAT         ;if COM present must be completion status
        IN DATAIN           ;input data from controller
        MOV M,A             ;move data to pointer
        INX H               ;increment pointer
        JMP RDREQ
```

APPENDIX E DMA PROGRAMING

DMA programming is actually simpler than the processor I/O scheme, because the driver routine does not have to know if the command is read or write. Before the data transfer the DMA is enabled (which resets the done bit). Commands which do not involve data transfers should use the processor I/O routine since the DMA is never turned on. These are check drive ready, check track, seek, recalibrate (class 0), and class 1, and class 6 commands.

GETCCN is identical with PI/O routine.

```
DMACOM:   MVI A,3
          OUT BCON          ;enable DMA channel
          LDA DMA+2         ;get most significant byte of address
          OUT DMAOUT        ;sent it to DMA address register
          LDA DMA+1
          OUT DMAOUT
          LDA DMA           ;least significant byte of address
          OUT DMAOUT
          MVI B,6           ;set up byte count
          LHLD CIOPB        ;set up command pointer
DCOMREQ:  IN PSTAT          ;look at host bus
          MOV C,A
          ORA A
          JP DCOMREQ        ;wait for REQ
          ANI 40H           ;see if input, output means illegal command
          JZ CMPSTAT        ;illegal, finish with PIO
          MOV A,M
          OUT DATAOUT       ;output command byte
          INX H
          DCR B             ;decrement byte pointer
          JNZ DCOMREQ       ;do more bytes
DONE?:    IN BSTAT          ;now wait for DONE bit
          ANI 1
          JZ DONE?          ;the transfer is complete and the
                             completion status is in the CSTAT
                    Register.
          IN CSTAT
          MOV C,A
          RET
```

8	7	6	5	4	3	2	1

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

S100 BUS — LS244 — 18D DIP SWITCH — 25LS2521

A16 A15 A13 A12 A11 A10 A9 A8 — 18O 110

A7 A6 A5 A4 A3 A2 — 7D 8136 8D — 4.7K RP5 — 7D DIP SWITCH

A1 A0 — LS244

SOUT PWR SINP SINT — LS14

SMEMR PHANTOM — LS14 — LS245 — 12C

DI7 DI6 DI5 DI4 DI3 DI2 DI1 DI0 — XFER II (2B6)

DO7 DO6 DO5 DO4 DO3 DO2 DO1 DO0 — 11C — XFER II (2C7)

1K RIS — +5 — BUFFERED ADDRESS (1C6) TO 2716

LS139 — 14C — LD DMA (2B7) — CLR DMA (2B6) — LD CON (1A6) — LD DTA (1C3)

LS139 — 14C — CLR PHANT (2D4) — RD STAT (1C4,1D3) — RD COMP (1B4) IN A1 — RD DTA (1C4)

LS13 — 13C — LS13 — 13C — LS132 — 15D — PROMOE (1D3)

MEMR (2D4) — LS13 — 14D — (1C3) PROMRD — R5 4.7K JUMPER TP5 — VCC

LS551 — 15C — XFER II (2C7) — XFER II (2B6) — IN (1B2,1B5,1C4,2C2,2D2)

LS551 — 9C — XFER II (2C7) — SOUT (1C8,2A8) — XFER II (2B6) — OUT (1B2,1B4,1B6,2C2,2C3,2C5)

(1B7) PROMOE — (2D4) PROMEN — 7D DIPSWITCH RP3-5 — R3 4.7K — 2716 — +5V

(1C7) BUFFERED ADDRESS

TA — 2716Ω — 2716 EOT PROM — Out A2

(1C3) INTEN — (2C3) DMA INT — (1B4, 1C2, 1C3, 1D5, 2B4, 2C5) REQ — (1C3) RINE — LS00 — 15B

LS244 — 10B — (1D5) REQ — (1B6) IN — (1C2) MSG — (2A5) COM — (1C2) BUSY — (1A5) PERR — (1D2) LINT — (2B4) DONE

RD STAT (1C6)

(1C3, 1C6, 2B5) LD CON — (2A7) RESET — LS00 — 13A

(1B4, 1B5) REQ OUT — 16B LS74 — PERR (1C5)

(1D5) REQ — 16B LS74 — T43B — 15A — ACK (1B1)

ENABLE DATA (1C2, 1C3)

DACK (2A4) — DMACK (2C2) — LS11 — 15C

(1B4) REQ OUT — (2A5) COM — (1C1) MSG — LS11 — 15C — (1C6) RD COMP

PARITY (1B2) — 7438 — 16A — (1B6) IN — LS132 — 15D — (1A6) OUT

LS259 — EVEN — ODD — 12A

9A LS374 — COMPLETION STATUS

8A LS374 — DATA

11B LS273 — CONTROLLER DATA

VCC — 15A LS74 — RESET (2A7) — INTERRUPT CONTROL — RD STAT (1C6)

LINT (1C5)

T43B — 14B — E11 — S100 BUS

E1 E2 E3 E4 E5 E6 E7 E8 E10 E9 — VI 0 VI 1 VI 2 VI 3 VI 4 VI 5 VI 6 VI 7 INT NMI

LS273 — 12B — LD CON (1A6) — RESET (2A7)

INTEN (1D5) — RINE (1D5) — N.U. — ENABLE DATA (1C5)

VCC — 16C LS74 — LS14 — PROMRD (1B6) — (2B3) — FROM WAIT STATE — T43B — 14B — READY

T43B — 16A — DATA9

(1A6) RDDTA — LS08 — 6A — DWT (2C3)

LD DTA (1C6) — LS08 — 13A — DRD (2C2)

REQ (1D5) — LS08 — 6A — (1A5) REQ OUT — (1A6)

(2A7) RESET — (1C5) ENABLE DATA — LS14 — (1B6) IN — (1A6) OUT

11A 8641 — 19A 8641

RP3-6 P1 — RESET RP2-7 — BUSY RP3-4 — MSG RP3-2 — D/C RP3-7 — REQ RP3-5 — I/O RP3-3 — ACK RP2-4 — PARITY RP2-3 — DATA T RP2-2 — DATA 6 RP2-5 — DATA 5 RP1-4 — DATA 4 RP1-6 — DATA 3 RP1-2 — DATA 2 RP1-3 — DATA 1 RP1-5 — DATA 0 RP1-7 — 220/330

SEL 44 — RESET 49 — BUSY 36 — MSG 42 — D/C 46 — REQ 48 — I/O 39 — ACK 38 — PARITY 13 — DATA T 8 — DATA 6 14 — DATA 5 12 — DATA 4 10 — DATA 3 3 — DATA 2 6 — DATA 1 4 — DATA 0 2

1 TO 49 HOST BUS

(2B6)

+5 — 4.7K — 8 — 220 — 330 — 1 — 2,3,4,5,6,7

ECO#018A.4	REV. E	FAB. REV. 04	9-13-83	CB
ECO#018A.1	REV. C1	PCB FAB. REV. 2	12-22-82	CJ
PCB FAB REV. 01	SCHEM REV B	10-29-81		CT
PCB FAB REV. 00	SCHEM. REV. A	10-8-81		

10.2.83 ECO#018A.5 | REV. E1 | FAB. REV. 04 | K.D

QTY REQD	PSCM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE: FRACTIONS ± — DECIMALS .XX ± .XXX ± — ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN C. THEIN	2/23/81
CHECKED	3/9/81
ISSUED	

NEXT ASSY | USED ON

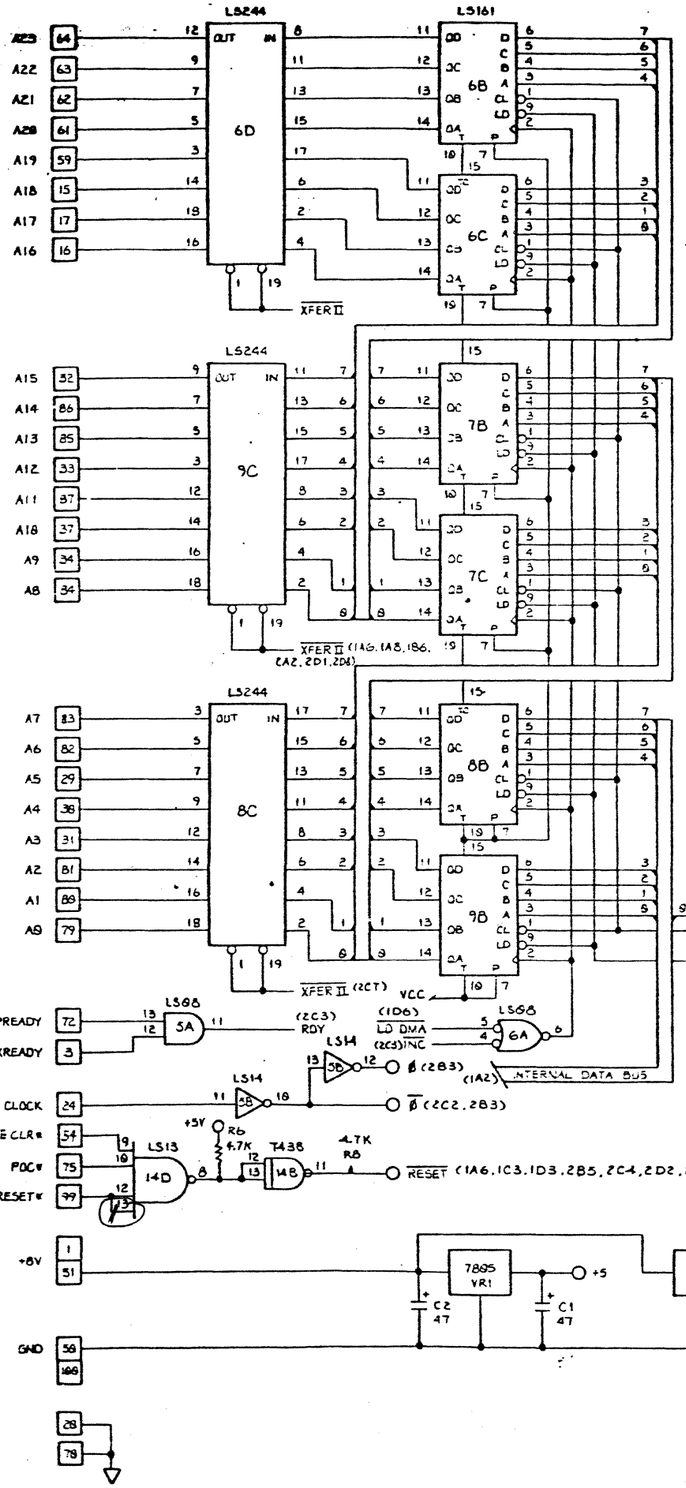
APPLICATION

DTC Data Technology Corporation

DTC 18-1 (PIO LOGIC)

SIZE	FSCM NO.	DWG. NO.	REV.
D		018A-99996	E

SCALE — SHEET 1 OF 2


LS244
LS161
6D
6B
6C
XFER II
9C
7B
7C
XFER II (1A6,1A8,1B6,
2A2,2D1,2D4)
8C
8B
9B
XFER II (2CT)
VCC
(1D6) LD DMA
(2C3) INC
LS08
5A
6A
PREADY
XREADY
(2C3) RDY
LS14
(2B3) Ø
(1A2) INTERNAL DATA BUS
MASTER CLOCK
SLAVE CLR#
POC#
RESET#
LS13
14D
R6 4.7K
T438
14B
4.7K R8
RESET (1A6,1C3,1D3,2B5,2C4,2D2,2D5)
+8V
GND
7805 VR1
7805 VR2
C2 47
C1 47
C3 47
.7 CER
CLR DMA (1C6)
XFER II (1A6,1B6,1B8,2A2,2C2,2C5)
LD CON (1A6)
(2AT) RESET
(1D5) REQ
(1B5,1C2,1C5,2C5) COM
DMA q ARM
DONE (1C5)
DATA
TP2
(1C5) DACK
LS74 4A
LS74 3A
LS74 2B
LS74 1B
R2
R7 4.7K
R1 100
100 pf C4
(2CT) XFER II
HOLDA (2B4)
(2B3) HOLDA
(2B6) XFER II
APRIO (2B4,2B3)
(1C2,2A3,2B7,2C4) Ø
LOST IT
(2A2) HOLDA
DIPSWITCH SW1
DIPSWITCH SW1 (BELOW 4B)
RP4-5
RP4-6
RP4-3
RP4-2
LS32
4C
4D
3D
T438
LS08
(2D3) SYNC
(2A7) Ø
(1C3) DRD
LS14
LS00
5C
5D
+5V
(1B6) IN
(2D3) SYNC
(1A6) OUT
DMACK (1C5)
(2B7) INC
(2B7) RDY
(1A6) OUT
DNT (1C4)
(1C2) MSG
DMA INT (1D5)
S175 1A
(2B3) Ø
RESET (2AT)
XFER I (2C2)
(2B3) XFER I
(2B6) XFER II
(2B3) HOLDA
PRIO (2B3)
HOLDA (2A2)
(2B7) INC
(2B7) RDY
(1A6) OUT
(1B6) IN
SYNC (2C2,2C3)
LS169
3B
(2A7) RESET
(2CT) XFER II
+5
VCC
LS244
LS08
5D
SMEMR
SINO
SMI
SOUT
SINP
SINTA
SHLTA
SXTRQ
PSYNC
PSTVAL
PDBIN
PWR
PHLDA
1DSB
2DSB
3DSB
CDSB
HOLD
DMA3
DMA2
DMA1
DMA0
HOLDA
CLR PHANT (1C6)
PROM EN (1D5)
RESET (2AT)
MEMR (1B7)
TP3
67
PHANTOM
LS00
7438
LS08
15B
15C
15D
14B
LS132
LS511
15C
LS08
2A
4B
5A
6A
LS08
4B
LS109
3B
LS08
2A
5A
5C
2A
3C
4D
3D
4C
LS32
LS08
3D
4D
T438
LS14
5B
LS00
5C
LS08
2A
5A
5C
2A
3C
4D
3D
4C
LS32
LS08
3D
4D
T438
LS14
5B
LS00
5C
LS08
2A
3C