NASA-AMES HYBRID COMPUTER FACILITIES AND THEIR APPLICATION TO PROBLEMS IN AERONAUTICS

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ABSTRACT

It has been our privilege at the Ames Research Center (Figure 1) to participate in the design and development of two advanced hybrid computing machines, the Ames linkage system and the digital logic simulator (DLS). Each of these is of the most recent design, and each has unusual capabilities for hybrid simulation.

The Ames digital logic simulator is described briefly, with the balance of the discussion in this first section directed toward three current problems selected to emphasize the tremendous range of application of this machine to simulation problems of all types.

The Ames linkage system is discussed in terms of those features which set it apart from other successful linkages rather than as a complete system, the discussion of which is beyond the scope of this paper. An outline of its operational characteristics for the reentry flight situation will be presented.

THE DIGITAL LOGIC SIMULATOR

The Ames digital logic simulator (DLS), a prototype of the EAI Series 350 Digital Operations System (DOS), was originally developed to cope with a class of control system problems where autopilot functions and control forces are formed by discrete on-off type signals and forces. In its first year of service, the DLS (shown in Figure 2) has been applied to a much wider variety of problems at the Ames Research Center than those originally foreseen, and promise for future applications seems unlimited. Particularly gratifying have been the new problems available to the analog simulation computers since being interconnected with the DLS. These areas include:

1. Data applications
    a. Data reduction
    b. Data readout
2. Simulation applications
    a. Simulation of logical control systems
    b. Simulation of transport delays
    c. Simulation display generation
3. Computer control applications
    a. Analog computer control
    b. Linkage system control

In the following discussion, there will be described briefly the logical elements available on the DLS and an illustration of the unique and versatile applications possible when these elements are combined with standard analog computers.

The DLS was designed as an accessory to the analog simulation computers, and was equipped,

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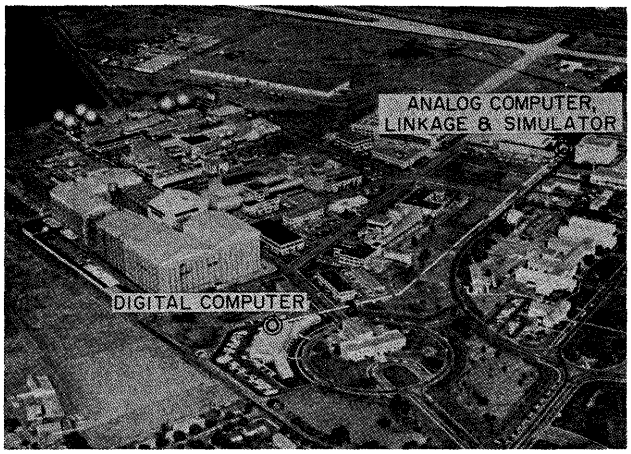


Figure 1. Aerial view of Ames Research Center showing the relative locations of the computer laboratories.

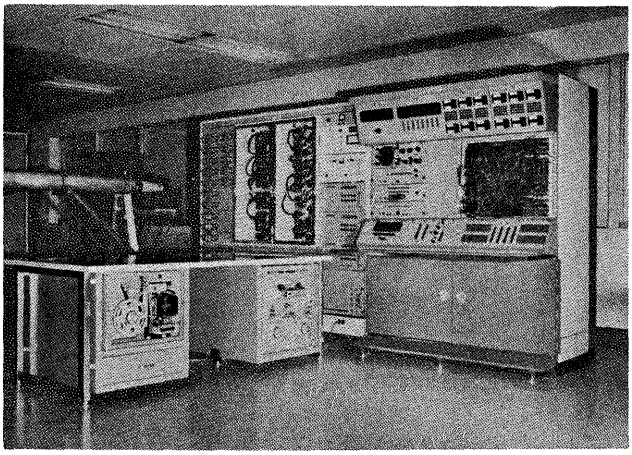


Figure 2. General view of Ames digital logic simulator showing main console and input-output equipment desk.

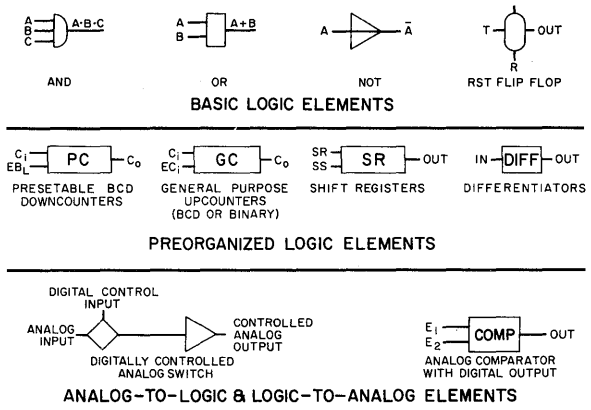


Figure 3. Programming elements available on the digital logic simulator.

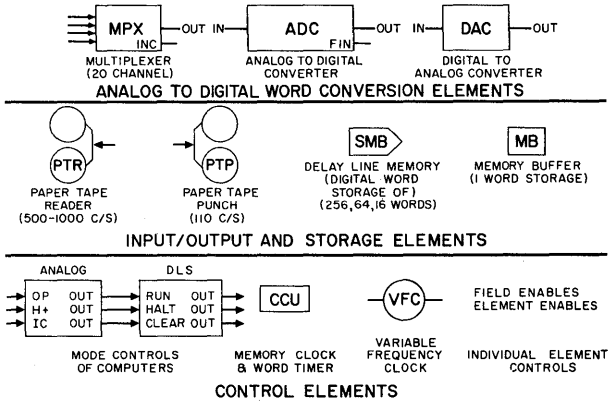


Figure 4. Programming elements available on the digital logic simulator.

therefore, to connect easily into the function with standard real-time computers. As presently constituted, the computer has the logical and digital components shown in figures 3 and 4, all of which are available for interconnection through a removable problem prepatch panel by the familiar analog patching method.

For purposes of illustration, the components have been divided into two general categories: logical operation, and digital word components. The logical operation components, shown in figure 3, are designed to permit direct mechanization of logic systems and their direct insertion into analog computer loops. The basic logic elements of figure 3 are the fundamental logic operations of the DLS and are self-explanatory. The preorganized logic elements shown would require sizable sections of basic logic to mechanize and, therefore, have been prepackaged to perform these more difficult functions with only simple input and output connections. This greatly simplifies programming and better utilizes available patch panel holes.

The comparators serve to introduce analog events into the logic computer, the state change of their digital output marking the coincidence of analog computer variables. The digitally-controlled analog switches (D/A switches) permit the introduction of logical events into control loops of the analog program by controlling the inputs to operational amplifiers.

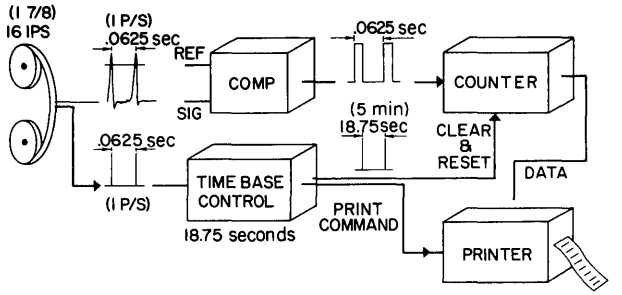
The digital word components illustrated in figure 4 consist of the MPX, ADC, and DAC units similar to those readily available on the commercial market. These units provide the capability of translating analog values into digital numbers and vice versa. The digital numbers so generated can be stored, outputted, or otherwise operated on by

use of the storage and readout elements shown. Included are memory elements (SM8, etc.), which are acoustic delay lines cut to various multiples of the 16-bit digital words used in the DLS for storage of digital numbers. The memory buffer (MB) is an element for holding single digital words for insertion into memory lines at the appropriate interval. The paper tape punch and reader permit fast input and output of DLS logic states or digital numbers.

One of the first applications of the DLS was the computation of average heart rate from electrocardiograph (EKG) signals that had been recorded on magnetic tape. The magnetic tapes contained continuous EKG data from two humans subjects enclosed in a small capsule for seven days. If one assumes one heart beat per second per subject, the data tapes contained an electrical record of 1.8 million heart beats. The data reduction requirement was to determine a time average of heart rate over a five minute period, to be computed continuously for the seven days' accumulation of test data. Figure 5 shows the basic program to compute heart rate for one of the two channels of this EKG data using DLS elements. A comparator detects the peaks of the EKG recording by having its reference level set so that only the main heart peak actuates it. The output pulses of the comparator are accumulated in a counter for five minutes and this accumulated content is printed out. The counter is then cleared and is ready to count peaks during the next interval.

Playback and data reduction in real time of these 168 hours of record would be very time consuming, so the tape (recorded at 1-7/8 inches per second) was played back at 16 inches per second, thus decreasing the data reduction time to 10.5 hours. The relative change in the timing of the program is shown in figure 5. The logic components and comparators present no difficulty at this increased data speed, since they still are orders-of-magnitude faster than playback events (i.e., comparators switch in 10 μ sec). Of concern at this playback rate is the speed of the printout mechanism. This problem is handled by devoting one register to holding and printing out, while another register accumulates the counts of the immediately following period. For two subjects, the printer is permitted nine seconds per printout, a very satisfactory safety margin for standard printers such as the Hewlett Packard 560.

The method of figure 5 has the disadvantage of responding readily to noise spikes and secondary heart actions, such as systoles. To aid in discriminating against these extraneous signals, a "window" generator shown in figure 6 was mechanized using a differentiator, two flip-flops, and a downcounter. The "window" action, so called because the comparator is only permitted to respond during the expected interval of the heart beat, is generated by latching the comparator until a preset counter interval has elapsed since the last heart beat. Figure 7 illustrates the final circuit configuration for one of the two channels. Timing marks from the data, instead of from machine-generated timing, can be used to operate the system at any tape speed, provided the window interval is adjusted to fit the playback pulse interval. Scaling the output readings for direct printout of average heart rate is accomplished by the double counting effect of the leading- and trailing-edge differentiator (abbreviated LE and TE in the figure), and division by 10 on the BCD counter by shifting the decimal point. These two actions result in the required division by five to give average beats per minute



	TAPE SPEED IPS	ECG RATE	AVERAGING INTERVAL	TOTAL RUNNING	READOUT = HEART BEATS / 5min
RECORD TIMING	1 7/8	~1 P/S	5 min	7 DAYS	350 360 355 358
PLAYBACK TIMING	16	.0625	18.75 sec	10.5 hr	

Figure 5. Basic method of computing average heart rate from ECG records.

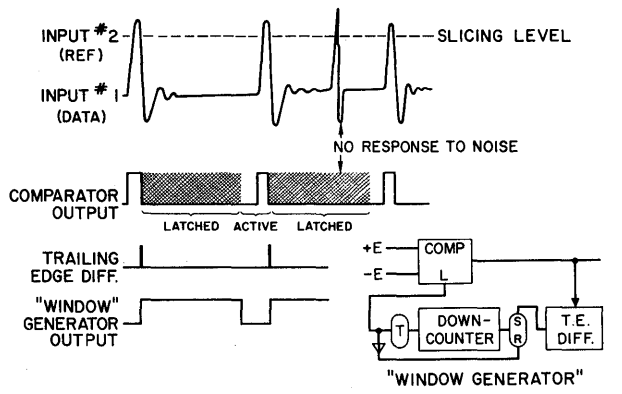


Figure 6. Noise discriminator technique for recurrent or periodic data.

over the five minute counting period. A summary of necessary logic elements shows:

19 flip-flops

90 AND gates

15 decades downcounting

8 decades upcounting

8 decades downcounting (used as holding registers)

Total running time, including tape handling, was two days.

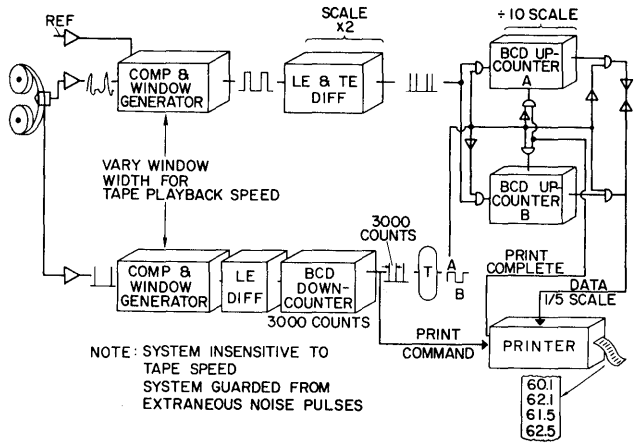


Figure 7. Detail of average heart-rate computation.

A somewhat allied technique of processing data by level selection and accumulation of resultant counts has been exploited by Mr. W. D. Cameron of the Ames Research Center staff. His technique has been reported separately in detail[1].

An example of the versatility of the DLS in flight simulation problems was particularly apparent in its application to a tracking task simulator shown in figure 8. In this investigation, tracking errors of pilots were studied. Figure 9 shows the degree of participation of the DLS in the simulation. The DLS function was to:

1. Control analog computer mode under pilot command

2. Generate control pulses for insertion into analog-computer dynamics

3. Accumulate control pulses for fuel consumption computation

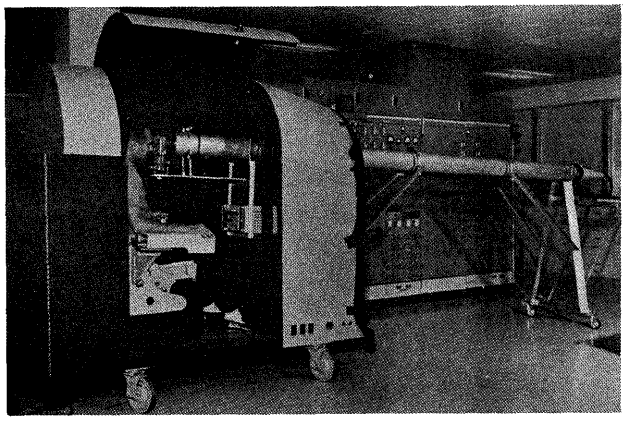


Figure 8. General view of tracking task simulator equipment.

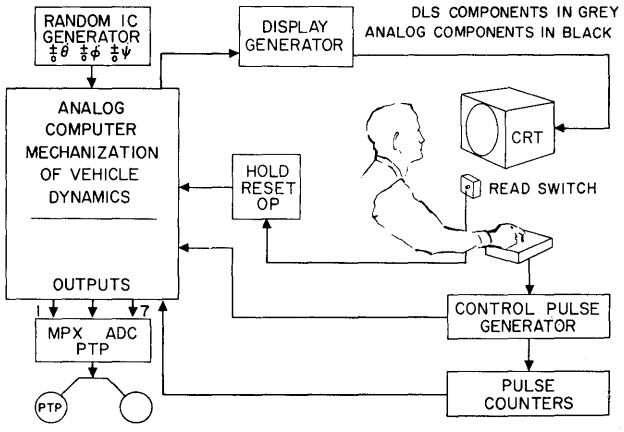


Figure 9. Block diagram of tracking task simulator showing digital logic simulator functions.

4. Randomly select ± zero reference independently for three integrator IC potentiometers

5. Generate the oscilloscope display pattern from analog computer outputs

6. Record all data output channels on punched paper tape.

In the operation of the simulator, random rotational inputs are applied to the problem and the pilot steers the tracking display by using a standard bang-bang controller. Upon superposition of the target dots, the pilot actuates the "Read" switch, which is the basic control input to the DLS, and the following sequence then occurs:

1. DLS places analog in hold

2. DLS reads out seven end-point quantities by actuating the MPX-ADC paper-tape-punch recording system

3. DLS places analog in IC

4. DLS sets three new IC conditions

5. DLS waits 0.5 second for IC charging time

6. DLS places analog in operate and

   a. Generates display to pilot

   b. Generates control pulses

   c. Accumulates control pulses

Of particular interest in this problem was the employment of the high-speed paper-tape-punch input-output (I/O) unit instead of the standard ADIOS* typewriter readout(2). Readout of seven quantities on the EAI ADIOS analog printout system took a minimum of 21 seconds, and additional readout points were essentially limited by this slow speed. Since hundreds of such runs are necessary, this waiting period amounts to hours of idle computer and pilot time. The DLS conversion and punch equipment was employed as shown in figure 10. The converted values are transferred in character groups of four bits to the punch drivers in parallel. It takes 3 lines of punching to represent a 12-bit binary word and one line for the sign. A fifth line is used for indexing. The maximum speed of the readout is, therefore, 22 binary words per second as the punch has a 110 character per second punching rate. The ADC, at 4,000 words/sec., presents no limit whatever to the output rate.

The time required for recording the necessary output data, placing new IC's on the analog, resetting, and putting into operate is 0.8 second as

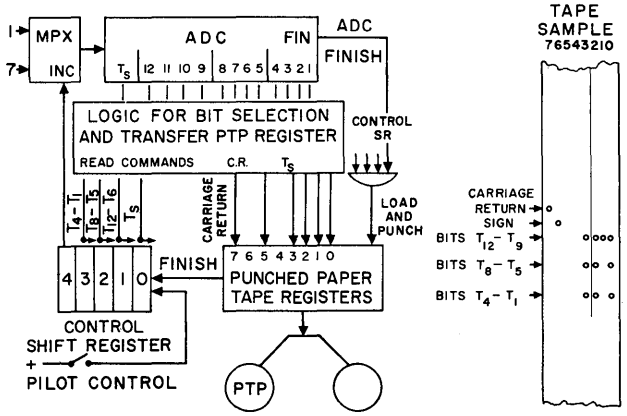


Figure 10. Simplified diagram of digital logic simulator program for output of analog data and sample tape format.

*Trade Mark, EAI

compared to 21 seconds of the ADIOS — a substantial improvement. In fact, for a human-operated device like this, it is too fast and some additional waiting time for human recovery has to be introduced. The interval of 0.8 second between repetitions of the task is just about long enough to push the read button and blink before a completely new run has begun.

After a series of runs is completed, paper tapes are taken to the data processing laboratory for immediate processing and storage on magnetic tape. When sufficient runs for statistical evaluation are completed, the standard digital data processors can compute any desired functions or otherwise service the data. This method of taking data represents a major saving in technical manpower in running this type of program, and makes analog-computed results instantly available to powerful digital computer analysis.

The DLS portion of the problem uses the following components:

42 flip-flops

108 AND gates

30 D/A switches

6 GC upcounters

9 PC downcounters

3 shift registers

7 comparators

1 MPX, ADC, PTP

2 DAC's

One of the principal reasons for including digital word units in the DLS was to provide the capability of simulating transport delays. Analog methods for approximating delays, such as the Padé approximation, require a large number of analog components for any reasonably accurate approximation. Digital methods for generating delays hold the promise of providing more accurate and more versatile delay approximations. For example, variable time delays are easily generated by digital methods but, for practical purposes, are impossible by analog methods. The basic scheme for generation of time delay using digital elements is illustrated in figure 11. The analog signal is periodically converted to digital numbers by the

ADC and these numbers are stored in a serial memory line. The sampling frequency is so chosen that when the memory line is just filled to overflowing, the oldest word enters the DAC at the required delay interval. The example shown in the figure uses a 256-word storage memory line and the desired delay is 2.5 seconds, which requires a 102.4-words-per-second sample of the analog input. From the sampling theorem, one can estimate upper frequency bounds of this delay. Conservatively, variables of up to 10 cps in frequency could be delayed accurately by this example. Low pass filtering of the analog input also should be included to prevent frequency folding errors[3].

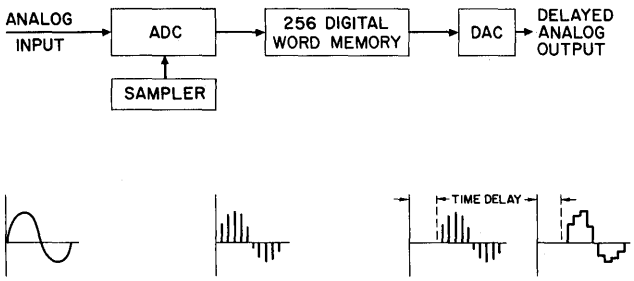
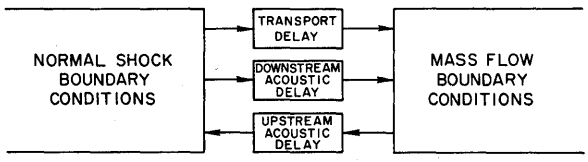


Figure 11. Basic digital logic simulator system for time delay simulation.

The first delay simulation using DLS components has been implemented at the Center, and some discussion of the preliminary experience using digital storage methods seems appropriate since it became much more involved than was originally expected.

The basic problem involved the simulation of a jet engine control system for a supersonic airplane, shown in figure 12. The transport delays between the engine inlet and exit of the aerodynamic shock of the disturbances were mechanized by using available DLS components of figures 3 and 4. The required delays were in the time scale of the problem ... 2.5, 1.67, and 0.714 seconds, respectively. Available delay lines are 256 (SM8), 64 (SM6) and 16 (SM4) words long. Noting that sampling rate is the ratio of line length to delay required, the chart of figure 12 shows the required sampling periods. These sampling frequencies are, unfortunately, unrelated harmonically. Because there are three simultaneous delay channels in operation but only one ADC in the analog realm, data skewing results and accurate sampling became very difficult to achieve even if a random access MPX and sample hold inputs were available. These latter components were not available, so an alternate scheme of sampling in the digital realm was devised. Illustrated in figure 13, the method uses the maximum updating rate of the MPX-ADC combination into 3 one-word MB units. Each signal is sampled 1,300 times/second and the MB is constantly supplied with new data. The digital sampling for the delay of each channel is effected by ANDing a "sample" signal with the MB output. Simultaneously with inputting the delay line, the proper word must be transmitted to the waiting DAC. If the proper word is not in the output position, however, the transfer process must be delayed until the memory circulates the desired word to the output position. This length of time varies depending on the memory access time. In the SM8, the access time is 2 milliseconds. This becomes the maximum holding time before the sampler can enter information into memory, but the average will be substantially less than 2 milliseconds. Notice, though, the updating of the MB continues so that when the appropriate transfer time does occur, later information has been put into the MB by the ADC-MPX combination. The effect on the word in the line is always to delay it somewhat. It is believed that the errors introduced by these delays are small compared to other system inaccuracies. However, problems of programming useful transport delays on digital equipment have been glossed over and considerable investigation is needed to find a program with maximum accuracy and minimum components for multiple channel delays. Such efforts are under way at this Center. Further, a substantial improvement in the programming methods for digital word components is required.



$$\text{SAMPLING RATE} = \frac{\text{LINE LENGTH}}{\text{DELAY REQ}}$$

DELAY CHANNEL	DELAY, sec	DELAY LINE	SAMPLE RATE, S/sec	SAMPLE INTERVAL, msec	DELAY LINE ACCESS TIME, msec
1	2.5	256	102.4	9.76	1.953
2	1.67	256	153.6	6.51	.488
3	.714	64	89.6	11.16	.122

Figure 12. Simplified block diagram of supersonic engine simulation using digital logic simulator delay program.

THE AMES LINKAGE SYSTEM

At Ames Research Center there is a variety of simulators for studying space flight and atmospheric reentry of manned vehicles. For a simulation, it is necessary to compute so many widely

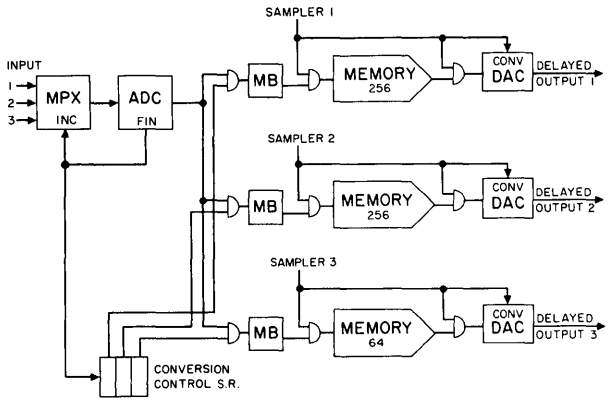


Figure 13. Program to introduce time delay in three analog signals using digital logic simulator techniques.

varying quantities that it is extremely difficult to use analog computers exclusively. Existing digital machines, though, do not have the dynamic response necessary for the real-time solution of descents into the atmosphere. Since the analog has the necessary dynamic response and the digital has the necessary dynamic range, however, the two machines used together can reproduce satisfactorily the flight characteristics of reentry vehicles. Moreover, the digital is required for the accurate solution of space vehicle displacement equations, and can directly reproduce the functions of the complex on-board digital computers presently proposed for future spacecraft. For these reasons, Ames Research Center undertook to provide a link between its extensive analog facilities and its modern digital facility to provide a combined computational facility that could reproduce satisfactorily the flight equations of space vehicles on a real-time basis.

Several successful linkage systems have been previously described[4,5] and many characteristics of these systems are shared by the Ames linkage. Therefore, only those features which make the Ames system unique and which present unusual design problems will be discussed.

Three major factors shaped the design of the linkage:

1. The physical separation of the analog and digital facilities.

2. The requirement for authentic reproduction of data display, data input and pilot input functions of a space vehicle.

3. The necessity for conservation of digital computer time for economic reasons.

Figure 1 shows the physical separation of the two computer facilities. The analog computer, the analog-digital and digital-analog converters, control equipment and the manned simulation machine are located in the building in the upper right-hand portion of the figure, and the digital facilities in the building at the lower left-hand portion of the figure. The crucial problem initially was whether or not the two computers could be successfully interconnected (an EAI PACE® 231-R analog computer and an IBM 7090 digital computer) over this one-half mile distance. Several transmission media, such as microwave radio, telemetry, etc., were examined for the communication link as was the form in which the data could be transmitted, that is, digital or analog, serial or parallel transmission. Digital signal transmission appeared the most desirable method of communication from the outset because of the large requirement for digital data displays in the simulator, but whether transmission of satisfactory digital wave shapes over this distance could be achieved was of paramount importance to the system design.

The oscillogram of figure 14 shows the results of a test, run by Packard Bell Computer Corporation, to show the electrical performance of a wire transmission system. The system requires special line drivers and line receivers to overcome the load and distortion effects of the 2500-foot cable on digital wave shapes. The distortion and successful recovery of the digital signals can be observed in the figure. The 5 μ sec delay shown by the oscillogram is introduced by the line length and the velocity-of-propagation characteristics of the transmission cable. The maximum rate at which data, in 2 μ sec pulses, are transmitted by an individual line is in excess of 100kc. A serial data transmission link between the computers, in the form of a single wire line for each direction, was considered, but was rejected for both economic and technical reasons. Serial transmission requires extremely high data rates and greatly complicates the logical design of the linkage, making it more expensive than parallel transmission which requires many lines but less logic. The design

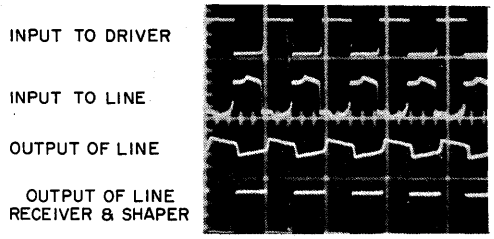


Figure 14. Oscillograph of 2500-foot transmission system performance.

selected was that of parallel digital transmission by wire cable. The white line shows the 2500-foot path of the underground conduit containing the 73 coaxial transmission lines that make the parallel digital signal connections between the two computers. The 73 lines permit parallel 16-bit-plus-sign data-word and parallel 10-bit sense-word communication in both directions simultaneously. RG 62 A/U cable was used — each line being individually manufactured 2500 feet long so that no intermediate connectors are required. Operational experience with this digital transmission link has been very satisfactory, with millions of words having been transmitted error-free in both directions.

The requirement for authentic reproduction of data display, data input, and pilot controls required communication between the simulator cockpit and the digital computer far in excess of that required by just the linkage of the two computers. The simulator cockpit displays and controls are shown in figure 15. The upper left panel is the mission time clock, which provides the basic time reference for the simulation. As shown in figure 16, the clock informs the digital computer of the length of time since the last operate period. This is necessary for the navigation phase during which the digital computer is on line only briefly at 15 minute intervals. Therefore, problem timing must be independent of the digital computer. The keyboard in the lower right-hand panel is the pilot's data input to the digital computer. As the pilot actuates the keyboard, the input appears on the computer check display panel in the upper center of figure 15 for his verification. The pilot input and the mission time do not actually enter the digital computer until the proper signals appear at

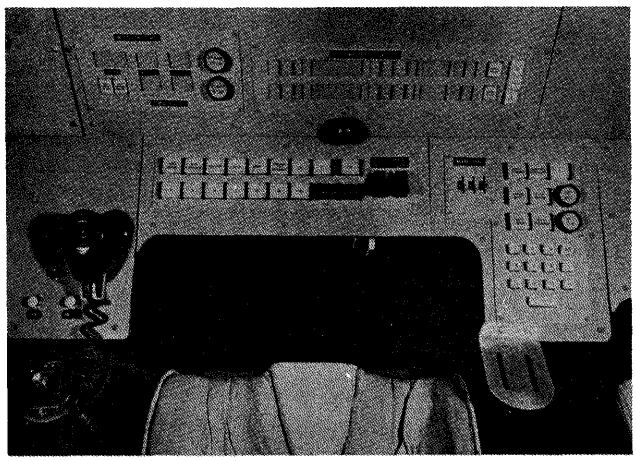


Figure 15. Interior view of simulated space vehicle showing the display and control panels.

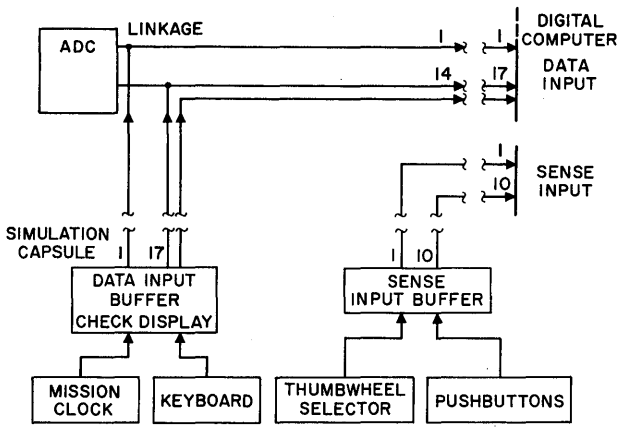


Figure 16. Information flow from capsule to digital computer.

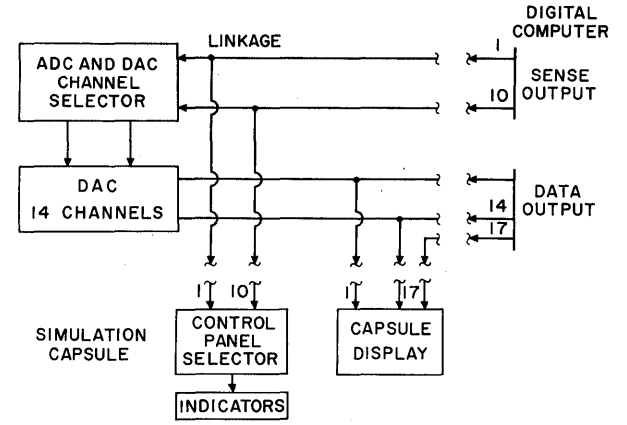


Figure 17. Information flow from digital computer to capsule.

the sense input terminals of the computer to identify the data. As shown in figure 15, sense inputs come from the large pushbuttons or thumbwheel switches, and represent command inputs to the digital computer. When the data do enter the digital computer, they are repeated to the second check display via the output data lines of figure 17 so that the pilot can verify his own input to the computer. In a like manner, the sense codes return signals on the output sense lines to actuate pushbutton indicator lamps, showing that the proper command has been received. The check and mission time displays are eight-element electroluminescent display wafers. The pushbuttons are standard computer hardware. All these signals are transmitted over the one-half mile of the parallel digital transmission system.

The pilot flight controls, not shown in figure 15, are normally mounted on the slotted bracket on the right. Any such controller feeds inputs to the analog computer section, as will be discussed later.

Figure 18 is a simplified block diagram of the signal paths between the computers. The conversion components of the linkage are the multiplexer (MPX), analog-to-digital converter (ADC), and the digital-to-analog converter (DAC). These are all conventional items of the 15kc, 13-bit-plus-sign class and do not need any explanation[6,7,8]. The sense output lines of the digital machine direct the selection of the DAC channels under the control of the digital program. Figures 16 and 17 also show this information path between the computer. Notice that only 14 lines are required to carry the digitized analog signals, but the pilot's manual data require a total of 17 lines.

The introduction of a linkage system into a digital facility to connect a large flight simulator with its myriads of people, problems, and delays is viewed with justifiable apprehension by those responsible for effective utilization of the digital equipment. Therefore, considerable effort has been expended to develop an efficient method of satisfying the simulator demands with only a minimum of interruption of the normal digital production demands. A digital computer program, called a data acceptance routine (DAR), has been devised and implemented. The DAR virtually eliminates the computer's standing idle for changes between production and simulation computations.

Figure 19 is a flow diagram of the DAR. To understand the diagram properly, two operating situations must be pointed out:

1. The data acceptance routine is stored permanently in the computer memory.

2. The simulation program magnetic tapes must be placed on the tape handling equipment of the digital computer.

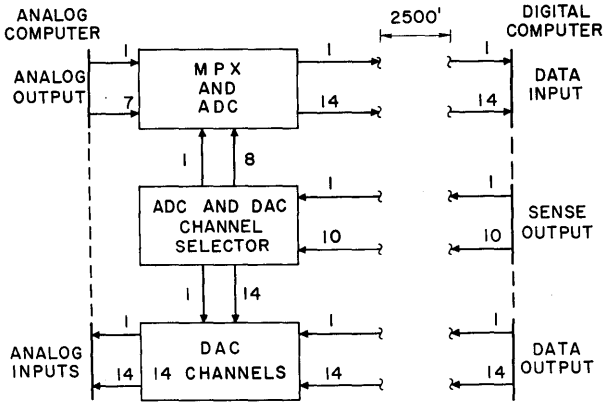


Figure 18. Signal linkage between analog and digital computers.

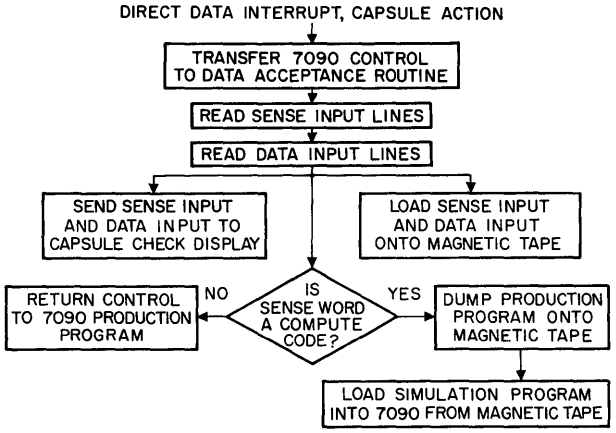


Figure 19. Flow diagram of data acceptance routine.

When the capsule generates a direct data interrupt signal (several of the large pushbuttons shown in figure 15 will generate this signal), the digital computer is halted and the data acceptance routine is entered. As illustrated in figure 19, the computer examines the previously discussed sense input and data input lines. If the sense input says the data are to be placed on the waiting simulation program tapes, it does so without disturbing the arithmetic registers of the computer which returns instantly to production operation. However, if the sense code indicates a computation is required, the production program is dumped, and the simulation program is loaded. The program computes, new data are transmitted to the capsule, and the production program is returned. Changeover time using the DAR is approximately 10 seconds.

The changeover capability is essential during the space flight phase of a simulated mission, since, as mentioned previously, only momentary operation every 15 minutes is required (although the mission can continue for several days). During the reentry phase, the combined computer system is required continuously for about 15 minutes to compute the rapidly changing flight conditions in the earth's atmosphere.

Figure 20 is a flow diagram of the computer operation for the reentry phase. The simulation program is loaded into the digital computer as a standard production program. The operator actuates the initial condition pushbutton and the digital sends the initial condition values to the analog and returns automatically to production work. After the checkout of the simulator is completed, the simulation must be reinstated, by production methods, into the digital computer. The operate cycle then commences, as shown on the chart, and continues until either the initial condition or halt pushbutton is

actuated, automatically exiting the simulation program and entering a production program into the computer. While a detailed discussion of the reentry mechanization is beyond the scope of this paper, a brief discussion is of interest.

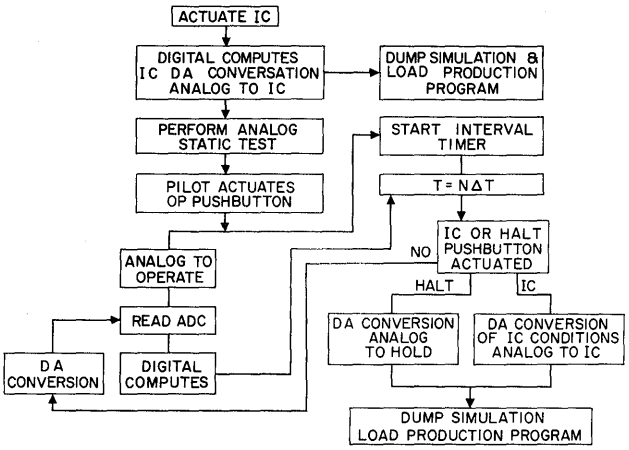


Figure 20. Flow diagram of reentry phase program.

The system of equations employed in this reentry phase is that devised by Fogarty and Howe of the University of Michigan[9]. This system, called the modified flight path axis system, introduces several special axis frames, two of which need explanation for this discussion. These two frames are called the E frame and H frame.

The origin of the E frame is at the center of gravity of the vehicle; the vector components point north, east, and down. The H frame differs from the E frame by the heading angle of the vehicle velocity vector. The analog computer receives the standard pilot inputs, calculates the aerodynamic and jet reaction forces in the body axis frame, and transforms these forces into the E frame. The E frame forces are then digitized and serve as inputs to the digital computer. The digital computer transforms E frame forces into H frame forces; calculates H frame and E frame velocities; calculates latitude, longitude, and altitude of the vehicle; and calculates dynamic pressure and Mach number. These values serve as outputs from the digital to the analog computer. The analog computer computes the standard body axis rotational equations, the conventional Euler angles, and the direction cosines[10]. With the digital computer programmed in Fortran, each computational cycle requires approximately 125 milliseconds if a parabolic integration routine is used to integrate the forces and velocities.

CONCLUSION

Two major hybrid computer systems have been described briefly, emphasizing those features which make them extremely valuable in the general field of research flight simulators.

The digital logic simulator represents a new computer concept in this Center. The machine has found widespread use in the simulation laboratory basically because of its general purpose design. The applications discussed have been selected to highlight the unique capabilities of this type of equipment in hybrid computation.

The Ames linkage system, on the other hand, while following the familiar "slender coupling"[11] design concept, has connected two remote computers together successfully in a simulation application. This, combined with extensive remote readout and control, and the unique data acceptance routine, makes elaborate space vehicle flight simulation possible at the Center. The use of the linkage in the reentry phase has been discussed.

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10. Ibid. p. 25.

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