SC31/BX

(RM02/RM03/RM05/RM80, RP06 COMPATIBLE)

DISK CONTROLLER

TECHNICAL MANUAL

EMULEX

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1.1 SCOPE

This manual provides information related to the capabilities, design, installation, and use of the SC31/BX Disk Controllers. In addition, this manual provides diagnostic and application information.

1.2 OVERVIEW

The SC31/BX Disk Controller is a one-board embedded controller for PDP-11 and VAX-11 computers manufactured by Digital Equipment Corporation (DEC). This controller can be used to interface any large disk having a Storage Module Drive (SMD) interface. The SC31/BX series of controllers is capable of emulating the DEC RJM02/05, RM80 and RJP06 Massbus disk subsystems. This controller is capable of operating with disk drives having different characteristics from those used in the DEC disk subsystems. The SC31/BX controller provides the capability of operating with a mixture of disks having storage capacities ranging from five to 600 megabytes.

1.3 FEATURES

Features that enhance performance and increase versatility are described in the following paragraphs. Table 1-1 lists and describes specifications for the SC31/BX Disk Controller.

1.3.1 Microprocessor Design

The SC31/BX design incorporates a unique (patent pending) 16-bit bipolar microprocessor to perform all controller functions. The microprocessor approach provides for a reduced component count, high reliability, easy maintainability, and most importantly, the ability to adapt a single set of hardware to a wide range of emulation capabilities through the use of microprogramming. The Emulex controllers achieve functional capability beyond that of the DEC controllers they emulate, by providing enhancement features such as built-in self-test during power-up, built-in disk formatting and the ability to work with disk drives of various capacities.

1.3.2 Packaging

The SC31/BX is constructed on a single hex-size multi-layer printed circuit board assembly (PCBA) which plugs directly into the PDP-11 or VAX-11 chassis, or an expansion chassis. No cabling is required between the computer and the disk controller. The controller obtains its power from the chassis in which it is mounted.

1.3.3 Self-Test

The controller incorporates an internal self-test routine which is executed upon power-up. This test exercises all parts of the microprocessor, buffer and disk data logic. Although this test does not completely test all controller circuitry, successful execution indicates a very high probability that the controller is operational. If the controller fails the self-test, it leaves the Fault LED ON and the controller cannot be addressed from the central processing unit (CPU).

1.3.4 Buffering

The controller contains a 4K x 16 bit high-speed random access memory (RAM) buffer used to store the device registers of the controller and drive being emulated plus fourteen sectors of data buffering. Because of the buffering and the strategies used to employ it, data late situations on the Unibus are not possible.

1.3.5 Error Correction

The controller incorporates a 32-bit error correcting code (ECC) capable of correcting single error bursts of up to 11 bits in length and detecting bursts of longer length. The controller determines the location of the error and the error pattern and passes this information to the PDP-11 which performs the actual correction. A 16-bit CRC is employed with the header of every sector.

1.3.6 Option and Configuration Switches

Two ten-pole and one four-pole DIP switches are used to configure the controller for various disk capacities, Unibus addresses and certain firmware options. It is possible to select one of several possible combinations of disk characteristics for the four drives which can be handled by the controller, including a mixture of disk sizes and drive type codes.

1.3.7 Dual Port Capability

The controller can operate with disk drives having dual port capability; therefore a second controller can have access to the drive on a priority basis.

1.3.8 Dual Access Capability

To provide compatibility with dual access drivers when configured for dual access, the Dual Access mode is provided. When in this mode, the controller sets DPM in the Drive Type Register and PGM in the Drive Status Register to imitate the DEC neutral state.

1.4 FUNCTIONAL COMPATIBILITY

1.4.1 Media Compatibility

The SC31/BX is media compatible with DEC RM02/RM03 packs when using a CDC 9762 drive or equivalent, and with DEC RM05 packs when using a CDC 9766 drive or equivalent.

1.4.2 Disk Mapping

Depending upon the type and capacity of the disk drive, one or two logical units may be mapped on it. Various mapping organizations are used; some do not leave direct 1:1 correlation between the logical and physical addresses.

1.4.3 Diagnostics

The controller executes the following standard DEC RM02/RM03 and DEC RP06 diagnostics:

```
ZRMA  -  Formatter
ZRMB  -  Performance Exerciser
ZRMC  -  Functional Controller, Part I*
ZRMD  -  Functional Controller, Part II*
ZRME  -  Functional Controller, Part III*
ZRMF  -  Extended Drive Test
ZRMI  -  Drive Compatibility Test

ZRJA  -  Mechanical and Read Write Test
ZRJB  -  Formatter
ZRJD  -  Multi-Drive Exerciser
ZRJG  -  Diskless Controller Test - Part 1 *
ZRJH  -  Diskless Controller Test - Part 2 *
ZRJI  -  Functional Controller Test - Part 1 *
ZRJJ  -  Functional Controller Test - Part 2 *
```

The diagnostics marked with an asterisk require certain patches to correct coding problems or to bypass unsupported maintenance functions. All diagnostics require patches to run with drive capacities other than that of a standard RM02/RM03 or RP06. In addition, the ZRMB Performance Exerciser will not run on any drive with more than 16 bad sectors.

Emulex has available self-sizing RM diagnostics which have all the required patches, will work on any size drive and can handle 126 bad sectors.

1.4.4 Operating Systems

The SC31/BX controller is compatible with DEC operating systems without modification when emulating any standard DEC disk subsystem. Patches to the operating system are required when operating with other than standard size disks. These patches

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numerically redefine the logical drive capacity to the operating system and generally do not involve modification to program instructions.

The RM02/03/05/80 and RP06 disk drives are not supported by all DEC operating systems, in particular, RT11.

Table 1-1

GENERAL SPECIFICATIONS

Functional

Emulation	DEC RM02/03/05/80, RP04/05/06
Media Compatibility	DEC RM02/03/05 with appropriate disk drives
Drive Interface	SMD
Drive Ports	4
Error Control	32-bit ECC for data and 16-bit CRC for headers. Correction of single error burst of up to 11 bits.
Sector Size	256 words (512 bytes)
Sectors/Track	Selectable for each drive
Tracks/Cylinder	Selectable for each drive
Cylinders/Drive	Selectable for each drive
Drive Type Code	Selectable for each drive
Computer Interface	SPC Unibus
Unibus Address Standard Alternates	776700 (20 Registers) 776300 (20 Registers) 776400 (20 Registers) 776600 (20 Registers)
Vector Address Standard Alternates	254 150, 370, 374, 354, 224, 270, 274
Priority Level	BR5
Data Bufferring	14 full sectors
Data Transfer	High speed NPR operation
Maximum Disk Data Rate	16 MHz (2 MBytes/second)

Table 1-1 (cont'd)

Self-Test	Extensive internal self-test on powering up
Indicators	Activity and Fault LEDs
Design	High-speed bipolar microprocessor using 2901 bit-slice components.
Physical	
Packaging	One DEC hex-size PCBA
Mounting	Any SPC slot in CPU or expansion box
Connectors	One 60-pin A Cable connector and four 26-pin B Cable connectors (Flat cable types)
Electrical	
Unibus Interface	DEC approved line drivers and receivers.
Drive Interfaces	Differential line drivers and receivers. A Cable cumulative length to 100 feet, B Cable length to 50 feet.
Power	+5 V, 8 A maximum -15 V, 1 A maximum

2.1 CONTROLLER ORGANIZATION

A block diagram showing the major functional elements of the SC31/BX controller is shown in Figure 2-1. The controller is organized around a 16-bit, high-speed bipolar microprocessor. The arithmetic and logic unit (ALU) and register file portion of the microprocessor are implemented with four, 2901 bit-slice components. The microinstruction is 48 bits in length and the control memory of 4K words is implemented with six 4K x 8 bit PROMs.

The controller incorporates a 4K x 16 bit high-speed RAM buffer which is used to store the controller's device registers plus fourteen sectors (3584 words) of data buffering.

The A Cable Register (ACR) provides the storage of all A Cable signals going to the disk drives. The inputs from the selected drive are testable by the microprocessor.

Serial data from the drive is converted into 16-bit parallel data and transferred to the buffer via the microprocessor. Likewise, the data accessed from the buffer by the microprocessor is serialized and sent to the drive under the control of the servo clock received from the drive. A 32-bit ECC shift register is used to generate and check the ECC for the data field. The same register is also used in a 16-bit CRC mode for the headers. The actual ECC polynomial operation is done independently of the microprocessor, but determination of the error position and error pattern is done under the control of the microprocessor.

The Unibus interface consists of a 16-bit bi-directional set of data lines and an 18-bit set of address lines. The Unibus interface is used for programmed input/output (I/O), CPU interrupts, and data transfers. The microprocessor responds to all programmed I/O and carries out the I/O functions required for the addressed controller register. The microprocessor also controls all NPR operations and transfers data between the Unibus data lines and the buffer.

2.2 PHYSICAL DESCRIPTION

The SC31/BX controller consists of a single hex-size PCBA which plugs directly into a PDP-11 chassis, or an expansion chassis. Figure 2-2 shows the PCBA.
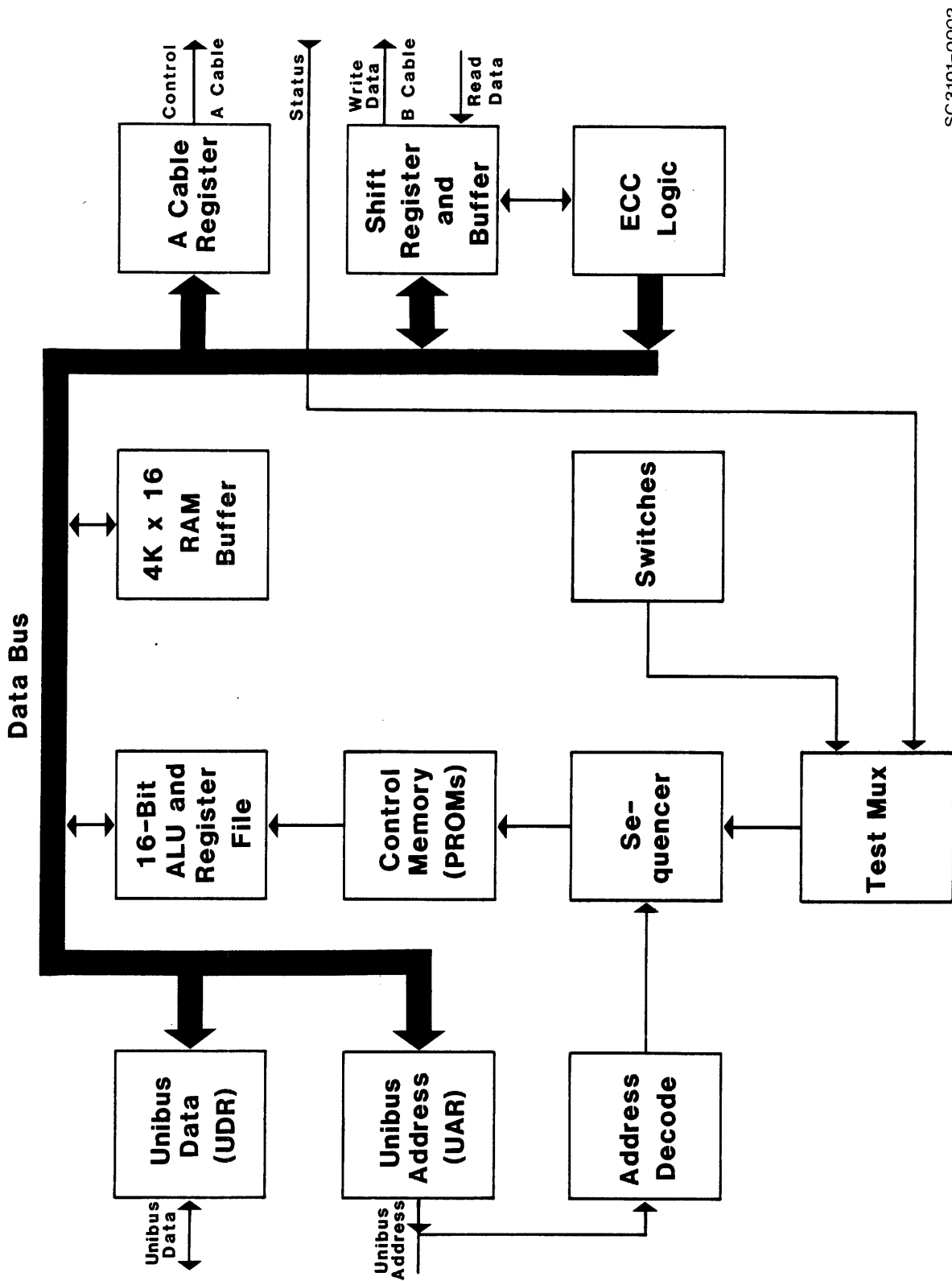
Figure 2-1 SC31 Block Diagram
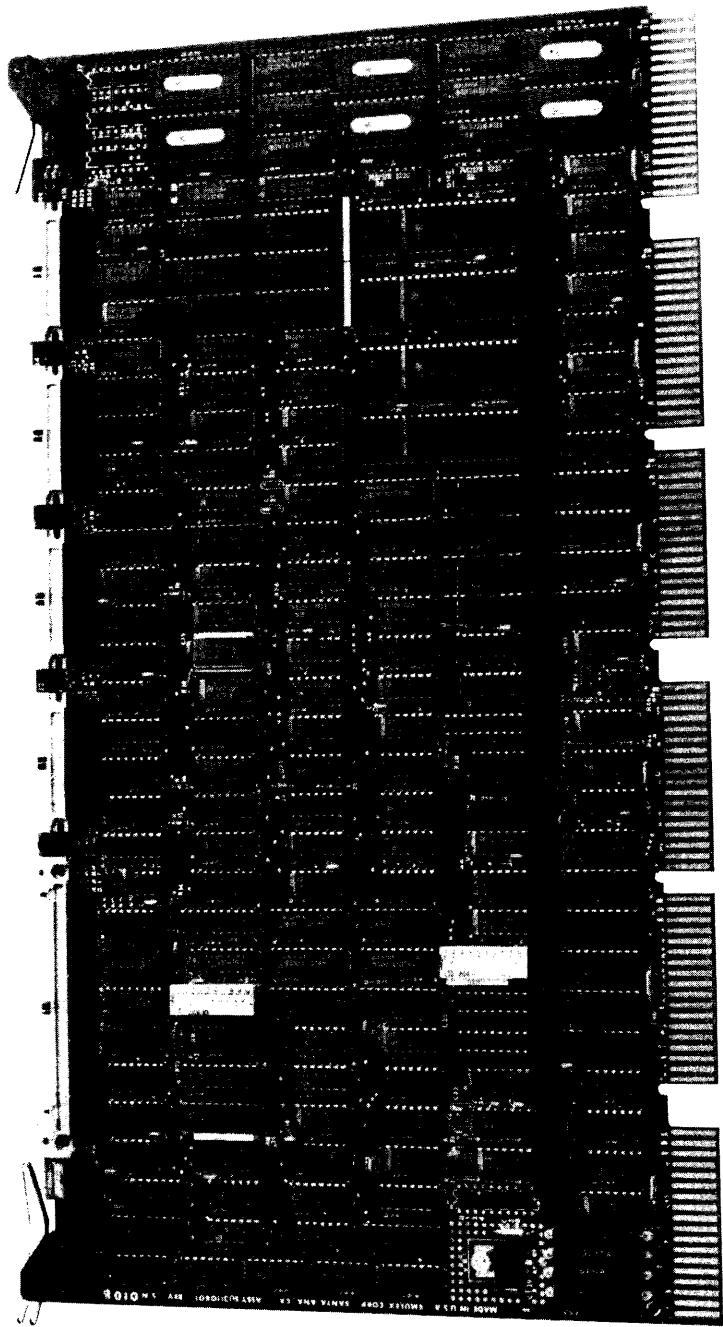
SC3101-0003

Figure 2-2   SC31 Controller Board

2.2.1 Connectors

2.2.1.1 A Cable Connector

The 60-pin flat cable connector labeled J1 at the top edge of the board is for the A Cable which daisy-chains to all the drives for control and status. Pin 1 is located on the left side of the connector.

2.2.1.2 B Cable Connector

The four 26-pin flat cable connectors labeled J2, J3, J4, and J5 are for the radial B Cables to each of four physical drives which may be attached to the controller. Pin 1 is located on the left side of the connector. The four B Cable ports are all identical and any drive may be plugged into any connector.

2.2.1.3 Test Connectors

Connectors J6 and J7 are used with the Emulex test panel during manufacturing test and factory repair. They have no use in normal operation.

2.2.2 Switches

The two ten-pole and one four-pole DIP switches labeled SW1, SW2 and SW3 are used to configure the controller. SW1 and SW2 provide firmware options, while SW3 provides selection of controller address and drive configurations.

2.2.3 Indicators

There are two LED indicators mounted between the connectors at the top of the board. They have the following use:

    Fault   -   Indicates unsuccessful self-test execution. A
                     flashing LED indicates successful self-test, but
                     unable to find any drive connected and/or
                     powered-up.

    Activity -   Indicates activity of disk Read or Write
                     operation.

2.2.4 PROMs

There are six PROM sockets, used for the control memory, located along the right edge of the board. The sockets are labeled PROM 0 through PROM 5 in a discontinuous physical order. The numbers on the top of the PROM ICs are Emulex part numbers which identify the unique pattern of the PROM. When inserting PROMs in the board, the ID numbers are placed in the same sequence as the PROM numbers on the board beside each socket. In addition, there are three PROM sockets in the lower left portion of the board. The PROM at U128

is the Drive Configuration PROM. The PROM at U129 is the Address Decode PROM. The PROM at U135 is the Buffer Address Auto Increment PROM.

2.3 INTERFACES

2.3.1 Disk Interface

The controller's disk interface conforms to the Flat Cable Interface Specification for the SMD, MMD, and CMD (CDC Document No. 64712400). The controller has been tested with most drives using the SMD interface and is compatible with the electrical and timing characteristics of such disk drives.

The following paragraphs define the electrical interface and the recommended cables.

2.3.1.1 Drivers and Receivers

The drivers for the A and B Cables are MC3453, which are equivalent to 75110A drivers. The receivers are MC3450 quad differential receivers, which are equivalent to 75108 receivers. The lines of the A Cable are terminated with 82 ohms to ground. The lines of the B Cable are terminated with 56 ohms to ground.

2.3.1.2 A Cable

The 60-conductor A Cable is daisy-chained to all disk drives and terminated at the last drive. The signals in this cable, along with their function when the control tag (Tag 3) is asserted, are listed in Table 2-1. The A Cable should be a 30 twisted pair flat cable with an impedance of 100 ohms and a cumulative length not greater than 100 feet.

2.3.1.3 B Cable

The 26-conductor B Cable is radial to all drives and contains the data and clock signals. The signals and grounds in this cable are listed in Table 2-1. The B Cable should be a 26-conductor flat cable with ground plane and drain wire. The impedance should be 130 ohms and the length not greater than 50 feet.

2.3.2 Unibus Interface

The controller interfaces to the Unibus via a Small Peripheral Controller (SPC) connector. The Unibus consists of 18 address lines and 16 bi-directional data lines, plus control signals for data and interrupt vector address transfer and for becoming bus master. The signal connections of the controller to the Unibus are shown in Table 2-2.

Table 2-1
Disk Drive Connections

Pins Lo/Hi	Signal	(Tag 3 Function)	From/To
A Cable:			
22,52	Unit Select Tag		To
23,53	Unit Select bit 0		To
24,54	Unit Select bit 1		To
26,56	Unit Select bit 2		To
27,57	Unit Select bit 3		To
1,31	Tag 1		To
2,32	Tag 2		To
3,33	Tag 3		To
4,34	Bit 0	(Write Gate)	To
5,35	Bit 1	(Read Gate)	To
6,36	Bit 2	(Servo Offset Plus)	To
7,37	Bit 3	(Servo Offset Minus)	To
8,38	Bit 4	(Fault Clear)	To
9,39	Bit 5	(AM Enable)	To
10,40	Bit 6	(Return to Zero)	To
11,41	Bit 7	(Data Strobe Early)	To
12,42	Bit 8	(Data Strobe Late)	To
13,43	Bit 9	(Release)	To
30,60	Bit 10		To
14,44	Open Cable Detect		To
15,45	Fault		From
16,46	Seek Error		From
17,47	On Cylinder		From
18,48	Index		From
19,49	Unit Ready		From
20,50	Address Mark Found		From
21,51	Busy (dual port only)		From
25,55	Sector		From
28,58	Write Protected		From
29	Power Sequence Hold		To
59	Power Sequence Pick		To
B Cable:			
8,20	Write Data		To
6,19	Write Clock		To
2,14	Servo Clock		From
3,16	Read Data		From
5,17	Read Clock		From
10,23	Seek End		From
22,9	Unit Selected		From
12,24	Index		From
13,26	Sector		From

Table 2-2
SPC Unibus Connections

Column	C		D		E		F	
Pin	1	2	1	2	1	2	1	2
A	NPGIN	+5V		+5V		+5V		+5V
B	NPGOUT					−15V		−15V
C	PA	GND		GND	A12	GND		GND
D		D15		BR7	A17	A15	BBSY	
E		D14		BR6	MSYN	A16		
F		D13		BR5	A02	C1		
H	D11	D12		BR4	A01	A00		
J		D10			SSYN	C0	NPR	
K		D09		BG7IN	A14	A13		
L		D08	INIT	BG7OUT	A11			
M		D07		BG6IN			INTR	
N	DCLO	D04		BG6OUT		A08		
P		D05		BG5IN	A10	A07		
R		D01		BG5OUT	A09			
S	PB	D00		BG4IN				
T	GND	D03	GND	BG4OUT	GND		GND	SACK
U		D02			A06	A04		
V	ACLO	D06			A05	A03		

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2.3.2.1 BR (Interrupt) Priority Level

The controller is hardwired for BR5. The other three Bus Grant signals are jumpered through.

2.3.2.2 Register Address

The controller's block of register addresses is decoded by a 2K X 4 bit PROM, located at U129. The specific address range is determined by configuration switch SW2 as discussed in paragraph 3.4.1.

2.3.2.3 DCLO and INIT Signals

The DCLO and INIT signals both perform a Controller Clear. The self-test is performed only if DCLO has been asserted.

2.4 DISK FORMAT

2.4.1 Disk Organization

The formatting of a disk pack and the mapping of one or two logical drives onto a physical drive varies with the drive capacity. Some of this information is supplied by the configuration PROM. The rest is computed based upon configuration PROM information.

2.4.2 Mapping

In most cases there is a 1:1 correspondence between logical and physical disk addresses. The controller has the capability to alter a logical address to a different physical address so that drives which do not match the number of tracks and cylinders of the unit being emulated may be accommodated.

Depending upon the type and capacity of the disk drive, one or two logical units may be mapped on it. The controller can handle a maximum of eight logical units distributed across a maximum of four physical drives. A logical drive may not be mapped across a physical unit boundary.

2.4.3 Sector Organization

Figure 2-3 shows the RM sector format used by the controller. With the exception of an additional two words, the RP sector format is the same. Each track of 20,160 bytes is divided into 32 sectors of 630 bytes. The four byte header is preceded by a preamble of 30 bytes ending in the sync byte and is followed by a two byte CRC. The 512 byte data field is preceded by a preamble of 20 bytes ending in the sync byte, and is followed by four bytes of ECC.

If the actual size of the useful data is less than 512 bytes, the remainder of the data field will be filled with zeros until 512 bytes have been written. During disk formatting procedures, each data track is located and recorded with header information by means

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```
------------------- Sector Length (RM)   630 Bytes -------------------

| Preamble Sync | Header CRC | Preamble Sync | Data Field | ECC | Recovery |

-----30-----    ----6-----   ------20-----   ---512----   -4-   ---58---
```
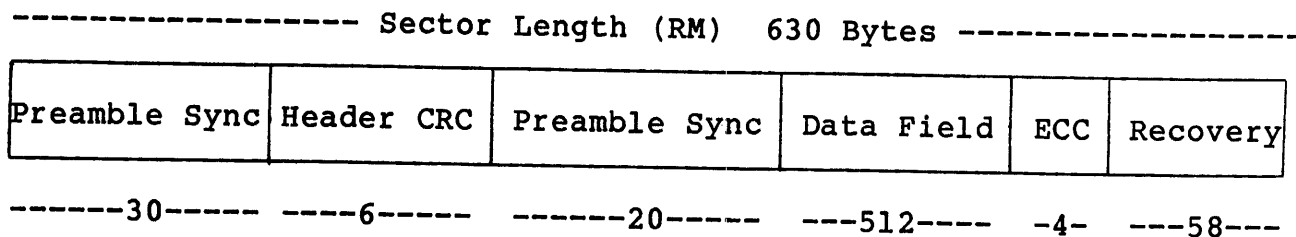
Figure 2-3   RM Sector Format

Header Word 1:

```
 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
| 1 | 1 |SSF| 1 | 0 |          Cylinder Address                   |
```

Header Word 2:

```
 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
| 0 | 0 |   Track Address    | 0   0   0 |     Sector Address     |
```

Header Word 3:

```
 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
|              Cyclic Redundancy Code (CRC)                       |
```
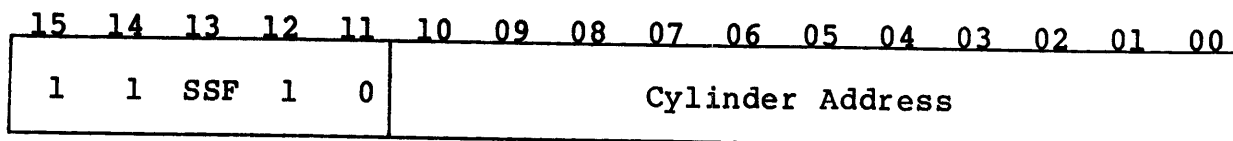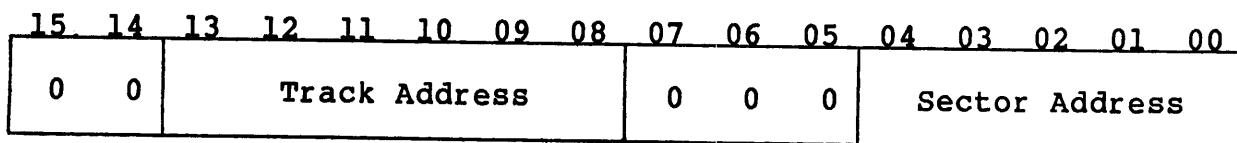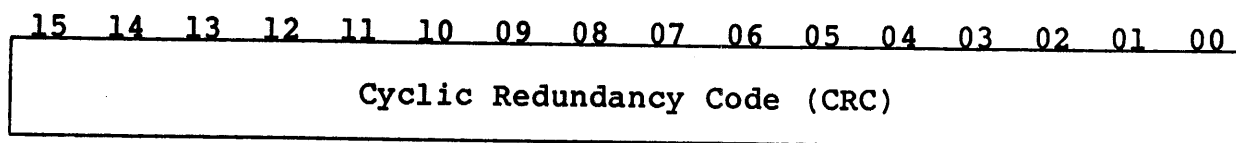
Figure 2-4   RM Header Format

of the Write Header and Data command. A disk pack should be formatted and the format verified before any real data is written on it. Once formatted, individual sectors, or groups of sectors, should not be reformatted unless absolutely necessary.

2.4.4 Header

2.4.4.1 Header Description

Figure 2-4 shows the RM header format, which consists of the following three words:

Word One -

This word contains the cylinder address. It contains a one-bit in bit 12 to identify 16-bit format to the software and one-bits in bit positions 14 and 15 to identify a good sector. For RM80 emulations, a one-bit in bit 13 indicates that the data for this sector has been relocated to the next sector.

Word Two -

The low-order byte of this word contains the sector address. Each track on the drive typically contains 32 sectors. The least significant six bits of the upper byte of this word contain the track address.

Word Three -

This is the CRC word which is generated and checked by the controller logic. This word is not available to the software.

2.4.4.2 Header Field Handling

After the drive reports that it is on cylinder, the controller locates the desired sector by means of the sector counters. A sector counter for each drive is maintained in the controller. The controller compares the first two words of the header with the desired track, sector and cylinder and then checks the CRC word for errors. An error in the header field is indicated by turning on the appropriate error bit in the error register (format error, header compare error, bad sector error, skip-sector error or CRC error). A header error is only valid when the sector count field of the RPLA/RMLA register and the sector field of the RPDA/RMDA register have already matched. It is immaterial where a CRC error occurs in the header field since the controller cannot determine its location in the field. Software may read the header to memory, however, by means of a Read Header and Data command. The header compare may be inhibited by setting the HCI bit in the RPOF/RMOF register.

2.5 GENERAL PROGRAMMING INFORMATION

2.5.1 Clearing the Controller

The controller is cleared by the following methods:

a. Controller Clear: Controller Clear is performed by writing a 1-bit into the CLR bit (bit 05 of RPCS2/RMCS2) or Unibus INIT. This causes the following registers to be cleared:

   RP Drives:

   RPCS1 bits <15:12>, <10:08>, <06:00>; RPCS2 bits <15:07>, <05:00>; RPBA bits <15:00>. Sets bit 06 of RPCS2 and bit 07 of RPCS1.

   In all RP drives: RPER1; RPER2; RPER3; RPDA; RPEC1; RPEC2; RPAS ATA bit; RPOF bits <07:00>, RPDS ATA, ERR and LST bits; RPMR bits <15:09>, <07:00>. Sets bit 08 of RPMR.

   RM Drives:

   RMCS1 bits <15:12>, <10:08>, <06:00>; RMCS2 bits <15:07>, <05:00>; RMBA bits <15:00>. Sets bit 06 of RMCS2 and bit 07 of RMCS1.

   In all RM drives: RMER1; RMER2; RMDA; RMAS ATA bit; RMEC2; RMDS ATA, ERR and LST bits; RMMR1 bits <15:04>, <02:00>. Sets bit 03 of RMMR1.

b. Error Clear: The Error Clear is performed by writing a one-bit into the TRE bit (bit 14 of RPCS1/RMCS1). This writing causes a clearing of RPCS1/RMCS1 bits 13 and 14, and bits <15:08> of RPCS2/RMCS2. RPCS1/RMCS1 SC bit (bit 15) is reset if RPAS/RMAS equals zero.

c. Drive Clear: The Drive Clear is a command. (Code 11) This command causes the following registers in the drive selected by U2-U0 to be cleared:

   RP Drives:

   ATA and ERR bits in RPDS; RPAS ATA bit; bits <15:09> and <07:00> in RPMR, bits <15:00> in RPER1, RPER2, RPER3, RPEC1, and RPEC2; and bits <07:00> in RPOF. Sets bit 08 of RPMR.

   RM Drives:

   ATA and ERR bits in RPDS; RMAS ATA bit; bits <15:04> and <02:00> in RMMR1; and bits <15:00> in RMER1, RMER2, and RMEC2. Sets bit 03 of RMMR1.

2.5.2 Interrupt Conditions

The controller generates an interrupt on the following conditions:

a. Upon termination of data transfer if interrupt enable is set when the controller becomes ready.

b. Upon assertion of attention or occurrence of a controller error (SC being set) if the controller is not busy and the interrupt enable is set.

c. When the program writes a one into IE and RDY at the same time. Note that this can be done by Read-Modify-Write instructions (BIS, BIC, etc.) which set the IE bit.

2.5.3 Termination of Data Transfers

A data transfer which has been successfully started may terminate in any of the following ways:

a. Normal Termination: Word count overflows to zero and the controller becomes ready at the end of the current sector.

b. Controller Error: An error occurs in the RPCS2/RMCS2 register bits <15:08>. Any of these errors sets TRE which terminates the data transfer immediately and makes the controller ready.

c. Drive Error: The ERR bit in the RPDS/RMDS register and at least one bit in an error register are set. TRE is also set, and the controller becomes ready. The ATA for the drive doing the data transfer becomes asserted.

d. Program-Caused Abort: By performing a Controller Clear or a RESET instruction, the program can cause an abort of any operation. Status and error information is lost when this abort is done, and both the controller and drive become ready immediately.

2.5.4 Ready Bits

RDY is the ready indicator for the controller. When RDY equals one, the controller is ready to accept a data transfer command. RDY is reset when the controller is doing a data transfer command. DRY is the ready indicator for the selected drive and is the complement of the drive's GO bit. To successfully initiate a data transfer command, both of these bits must be asserted; however, a non-data transfer command (Search, Drive Clear) may be issued to a drive at any time DRY is asserted, regardless of the state of the RDY bit.

When a Data Transfer command is successfully initiated, both RDY and DRY become negated. When a non-data transfer command is successfully initiated, only DRY becomes negated.

The assertion of RDY after the execution of a Data Transfer command does not occur until the DRY bit is set and the controller is done. RDY is asserted on the completion of the last memory cycle (or at the time of an abort condition) and the last disk transfer.

If any command other than Drive Clear is issued to a disk drive which has ERR asserted, the command is ignored by the drive. If a Data Transfer command is issued to a drive which has ERR asserted, the drive does not execute the command and the missed transfer error bit (MXF, bit 09 in RPCS2/RMCS2 register) is set.

2.6 DUAL CONTROLLER OPERATION

SMD drives may be equipped with a Dual Port option which allows two controllers (generally on separate computers) to access the drive. The SC31 controller supports this type of operation as a standard feature. Most of the dual port functions of the DEC controller being emulated are supported, and those which are not should be transparent to a properly written dual port driver.

2.6.1 Dual Port Drives

The two drive ports are known as Channel I and Channel II. Each channel has a disable switch which disables the port and prevents the computer from having access to it. Access to the drive in Dual Port operation is switched back and forth between the two controllers under program control of the two computers involved, as described in the following sections. Table 2-3 summarizes the controller's register responses in Dual Port operation.

2.6.2 Unseized State

The drive is in the unseized state when it is not connected to either controller. The CPU must issue a request for the controller to seize the drive. This request is made in one of the following ways:

a. Writing into any drive register, including read-only registers.

b. Writing a one into the drive's ATA bit in RPAS/RMAS.

2.6.3 Seized State

The drive is seized when it is logically connected to one of the controllers. At that time, the DVA (RPCS1/RMCS1, bit 11) is set, indicating that the drive is ready to communicate with the controller which has seized it. If the drive is seized by the other controller, then the DVA bit is reset, all the drive registers read as zeros and any write to a register is ignored. However, any attempt to seize a drive which is busy with the other port will cause the request to be remembered and acted upon when the drive is released by the other controller.

2.6.4 Returning to the Unseized State

The drive is released and returned to the unseized state by issuing
a release command. In addition, a one second timer in the
controller' will timeout and release the drive if one of the events
listed in section 2.6.2 for seizing the drive is not performed
periodically to keep resetting the timeout timer. Furthermore,
reading RPCS1/RMCS1 while the drive is already seized will set the
timeout timer back to one full second. Reading RPCS1/RMCS1 while
the drive is unseized will have no effect on the timer. This
allows the programmer to check the DVA bit in RPCS1/RMCS1 which, if
set, assures the programmer that his operation will complete
without timing out.

When the controller sees a previously busy drive becoming unseized,
it checks its Request flag. If the drive had been previously
requested while busy on the other port, the controller will seize
the drive, set the DVA bit and set the ATA bit which causes an
interrupt to the CPU if the IE bit is set. If the CPU does not
respond to the Attention within one second the drive will be
released, but the ATA bit remains set.

2.6.5 DEC Compatibility

The SC31/BX controller differs from the equivalent DEC controller
in three important areas. First, there is no neutral state. Since
the controller does not have instantaneous access to all drives at
the same time (a limitation of the daisy-chained A Cable and the
microprocessor organization of the controller), the controller
assumes a drive is busy on the other port if the controller has not
already seized that port. The DEC controllers can switch from
neutral to seized state within the time required to do a single
Read or Write of a drive register. In that case no ATA is set and
the drive would appear to have been already seized.

Second, the Release command is not instantaneous since the
controller takes a few microseconds to execute the command. During
this time the drive will appear to the CPU to be unseized.

Third, during a Data Transfer, the timeout timers will not operate
and the drives can not be polled to determine if they are not busy.
Therefore, no drives are seized or released during the execution of
a Data Transfer operation.

The software driver should not issue a Release command and then
attempt to save the current status of a drive, since the Release
command has a drive clear implied within it, and the reading of the
drive's registers will return all zero data. In order to allow the
other controller time to poll the drive, the CPU should not
communicate with any of the released drive's registers until
required to seize the drive again.

2.6.6 Dual Port Drives in Single Port Mode

When using an operating system which does not have dual port drive software support, it may still be advantageous to use dual port drives while operating the controller in Single Port mode. This will allow for a non-dynamic type of operation between two CPUs. In this type of operation the controller does not release the drive and, in effect, it is seized by both controllers all the time.

The one-second-timeout timer (and the Release command) operate exactly as stated in paragraph 2.6.4. Even when released, a drive will still appear to be seized to the releasing controller. The ATA bit is not set is when the other controller finds the drive not busy. Should a command be issued to a controller while a drive is busy on the other port, the controller will wait until the drive becomes unbusy before executing the command. No timer exists in this case.

This mode of operation eliminates the need for manually switching the drive from one controller to another.

2.6.7 Dual Access Mode

To provide compatibility with software configured for dual access, the Dual Access mode is supported on the SC31/BX. Register access and drive states during Dual Access mode are described in Table 2-3.

This mode is enabled by setting SW2-9 to ON (closed). When in this mode, the controller sets Dual Port Mode (Drive Type Register) and Programmable (Drive Status Register) bits to imitate the DEC neutral state.

When DPM and PGM are set, the operating system will attempt to seize a drive by simply writing a command to it. If the drive is unbusy the command is executed. The operating system will not issue a command to a drive when that drive is busy.

The operating system's choice of controller depends on whether or not a controller is currently executing a command, and what type of command it is. A controller executing a Data Transfer command can not accept another data transfer. A controller executing positioning or a housekeeping commands may be given any command for a non-busy drive.

The first time the SC31 sees a drive, it is ignored for one second. This one-second stall occurs once for each drive on the controller. It prevents the controller from seeing erroneous status information when power is applied to the drive after the controller has been powered-up. For a drive in Dual Port mode the stall will prevent the other CPU from accessing the drive until the stall completes. The Dual Access option switch bypasses the stall in all cases. For proper system operation with the Dual Access switch option ON, all

drives must have power applied before either controller is powered-up.

Setting the Dual Port Option switch overrides the Dual Access Option, except for the one-second stall override.

Table 2-3
Register Access on Dual Controller Operation

```
Controller Action              Response With Respect To Action On Ch. I
   Drive State:
-----------------------------------------------------------------------
```

Read RPCS1/RMCS1

    Drive Not Seized: Reads the controller portion of the
                                 RPCS1/RMCS1 only. The drive's portion
                                 is read as all zeros. No request flag
                                 is set.

    Drive Seized by Ch. I: DVA = 1; reads the register.

    Drive Seized by Ch. II: DVA = 0; reads all zeros for the drive's
                                 portion of the register. No flags set.

Read any other drive register

    Drive Not Seized: Reads all zeros.

    Drive Seized by Ch. I: Reads the register.

    Drive Seized by Ch. II: Reads all zeros.

Write RPCS1/RMCS1

    Drive Not Seized: The function code is attempted, and a
                                 Port Request flag is set. An OPI error
                                 usually results.

    Drive Seized by Ch. I: Loads the Function code. (Switches to
                                 unseized if the function is a Release).

    Drive Seized by Ch. II: The Function code is attempted, and a
                                 Port Request flag is set. An OPI error
                               usually results.

Write any other drive register

    Drive Not Seized: The Write is ignored, and a Port Request
                                 flag is set.

    Drive Seized by Ch. I: Loads the register.

    Drive Seized by Ch. II: The Write is ignored, and a Port Request
                                 flag is set.

```
-----------------------------------------------------------------------
```

BLANK

This section describes the step-by-step procedure for installation of the SC31/BX Disk Controller in a PDP-11 system. The following list is an outline of the procedure. Each step corresponds to a second level heading in this section (i.e., item one, Inspect the SC31/BX, is covered in paragraph 3.1).

Emulex recommends that Section 3 be read in its entirety before installation is begun.

1. Inspect the SC31/BX.

2. Prepare the disk drives.

3. Prepare the PDP-11.

4. Configure the SC31/BX.

5. Install the SC31/BX.

6. Route the drive I/O cables.

7. Test the controller.

8. Patch the operating system if required.

3.1 INSPECTION

Before unpacking the SC31/BX, examine the packaging for any signs of damage. Notify the carrier if any damage is noted.

Make a visual inspection of the board after unpacking. Check specifically for bent or broken connector pins, damaged components or any other evidence of physical damage. Examine the PROMs to ensure that they are firmly and completely seated in their sockets.

3.2 DISK DRIVE PREPARATION

The disk drive must be configured for the proper number of sectors and have an ID plug or address selection switches properly configured.

3.2.1 Drive Placement

Uncrate and install the disk drives according to the manufacturer's instructions. Position and level the disk drives in their final places before beginning the installation of the SC31/BX. This positioning allows the I/O cable routing and length to be accurately judged. Place the drives side-by-side to make installation of the daisy-chained A Cable simpler.

3.2.2 Local/Remote

The local/remote switch controls whether the disk drive can be powered up from the drive (local) or the controller (remote). Place the switch in the REMOTE position. With the CPU powered down, press the Start switch on the front panel of each of the drives (the Start LED will light, but the drive will not spin up and become ready). When the CPU is powered up, the drives will spin up sequentially. This sequential power-up prevents the heavy current draw that would be caused if all the drives were powered up at once. When in the remote mode the drives will power down when the CPU is powered down. While the CPU is powered on, the drives may be powered up and down individually (to change disk media, for example) by using the drive Start switch.

3.2.3 Sectoring

See Appendix A, Configuration Selection, for the correct sector count settings for the disk drives in use. The exact method of entering the sector count differs from one drive manufacturer to another and the particular drive manual should be consulted for the exact procedure.

3.2.4 Drive Numbering

An address from 0 to 3 must be selected for each drive. Be careful that no two drives are assigned the same number. To determine the number that each drive should be assigned, the user must first decide on the particular configuration that will be used. The drive numbers should then be assigned according to that configuration by matching the number of cylinders and tracks in Table A-2 to the drives. See paragraph A.2.1.2 for an example.

CDC drive addresses are selected by means of an ID plug. Drives by other manufacturers have their addresses selected by switches on one of the logic cards. Consult the particular drive manual for the exact procedure.

3.2.5 Sector and Index Modifications

It may be necessary to move the Sector and Index signals from the A Cable to the B Cable. See Section 3.4.3. Instructions for doing this for commonly used drives is included in Appendix B.

3.3 SYSTEM PREPARATION

Power down the system and switch OFF the main AC breaker at the rear of the cabinet (the AC power indicator will remain lit). Slide the CPU out of the cabinet and remove the cover.

PROMs

SC3101-0004

J5

J4

Fault LED

J3

Activity LED

J2

J1

SW1

SW2

U135 Auto Increment PROM

SW3

U129 Address PROM

U128 Configuration PROM
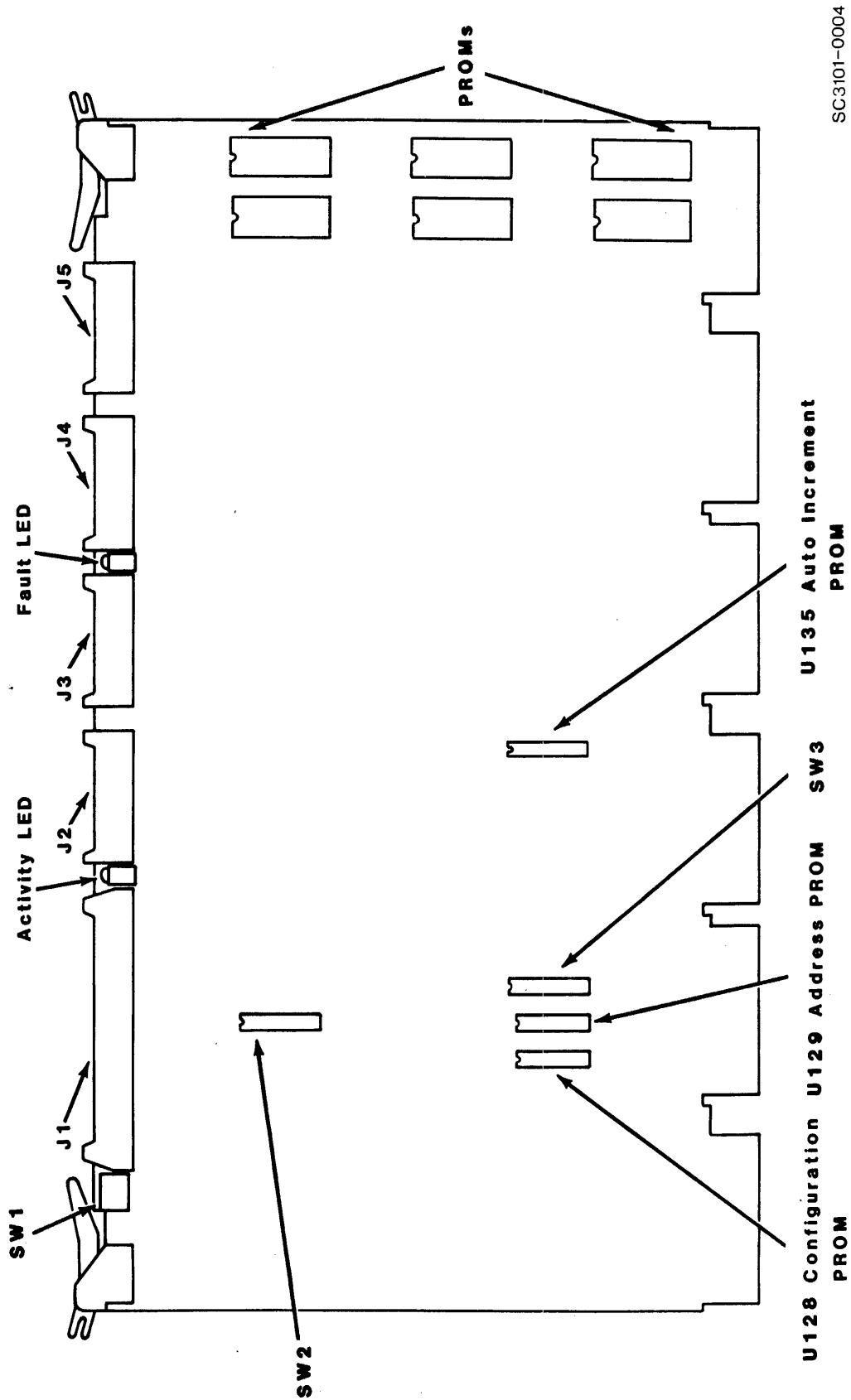
Figure 3-1 SC31 Controller Assembly

3-3

Refer to Figure 3-1 for the locations of the configuration switch, PROMs and connectors on the SC31 Controller Board.

3.4.1 Controller Address Selection

All Unibus controllers have a block of several command and status registers through which the system can command and monitor the controller. The blocks are 2-20 registers long, and are addressed sequentially from a starting address assigned to that device type, in this case a disk controller. On the SC31 register addresses are decoded by decode PROM 798, located at U129. One of four starting addresses for the controller's Unibus registers is selected by DIP switch SW3. See Table 3-1 for register address switch settings. Make sure only one of the four switches is closed.

Table 3-1
Controller Address Switch Settings

SW3-6	SW3-7	SW3-8	SW3-9	Address
C	O	O	O	776700 (Standard)
O	C	O	O	776300 (Alternate)
O	O	O	C	776400 (Alternate)
O	O	C	O	776600 (Alternate)

3.4.2 Interrupt Vector Address

The interrupt vector address is selected by means of SW2-1, SW2-2 and SW2-3. The standard vector address is 254. Table 3-2 lists the switch settings for the standard and alternate interrupt vector addresses.

Table 3-2
Interrupt Vector Address Switch Settings

SW2-3	SW2-2	SW2-1	Vector
O	O	O	254 (Standard)
O	O	C	150 (Alternate)
O	C	O	370 (Alternate)
O	C	C	374 (Alternate)
C	O	O	354 (Alternate)
C	O	C	224 (Alternate)
C	C	O	270 (Alternate)
C	C	C	274 (Alternate)

3.4.3 Drive Configuration Selection

The phrase "drive configuration selection" describes the process that is used to select the logical disk drives that will be emulated by the SC31/BX controller when using a given set of

physical disk drives. Using those disk drives and the SC31/BX, the user emulates a specific type and arrangement of DEC subsystems. (The emulated system is referred to as a logical disk drive.) Setting SW3-1 through SW3-5 and SW3-10 on the controller allows selection of the logical disk drive configuration (limited, of course, by the physical disk drives available).

The SC31/BX has the capability to emulate both RM and RP type drives when certain configurations are selected. The drive types are roughly divided into three groups: RM02/03/05, RM80 and RP04/05/06. Each physical drive can support any drive type. When a physical drive has two logical units assigned to it, each logical unit has the same type and capacity, except the CDC 9448-96 drive. It has an RM02 as one logical unit and a different capacity RM03 as the other unit (see configuration numbers 20 and 22). Examples of configurations with mixed (both RP and RM) drive types may be seen in configuration numbers 42 and 43 in Table A-2.

For ease of manual maintenance, the configuration table for the SC31/BX is contained in Appendix A.

3.4.4 Index and Sector Pulse Selection

The SC31/BX controller is designed to have the Index and Sector signals on the B Cable from each physical drive. The signals are necessary for proper operation of the sector counters associated with each drive. Both the RP and RM emulations require an updated sector counter which can be read by the CPU. Failure to have a valid sector counter may cause incorrect operation of the rotational position sensing software.

Depending on the disk drive, the Index and Sector pulse signals may be carried on the A instead of the B Cable. For example, standard CDC drives provide the Index and Sector signals on the A Cable; however they may be moved to the B Cable by minor rewiring of the drive backplane or by ordering this configuration from the factory. The procedure for making this modification to several of the more common drives is described in Appendix B. If the procedure for the drive in question is not covered there, it is generally described in the drive manual.

It is possible to operate with the Index and Sector signals on the A Cable by placing switch SW2-8 in the ON position. When operating in this manner there is considerable loss of capabilities and performance including: the Search command operates as a Seek; the sector counter in RPLA/RMLA will be incorrect; each transfer must wait for an Index pulse to sync-up the sector counter. Also, some of the lower level diagnostics will produce some errors.

3.4.5 SC31/BX Options

3.4.5.1 Logical Unit Swap

The SC31/BX has the ability to swap logical units 0-3 with 4-7. For example, in configuration 20, logical unit 0 would be an RM02, logical unit 4 would be an RM03, logical unit 1 would be an RM02, logical unit 5 would be an RM03, logical unit 2 would be an RM02 and logical unit 6 would be an RM03. This swap is accomplished by setting option switch SW2-4 ON (closed).

3.4.5.2 Replacement Track Mode

This option functions with RP units only, and requires a custom formatter provided by the user. When this mode is enabled, the DEC Formatter and some subtests in the Functional diagnostics will fail. This mode is enabled by setting option switch SW2-5 ON.

3.4.5.3 Dual Port Mode

Dual Port mode is selected by setting SW2-6 ON. This option should only be selected when used in conjunction with a properly written dual port driver. See paragraph 2.6. In addition, this mode should only be selected when the disk drive has dual ports and is configured for Dual Port operation. When this mode is enabled, the Functional diagnostics will not run.

3.4.5.4 DMA Bandwidth Control

This feature is enabled by setting SW2-7 ON and loading the proper register with a desired additional delay time period. See paragraph 5.5.1 for complete information on enabling this feature. When this feature is enabled, some subtests in the Functional diagnostics will fail.

3.4.5.5 Sector and Index Signals

Option switch SW2-8 switches the Sector and Index signal from the B Cable to the A Cable. See paragraph 3.4.4 for more information. When this feature is enabled, some subtests in the Functional diagnostics will fail.

3.4.5.6 Dual Access Mode

In order to provide compatibility with dual access software when it is configured for dual access, this mode is provided. To enable the Dual Access mode, SW2-9 must be ON. This mode should be selected only when the disk drive has dual ports and is configured for Dual Port operation. When this mode is enabled, some subtests in the Functional diagnostics will fail. See paragraph 2.6.7 for programming operation.

TOP OF BACKPLANE

SLOTS

TYPICAL SOCKET
(REAR VIEW)

LAST
SLOT
(BUS TERMINATOR
OR UNIBUS OUT)

FIRST
SLOT
(UNIBUS
IN)

SC3101-0001
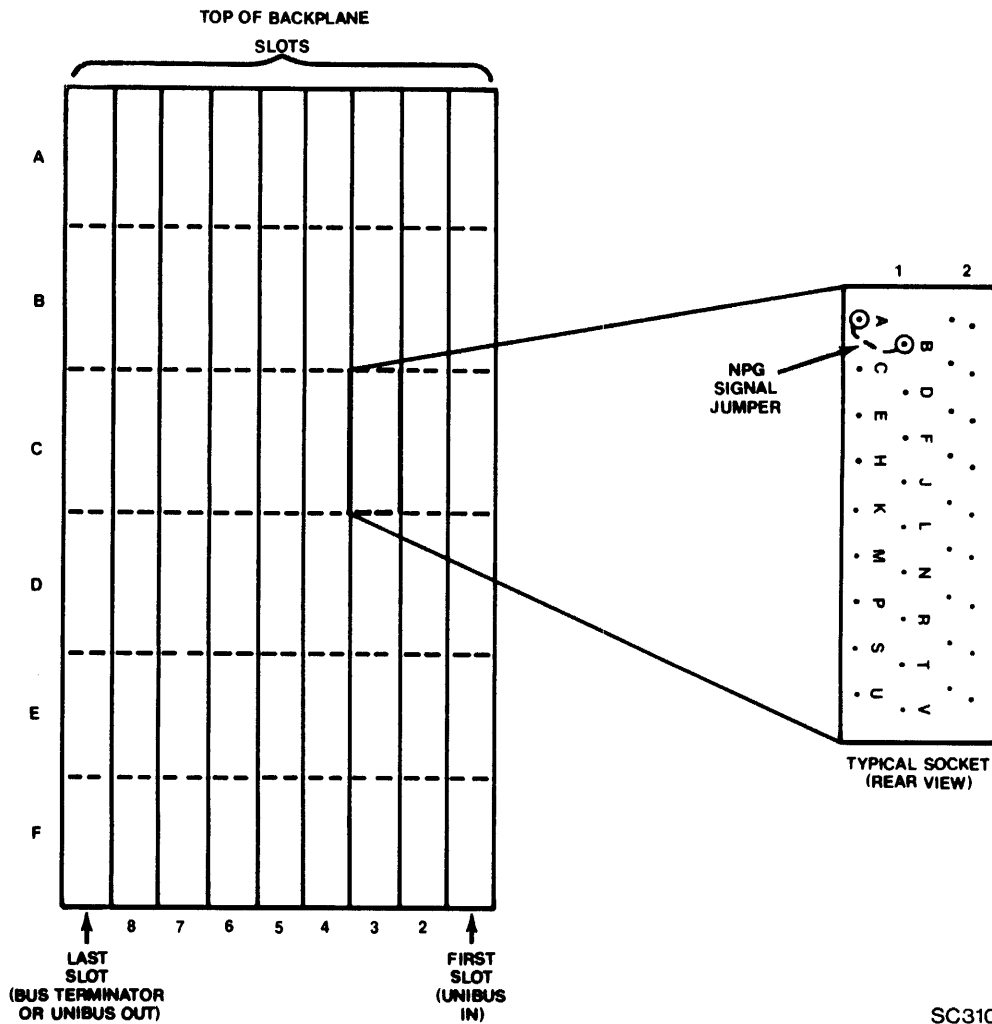
Figure 3-2   NPG Signal Jumper Location

3.4.5.7   Sector Interleave

Option switch SW2-10 enables a 2:1 sector interleave (1:1 is the default). This feature requires an even number of sectors per track. When this feature is enabled, some subtests in the Functional diagnostics will fail.

NOTE: Media compatibility (see paragraph 1.4.1) exists only so long as the SC31 is used with a 1:1 sector interleave.

3.4.5.8   Defeat Suspended DMA Option

Normally the controller will suspend its DMA operations temporarily whenever it sees the BSACK signal active on the bus. This feature prevents data late conditions from occurring on other devices. A jumper can be installed from 'M' to ground to defeat this feature.

3-7

3.4.5.9 Mapping Two RP06s on 19 Head Drives

This option allows two standard DEC RP06 drives to be mapped onto a 19-head drive. The drive must have 44 sectors per track, 815 cylinders, and at least 19 heads.

This option is enabled by setting switch SW1-3 ON (closed). Setting switch SW1-3 OFF (open) disables this option. SW1-3 should be OFF for use with drives with more than 19 heads.

NOTE: Use of this option requires Rev. E and above firmware.

3.5 PHYSICAL INSTALLATION

3.5.1 SPC Slot Selection

The controller may be placed in any SPC slot along the Unibus without regard to NPR priority. The controller contains adequate buffering to prevent data lates and will automatically get off the bus if any other device is waiting for the Unibus (suspend DMA). If the system contains a Unibus repeater, the controller will not give priority to devices which are on the CPU side of the repeater when the controller is on the far side of the repeater. This may require that the controller be placed on the CPU side of the repeater or that all DMA devices be on the far side of the repeater.

3.5.2 NPG Signal Jumper

The NPG signal jumper between pins CA1 and CB1 on the backplane must be removed so that the NPG signal passes through the controller. See Figure 3-2.

3.5.3 Mounting

The controller board should be plugged into the Unibus backplane with components oriented in the same direction as the CPU and other modules. Always insert and remove the board with the computer power OFF to avoid possible damage to the circuitry. Be sure that the board is properly positioned in the throat of the connector before attempting to seat the board by means of the extractor handles.

3.5.4 PROM Replacement

There are six emulation PROMs on the SC31 PCBA, located along the right edge of the board (when viewed from the component side). The sockets are labeled PROM 0 through PROM 5 in a discontinuous physical order. When these PROMs are replaced, the ID numbers (found on top of the PROM) are placed in the same sequence as the PROM numbers silkscreened on the board next to each socket.

DAISY CHAINED SYSTEM

CONTROLLER I

DRIVE 0 — IJ3 (A), IJ4 (A), IJ2 (B) / IIJ3 (A), IIJ4 (A), IIJ2 (B)

DRIVE 1 — IJ3 (A), IJ4 (A), IJ2 (B) / IIJ3 (A), IIJ4 (A), IIJ2 (B)

DRIVE 2 — IJ3 (A), IJ4 (A), IJ2 (B) / IIJ3 (A), IIJ4 (A), IIJ2 (B)

DRIVE N — IJ3 (A), IJ4 (TERM), IJ2 (B) / IIJ3 (A), IIJ4 (A/TERM), IIJ2 (B)

CONTROLLER II

DUAL CHANNEL UNITS ONLY
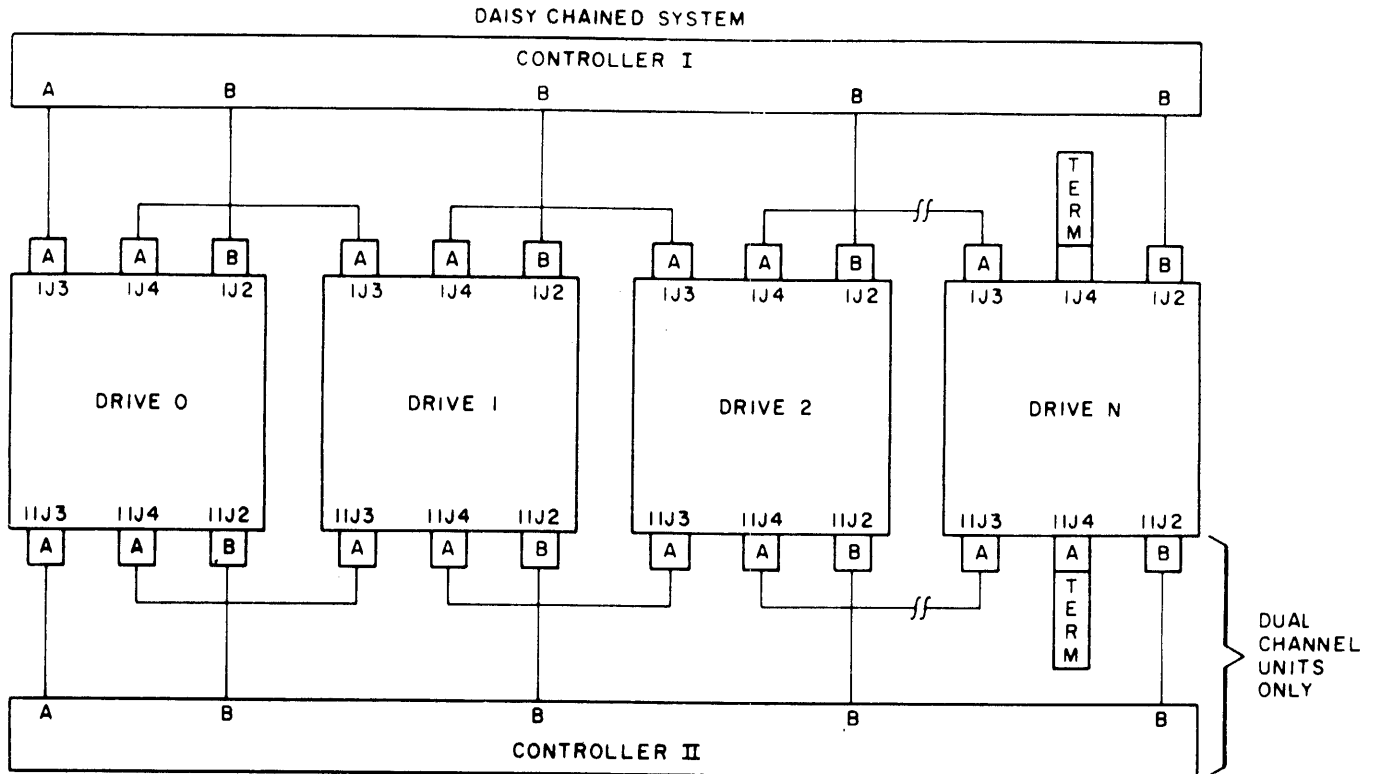
NOTES:

1. MAXIMUM INDIVIDUAL A CABLE LENGTHS = 100 FEET

2. MAXIMUM INDIVIDUAL B CABLE LENGTHS = 50 FEET

SC3101-0000

Figure 3-3.   SC31 Cabling Diagram

3.6   CABLING

The subsystem cabling of the drives and controller is shown in Figure 3-3.

3.6.1   A Cable

The 60-wire A Cable should be plugged into the connector on the controller and wired to the first drive. If more than one drive is used, it is then daisy-chained to the other drives. The last drive on the A Cable must have a terminator installed. This part is available from the drive manufacturer. The terminator is generally plugged into one of two A Cable connectors on the drive. In some cases, a ground wire emerging from the terminator assembly will have to be connected to the drive to provide a ground return for the resistors in the terminator. Pin 1 of the board connector is on the left. Pin 1 of the cable connector has a notch on the connector body to identify it. Twist and flat cable will have brown-brown twist followed by red-brown twist on the pin 1 edge of the cable. The cable will normally egress to the rear of the controller.

NOTE: The connector is not keyed and can be physically reversed in the header. No damage should result, but the system will not operate.

3.6.2 B Cable

Each drive must have a 26-wire B Cable wired from the drive to one of the B ports of the controller. It makes no difference which B port connection is used by a drive. No external terminators are used with the B Cable. Pin 1 of the cable connector has a notch on the connector body to identify it. The pin 1 edge of the cable has a black stripe.

NOTE: Observe the same caution on connector reversal given in paragraph 3.6.1.

3.6.3 Grounding

For proper operation of the disk subsystem, it is very important that the disk drives have a good ground connection to the logic ground of the computer. The ground connection should be a 1/4 inch braid (preferably insulated) or AWG No. 10 wire or larger. The grounding wire may daisy-chain between drives. If the drive has a switch or jumper which connects the logical signal ground to the cabinet ground (dc ground to ac ground), this connection should be removed once the drive is put on-line with the controller. It can be connected for performing local off-line maintenance on the drive.

NOTE: Failure to observe proper grounding methods will generally result in marginal operation with random error conditions. In particular, care must be taken when Fujitsu Eagle and CDC disk drives are placed on the same line. The procedure below should be followed on any system which mixes Fujitsu Eagles and CDC drives on the same daisy chain:

1. Disable Tags 4 and 5 on the Eagle as described on pages 3-7 of the Fusjitsu manual.

2. Use one of the following three grounding procedures:

    A. Install CDC drives with chassis (AC) and signal (DC) grounds connected together at the drive. Refer to the system grounding section of the CDC drive manual for details.

        Install grounding strap SG (DC) to FG1 (AC) on the Eagle.

        Install separate ground straps from each drive to the common system ground on the CPU.

B. Install FCC-approved drive cables and attach all cable shields to the CPU and drive chassis grounds.

C. Separate the chassis (AC) and signal (DC) grounds on each drive.

Install FCC-approved cables and attach the shield grounds to the chassis (AC) ground of each drive. Daisy chain the signal (DC) ground of each drive to the signal (DC) ground of the controller.

3. If the cable from the controller to the **first** drive is less than 25 feet, place the Eagles first in the daisy chain. If the cable from the controller to the **first** drive is more than 25 feet, place the Eagles last on the daisy chain, closest to the terminator. If the **total** daisy chain length is more than 50 feet, use FCC approved cables whenever possible.

3.7 TESTING

3.7.1 Self-Test

When power is applied to the CPU, the controller will automatically execute a built-in self-test. This self-test is not executed with every bus INIT but only on powering-up. If the self-test has been executed successfully, the Fault LED on the top edge of the controller board will be OFF or flashing. The Fault LED flashes when the controller cannot properly address at least one drive after successfully executing its self-test. This will occur if the A and B Cables are not properly plugged in, a drive is not powered-up with a code plug, or two drives have an identical code plug. If the Fault LED is ON steadily the controller did not pass its self-test and the controller cannot be addressed from the CPU.

3.7.2 Register Examination

After powering-up the CPU and noting that the FAULT indicator is not ON steadily, a quick check should be made to ensure that the controller registers can be read from the computer console. The RPCS1 register will contain 004200 if the drive is available, and 000200 if it is not. If the CPU has a console emulator, all the registers of the controller should be examined.

3.7.3 Hardware Formatting the Disk

The controller has the means to format the disk by writing standard headers and zero data in all sectors of the disk. This format does not verify the data or headers.

If the drive is on-line, the formatting is carried out as follows:

1) INIT the controller from the PDP-11 console or deposit a 40 at 776710 or 776310.

2) Deposit the drive number (if other than 0) in RPCS2/RMCS2 at 776710 or 776310.

3) Deposit a 000021_8 (Read-in Preset command) in RPCS1/RMCS1 at 776700 or 776300. This sets Volume Valid.

4) Deposit a 177777_8 in RPCC/RMHR at 776736 or 776336 to enable the optional Format command to be executed.

5) Deposit a 000077_8 (Format command) in RPCS1/RMCS1 at 776700 or 776300. The ACTIVITY indicator on the left side of the board will flash as long as the formatting is underway.

6) Examine RPDS/RMDS at 776712 or 776312 to see if the drive's ERR (bit 14) is set, indicating an error. If there is an error resulting from the format operation, RPER1/RMER1, RPER2 and RPER3/RMER2 should be examined to determine the cause of the error, and RPDA/RMDA and RPDC/RMDC should be examined to see how far the formatting progressed.

3.7.4 Diagnostics

The DEC diagnostics should be run. Generally it will be necessary to run only the Formatter and the Performance Exerciser. Appendix C contains patches to the DEC RM02/03 diagnostics.

3.8 OPERATING SYSTEM PATCHES

If the disk drive has a different capacity than the DEC disk for the selected Drive Type Code, it will be necessary to patch the operating system. RSTS/E and RSX-11M patches can be found in the Emulex Patch Document.

4.1 OVERVIEW

There are 20 device registers in the SC31/BX. These are used to interface the controller to the drives and the computer. The registers are loaded and/or read under program control in order to initiate selected disk commands and monitor status and error conditions. Most registers can be written into with word or byte operations.

The SC31/BX has the ability to emulate both RM and RP type drives when certain configurations are selected. Each physical drive can support any drive type, and when a physical drive has two logical units assigned to it, each logical unit is the same type and capacity. Consequently, many registers in this section are both (but not simultaneously) RP and RM registers. Those that are not are indicated as such by their single (unslashed) mnemonic and are broken down into two third level headings. The second level header gives the address which is common to both registers. For example, section 4.12 lists 776724 as the address which pertains to both RMMR1 (4.12.1) and RPMR (4.12.2). Whether an RP or an RM register is activated depends on the drive configuration setup of the user (see Table A-2).

4.1.1 Common Features

The RPWC/RMWC, RPBA/RMBA, RPCS2/RMCS2, RPDB/RMDB and bits <15:12> and <10:06> of RPCS1/RMCS1 are common to all drives. Loading and reading of these registers is independent of the unit selected. A separate set of the other registers and bits 11 and <05:00> of RPCS1/RMCS1 exists for each of the drives. Loading and reading of these registers is dependent on the drive selected by the unit number in RPCS2/RMCS2. In addition, the eight ATA bits in RPAS/RMAS are each associated with an individual drive. Any attempt to write into the drive registers (except RPAS/RMAS) while the drive's GO bit is asserted will cause a Register Modification Refused error and the register is not modified.

4.2 CONTROL/STATUS REGISTER ONE (RPCS1/RMCS1) 776700

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SC	TRE	0	0	DVA	PSEL	A17	A16	RDY	IE	F4	F3	F2	F1	F0	GO
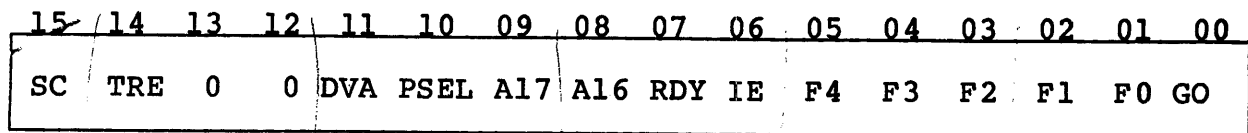
```
---Common To---        ---- Common To----
   All Drives              All Drives
```

The RPCS1/RMCS1 register can be read or written by program control, and is used to store the current disk command function code and operational status of the controller. Setting the GO bit will cause the controller to recognize the function code in the register

and initiate the operation for the selected drive. The actual start of execution of the command does not begin when the function code is loaded into the control register, but commences when the controller has finished any previous operation and polls through the drive RPCS1/RMCS1 registers in search of a command needing initiation.

Special Condition (SC) - Bit 15

This read only bit is set as long as TRE in RPCS1/RMCS1 or any of the drive ATA bits are set. This bit causes a CPU interrupt if IE is also set.

Transfer Error (TRE) - Bit 14

This read/write bit is set by DLT, WCE, UPE, NED, NEM, PGE, MXF, or a drive error during a Data Transfer. Writing a one into the bit causes the Controller Error bits in RPCS2/RMCS2 to be cleared. These Controller Error bits are also cleared at the start of every Data Transfer operation.

Drive Available (DVA) - Bit 11

This read-only bit is set when the drive is seized by the controller. When not in Dual Port mode, the drive is seized as long as it is powered-up.

Port Select (PSEL) - Bit 10

This is a read/write bit that has no effect on any controller operations. (For diagnostic compatibility.)

Extended Bus Address (A16, A17) - Bits <09:08>

Upper extension of the RPBA/RMBA register. This two-bit counter is incremented by one every time RPBA/RMBA overflows. These bits cannot be altered if RDY equals zero and no error results when attempted.

Ready (RDY) - Bit 07

This read-only bit is reset when the controller starts a Data Transfer Command (codes 51 - 77) and is set at the termination of the Data Transfer operation.

Interrupt Enable (IE) - Bit 06

When IE is set an interrupt can be generated when RDY is asserted at the end of a data transfer or by any ATA being asserted. It is reset automatically when the interrupt is accepted by the CPU. When a zero is written into IE by the program, any pending interrupts are cancelled. An interrupt is generated by writing ones into IE and RDY at the same time.

Function Code (F4-F0) - Bits <05:01>

F4-F0 and the GO bit make up the Function (command) code which determine the action to be performed by the controller and drive as shown below:

01	No Operation	35	Suspended DMA Stall Count*
03	Unload (RP only)	37	Transparent ECC Correction*
05	Seek Command	41	Word Count Equals Sector Count*
07	Recalibrate	51	Write Check Data
11	Drive Clear	53	Write Check Header and Data
13	Release	55	Physical Write Check Header and Data*
15	Offset Command	61	Write Data
17	Return to Centerline	63	Write Header and Data
21	Read-In Preset	65	Physical Write Header and Data*
23	Pack Acknowledge	71	Read Data
25	DMA Bandwidth Set*	73	Read Header and Data
27	DMA Burst Length*	75	Physical Read Header and Data*
31	Search Command	77	Format*

*Optional

GO (GO) - Bit 00

The GO bit must be set to cause the controller to respond to a command. The GO bit is reset after command termination.

4.3 WORD COUNT REGISTER (RPWC/RMWC) 776702

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
						Two's Complement Word Count									
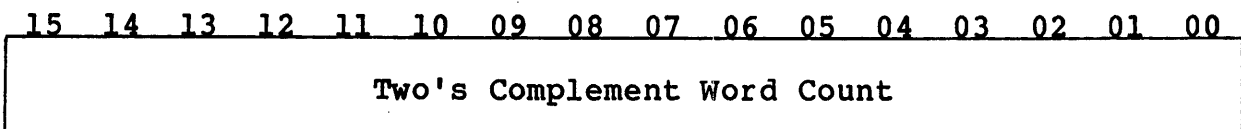
The RPWC/RMWC register is loaded with the two's complement of the number of data words to be transferred to or from main memory. The register is incremented by one after each word transferred, and accommodates a maximum transfer of 65,536 words. The RPWC/RMWC register is not cleared by INIT or Controller Clear.

4.4 UNIBUS ADDRESS REGISTER (RPBA/RMBA) 776704

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
						Memory Address									
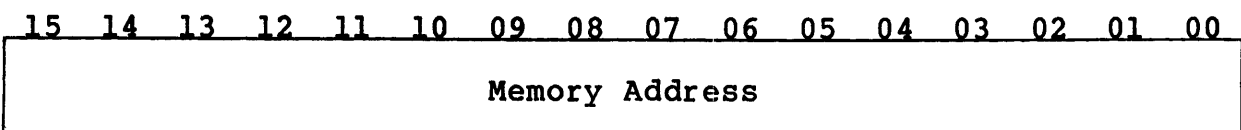
The RPBA/RMBA register is initially loaded with the low-order 16 bits of the memory address for a Data Transfer. The low-order bit (00) is always forced to a zero. The RPBA/RMBA register is incremented by two after transfer of a word to or from memory, unless the BAI bit is set. RPBA/RMBA is cleared by INIT or Controller Clear.

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4.5 DISK ADDRESS REGISTER (RPDA/RMDA) 776706

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Track Address								Sector Address							
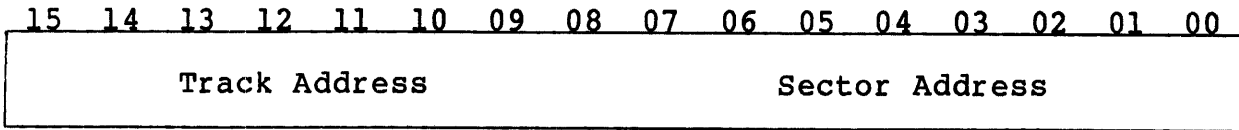
This register is used to address the sector and track on the disk
to or from which a transfer is desired. It can only be loaded as a
word. The RPDA/RMDA is incremented each time a sector of data is
transferred so that consecutive blocks are automatically addressed
when the word count indicates that more than one block is to be
transferred. At the end of a transfer, RPDA/RMDA contains the
address of the sector following the last one involved in the data
transfer.

For RM drives, this register is a full 16-bit read/write register.
For RP drives, only bits <13:08> and <04:00> are read/write. The
rest are zeros.

The RPDA/RMDA contains a sector counter providing up to 32 or 64
sectors per track. The register also contains a track counter
which is incremented by one every time the sector counter overflows
its maximum count. When the sector address and the track address
reach their maximum counts, they are reset to zero and the
RPDC/RMDC is incremented by one. The Invalid Address error (IAE,
RPER1/RMER1, bit 10) is set if the address in the RPDA/RMDA is
invalid when a Data Transfer, Seek, or Search function is
initiated. The maximum sector and track addresses are obtained
from the selected configuration.

4.6 CONTROL/STATUS REGISTER TWO (RPCS2/RMCS2) 776710

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT	WCE	UPE	NED	NEM	PGE	MXF	MDPE	OR	IR	CLR	PAT	BAI	U2	U1	U0
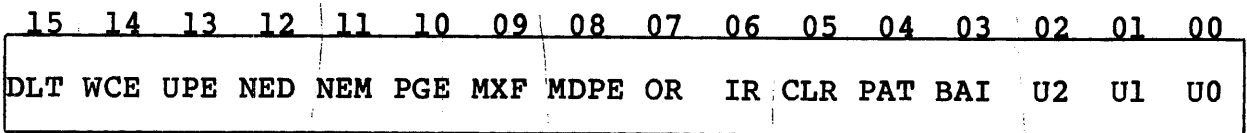
The RPCS2/RMCS2 register can be read or written under program
control and is used to store the current drive select code and
controller operational status. In addition, the register can
initiate a Controller Clear operation. It is recommended that
writes to the unit select bits be done with byte operations since
two of the error bits in the upper byte are read/write.

Data Late (DLT) - Bit 15

This bit cannot normally be set because of the fourteen-sector
buffer in the controller. It can be set by accessing RPDB/RMDB
without the appropriate status bit (06 or 07) in RPCS2/RMCS2 set to
a one. This is a read-only bit.

Write Check Error (WCE) - Bit 14

Set when the controller is performing a Write Check operation and a word from the disk does not match the corresponding word in memory. When the mismatch occurs, the reading of the disk terminates and the WCE bit is set. The memory address displayed in RPBA/RMBA is the address of the word following the one which did not match (if BAI is not set). The mismatched data word on the disk is displayed in the data buffer (RPDB/RMDB). RPDA/RMDA and RPDC/RMDC contain the address of the sector following the one that caused the error. This is a read-only bit.

Unibus Parity Error (UPE) - Bit 13

Set if a parity error occurs in the Unibus memory while the controller is performing a Write or Write Check command. When the error occurs, the RPBA/RMBA register contains the address of the word following the word with the parity error (if BAI is not set). This is a read/write bit.

Nonexistent Drive (NED) - Bit 12

Set when the program Reads or Writes a device register associated with a drive (selected by U2-U0) which is not recognized because of a wrong code plug, not powered up, or is non-existent. This is a read-only bit.

Nonexistent Memory (NEM) - Bit 11

Set when the controller is performing an NPR transfer and the memory does not respond within 10 microseconds. The memory address displayed in RPBA/RMBA is the address of the word following the memory location causing the error. This is a read-only bit.

Program Error (PGE) - Bit 10

Set when the program attempts to initiate a Data Transfer operation while the controller is currently performing one. This is a read-only bit.

Missed Transfer (MXF) - Bit 09

Set if a Data Transfer cannot be executed (RPDS/RMDS ERR bit equals one). This is a read/write bit.

Massbus Data Bus Parity (MDPE) - Bit 08

This read-only bit is always a zero.

Output Ready (OR) - Bit 07

Set when a word is present in RPDB/RMDB and can be read by the program. Cleared by reading RPDB/RMDB. Any attempt to Read RPDB/RMDB register before OR is asserted will cause a DLT error. This is a read-only bit.

Input Ready (IR) - Bit 06

This read-only bit is always a one.

Controller Clear (CLR) - Bit 05

When a one-bit is written into this bit position, the controller is initialized. This is a write-only bit. It is always read as a zero.

Parity Test (PAT) - Bit 04

This read-write bit has no effect on any controller operation. (For diagnostic compatibility.)

Unibus Address Increment Inhibit (BAI) - Bit 03

When BAI is set, the controller will not increment the RPBA/RMBA register during data transfers, causing all data words to be read from or written into the same memory location. This is a read/write bit.

Unit Select (U2-U0) - Bits <02:00>

These bits select one of eight drives for communicating with the CPU. The Unit Select bits can be changed at any time without interfering with current operations. These are read/write bits.

4.7 DRIVE STATUS REGISTER (RPDS/RMDS) 776712

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATA	ERR	PIP	MOL	WRL	LST	PGM	DPR	DRY	VV	0	0	0	0	0	OFM

This register contains various status indicators for the drive selected by the unit number in RPCS2/RMCS2. The register is a read-only register.

Attention Active (ATA) - Bit 15

An Attention condition will set the ATA bit in this register and The Attention Summary register (RPAS/RMAS). It is cleared by INIT, Controller Clear, loading a command with the GO bit set or loading a 1-bit in RPAS/RMAS register corresponding to the drive's unit number. The last method of clearing the ATA bit will not clear the error indicators.

An Attention condition is caused by: an error in the error registers; the completion of a positioning operation; the change of state of the MOL bit; Dual Port operation with the drive presently available if previously not available; correct sector identification for the Search command; completion of the Unload command.

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Error (ERR) - Bit 14

Set when one or more of the errors in the error registers (RPER1/RMER1, RPER2 or RPER3/RMER2) for a selected drive is set. While ERR is asserted, commands other than Drive Clear are not accepted.

Positioning in Progress (PIP) - Bit 13

Set when a positioning command is accepted. These commands are: Seek, Offset (RP drives only), Return-to-Centerline (RP drives only), Recalibrate, and Search. Cleared when the moving function is completed at the time the DRY and ATA bits are set. Also set during implied and mid-transfer seeks executed as part of a data transfer command. For RM02/03/05 drives, set if MOL equals zero.

Medium On-Line (MOL) - Bit 12

Set when the Unit Ready line from the drive is asserted indicating that the drive is up to speed, the heads are positioned over the recording tracks and no fault condition exists within the drive. Cleared when the spindle is powered down or the drive is off-line. Whenever the MOL bit changes state, the ATA bit is set.

Write-Lock (WRL) - Bit 11

Set when the Write Protected line from the drive is asserted as enabled by a switch located on the drive. A Write command on a write-locked drive will cause the Write-Lock error (WLE, bit 11 of RPER1/RMER1) to be set. For RM80 drives, set if MOL equals zero.

Last Sector Transfer (LST) - Bit 10

Set when the last addressable sector on the disk pack has been read or written. Cleared when a new write to RPDA/RMDA is received.

At the time LST is set, the RPDA/RMDA register is reset to zero and the RPDC/RMDC register increments by one to the first illegal cylinder address. If the RPWC register is not zero, a mid-transfer Seek command will abort, causing the AOE status bit (RPER1/RMER1, bit 09) to be set, indicating that the desired cylinder register overflowed during a Read or Write.

Programmable (PGM) - Bit 09

This bit is set when Dual Port or Dual Access operation is enabled.

Drive Present (DPR) - Bit 08

This bit is set if the controller has seized the drive and is reset when the other controller has seized the drive. This bit is a reflection of the DVA bit in RPCS1/RMCS1.

Drive Ready (DRY) - Bit 07

Set at the completion of every command and cleared at the
initiation of a command. When set, this bit indicates the
readiness of the drive to accept a command. If a mechanical
movement command was initiated, the ATA bit will also be set when
DRY is set. This bit is the complement of the drive's GO bit.

Volume Valid (VV) - Bit 06

Set by the Pack Acknowledge or Read-In Preset commands. Cleared
whenever the drive cycles up from the OFF state. When reset, this
bit indicates that the drive has been off-line and a disk pack may
have been changed.

Offset Mode (OFM) - Bit 00

This bit is enabled only with RM drives. Set by the Offset command
to indicate that a read will be done with the heads in the offset
position as determined by RMOF bit 07. Cleared by a Read-In
Preset, Return-to-Centerline, Recalibrate or Write command, or a
mid-transfer Seek command.

4.8   ERROR REGISTER ONE (RPER1/RMER1)   776714

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DCK	UNS	OPI	DTE	WLE	IAE	AOE	HCRC	HCE	ECH	WCF	FER	PAR	RMR	ILR	ILF

The RPER1/RMER1 register is a read/write register that is used to
store the error status of the drive whose unit number is in
RPCS2/RMCS2. The RPER1/RMER1 register can only be written as a
word. Any attempt to Write a byte will cause an entire word to be
written. If the program attempts to Write into this register while
the drive is busy, an RMR (RPER1/RMER1 register, bit 02) error is
set, and the contents of the register are not otherwise modified.
Writing zeros into this register should not be used as the normal
way of clearing errors. The Drive Clear command should be used
instead.

Data Check (DCK) - Bit 15

Set during a Read operation when the ECC hardware detects an ECC
error. The Data Transfer terminates with the current sector. If
the Error Correction Inhibit (ECI) bit is off, the controller will
go into the error correction process, and the RDY bit will not be
set until the end of the process. If ECI bit is on, the error
correction process is inhibited, the Data Transfer terminates
immediately.

Unsafe (UNS) - Bit 14

This bit is a composite error bit of the unsafe and seek incomplete error conditions in RPER2 and RPER3/RMER2 registers. With UNS set, correct results on any operation cannot be guaranteed. Some faults must be cleared by manual intervention at the drive.

Operation Incomplete (OPI) - Bit 13

Set when a Read or Write command involving header search cannot find the physical sector within three Index pulses. Also set during a Search operation where a sector count match is not made within three Index pulses. When OPI is set, the GO bit is cleared and the RDY bit is set.

Drive Timing Error (DTE) - Bit 12

Set when either the header or data sync pattern is not found. When DTE is set, the GO bit will be cleared and the RDY bit set. Also set if a Sector pulse occurs before the end of a sector's data field.

Write Lock Error (WLE) - Bit 11

Set when a Write command is issued to a write-locked drive.

Invalid Address Error (IAE) - Bit 10

Set when the address in RPDC/RMDC or RPDA/RMDA is invalid and a Seek, Search or Data Transfer command is initiated.

Address Overflow Error (AOE) - Bit 09

Set when the RPDC/RMDC register overflows during a Read or Write operation indicating that the address has exceeded the cylinder address limit. With AOE set, the controller will terminate the operation when the last sector of the last cylinder has been read or written.

Header CRC Error (HCRC) - Bit 08

Set by a CRC error in the header. If a CRC error is detected during a Read or Write command, the controller will not make any Data Transfer. In the event of a CRC error during a Read Header and Data command, the entire sector will be transferred with the HCRC bit set.

Header Compare Error (HCE) - Bit 07

Set when the first two words of the header read at the sector whose count is equal to the desired sector field of RPDA/RMDA do not match the contents of RPDC/RMDC and RPDA/RMDA. If the HCE bit is set during a Read or Write command, the controller will not perform any Data Transfer. In the event of a Read Header and Data command, the entire sector will be transferred with the HCE bit set.

ECC Hard Error (ECH) - Bit 06

Set when the error correction procedure indicates that the error was a non-correctable ECC error. DCK (bit 15) is also set.

Write Clock Fail (WCF) - Bit 05

This bit is normally a zero unless written into.

Format Error (FER) - Bit 04

Set if the FMT16 bit in RPOF/RMOF does not match bit 12 in word 1 of a sector's header. The controller does not implement 18-bits per word mode. If FER is set, then HCE may not be set.

Parity Error (PAR) - Bit 03

This bit is normally a zero unless written into.

Register Modification Refused (RMR) - Bit 02

Set when a Write is attempted to any drive register (except RPMR/RMMR1 or RPAS/RMAS) with DRY equals zero. The drive will continue to execute the command in progress.

Illegal Register (ILR) - Bit 01

This bit is normally a zero unless written into.

Illegal Function (ILF) - Bit 00

Set when the function code in RPCS1/RMCS1 is illegal and the GO bit is set.

4.9 ATTENTION SUMMARY REGISTER (RPAS/RMAS)   776716

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	ATA 7	ATA 6	ATA 5	ATA 4	ATA 3	ATA 2	ATA 1	ATA 0

The RPAS/RMAS register allows the program to examine the attention status of all drives with only one Register Read operation. It also provides a means of resetting the attention logic in a selected group of drives. The eight low-order bits of this register correspond to the ATA bits in the RPDS/RMDS of the drive having the same unit number as the bit position of this register.

A drive's ATA bit can be reset by loading a one into the bit position corresponding to the drive's unit number. Loading a zero has no effect. For a program to use the RPAS/RMAS without losing status information, the program must use MOV instructions for all

Writes to this register. An instruction that does a Read-Restore (such as BIS) may cause bits that became asserted just prior to the Read to be lost. This register can be read or written at any time.

A persistent error, just like any error condition, will cause the ATA bit to be reasserted. Attempts by the controller to clear the error will not work in this case.

4.10 LOOK-AHEAD REGISTER (RPLA/RMLA) 776720

15	14	13	12	11	10 09 08 07 06	05	04	03	02	01	00
0	0	0	0	0	Sector Counter	0	0	0	0	0	0

The RPLA/RMLA register contains the drive sector counter and is used to present the angular position of the disk relative to the read/write heads for the disk whose unit number appears in RPCS2/RMCS2. The purpose of this register is to provide the programmer with a means of optimizing disk accesses by minimizing rotational delays. The counter counts from zero to the maximum sector count selected in the drive.

4.11 DATA BUFFER (RPDB/RMDB) 776722

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
							Data Buffer								

The RPDB/RMDB register provides a maintenance tool to check the controller data paths. The IR (Input Ready) and OR (Output Ready) status indicators in RPCS2/RMCS2 registers are provided so that the programmer can determine when words can be read from or written into RPDB/RMDB.

RPDB/RMDB is used as an access to the Silo Buffer for a DEC drive. This controller has no Silo Buffer. All Write operations to this register are ignored. If a Write-Check error occurs, the data word, as read from the disk, is placed in RPDB/RMDB and the OR bit in RPCS2/RMCS2 is set. Reading RPDB/RMDB resets OR. Any further attempts to read RPDB/RMDB will create a DLT error.

4.12 MAINTENANCE REGISTERS 776724

4.12.1 Maintenance Register (RMMR1)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	MUR	MOC	MSER	MDF	0	0	MWP	0	0	DMD

RMMR1 is a read/write register that allows a program to simulate various signals from the disk for diagnostic testing of the

controller. The DMD bit must be set before any other bit has an effect on the controller. This register may be written into as a word or a byte. Writing to RMMR1 can occur at any time regardless of the status of the drive. A drive or controller Clear resets this register except for bit 03, which is set.

Maintenance Unit Ready (MUR) - Bit 09

Set by a diagnostic program to simulate the Unit Ready signal from the drive.

Maintenance On Cylinder (MOC) - Bit 08

Set by a diagnostic program to simulate the On Cylinder signal from the drive.

Maintenance Seek Error (MSER) - Bit 07

Set by a diagnostic program to simulate the Seek Error signal from the drive.

Maintenance Drive Fault (MDF) - Bit 06

Set by a diagnostic program to simulate the Fault signal from the drive.

Maintenance Write Protect (MWP) - Bit 03

Set by a diagnostic program to simulate the Write Protect signal from the drive.

Diagnostic Mode (DMD) - Bit 00

Set by the diagnostic program to reconfigure the drive into Maintenance mode. None of the other bits in this register have any effect on the controller unless DMD is one. Before a drive can be set to Maintenance mode, it must first be ready and not busy. No positioner motion is initiated for a Seek, Home, Search or Implied Seek and all Data Transfer commands are ignored.

4.12.2 Maintenance Register (RPMR)

The Maintenance mode is not supported for RP units, except that if DMD equals one, then no Seek operations occur, and all Data Transfers are bypassed.

4.13 DRIVE TYPE REGISTER (RPDT/RMDT) 776726

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	MOH	0	DPM	0	0	0	Drive Type Code							

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Moving-Head (MOH) - Bit 13

This bit is always a one indicating that the drive is a moving-head device.

Dual Port Mode (DPM) - Bit 11

When set, this bit signifies that the drive is operating in Dual Port mode as selected by SW2-6 or Dual Access mode as enabled by SW2-9.

Drive Type Code - Bits <07:00>

This code specifies the type of drive as follows:

```
20 - RP04    21 - RP05    22 - RP06
24 - RM03    25 - RM02    26 - RM80    27 - RM05
```

4.14 SERIAL NUMBER REGISTER (RPSN/RMSN) 776730

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SW2 -8	SW2 -7	SW2 -6	SW2 -5	SW2 -4	SW2 -3	SW2 -2	SW2 -1	Firmware Rev.				Port No.			

The purpose of the RPSN/RMSN register was to distinguish a drive from similar drives attached to the controller by means of a four-decade serial number. Here, it consists of the controller port number for which the drive is attached, the firmware revision level, and the eight SW2 switch settings.

4.15 OFFSET REGISTER (RPOF/RMOF) 776732

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	0	0	FMT 16	ECI	HCI	SSEI	0	OFS 7	X	OFS 5	OFS 4	X	X	X	X

The RPOF/RMOF register contains inhibit bits, the drive offset direction bit and two offset function bits. The offset direction bit determines if a Read will be done with the heads and/or PLO advanced or retarded from normal position.

The following paragraph describes functions which exists with RP drives only. Although bit 07 is not exclusive to RP drives, bits 05 and 04 are. The status of OFS5 and OFS4 determines the actual offset. Bits <12:10> are cleared by a Read-in Preset command. Bits <07:00> are reset by INIT, and Drive Clear command. Bits marked 'X' are read/write but they have no affect on controller operation.

With RM drives, bits <15:00> are cleared by a Read-In Preset, but no bits are reset by INIT or Drive Clear command. SSEI is used in RM80 drives only.

Format Bit (FMT 16) - Bit 12

Set for 16 bit mode and reset for 18 bit mode. Since the controller only handles 16 bits/word format, this bit should always be a one. When reset, the controller operates with two fewer sectors per track.

Error Correction Code Inhibit (ECI) - Bit 11

Set to inhibit error correction when an ECC error is detected.

Header Compare Inhibit (HCI) - Bit 10

Set to inhibit header compare and CRC check. With HCI set, the controller depends only on the sector count for sector identification. It is recommended that the HCI bit be reset during a Write operation.

Skip-Sector Error Inhibit (SSEI) - Bit 09

For RM80 emulations only. Set to inhibit Skip-Sector errors during a header check. When this bit is set the drive operates with one extra sector per track. This bit is reset whenever a Data Transfer command increments RMDA to a new track address. This bit cannot be set unless the FMT16 bit is already set.

Offset Direction (OFS7) - Bit 07

Set under software control to select the direction of positioner and/or PLO offset. A one retards and a zero advances.

PLO Offset Enable (OFS5) - Bit 05

This bit enables the data strobe advance/retard and is enabled only with RP drives. There is no PLO offset with RM drives.

Positioner Offset Enable (OFS4) - Bit 04

This bit enables the positioner offset. This bit is enabled only with RP drives. For RM drives positioner offset is implied.

4.16 DESIRED CYLINDER REGISTER (RPDC/RMDC) 776734

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0				Desired Cylinder Address							

The RPDC/RMDC register contains the address of the cylinder to which the positioner is to move. The RPDC/RMDC register will be cleared by the Read-in Preset command. Following an initial load, the value in the RPDC/RMDC register will be incremented by one whenever the RPDA/RMDA register is reset to zero during a Data

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Transfer. When the RPDC/RMDC register is incremented and the RPWC/RMWC register is not equal to zero, a mid-transfer Seek is initiated by the controller.

The Invalid Address Error (IAE) bit will be set when, upon asserting the GO bit, the RPDC/RMDC register contains an address greater than the largest addressable cylinder.

4.17 CURRENT CYLINDER AND HOLDING REGISTERS 776736

4.17.1 Current Cylinder Register (RPCC)

15	14	13	12	11	10 09 08 07 06 05 04 03 02 01 00
0	0	0	0	0	Current Cylinder Address

The RPCC register is a read-only register that reflects the approximate position of the positioner. It is made equal to RPDC at the end of a Seek operation. Other functions are as follows: If the register is written into with one of the values listed below, it is possible to read out the configured size of the selected disk from the same register.

        100027 - Maximum cylinder address
        100030 - Maximum track address
        100031 - Maximum sector address (FMT16 bit must be set)

Writing a 177777_8 into the register enables several optional commands (see Section 5) to be executed when loaded into RPCS1. The enable remains set until either the end of a Data Transfer command or the writing of some data other than 177777_8 into RPCC.

4.17.2 Holding Register (RMHR)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RMHR is a read-only register that always returns a zero when read except as follows: If the register is written into with one of the values listed below, it is possible to read out the configured size of the selected disk from the same register.

        100027 - Maximum cylinder address
        100030 - Maximum track address
        100031 - Maximum sector address (FMT16 bit must be set)

Writing a 177777_8 into the register enables several optional commands (see Section 5) to be executed when loaded into RMCS1. The enable remains set until either the end of a Data Transfer command or the writing of some data other than 177777_8 into RMHR.

4.18 MAINTENANCE AND ERROR REGISTERS TWO 776740

4.18.1 Maintenance Register Two (RMMR2)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
11777_8															

RMMR2 is a read-only register. It will return a 11777_8 when read with drive connected and selected via RMCS2.

4.18.2 Error Register Two (RPER2)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	PLU	0	IXE	0	MDS	DCU	0	0	0	0	0	0	0	0

Error Register 2 is a read/write register that contains status information relating to the performance of the drive whose unit number is in RPCS2. This register may be written as a word only. If any bit is set in this register, then the ERR bit is RPDS is also set. In some cases, the UNS bit in RPER1 will also be set. Writing zeros into this register should not be used as the normal way of clearing errors. A Drive Clear or a Controller Clear should be used instead. If the program attempts to write into this register while the drive is busy, the RMR bit in RPER1 will be set and the Write will be ignored.

PLO Unsafe (PLU) - Bit 13

Set if the controller does not detect at least 16 servo clocks within 3.0 microseconds.

Index Error (IXE) - Bit 11

Set when the controller detects more than 128 Sector pulses without an Index pulse, with Sector and Index on the B Cable.

Multiple Drive Select (MDS) - Bit 09

Set if more than one drive responds to a logical address on the A Cable.

DC Power Unsafe (DCU) - Bit 08

Set if the -5Vdc power supply to the cable drivers and receivers is not proper.

4.19 ERROR REGISTERS TWO AND THREE   776742

4.19.1 Error Register Two (RMER2)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BSE	SKI	OPE	IVC	LSC	LBC	MDS	DCU	DVC	ACU	SSE	0	DPE	0	0	0

RMER2 is a read-write register that contains status information relating to the electromechanical performance of the drive whose unit number is in RMCS2. This register may be written as either a word or a byte. If any bit is set in this register, then the ERR bit in RMDS is also set. In some cases, the UNS bit in RMER1 will also be set. Writing zeros into this register should not be used as the normal way of clearing errors. A Drive Clear or a Controller Clear should be used instead. If the program attempts to write into this register while the drive is busy, the RMR bit in RMER1 will be set and the Write will be ignored.

Bad Sector Error (BSE) - Bit 15

Set whenever the controller detects a zero in bit 14 or 15 of the first header word and the HCI bit in RMOF equals zero. HCE in RMER1 may also be set.

Seek Incomplete (SKI) - Bit 14

Set whenever a Seek Error is received from the drive. This error also sets the UNS bit in RMER1. The controller automatically issues a Fault Clear and a Return-to-Zero to the drive if a Seek Error is detected.

Operator Plug Error (OPE) - Bit 13

Set whenever the drive's address plug is removed and then reinstalled. This bit can be cleared by issuing a Drive Clear.

Invalid Command (IVC) - Bit 12

Set whenever any command is issued to a drive with MOL equals zero. Set whenever any command except a Read-in Preset or a Pack Acknowledge is issued to a drive with VV equals zero.

Loss of Sector Clock (LSC) - Bit 11

Set when the controller detects more than 128 Sector pulses without an Index pulse, with Sector and Index on the B Cable.

Loss of Bit Clock (LBC) - Bit 10

Set if the controller does not detect at least 16 servo clocks within three microseconds.

Multiple Drive Select (MDS) - Bit 09

Set when more than one drive responds to a logical address on the A
Cable. This bit cannot be set by a program.

D.C. Power Unsafe (DCU) - Bit 08

Set if the -5 Vdc power supply to the cable drivers and receivers
is not proper. This bit cannot be set by a program.

Device Check (DVC) - Bit 07

Set if a Fault indication is received from the drive. This error
also sets the UNS bit in RMER1. The controller automatically
issues a Fault Clear and a Return-to-Zero to the drive if a Fault
is detected.

AC Power Unsafe (ACU) - Bit 06

Set if an ACLO indication is received from the Unibus.

Skip-Sector Error (SSE) - Bit 05

For RM80 emulations only. Set whenever bit 13 of the header Word
One is set and bit 09 of RMOF is reset. This error indicates that
the sector has been skipped and the data resides in the next
sector. This bit cannot be written into unless the drive is an
RM80.

Data Parity Error (DPE) - Bit 03

This bit is normally a zero unless written into.

4.19.2 Error Register Three (RPER3)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OCYL	SKI	OPE	0	0	0	0	0	0	ACL	0	0	URW	0	0	0

Error Register Three is a read/write register that contains status
information relating to the electromechanical performance of the
drive whose unit number is in RPCS2. This register may be written
as a word only. If any bit is set in this register, then the ERR
bit in RPDS is also set. In some cases, the UNS bit in RPER1 will
also be set. Writing zeros into this register should not be used
as the normal way of clearing errors. A Drive Clear or a
Controller Clear should be used instead. If the program attempts
to write into this register while the drive is busy, the RMR bit in
RPER1 will be set and the Write will be ignored.

Off-Cylinder (OCYL) - Bit 15

Set if an off-cylinder indication occurs at the completion of a Seek operation. Also sets UNS in RPER1.

Seek Incomplete (SKI) - Bit 14

Set whenever a Seek Error is received from the drive. This error also sets the UNS bit in RPER1. The controller automatically issues a Fault Clear and a Return-to-Zero to the drive when a Seek error is detected.

Operator Plug Error (OPE) - Bit 13

Set whenever the drive's address plug is removed and then reinstalled. Can be cleared by issuing a Drive Clear.

AC Power Unsafe (ACL) - Bit 06

Set if an ACLO indication is received from the Unibus.

Unsafe to Read or Write (URW) - Bit 03

Set if a fault indication is received from the drive. Also sets UNS in RPER1. The controller automatically issues a Fault Clear to the drive when a fault indication is received from the drive.

4.20 ECC POSITION REGISTER (RPEC1/RMEC1) 776744

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	ECC Position												

The Error Correction Code (ECC) Position register is a read-only register that contains the position of the error pattern as determined by the ECC correction procedure. The error position is the number of bit positions from the beginning of the sector's data field to (and including) the right-most bit position of the error pattern stored in RPEC2/RMEC2. If the detected error is not correctable using ECC, the ECH error bit in RPER1/RMER1 will be set.

4.21 ECC PATTERN REGISTER (RPEC2/RMEC2) 776746

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	Error Pattern										

The Error Correction Code (ECC) Pattern register is a read-only register that contains the 11-bit error correction pattern obtained from the ECC correction procedure. A one in the error pattern indicates a bit of the data in memory from the last read sector

which is in error. The error pattern may straddle two 16-bit words in memory. The bit displacement to the right-most bit of the pattern is determined by the bit count in RPEC1/RMEC1. The actual correction is done by an exclusive-OR of the error pattern and the data in memory.

5.1 OVERVIEW

Operations on the drive selected by the Unit Select bits in
RPCS2/RMCS2 are initiated by loading the function code and GO bit
into RPCS1/RMCS1. The function code specifies a specific command.
The commands can be divided into three categories: Data Transfer
commands, Positioning commands, and Housekeeping commands.
Commands and their corresponding function codes (always odd since
the GO bit must be asserted to execute the command) are described
below.

Some commands are divided into two descriptions, one of which
describes how it functions with RP drives, and the other describing
its function with RM drives. Those that are divided as such can be
distinguished by the fourth level heading.

5.2 . DATA TRANSFER COMMANDS

These commands involve Data Transfers to or from the disk and are
designated by function codes 51 through 77.

All Data Transfer commands have seek and sector search functions
implied. When the desired cylinder does not equal the current
cylinder during the execution of the Data Transfer, a Seek command
will be issued to the desired cylinder. The controller will then
search the desired track for the desired sector and, when found,
will start the Data Transfer. On all commands except the Write
Header and Data command (which is the format operation) and Read
Header and Data command, a match of the sector header must be made
before the Data Transfer is started. If the header compare inhibit
(HCI bit 10 in RPOF/RMOF) is set, the header will not be compared
or checked and, like the Write Header and Data command, the
transfer will be started based on the pre-recorded Sector pulses.
With the HCI bit set, header errors will not be reported. With the
HCI bit cleared, the transfer will be aborted if a header error is
detected. The Read Header and Data command aborts only the
transfers following the sector that caused the error. A Write
Check Header and Data command operates the same as the Read Header
and Data command.

The desired sector, track and cylinder addresses are updated after
the transfer of a sector. Therefore, at the end of a transfer, the
disk is set up to transfer the next sequential sector. This allows
multiple sector transfers and spiral transfers across tracks and
cylinders. When the desired cylinder address changes during a Data
Transfer operation, the implied Seek is performed and is termed a
Mid-Transfer Seek.

The header size is two words for RM drives, and four words for RP
drives. In all cases the data field size is 256 words.

The Data Transfer commands are described below:

5.2.1 Write Check Data (51)

This command reads data from the selected drive and compares it on a word by word basis with that obtained from memory. If the data fails to compare, the WCE status bit is set and the command is terminated immediately. For additional information on Write Check errors see Section 4.11 and the WCE bit in Section 4.6.

5.2.2 Write Check Header and Data (53)

This command reads the header field and data field from the selected drive and compares it on a word by word basis with data obtained from memory. If the header and data fail to compare, the WCE status bit is set and the command is terminated immediately.

5.2.3 Write Data (61)

This command writes the 256-word data field of the selected sector with words obtained from memory. A two word ECC is appended to each sector. If the word count in RPWC/RMWC goes to zero during the sector, the rest of the sector is zero filled. After a sector transfer the word count in RPWC/RMWC is checked; if not zero, the Data Transfer operation is continued to the next sector; otherwise the command is terminated by setting the RDY bit.

5.2.4 Write Header and Data (format operation) (63)

This command writes the header field and the data field of the selected sector with words obtained from memory. A one word CRC is appended to each header field, and a two word ECC is appended to each data field. After a sector transfer the word count in RPWC is checked; if not zero, the Data Transfer operation is continued to the next sector; otherwise the command is terminated by setting the RDY bit. If RPWC/RMWC goes to zero during the sector, the rest of the sector is zero filled.

5.2.5 Read Data (71)

This command reads the 256-word data field from the selected sector and transfers the data to memory. When the sector data transfer is complete, the ECC is checked to ensure that the data read from the disk was error free. If a data error occurred, the ECC correction procedure is initiated (if the ECI bit in RPOF/RMOF is reset) to determine whether the error is correctable. When finished, the command is terminated to allow software to apply the correction information. Assuming no data errors, the word count in RPWC/RMWC is checked; if not zero, the data transfer operation is repeated with the next sector. No data is transferred after RPWC/RMWC goes to zero.

5.2.6 Read Header and Data (73)

This command transfers the header field and the data field from the selected sector to memory. When the sector data transfer is complete, the ECC is checked to ensure that the data read from the disk was error free. If a data error occurred, the ECC correction procedure is initiated (if the ECI bit in RPOF/RMOF is reset) to determine whether the error is correctable. When finished, the command is terminated to allow software to apply the correction information. Assuming no data errors, the word count in RPWC is checked; if not zero, the Data Transfer operation is repeated with the next sector.

5.3 POSITIONING COMMANDS

Positioning commands are mechanical movement commands used to position the heads over the disk pack and take milliseconds to complete. Upon initiating the Positioning commands, the controller will set the PIP bit and reset the DRY bit. Upon completion of the Positioning operation, the controller resets the PIP and GO bits, sets the DRY bit and sets the ATA bit. The Positioning commands are described below:

5.3.1 Unload (03)

This command is valid for RP units only. The command is intended to cause the drive to retract its heads and stop the spindle. This can not be done with SMD-type drives, so the command is simulated. A three second cycle-down/cycle-up sequence is generated in the controller. At the end of the sequence, the controller resets the GO bit, resets Volume Valid, sets MOL, DRY and ATA, and performs a Drive Clear. The MOL bit is reset for the duration of the cycle-down/cycle-up sequence.

5.3.2 Seek Command (05)

This command causes the heads to be moved to the cylinder address specified by the contents of RPDC/RMDC. When the controller sees the Seek command with the GO bit set, it sends the cylinder address to the corresponding drive. Any attempt to write into RPDC/RMDC while the Seek is in progress will cause the RMR bit to be set and RPDC/RMDC will not be modified. Upon completion of the Seek operation, the ATA and DRY bits in RPDS/RMDS are set, and the GO bit is reset. If the drive is unable to complete a move within 500 milliseconds or if it has moved the carriage to a position outside the recording field, the drive asserts the Seek Error signal and the controller sets the appropriate seek error bit(s). The ERR, ATA and DRY bits in RPDS/RMDS are also set. The controller will automatically issue a Fault Clear and a Return-to-Zero to the drive so that Drive Clear command can clear the error. The Seek Error is not reported until the Return-To-Zero terminates.

5.3.3 Recalibrate (07)

This command will cause the drive positioner to position the heads over cylinder 0. A Return-to-Zero is automatically performed with each Head Load sequence, and whenever a Fault or Seek Error is detected.

5.3.4 Offset Command (15)

5.3.4.1 Offset Command for RP Drives

The command causes the positioner to be offset by an incremental amount from the track centerline and/or the data strobe to be advanced or retarded by a small amount on the next Read operation. This operation offers additional data recovery attempts over that provided by the ECC capability. An Offset command uses the contents of RPOF to determine the offset. At the completion of the Offset operation, the ATA bit is set indicating that a Read command can be issued. The actual Offset is simulated during this time and instead occurs at the beginning of the following Read command.

The RPOF register (except for FMT16, ECI and HCI bits) is cleared and the drive will leave the Offset state by any one of the following methods:

1) Seek to another cylinder by means of a Seek command or Mid-Transfer Seek operation.

2) A Write command.

3) A Return-to Centerline command.

5.3.4.2 Offset Command for RM Drives

This command causes the OFM bit in RMDS to be set. Subsequent reads will be done with the heads offset from the track centerline in the direction specified by RMOF bit 07. This operation offers additional data recovery attempts over that provided by the ECC capability when an ECC error is detected. If an ECC hard error occurs, two offset positions should be used. At the completion of the Offset command, the ATA bit is set, indicating that a Read command should be issued to the cylinder and track in order to recover data.

The OFM bit in RMDS will be cleared by any one of the following methods:

a. Seek to another cylinder by means of implied or Mid-Transfer Seek.
b. Write command.
c. Return-To-Centerline command.
d. Recalibrate command.
e. Read-In Preset command.

5.3.5 Return-to-Centerline Command (17)

5.3.5.1 Return-to-Centerline Command for RP Drives

This command is used to clear bits <07:00> in RPOF, and set the ATA bit in RPDS. This command is simulated. The actual return-to-centerline occurs at the completion of the Read command.

5.3.5.2 Return-to-Centerline Command for RM Drives

This command is used to clear the OFM bit, set the ATA bit in RMDS and clear bit 07 in RMOF.

5.3.6 Search Command (31)

The Search command causes the controller to first perform a Seek to the desired cylinder and then compare the sector counter with the desired sector in the RPDA/RMDA register. When they match, it sets the ATA bit, causing an Interrupt to the computer if IE in RPCS1/RMCS1 is set. An unsuccessful completion of a Search command occurs when a sector count and desired sector address match is not made during the interval of three Index pulses. In this case the OPI bit is set.

5.4 HOUSEKEEPING COMMANDS

Housekeeping commands are used to place drive logic into a known or initialized state and usually take only a few microseconds to execute. The Housekeeping commands are listed below.

5.4.1 No Op (01)

This command does not perform any operation, except to clear the ATA bit.

5.4.2 Drive Clear (11)

5.4.2.1 Drive Clear for RP Drives

This command causes the following registers and conditions associated with the drive selected by the Unit Select bits in RPCS2 to be cleared: ATA, and ERR bits in RPDS; RPAS ATA bit; bits <15:09> and <07:00> in RPMR, bits <15:00> in RPER1, RPER2, RPER3, RPEC1, and RPEC2, and bits <07:00> in RPOF. Sets bit 08 of RPMR.

5.4.2.2 Drive Clear for RM Drives

This command causes the following registers and conditions associated with the drive selected by the Unit Select bits in RMCS2 to be cleared: ATA, and ERR bits in RMDS; RMAS ATA bit; bits <15:04> and <02:00> in RMMR1; and bits <15:00> in RMER1, RMER2 and RMEC2. Sets bit 03 of RMMR1.

5.4.3 Release Command (13)

This command performs a Drive Clear function and releases the drive
for use by the other port when in Dual Port mode of operation.

5.4.4 Read-In Preset (21)

5.4.4.1 Read-In-Preset for RP Drives

This command sets the VV (volume valid) bit, clears the ATA bit in
RPDS, clears the RPDC and RPDA registers, and clears the FMT16, HCI
and ECI bits in the RPOF register.

5.4.4.2 Read-In-Preset for RM Drives

This command sets the VV (volume valid) bit in RMDS, clears the
RMDC, RMDA, and RMOF registers, and resets the OFM and ATA bits in
RMDS.

5.4.5 Pack Acknowledge (23)

This command sets the VV bit for the selected drive. This command
or a Read-In Preset command must be issued before any Data Transfer
Or Positioning command can be given if the pack has gone off-line
and then on-line (i.e., MOL change of state). It is primarily
intended to avoid unknown pack changes.

5.5 OPTIONAL COMMANDS

With the exception of DMA Bandwidth Control (Op Code 25), the
optional commands can be enabled only by writing a 177777_8 into
RMHR/RPCC. They remain enabled until either the end of a Data
Transfer command, or the writing of some data other than 177777_8
into RMHR/RPCC.

5.5.1 DMA Bandwidth Set (25)

This op code is enabled by setting DIP switch SW2-7 ON (closed).
The function of this code is to extend the delay between bursts, so
that the amount of bus bandwidth used by the controller during DMA
is reduced. The standard delay is five usec. An additional delay
(as caused by this op code) is in addition to the standard delay
and any delay caused by DMA suspensions. The amount of additional
delay is programmable on a drive-by-drive basis. The additional
delay is programmed by the following methods:

> 1. Enable this op code by setting SW2-7 ON.
>
> 2. Load RPWC/RMWC with an unsigned positive number
>   which represents the desired amount of additional
>   delay.
>
> 3. Execute this op code.

Counts from zero to 65535_{10} are programmable, with each count adding 2 usec of delay and a count of zero representing a base of two usec.

5.5.2 DMA Burst Length (27)

This op code allows the user to specify the number of words (from one to 128) per DMA burst. To enable this code, load RPWC/RMWC with an unsigned positive number (representing the desired burst length minus one) into the low-order seven bits, then enable and execute this command. This command can be executed from any on-line drive, but it will affect all drives.

The default burst length at power-up is 16. If the user programs a burst length of four, the microcode assumes that the controller is on a VAX Unibus and adapts itself as follows:

1.   the burst length is four,

2.   the amount of time between bursts is one usec,

3.   The burst cannot be suspended, but a BSACK that occurs during a burst will cause a suspend at the end of a burst,

4.   the DMA Bandwidth control will not function, and

5.   the DMA routines adjust themselves so that they are optimized for the VAX Unibus.

5.5.3 Suspended DMA Stall Count (35)

This op code allows the user to specify the amount of additional DMA suspend time to stall if eight or fewer DMA cycles occur between BSACKs. To enable this code, load RPWC/RMWC with an unsigned positive number which represents the desired additional delay, then enable and execute this command. A count of one represents a base of two usec and each additional count adds another two usec. The count can be loaded from any on-line drive, but will affect all drives. The default count at power-up is 10 (20 usec).

5.5.4 Transparent ECC Correction (37)

When this feature is enabled, correctable ECC errors are fixed within the controller before the data is transferred to the memory on a Read, or Read Header and Data operation. Reading continues with the next sector if the data is ECC correctable. If the data is not ECC correctable, Data Transfers terminate with the bad sector and an uncorrectable read error is flagged in the normal manner. Upon completion of the Read, RPEC2/RMEC2 will contain the number of corrected ECC errors for the current command. It is preset to zero at the start of a Read command.

When disabled, Read Errors are handled in the normal manner and
RPEC2/RMEC2 is not precleared. A cumulative corrected error count
is maintained for each drive and may be read out of RPCC/RMHR by
writing a 100023₈ into RPCC/RMHR and then reading the register. It
is cleared only upon power up.

This code can be set during a Write but it is not used during the
Write unless the drive is an RM80 (see Automatic Skip-Sector
Feature, paragraph 5.4.8). Because a separate flag exists in
RPOF/RMOF for each drive, the op code enables this feature only for
the drive selected in RPCS2/RMCS2. Bit 14 of RPOF/RMOF reflects
the status of Transparent ECC mode. A one indicates that the
function is enabled. It is cleared at the end of any Data Transfer
and at the beginning of any Write Check, since the function is not
supported during a Write Check.

5.5.5 Word Count Equals Sector Count (41)

When this feature is enabled, the contents of RPWC/RMWC contain the
number of sectors to be transferred, rather than the number of
words. It is valid for Read, or Read Header and Data operation and
for Write or Write Header and Data operation. This command is not
supported during a Write Check. Partial sector transfers cannot be
done in this mode.

When disabled, RPWC/RMWC contains a word count. The count is
negative in both cases.

Because a separate flag exists in RPOF/RMOF for each drive, the op
code enables this command only for the drive selected in
RPCS2/RMCS2. Bit 13 of RPOF/RMOF reflects the status of RPWC/RMWC
equals sector count. A one indicates that the function is enabled.
This bit is cleared at the end of any Data Transfer and at the
start of any Write Check.

This command is primarily intended for users who wish to transfer
very long bursts of data through single Unibus I/O ports.

5.5.6 Physical Read/Write/Write Check Header and Data

This heading comprises three op codes which are designed for users
who wish to write their own custom formatter programs to take
advantage of the track replacement feature offered on the
RP04/05/06. The RP04/05/06 drives have two extra words in the
header which the controller can utilize to specify an alternate
track and cylinder in place of the current (assumed defective)
track. Users who wish to take advantage of this mode should
contact Emulex for details.

5.5.7 Format (77)

5.5.7.1 Format for RP Drives

This command executes a Return-to-Zero; clears RPDC, RPDA; sets FMT16 in RPOF; and formats the entire pack in standard format. Each sector has the FMT16 bit set in header word 1, all zeros in header words 3 and 4, and an all 0's data field. RPDC will be set to the last cylinder number plus one at completion, and the LST bit in RPDS will be set.

5.5.7.2 Format for RM Drives

This command executes a Return-to-Zero; clears RMDC, RMDA; sets FMT16 in RMOF; and formats the entire pack in standard format. Each sector has bits <15:14> and the FMT16 bit set in header word 1 and an all 0's data field. RMDC will be set to the last cylinder number plus one at completion, and the LST bit in RMDS will be set.

5.5.8 Automatic Skip-Sector Feature

This feature enables drives running as RM80 units to automatically execute the Skip-Sector function which is standard in the RM80. The firmware will set the Skip-Sector Error inhibit bit in RMOF if either Transparent ECC mode (op code 37) or Word Count Equals Sector Count mode (op code 41) is enabled and a Skip-Sector Error is encountered. In this case the firmware will also bump the number of usable sectors per track by one (to gain access to the skip-sector), bump RMDA by one and continue the Data Transfer with the next sector.

As is the case in the normal mode, the Skip-Sector enable is reset if the end of the track is reached. Therefore, multiple skip errors can occur and all will be skipped. This feature functions for Read Data and Write Data commands only.

To ensure proper operation of this feature, the Skip-Sector error inhibit bit in RMOF must be reset immediately prior to the execution of a Read or Write. The firmware will ignore all other header errors except a CRC error on the sector being skipped, and will ignore only Skip-Sector errors on all remaining sectors of the track. This is in compliance with standard DEC RM80 formatters.

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APPENDIX A

SC31/BX CONFIGURATION AND OPTION SELECTION

A.1 INTRODUCTION

To allow the SC31/BX user maximum flexibility in disk drive
selection, the SC31/BX supports a wide variety of disk types. This
appendix provides the switch settings which make possible this
flexibility.

A.2 CONTROLLER CONFIGURATION

The SC31/BX unit is capable of supporting a wide variety of disk
drives. Switches SW3-10, and SW3-5 through SW3-1 select the
various configurations that are supported, and a list of these
drive types and capacities may be found in Table A-1. Table A-2
lists the proper switch settings for each of the various
configurations.

A.2.1 Physical vs Logical Disk Numbering

A primary feature of the SC31/BX is its ability to emulate eight
DEC disk subsystems using four physical disk drives. This is
accomplished by mapping two logical disk subsystems onto one disk
drive which contains twice as much capacity as the standard DEC
subsystem. In the event of this usage the mapping of logical units
onto physical units is as follows:

Physical Unit Number	Logical Unit Numbers
0	0 and 4
1	1 and 5
2	2 and 6
3	3 and 7

The physical/logical assignments for specific disk configurations
can be found by comparing the Physical drive column to the Logical
drive column in Table A-2.

A.2.1.2 Unit Number Assignment

The disk drives need to be assigned a distinct unit number. This
number may be determined after the configuration to use has been
decided upon. The unit number for each drive must correspond to
the physical unit number found in Table A-2. Thus, for
configuration 04, unit 0 would be an 823 cylinder, 19 track drive;
unit 1 would be an 823 cylinder, 19 track drive; unit 2 would be an
842 cylinder, 40 track drive; and unit 3 would be an 842 cylinder,
40 track drive.

A.2.2 Sectoring CDC Drives and the 2351A Fujitsu

To allow CDC drives and the 2351A Fujitsu to function properly with the SC31/BX, some alterations must be made to the sector select switch settings found in their manuals.

To configure CDC drives for 33 sectors, switch 0 must be CLOSED, with all other switches set as per the CDC manual. To configure the 2351A Fujitsu for 48 sectors, the jumpers at location BC7 must be set such that bit one is jumpered 2-3 (rather than 3-4), bit 2 is jumpered as 6-7 (rather than 5-6), and all other jumpers are as per the Fujitsu manual.

A.2.3 Drive Configuration Selection

The SC31/BX emulates five different DEC disk subsystems, the RM02, RM03, RM05, the RM80 and the RP06. The RM02 and RM03 have an unformatted capacity of 80 Mb. The RM05 has an unformatted capacity of 300 Mb, and the RM80 has an unformatted capacity of 160 Mb. The RP06 has an unformatted capacity of 200 Mb.

There are essentially three different types of drive configurations. With the first type, each emulated DEC drive exists on one physical drive. In the second type, two emulated drives are mapped onto one physical drive. The third type is a combination of the first two.

To find the configuration switch settings which are compatible with your system use the following procedure:

1. Locate your drive type and size in Table A-1. Note the KEY assigned to each type of drive you intend to use.

2. Scan down the KEY column of Table A-2 until you find your drive's number. Check the corresponding emulation in the Logical Drive column. If the emulation is not one that you require, continue to scan the KEY column in search of the required emulation.

3. After finding a suitable match for Drive 0, check the drive key and type for Drives 1, 2 and 3 for that configuration row. It is not necessary to use all drive ports.

4. When you have found an entire configuration which is suitable, set the configuration switches as indicated.

TABLE A-1
DRIVES SUPPORTED

Mfg.	Model	Key	Physical Cyl	Trk	Sec	Configurations
Ampex	330	1024-16	1024	16	32	40
Ampex	330	1024-16	1024	16	33	16,17
Ampex	9380	823-05	823	5	32	00-02,07,10,13-15, 25,36,42
Ampex	93160	1645-05	1645	5	32	34,35,36
APS	4830#	823-10	823	10	64	04,12-15,20-23,32, 33,43
CDC	9448-96	823-06	823	6	32	20,22
CDC	9715-340	711-24	711	24	32	56,57
CDC	9730-80	823-05	823	5	32	00-02,07,10,13-15, 25,36,42
CDC	9730-160	823-10	823	10	32	01-03,10,21,23,51,53
CDC	9730-160*	1646-05	823	10	33	45,46
CDC	9762	823-05	823	5	32	00-02,07,10,13-15, 25,36,42,64,65,70,71
CDC	9766	823-19	823	19	32	04,12-15,20-23,32, 33,43,57,62,63,66,67
CDC	9771	1024-16	1024	16	64	62-65
CDC	9771	1024-16A	1024	16	84	66-71
CDC	9775	842-40	842	40	32	04-07,11
CDC	9775*	1684-19	842	38	33	47
Century	T82RM	823-05	823	5	32	00-02,07,10,13-15, 25,36,42
Century	T302RM	823-19	823	19	32	04,12-15,20-23,32, 33,43,57
Century	T306	823-19	823	19	32	04,12-15,20-23,32, 33,43,57
Century	T306	815-19	815	19	22	60
Fujitsu	2280	823-05	823	5	32	00-02,07,10,13-15, 25,36,42
Fujitsu	2284	823-10	823	10	32	01-03,10,21,23,51,53
Fujitsu	2294	1024-16	1024	16	32	40
Fujitsu	2294	1024-16	1024	16	33	16,17
Fujitsu	2312	589-07	589	07	33	24,25
Fujitsu	2351A	842-20	842	20	44	41-44,53,55
Fujitsu	2351A	842-20	842	20	48	26,27
Memorex	677	819-19	819	19	22	52
Memorex	677-30	823-19	823	19	32	04,12-15,20-23,32, 33,43,57
NEC	D2351	760-19	760	19	62	61
Priam	3350	561-03	561	3	32	37
STC	8775	1124-30	1124	30	33	30-32
Techstor	160	700-12	700	12	32	50

*Mapped configurations. The controller divides the number of tracks by two and multiplies the number of cylinders by two as seen by the software. This is done to reduce the amount and/or complexity of software patches required to operate an expanded size drive.

#Set sector size to 630 bytes/sector (switch count equals 629) and enable the track length compatibility switch located on the slog board. This makes the drive look like a CDC 9766.

TABLE A-2
DRIVE CONFIGURATIONS FOR PROM 897[1]

CONF. NO.	SW-3 10	5	4	3	2	1	PHYSICAL KEY	Unit	LOGICAL Unit(s) = Dr Type	Rev
00	O	O	O	O	O	O	823-05	0	0 = RM02	A
							823-05	1	1 = RM02	A
							823-05	2	2 = RM02	A
							823-05	3	3 = RM02	A
01	O	O	O	O	O	C	823-05	0	0 = RM02	A
							823-05	1	1 = RM02	A
							823-10	2	2,6 = RM02/RM02	A
							823-10	3	3,7 = RM02/RM02	A
02	O	O	O	O	C	O	823-05	0	0 = RM02	A
							823-10	1	1,5 = RM02/RM02	A
							823-10	2	2,6 = RM02/RM02	A
							823-10	3	3,7 = RM02/RM02	A
03	O	O	O	O	C	C	823-10	0	0,4 = RM02/RM02	A
							823-10	1	1,5 = RM02/RM02	A
							823-10	2	2,6 = RM02/RM02	A
							823-10	3	3,7 = RM02/RM02	A
04	O	O	O	C	O	O	823-19	0	0 = RM05	A
							823-19	1	1 = RM05	A
							842-40	2	2,6 = RM05	A
							842-40	3	3,7 = RM05	A
05	O	O	O	C	O	C	823-19	0	0 = RM05	A
							842-40	1	1,5 = RM05/RM05	A
							842-40	2	2,6 = RM05/RM05	A
							842-40	3	3,7 = RM05/RM05	A
06	O	O	O	C	C	O	842-40	0	0,4 = RM05/RM05	A
							842-40	1	1,5 = RM05/RM05	A
							842-40	2	2,6 = RM05/RM05	A
							842-40	3	3,7 = RM05/RM05	A
07	O	O	O	C	C	C	823-05	0	0 = RM02	A
							823-10	1	1,5 = RM02/RM02	A
							823-19	2	2 = RM05	A
							842-40	3	3,7 = RM05/RM05	A
10	O	O	C	O	O	O	823-10	0	0,4 = RM02/RM02	A
							823-10	1	1,5 = RM02/RM02	A
							823-10	2	2,6 = RM02/RM02	A
							823-05	3	3 = RM02	A
11	O	O	C	O	O	C	842-40	0	0,4 = RM05/RM05	A
							842-40	1	1,5 = RM05/RM05	A
							842-40	2	2,6 = RM05/RM05	A
							823-19	3	3 = RM05	A

[1]PROM #897 requires Revision B or above firmware.

CONF. NO. 10	SW-3 5	 4	 3	 2	 1	PHYSICAL KEY	 Unit	LOGICAL Unit(s)= Dr Type	 Rev
12 O	O	C	O	C	O	823-19	0	0 = RM05	A
						823-19	1	1 = RM05	A
						823-19	2	2 = RM05	A
						823-19	3	3 = RM05	A
13 O	O	C	O	C	C	823-05	0	0 = RM02	A
						823-05	1	1 = RM02	A
						823-05	2	2 = RM02	A
						823-19	3	3 = RM05	A
14 O	O	C	C	O	O	823-05	0	0 = RM02	A
						823-05	1	1 = RM02	A
						823-19	2	2 = RM05	A
						823-19	3	3 = RM05	A
15 O	O	C	C	O	C	823-19	0	0 = RM05	A
						823-19	1	1 = RM05	A
						823-19	2	2 = RM05	A
						823-05	3	3 = RM02	A
16 O	O	C	C	C	O	1024-16	0	0 = RM05	A
						1024-16	1	1 = RM05	A
						1024-16	2	2 = RM05	A
						1024-16	3	3 = RM05	A
17 O	O	C	C	C	C	1024-16	0	0 = RM05	A
						1024-16	1	1 = RM05	A
						1024-16	2	2 = RM05	A
						823-19	3	3 = RM05	A
20 O	C	O	O	O	O	823-06	0	0,4 = RM03/RM02*	A
						823-06	1	1,5 = RM03/RM02*	A
						823-06	2	2,6 = RM03/RM02*	A
						823-19	3	3 = RM05	A
21 O	C	O	O	O	C	823-10	0	0,4 = RM02/RM02	A
						823-10	1	1,5 = RM02/RM02	A
						823-10	2	2,6 = RM02/RM02	A
						823-19	3	3 = RM05	A
22 O	C	O	O	C	O	823-19	0	0 = RM05	A
						823-06	1	1,5 = RM03/RM02*	A
						823-06	2	2,6 = RM03/RM02*	A
						823-19	3	3 = RM05	A
23 O	C	O	O	C	C	823-19	0	0 = RM05	A
						823-10	1	1,5 = RM02/RM02	A
						823-10	2	2,6 = RM02/RM02	A
						823-10	3	3,7 = RM02/RM02	A
24 O	C	O	C	O	O	589-07	0	0 = RM02	A
						589-07	1	1 = RM02	A
						589-07	2	2 = RM02	A
						589-07	3	3 = RM02	A
25 O	C	O	C	O	C	589-07	0	0 = RM02	A
						589-07	1	1 = RM02	A
						589-07	2	2 = RM02	A
						823-05	3	3 = RM02	A

TABLE A-2, cont.

CONF. NO.	SW-3 10	5	4	3	2	1	PHYSICAL KEY	Unit	LOGICAL Unit(s) = Dr Type	Rev
26	O	C	O	C	C	O	842-20	0	0 = RM02*	A
							842-20	1	1 = RM02*	A
							842-20	2	2 = RM02*	A
							842-20	3	3 = RM02*	A
27	O	C	O	C	C	C	842-20	0	0 = RM80*	A
							842-20	1	1 = RM80*	A
							842-20	2	2 = RM80*	A
							842-20	3	3 = RM80*	A
30	O	C	C	O	O	O	823-19	0	0 = RM05	A
							1124-30	1	1,5 = RM05/RM05	A
							1124-30	2	2,6 = RM05/RM05	A
							1124-30	3	3,7 = RM05/RM05	A
31	O	C	C	O	O	C	1124-30	0	0,4 = RM05/RM05	A
							1124-30	1	1,5 = RM05/RM05	A
							1124-30	2	2,6 = RM05/RM05	A
							1124-30	3	3,7 = RM05/RM05	A
32	O	C	C	O	C	O	1124-30	0	0,4 = RM05/RM05	A
							1124-30	1	1,5 = RM05/RM05	A
							1124-30	2	2,6 = RM05/RM05	A
							823-19	3	3 = RM05	A
33	O	C	C	O	C	C	823-19	0	0 = RM02*	A
							823-19	1	1 = RM02*	A
							823-19	2	2 = RM02*	A
							823-19	3	3 = RM02*	A
34	O	C	C	C	O	O	1645-05	0	0,4 = RM02/RM02	A
							1645-05	1	1,5 = RM02/RM02	A
							1645-05	2	2,6 = RM02/RM02	A
							1645-05	3	3,7 = RM02/RM02	A
35	O	C	C	C	O	C	823-05	0	0 = RM02	A
							1645-05	1	1,5 = RM02/RM02	A
							1645-05	2	2,6 = RM02/RM02	A
							1645-05	3	3,7 = RM02/RM02	A
36	O	C	C	C	C	O	1645-05	0	0,4 = RM02/RM02	A
							1645-05	1	1,5 = RM02/RM02	A
							1645-05	2	2,6 = RM02/RM02	A
							823-05	3	3 = RM02	A
37	O	C	C	C	C	C	561-03	0	0 = RM02*	A
							561-03	1	1 = RM02*	A
							561-03	2	2 = RM02*	A
							561-03	3	3 = RM02*	A
40	C	O	O	O	O	O	1024-16	0	0 = RM05*	A
							1024-16	1	1 = RM05*	A
							1024-16	2	2 = RM05*	A
							1024-16	3	3 = RM05*	A
41	C	O	O	O	O	C	842-20	0	0,4 = RP06/RP06	A
							842-20	1	1,5 = RP06/RP06	A
							842-20	2	2,6 = RP06/RP06	A
							842-20	3	3,7 = RP06/RP06	A

CONF. NO.	SW-3 10	5	4	3	2	1	PHYSICAL KEY	Unit	LOGICAL Unit(s) = Dr Type	Rev
42	C	O	O	O	C	O	842-20	0	0,4 = RP06/RP06	A
							842-20	1	1,5 = RP06/RP06	A
							842-20	2	2,6 = RP06/RP06	A
							823-05	3	3 = RM02	A
43	C	O	O	O	C	C	842-20	0	0,4 = RP06/RP06	A
							842-20	1	1,5 = RP06/RP06	A
							842-20	2	2,6 = RP06/RP06	A
							823-19	3	3 = RM05	A
44	C	O	O	C	O	O	842-20	0	0 = RP06*	A
							842-20	1	1 = RP06*	A
							842-20	2	2 = RP06*	A
							842-20	3	3 = RP06*	A
45	C	O	O	C	O	C	823-10	0	0 = RM02*	A
							823-10	1	1 = RM02*	A
							823-10	2	2 = RM02*	A
							823-10	3	3 = RM02*	A
46	C	O	O	C	C	O	823-10	0	0 = RM03*	A
							823-10	1	1 = RM03*	A
							823-10	2	2 = RM03*	A
							823-10	3	3 = RM03*	A
47	C	O	O	C	C	C	842-40	0	0 = RM05*	A
							842-40	1	1 = RM05*	A
							842-40	2	2 = RM05*	A
							842-40	3	3 = RM05*	A
50	C	O	C	O	O	O	700-12	0	0 = RM02*	A
							700-12	1	1 = RM02*	A
							700-12	2	2 = RM02*	A
							700-12	3	3 = RM02*	A
51	C	O	C	O	O	C	823-10	0	0 = RM80	A
							823-10	1	1 = RM80	A
							823-10	2	2 = RM80	A
							823-05	3	3 = RM02	A
52	C	O	C	O	C	O	842-20	0	0,4 = RP06/RP06	A
							842-20	1	1,5 = RP06/RP06	A
							842-20	2	2,6 = RP06/RP06	A
							819-19	3	3 = RP06	A
53	C	O	C	O	C	C	823-10	0	0,4 = RM03	B
							823-10	1	1,5 = RM03	B
							842-20	2	2,6 = RP06	B
							842-20	3	3,7 = RP06	B
54	C	O	C	C	O	O	823-10	0	0 = RM80	C
							823-10	1	1 = RM80	C
							823-10	2	2 = RM80	C
							823-10	3	3 = RM80	D

TABLE A-2, cont.

CONF. NO.	10	5	4	3	2	1	PHYSICAL KEY	UNIT	LOGICAL Units = Dr Type	Rev
55	C	O	C	C	O	C	842-20	0	0,4 = RP06/RP06	D
							842-20	1	1,5 = RP06/RP06	D
							819-19	2	2 = RP06	D
							819-19	3	3 = RP06	D
56	C	O	C	C	C	O	711-24	0	0 = RM05	D
							711-24	1	1 = RM05	D
							711-24	2	2 = RM05	D
							711-24	3	3 = RM05	D
57	C	O	C	C	C	C	711-24	0	0 = RM05	D
							711-24	1	1 = RM05	D
							711-24	2	2 = RM05	D
							823-19	3	3 = RM05	D
60	C	C	O	O	O	O	842-20	0	0,4 = RP06	E
							842-20	1	1,5 = RP06	E
							842-20	2	2,6 = RP06	E
							815-19	3	3 = RP06	E
61	C	C	O	O	O	C	760-19	0	0,4 = RP06/RP06*	F
							760-19	1	1,5 = RP06/RP06*	F
							760-19	2	2,6 = RP06/RP06*	F
							760-19	3	3,7 = RP06/RP06*	F
62	C	C	O	O	C	O	823-19	0	0 = RM05	G
							823-19	1	1 = RM05	G
							1024-16	2	2,6 = RM05/RM05	G
							1024-16	3	3,7 = RM05/RM05	G
63	C	C	O	O	C	C	1024-16	0	0,4 = RM05/RM05	G
							1024-16	1	1,5 = RM05/RM05	G
							823-19	2	2 = RM05	G
							823-19	3	3 = RM05	G
64	C	C	O	C	O	O	1024-16	0	0,4 = RM05/RM05	G
							1024-16	1	1,5 = RM05/RM05	G
							823-05	2	2 = RM03	G
							823-05	3	3 = RM03	G
65	C	C	O	C	O	C	823-05	0	0 = RM03	G
							823-05	1	1 = RM03	G
							1024-16	2	2,6 = RM05/RM05	G
							1024-16	3	3,7 = RM05/RM05	G
66	C	C	O	C	C	O	823-19	0	0 = RM05	G
							823-19	1	1 = RM05	G
							1024-16A	2	2,6 = RM05/RM05	G
							1024-16A	3	3,7 = RM05/RM05	G
67	C	C	O	C	C	C	1024-16A	0	0,4 = RM05/RM05	G
							1024-16A	1	1,5 = RM05/RM05	G
							823-19	2	2 = RM05	G
							823-19	3	3 = RM05	G

CONF. NO.	10	5	4	3	2	1	PHYSICAL KEY	UNIT	LOGICAL Unit(s) = Dr Type		Rev
70	C	C	C	O	O	O	823-05	0	0	= RM03	G
							823-05	1	1	= RM03	G
							1024-16A	2	2,6	= RM05/RM05	G
							1024-16A	3	3,7	= RM05/RM05	G
71	C	C	C	O	O	C	1024-16A	0	0,4	= RM05/RM05	G
							1024-16A	1	1,5	= RM05/RM05	G
							823-05	2	2	= RM03	G
							823-05	3	3	= RM03	G

*Non-Standard drive size. This size is not supported by DEC software or diagnostics. See the Table A-3 for actual size.

C = closed, O = open

TABLE A-3
NON-STANDARD DRIVE SIZES

Config.	Drive Type and Description
20	RM03 is 164 cylinders mapped on a 9448 cartridge
22	RM03 is 164 cylinders mapped on a 9448 cartridge
26	RM02 is a 20 track, 842 cylinder, 48 sector drive
27	RM80 is a 20 track, 842 cylinder, 48 sector drive
33	RM02 is a 19 track, 823 cylinder drive
37	RM02 is a 3 track, 561 cylinder drive
40	RM05 is a 16 track, 1024 cylinder drive
44	RP06 is a 19 track, 1772 cylinder drive
45	RM02 is a 5 track, 1646 cylinder drive
46	RM03 is a 5 track, 1646 cylinder drive
47	RM05 is a 19 track, 1684 cylinder drive
50	RM02 is a 12 track, 700 cylinder drive
61	RP06 is a 19 track, 760 cylinder, 31 sector drive
66	RM05 is a 16 track, 1024 cylinder, 42 sector drive
67	RM05 is a 16 track, 1024 cylinder, 42 sector drive
70	RM05 is a 16 track, 1024 cylinder, 42 sector drive
71	RM05 is a 16 track, 1024 cylinder, 42 sector drive

A.3 USER SELECTABLE OPTIONS

Several other options, including the register starting address for the SC31/BX can be user selected. The factory switch settings are listed in Table A-4. The functions of the switches that select those options are defined in Tables A-5, A-6, and A-7, below.

TABLE A-4
FACTORY SWITCH SETTINGS

SW1-1	OFF	SW2-1	OFF	SW3-1	OFF
SW1-2	OFF	SW2-2	OFF	SW3-2	OFF
SW1-3	OFF	SW2-3	OFF	SW3-3	OFF
SW1-4	OFF	SW2-4	OFF	SW3-4	OFF
		SW2-5	OFF	SW3-5	OFF
		SW2-6	OFF	SW3-6	ON
		SW2-7	OFF	SW3-7	OFF
		SW2-8	OFF	SW3-8	OFF
		SW2-9	OFF	SW3-9	OFF
		SW2-10	OFF	SW3-10	OFF

The factory switch settings enable a standard interrupt vector address of 254, a standard Unibus address of 776700 and drive configuration #00.

TABLE A-5
OPTION SWITCH SW1 SETTINGS

Switch	Open	Closed	Function
SW1-1	Run	Halt-Reset	Controller Run/Halt Reset
SW1-2			Not used[1]
SW1-3	Disable	Enable	2 RP06s mapped on 19-head drives[2]
SW1-4			Not used[1]

[1]All unused switches must be OFF.
[2]Requires Rev. E and above firmware. See paragraph 3.4.5.9.

TABLE A-6
OPTION SWITCH SW2 SETTINGS

Switch	Open	Closed	Function
SW2-1			Interrupt vector select #1[1]
SW2-2			Interrupt vector select #2[1]
SW2-3			Interrupt vector select #3[1]
SW2-4	Disable	Enable	Swap logical units 0-3 with 4-7

TABLE A-6
OPTION SWITCH SW2 SETTINGS

Switch	Open	Closed	Function
SW2-5	Disable	Enable	Replacement track mode (RP units only)[2,6]
SW2-6	Disable	Enable	Dual port mode[6]
SW2-7	Disable	Enable	DMA bandwidth control[3,6]
SW2-8	B Cable	A Cable	Sector and index signals[6]
SW2-9	Disable	Enable	Dual access mode[4,6]
SW2-10	1:1	2:1	Sector interleave[5,6]

[1]See paragraph 3.4.2.

[2]Requires custom user formatter. Will fail DEC formatter.

[3]See paragraph 5.5.1.

[4]See paragraph 2.6.7.

[5]Requires an even number of sectors per track.

[6]Will fail some subtests in Functional diagnostics if enabled.

TABLE A-7
OPTION SWITCH SW3 SETTINGS

Switch	Open	Closed	Function
SW3-1			Drive configuration[1]
SW3-2			Drive configuration[1]
SW3-3			Drive configuration[1]
SW3-4			Drive configuration[1]
SW3-5			Drive configuration[1]
SW3-6		776700	Controller address (Standard)
SW3-7		776300	Controller address (Alternate)
SW3-8		776600	Controller address (Alternate)
SW3-9		776400	Controller address (Alternate)
SW3-10			Drive configuration[1]

[1]See Table A-2.

BLANK

APPENDIX B

DRIVE MODIFICATIONS

This appendix provides modifications to commonly used drives for moving the Sector and Index signals from the A Cable to the B Cable.

B.1 CDC 9766

Remove (Ch. I)		Remove (Ch. II)	
Sector +	J4-55	Sector +	J4-55
Sector -	J4-25	Sector -	J4-25
Index +	J4-48	Index +	J4-48
Index -	J4-18	Index -	J4-18

Move Wire (Ch. I)	Orgin	From	To
Sector +	PA01-5B	J3-55	J2-26
Sector -	PA01-5A	J3-25	J2-13
Index +	PA01-6B	J3-48	J2-24
Index -	PA01-6A	J3-18	J2-12

Move Wire (Ch. II)	Orgin	From	To
Sector +	PA03-5B	J3-55	J2-26
Sector -	PA03-5A	J3-25	J2-13
Index +	PA03-6B	J3-48	J2-24
Index -	PA03-6A	J3-18	J2-12

Rework transmitter card FTVV in location A01 (Ch. I) and A03 (Ch. II). Locate the jumper at center bottom of board (as viewed with connector on the right). Remove jumper and reinsert one set of holes lower (i.e., from center hole to hole below original jumper). Remove the letter "F" from the card type designation FTVV and mark "G" in its place so that the card type becomes GTVV.

NOTE - On later models of the 9766, CDC will ship units with an enhancement feature which will allow easy switchover to the B Cable as follows: Cut the cable tie securing PD90 to the I/O cable and plug PD90 into JD90 pins 13 and 14 (Ch. I) and pins 11 and 12 (Ch. II) as indicated on the top of the connector.

B.2 TRIDENT DRIVES

Sector and Index are on both the A and B Cables.

B.3 FUJITSU DRIVES

Sector and Index are on both the A and B Cables.

B.4 CDC 9775

Rework transmitter-receiver card CFAX in location A04 (Ch. I) and B04 (Ch. II). When viewing card with connector on the right, locate four jumpers to the left of the I/O connectors and above the terminator ground lug. The bottom end of the jumpers must be removed from the holes to which they are soldered and moved to the holes immediately above. Next, find the small jumper to the right of the third IC from the connector edge of the board on the bottom row of ICs. This jumper must be removed and reinserted so that it connects the top and middle holes rather than the original connection of the bottom and middle. This connection ungates the sector and index driver.

Remove the letter "C" from the card type designation CFAX and mark a "D" in its place so that the card type becomes DFAX.

B.5 CDC 9762

Remove (Ch. I)	Add (Ch. I)
B01-06B to JA82-18B	B01-06B to JA82-43B
B01-06A to JA82-18A	B01-06A to JA82-44A
B01-05B to JA82-25B	B01-05B to JA82-45B
B01-05A to JA82-25A	B01-05A to JA82-45A

Remove (Ch. II)	Add (Ch. II)
B03-06B to JA83-18B	B03-06B to JA83-43B
B03-06A to JA83-18A	B03-06A to JA83-44A
B03-05B to JA83-25B	B03-05B to JA83-45B
B03-05A to JA83-25A	B03-05A to JA83-45A

Rework transmitter card FTVV in location B01 (Ch. I) and B03 (Ch. II). Locate jumper at center bottom of board (as viewed with connector on the right). Remove jumper and reinsert one set of holes lower (i.e., from center hole to hole below original jumper). Remove the letter "F" from the card type designation FTVV and mark a "G" in its place so that the card type becomes GTVV.

NOTE - On later models of the 9775, CDC will ship units with an enhancement feature which will allow easy switchover to the B Cable as follows: Remove the jumper plug on (B07) of the logic chassis backpanel.

B.6 CDC 9730

Rework transmitter-receiver card CFAX in location A04 (Ch. I) and B04 (Ch. II). When viewing card with connector on the right, locate four jumpers to the left of the I/O connectors and above the terminator ground lug. The bottom end of the jumpers must be removed from the holes to which they are soldered and moved to the holes immediately above. Next, find the small jumper to the right of the third IC from the connector edge of the board on the bottom row of ICs. This jumper must be removed and reinserted so that it connects the top and middle holes rather than the original connection of the bottom and middle. This connection ungates the sector and index driver.

Remove the letter "C" from the card type designation CFAX and mark a "D" in its place so that the card type becomes DFAX.

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APPENDIX C

EMULEX MODIFICATIONS TO DEC RM02 DIAGNOSTICS

This appendix describes the modifications required in the Digital
Equipment Corporation RM02/RM03 diagnostics to run on the Emulex
SC31/BX and other controllers in self-sizing mode. Once modified,
these diagnostics will run on any current and future configurations
of this emulation.

Part one includes all known programming errors, and all
modifications required to bypass unsupported portions of the DEC
maintenance mode. Part two describes the self-sizing
modifications.

C.1 CZRMJB0 - RM03/RM02 DISKLESS DIAGNOSTIC

Product Code: AC-B018B-MC

This diagnostic runs exclusively in Maintenance mode. Since only a
subset of the RM02 Maintenance mode features are emulated in the
Emulex controller, this diagnostic is not run.

C.2 CZRMCB0 - RM03/RM02 FUNCTIONAL TEST - PART 1

Product Code: AC-A9997B-MC

MODIFICATIONS (Part 1)

Item	Location	From	To
1.	25024, 25026	4737, 43216	137,25622
2.	10730	40001	0
3.	13062	1012	412
4.	26600	1007	407
5.	27014	1011	411
6.	35570	1406	406
7.	45152	4	10
8.	60000	7	1405
9.	66074	13746	12746
10.	10356-10362	5007, 110102, 1	11102, 105002, 240

Item	Explanation

1. This modification bypasses an OPI test to comply with DEC
   hardware ECOs #7684-0004, 7684-0007, 7684-0009.

2. This modification is only required on very fast processors.
   It changes a Drive Clear test to run in Normal mode instead
   of Maintenance mode.

3. This modification bypasses a "lost of bit clock" test which is run in Maintenance mode.

4. This modification bypasses an "RMR" test which, as written, can only be run in Maintenance mode.

5. This modification bypasses a Massbus Parity Error test. Since there is no massbus on the Emulex controller, there is no massbus parity to test.

6. This modification bypasses a test of the RMLA register that is done in 18-bit mode.

7-10. Unidentified program bugs.

MODIFICATIONS (Part 2)

Location	From			To		
7634	24024			20024		
7654	24025			20027		
7732-7734	12706, 1100			4737, 104106		
27500-27502	12737, 1466			13737, 104400		
30522-30524	22726, 1000			23726, 104400		
31372-31374	12737, 1466			13737, 104400		
32022-32024	12737, 1466			13737, 104400		
32240-32242	22737, 1466			23737, 104400		
32730-32732	12737, 2400			13737, 104410		
33224	3400			37400		
33250-33252	12737, 2400			13737, 104410		
33344-33346	12737, 1467			13737, 104402		
33636	2000			4000		
33662-33664	12737, 1467			13737, 104402		
36364	633			40		
36370	634			41		
36754	634			40		
36760	633			41		
37436-37440	12737, 2400			13737, 104410		
37700	4000			40000		
37724-37726	12737, 2400			13737, 104410		
40032-40034	12737, 1467			13737, 104402		
40304	2000			4000		
40330-40332	12737, 1467			13737, 104402		
51114	177770			177700		
51134-51140	23727, 51702, 240			23737, 51702, 104412		
51150-51152	162737, 5			163737, 104412		
51224-51226	22737, 1467			23737, 104402		
51340-51342	22737, 1467			23737, 104402		
51600	176000			170000		
52236-52242	23727, 1432, 1466			23737, 1432, 104400		
52304-52310	123727, 1405, 4			123737, 1405, 104404		
57730-57736	23727, 1432, 1466			23737, 1432, 104400		
57776-60002	123727, 7, 4			123737, 1405, 104404		

The following subroutine must be inserted where indicated. The previous contents of the locations should all be zeros.

Locations: 104106-104174

Contents: 13700, 1276, 062700, 36, 12701, 104400, 12710, 100027,
              11021, 11011, 5221, 12710, 100030, 11021, 11011, 5221,
              105021, 116121, 177775, 12710, 100036, 16100, 177776,
              6200, 6200, 6200, 10011, 207.

C.3   CZRMDB0 – RM03/RM02 FUNCTIONAL TEST – PART 2

Product Code: AC-B000B-MC

MODIFICATIONS (Part 1)

Item	Location	From	To
1.	40452	4	10
2.	63360	13746	12746

Both of the above modifications correct unidentified program bugs.

MODIFICATIONS (Part 2)

Location	From	To
7656	24024	20024
7674	24025	20027
7732-7734	12700, 1100	4737, 101550
17514-17516	12737, 2037	13737, 102514
20374-20376	12737, 1466	13737, 102500
22272-22274	22737, 2000	23737, 102506
22300	103402	101402
23014-23016	22737, 1466	23737, 102500
23076-23100	12737, 1466	13737, 102500
23104-23106	12737, 2037	13737, 102514
23374-23376	12737, 1466	13737, 102500
23402-23404	12737, 2037	13737, 102514
24406-24410	12737, 2400	13737, 102510
25066	3400	37400
25126-25130	12737, 1467	13737, 102502
25614	1777	3777
34714	5737	0
36766-36770	122763, 4	123763, 102504
44414	177770	177700
44434-44440	23727, 45202, 240	23737, 45202, 102512
44450-44452	162737, 240	163737, 102512
44474-44500	23727, 45200, 5	23737, 45200, 102506
44510-44512	162737, 5	163737, 102506
44524-44526	22737, 1467	23737, 102502

```
44640-44642    22737, 1467           23737, 102502
45100          176000                170000
45536-45542    23727, 1434, 1466     23737, 1434, 102500
45604-45610    123727, 1407, 4       123737, 1407, 102506
53764-53766    22737, 1466           23737, 102500
54002-54004    122737, 4             123737, 102504
```

The following subroutine must be inserted where indicated. The previous contents of the locations should be all zeros.

Location: 101550-10646

Contents: 13700, 1276, 62700, 36, 12701, 102500, 12710, 100027,
             11021, 11011, 5221, 12710, 100030, 11021, 11011, 5221,
             105021, 116121, 177775, 12710, 100036, 16100, 177776,
             6200, 6200, 6200, 10021, 112721, 37, 116111, 177767,
             207.

C.4   CZRMEB0 - RM03/RM02 FUNCTIONAL TEST - PART 3

Product Code: AC-B003B-MC

MODIFICATIONS (Part 1)

Item	Location	From	To
1.	31032	42702	52702
2.	30070, 30072	404, 240	402, 0
	30076,30100	137, 30470	5237, 1336
3.	30416, 30420,	404, 240	402, 0
	30424, 30426	137, 30470	5237, 1336
4.	44472	4	10
5.	67364	13746	12746

Item	Explanation

1. This modification reverses a DEC patch that eliminated Bus-Address-Increment-Inhibit mode in a Write test. The DEC controller gets Data Late errors in this mode. The Emulex controllers do not.

2. This modification increments the saved contents of RMDA after attempting a write with the ERR bit in RMDS set. The DEC controller increments RMDA during the illegal attempt. Emulex controllers do not. The modification allows a subroutine to pass the test.

3. Same as Item 2, except that this is for an attempted Read with ERR set.

4-5. Unidentified program bugs.

MODIFICATIONS (Part 2)

Location	From	To
7632	24024	20024
7652	24025	20027
7706-7710	12706, 1100	4737, 111760
20040-20042	12737, 1466	13737, 112100
20444-20442	12737, 1466	13737, 112100
22076-22100	12737, 2037	13737, 112114
32604-32610	23727, 1434, 1400	23737, 1434, 112100
32710-32712	12737, 2037	13737, 112114
36722-36724	22737, 2037	23737, 112114
41000-41002	12737, 2000	13737, 112116
41006-41010	12737, 1466	13737, 112100
42012-42014	12737, 2012	13737, 112120
42426-42430	112737, 4	123737, 112104
42446-42450	22737, 1466	23737, 112100
42516-42520	122737, 4	123737, 112104
42536-42540	22737, 1466	23737, 112100
43006-43010	122763, 4	123763, 112104
50434	177770	177700
50454-50460	23727, 51222, 240	23737, 51222, 112112
50470-50472	162737, 240	163737, 112112
50514-50520	23727, 51220, 5	23737, 51220, 112106
50530-50532	162737, 5	163737, 112106
50544-50546	22737, 1467	23737, 112102
50660-50662	22737, 1467	23737, 112102
51120	176000	170000
51556-51562	23727, 1434, 1466	23737, 1434, 112100
51624-51630	123727, 1407, 4	123737, 1407, 112104
60004-60006	22737, 1466	23737, 112100
60022-60024	122737, 4	123737, 112104

The following subroutine must be added to the test at:

Locations: 111760-112052

Contents: 13700, 1276, 62700, 36, 12701, 112100, 12710, 100027,
            11021, 11011, 5221, 12710, 100030, 11021, 11011, 5221,
            105021, 116121, 177775, 12710, 100036, 16100, 177776,
            6200, 6200, 6200, 10021, 112721, 37, 116121, 177767,
            105021, 116121, 177776, 112721, 12, 116111, 177776,
            207.

C.5 CZRMFB0 - RM03/RM02 EXTENDED DRIVE TEST

Product Code: AC-B0006B-MC

MODIFICATIONS (Part 1)

Item	Location	From	To
1.	21464	13746	12746
2.	27722-27726	5737, 4322, 1011	32737, 100000, 4350
	27730-27734	32737, 100000, 4350	1405, 12737, 177777
	27736-27742	1405, 12737, 177777	1446, 137, 30370
	27744-27750	1446, 137, 30370	5737, 4322, 1401
3.	37246	1750	1503
4.	37604	10164	110164
5.	41674	10164	110164
6.	43064-43066	5702, 1426	4737, 44770
	43070-43072	4737, 44770	5702, 1424

All of the above are unidentified program bugs.

MODIFICATIONS (Part 2)

*Note: Required only on drives of less than 100 logical cylinders.

Location	From	To
1774	400	1466
2040	400	1466
2176	144	100*
37270-37272	22705, 20024	122705, 24
37276-37300	22705, 24024	122705, 27
37312-37314	22705, 20025	122705, 25
37320-37322	22705, 24025	122705, 25
17574-17576	20127, 1466	20137, 1574
17602-17604	20227, 4	20237, 1602
17022-17026	22700, 5, 3365	23700, 1602, 2365
17222-17224	122737, 4	123737, 1602
20312-20314	122737, 5	123737, 1602
20320	3370	2370
33530-33534	122702, 5, 3003	123702, 1602, 2003

The following subroutine must be inserted where indicated.   It replaces an existing subroutine of similar function that is no longer needed.   The contents of the existing routine are not shown.

Locations: 26632-27004

Contents: 104412, 113704, 1102, 6304, 16401, 1620, 13704, 1450,
             62704, 36, 12702, 1566, 5003, 12122, 6237, 1566,
             103002, 12122, 401, 5022, 5203, 20327, 14, 1405, 20327,
             3, 1363, 24242, 761, 12714, 100027, 11405, 12703, 1574,
             5713, 1412, 21327, 1466, 1407, 21327, 1465, 1002, 5305,
             402, 20513, 2001, 10513, 12714, 100030, 11437, 1602,
             104413, 207.

C.6 CZRMIB0 - RM03/RM02 DRIVE COMPATIBILITY TEST

Product Code: AC-B015B-MC

MODIFICATIONS (Part 1)

Item	Location	From	To
1.	21000	13746	12746

The above item is an unidentified program bug.

There are no Part 2 modifications to this test. It is impractical
to rewrite this test. To do so would require allocating an
indeterminate amount of buffer space near the beginning of the
test. The test uses cylinders 0-800 (but not all of them), and
tracks 0-4. Any configuration with 801 or more cylinders and 5 or
more tracks is compatible with this test.

C.7 CZRMAC0 - RM03/RM02 FORMATTER

Product Code: AC-9252C-MC

MODIFICATIONS (Part 1)

Item	Location	From	To
1.	12632	10011	1
2.	23630	13746	12746
3.	27154	1750	1503
4.	27512	10164	110164
5.	31602	10164	110164
6.	32772-32774	5702, 1426	4737, 34676
	32776-33000	4737, 34676	5702, 1424

Item	Explanation
1.	This modification alters the number of tracks that must be formatted before a bad sector file can be written. Since the format OP code does not write a bad sector file, and since the Performance Exerciser will not run without one, this modification allows any size Format or Verify to create a bad sector file. If the number is not altered, then the entire pack must be formatted before a bad sector file can be written.

2-6. Unidentified program bugs.

MODIFICATIONS (Part 2)

Location	From	To
30044	4037	406
11260-11262	112737, 4	113737, 31472
11266-11270	12737, 1466	13737, 31470
11510-11512	22737, 151466	23737, 31466
11520-11522	22737, 2000	23737, 31464
12530-12532	12702, 1466	13702, 31470
12560-12562	12737, 5	13737, 5660
12612-12614	62737, 5	63737, 5660
15200-15202	22737, 1466	23737, 31470
15210-15212	122737, 4	123737, 31472
15402-15404	12737, 1466	12737, 31470
15410-15412	112737, 4	113737, 31472
16410-16412	22737, 4	23737, 31472
16430-16432	22737, 1466	23737, 31470
16440-16442	122737, 4	123737, 31472
16502-16504	22737, 1467	23737, 5652
20070-20072	12737, 1466	13737, 31470
20076-20100	12737, 4	13737, 31472
27176-27200	22705, 20024	122705, 24
27204-27206	22705, 24024	122705, 27
27220-27222	22705, 20025	122705, 25
27226-27230	22705, 24025	122705, 25
10734-10740	12737, 1466, 1320	104412, 13703, 26644
10742-10746	132762, 3, 26526	13702, 1220, 10263
10750-10752	1003, 12737	10, 4737
10754-10756	1466, 1320	31320, 104413

The following subroutine must be inserted where indicated. It
replaces a rotational position-sensing routine that the formatter
does not need, since it only formats one drive at a time. The
contents of the existing routine are not shown.

Locations: 31320-31452

Contents: 62703, 36, 12713, 100027, 11304, 12713, 100030, 11305,
           12713, 100036, 10437, 1320, 10537, 1324, 12703, 31464,
           105023, 110523, 10413, 52723, 150000, 10423, 10523,
           5204, 5205, 10437, 5652, 10537, 5660, 10437, 5666,
           10537, 5674, 10437, 5704, 10537, 5712, 10437, 5730,
           10537, 5736, 10437, 5754, 10537, 5762, 207.

C.8 CZRMBB0 - RM03/RM02 PERFORMANCE EXERCISER

Product Code: AC-A994B-MC

MODIFICATIONS (Part 1)

Item	Location	From	To
1.	11134-11136	400, 46116	100000, 46144
2.	32144	13746	12746
3.	35130	1750	1503
4.	35466	10164	110164
5.	37556	10164	110164
6.	41036-41040	5702, 1426	4737, 34676
	41042-41044	4737, 34676	5702, 1424

All of the above items are unidentified program bugs.

MODIFICATIONS (Part 2)

Location	From	To
4440	57512	60410
4472	57512	60410
6364-6366	22760, 1465	26060, 106
13534-13540	123727, 1415, 5	240, 4737, 60304
13554-13560	23727, 1412, 151466	240, 4737, 60230
16654-16656	62705, 5	66005, 112
16672-16676	20527, 4, 101402	26005, 112, 3002
16700-16702	162705, 5	16005, 112
22614-22616	112766, 4	116066, 112
25442-25446	10004, 62704, 2	10046, 4737, 60064
25664	12737	402
25762-25764	16403, 55252	4737, 60206
26214-26220	12737, 1466, 40674	240, 4737, 60262
26222-26226	112737, 4, 46073	240, 4737, 60326
35152-35154	22705, 20024	122705, 24
35160-35162	22705, 24024	122705, 27
35174-35176	22705, 20025	122705, 25
35202-35204	22705, 24025	122705, 25

The following subroutine must be added to the end of the program at the indicated locations.

Locations: 60064-60204

Contents: 10146, 111001, 13704, 34620, 4037, 35050, 401, 403,
             105761, 34512, 1375, 105761, 34472, 3424, 62704, 36,
             6301, 6301, 62701, 60350, 12714, 100027, 11421, 11400,
             5300, 10037, 1446, 12714, 100030, 11421, 11437, 1444,
             12714, 100036, 12601, 16604, 2, 12600, 62704, 2, 200.

Locations: 60206-60346

Contents: 16403, 55252, 13763, 1444, 16, 13763, 1444, 24, 207,
              5046, 111016, 6316, 6316, 67716, 60350, 13646, 52716,
              150000, 5216, 22637, 1412, 207, 5046, 111016, 6316,
              6316, 62716, 60350, 13637, 46074, 207, 5046, 111016,
              6316, 6316, 62716, 60352, 123637, 1415, 207, 5046,
              111016, 6316, 6316, 62716, 60352, 113637, 46073, 207.

Those users running on drives with more than 80 Mb capacity will
require the following patches. The Performance Exerciser limits
the number of allowable bad sectors on any drive to 16, even though
the Bad Sector File can handle 126. The following patches allow
the program to run with 126 bad sectors or less. The first two
patches move the base address of the buffer. These locations have
already been patched, and the "from" column reflects those patches.

Location	From	To
4440	60410	70410
4472	60410	70410
17202	20	176
17206	62702	16002
20274	12701	16001
20300	60001	240
20304	20	176
25504	14	22
25510	162	154
25716	122	126
26166	62701	16001
26174	40	400
26344	62701	16001
26352	40	400
43146	0	60410
43452	0	61410
43756	0	62410
44262	0	63410
44566	0	64410
45072	0	65410
45376	0	66410
45702	0	67410

C.9   CZRMGB0 - RM03/RM02 DUAL PORT LOGIC TEST - PART 1

Product Code: AC-B009B-MC

See note under Dual Port Logic Test - Part II.

C.10   CZRMHB0 - RM0

Product Code: AC-B012B-MC

Neither Dual Port Logic Test can be run. They require that the
drive under test be tied to a single controller via a special cable
from the second port, and that the drive have a "neutral" position.

The neutral position allows any asynchronous request via either port to immediately seize the drive without having to wait for it. This controller does not have the ability to examine any drive at any given moment since only one drive can be addressed at a time via the A Cable. Therefore, with this controller, a "neutral" position must appear as a "busy" to both controllers. The lack of an immediately seizable state will cause errors in almost all of the subtests in each of the dual controller logic diagnostics.

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Appendix D

Modifications to DEC RP06 Diagnostics

This appendix describes the modifications required in the Digital
Equipment Corporation RP06 diagnostics to run on the Emulex model
SC31/BX Controller.

The modifications are in two parts. Part one contains
modifications that correct program errors and bypass unsupported
features, such as diagnostic mode. Part two contains modifications
to change the number of cylinders from 815 to some other value.

Users running on LSI-11 systems without 4 levels interrupt and
explicit Processor Status Word (PSW) addressing will require ECO
#254 for additional PSW patches.

D.1   CZRJGB0   =   RP04/5/6 Diskless Controller Test - Part 1

      Product Code: AC-9208B-MC

                    MODIFICATIONS (Part 1)

Item   Location   From   To

  1.   5714, 5716   5737, 1700   5777, 173760
  2.   10776   4537   406
  3.   11052, 11062   104200, 104200   4200, 4200
  4.   11140, 11150   10, 10   0, 0
  5.   11310, 11330   1642, 176714   1632, 176702
  6.   11364, 11400   5, 401   1, 1
  7.   11542, 11560, 11562 1644, 17437, 176706   1634, 177776, 176704
  8.   11620   4037   474
  9.   12564   177777   0
 10.   12734, 12746   4276, 4276   4200, 4200
 11.   13010, 13022   17437, 17437   0, 0
 12.   13064, 13076   116000, 116000   16000, 16000
 13.   13664   17437   0
 14.   14004   4276   4200
 15.   14022   116000   16000
 16.   14202, 14204   4737, 42614   137, 15444
 17.   16352, 16354   12706, 1000   137, 41064
 18.   12520   177777   175777

   Item   Explanation

    1. This modification fixes an unidentified program error. The
        purpose of the instruction is to test for the presence of
        an RH70 controller vs. an RH11 controller. It does this by
        testing for the existence of an RH70 register whose address
        is in location 1700_8. As written, however, the program
        checks for the existence of location 1700_8, not the

existence of the location whose address is in 1700_8. This fix corrects the instruction.

2. This modification branches around a portion of the test that only works in maintenance mode.

3-7. These modifications alter bits in the expected results of certain registers, after various register operations, to reflect their expected status when the controller is not in maintenance mode.

8. This modification branches around a portion of the test that can only be run in maintenance mode.

9-15. Same as modification 3-7.

16-17. These modifications jump around maintenance mode read/write tests. These tests can only be run in maintenance mode.

18. Allow for either a 10-bit or 11-bit cylinder address register.

NOTE: This test assumes that the controller is being tested after a system power-up. Certain registers which are not cleared by a Bus Init are assumed to be zeroed, as would be the case on a power-up.

There are no part two modifications to this diagnostic.

D.2 CZRJHB0 = RP04/5/6 Diskless Controller Test - Part 2

Product Code: AC-9213B-MC

MODIFICATIONS (Part 1)

Item	Location	From	To
1.	21250, 21252	5737, 15020	5777, 173544
2.	24170	15010	15014
3.	26756	177677	175777
4.	30650, 30652	4037, 45702	137, 44132
5.	30646	31154	44132

Item   Explanation

1. This is an unidentified program error. It is exactly the same error as outlined in Modification 1 of the Diskless Controller Test - Part 1.

2. This modification corrects a program error to ensure that all of the controller registers are tested.

3. This modification corrects a program error to test the status of the PSEL bit (the bit under test) instead of the IE bit (which is not under test).

4-5. These modifications jump around those data I/O tests that can only be run in maintenance mode.

There are no part two modifications to this diagnostic.

D.3 CZRJIB0 - RP04/5/6 Functional Controller Test - Part 1

Product Code: AC-9218B-MC

MODIFICATIONS (Part 1)

Item	Location	From	To
1.	6526, 6530	5737, 2340	5777, 173606
2.	12744	1005	1003
3.	17732, 20410	30500, 30500	10500, 10500
4.	21344, 21474	20400, 20400	400, 400
5.	22430, 22724	30500, 30500	10500, 10500
6.	23014	116000	16000
7.	33656, 34356	30500, 30500	10500, 10500
8.	41210-41216	240, 240, 240, 240	32777, 200 141104, 1774
9.	42300-42304	240, 32777, 100	4737, 400, 30377
	400-406	402, 0, 406, 0	12703, 100, 5303
	410-414	412, 0, 416	1376, 12703 100, 207
10.	15472	177777	157777
11.	15506	177777	175777

Item	Explanation

1. This is an unidentified program error. It is the same error that is outlined in Modification 1 of the Diskless Controller Test - Part 1.

2. This modification changes a branch to bypass a maintenance mode test.

3-5. These modifications remove the "PIP" bit from a test of RPDS. The "PIP" bit will set during these tests, but not as quickly as in the DEC controller.

6. This test removes the sign change bit from a test of RPOF. Since there is no hardware signal from a storage module drive available to the controller to indicate a phase change in the PLO, this bit is not implemented.

7. Same as modifications 3-5.

8. This modification changes a maintenance mode seek to a normal seek.

9. This modification inserts a timeout loop into the program between the loop that waits on some bit becoming set and the routine that tests for IE equals zero, thus indicating that the interrupt occurred and was serviced. This same timeout loop exists in Part 2 of the functional test. The use of maintenance mode in certain parts of this test may have eliminated the need for the timeout in this test.

10. Allows for either a 5-bit or a 6-bit track address register.

11. Allows for either a 10-bit or an 11-bit cylinder address register

There are no part three modifications to this diagnostic.

D.4 <u>CZRJJB0</u> <u>-</u> <u>RP04/5/6 Functional Controller Test - Part 2</u>

Product Code: AC-9223B-MC

MODIFICATIONS (Part 1)

Item	Location	From	To
1.	6412, 6414	5737, 2240	5777, 173622
2.	15342, 15352	177702, 2410	177672, 2370
3.	15366, 15370	200,0	0, 1
4.	15404, 15414, 15430	177774, 2574, 200	177672, 2370, 0
5.	21446, 21456, 21512	3402, 0, 200	3400, 177777, 0
6.	23132, 23142	177502, 2574	177400, 2370
7.	23110, 23120	177410, 2410	177400, 2370
8.	26622, 26630	204, 102, 1200	0, 0, 1000, 0
	26636, 26644	100	
9.	26706, 26714, 26734	2164, 177774, 100	2370, 177672, 0
10.	27366, 27270	13700, 2270	137, 27646
11.	33566	25	1000

Item	Explanation
1.	This is an unidentified program error. It is the same error that is outlined in Modification 1 of the Diskless Controller Test - Part 1.
2-4.	These modifications alter the expected contents of RPBA/RMBA, RPWC/RMWC, and the IR and OR bits in RPCS2/RMCS2 at the completion of an aborted write test to compensate for the lack of a SILO buffer. This controller does not alter the values of those registers if the write command cannot be done. The DEC controller does.
5-9.	Same as 2-4 above.

10. This modification jumps around a maintenance mode test.

11. This modification increases a stall timer to compensate for the delay between the detection of an error and the setting of the interrupt. This modification is required on processors with cache memory.

MODIFICATIONS - Part 2

Location	From	To
11706	11456	10000+C-1
11770	1456	C-1
12256	1456	C-1
17366	11457	10000+C
17444	1457	C
21156	11456	10000+C-1
21240	11457	10000+C
21316	1456	C-1
21576	1457	C
21606	1456	C-1
21704	11456	10000+C-1
22012	1456	C-1
22244	1457	C

NOTE: "C" = #Logical cylinders per drive

D.5 **DZRJA-B-D** = **RP04/5/6 Mechanical and Read-Write Test**

Product Code: MAINDEC-11-DZRJA-A-D

MODIFICATIONS Part 2

All of the following locations are changed from '1456' to 'C-1':

1614, 1616, 1620, 1672, 1740, 2004, 2026, 2050, 2072, 2112, 2132, 2170, 2220, 2260, 2312, 2336, 2404, 2450, 2472, 2514, 2536, 2556, 2576, 2634, 2664, 2724, 2756.

D.6 **CZRJBB0** = **RP04/5/6 Formatter Program**

Product Code: AC-9185B-MC

MODIFICATIONS - Part 2

Location	From	To
3352	1456	C-1

D.7 **CZRJDC0** = **RP04/5/6 Multidrive Exerciser**

Product Code: AC-9195C-MC

MODIFICATIONS - Part 2

Location	From	To
16676	1457	C
25504	1456	C-1

D.8   CZRJCB0   =   RP04/5/6 Head Alignment Program

   Product Code: AC-9190B-MC

This test is not run. The test is designed to use the hardware and
25 microinch steps in the DEC drives to find the point at which the
head crosses the center of the recorded track. Storage module
drives do not have a signal available to the controller that would
allow the detection of the cross-over point, as they have only a
+/-400 microinch offset from nominal.

D.9   CZRJEB0   =   RP04/5/6 Dual Controller Logic Test - Part 1

   Product Code: AC-9200B-MC

See note under section D.10.

D.10   DZRJF-A-D   =   RP04/5/6 Dual Controller Logic Test - Part 2

   Product Code: MAINDEC-11-DZRJF-A-D

Neither of these two tests can be run. They require that the drive
under test be tied to a single controller via a special cable from
the second port, and that the drive have a "neutral" position. The
neutral position allows any asynchronous request via either port to
immediately seize the drive without having to wait for it. This
controller does not have the ability to examine any drive at any
given moment since only one drive can be addressed at a time via
the A-cable. The "busy" signal is a function of the addressed
drive. Therefore, with this controller a "neutral" position must
appear as a "busy" to both controllers. The differences are enough
that the lack of an immediate seizable state will cause errors in
almost all of the sub-tests in each of the dual controller logic
diagnostics.