SECTION II
INSTRUCTION FLOW CHARTS

The Instruction Flow Charts in this section indicate the active control signals and the resulting data flow paths for individual steps in the execution of each MP12 instruction. A simplified block diagram is used to indicate the data flow paths and major units involved in the execution of each instruction.

Control signals referenced by the Instruction Flow Charts are listed on the next page with a cross-reference to the page number in the schematic diagram section where the signal originates.

A special feature of the MP12 permits the processor to execute a single instruction repeatedly for diagnostic purposes. The Instruction Flow Charts can then be used to verify processor operation at the instruction level. The procedure for using this feature is as follows:

1. Place the processor on the extender card and apply power to the system.

2. Toggle the Reset switch.

3. Place the Display switch in the AC position.

4. Enter the instruction to be executed into the Switch Register.

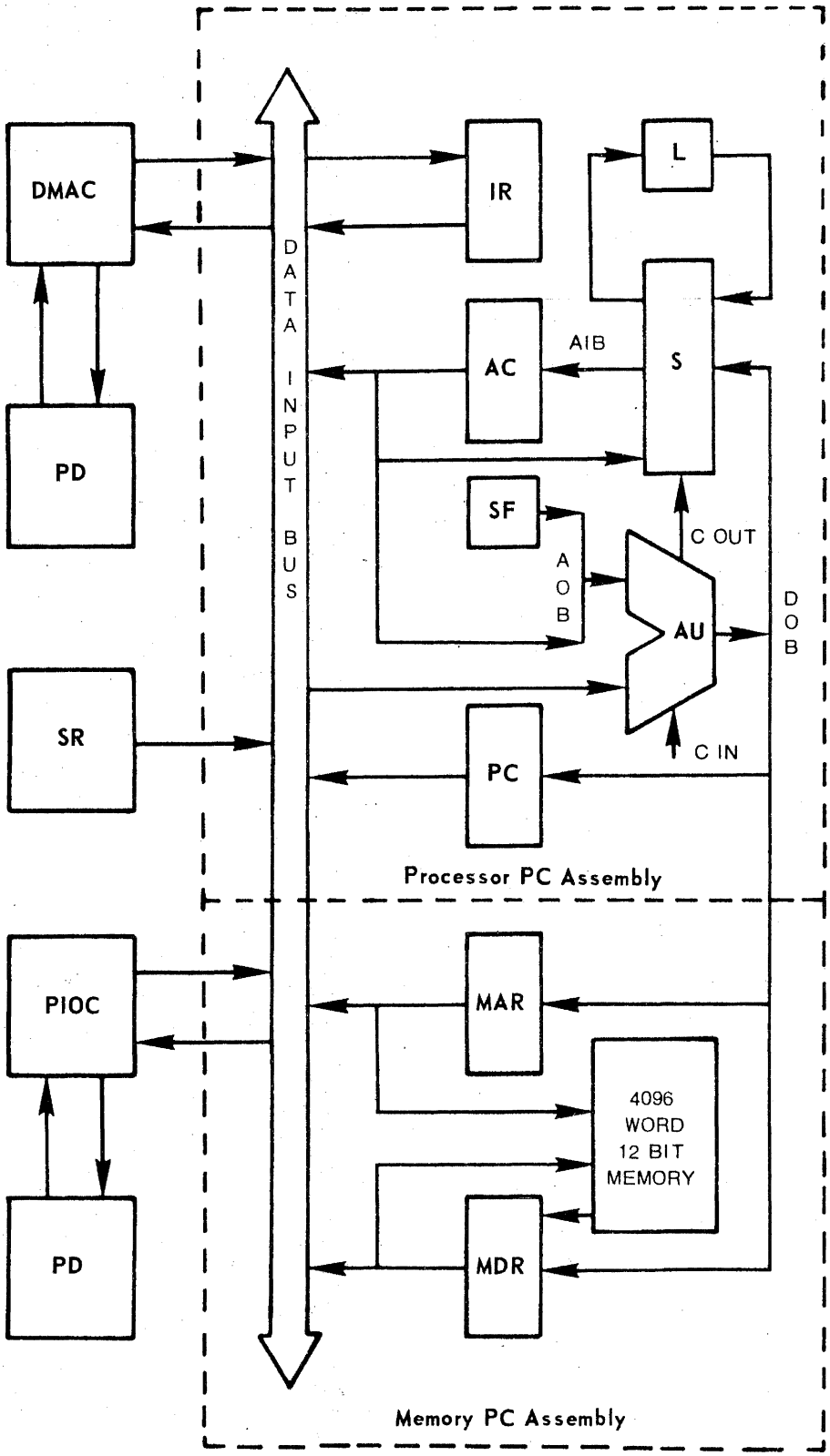
5. Toggle the Alter switch.

6. Connect the test points labeled TEST and GND located behind the control panel together using a clip lead.

7. Toggle the Run switch. The processor will now repetitively execute the instruction.

Signal Mnemonic	Schematic Page	Signal Name/Function
C-AC-AIB	22	Connect-Accumulator-Accumulator Input Bus
C-AC(RAL)-AIB	22	Connect-Accumulator Rotated Left-Accumulator Input Bus
C-AC(RAR)-AIB	22	Connect-Accumulator Rotated Right-Accumulator Input Bus
C-AC-AOB	21	Connect-Accumulator-Accumulator Output Bus
C-AC-DIB	21	Connect-Accumulator-Data Input Bus
C-ACC-DIB	21	Connect-Accumulator Complemented-Data Input Bus
C-DOB-AIB	22	Connect-Data Output Bus-Accumulator Input Bus
C-IR-DIB (05-11)	26	Connect-Instruction Register Bits 05-11-Data Input Bus
C-MD-DIB	19	Connect-Memory Data-Data Input Bus
C-PC-DIB (00-04)	20	Connect-Program Counter Bits 00-04-Data Input Bus
C-PC-DIB (05-11)	20	Connect-Program Counter Bits 05-11-Data Input Bus
C-SKIP-AOB	39	Connect-Skip Flag-Accumulator Output Bus
C-SR-DIB	21	Connect-Switch Register-Data Input Bus
HALT	27	Halt
/C-IN	39	Carry Input
/L-AC	23	Load Accumulator
/L-IR	34	Load Instruction Register
/L-MA	20	Load Memory Address Register
/L-MD	19	Load Memory Data Register
/L-PC	20	Load Program Counter Register
/PIO-CONNECT-DATA	33	Programmed Input/Output-Connect Data
/PIO-LOAD-DATA	33	Programmed Input/Output-Load Data
/PIO-SELECT	33	Programmed Input/Output-Select
/R-AC	23	Reset Accumulator
/C-MA-DIB	20	Connect-Memory Address-Data Input Bus

MAJOR CONTROL SIGNALS



AC	Accumulator
AIB	Accumulator In Bus
AOB	Accumulator Out Bus
AU	Arithmetic Unit
C IN	Carry In
C OUT	Carry Out
DMAC	Direct Memory Access Controller
DOB	Data Out Bus
IR	Instruction Register
L	Link
MAR	Memory Address Register
MDR	Memory Data Register
PC	Program Counter
PD	Peripheral Device
PIOC	Processor Input/Output Controller
S	Shifter
SF	Skip Flag
SR	Switch Register

SIMPLIFIED BLOCK DIAGRAM

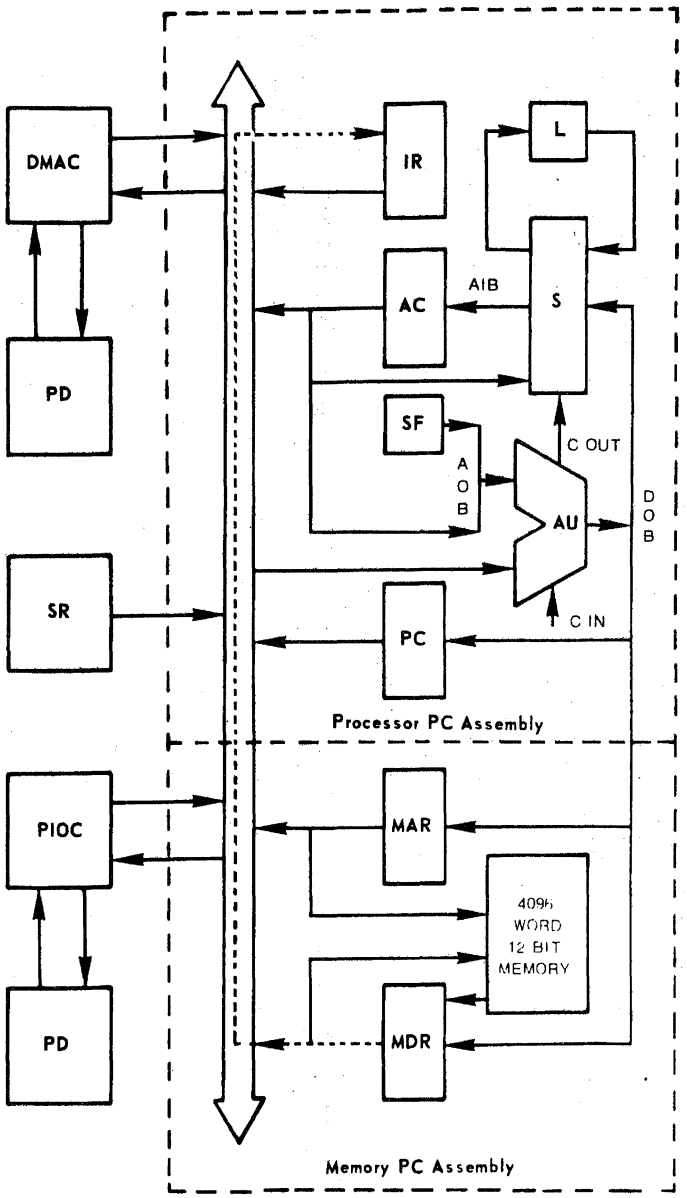
AND INSTRUCTION

Instruction - AND

State - Fetch
Timg - PA

Signals Asserted
C-MD-DIB
/L-IR

Other Operations
Read Memory
Clear Skip Flip-Flop



Description

During the first half cycle of the Fetch state the instruction word is read from the memory storage elements and transferred to the Instruction Register by way of the Memory Data Register and Data Input Bus.

AND INSTRUCTION

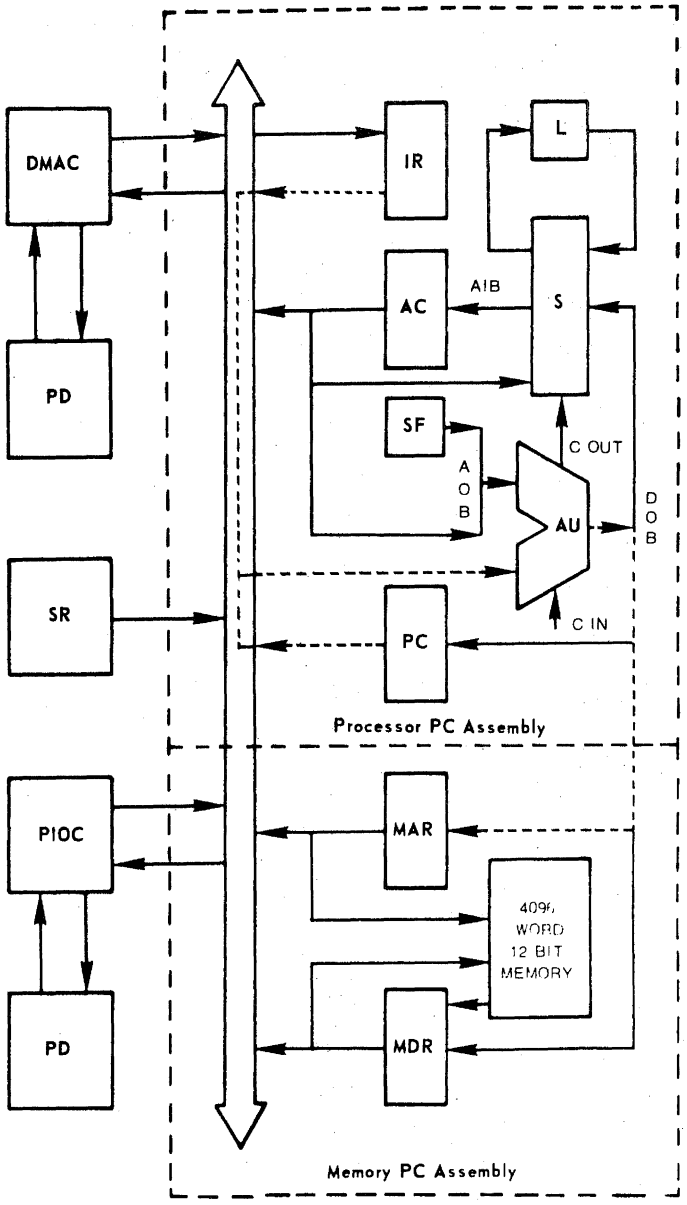
Instruction - AND

State - Fetch
Time - PB

Signals Asserted
- C-PC-DIB (00-04) If IR04 = 1
- C-IR-DIB (05-11)
- /L-MA

Other Operations
- Write Memory

Next State
- Defer If IR03 = 1
- Execute If IR03 = 0



Description

During the second half cycle of the Fetch state the memory address specified by the instruction word is generated and transferred to the Memory Address Register. The instruction word is restored to the memory storage elements by the memory write operation.

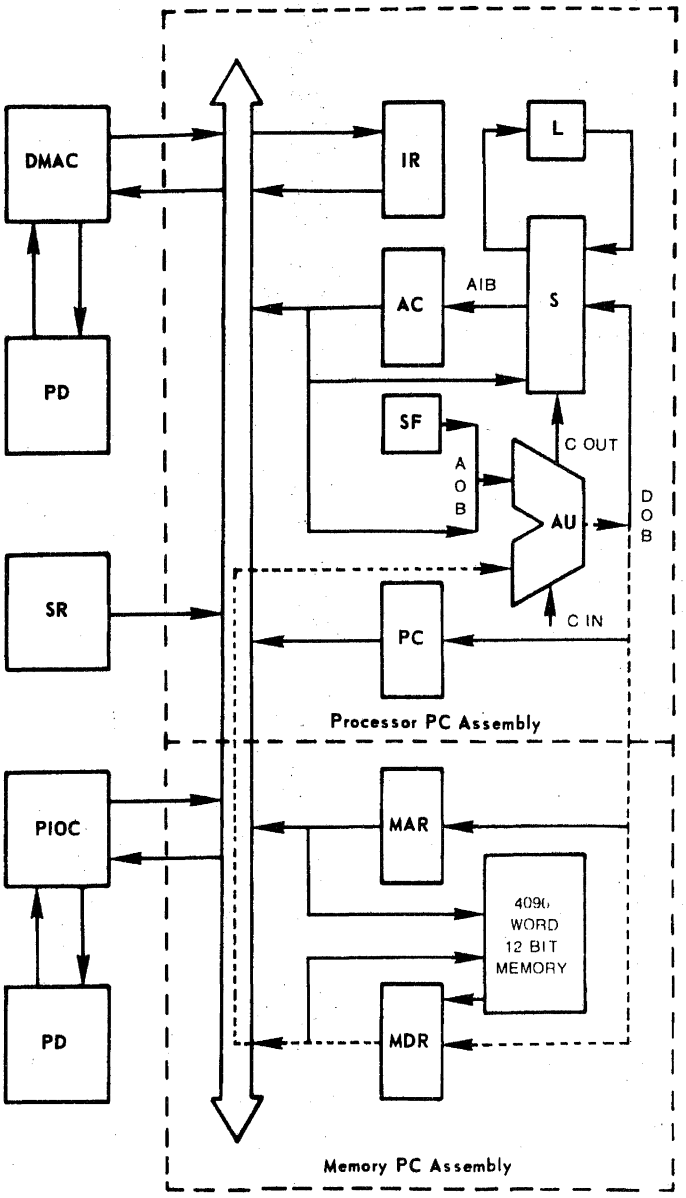
AND INSTRUCTION

Instruction - AND

State - Defer
Time - PA

Signals Asserted
C-MD-DIB
/C-IN If (MAR) = 0010_8 to 0017_8
/L-MD

Other Operations
Read Memory



Description

During the first half cycle of the Defer state the address word is read from the memory storage elements and transferred by way of the Memory Data Register, Data Input Bus, and Arithmetic Unit to the Memory Data Register. If Auto-Indexing is specified by the instruction word, one is added to the address word by the arithmetic unit before it is transferred back to the Memory Data Register.

AND INSTRUCTION

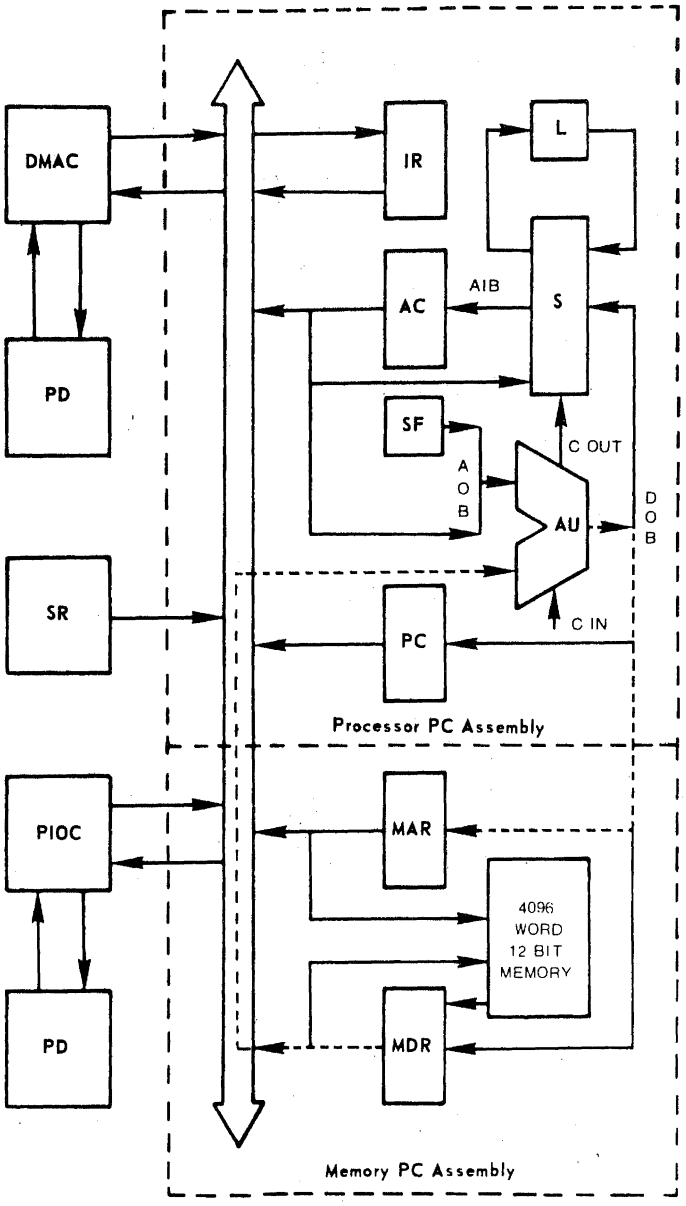
Instruction - AND

State - Defer
Time - PB

Signals Asserted
C-MD-DIB
/L-MA

Other Operations
Write Memory

Next State
Execute



Description

During the second half cycle of the Defer state the address word contained in the Memory Data Register is transferred to the Memory Address Register to be used during the next state. The address word is restored to the memory storage elements by the memory write operation.

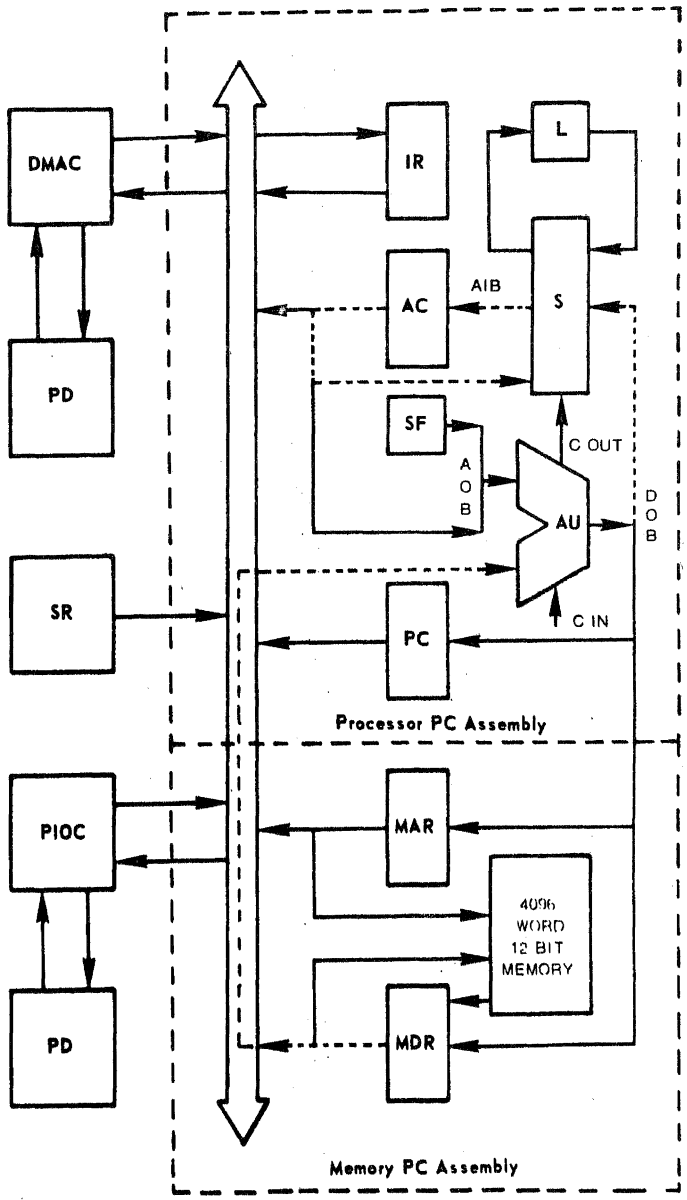
AND INSTRUCTION

Instruction - AND

State - Execute
Time - PA

Signals Asserted
- C-MD-DIB
- C-DOB-AIB
- C-AC-AIB
- /L-AC

Other Operations
- Read Memory



Description

During the first half cycle of the Execute state the operand specified by the instruction is read from the memory storage elements and transferred to the Shifter by way of the Memory Data Register, Data Input Bus, and Arithmetic Unit. The Shifter forms the logical AND of the memory operand and the Accumulator contents and transfers the result to the Accumulator.

AND INSTRUCTION

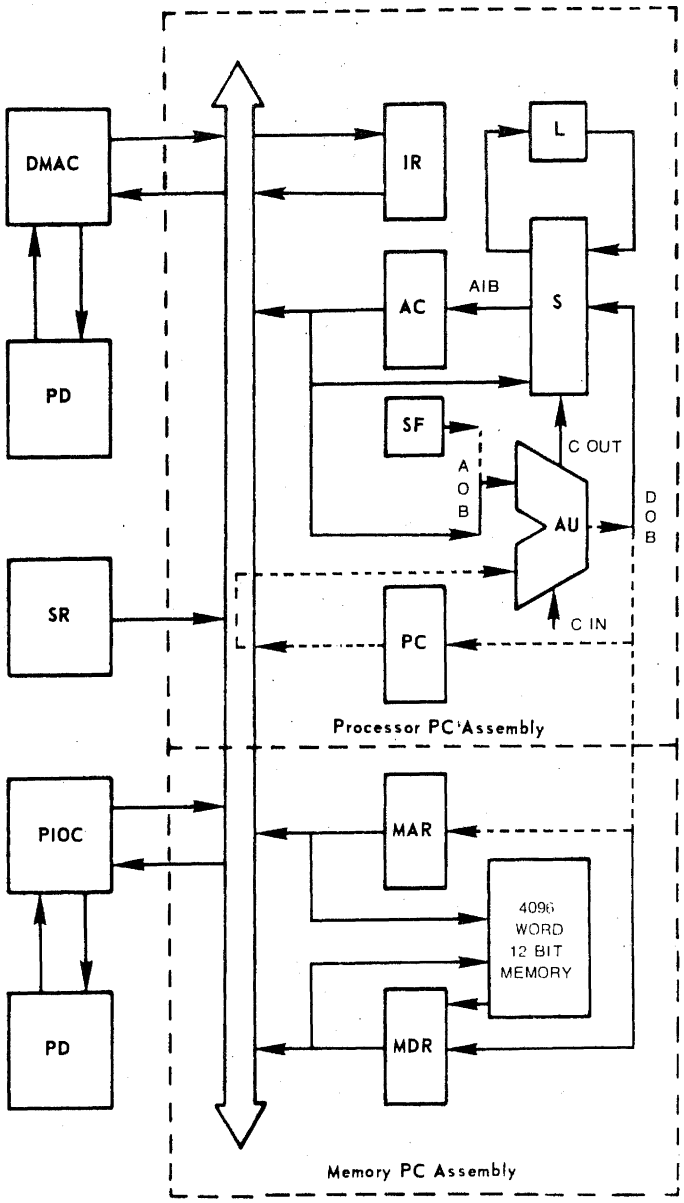
Instruction - AND

State - Execute
Time - PB

Signals Asserted
- C-PC-DIB (00-04)
- C-PC-DIB (05-11)
- /C-IN
- /L-PC
- /L-MA
- C-SKIP-AOB

Other Operations
- Memory Write

Next State
- Fetch If Run = 1



Description

During the second half cycle of the Execute state the address of the next instruction to be executed is generated by adding one to the address contained in the Program Counter and transferring the result to the Memory Address Register and to the Program Counter.

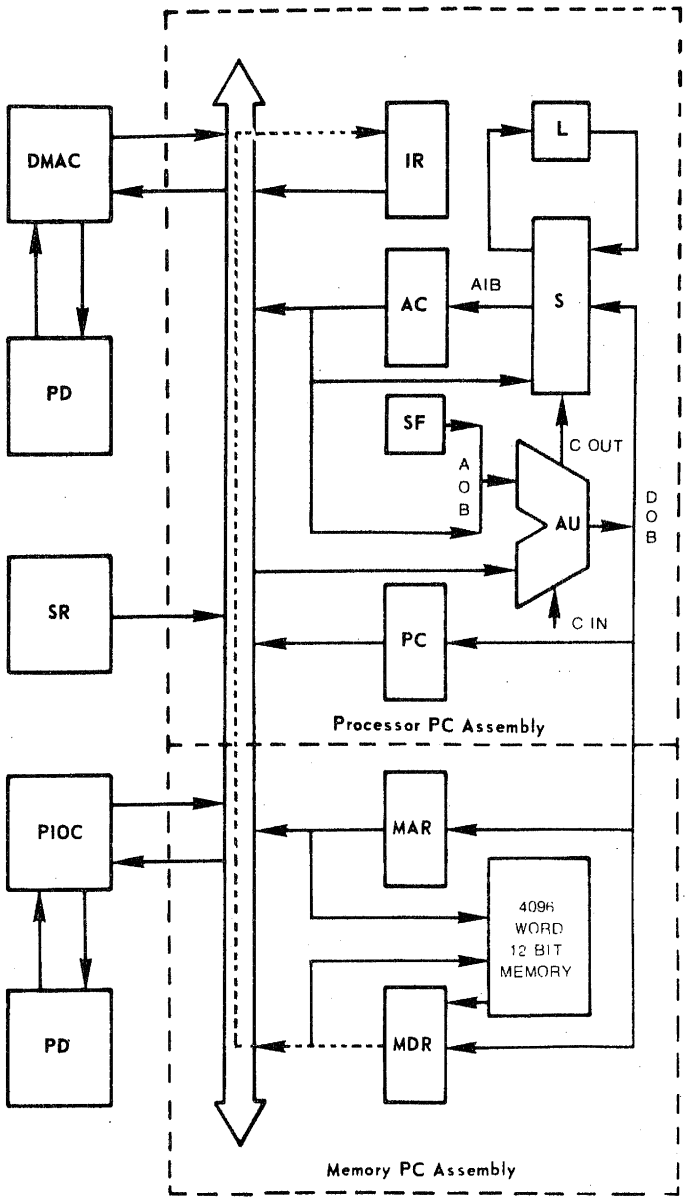
TAD INSTRUCTION

Instruction - TAD

State - Fetch
Time - PA

Signals Asserted
C-MD-DIB
/L-IR

Other Operations
Read Memory
Clear Skip Flip-Flop



Description

During the first half cycle of the Fetch state the instruction word is read from the memory storage elements and transferred to the Instruction Register by way of the Memory Data Register and Data Input Bus.

TAD INSTRUCTION

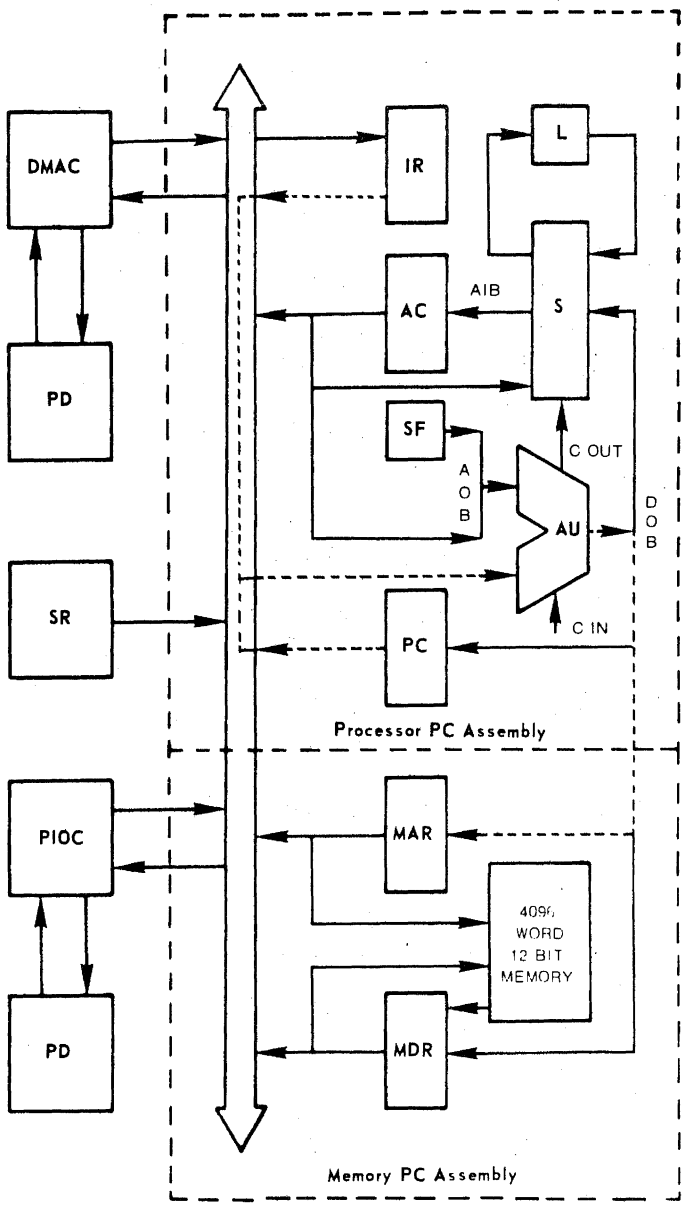
Instruction - TAD

State - Fetch
Time - PB

Signals Asserted
- C-PC-DIB (00-04) If IR04 = 1
- C-IR-DIB (05-11)
- /L-MA

Other Operations
- Write Memory

Next State
- Defer If IR03 = 1
- Execute If IR03 = 0



Description

During the second half cycle of the Fetch state the memory address specified by the instruction word is generated and transferred to the Memory Address Register. The instruction word is restored to the memory storage elements by the memory write operation.

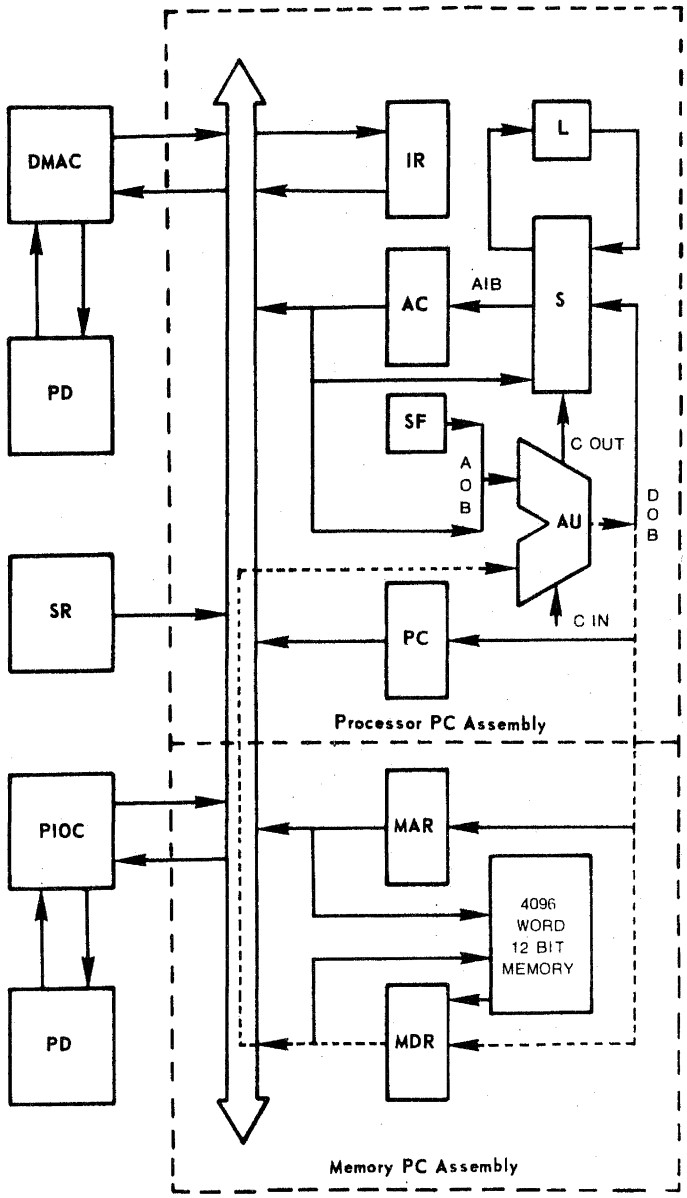
TAD INSTRUCTION

Instruction - TAD

State - Defer
Time - PA

Signals Asserted
C-MD-DIB
/C-IN If (MAR) = 0010_8 to 0017_8
/L-MD

Other Operations
Read Memory



Description

During the first half cycle of the Defer state the address word is read from the memory storage elements and transferred by way of the Memory Data Register, Data Input Bus, and Arithmetic Unit to the Memory Data Register. If Auto-Indexing is specified by the instruction word, one is added to the address word by the arithmetic unit before it is transferred back to the Memory Data Register.

TAD INSTRUCTION

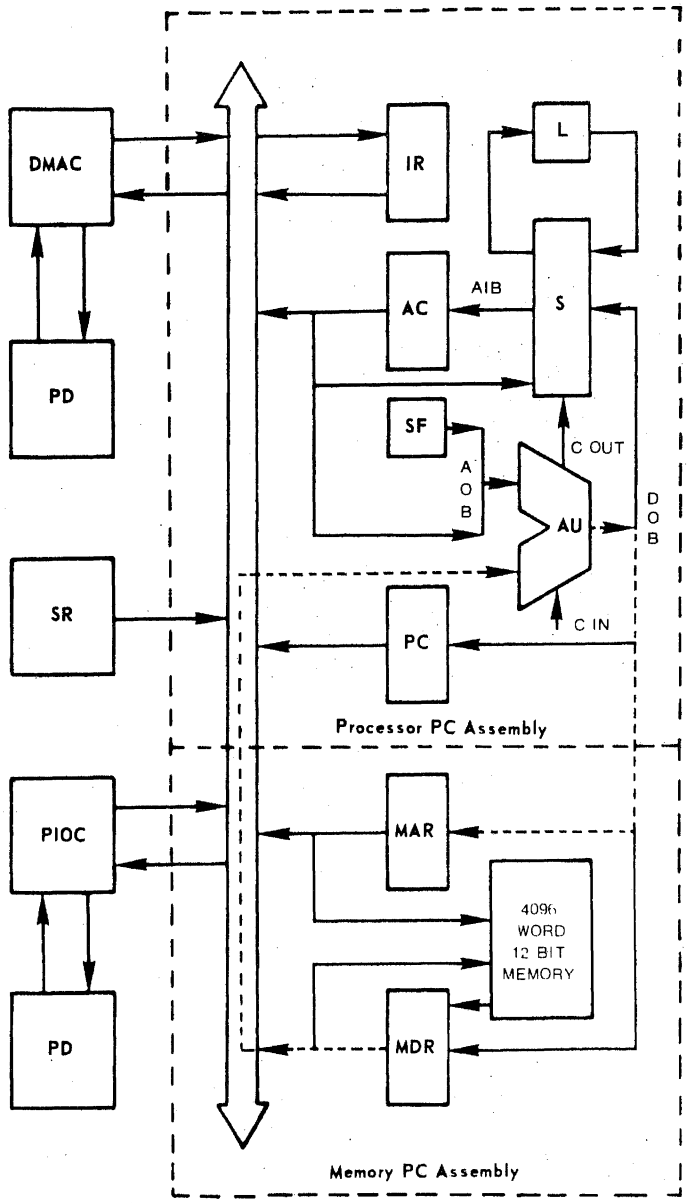
Instruction - TAD

State - Defer
Time - PB

Signals Asserted
C-MD-DIB
/L-MA

Other Operations
Write Memory

Next State
Execute



Description

During the second half cycle of the Defer state the address word contained in the Memory Data Register is transferred to the Memory Address Register to be used during the next state. The address word is restored to the memory storage elements by the memory write operation.

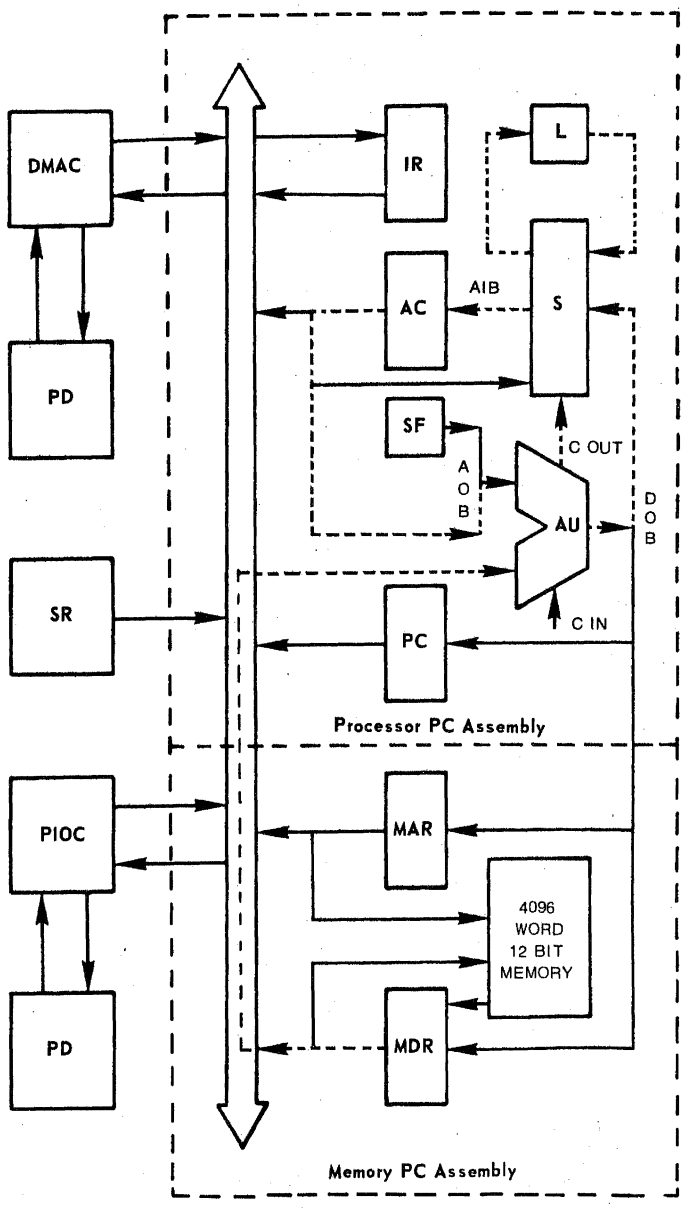
TAD INSTRUCTION

Instruction - TAD

State - Execute
Time - PA

Signals Asserted
- C-MD-DIB
- C-DOB-AIB
- C-AC-AOB
- /L-AC

Other Operations
- Memory Read
- Complement Link If C-OUT = 1



Description

During the first half cycle of the Execute state the operand specified by the instruction word is read from the memory storage elements and transferred by way of the Memory Data Register and Data Input Bus to the Arithmetic Unit. The Arithmetic Unit forms the sum of the memory operand and the accumulator contents and transfers the result back to the accumulator by way of the Shifter.

TAD INSTRUCTION

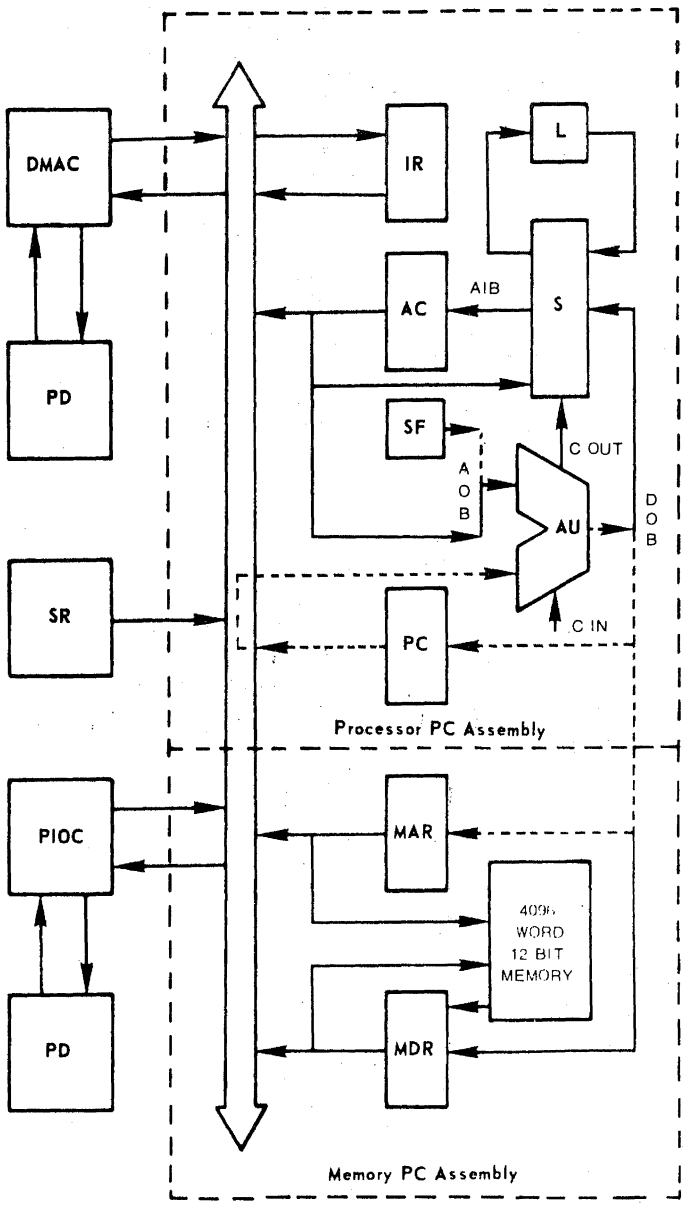
Instruction - TAD

State - Execute
Time - PB

Signals Asserted
- C-PC-DIB (00-04)
- C-PC-DIB (05-11)
- /C-IN
- /L-PC
- /L-MA
- C-SKIP-AOB

Other Operations
- Memory Write

Next State
- Fetch If Run = 1



Description

During the second half cycle of the Execute state the address of the next instruction to be executed is generated by adding one to the address contained in the Program Counter and transferring the result to the Memory Address Register and to the Program Counter.

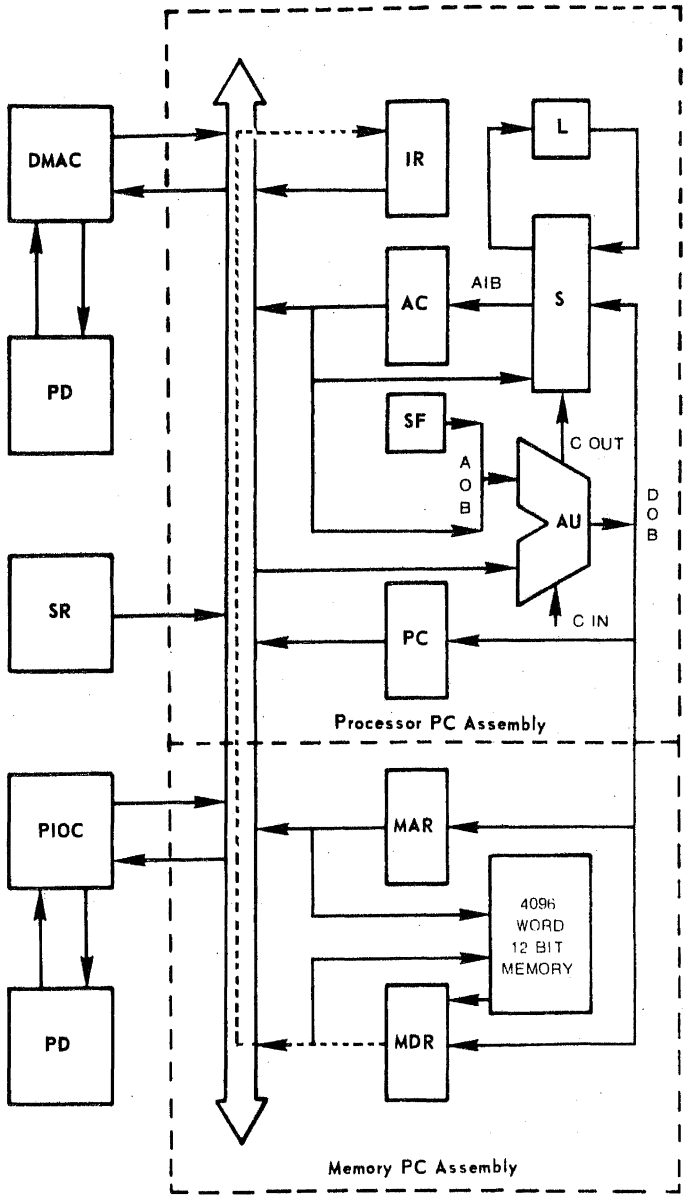
ISZ INSTRUCTION

Instruction - ISZ

State - Fetch
Time - PA

Signals Asserted
C-MD-DIB
/L-IR

Other Operations
Read Memory
Clear Skip Flip-Flop



Description

During the first half cycle of the Fetch state the instruction word is read from the memory storage elements and transferred to the Instruction Register by way of the Memory Data Register and Data Input Bus.

ISZ INSTRUCTION

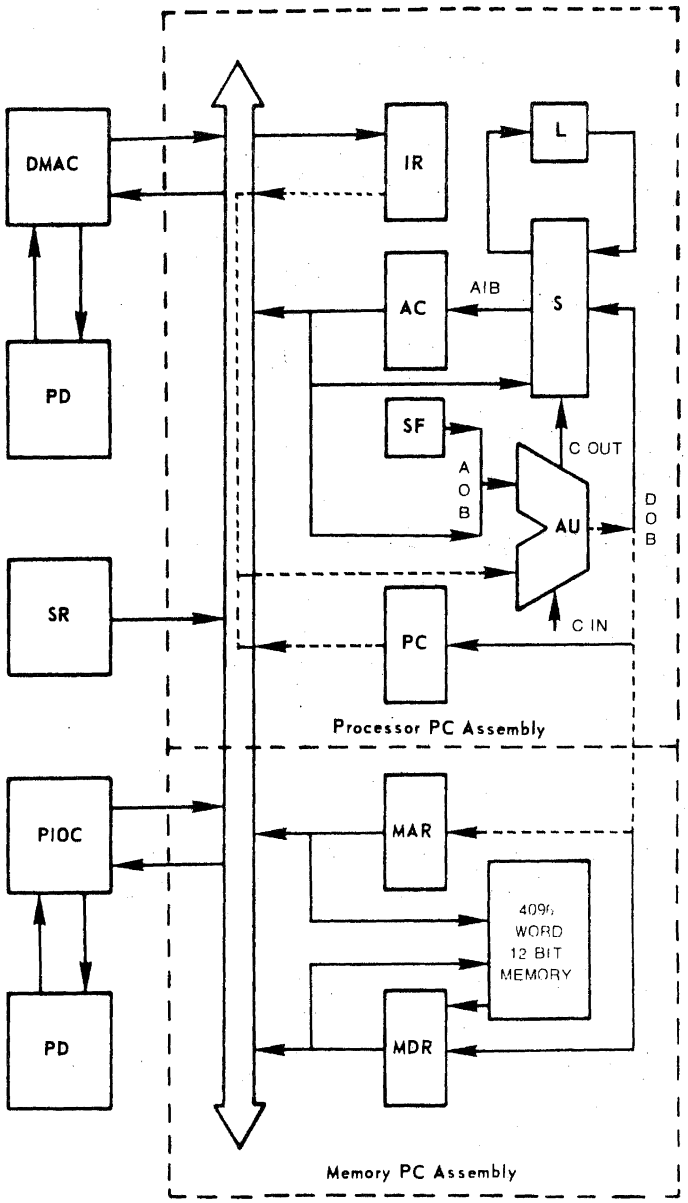
Instruction - ISZ

State - Fetch
Time - PB

Signals Asserted
- C-PC-DIB (00-04) If IR04 = 1
- C-IR-DIB (05-11)
- /L-MA

Other Operations
- Write Memory

Next State
- Defer If IR03 = 1
- Execute If IR03 = 0



Description

During the second half cycle of the Fetch state the memory address specified by the instruction word is generated and transferred to the Memory Address Register. The instruction word is restored to the memory storage elements by the memory write operation.

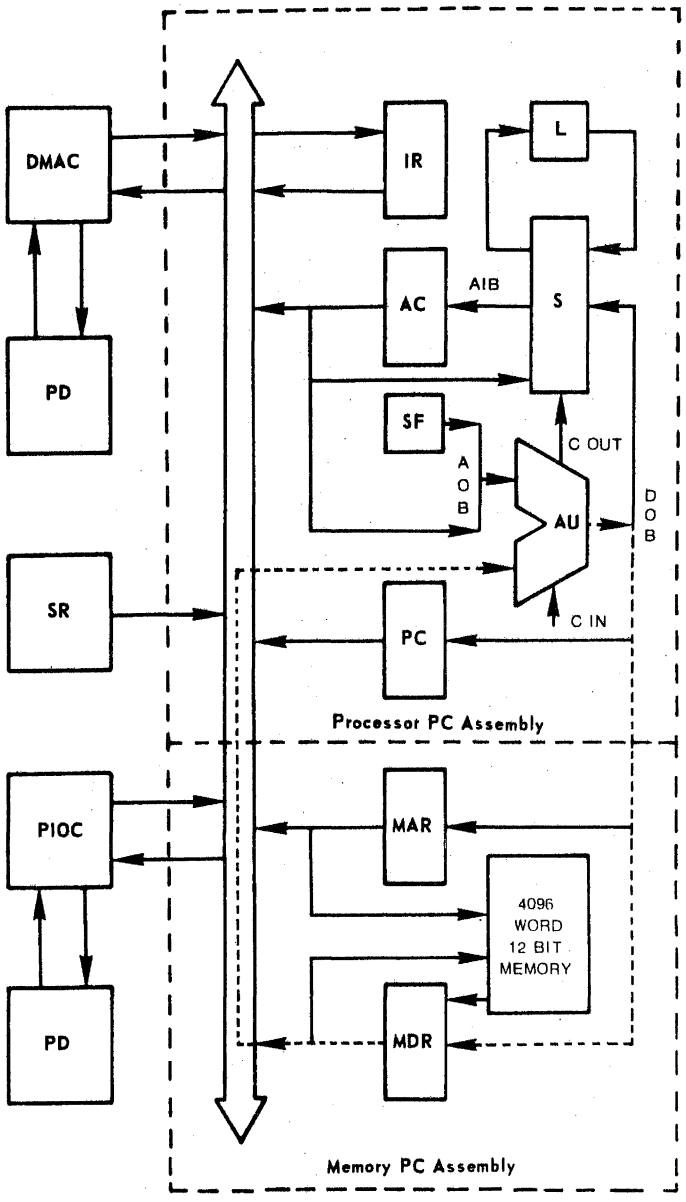
ISZ INSTRUCTION

Instruction - ISZ

State - Defer
Time - PA

Signals Asserted
- C-MD-DIB
- /C-IN If (MAR) = 0010_8 to 0017_8
- /L-MD

Other Operations
- Read Memory



Description

During the first half cycle of the Defer state the address word is read from the memory storage elements and transferred by way of the Memory Data Register, Data Input Bus, and Arithmetic Unit to the Memory Data Register. If Auto-Indexing is specified by the instruction word, one is added to the address word by the arithmetic unit before it is transferred back to the Memory Data Register.

ISZ INSTRUCTION

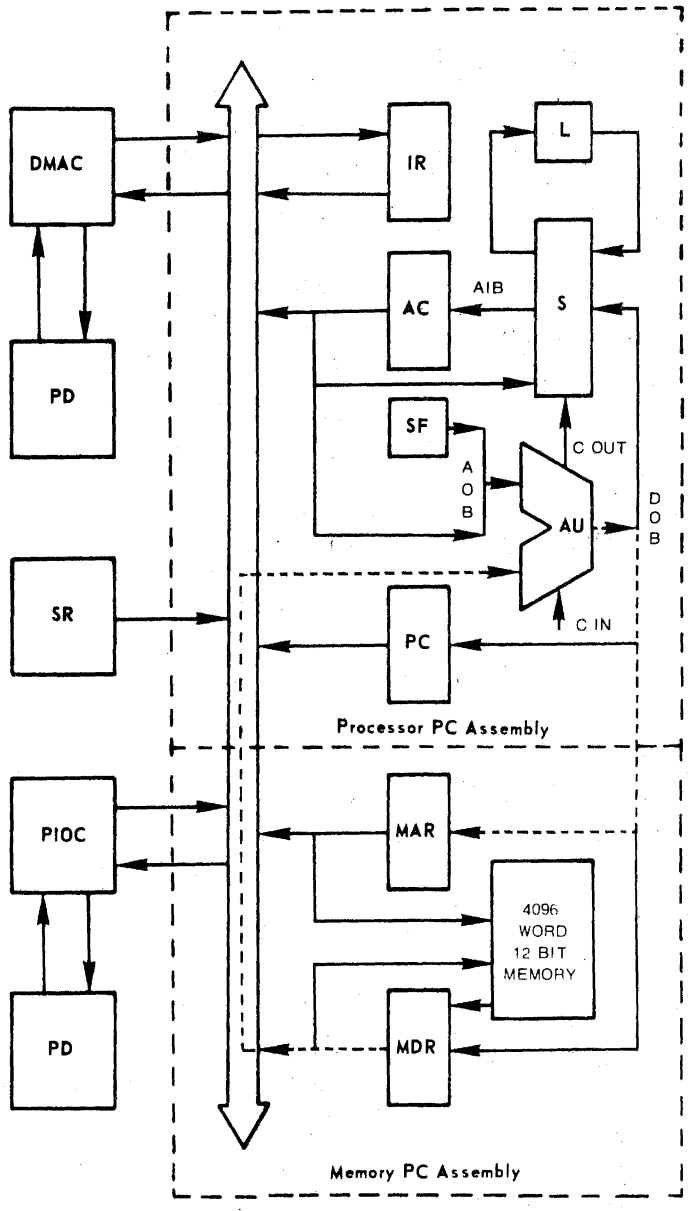
Instruction - ISZ

State - Defer
Time - PB

Signals Asserted
C-MD-DIB
/L-MA

Other Operations
Write Memory

Next State
Execute



Description

During the second half cycle of the Defer state the address word contained in the Memory Data Register is transferred to the Memory Address Register to be used during the next state. The address word is restored to the memory storage elements by the memory write operation.

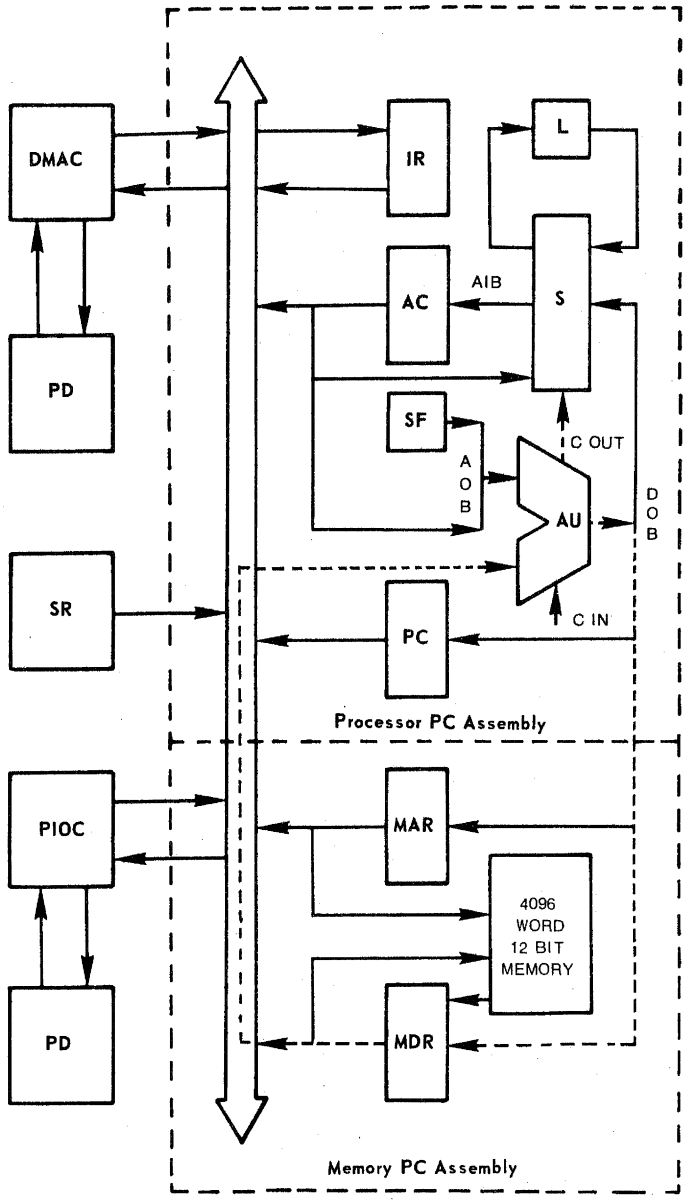
ISZ INSTRUCTION

Instruction - ISZ

State - Execute
Time - PA

Signals Asserted
C-MD-DIB
/C-IN
/L-MD

Other Operations
Set Skip Flip-Flop If C-OUT = 1



Description

During the first half cycle of the Execute state the memory operand specified by the instruction word is read from the memory storage elements and transferred by way of the Memory Data Register and Data Input Bus to the Arithmetic Unit. The arithmetic unit adds one to the memory operand and transfers the result to the Memory Data Register to be stored. If the add operation results in a carry the skip flip-flop is set.

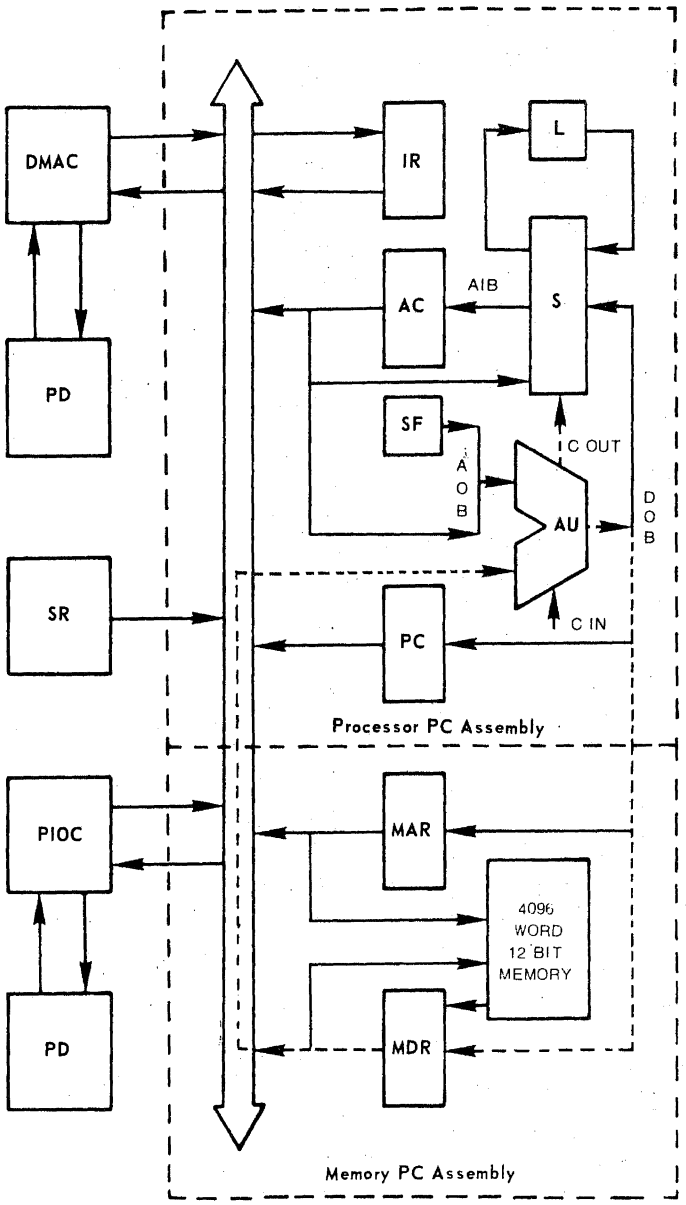
ISZ INSTRUCTION

Instruction - ISZ

State - Execute
Time - PA

Signals Asserted
C-MD-DIB
/C-IN
/L-MD

Other Operations
Set Skip Flip-Flop If C-OUT = 1



Description

During the first half cycle of the Execute state the memory operand specified by the instruction word is read from the memory storage elements and transferred by way of the Memory Data Register and Data Input Bus to the Arithmetic Unit. The arithmetic unit adds one to the memory operand and transfers the result to the Memory Data Register to be stored. If the add operation results in a carry the skip flip-flop is set.

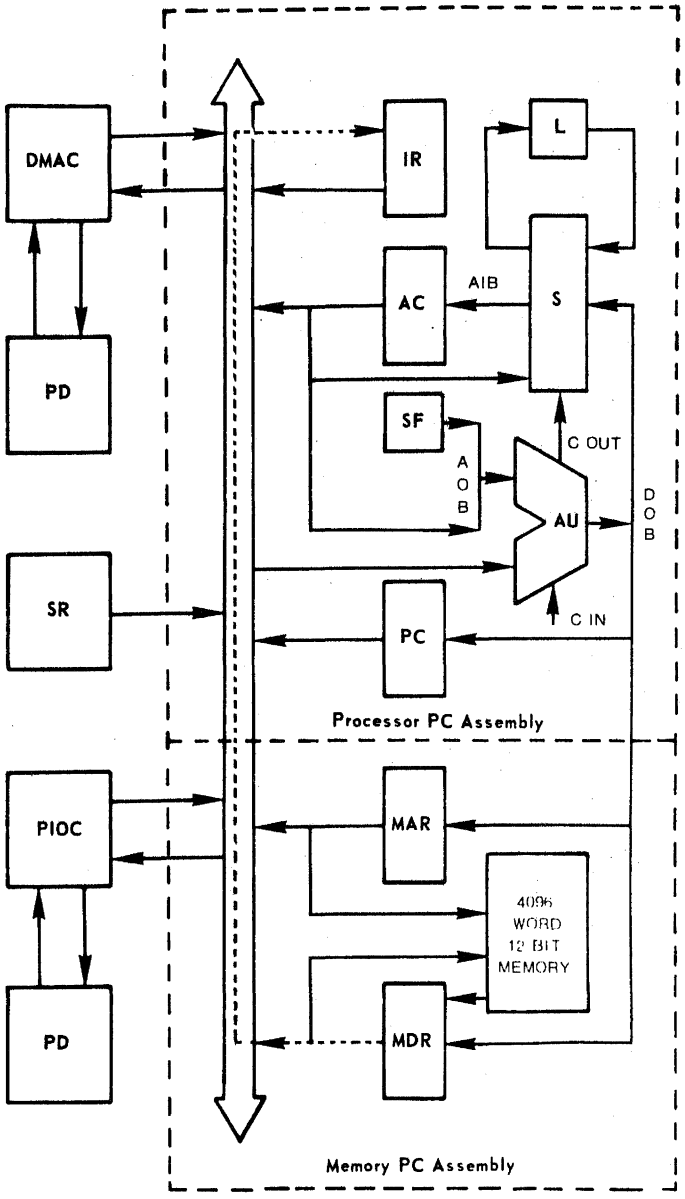
DCA INSTRUCTION

Instruction - DCA

State - Fetch
Time - PA

Signals Asserted
C-MD-DIB
/L-IR

Other Operations
Read Memory
Clear Skip Flip-Flop



Description

During the first half cycle of the Fetch state the instruction word is read from the memory storage elements and transferred to the Instruction Register by way of the Memory Data Register and Data Input Bus.

DCA INSTRUCTION

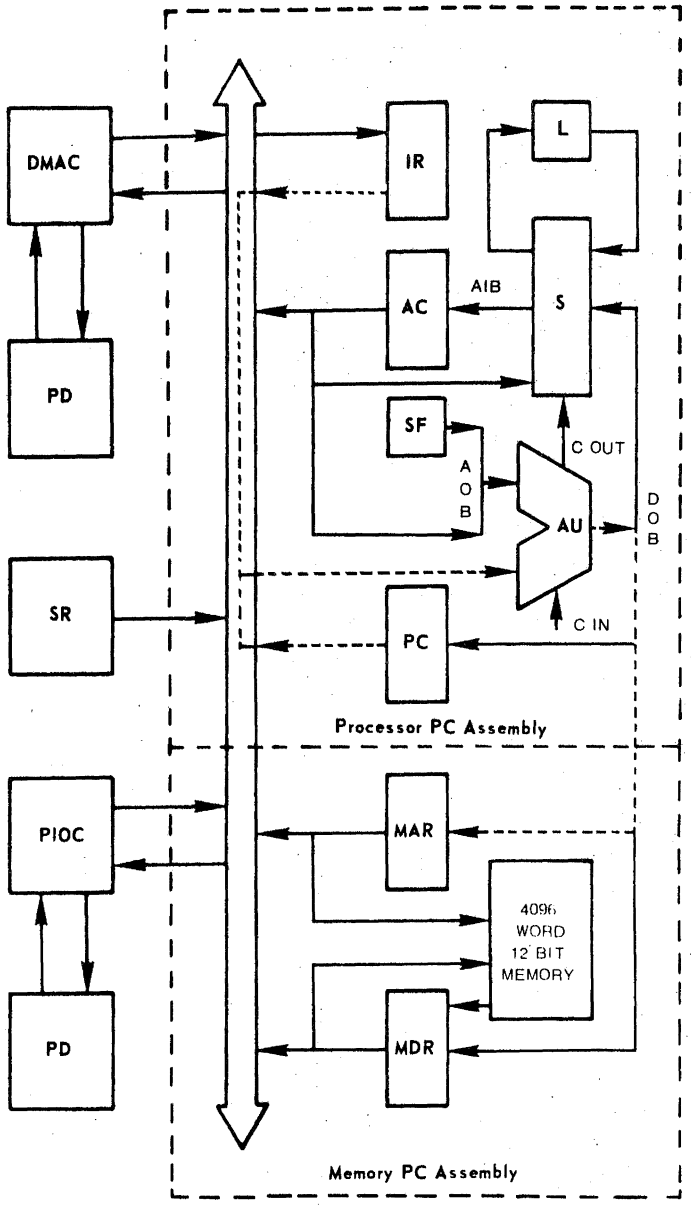
Instruction - DCA

State - Fetch
Time - PB

Signals Asserted
- C-PC-DIB (00-04) If IR04 = 1
- C-IR-DIB (05-11)
- /L-MA

Other Operations
- Write Memory

Next State
- Defer If IR03 = 1
- Execute If IR03 = 0



Description

During the second half cycle of the Fetch state the memory address specified by the instruction word is generated and transferred to the Memory Address Register. The instruction word is restored to the memory storage elements by the memory write operation.

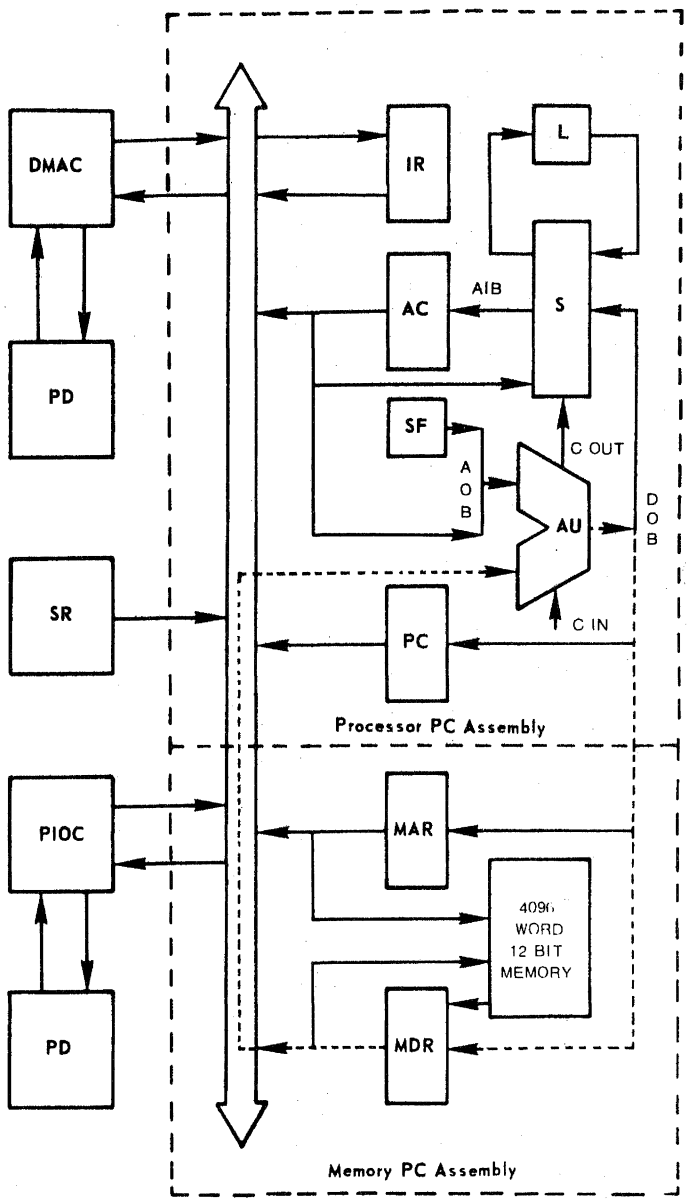
DCA INSTRUCTION

Instruction - DCA

State - Defer
Time - PA

Signals Asserted
C-MD-DIB
/C-IN If (MAR) = 0010_8 to 0017_8
/L-MD

Other Operations
Read Memory



Description

During the first half cycle of the Defer state the address word is read from the memory storage elements and transferred by way of the Memory Data Register, Data Input Bus, and Arithmetic Unit to the Memory Data Register. If Auto-Indexing is specified by the instruction word, one is added to the address word by the arithmetic unit before it is transferred back to the Memory Data Register.

DCA INSTRUCTION

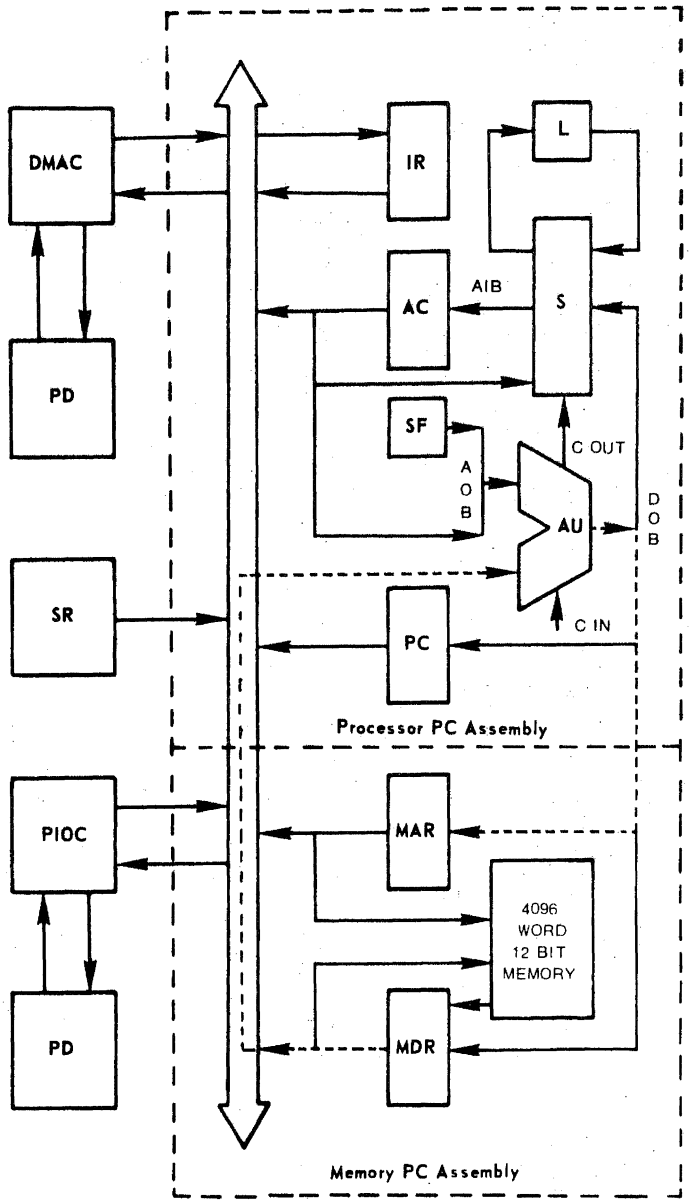
Instruction - DCA

State - Defer
Time - PB

Signals Asserted
C-MD-DIB
/L-MA

Other Operations
Write Memory

Next State
Execute



Description

During the second half cycle of the Defer state the address word contained in the Memory Data Register is transferred to the Memory Address Register to be used during the next state. The address word is restored to the memory storage elements by the memory write operation.

DCA INSTRUCTION

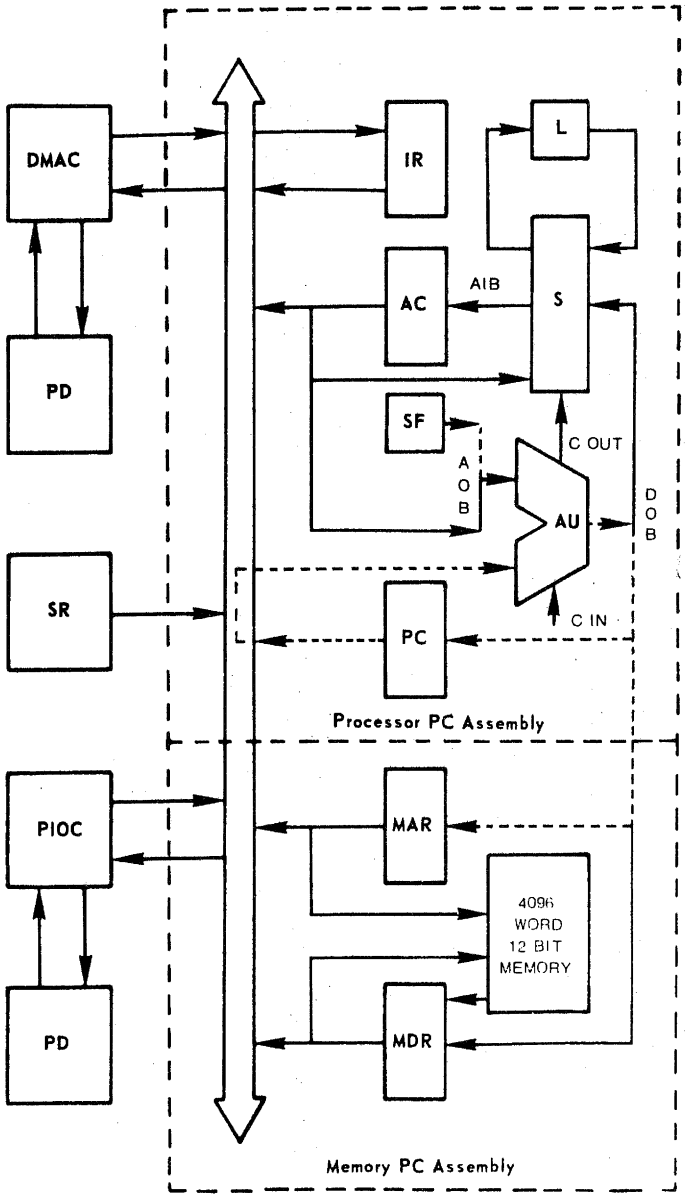
Instruction - DCA

State - Execute
Time - PB

Signals Asserted
- C-PC-DIB (00-04)
- C-PC-DIB (05-11)
- /C-IN
- /L-PC
- /R-AC
- C-SKIP-AOB

Other Operations
- Memory Write
- Clear Accumulator

Next State
- Fetch If Run = 1



Description

During the second half cycle of the Execute state the address of the next instruction to be executed is generated by adding one to the address contained in the Program Counter and transferring the result to the Memory Address Register and to the Program Counter.

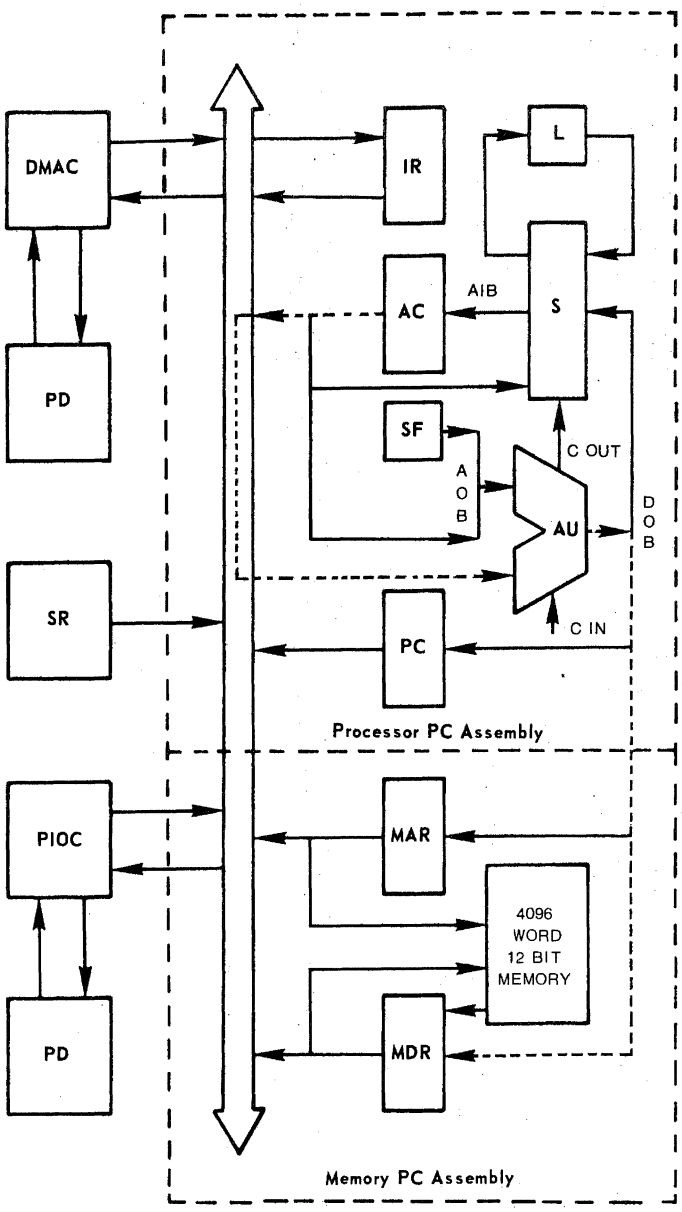
DCA INSTRUCTION

Instruction - DCA

State - Execute
Time - PA

Signals Asserted
C-AC-DIB
/L-MD

Other Operations
Read Memory (Clear)



Description

During the first half cycle of the Execute state the memory location specified by the instruction word is cleared and the contents of the accumulator is transferred by way of the Data Input Bus, Arithmetic Unit and Data Output Bus to the Memory Data Register to be stored.

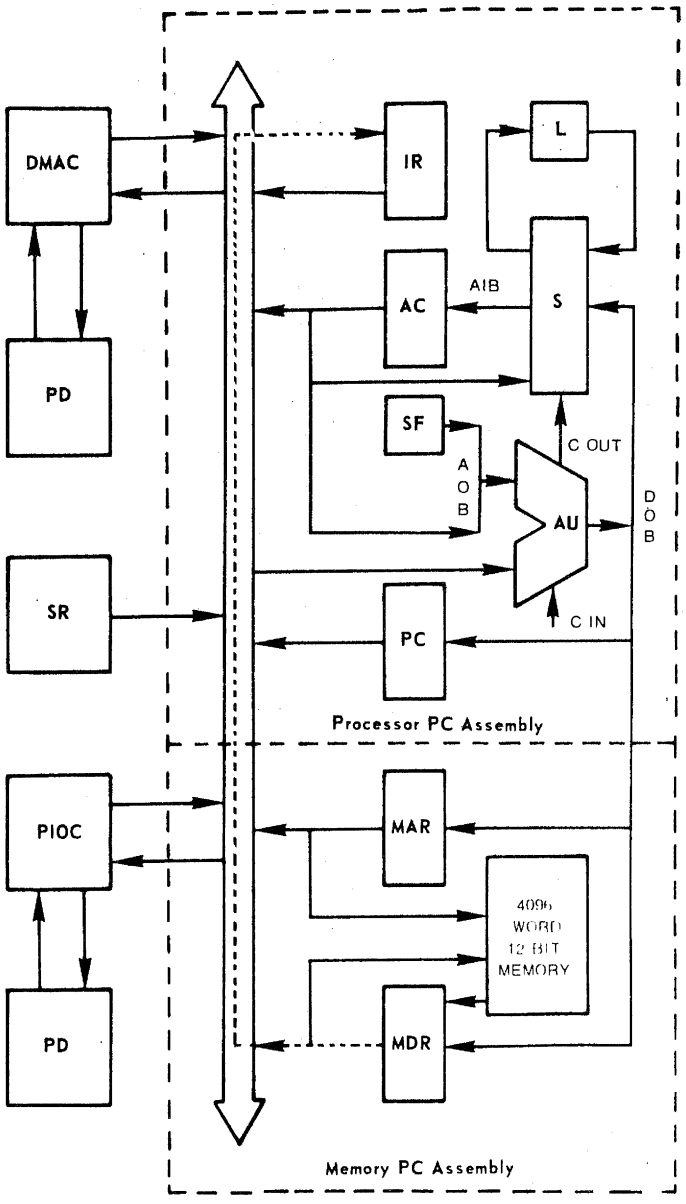
JMS INSTRUCTION

Instruction - JMS

State - Fetch
Time - PA

Signals Asserted
C-MD-DIB
/L-IR

Other Operations
Read Memory
Clear Skip Flip-Flop



Description

During the first half cycle of the Fetch state the instruction word is read from the memory storage elements and transferred to the Instruction Register by way of the Memory Data Register and Data Input Bus.

JMS INSTRUCTION

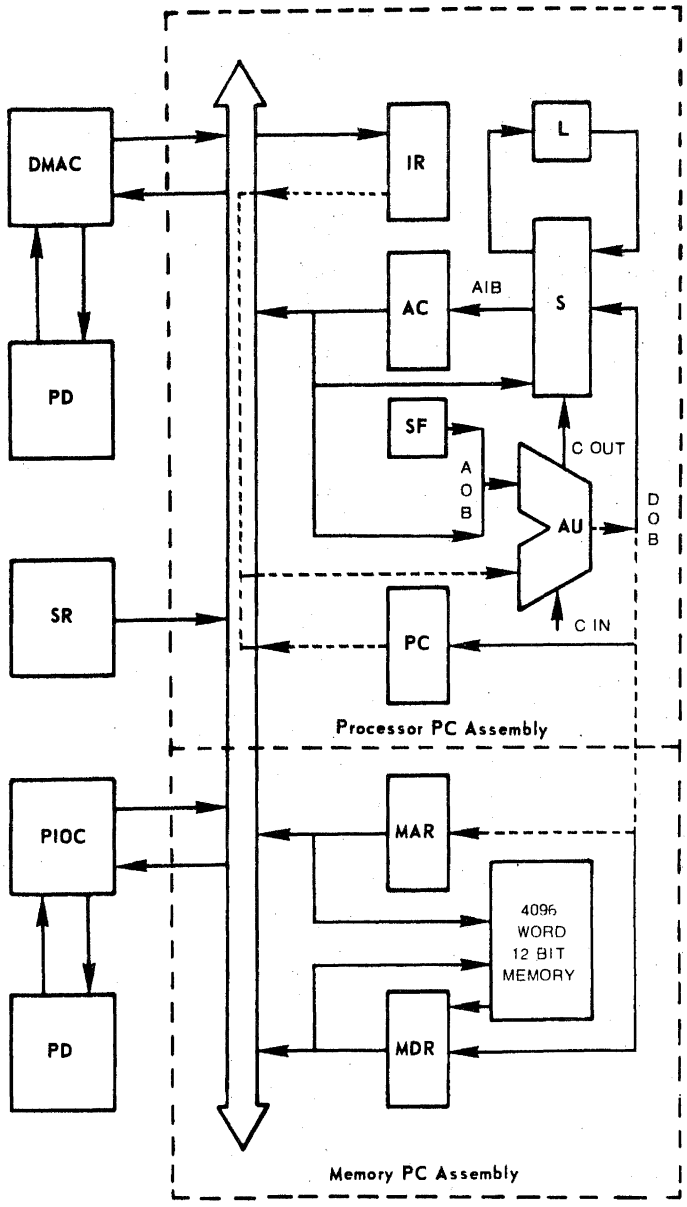
Instruction - JMS

State - Fetch
Time - PB

Signals Asserted
- C-PC-DIB (00-04) If IR04 = 1
- C-IR-DIB (05-11)
- /L-MA

Other Operations
- Write Memory

Next State
- Defer If IR03 = 1
- Execute If IR03 = 0



Description

During the second half cycle of the Fetch state the memory address specified by the instruction word is generated and transferred to the Memory Address Register. The instruction word is restored to the memory storage elements by the memory write operation.

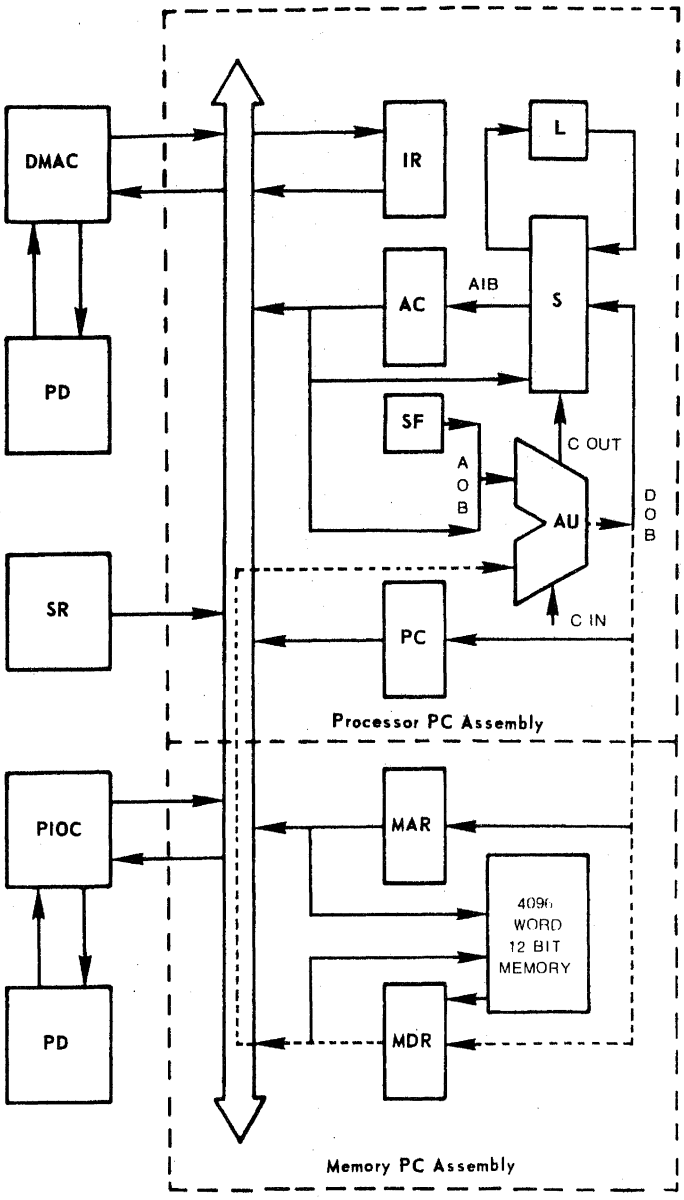
JMS INSTRUCTION

Instruction - JMS

State - Defer
Time - PA

Signals Asserted
C-MD-DIB
/C-IN If (MAR) = 0010_8 to 0017_8
/L-MD

Other Operations
Read Memory



Description

During the first half cycle of the Defer state the address word is read from the memory storage elements and transferred by way of the Memory Data Register, Data Input Bus, and Arithmetic Unit to the Memory Data Register. If Auto-Indexing is specified by the instruction word, one is added to the address word by the arithmetic unit before it is transferred back to the Memory Data Register.

JMS INSTRUCTION

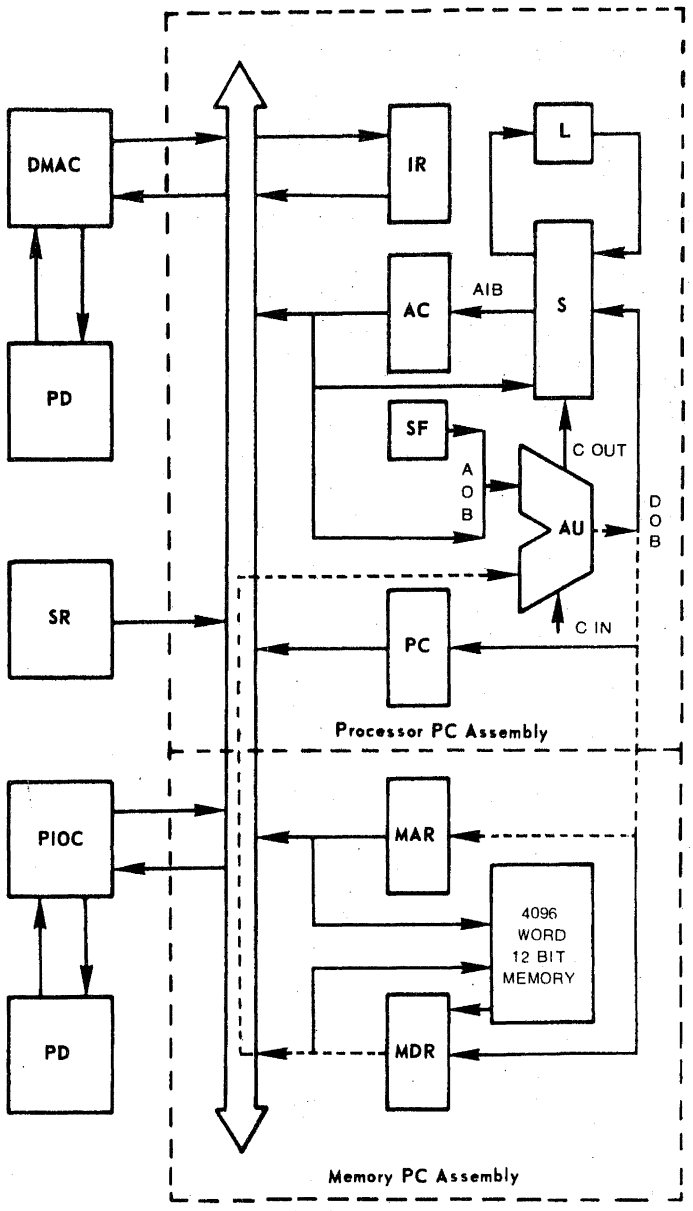
Instruction - JMS

State - Defer
Time - PB

Signals Asserted
C-MD-DIB
/L-MA

Other Operations
Write Memory

Next State
Execute



Description

During the second half cycle of the Defer state the address word contained in the Memory Data Register is transferred to the Memory Address Register to be used during the next state. The address word is restored to the memory storage elements by the memory write operation.

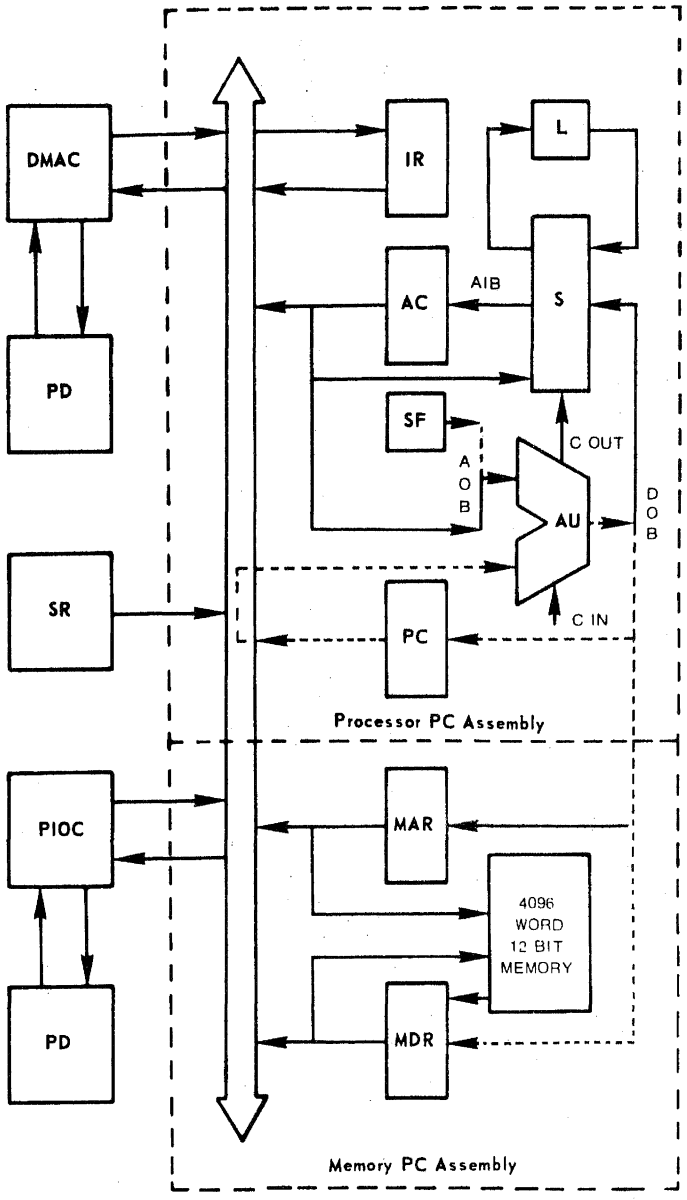
JMS INSTRUCTION

Instruction - JMS

State - Execute
Time - PA

Signals Asserted
C-PC-DIB (00-04)
C-PC-DIB (05-11)
/L-MD
/C-IN

Other Operations
Read Memory (Clear)



Description

During the first half cycle of the Execute state the memory location specified by the instruction word is cleared and the contents of the Program Counter are transferred to the Memory Data Register by way of the Data Input Bus, Arithmetic Unit, and Data Output Bus to be stored. The arithmetic unit adds one to the word during the transfer.

JMS INSTRUCTION

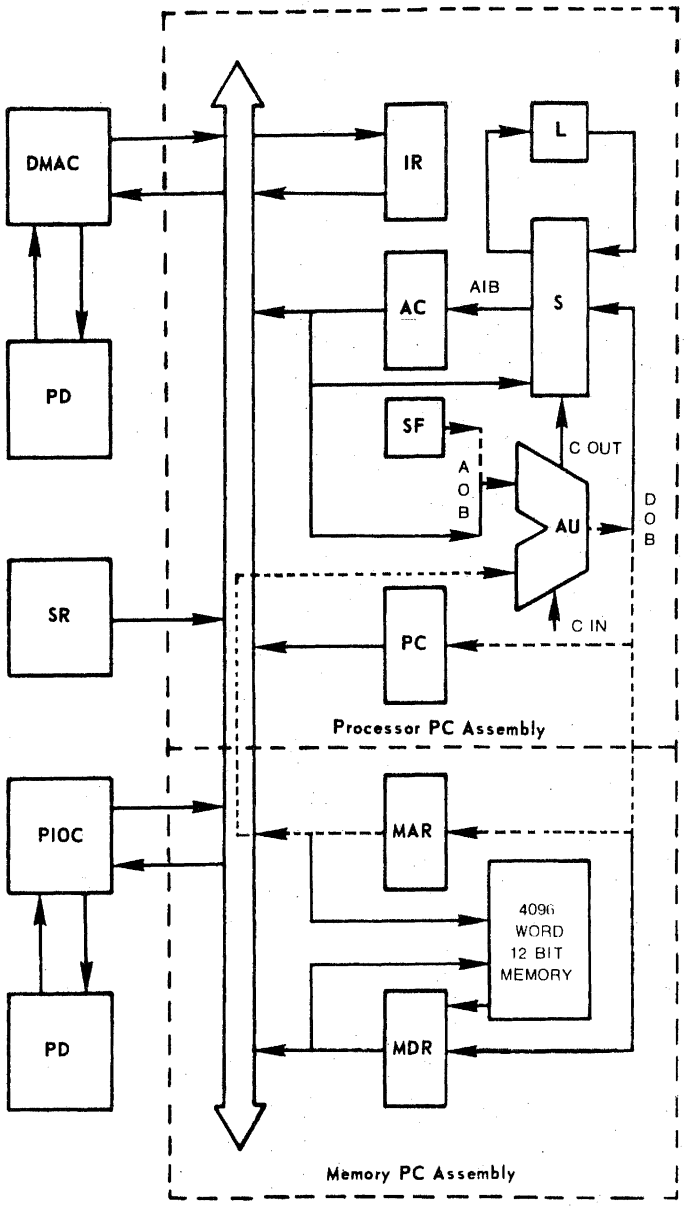
Instruction - JMS

State - Execute
Time - PB

Signals Asserted
- /C-MA-DIB
- /C-IN
- /L-PC
- /L-MA
- C-SKIP-AOB

Other Operations
- Memory Write

Next State
- Fetch If Run = 1



Description

During the second half cycle of the Execute state the address of the next instruction to be executed is generated by adding one to the address contained in the Memory Address Register and transferring the result to the Memory Address Register and to the Program Counter.

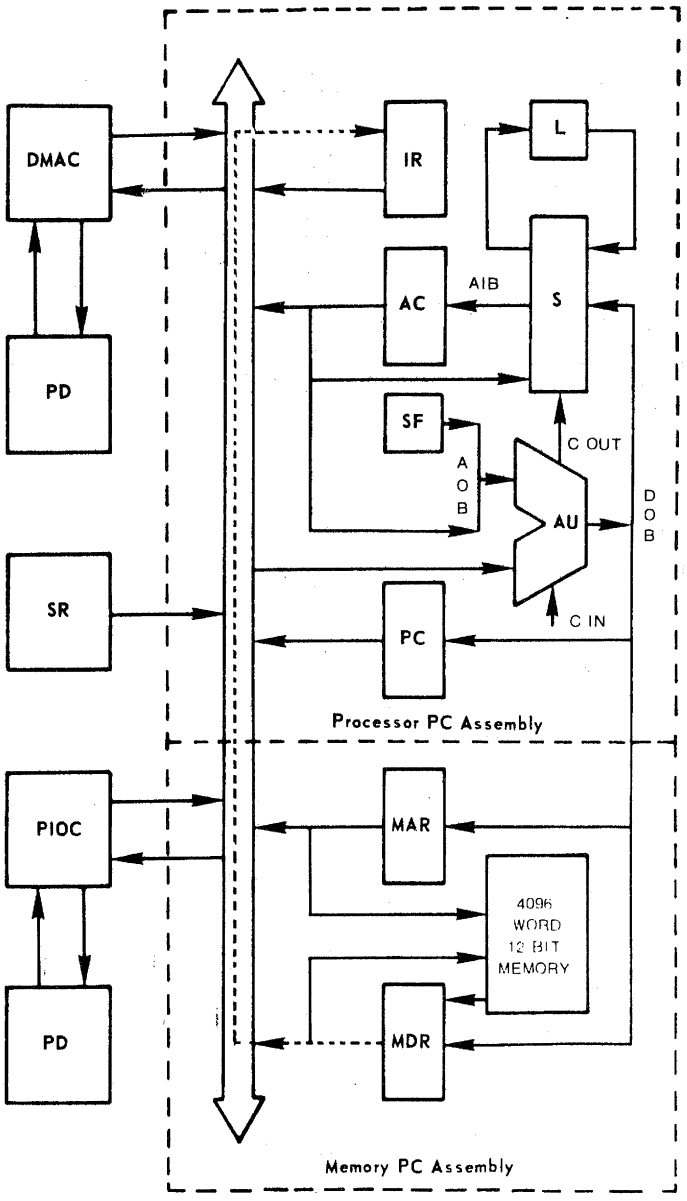
JMP INSTRUCTION

Instruction - JMP

State - Fetch
Time - PA

Signals Asserted
C-MD-DIB
/L-IR

Other Operations
Read Memory
Clear Skip Flip-Flop



Description

During the first half cycle of the Fetch state the instruction word is read from the memory storage elements and transferred to the Instruction Register by way of the Memory Data Register and Data Input Bus.

JMP INSTRUCTION

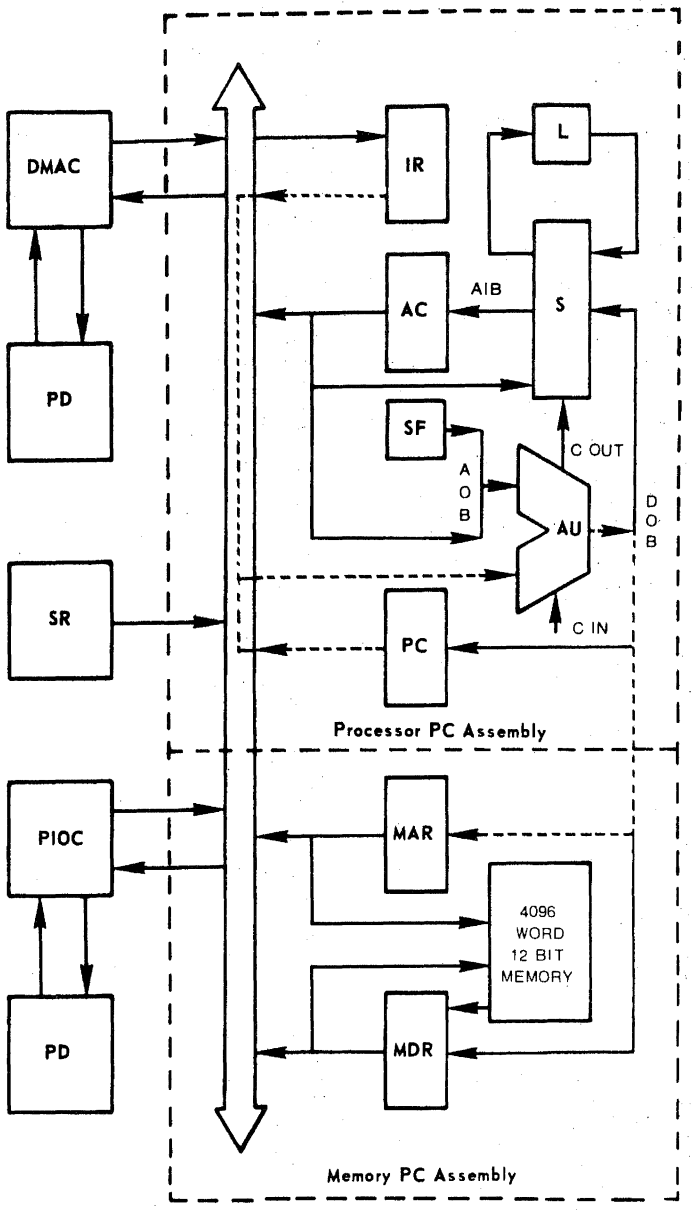
Instruction - JMP

State - Fetch
Time - PB

Signals Asserted
- C-PC-DIB (00-04) If IR04 = 1
- C-IR-DIB (05-11)
- /L-MA
- /L-PC If IR03 = 0

Other Operations
- Write Memory

Next State
- Defer If IR03 = 1
- Fetch If IR03 = 0 and Run = 1



Description

During the second half cycle of the Fetch state the memory address specified by the instruction word is generated and transferred to the Memory Address Register and to the Program Counter if indirect addressing is not specified. The instruction word is restored to the memory storage elements by the memory write operation.

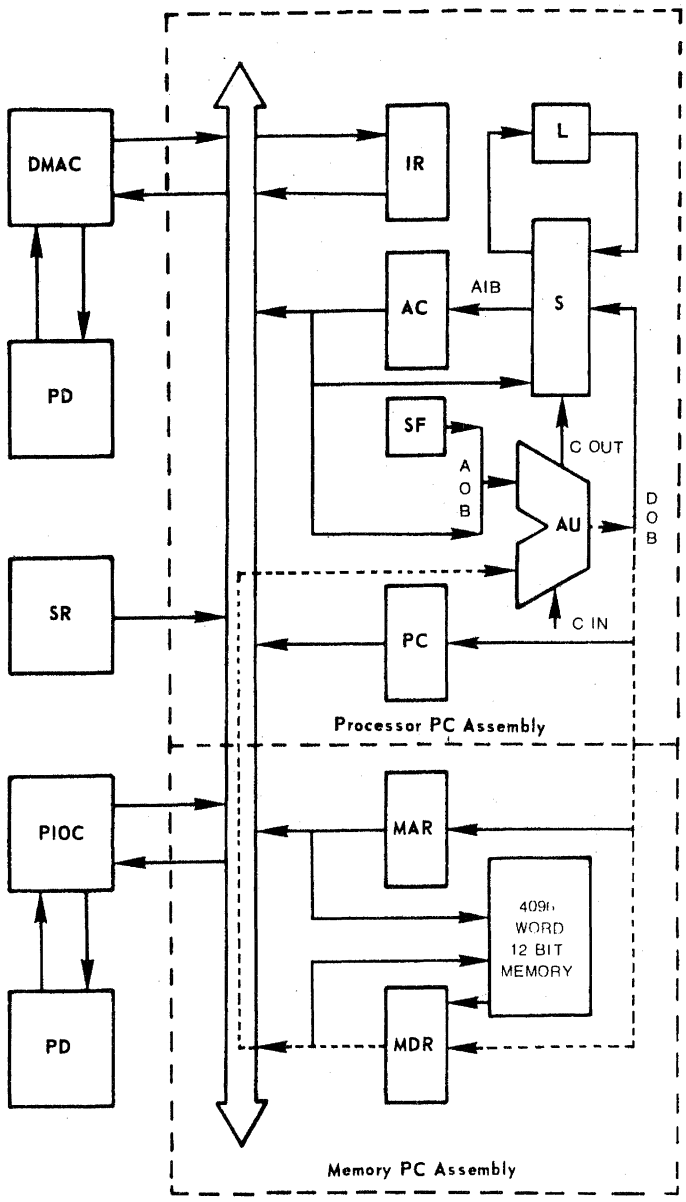
JMP INSTRUCTION

Instruction - JMP

State - Defer
Time - PA

Signals Asserted
C-MD-DIB
/C-IN If (MAR) = 0010_8 to 0017_8
/L-MD

Other Operations
Read Memory



Description

During the first half cycle of the Defer state the address word is read from the memory storage elements and transferred by way of the Memory Data Register, Data Input Bus, and Arithmetic Unit to the Memory Data Register. If Auto-Indexing is specified by the instruction word, one is added to the address word by the arithmetic unit before it is transferred back to the Memory Data Register.

JMP INSTRUCTION

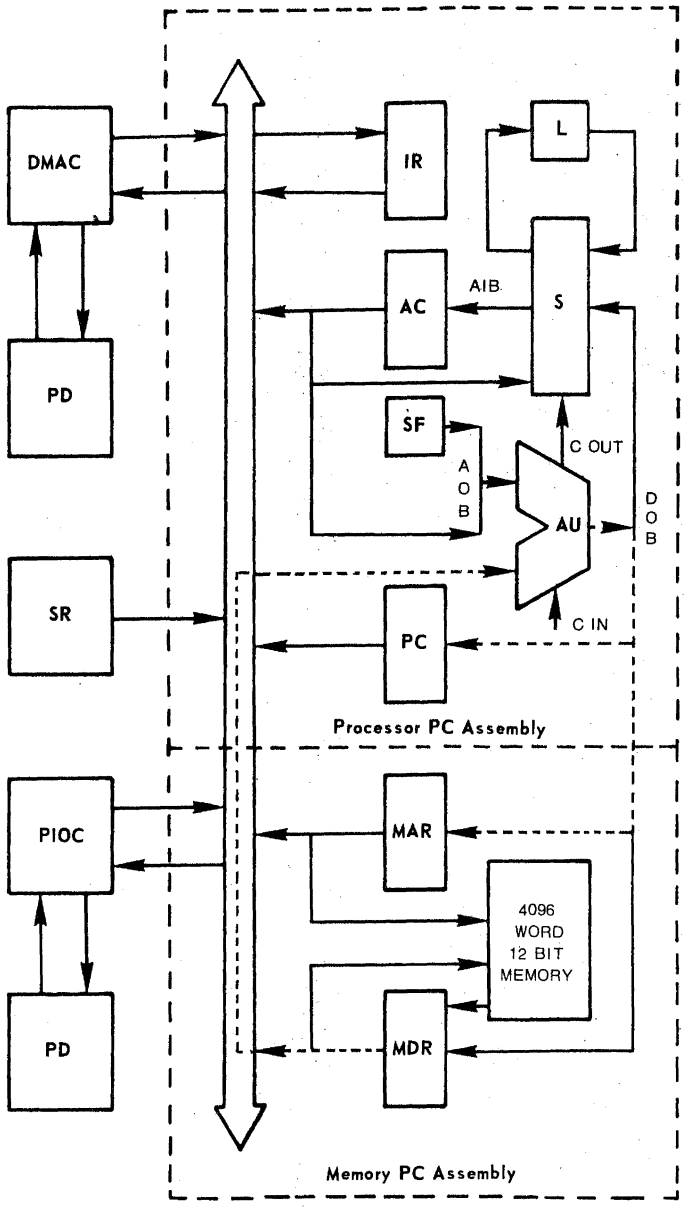
Instruction - JMP

State - Defer
Time - PB

Signals Asserted
C-MD-DIB
/L-MA
/L-PC

Other Operations
Write Memory

Next State
Fetch If Run = 1



Description

During the second half cycle of the Defer state the address word contained in the Memory Data Register is transferred to the Memory Address Register and to the Program Counter to be used during the next state. The address word is restored to the memory storage elements by the memory write operation.

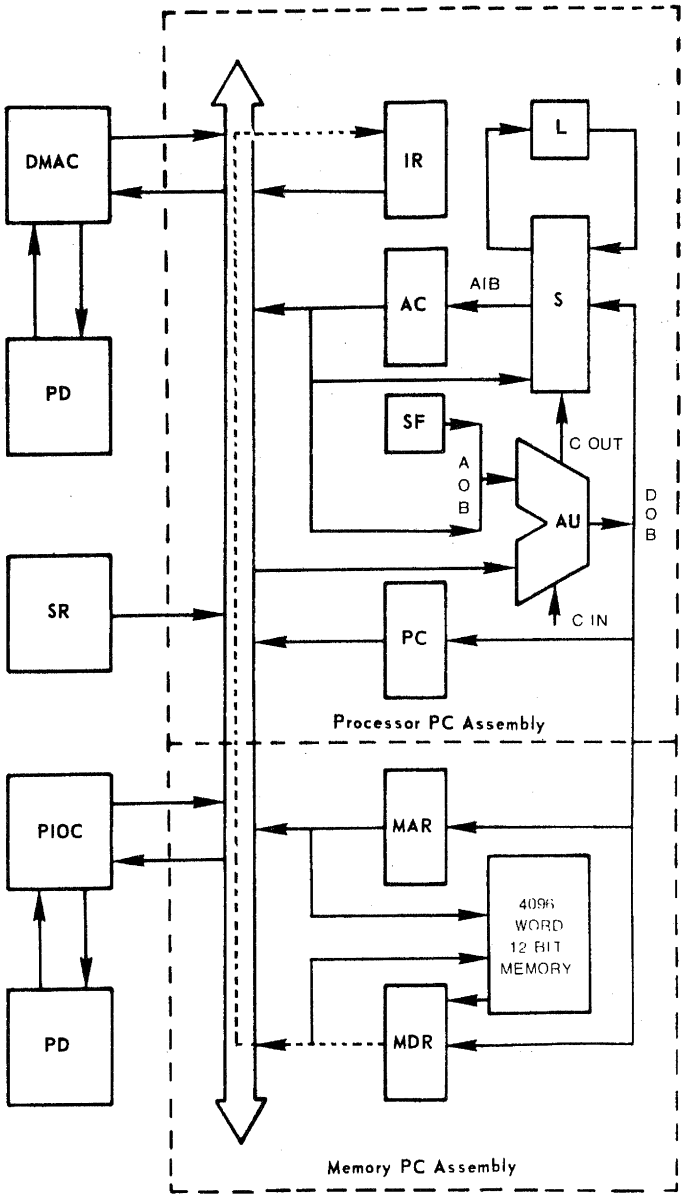
IOT INSTRUCTION

Instruction - IOT

State - Fetch
Time - PA

Signals Asserted
C-MD-DIB
/L-IR

Other Operations
Read Memory
Clear Skip Flip-Flop



Description

During the first half cycle of the Fetch state the instruction word is read from the memory storage elements and transferred to the Instruction Register by way of the Memory Data Register and Data Input Bus.

IOT INSTRUCTION

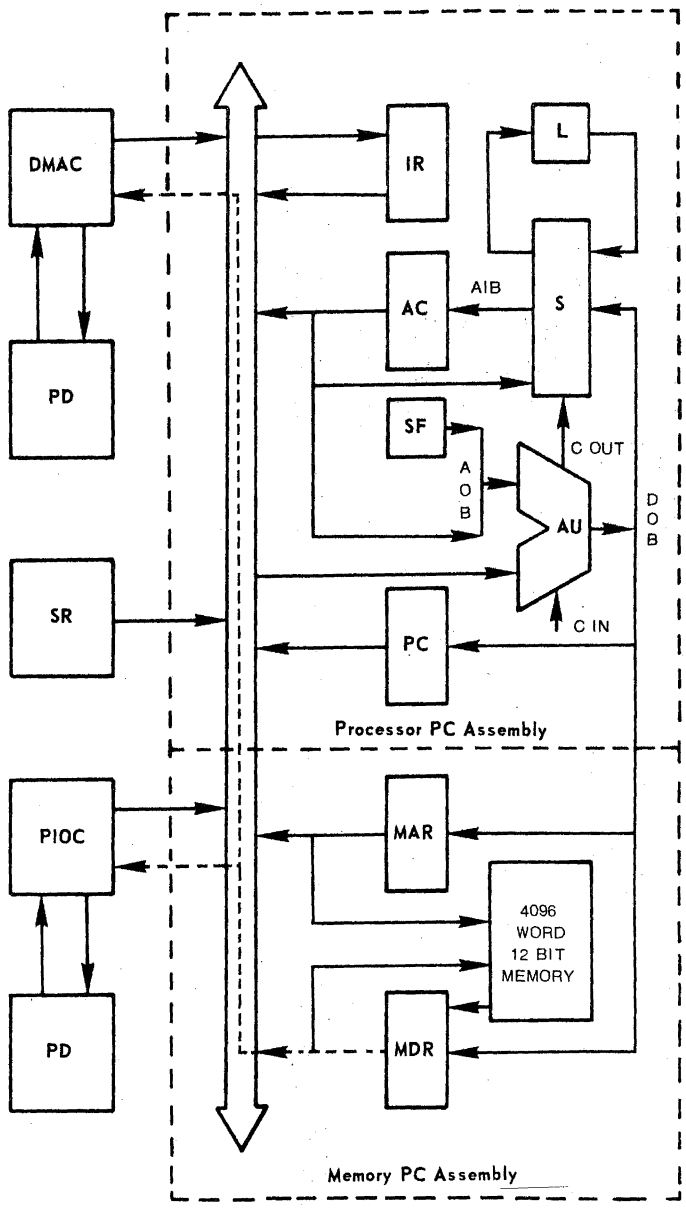
Instruction - IOT

State - Fetch
Time - PB

Signals Asserted
C-MD-DIB
/PIO-SELECT

Other Operations
Write Memory

Next State
Execute



Description

During the second half cycle of the Fetch state the instruction word contained in the Memory Data Register is transmitted to all peripheral controllers by way of the Data Input Bus. The peripheral controller addressed by the IOT instruction is selected and loads the control code field into the peripheral control register. The instruction word is restored to the memory storage elements by the write operation.

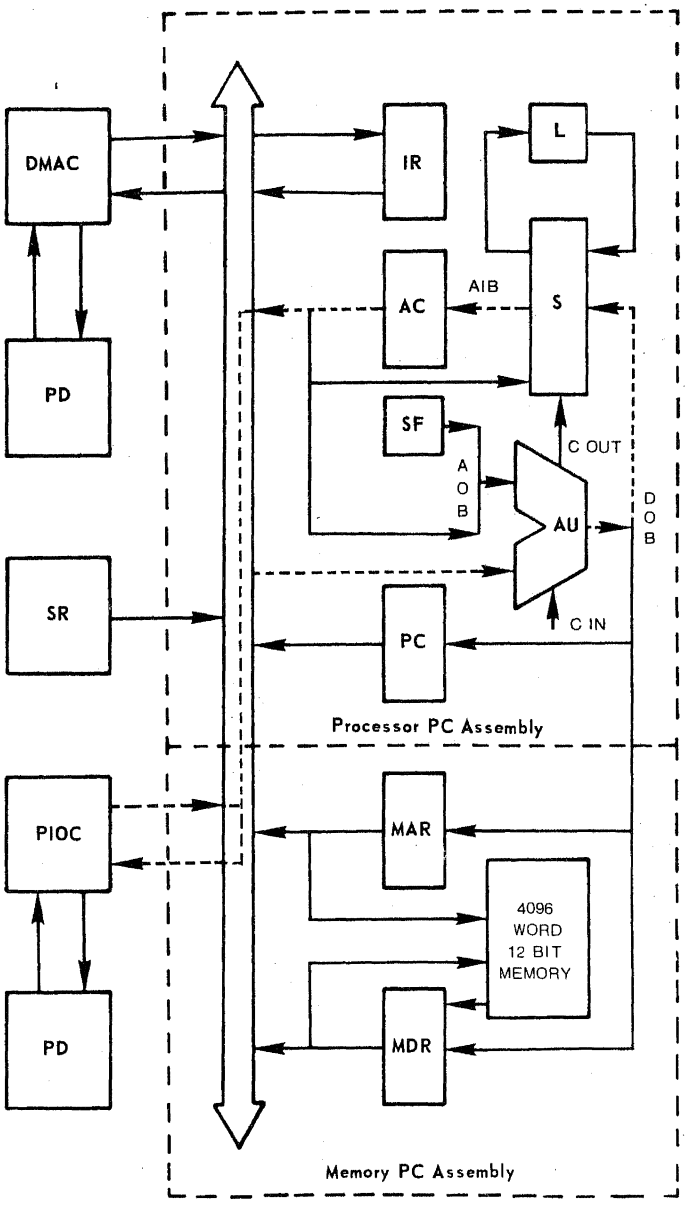
IOT INSTRUCTION

Instruction - IOT

State - Execute
Time - PA

Signals Asserted
- /PIO-CONNECT DATA
- /PIO-LOAD DATA
- C-AC-DIB If /PIO-DISCONNECT AC is not asserted

Other Operations
- Set Skip Flip-Flop If /PIO-SKIP is asserted



Description

During the first half cycle of the Execute state the Input/Output data word is transferred by way of the Data Input Bus, Arithmetic Unit and Shifter to the accumulator. The peripheral controller can connect data to the Data Input Bus or signal the processor to connect the accumulator data to the bus. The peripheral controller can set the skip flip-flop by asserting the /PIO-SKIP signal.

IOT INSTRUCTION

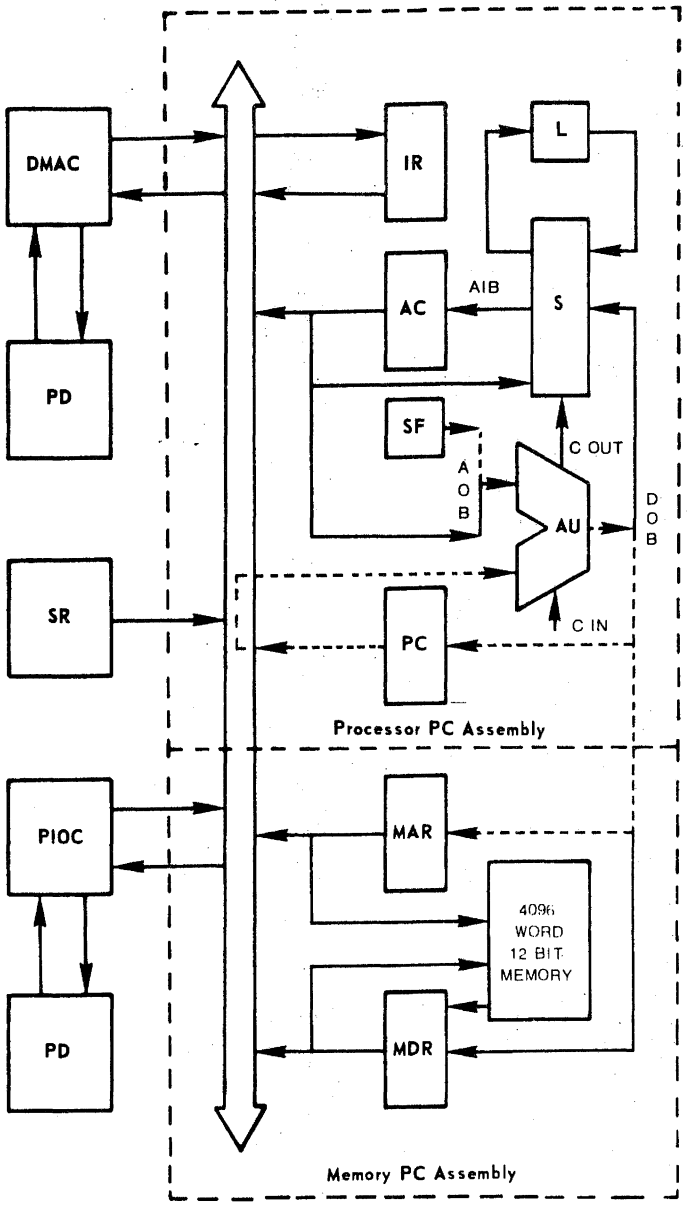
Instruction - IOT

State - Execute
Time - PB

Signals Asserted
- C-PC-DIB (00-04)
- C-PC-DIB (05-11)
- /C-IN
- /L-PC
- /L-MA
- C-SKIP-AOB

Other Operations
- Memory Write

Next State
- Fetch If Run = 1



Description

During the second half cycle of the Execute state the address of the next instruction to be executed is generated by adding one to the address contained in the Program Counter and transferring the result to the Memory Address Register and to the Program Counter.

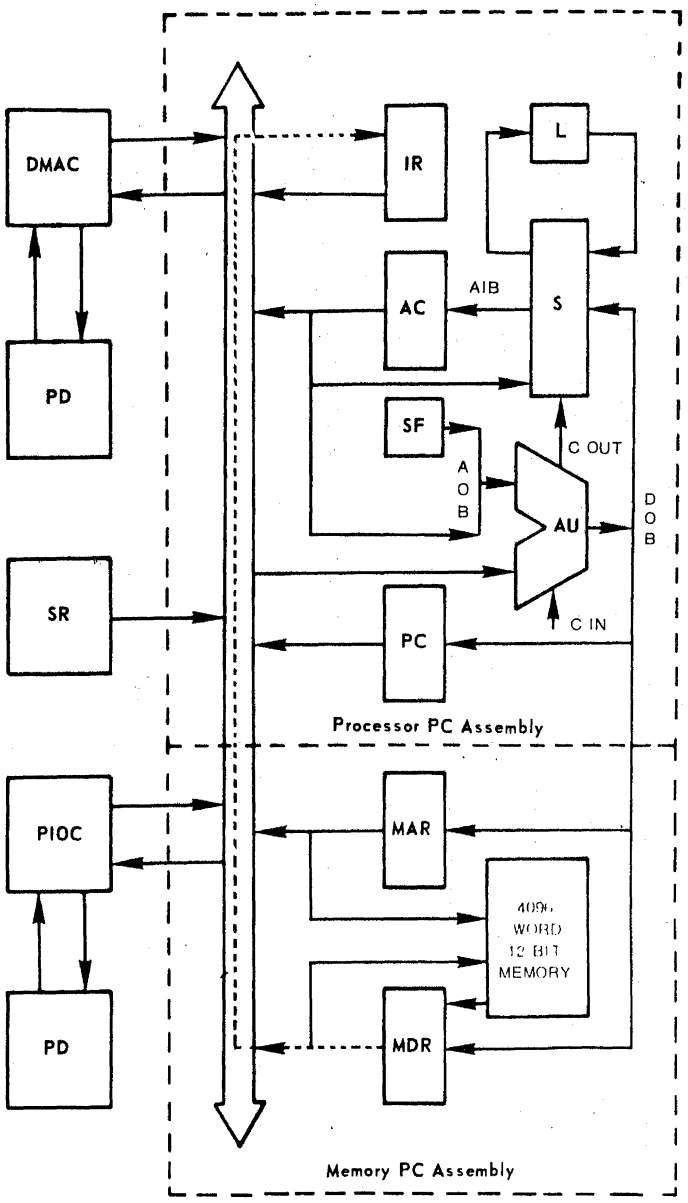
OPERATE GROUP 1 INSTRUCTION

Instruction - OPERATE GROUP 1

State - Fetch
Time - PA

Signals Asserted
C-MD-DIB
/L-IR

Other Operations
Read Memory
Clear Skip Flip-Flop



Description

During the first half cycle of the Fetch state the instruction word is read from the memory storage elements and transferred to the Instruction Register by way of the Memory Data Register and Data Input Bus.

OPERATE GROUP 1 INSTRUCTION

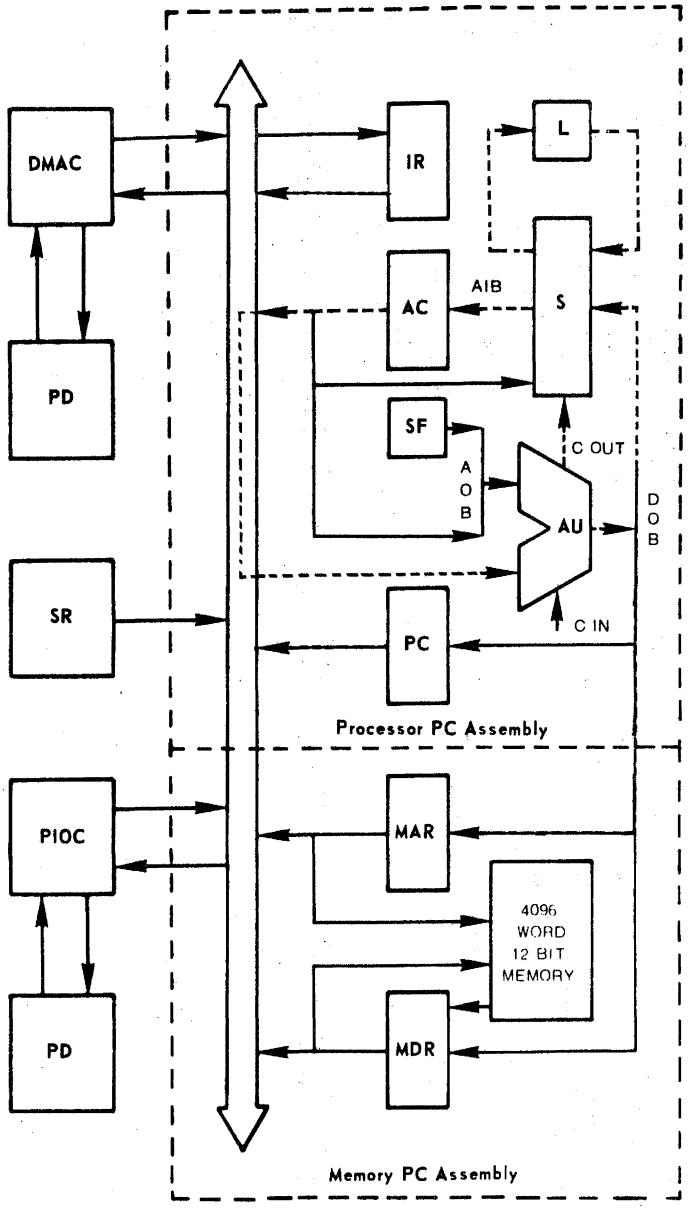
Instruction - OPERATE GROUP 1

State - Fetch
Time - PB

Signals Asserted
C-AC-DIB If IR04 ⊻ IR06 = 0
C-ACC-DIB If IR06 = 1
/C-IN If IR11 = 1
/L-AC

Other Operations
Link Result

L_n	IR05	IR07	C-OUT	L_{n+1}
0	X	0	0	0
0	X	0	1	1
0	X	1	0	1
0	X	1	1	0
X	1	0	0	0
X	1	0	1	1
X	1	1	0	1
X	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1



Next State
Execute

Description

During the second half cycle of the Fetch state sequence 1, 2, and 3 operations are performed in accordance with the micro-coded instruction word format.

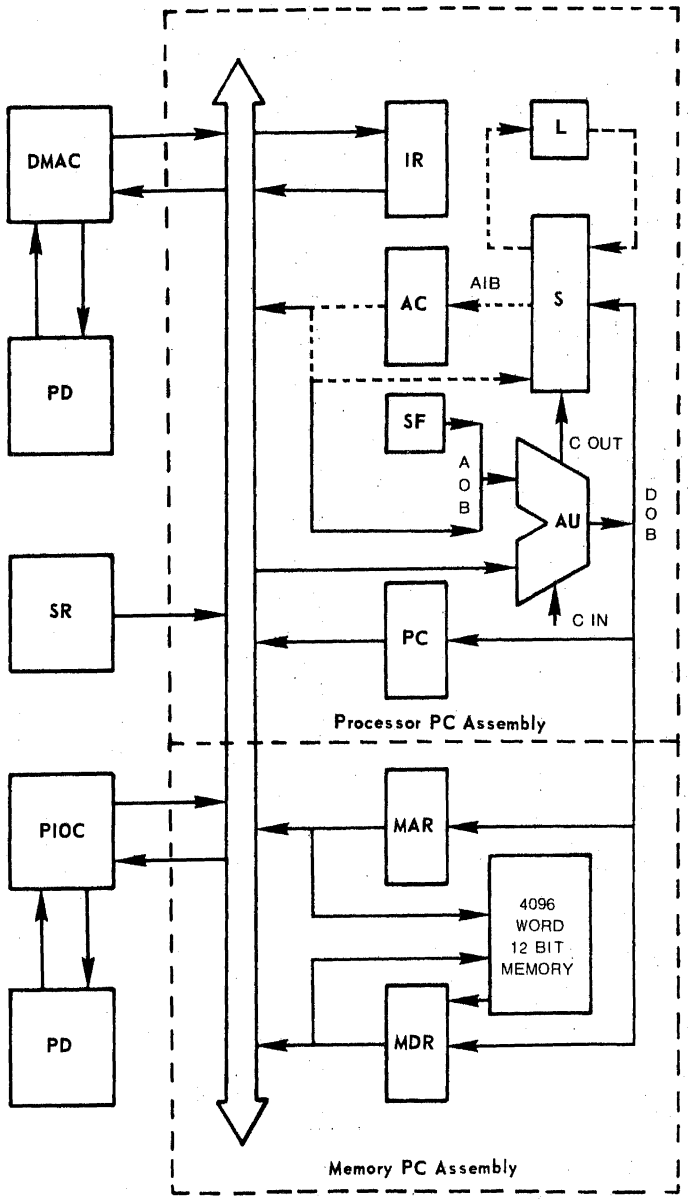
OPERATE GROUP 1 INSTRUCTION

Instruction - OPERATE GROUP 1

State - Execute
Time - PA

Signals Asserted
C-AC(RAR)-AIB If IR08 = 1
C-AC(RAL)-AIB If IR09 = 1
/L-AC If IR08 ∨ IR09 = 1

Other Operations



Description

During the first half cycle of the Execute state sequence four operations are performed in accordance with the micro-coded instruction format.

OPERATE GROUP 1 INSTRUCTION

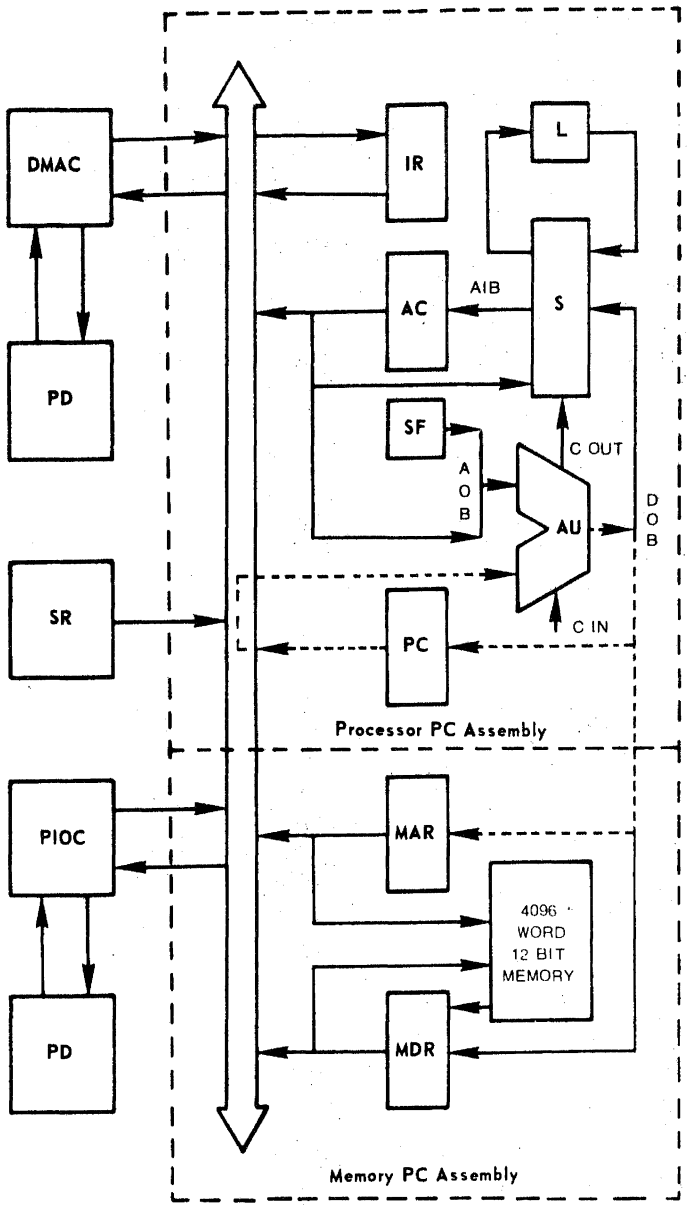
Instruction - OPERATE GROUP 1

State - Execute
Time - PB

Signals Asserted
- C-PC-DIB (00-04)
- C-PC-DIB (05-11)
- /C-IN
- /L-PC
- /L-MA
- C-AC(RAR)-AIB If IR08 IR10 = 1
- C-AC(RAL)-AIB If IR09 IR10 = 1
- /L-AC If (IR08∨IR09) IR10 = 1

Other Operations
- Memory Write

Next State
- Fetch If Run = 1



Description

During the second half cycle of the Execute state sequence five operations are performed in accordance with the micro-coded instruction format. The address of the next instruction to be executed is generated by adding one to the address contained in the Program Counter and transferring the result to the Memory Address Register and to the Program Counter.

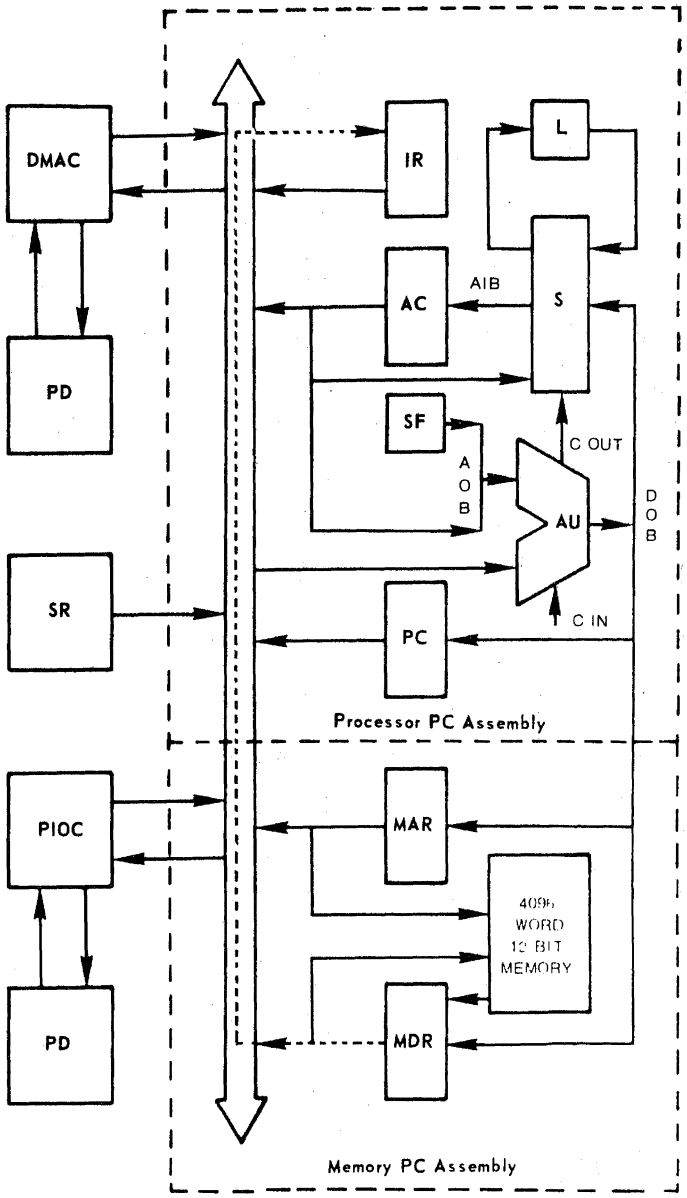
OPERATE GROUP 2 INSTRUCTION

Instruction - OPERATE GROUP 2

State - Fetch
Time - PA

Signals Asserted
C-MD-DIB
/L-IR

Other Operations
Read Memory
Clear Skip Flip-Flop



Description

During the first half cycle of the Fetch state the instruction word is read from the memory storage elements and transferred to the Instruction Register by way of the Memory Data Register and Data Input Bus.

OPERATE GROUP 2 INSTRUCTION

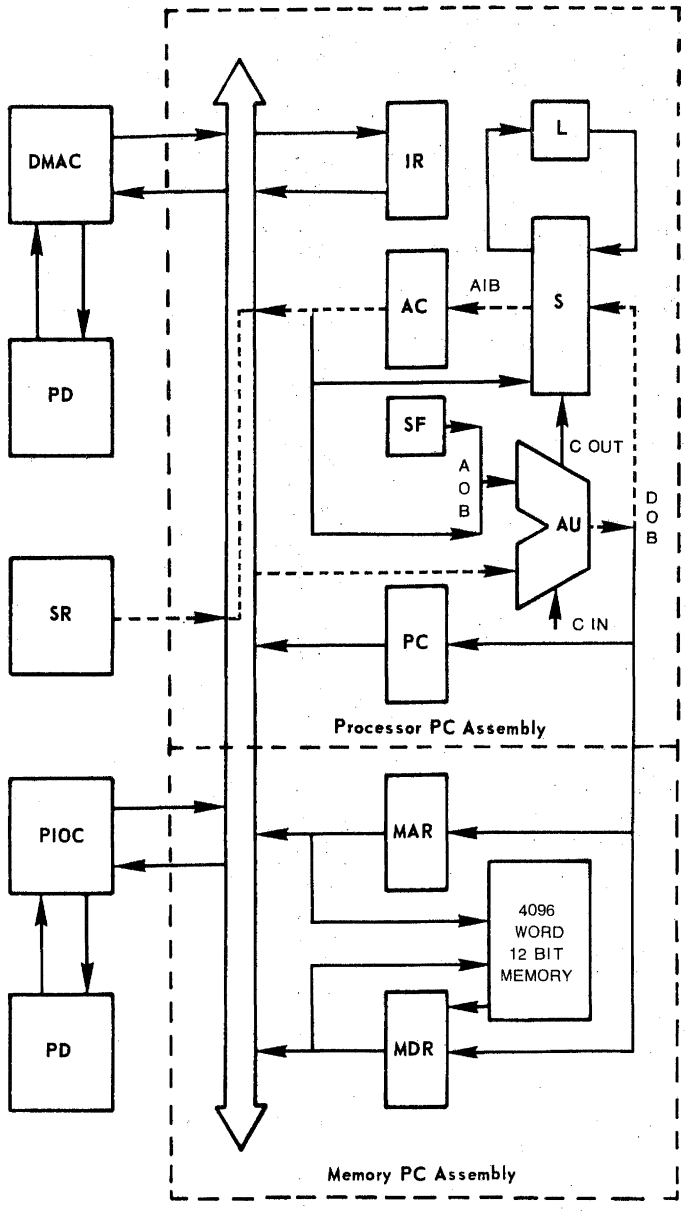
Instruction - OPERATE GROUP 2

State - Fetch
Time - PB

Signals Asserted
- C-AC-DIB If IR04 = 0
- C-SR-DIB If IR09 = 1
- HALT If IR10 = 1
- /L-AC

Other Operations
- Memory Write
- Test for skip condition specified by IR05-IR08 and set skip flip-flop if condition satisfied.

Next State
- Execute



Description

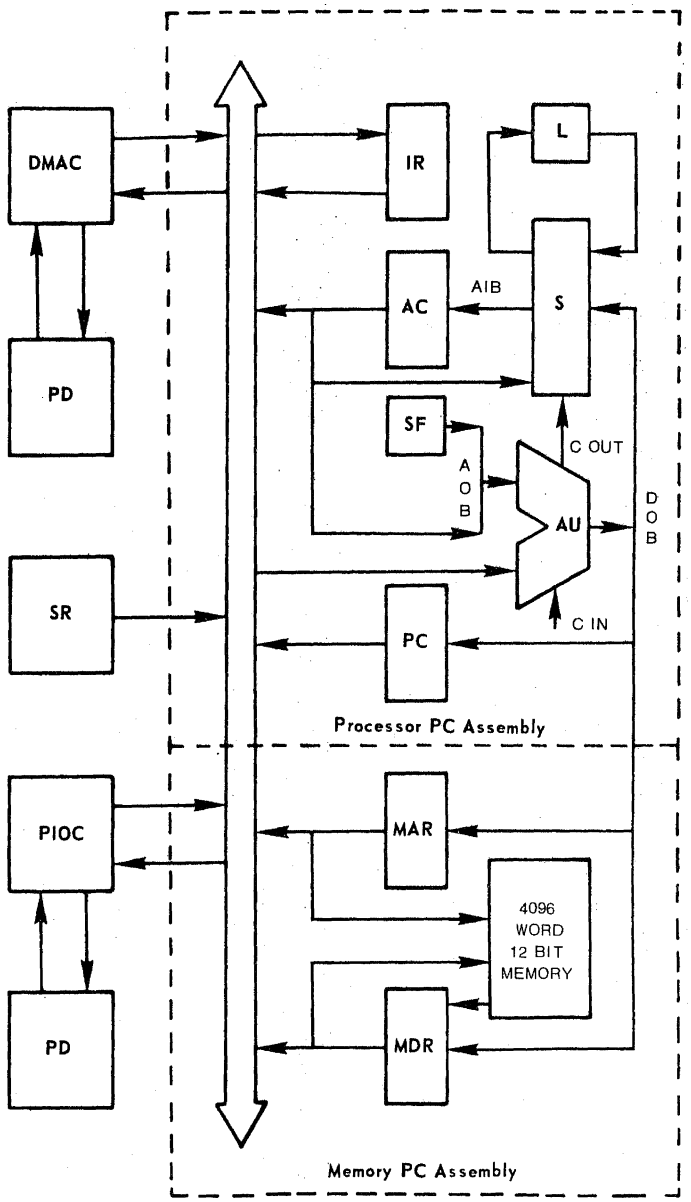
During the second half cycle of the Fetch state sequence 1, 2, and 3 operations are performed as specified by the micro-coded instruction word. The memory write operation restores the instruction word to the memory storage elements.

OPERATE GROUP 2 INSTRUCTION

Instruction - OPERATE GROUP 2

State - Execute
Time - PA

Signals Asserted
None



Description

During the first half cycle of the Execute state no operation is performed.

OPERATE GROUP 2 INSTRUCTION

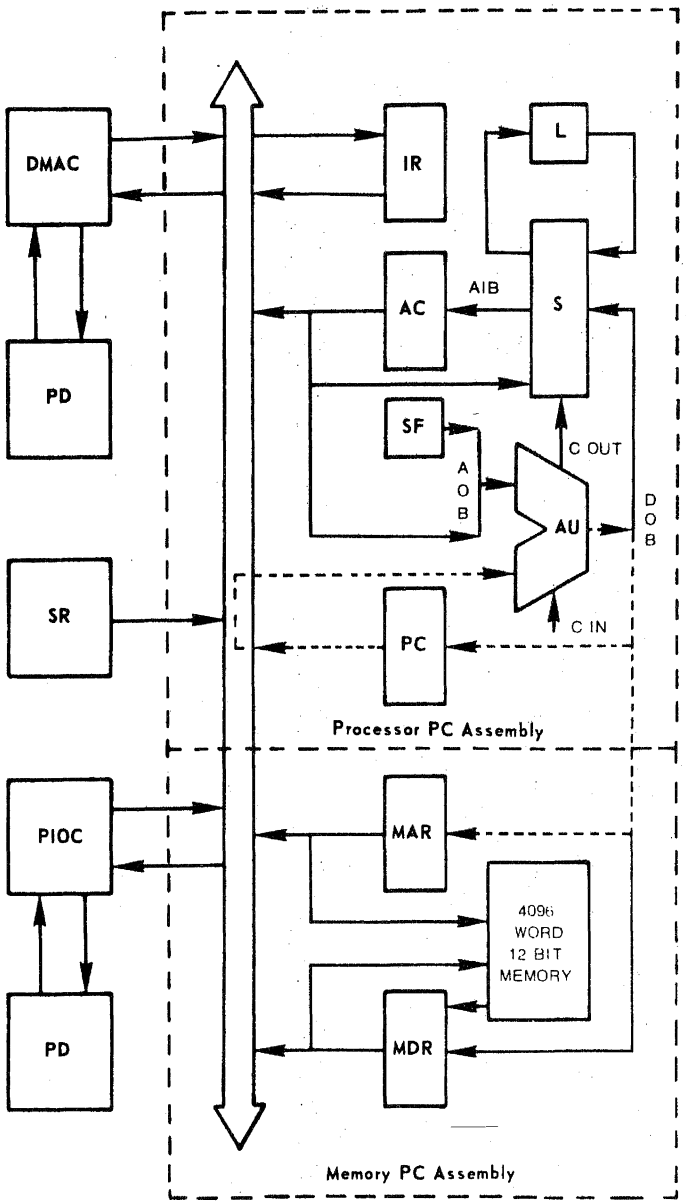
Instruction - OPERATE GROUP 2

State - Execute
Time - PB

Signals Asserted
- C-PC-DIB (00-04)
- C-PC-DIB (05-11)
- /C-IN
- /L-PC
- /L-MA
- C-SKIP-AOB

Other Operations
- Memory Write

Next State
- Fetch If Run = 1



Description

During the second half cycle of the Execute state the address of the next instruction to be executed is generated by adding one to the address contained in the Program Counter and transferring the result to the Memory Address Register and to the Program Counter.