SENTRY

RS232C VKT INTERFACE

Reference Manual

FAIRCHILD
SYSTEMS TECHNOLOGY
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

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PREFACE

This manual describes in detail the RS232C VKT Interface that is used in the Sentry V, VII and VIII test systems. Included are both software and hardware descripitions.

For additional and supporting material refer to the following manuals.

Sentry User's Manual 67095733
Sentry FACTOR Reference Manual 67095738
FST-2 CPU Peripheral Diagnostics 67095731
FST-2 CPI Interface Manual 67095734

The individual using this manual should have been through the Sentry programming and maintenance classes or should have had on the job experience with the Sentry system.

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SECTION 1

INTRODUCTION TO RS232C VKT INTERFACE

The RS232C VKT interface is a one card interface, compatible with the Sentry FST-2 computer. This one card interface meets EIA RS232C standards, and replaces the three card CRT controller presently used in the FST-2. (See Figures 1-1 and 1-2.)

Since this new interface conforms to EIA RS232C standards, the present TTL interfaced VKT can no longer be used. Replacing the Hazeltine 2000C I/O board with their standard RS232C I/O board, lets the 2000C interface the FST-2 with RS232C EIA levels.

The primary purpose of the RS232C VKT interface is to reduce the present three card controller, and update to EIA RS232C interface levels. At the same time, a second RS232C VKT interface is introduced to the FST-2 for the new foreground/background software.

These two RS232C VKT interfaces will reside in the A2 chassis. The two interfaces are assigned to the A2/F4 and A2/F6 slots.

The A2/F4 slot shall be for foregound and, thus, answer to SPUs with unit ADR of 30 and 20 for screen and keyboard respectively. The interrupt address shall be 3 and 2 for screen and keyboard respectively.

The A2/F6 slot shall be for background and, thus, answer to SPU with unit ADR of 31 and 21 for screen and keyboard respectively. The interrrupt address shall be 43 and 52 for screen and keyboard respectively.

Both VKT interfaces shall have interrupt priority of 2 and 1 for screen and keyboard respectively.

Both RS232C VKT interfaces communicate with the FST-2 CPU over the N BUSS on a character basis with full duplex capability.

The RS232C VKT interface has been designated an FST 97420113.

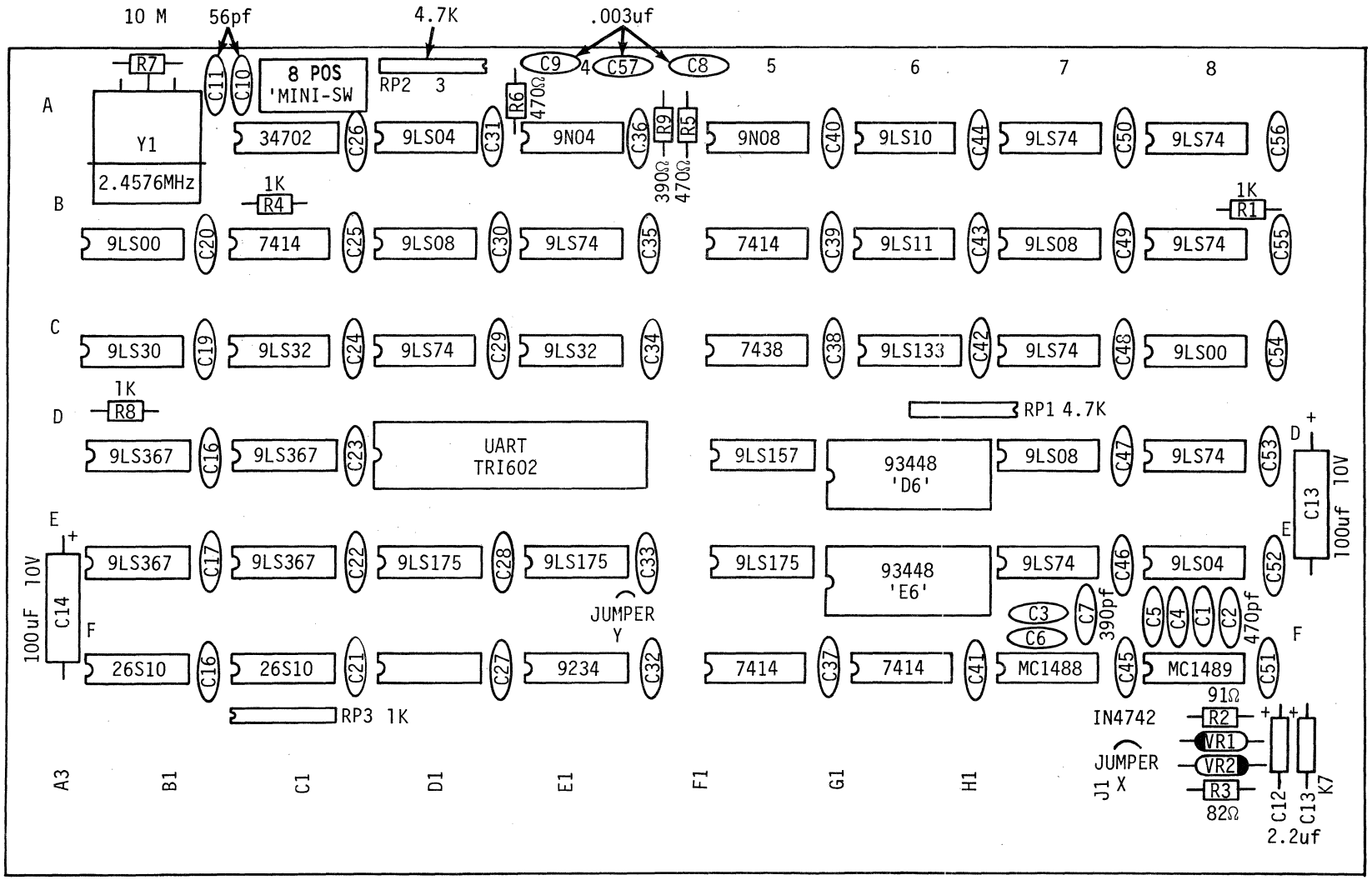
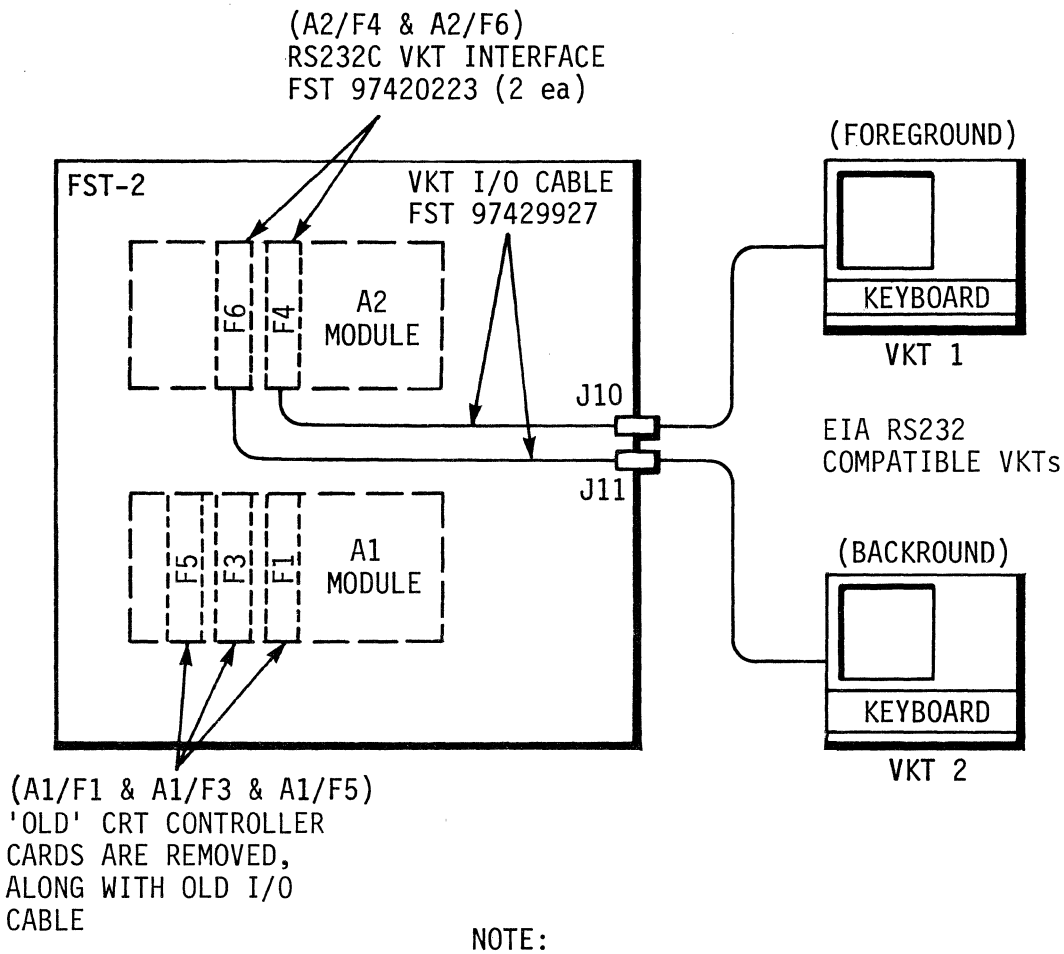


Figure 1-1 Component Location RS232C VKT Interface Board



NOTE:
Hazeltine 2000C uses standard RS232C I/O board (Hazeltine PN 5DTD150902).

Figure 1-2
Typical FST-2 Configuration with Dual RS232C VKT Interfaces

SECTION 2

LOGIC DESCRIPTION

2.1 OPERATIONAL PURPOSE

The RS232C VKT interface is primarily designed to accept parallel data from the FST-2 'N BUS', and transform this into serial data conforming to EIA RS232C standard. The serial data has start, stop and parity bits added and is sent to an RS232C compatible terminal. The terminal, in turn, transmits serial RS232C data (entered via operator) to the RS232C VKT interface. The VKT interface, in turn, transforms this serial RS232C data back to a parallel format, and notifies the FST-2 (via interrupt) that data is available for transfer to FST-2 via 'N BUSS'.

The VKT interface responds to 'SPU' commands with a 'unit select address' 30 and 20 for the screen and keyboard respectively. A second VKT interface responds to same commands, but with a 'unit select address' of 31 and 21 for screen and keyboard respectively.

Interrupts notify the FST-2 when a transmission to the terminals screen is complete, and also when data from the terminal is received. The two VKT boards operate with different interrupt address; however, they still maintain the same FST-2 priority of 2 and 1 for the screen and keyboard respectively.

The VKT interface used in the 'foreground' application issues an interrupt address of 3 and 2 for the screen and keyboard respectively, while the VKT interface used in the 'background' application issues an interrupt address of 53 and 52 for screen and keyboard respectively.

Since both VKT interfaces may try to interrupt simultaneously, priority is resolved between the two boards by address, so that only one can interrupt at a given time.

The VKT interface incorporates the following circuitry:

- FST-2 'N BUSS' Interface
- FST-2 Timing Interface
- FST-2 Address and Command Decoding
- Command Error Detection
- Screen (Printer) Status
- Keyboard (Reader) Status

- UART (Universal Asynchronous Receiver Transmitter)
- BAUD Rate Generator
- EIA RS232C Interface
- Screen (Transmission) Interrupt
- Keyboard (Receiver) Interrupt
- Screen (Printer) Interrupt Status
- Keyboard (Reader) Interrupt Status

2.1.1 FST-2 'N BUSS' Interface

See Figure 2-1A.

At the top left corner, two 26S10s F1 and F2 are quad buss transceivers, which interface to FST-2 'N BUSS' bits BNØØ through BNØ7. All data for transmission or reception travels to or from 'N BUSS' via these two buffers. Pins F1-12 and F2-12 when low, enable F1 and F2 to put data out to the 'N BUSS'. When F1-12 and F2-12 are high (+5v) F1 and F2 act as receivers only.

Devices F5, F6, B5 and B2 are Schmitt Trigger (7414) Receivers which transfer command information from the N BUSS to the VKT interface. They also offer hysterisis for line noise immunity.

On the right side of Figure 2-1A, device C5 is a line driver for 'N BUSS' status bits BN2Ø through BN23. The driver is enabled by device A5-3 (9N08) going high (+5v).

2.1.2 FST-2 Timing Interface

The timing signals brought from the FST-2, along with their descriptive use are as follows:

See Figures 2-1A and 2-1B.

A. T1 comes from the FST-2 via device B2 (Figure 2-1A, left, bottom), and is used for two purposes:

   1. I/O commands are initiated at T1 time via device B1 (9LS00). These commands put one of the following on line to FST-2:

      a. Received data via device B1-3 enabling C1-12 (9LS30 driver enable) and D2-1 and 15 and E1-15 (9LS367 rec. data tri-state buffer).

      b. Transmit data reg. load via device B1-6 giving S. WRITE/ which goes to Figure 2-1A devices E3-9 and E4-9 (9LS175 data latch enable) at the end of T1 time, data 0D0-0D7 from Figure 2-1A devices F1 and F2 (receivers) are loaded into latches E3 and E4.

c. Keyboard (reader) interrupt status via device B1-8 enabling device D1-1 (9LS367 tri-state buffer).

d. Screen (printer) interrupt status via device B1-11 enabling device E1-1 (9LS367 tri-state buffer).

2. T1 also goes to Figure 2-1B device D7-10 to clock off interrupt address circuit, once an address has been issued the previous T5 cycle.

B. T2 comes from FST-2 via device B2 (Figure 2-1A, left, bottom) and is used to reset the command I/O register (E5 (LS175)) after commands are issued at T1 time. T2 is also used to clock device E7-3 (Figure 2-1B) the printer busy F/F.

C. T5 comes from FST-2 via device F5 (Figure 2-1A, left, bottom) and is used for three purposes:

1. Reset 1/2 of command error F/F device C3-13 (Figure 2-1A).

2. Enable interrupt address issuing via device F5-6 which feeds Figure 2-1B device C8-10 and 5.

3. Clock Reader Busy flip flop B4-3 and B4-11 (Figure 2-1B).

D. PS comes from device F5-2 (Figure 2-1A, left, bottom) and enables F3-1 and F4-1 (9324 comparators) during PS (unit select) time to see if the VKT board's address is being selected.

E. CP3 comes from device B5-12 (Figure 2-1A, left, bottom) and is used from three purposes which are as follows:

1. CP3 is used during last protion of PS cycle to determine whether a command error exists. CP3 via B5-12 enables B3-1 (9LS08) during last portion of PS cycle.

2. CP3 via B5-12 goes to Figure 2-1B device B6-13, and enables an interboard priority between VKT board #1 and VKT board #2, which decides which board will generate an interrupt address.

3. CP3 via B5-12 goes to Figure 2-1B device B7-5 and 10, and enables B7 to look for Sentry System Priority during GPINT time.

F. RESET (from the FST-2 panel) comes from device B2-6 (Figure 2-1A) and goes to D3-21 (Figure 2-1B) to reset the UART.

G. RESET/ comes forn A4-12 (9N04) and resets the I/O command register via devices D7-3 (9LS08) to device E5-1 (9LS175). It also resets the command error F/F C3-1 (9LS74) and goes on to Figure 2-1B. On Figure 2-1B as MRST/ it resets the screen interrupt logic via B7-3 (9LS08) and the keyboard interrupt logic via B7-11. It also resets the transmitter data registers E3-1, and E4-1 (9LS175s). Reset/ also resets the Printer Busy and Keyboard Busy F/F E7-1 and B4-13 respectively. Thus, it can be seen that depressing the FST-2 Panel Reset Switch will initialize all logic to a zero holding state.

H. T4 comes into Figure 2-1B via B5-3 (left, middle), and is used via B5-6 (7414) as a time enable for interboard priority decisions.

I. IP (interrupt priority) comes via Figure 2-1B device B5-11 (7414), and is used to issue gated priority to other FST-2 boards if an interrupt request, and a PON condition is met. This is done via device A6-5 and 10 (9LS10).

2.1.3 FST-2 Address and Command Decoding

See Figure 2-1A.

At PS time comparators F3 and F4 look for the select address of their unit. The least significant bit for compare, can be modified from a '0' to a '1' by switch S1-5 through inverter A3-2 to device F3-3 (9324). When two VKT interface boards are used, S1-5 goes to the 'ON POSITION' on VKT INTF #2, which modifies it's unit select to a 1. S1-5 also feeds E2-10 and 14 via device A3-2, which modifies the interrupt address second LSB to a '5' (OCTAL CODE). Therefore, VKT INTF #2 ends up with a different unit select address, and a different interrupt address than VKT INTF #1.

If at PS time, the comparators F3 and F4 determine the unit address has been selected, they enable PROM D6 and E6 to decode the command instruction via A5-3 (9N08) to A4-2 (9N04) to D6-20 and E6-20 (93448). The I/O cycle command register E5-9 (9LS175) is also enabled at this time.

There are two types of instructions to decode: one is interface only commands, and the other are I/O commands (data to transfer). PROM D6 is programmed to decode all interface only commands, and PROM E6 (93448) is programmed to decode all I/O cycle comands. The I/O cycle commands from PROM E6 are latched at the end of PS, and are executed the following T1 cycle via device B1 (9LS00).

A detailed description of the Command Decoding can be found on page of this manual.

2.1.4 Command Error Detection

See Figure 2-1A.

During a PS cycle, if our unit address is on 'N BUSS' bits BN00-BN07 and 'N BUSS' bits BN11, BN14, and BN15 are low, the comparators F3 and F4 give an A=B on pin 14. This signal becomes address select via A5-3 (9N08) and enables C6-1 (9LS133) to look for any command being decoded from PROM D6 or PROM E6.

The output of C6-9 (9LS133) is monitored during the PS cycle by B3-9 and B3-5 (9LS08). B3-3 (9LS08) enables B3-10 and B3-4 at CP3 time during the PS cycle, when our unit is addressed. At that time, if no valid commands are decoded (C6-9 is high for a valid decode) B3-8 will pulse high for the duration of CP3 time. In turn, A3-6 (9LS04) will pulse low, setting F/F C3-4 (9LS74). C3-5 (Q output) is the command error flag, and goes to mux chip D5-6 and 5 which places the error flag into the screen and keyboard status registers respectively. C3-5 also acts as an inhibit signal at C2-2 and 10, which will be explained later. C3-5 (Command Error Flag) is also sent to E1-10 and D1-10 the screen and keyboard interrupt status registers.

The command Error Flag on C3-5 can be cleared by either 1 of 2 events occurring. If, on the next PS cycle, a valid command occurs, then B3-6 will pulse high, and feeds C2-5 (9LS32) which clocks C3-3 (9LS74). C3-2 (9LS74) has a ground for its data input, thus the clock from C2-6 (9LS32) will clear the 'Q' output and thus the command error flag on C3-5 (9LS74). The second event which could clear the command error flag is during the next PS cycle, with our unit address, a read screen interrupt status or read keyboard interrupt status (both are I/O cycle commands) is latch at E5-7 or E5-2 respectively. Then upon the execution of either of these commands (the following T1 cycle) B3-11 (9LS08) will clock C3-11 which in turn presents a high on C3-9, which feeds via C2-6 (9LS32) to C3-3 (9LS74) and thus clocks C3-5 to a low, or resets the command error flag. Device C2-3 and 8 (9LS32) are inhibited (by the command error flag) so that the screen or keyboard interrupt status registers may be read without resetting the command error flag, until after the event happens.

2.1.5 Screen (Printer) Status

See Figure 2-1A.

F/F E7-5 and 6 (9LS74 Figure 2-1B) give the screen status of busy, and idle respectively. F8-4 (1489 Figure 2-1B) has the signal VKT DSR coming in on I/O pin J9. This signal from the terminal, is inverted by F8-6 to become DSR/. As long as the terminal remains on line F8-6 will be low; however, should the terminal go off line (local), F8-6 will go high letting us know the terminal is off line.

During system intitialization (FST-2 reset switch depressed) F/F E7-1 and 13 (9LS74) are reset by the signal MRST/ (derived from Reset/ (A4-12 on Figure 2-1A). This initialization puts PRT IDLE high (5v) and PRT BUSY low on E7-6 and 5 respectively (Figure 2-1B). If the terminal is on line E8-10 (9LS04 Figure 2-1B) will hold a high on the data input of F/F E7-12 (9LS74 Figure 2-1B). At this time, if the I/O command S. WRITE occurs at E7-11 (9LS74) the F/F will clock a high to E7-9 at the end of T1. At the end of T2 time, E7-5 will go high (PRT BUSY) and E7-6 will go low (PRT IDLE). These two signals along with DSR/ from F8-6 are fed to a mux device D5 (9LS157 Figure 2-1A). These signals along with the command error flag from C3-5 (9LS74 Figure 2-1A) make up the screen (printer) status register signals.

During a PS cycle, with PROMs D6 and E6 (93448 Figure 2-1A) decoding screen commands the mux device D5 (9LS157) will place the screen (PRT) status signals to buss driver C5 (9N38) which in turn drives the buss as follows:

A. BN20/ becomes DSR/

B. BN21/ becomes PRT BUSY/

C. BN22/ becomes COMD ERR/

D. BN23/ becomes PRT IDLE/

In this way, the FST-2 is able to read the status of the screen (printer) circuitry of the RS232C VKT INTF board.

2.1.6 Keyboard (Reader) Status

See Figures 2-1A and 2-1B.

F/F B4-5 and 6 (9LS74 Figure 2-1B) gives the keyboard status of IDLE, and BUSY respectively.

During system initialization, (FST-2 reset switch depressed), F/F B4 (9LS74 Figure 2-1B) is reset by the signal MRST/ (derived from Reset/ (A4-12 on Figure 2-1A)). This initialization puts RDR BUSY high (+5v) and RDR IDLE low on B4-6 and 5 respectively, the following T5 time. The initialization also resets the UART D3-2 (Sheet 2), which in turn places D3-19 (Data Available) signal low. This signal feeds to B4-2 as a data signal.

When the UART (D3 Figure 2-1B) receives a serial data byte from the terminal, D3-19 the data available signal, will go high. This puts the B4-2 data input high, thus the next T5 clocks B4-3 making RDR BUSY low, and RDR IDLE high, B4-6 and 5 respectively. These signals along with DSR/ from F8-6 are fed to mux device D5 (Figure 2-1A). Command error from C3-4 (9LS74 Figure 2-1A) is also fed to device D5 as a status signal.

During a PS cycle, with PROM D6 (93448 Figure 2-1A) decoding Read Commands, B6-6 (9LS11) will go low, causing the mux device D5 (9LS157) to select and place the keyboard status signals to buss driver C4 (9N38), which in turn drives the buss as follows:

A. BN20/ becomes DSR/

B. BN21/ becomes RDR BUSY/

C. BN22/ becomes COMD ERR/

D. BN23/ becomes RDR IDLE/

In this way, the FST-2 is able to read the status of the keyboard (reader) circuitry of the RS232C VKT INTF board.

2.1.7 UART (Universal Asynchronous Receiver Transmitter)

See Figure 2-1A.

A. UART Description

UART means Universal Asynchronous Receiver and Transmitter. The four registers listed below are contained within the device:

1. Transmit Data Input Register
2. Receiver Data Output Register
3. UART Status of Operation Register
4. UART Mode Control Register

The UART is used in an asynchronous manner indicating that the transmit function is independent of the receiver function. A single clock called Baud Rate (data bit transfer rate) is used to serialize and de-serialize transmit and receive data (both operating at the same clock rate). The basic function of a UART is to convert parallel input transmitter data to serial, add start, stop and parity bits to the input data, then transmit this in serial format to a receiver of like kind. The receiver accepts the start bit, then retrieves the serial received data and checks it for parity, framing or overrun errors. The last thing the receiver does, is convert the serial received data to a parallel format and place it in the receiver data register.

The UART D3 (Figure 2-1B) is connected in such a manner that full duplex (simultaneous receive and transmit) operations may take place. Both the transmitter and receiver sections have separate interrupt logic paths which allow the full duplex operation to take place.

B. Transmitter

Latches E3 and E4 (9LS175s Figure 2-1B) make up the transmitter data latch. When S. WRITE is decoded during a PS cycle, the following T1 cycle will initiate S. WRITE/ (strobe write), which at the end of the T1 cycle will latch the transmit data, available on 0D0 through 0D7 from the 'N BUSS'.

The same S. WRITE/ which latches the transmitter data also clocks E7-11 (9LS74 Figure 2-1B). This causes E7-9 to go high, and E7-8 to go low. E7-9 provides an enable signal to E7-2 and D7-12 (9LS08). E7-3 will be clocked at the end of the next T2 time which causes E7-5 to go high and E7-6 to go low, PRT BUSY and PRT IDLE respectively. E7-9 being high, also enables D7-12 (9LS08) to look for a CTS (clear to send) from the RS232C buss. E7-8 being low causes F7-8 (1488) to raise the RTS (Request to Send) signal on the RS232C buss. The RS232C buss upon seeing the RTS flag, will raise the CTS (Clear to Send) flag going to F8-10 (1488) via I/O pin J8. This CTS signal goes via E8-8 to the pulse network D7-11 and A4-8 (9N04) which provides an approximate 2us strobe to the UART D3-23. The UART upon receipt of this strobe will then transmit the data contained in latches E4 and E3 (9LS175s).

Upon completion of the transmission, the UART will raise its EOC (End of Character) flag on D3-24. This flag goes to pulse network A4-12 (9N08) and A4-6 (9N04) which pulses and resets E7-13 (9LS74) the RTS F/F. This causes E7-5 to go low at the end of the next T2 clock at E7-3. This results in PRT Busy going low, and PRT Idle going high. At the same time, the EOC flag goes to B6-10 (9LS11), and if DSR is high (from E8-10 9LS04), and RTS/ is high from E7-8 (9LS74), then A7-2 is enabled with a high for an interrupt request. A7-3 (9LS74) upon receipt of the next IP signal will clock the interrupt request into the interrupt circuitry.

C. Receiver

When the UART D3 (Figure 2-1B) has received a serial byte of data and transformed this into a parallel format and loaded it into the UART receiver register, it raises the DA (Data Available) flag on D3-19.

This DA flag places a high on B4-2 (9LS74). The next T5 clock will then clock B4-5 high, and B4-6 low. This drops the normally high RDR BUSY (B4-6), and raises RDR IDLE (B4-5). The RDR IDLE feeds B4-12 and A7-12 (9LS74). The next IP will clock A7-9 high, thus giving an interrupt request to the interrupt circuitry. The next T5 will clock B4-9 high, and when the E6 Prom decodes RD, the following T1 SRD/ will reset B4-5. This causes the next T5 to clock B4-9 low which causes the pulse network A4-12 and A4-4 (9N04) to produce an approx. 2 s pulse, which resets the DA (Data Available) flag on D3-18.

In this way the FST-2 is able to retrieve receive data from UART, and the RDR BUSY or RDR Idle status signals.

2.1.8 Baud Rate Generator

See Figure 2-1B.

The baud rate generator consists of the one chip A2 (34702), and a 2.4576MHz crystal reference, along with four programmable switches to select the baud rate.

The UART requires a frequency 16X the selected baud rate, and thus this is what A2 generates from pin 10.

The baud rate is programmable per the switch settings of S1-1 through S1-4, with rates available per the following chart:

PROGRAM BAUD RATE

BAUD RATE	S1-1	S1-2	S1-3	S1-4
300	OFF	ON	OFF	OFF
1200	OFF	OFF	ON	OFF
2400	ON	ON	OFF	OFF
4800	OFF	ON	ON	OFF
9600	ON	ON	ON	OFF

2.1.9 EIA RS232C Interface

See Figure 2-1B.

Devices F7 and F8, MC1488 and MC1489 respectively make up the RS232C interface to a terminal. The terminal, in turn, also will have an RS232C interface. Basically, the MC1488 (F7) is a driver level convertor, and the MC1489 (F8) is a receiver level convertor. Per EIA RS232C specifications, the levels on the buss between terminal and interface should be converted from '0v' and '5v' logic levels to mark and space levels respectively. The mark level is defined as a -4v to -15v level, while the space level is defined as a +4v to +15v level.

Therefore, the purpose of the MC1488 (F7) is to convert '0v' and '+5v' logic levels from the VKT interface to -12v and +12v logic levels on the RS232C buss. Consequently, the MC1489 (F8) is to convert -12v and +12v logic levels from the RS232C buss, back to '0v' and '+5v' TTL logic levels used by the VKT interface board.

The data transfer from VKT interface to terminal, and from terminal to VKT interface is serial 7 bit ASCII. This ASCII data has start, stop, and parity bits added, which are detected and removed by the UART (D3 Figure 2-1B). F7-3 (1488) is the serial transmitter data line, while F8-13 (1489) is the serial receiver line of the RS232C buss.

A. Transmit

With the terminals DSR (data set ready) signal on, and the decoding of S. WRITE/ at T1 time, E7-8 (9LS74 Figure 2-1B) will be clocked low, which goes to F7-9 and 10 (1488) who, in turn, raises the RTS (request to send) flag via F7-8 on the RS232C buss. From previous descriptions you will also recall that transmitter data is latched by E4 and E3 (9LS175s) at the same time.

When the CTS (clear to send) flag comes true at F8-10 (1489), the minus OR gate (D7 9LS08) will go high causing the pulse network A4-8 (9N04) to issue an approximate 2 us data strobe to UART D3-23. This will start the parallel to serial conversion, and the UART will add the start, stop, and parity bits to the serial ASCII data.

Upon the last bit of the serial character being transmitted via F7-3 (1488), D3-24 will raise its EOC (end of character) flag which eanbles 7A-5 upon the next IP clock to generate the interrupt request to the interrupt circuitry.

B. Receive

The terminal raises its RLSD (receive line signal detector) line on the RS232C buss which goes to F8-1 (1489). This signals via F8-3 to C4-10 (9LS32) removes the UART receiver (D3-20) from the mark state, and thus, enables us to now receive serial data from the terminal. The terminal, in turn, will now send its serial data character into the interface via F8-13 (1489) to C4-9 (9LS32) to D3-20 (UART).

Upon processing the received serial character (removing start, stop, and parity bits, and converting to parallel format) the UART will raise its DA (data available) flag which enables B4-5 upon the next T5 clock to generate the interrupt request to A7-12. A7-9 then clocks the interrupt request to the interrupt circuitry upon the IP clock.

The signal DTR (data terminal ready) on F7-6 will go high when power is applied to the interface. This is our signal to the terminal, via the RS232C buss, to tell him we are up and 'ON LINE'.

I/O pin J2 has the common signal ground line between the terminal and VKT interface board, while chassis ground on I/O pin J5, can be jumpered to ground via Jumper 'X', if required. Our 5V RTN is also chassis ground on the FST-2.

2.1.10 Screen (Transmission) Interrupt

See Figures 2-1A and 2-1B.

The UART, upon end of transmission, requests a transmitter done interrupt via B6-10 (9LS74 Figure 2-1B). B6-8 feeds A7-2 (9LS74 Figure 2-1B) which, upon receipt of the next IP (interrupt priority) signal latches the transmitter done interrupt request on A7-5 (9LS74). If PRT PON/ has set C7-4 (9LS74), then A6-3 (9LS10) will be enabled, and thus, upon receipt of the IP signal on A6-5 (9LS10) a signal called PRT GPINT/ (printer gate priority interrupt) will be issued from A6-6. PRT GPINT/ goes via A5-6 (9N08) to Figure 2-1A as GPINT/. GPINT/ enables the priority register D1-15 (9LS367) Figure 2-1A, and buss drivers F1-12 and F2-12 (26S10 Figure 21A). Thus, the VKT interface places its priority interrupt bits on line for an interrupt priority.

Note that D1-14 (9LS367 Figure 2-1A) is always high (Bit 0) by going to pull up resister R8 (Figure 2-1A). D1-12 is dependent on RDR GPINT/ for a low, otherwise is always high. This means if only the receiver is interrupting, only 'Bit 0' is active for the priority poll, however, should the transmitter try to interrupt, then both 'Bit 0' and 'Bit 1' will be active. The drivers F1 and F2 (26S10s (Figure 2-1A)) simply invert and drive the buss during this priority polling.

A6-6 (9LS10 Figure 2-1B) also feeds the data input of F/F A8-2 (9LS74 Figure 2-1B). During the last portion of GPINT/ (IP TIME) if nobody of higher priority enables C8-2 (9LS00), Then B7-10 (9LS08 Figure 2-1B) will be enabled by CP3 to clock A8-3. The Sentry priority resolution is made at this time, and if A8-3 (9LS74) is clocked, then A8-6 goes high and enables the interrupt address F/F B8-12 (9LS74 Figure 2-1B).

During T4 time, a VKT 1 and VKT 2 priority is resolved. At the end of IP time A8-5 (9LS74 Figure 2-1B) goes low, and feeds D7-4 (9LS08 Figure 2-1B) which generates the interboard signal VKT PRI OUT/. At the last portion of T4 time B6-2 (9LS11) is enabled with a high, if VKT 2 (higher address) is not trying to interrupt. B6-12 will then issue a clock to B8-11 (9LS74) at CP3 time.

When B8-11 (9LS74 Figure 2-1B) is clocked at CP3 time of T4 time, B8-9 goes high enabling C8-9 (9LS00). C8-10 (9LS00) will receive the T5 clock (issue interrupt address clock) causing C8-8 to issue PRT GINTAD/. This signal via minus OR A5-8 goes to Figure 2-1A as GINTAD/ (gate interrupt address).

GINTAD/ enables the buss drivers F1-12 and F2-12 via C1-9 (9LS130 Figure 2-1A), and also enables the interrupt address register E2-1 (9LS367 Figure 2-1A). As can be seen, A3-2 (9LS04) depends on S1-5 switch setting, off or on LSB '0' or '1' respectively, which in turn feeds the interrupt address register E2-14 and E2-10. In this way, when interface address LSB=1, then the interrupt address will issue a 53 address instead of 3.

RDR GINTAD/ (a high when printer is interrupting) feeds E2-6 (9LS367) which changes the normal reader address of 2 to 3 by activating Bit 0 of the interrupt address register. In this way, the screen (printer) interrupt address is issued to the 'N BUSS'.

On Figure 2-1B, when the PRT GINTAD/ is issued from C8-8 at T5 time, then at the end of T5, D8-3 (9LS74) will be clocked. Once D8-3 is clocked, D8-6 will go low and hold B8-13 (9LS74) the interrupt address enable F/F in the reset mode. This circuit ensures that an interrupt address in only issued once.

Upon the FST-2 servicing the interrupt, it will issue the command PRT PCOMP/ at PS time, which resets both the interrupt request circuit A7-5 (9LS74 Figure 2-1B) and the interrupt address circuit and D8-1 (9LS74 Figure 2-1B). This then reenables the interrupt circuitry for the next transmission done interrupt.

NOTE

If only one VKT interface board is going to be used, then the interboard priority is inhibited by installing jumper 'Y' at C4-2 (9LS32 Figure 2-1B). This places a high on 4C-3 always enabling B6-2 (9LS11 Figure 2-1B). Naturally, this single board will have an LSB of '0' for its address. (S1-5 is always off.)

2.1.11 Keyboard (Receiver) Interrupt

The UART (D3 Figure 2-1B), upon finishing its processing of the serial received data, requests an interrupt via B4-5 (9LS74 Figure 2-1B) as previously explained under the UART description.

B4-5 (9LS74) eanbles A7-12 (9LS74 Figure 2-1B) when it goes high. A7-11 (9LS74) will latch the receiver done interrupt request when clocked by the next IP clock. If RDR PON/ has set C7-10 (9LS74) then A6-9 will be priority enabled.

With A6-11 (9LS10) going high at IP time, and A6-9 enabled from C7-9 (9LS74), the IP cycle shall cause A6-8 (9LS10) to issue RDR GPINT/. This signal goes through the minus OR 5A-5 and via 5A-6 goes to Figure 2-1A of the schematic as GPINT/. GPINT/ operates as per the screen (printer) interrupt description on Figure 2-1A, with the exception that priority register (D1 (9LS367 Figure 2-1A)) will only isssue Bit 0 with RDR GPINT/. The issuing to the buss drivers F1 and F2 (9LS10) is also the same as the previous description.

A6-8 (9LS10 Figure 2-1B) also feeds A8-12, the priority F/F. If at CP3 time during IP time, no Sentry board with a higher priority is on line, then C8-11 will enable B7-4 with a high. At this time, CP3 will cause B7-6 (9LS08) to clock A8-11 (9LS74 Figure 2-1B). This says we have passed the Sentry priority polling, and now go on to the interboard priority.

At T4 time, if no higher priority is on C4-2, then B6-2 (9LS11) is enabled at CP3 time during T4 time. B6-12 will now clock the interrupt address enable F/F B8-3 (9LS74 Figure 2-1B). B8-5 going high, now enables C8-4 (9LS00). GINTAD/ operates the same as the screen interrupt description with the exception that with RDR GINTAD/ , the address issued from E2 will be 2 for the keyboard (RDR), or 52 with the LSB of the board address equal to '1' instead of '0'.

The following T1 time D7-10 shall cause D7-8 (9LS08 Figure 2-1B) to clock the address issued once F/F D8-11 (9LS74). D8-8 will now go low, inhibiting the address enable F/F B8-1 (9LS74), by holding it in reset. By this method, the keyboard (receiver) intrrupt address is only issued once.

During the FST-2 service of the keyboard (receiver (interrupt)) a RD signal will be latched at PS time. At T1 time, the keyboard interrupt request logic B4 (9LS74 Figure 2-1B) is reset by a SRD/ while the address lgoic A7-13 (9LS74), A8-10 (9LS74), and D8-13 (9LS74) will be reset via B7-11 (9LS08) when the RDR PCOMP/ signal is decoded.

The keyboard interrupt logic is now enabled again, as long as C7-9 (RDR PON) remains high, so consequent servicing of further received characters can be processed.

Again, if only one VKT interface board is used in a system, then jumper 'Y' will be installed which goes to C4-2. This constantly enables B6-2 (9LS11) so there is no interboard (VKT 1 to VKT 2) priority decision to be made.

When a single board is used, the LSB of the Board Address is '0', therefore, S1-5 remains in the 'OFF' position, as also explained in the screen interrupt description.

2.1.12 Screen (Printer) Interrupt Status

Beginning on Figure 2-1B, when C7-4 (9LS74) is set by the signal PRT PON/, then C7-5 goes high, and besides feeding the interrupt address logic, it also feeds back to Figure 2-1A.

The screen interrupt status register is E1-1 (9LS367 Figure 2-1A). E1-2 has the signal L. PRT PON (interrupt enabled) coming from C7-5 (Figure 2-1B). E1-4 has the signal PRT INP (printer interrupt in process) which comes from the screen interrupt address logic D8-5 (9LS74 Figure 2-1B). E1-10 has the signal CMD ERROR which comes from command error F/F C3-5 (Figure 2-1A).

When PROM E6 decodes read screen interrupt status (from E6-13) during a PS cycle, it is latched (data transfer command) by E5-7 (9LS175 Figure 2-1A). The following T1 cycle will cause B1-11 (9LS00) to pulse low enabling E1-1, and the buss drivers F1 and F2 (26S10). In this way, whatever data is available at E1 will now be placed on the 'N BUSS' for the FST-2 computer to read.

2.1.13 Keyboard (Reader) Interrupt Status

Beginning on Figure 2-1B, when C7-10 (9LS74) is set by the signal RDR PON/, then 7C-9 goes high, and besides feeding the interrupt address logic, it also feeds back to Figure 2-1A.

The keyboard (receiver) interrupt status register is D1-1 (9LS367 Figure 2-1A). D1-2 has the signal L. RDR PON (interrupt enabled) coming from C7-9 (Figure 2-1B.). D1-4 has the signal RDR INP (reader interrupt in process) which comes from the keyboard interrupt address logic D8-9 (9LS74 Figure 2-1B). D1-10 has the CMD ERROR signal from command error F/F C3-5 (9LS74 Figure 2-1A). D1-6 had the signal RD. ERR which comes from UART D3-13,14, and 15 via plus OR C4-6 (9LS32 Figure 2-1B).

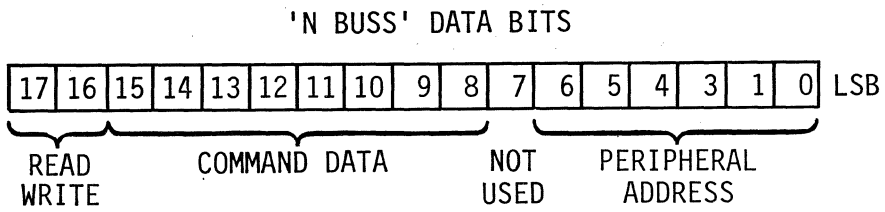
When PROM E6 decodes read keyboard interrupt status (from E6-11) during a PS cycle, it is latched (data transfer command) by E5-2 (9LS175 Figure 2-1A). The following T1 cycle will cause B1-8 (9LS00 Figure 2-1A) to pulse low enabling D1-1 (9LS367 Figure 2-1A) and C1-11 (9LS30 Figure 2-1A). This enables the keyboard (reader) interrupt status register D4 (9LS367) and the 'N BUSS' drivers F1-12 and F2-12 via C1-8 (9LS30). In this way, whatever data is available at D1 will not be placed on the 'N BUSS' for the FST-2 computer to read.

2.1.14 Detailed Command Decoding

FST-2 SPU Command Decode

A. SPUs are divided into I/O data commands and interface action only commands. All SPU commands occur at PS time, but only I/O data commands (data transfer required) are saved and activated the following T1 time.

B. The FST-2 Accumulator data is decoded per the following at PS (peripheral select) time:



C. As shown above, bits 0-6 are compared for a Peripheral Select Address. If an address compare comes true, the command data N BUSS bits 8-15 are decoded, a long with bits 16 and 17 which indicate SPU type. Data instructions are held until the following T1 for execution; however, non data SPUs are executed during the PS decode cycle.

D. A list of the SPU commands applicable to the RS232C VKT INTF are shown below with corresponding Mnemonic, Description, Op-Code, and the Accumulator Buss Data Bits.

RS232C VKT INTERFACE COMMANDS

OP-Code	Mnemonic	Description	FST-2 'N Buss' Data Bits																	
			17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
06000020	STST	(NOOP)Reader Status	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	X	X	X
06000030	STST	(NOOP)Printer Status	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	X	X	X
06073020	PON	Reader Interrupt Enable	0	0	0	0	0	1	0	1	1	0	0	0	0	1	0	X	X	X
06013030	PON	Printer Interrupt Enable	0	0	0	0	0	1	0	0	1	0	0	0	0	1	2	X	X	X
06022020	POFF	Reader Interrupt Disable	0	0	0	0	0	1	0	0	1	0	0	0	0	1	0	X	X	X
06022030	POFF	Printer Interrupt Disable	0	0	0	0	0	1	0	1	1	0	0	0	0	1	1	X	X	X
06002020	PCOMP	Reader Interrupt Complete	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	X	X	X
06002030	PCOMP	Printer Interrupt Complete	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	X	X	X
06602420	RD	Read Reconded Data	1	1	0	0	0	0	0	0	1	1	0	0	0	1	0	X	X	X
06421430	WRIT	Write Transferred Data	1	0	0	0	1	0	0	0	1	1	0	0	0	1	1	X	X	X
06611420	RDS	Read Status (Reader)	1	1	0	0	0	1	0	0	1	1	0	0	0	1	0	X	X	X
06611430	RDS	Read Status (Printer)	1	1	0	0	0	1	0	0	1	1	0	0	0	1	1	X	X	X
06403430	TTPR	Select & Print	1	0	0	0	0	0	0	1	1	1	0	0	0	1	1	X	X	X
06413430	TTPU	Select & Punch	1	0	0	0	0	1	0	1	1	1	0	0	0	1	1	X	X	X

NOTES

1. Those commands with either bit 16 or 17 true, are data transfer instructions, and all other are interface action only commands.

2. TTPR and TTPU are decoded as write data instructions, and are not applicable to a teletype console.

PROMs as Decoders.

Comparators F3 (9324) and F4 (9324) are used for the peripheral address decode, (N BUSS bits 0-7). The comparator F4 also decodes N BUSS bits 11, 14 and 15 which are always zero in all commands (Ref: SPU Command Chart also).

PROM D6 is used to decode all interface action only commands, and has N BUSS bits 3, 4, 8, 9, 10, 12, 13, 16 and 17 going to its address lines A0-A8 respectively. (See Chart 1 for SPUs and PROM data.)

PROM E6 is used to decode all transfer commands, and has N BUSS bits 3, 4, 8, 9, 10, 12, 13, 16 and 17 going to its address lines A0-A8 respectively. (See Chart 2 for SPUs and PROM data.)

PROM 'D6' CHART 1

SPU COMMAND	HEX PROM ADDRESS	HEX PROM DATA
STST RDR/	0 0 2	FE
STST PRT/	0 0 3	FD
PON RDR/	0 3 A	FB
PON PRT/	0 3 B	F7
POEF RDR/	0 2 A	EF
POEF PRT/	0 2 B	DF
PCOMP RDR/	0 0 A	BF
PCOMP PRT/	0 0 B	7F

NOTE

All other address locations for PROM 'd6' are left with 'FF' HEX DATA.

PROM 'E6' CHART 2

SPU COMMAND	HEX PROM ADDRESS	HEX PROM DATA
RD REC DATA	1 8 E	B1
WRITE	1 4 F	72
TTPR	1 1 F	72
TTPU	1 3 F	72
RDS RDR	1 A E	E4
RDS PRT	1 A F	D8

NOTE

All other address locations for PROM 'E6' are programmed for 'FØ' HEX DATA.

2.1.15 Detailed Register Definition

A. A list of the registers used on the VKT interface are as follows:

a. Transmitter Data Register (Write only ASCII Data)

b. Receiver Data Register (Read only ASCII Data)

c. Screen (Printer Status Register (Read only)

d. Keyboard (Reader) Status Register (Read only)

e. Screen (Printer) Int. Status Register (Read only)

f. Keyboard (Reader) Int. Status Register (Read only)

B. The Transmitter Data Register has the following bit definitions:

DATA BIT	SIGNAL
7	
6	ASCII
5	DATA
4	Right Justified
3	DBØ=LSB
2	
1	
0	

C. The Receiver Data Register has the following bit definitions:

DATA BIT	SIGNAL
7	
6	ASCII
5	DATA
4	Right Justified
3	DBØ=LSB
2	
1	
0	

D. The Screen (Printer) Status Register has the following bit definitions:

DATA BIT	SIGNAL	
20	DSR	(Terminal is ON LINE (RDY))
21	PRT BUSY	(Printer Busy (transmission in process))
22	CMD ERR	(Command Error)
23	PRT IDLE	(Screen (Printer) is Idle))

E. The Keyboard (Reader) Status Register has the following bit definitions:

DATA BIT	SIGNAL	
20	DSR	(Terminal is ON LINE (RDY))
21	RDR BUSY	(Reader Busy (receiption in process))
22	CMD ERR	(Command Error)
23	PRT IDLE	(Keyboard (Reader) is Idle))

F. The Screen (Printer) Int. Status Register has the following bit definitions:

DATA BIT	SIGNAL	
0	N/U	(Not used)
1	PRT INP	(Printer Interrupt in Process)
2	L PRT PON	(Printer Interrupt Enabled)
3	CMD ERR	(Command Error)

G. The Keyboard (Reader) Int. Status Register has the following bit definitions:

DATA BIT	SIGNAL	
0	RD ERR	(Receiver Data is in Error)
1	RDR INP	(Receiver Interrupt in Process)
2	L RDR PON	(Receiver Interrupt Enabled)
3	CMD ERR	(Command Error)

2.1.16 Reference For Additional Data

Below is a list of references, which can be used to derive additional data beyond the scope of this document.

A. EIA STANDARD RS232C (August 1969)

B. Western Digital Application Report #1 (UART TR1602)

REVISIONS				
ZONE	REV	DESCRIPTION	BY	DATE	APPROVAL
	1	ENG. PRTO			
	2	RELEASED PER EN 6589	M-Lu	3-25-77	4-2-77
	3	EN 6814	J.A.H.	7/26/77	8-2-77
	4	EN6825	J.A.H.	8/1/77	8-2-77

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D	25677	97420113-04	4

SCALE NONE SHEET 1 OF 2

97420113-04 [4]

FOLD 3 FOLD 2 FOLD 1

Figure 2-1A Schematic, Sentry - P.C. Board - RS232C VKT Interface

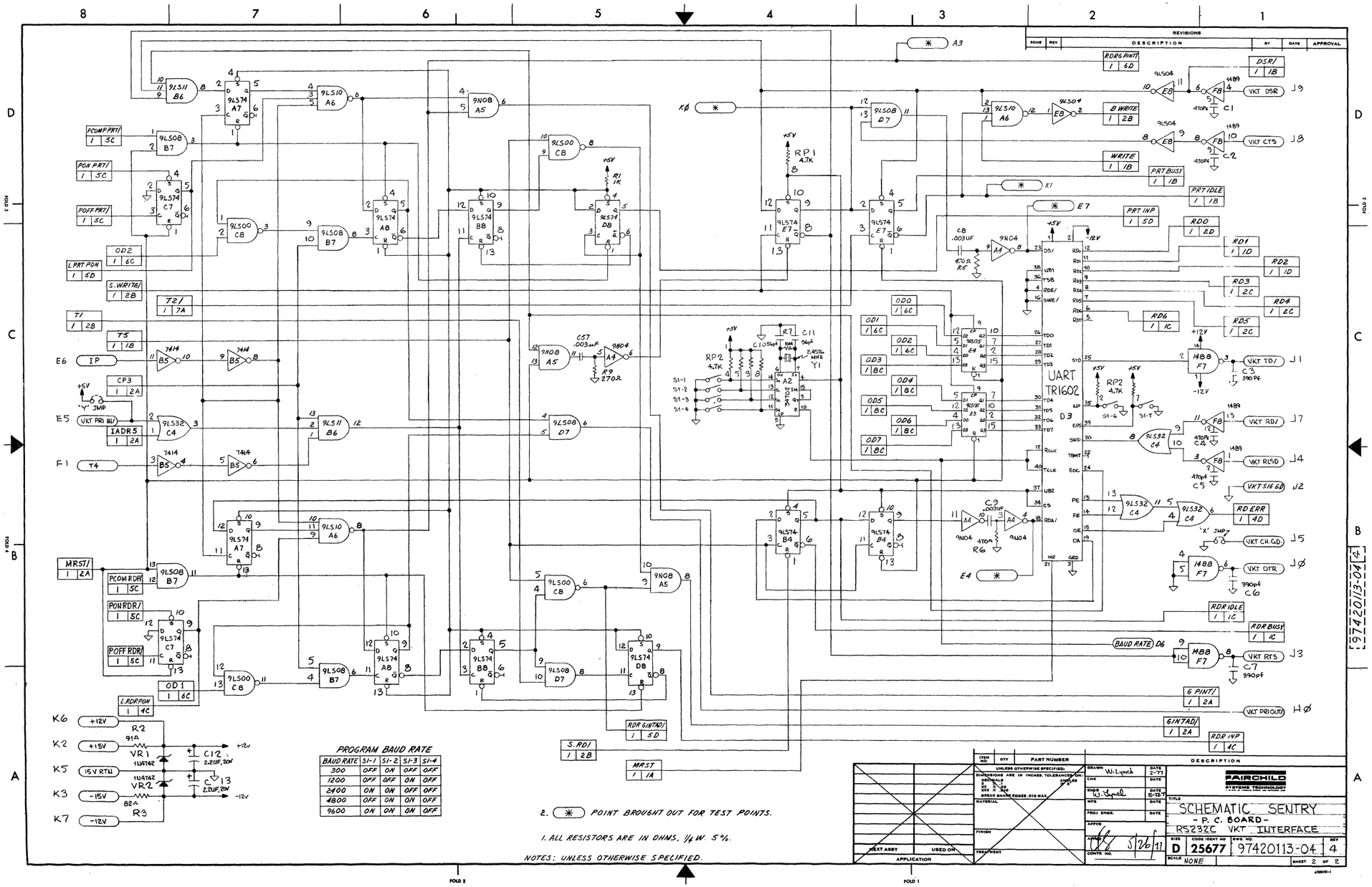

Figure 2-1B Schematic, Sentry
- P.C. Board -
RS232C VKT Interface

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