Four-Phase Systems, Inc.

GA-2160
CMOS Gate Array
User's Design Manual

Contents

Figures

Chapter 1
Introduction

The Four-Phase Systems GA-2160 Gate Array chip is a metal-gate CMOS transistor logic array providing 2,160 Complementary Metal Oxide Silicon transistor pairs, which may be interconnected to form a semi-custom LSI part. It provides 82 input and output pads plus power and ground. The configuration is suitable for use in conventional 68-and 84-pin square packages. The 2160 operates with + 5 volt power supplies for compatibility with TTL designs.

THE GATE ARRAY CONCEPT

In a gate array, a great many general-purpose circuit elements are produced on a wafer, before any specific circuit is needed, except that the two last (topmost) layers, which contain the gates and the metal that interconnects the elements to form the effective logic functions of the design, are left off. Then, when a new LSI design is needed, special gate and interconnect masks are generated for the new design.

Once a gate array such as the GA2160 has been developed, a family of circuits may be generated from it with ease. As many semicustom circuits may be derived as required, simply by generating the needed gate and metal interconnection masks, according to the specific logic functions of the design. This provides the advantage of quick and inexpensive chip design.

A second advantage is that the logic gate array may be pre-fabricated and kept on the shelf until needed, at which time the two custom masks are applied to it. Aside from reducing chip development time, this means that efficient high-volume runs of the processing steps before gate and metal may be made.

Also, in a concept that supports the gate array approach, the work of the designer is simplified greatly by the use of macro logic cells. A macro logic cell ("macro") is a standardized arrangement of CMOS transistors forming a conventional logic element: e.g., a gate, latch, or switch, or, in the case of more complex macros and their conventional combinations, a counter, multiplexor, or decoder. The 2160 is supported by a library of such macros, which are described in detail in this manual, and the circuit logic designer uses them as his tools; he need not be concerned with the details of the CMOS transistor placement or routing except as regards performance and the number of available transistors. The circuit layout — i.e., cell placement and routing — is performed by Four-Phase personnel using special routing techniques.

With macro logic cells and a gate array approach, the difficulty of designing with the 2160 is reduced significantly. This manual provides the information needed by the engineer specifying a semi-custom circuit that is to be implemented as a gate array.

CMOS LSI TECHNOLOGY

Metal-gate Complementary MOS technology has numerous features that make it attractive for semi-custom LSI technology. These include:

- Simplicity of logic design. Each CMOS logic circuit can be constructed from a small number of active element pairs. This allows a large number of circuits to be placed on a chip.

- Good packing density. 2,160 transistor pairs are supported on a chip, also contributing to the number of circuits that can be placed on the chip.

- Well-defined logic levels. The two logic levels in CMOS are the positive and negative supply voltages.

- Ease of breadboarding. A good selection of standard parts is available, including MSI functions.

- A stable and reliable process. The Four-Phase Metal-Gate CMOS process has been in use for several years as a watch-chip process.

- Ease of interface to TTL and NMOS. A +5 volt power supply is specified for compatibility.

- Low power consumption. CMOS draws very little quiescent power.

- Good noise immunity. Typical noise immunities in CMOS approach 50% of power supply voltage.

CMOS WAFER PROCESSING

The Four-Phase 2160 Gate Array is produced by a standard IC manufacturing process, Metal Gate CMOS. This process is the same as the one used to produce standard CMOS logic devices of the 4000 and 74C series.

The starting point for the Metal Gate CMOS process is a wafer of lightly doped N-type silicon. The first step in manufacturing is to grow a protective layer of oxide over the entire surface of the wafer, by exposing it to steam at high temperature for several hours. This gives a uniform initial oxide (silicon dioxide) layer, completely covering the silicon. All further processing takes place through openings etched in the initial oxide layer.

The etched patterns for later steps are produced by photolithographic techniques. The desired pattern is produced as an image on a high-resolution photographic plate, or photomask. A photosensitive layer, called photoresist, is deposited on the surface of the silicon layer, and the photomask is used to expose the photoresist to ultraviolet light. The unexposed areas of photoresist are removed chemically, leaving the circuit pattern as openings in the photoresist. The wafer is then dipped into dilute hydrofloric acid, which etches away the exposed oxide layer, but leaves the photoresist and the silicon unetched.

The photoresist is then chemically removed, leaving the initial oxide film with the desired pattern of openings to the N-type silicon. These openings are the places where NMOS devices will be generated on the wafer. The wafer is exposed to a source of boron atoms, which penetrate the exposed silicon but not the oxide layer. The wafer is then heat treated in a furnace, allowing the boron atoms to diffuse into the silicon and form P-wells. Next a new protective oxide layer is grown over the surface to prepare the wafer for the next photographic step.

The next photomask defines the P+ regions, which forms PMOS transistors and underpass resistors, and also forms a guard band or P-well contact around the areas where the NMOS transistors will be built. The P+ pattern is photographically etched into the wafer, and another boron diffusion step is performed. Then a third oxide layer is grown over the wafer, preparing for the adding of the NMOS transistors.

The third, N+, photomask defines the NMOS transistors and places a boundary or "channel stop" around the PMOS transistors. The N+ diffusion uses phosphorous rather than boron. Again, an oxide film is grown over the silicon in preparation for the next mask step, the thin oxide gate step.

The fourth photomask, the gate mask, defines the active gate areas for both the NMOS and PMOS transistors and the selected contact areas. After these areas are etched in the oxide layer, a thin layer of oxide is grown. This thin layer will be the dielectric in the MOS gates. At this point, all the transistors and underpasses have been produced.

Up to this point, the processing of the 2160 is the same as for any conventional CMOS part. But now, the wafer may be placed in inventory, awaiting a custom masks that are programmed to define the gates and interconnects that produce a particular semi-custom circuit.

All that remains is to make contact to the various areas and interconnect them. For this purpose, a fifth mask, the selected contact mask, is used to remove the thin oxide from the contact windows. Next, a thin layer of aluminum is deposited over the entire top surface of the wafer.

This sixth photomask, the metal mask, defines a pattern in the protective layer of photoresist over the areas where metal is required, and all the unprotected metal is etched away. The wafer is now essentially completed; only a protective layer of glass remains to be deposited. This is etched using the pad mask, leaving only the contact pads unprotected by the glass. The wafer is now ready for testing.

1 May 1981

Chapter 2
2160 Gate Array Description

CMOS DEVICES

Complementary MOS logic makes use of Field Effect Transistors (FETs), also referred to as MOS transistors or MOSFETs. The FET employs an electric field (charge) on its "gate" electrode to control the flow of current between its "source" and "drain" electrodes. The 2160 and similar technologies employ only enhancement mode transistors, such that the transistor is turned on when positive charge is applied to its gate, off when negative charge is applied.

Another distinction within the subject of FETs is NMOS vs. PMOS transistors. An NMOS transistor conducts using negative charges (electrons); a PMOS transistor uses positive charges ("holes"). Complementary MOS (CMOS) refers to the fact that in this technology, the two types of transistors are used in pairs: each logic function employs an NMOS/PMOS pair, taking advantage of the fact that the PMOS transistor conducts at one logic level (zero volts, or ground, as referenced to the +5 volt supply voltage), and the NMOS transistor conducts at the other (+5 volt) level. And the thresholds of the two types of devices are controlled such that each device is hard off at the on voltage of the other. NMOS and PMOS transistors are constructed side by side on the silicon wafer, and they are interconnected via aluminum traces (metal or interconnect layer) at logic implementation time to form the semi-custom CMOS circuitry. The way the pairs are arranged to create the logic elements is explained in Chapter 3, "CMOS Logic Design".

Figure 2-1 shows a cross-section of a PMOS transistor, and its circuit symbol. The substrate is N-type as the wafer is manufactured, and the source and drain are P + diffusions. A negative voltage (with respect to source; ground in this case) applied to the gate will tend to attract free positive charges — ie, holes — to form a conducting channel between source and drain. Similarly, a positive voltage (e.g., +5 volts) applied to the gate will tend to repel free positive charges and prevent conduction between source and drain.
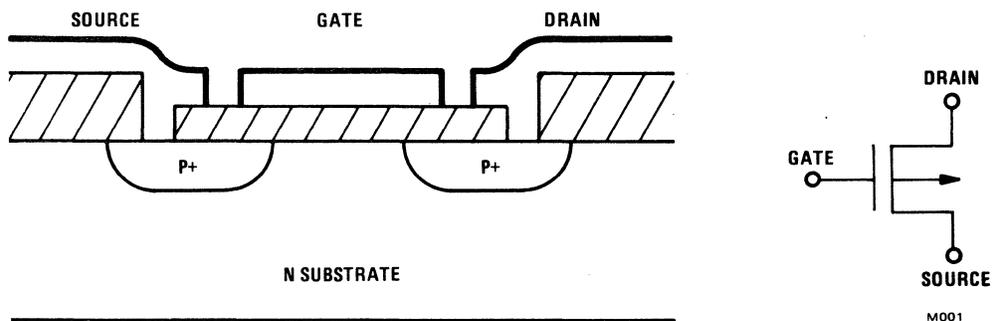
Figure 2-1. Cross-Section of PMOS Transistor

Since the NMOS transistor is constructed on the same silicon chip as the PMOS transistor, an isolation tub must be defined, consisting of a deep diffusion of p + type. This is referred to as the p-well and serves as the substrate for the NMOS devices. Figure 2-2 shows a cross-section of an NMOS transistor, with its P type diffusion substrate, and its source and drain as N + diffusions. The operation of te NMOS device is similar to the PMOS device except for the opposite polarity of voltages. A positive voltage (e.g., +5 volts) applied to the gate will tend to attract free negative charges — ie, electrons — to the channel area, and form a conducting path between the source and drain. Similarly, a negative voltage (e.g., ground) applied to the gate will tend to repel free electrons and prevent conduction between source and drain.
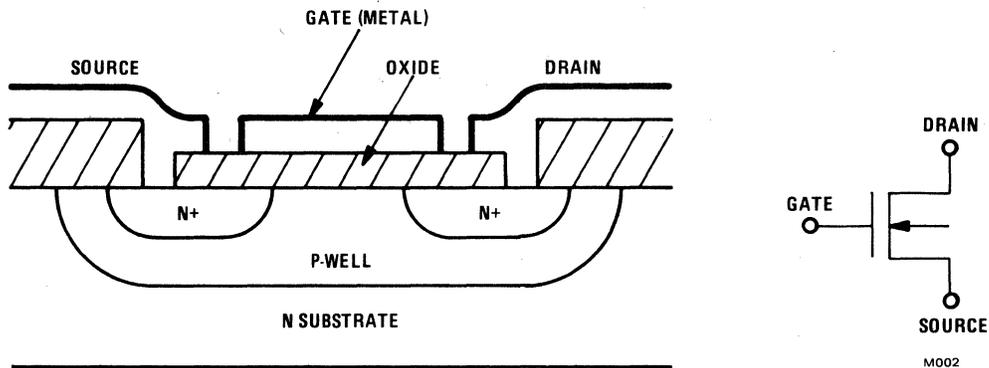
**Figure 2-2. Cross-Section of NMOS Transistor**

The gate of a FET is electrically isolated from the rest of the transistor by a silicon dioxide layer, and practically no DC gate current flows, regardless of the conducting state of the source-drain path of the transistor. Because of this isolation, the gate plate and the semiconductor, separated by the oxide which will act as a dielectric, together act as a capacitor. The value of the capacitor will vary by the depletion layer of the silicon substrate, depending on the gate plate potential. Figure 2-3 shows an MOS capacitor, in theory; in practical terms within the gate array, capacitors are furnished by the transistors themselves.
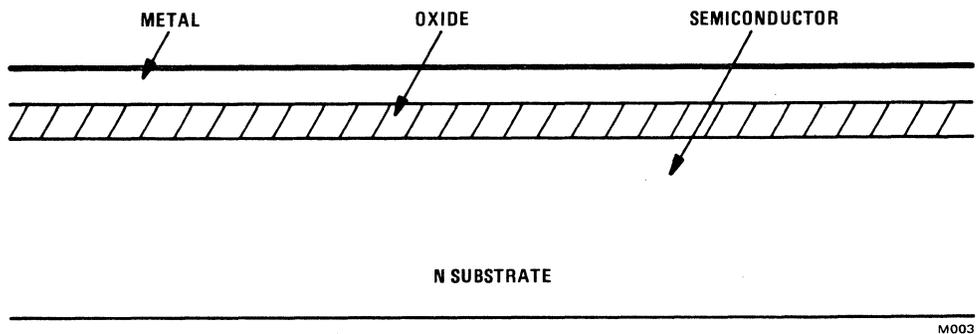
Figure 2-3. MOS Capacitor

Figure 2-4 shows an MOS diffusion cross-under. It is used to implement signal crossings and also functions as a resistive element in the circuit. A cross-under typically presents a resistance of approximately 650 ohms and a junction capacitance of 0.2 pf. .
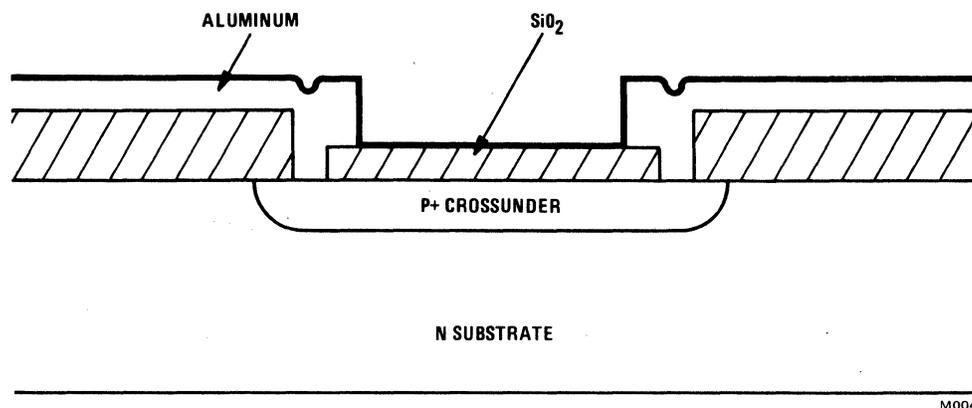
Figure 2-4. MOS Crossunder (Resistive Element)

Chapter 3
CMOS Logic Design

THE MACRO CONCEPT

The Engineer designing with the 2160 Gate Array chip has at his disposal a library of macro logic elements, embodying commonly used logic elements: gates, inverters, switches, latches, counters, multiplexors, decoders, and the like. Macro elements for input and output buffers are also provided. The designer using the 2160 plans his circuit in terms of the macro elements, using conventional logic symbols. In the short run, placement of and routing between such elements will be performed by Four-Phase personnel; CAD software for these functions is in preparation.

This chapter presents the Four-Phase macro logic cell library, which is constantly under study for updating and enhancement. Whenever a new macro is added to the library, the fact will be published. Most of the macros, however, are simple and rather obvious logic elements, similar to SSI functions. Candidate macros for inclusion will probe into the low end of the area of MSI functions. Interesting ways to combine macros into more complex functions are suggested in Chapter 4, "Macro Cell Design Suggestions".

Illustrations accompanying the description of each macro show its characteristics and specifications; these are also tabularized in "Summary of Macro Characteristics" at the end of the chapter. Also each macro is assigned a number, which appears in all the documentation and must appear with the macro every time it is used in a logic diagram. This number ties the macros to their metal mask patterns for layout people, CAD, etc.

In principle, all the CMOS logic circuits are based on two simple elements, the simple inverter and the transmission gate or switch. Elements of the inverter are serialized or paralleled to form more complex elements; switches are paralleled or serialized as well. In this context, the switch is described first, followed by the inverter and circuits based on it.

SWITCH (TRANSMISSION GATE)

A CMOS transmission gate acts as a single pole, single throw switch, conducting or open depending on the states of its control inputs. The theoretical switch has zero forward and reverse resistance when closed and infinite resistance when open. A CMOS switch made of one NMOS and one PMOS transistor in parallel (one transistor pair) approaches these characteristics; see Figure 3-1. When the gate of the NMOS transistor is high (+5 volts), and the gate of the PMOS transistor is low (ground), both transistors are on, and the switch presents a low impedance between input and output. Similarly, if the control voltages are reversed (N gate low, P gate high), both transistors are turned off, and the switch is open; the path from input to output is disabled. The combination of switches with simple gates and inverters form the more complex CMOS circuits.

To prevent inadvertent short circuits, it is the responsibility of the designer to ensure that one gate of a switch receives high voltage, the other low. For this purpose, clock pulses with minimum skew between the signal and its inverse are required. On-board clock generators are provided to achieve this; see "Clock Generators" in this chapter.

Performance and Transistor Count

Note that the switch only allows or disallows the flow of current; it provides no drive. Use of switches thus affects loading on previous stages. Each switch represents approximately 25 nanoseconds delay in the data path, based on simulation information. One transistor pair.

SIMPLE INVERTER

Most CMOS logic circuits are based upon the simple inverter. See Figure 3-2 for the logic symbol, circuit schematic, and other other characteristics of a typical inverter. The basic inverter macro uses one transistor pair. The gates of both transistors are connected to the input, the drains to the output, and the sources are connected to the respective power supplies: VDD (+5 volts) for the PMOS device; VSS (ground) for the NMOS device.
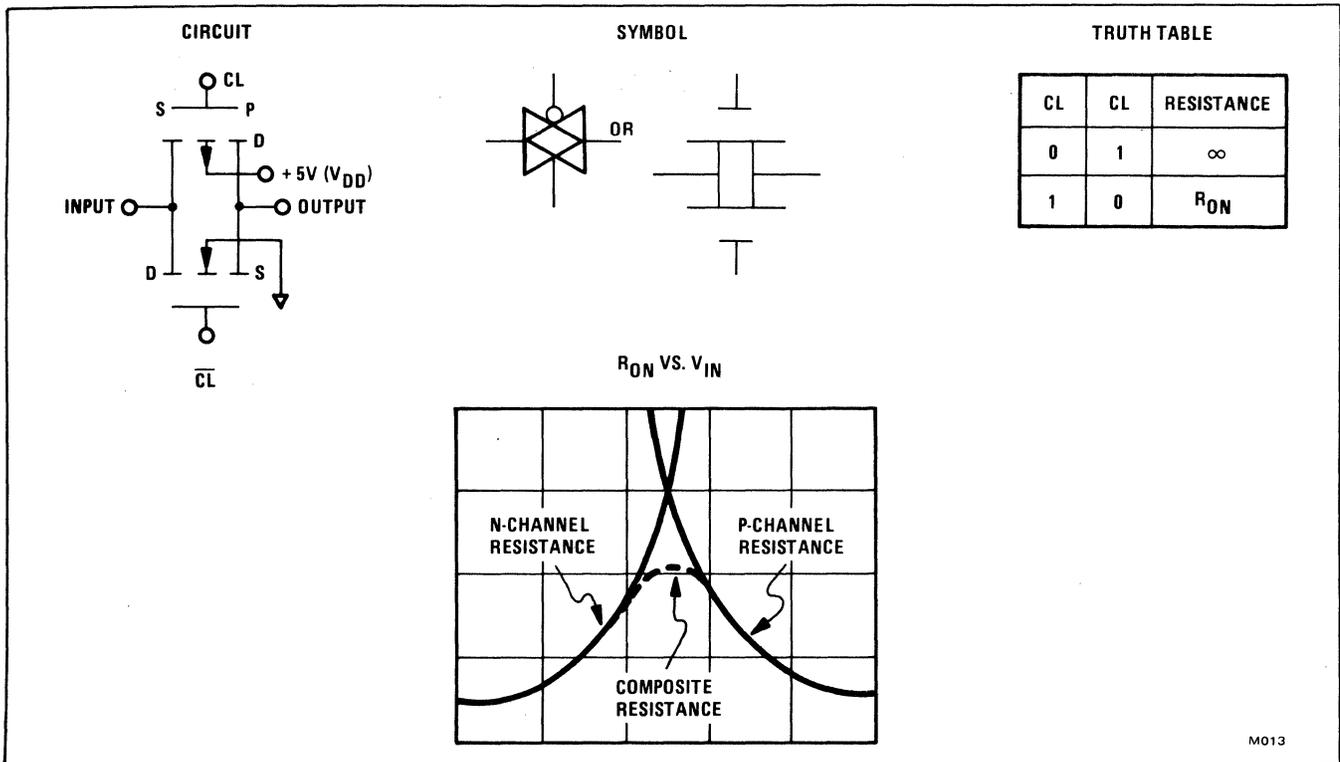
Figure 3-1.   Switch or Transmission Gate
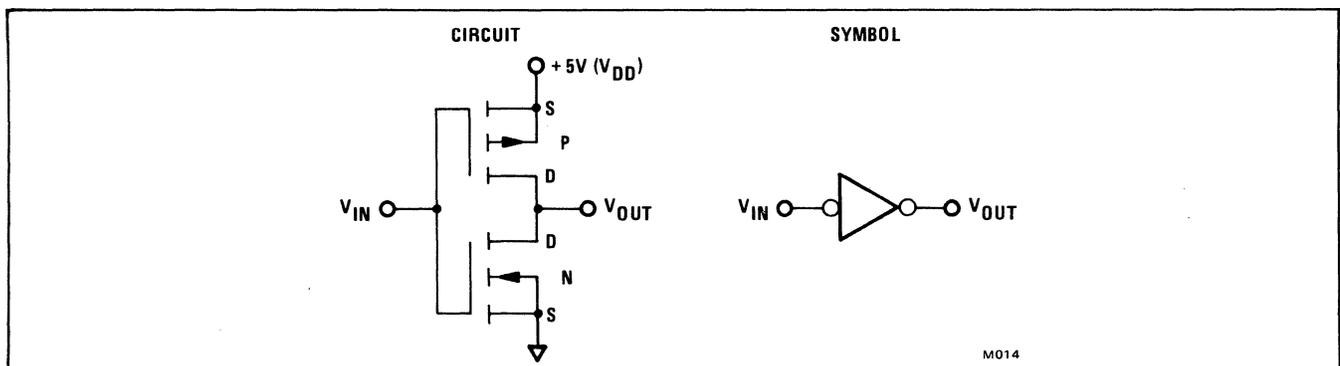
Figure 3-2.   Basic Inverter Circuit Macro

When the input voltage is low ("zero" or ground), the gate of the PMOS device is biased negative with respect to its source (+5), and the PMOS device is turned on; similarly, the gate of the NMOS device is equal to its reference (ground), and the NMOS device is off. Thus, there is a low impedance between the output and the supply voltage, and a high impedance between the output and ground, and the output is high. Again, when the input voltage is high ("one" or +5 volts), the gate of the PMOS device is biased equal to its refererence or source electrode, and this device is turned off. But the gate of the NMOS device is biased positive compared to its reference (source = ground), and the NMOS transistor conducts. Thus, a high impedance exists between output and source voltage, a low impedance between output and ground, and the output is zero. Note the important implication here that when one transistor of the complementary pair is conducting, the other is hard off. This means that there is no low impedance path from power to ground for either stable state, and standby power is only the product of supply voltage and leakage current (which is supposed to be negligible in an MOS transistor).

This discussion illustrates the general principle of CMOS inverter-based logic: in every instance where a high output is required, a conducting path must be created — via PMOS transistors whose gates are negatively biased (on) — from the power supply to the output. And, at the same time, all paths to ground, via NMOS transistors, must be interrupted by biasing to ground the gates of the appropriate NMOS transistors (at least one per serial path). And in every instance where a low output is required, at least one conducting path from output to ground must be established via an NMOS device or devices, and every serial path from power to output via PMOS devices must be interrupted.

It follows also that in CMOS logic, active power is dissipated only during the transitions between logic states. During the crossover from one state to another, there is a brief period when both transistors are on or partly on, thus creating a low impedance path from supply to ground. The amplitude and duration of the resultant current spike depend on the size of the transistors, the supply voltage, and the input signal transition time. In 2160 technology, the current spike is well within the current handling capabilities of the transistors. The average value of this current is proportional to the repetition rate of the signal transistions. Current is also drawn from the supply rails to charge and discharge the load capacitances whenever the output voltage of a stage changes state. This power component is proportional to the frequency of signal changes, the load capacitances, the slew rate of the input signal, and the square of the voltage swing. The current relationships are shown in Figure 3-3.

Performance and Transistor Count

A simple inverter requires an average off 14 nanoseconds to switch into a 1/3 pf load; 18 nanoseconds to switch into a 1 pf load. The gates of the inverter offers a load capacitance of 1/3 pf to the previous stage. One transistor pair.
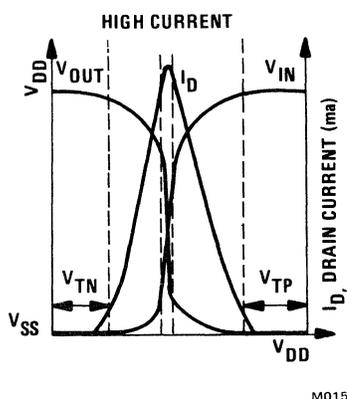
Figure 3-3. CMOS Inverter Electrical Characteristics

2-INPUT NOR GATE

A logic "OR" gate has a high output voltage whenever one or more of its inputs is high; a "NOR" gate is a Negative OR, such that the output voltage is low whenever one or more input is high. The summary of a 2-input NOR macro is shown in Figure 3-4, which should be compared to Figure 3-2 (inverter) and 3-6 (NAND gate).

Two N-Channel/P-Channel transistor pairs are employed in this macro. The two PMOS transistors are in series, and the NMOS devices are in parallel. Each input controls one PMOS and one NMOS transistor; i.e., one complementary pair. If either input is high, then the corresponding PMOS device is off, creating an open circuit to the supply voltage. At the same time, a high input will turn on the corresponding NMOS device, grounding the output. But if both inputs are low, both PMOS devices will conduct and both NMOS devices will be open, connecting + 5 volts to the output.

Performance and Transistor Count

From Simulations, the 2-input NOR gate switches in an average of 29 nanoseconds into 1/3 pf, 38 nanoseconds into 1 pf. Two transisor pairs used.

CIRCUIT

A

B

P

P

+5V (V_DD)

N

N

V_OUT

SYMBOL

A
B

V_OUT

TRUTH TABLE

A	B	V_{OUT}
0	0	1
0	1	0
1	0	0
1	1	0

M016
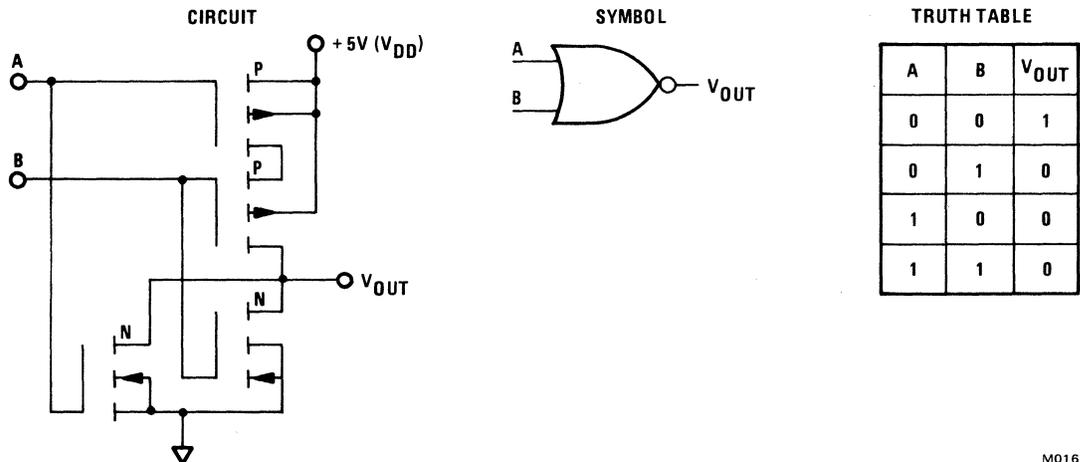
Figure 3-4. 2-Input NOR Gate

3-INPUT NOR GATE

This macro is similar to the 2-input gate on the preceding page. See Figure 3-5 for the pertinent data. Three complementary transistor pairs are used, with the three PMOS devices in series and the three NMOS devices in parallel, and one input is wired to the gate of each transistor in each NMOS/PMOS pair. A logic one (+ 5 volts) on any one or more inputs, then, will create high impedance in the PMOS stack and disconnect the output from the supply voltage. And the corresponding logic one applied to any of the NMOS transistors will short the output to ground. Only when all three inputs are zeros (ground) will the three transistors in the PMOS stack conduct, connecting supply to output, and all three NMOS transistors will turn off, isolating the output from ground.

Performance and Transistor Count

The 3-input NOR gate will switch in an average of 50 nanoseconds into 1/3 pf or 65 ns into 1 pf, from simulation information. Three transistor pairs used.

CIRCUIT

SYMBOL

A
B
C

V_OUT

TRUTH TABLE

A	B	C	V_{OUT}
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

M017
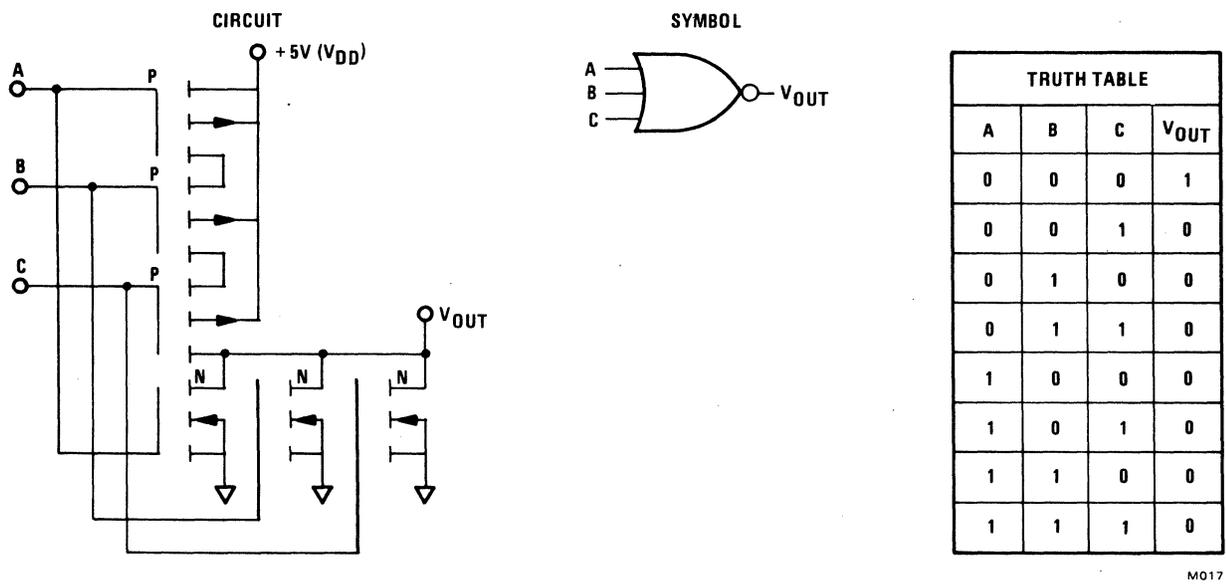
Figure 3-5. 3-Input NOR Gate

2-INPUT NAND GATE

A logic "AND" gate has a high output voltage whenever all of its inputs are high; a "NAND" gate is a Negative AND, such that the output voltage is low whenever all the inputs are high. The summary of a 2-input NAND macro is shown in Figure 3-6, which may be compared to Figures 3-2 (basic inverter) and 3-4 (NOR gate).

Two NMOS/PMOS transistor pairs are employed in the 2-input NAND gate. The PMOS transistors are wired in parallel, with the NMOS transistors in series with both of them. Each input is wired to the gate of one each of the PMOS and NMOS transistors, and the output is taken from the point between the drain electrodes of the PMOS transistors and the top of the NMOS stack. When an input is low, the corresponding PMOS transistor is biased negatively, it conducts, and a low impedance path is established between power supply and output. That same low input, applied to the gate of the corresponding NMOS device, biases it to ground, and the NMOS device is turned off. Thus, the path from output to ground is interrupted, and the output is high. When both inputs are high, however, both PMOS transistors are turned off, and there is no path from power to output; but both NMOS transistors are turned on, and the output is grounded.

Performance and Transistor Count

The 2-input NAND gate will switch in 20.5 nanoseconds average into 1/3 pf and 35 ns average into 1 pf, based on simulations. Two transistor pairs.

CIRCUIT

SYMBOL

TRUTH TABLE

A	B	V_{OUT}
0	0	1
0	1	1
1	0	1
1	1	0

M018
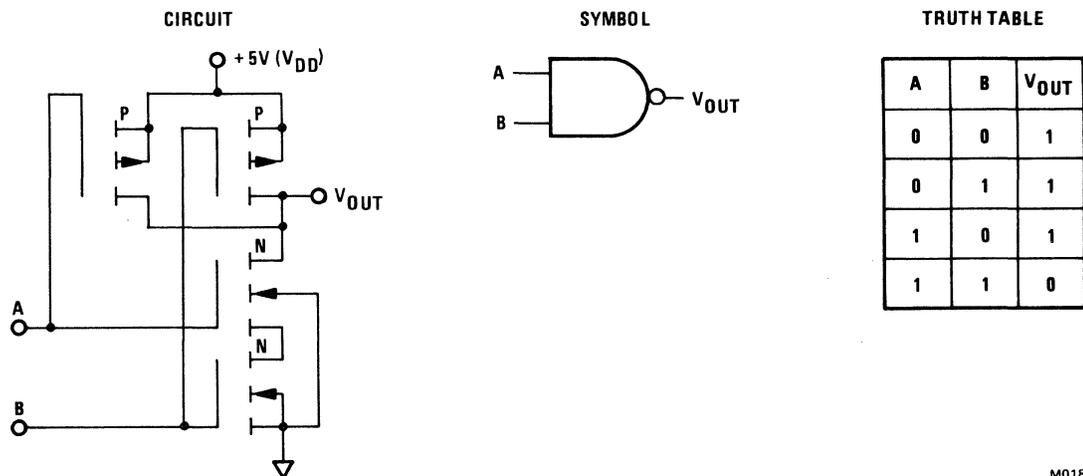
Figure 3-6.   2-Input NAND Gate

3-INPUT NAND GATE

This macro is derived from the 2-input gate on the previous page; see Figure 3-7. Three complementary transistor pairs are used, with the three PMOS devices wired in parallel with one another, and the three NMOS devices in a series stack, serial with the PMOS devices. The output is taken from the point between the NMOS stack and the common drain connection of the PMOS devices. Each input is wired to the gate of one each PMOS and NMOS devices, such that, if any one input is zero, a conduction path will be created between power and output, and the ground path to the output will be broken. Only if all three inputs are ones will all three paths from power supply to output be broken, and path from output to ground completed, driving the output low.

Performance and Transistor Count

The 3-input NAND gate will switch in 38 nanoseconds average into 1/3 pf and 53 ns into 1 pf, from simulations. Three transistor pairs.

A	B	C	V_{OUT}
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

M019
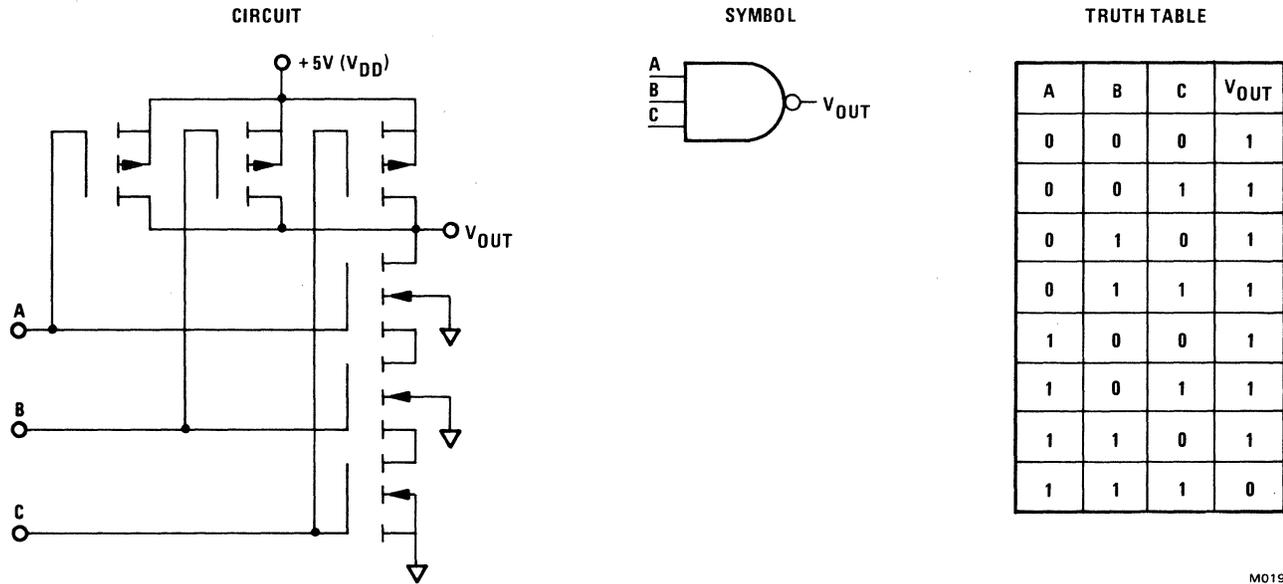
Figure 3-7. 3-Input NAND Gate

COMPLEX GATES

Each of the gate macros discussed so far implements only one logic function and one inversion. For performance, ease of design, and transistor resource saving, however, it is often convenient to implement two levels of logic with a single macro. Such circuits are referred to as complex gates, and offer one principal area where expansion of the macro library may be considered.

AND/NOR and OR/NAND Gates

Figure 3-8 shows an AND/NOR and Figure 3-9 an OR/NAND macro. In each instance, a function that might have been implemented in five transistor pairs has been reduced to three pairs, with a corresponding improvement in performance. The reader is invited to study the implementation of the logic: in the AND/NOR macro, C false drives V_{out} true unless overridden by both A and B true, which force V_{out} false, but C true always drives V_{out} false. In the conceptually symmetrical OR/NAND macro, C false always drives drive V_{out} true, but C true drives V_{out}false unless overridden by A and B both false, which forces V_{out} true.

Performance and Transistor Count

Performance to be supplied. Three transistor pairs.

Figure 3-8.   AND/NOR Gate

A	B	C	V_{OUT}
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Figure 3-9.   OR/NAND Gate

A	B	C	V_{OUT}
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0
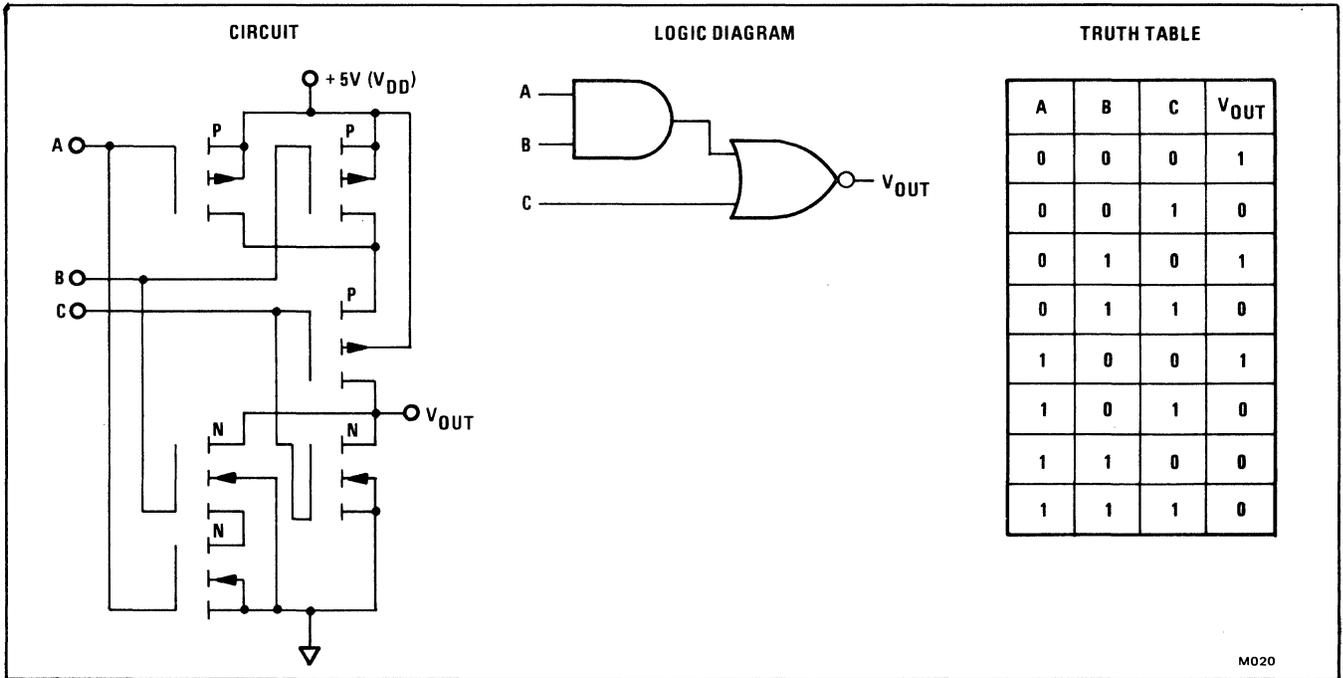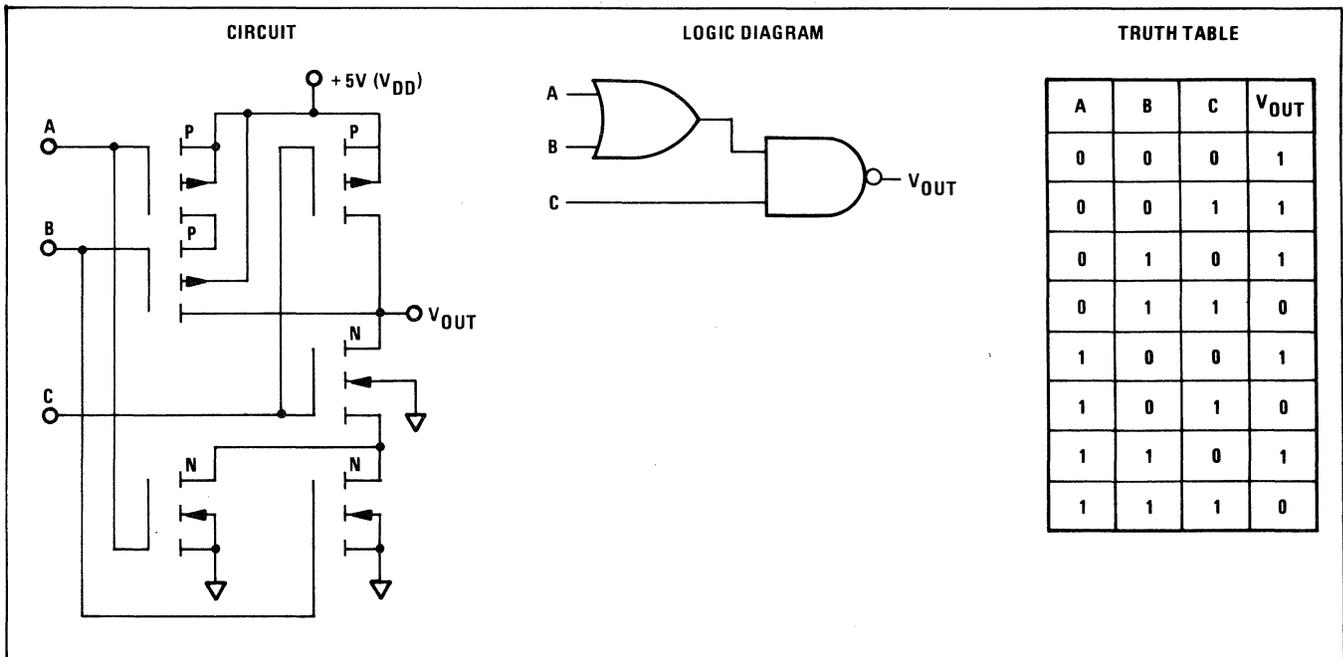
## Exclusive OR and Exclusive NOR Gates

Macros for the Exclusive OR (difference) Gate are illustrated in Figures 3-10 and 3-11; see Figures 3-12 and 3-13 for the Exclusive NOR (match) Gate. These conceptually simple logic functions are relatively expensive in many forms of logic; in CMOS they are performed with five transistor pairs. In the supported macros, drive is always provided in the AND/NOR and OR/NAND versions. In the switching versions, inverters are included on the outputs to provide drive into the next stage; if such gates with one fewer transistor pair are needed and drive capability is not required, macros without the output inverters may be placed in the library. Note that the inputs to these switching macros are slightly assymetrical, in that one input drives two transmission gates and an inverter, but the other drives a transmission gate and an inverter. It is believed that the effect of this assymetry on performance will be negligible, but if a symmetrical design is needed, it may be performed in NAND/NOR logic, at some cost in performance, although the transistor-pair count is the same, five.

Performance and Transistor Count

Performance to be supplied. Five transistor pairs.

LOGIC CIRCUIT

SYMBOL

TRANSISTOR CIRCUIT

TRUTH TABLE

A	B	V_{OUT}
0	0	0
0	1	1
1	0	1
1	1	0

M022
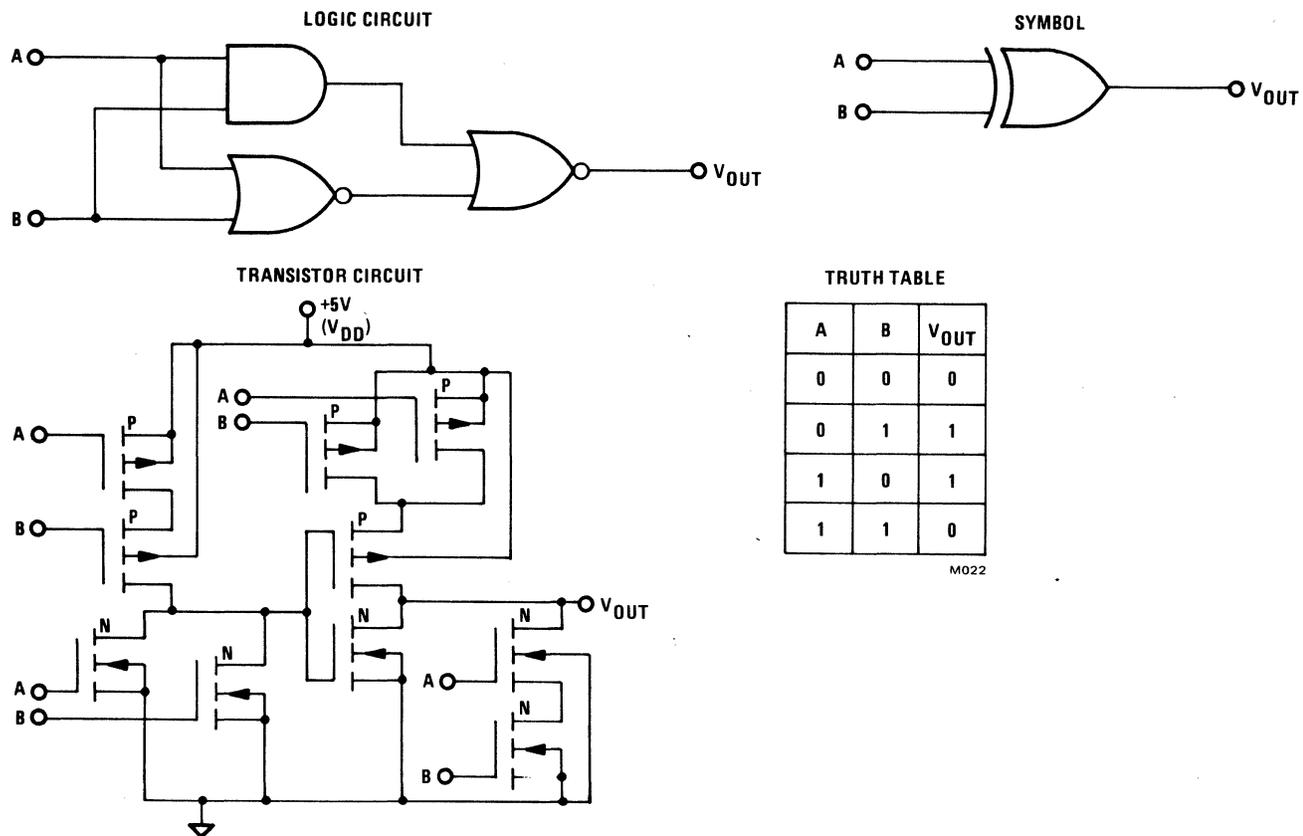
Figure 3-10.   Exclusive OR Gate (AND/NOR Version)

CIRCUIT DIAGRAM

TRUTH TABLE

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

M036
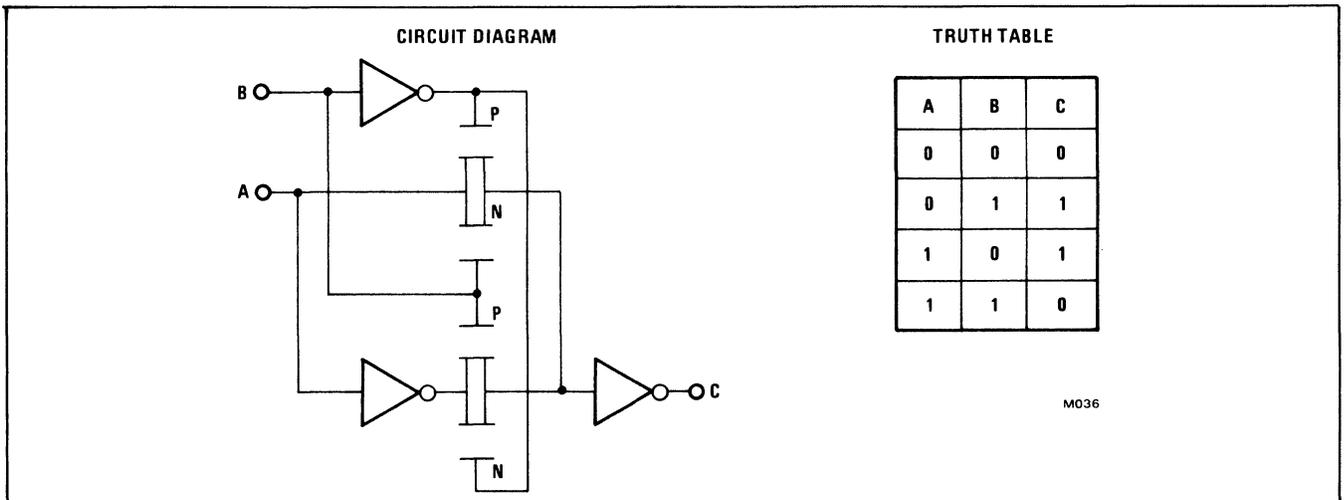
Figure 3-11.   Exclusive OR Gate (Switch Version)

TRANSISTOR CIRCUIT   LOGIC CIRCUIT   TRUTH TABLE

A	B	V_{OUT}
0	0	1
0	1	0
1	0	0
1	1	1

M023
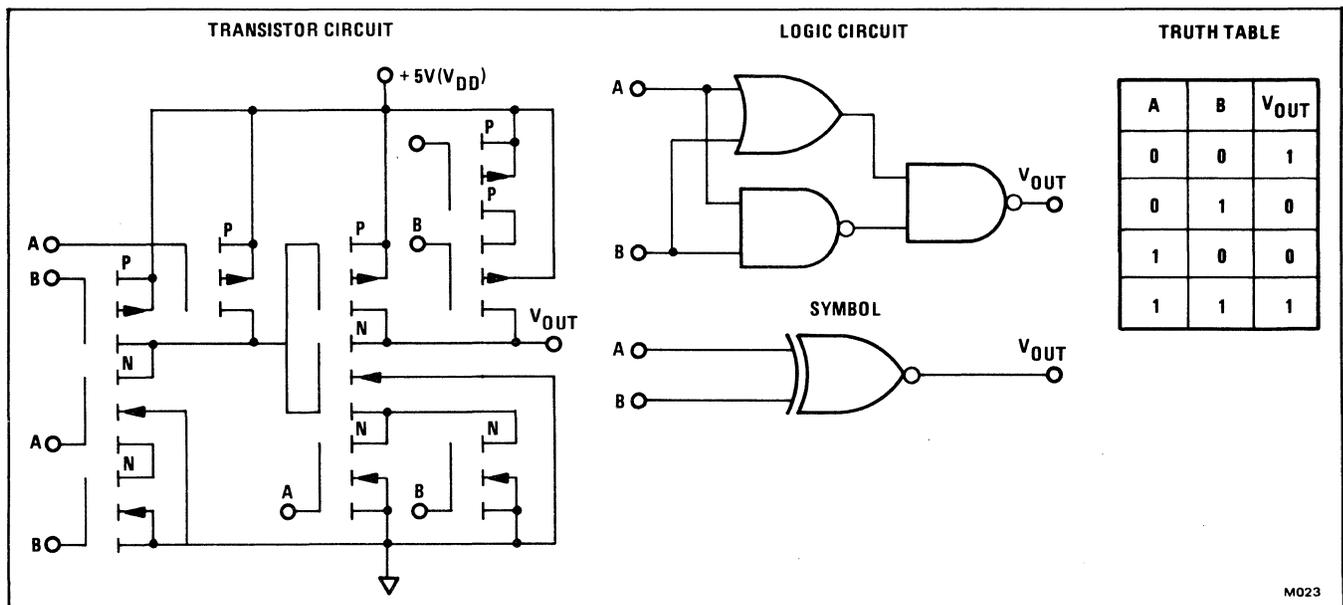
Figure 3-12.   Exclusive NOR Gate (OR/NAND Version)

CIRCUIT DIAGRAM

TRUTH TABLE

A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

M037
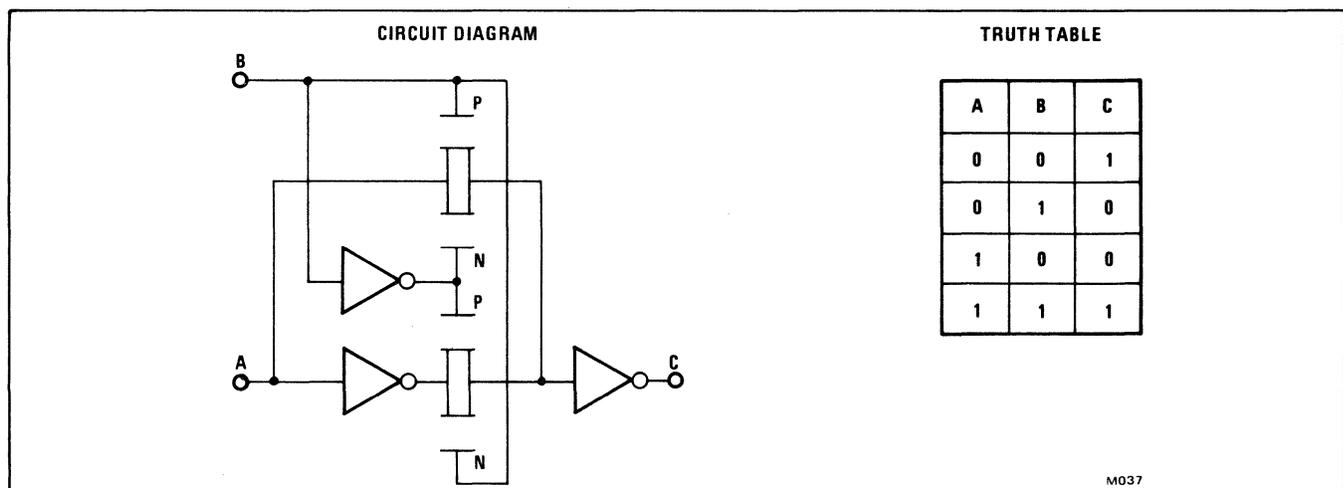
Figure 3-13.   Exclusive NOR Gate (Switch Version)

Exclusive NOR-NOR Gate

Figure 3-14 shows the Exclusive NOR-NOR gate macro, which is required for the Decade Counter (see "Macro Cell Design Suggestions" in Chapter 4). This macro is shown in detail also, in the hope that it may occasionally find use on its own merits.

Performance and Transistor Count

Performance to be supplied. Six transistor pairs are needed.

SYMBOL

TRUTH TABLE

A	B	C	V_{OUT}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

M024
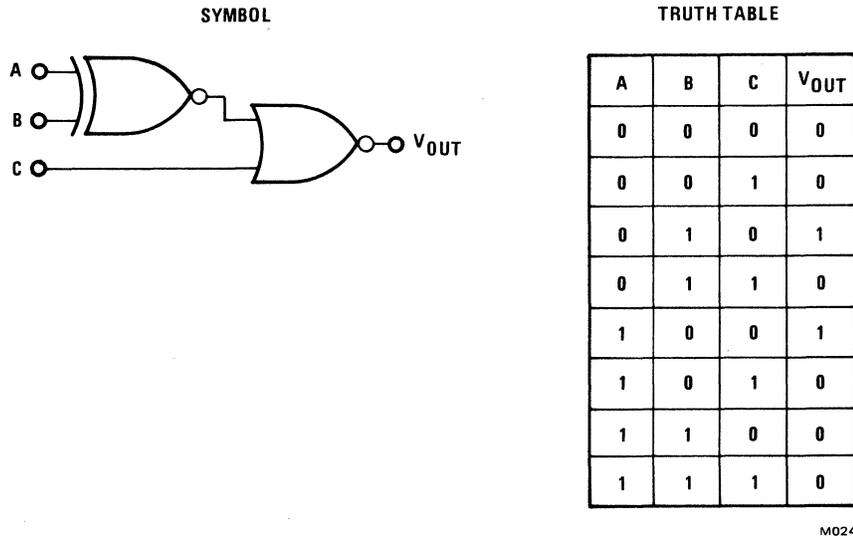
Figure 3-14.   Exclusive NOR-NOR Gate

Miscellaneous Complex Gates

Special macros are supported for certain widely-used circuit elements. Figure 3-15 shows two combinations of gates included for use in building a decade counter. Other complex macros will be included in the library.

Performance and Transistor Count

Performance to be supplied. 4-gate AND/NOR circuit uses seven transistor pairs; NAND/NAND circuit uses 10 transistor pairs.

M025
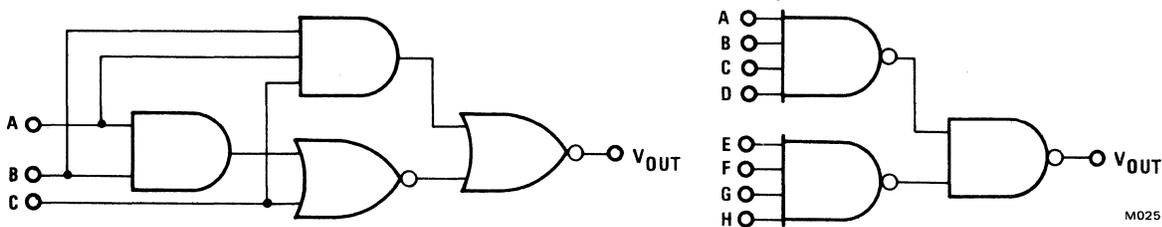
Figure 3-15.   Miscellaneous Macro Cells

LATCHES AND FLIP FLOPS

One-bit memory elements are formed in many ways in CMOS. All, however, make use of one of two principles for data storage: either cross-coupled inverters — as in a simple Set/Reset Latch — or switched feedback — as in many more complex latches.

R-S Latch

Figure 3-16 shows an R-S latch formed by cross-connecting two 2-Input NOR gates. The operation of this macro is as follows: starting with both the S and R inputs and the Q output low, the S input being low will force the $\overline{Q}$ output high. But the $\overline{Q}$ signal is applied to the A gate, and the $\overline{Q}$ and R inputs both being low tend to hold the Q output low. Thus, both inputs to the B gate are low, Q is kept high, and the situation is stable; the latch will remain in this state as long as power is applied and the set input remains low.

If set goes high, $\overline{Q}$ is forced low, the $\overline{Q}$ input to the A gate will go low, and Q will be forced high. Q applied to the B gate then will hold $\overline{Q}$ low, regardless of the state of the S input, until the R input changes. If S is low and R changes to high, the latch will toggle again. If both inputs are high at the same time — normally an illegal condition — both outputs will go low until one of the inputs goes low again.

Performance and Transistor Count

Performance to be supplied. Two transistor pairs.

SYMBOL

TRUTH TABLE

R	S	Q	$\overline{Q}$
0	1	1	0
1	0	0	1
1	1	0	0
0	0	NO CHANGE	

M026
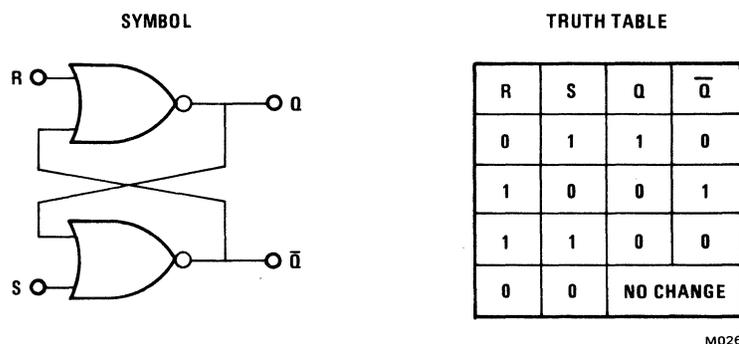
Figure 3-16.   Set/Reset Latch

Clocked Latch

This form of latch is based on a different concept from the RS latch on the previous page. See Figure 3-17. Two inverters and two transmission gates (switches) are used. One transmission gate gates the data into the latch, the other performs the feedback switching for the latch. The same clock, inverted and uninverted, is used to control the two swiches, but the clocks to the two switches are in opposite senses, such that when one switch is conducting the other is off. Thus, when the data switch is conducting, data is allowed in, but the recirculation switch is off and the data is not stored. Then, when the clocks change sense, the data switch is cut off and the last value of D is latched and recirculated. Note that this kind of latch operates as a moderate edge detector circuit, latching data that was stable at the end of a clock pulse; the data must be stable for about 30 nanoseconds before the end of the clock to be latched reliably. The clocked latch serves as the basis for many types of complex CMOS logic circuits, and is supported as a macro.

Performance and Transistor Count

Performance to be supplied. Four transistor pairs.

LOGIC CIRCUIT

SYMBOL

TRUTH TABLE

CK	D	Q	Q̄
1	1	1	0
1	0	0	1
↓	X	NO CHANGE	
0	X	NO CHANGE	
↑	1	1	0
↑	0	0	1

M027
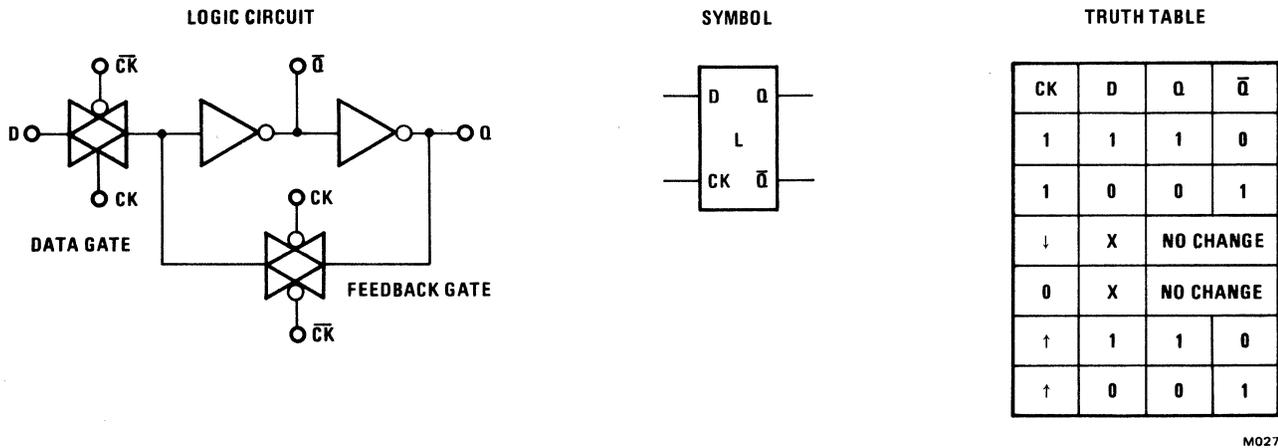
Figure 3-17. Clocked Latch

The two inverters furnish delay, drive, and sampling points for the Clocked Latch. If either a Set or Reset input is required, one of the inverters may be replaced with a NOR gate, at a slight cost in performance. In general, the use of resets on latches is encouraged, to provide a known starting point for testing and operation; at a minimum, most latches should be reset on power on.

Figure 3-18 shows a Clocked Latch with reset macro. Note that the Q̄ output is taken from a special inverter on the output, rather than from the inverter before the NAND gate. This is an instance of trading a transistor pair for performance.

Performance and Transistor Count

Performance to be supplied. Five transistor pairs.

LOGIC CIRCUIT

SYMBOL

TRUTH TABLE

R	CK	D	Q	Q̄
1	X	X	0	1
0	1	1	1	0
0	1	0	0	1
0	↓	X	NO CHANGE	
0	0	X	NO CHANGE	
0	↑	1	1	0
0	↑	0	0	1

M028
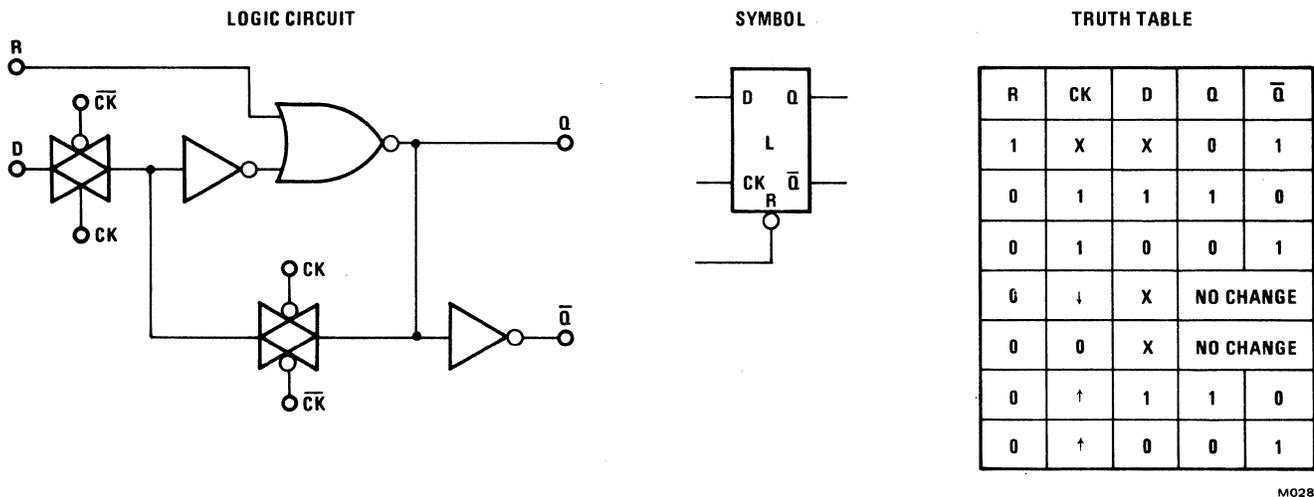
Figure 3-18.   Clocked Latch with Reset

1 May 1981

D Flip-Flop

The D flip-flop is a simple master-slave dual latch. Figure 3-19 shows such a latch, composed of two Clocked Latches in sequence, the second ("slave") with its clocks connected in the opposite sense from the first ("master"). When the clock signal is low, the data input is gated into the master latch, but is blocked from entering the slave section, which is held in its current state by the recirculation loop. When the clock signal goes high, the data input is blocked, the master section latches the input data, and the output of the master section feeds forward through the slave section to the output. When the clock signal goes low again, the slave section latches the data, and the data gate input on the master section opens again. Set or reset capability may be added by replacing the appropriate inverters with NOR gates. Figure 3-20 shows a master-slave flip-flop with sets and resets.

Performance and Transistor Count

Performance to be supplied. Eight transistor pairs without set or reset. A set or reset function adds two transistor pairs each.

LOGIC CIRCUIT

SYMBOL

TRUTH TABLE

CK	D	Q	$\overline{Q}$
↑	1	1	0
↑	0	0	1
1	X	NO CHANGE	
↓	X	NO CHANGE	
0	X	NO CHANGE	

M029
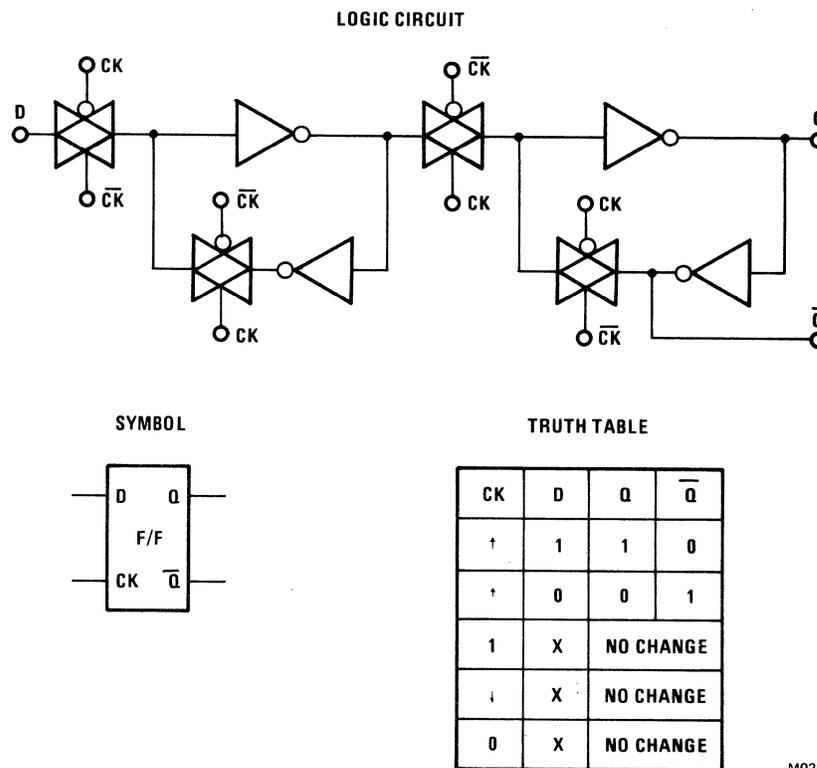
Figure 3-19.   D Flip-Flop

LOGIC CIRCUIT

SYMBOL
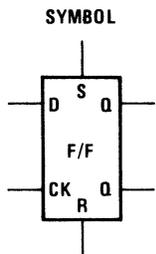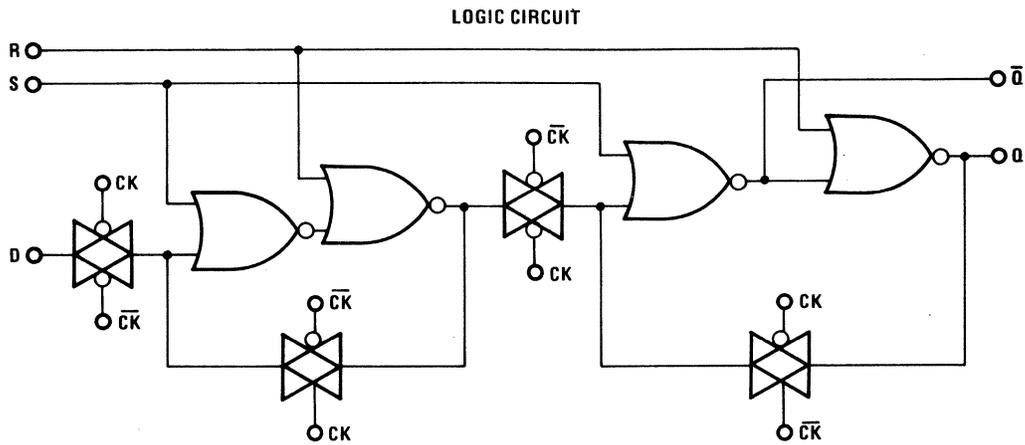
TRUTH TABLE

R	S	CK	D	Q	$\bar{Q}$
1	0	X	X	0	1
0	1	X	X	1	0
1	1	X	X	0	0
0	0	↑	1	1	0
0	0	↑	0	0	1
0	0	1	X	NO CHANGE	
0	0	↓	X	NO CHANGE	
0	0	0	X	NO CHANGE	

M030

Figure 3-20.   D Flip-Flop with Set and Reset

J-K Flip-Flop

A J-K flip-flop in CMOS is configured by adding an AND/NOR configuration of logic gates to the D input of a master-slave flip-flop. See Figure 3-21 for the schematic of this combination. The AND gate and NOR gate it feeds are the supported macro. In practice, if either of the inputs is not needed, the corresponding gates will be eliminated in the layout process.

Performance and Transistor Count

Performance to be supplied. Seventeen transistor pairs.

FULL J-K FLIP-FLOP

TRUTH TABLE

Q	J	K	D
1	X	0	1
1	X	1	0
0	0	X	0
0	1	X	1
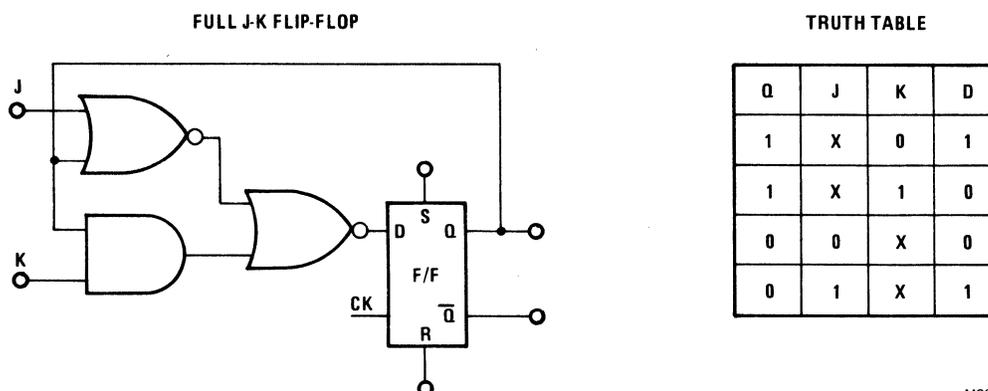
M031

Figure 3-21.   J-K Flip-Flop

INTERNAL BUFFER INVERTERS

For internal circuits that need to drive more than the normal complement of stages, special buffer inverter circuits are provided, constructed of various numbers of transistor pairs in parallel and able to drive more than the standard CMOS load (1 picofarad). The symbol for the buffer inverter is the same as a single inverter; the number of transistor pairs for a given appplication will be determined at layout time.

INPUT AND OUTPUT CIRCUITS

Each of 82 pins on the 2160 may serve as input and/or output buffers. Certain compromises are required of combined buffers; the simple cases will be shown first.

Every input to a CMOS chip must have a protection circuit to shunt away static charges. The gate of any MOS device presents such a high impedance (typically 10^{14} ohms) that many normal conditions can produce static voltages large enough to rupture the thin gate oxide and destroy the chip. A clamp diode to each of the N-type substrate and the P-type well will limit the static gate voltage during handling to about 30 volts maximum; typially the gate rupture voltage is on the order of 60-100 volts. These protection devices are provided routinely in the 2160 gate array.

For many applications, it is useful to include a pull-up device on the input. N channel devices biased to + 5 volts are provided for this purpose and supported as a macro; see Figure 3-22 for this macro.
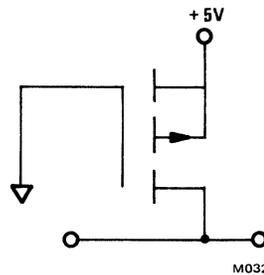

Figure 3-22.   Pull-Up Device

Power On Reset Circuit

Power on reset may be used for system initialization, to bring essential latches to a known state at power up time. This circuit uses an external capacitor with an internal Schmitt Trigger (formed by the NAND gates) to generate a pulse at power up. See Figure 3-23 for this circuit.
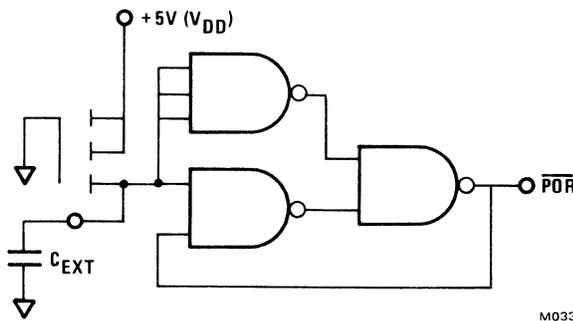

Figure 3-23.   Power On Reset Circuit

Input Buffers

As with other circuits in the CMOS gate array, on input pins groups of transistors are used for logic and buffering purposes, with PMOS devices biased toward the +5 volt power supply, NMOS devices biased toward ground. Two configurations of input buffers are used, one to support CMOS input levels, the other for TTL input levels. Figure 2-4 shows these two configurations. Note that both these configurations are inverters, with a nominal delay of 15 nanoseconds into no load or 40 nanoseconds into 1 pf according to simulation data.

This form of input buffering also provides noise immunity and good pulse squaring; in most circuit applications Schmitt triggering on the input should not be required. The noise immunity of CMOS is very good; typical noise immunity is between 30% and 50% of the supply voltage.
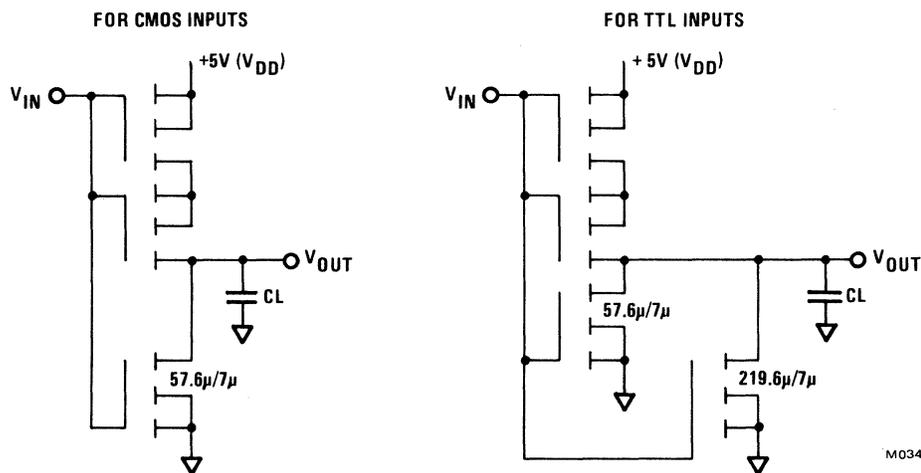

Figure 3-24.   Input Buffer Configurations

Output Buffers

The 2160 Output Buffer makes use of numerous pairs of large transistors to form a high-current inverter. The CMOS output driver is capable of driving 100 picofarads of capacitance (PC card lands, connectors, etc.) plus two LS Schottky or one standard TTL loads. The standard CMOS output driver with multiplexing is shown in Figure 3-25. Tristating ("floating") an output buffer is performed in logic in the gate array; the circuit is shown in Figure 3-26. Eight transistor pairs from the array are consumed to perform the tristating logic.

Note that the input and output buffers can share each of the 82 pins on the chip; when such sharing is done, certain compromises will be required. If the input buffer requires two stages of inversion for pulse squaring, part of the transistor resource thus consumed must come from the output buffer. In this instance, the output buffer thus formed would be capable of driving one LS Schottky load and 100 pf.

CLOCK GENERATORS

The D latch shown in Figure 3-19 can experience a problem if skewing exists between its clocks; i.e., if CK and $\overline{CK}$ are not in perfect phase. The problem evidences itself, for example, if the skew between the two clocks is approximately the same as the delay through the first inverter in the master section. In that case, the switches that gate data to the master and slave sections may both conduct at the same time, and the data may be gated through on the first clock, not the second, creating a race condition. A similar condidition can occur on the simpler, clocked latch in Figure 3-17.

The solution to this problem, of course, is to use clocks without significant skew. It may prove difficult to do this externally, however, because of delays on the PC card and similar problems; therefore it is recommended that special on-chip clock generators be used, as shown in Figure 3-27. These consist merely of inverters, but the sizes will be adjusted to suit the needs of the individual circuit layouts.
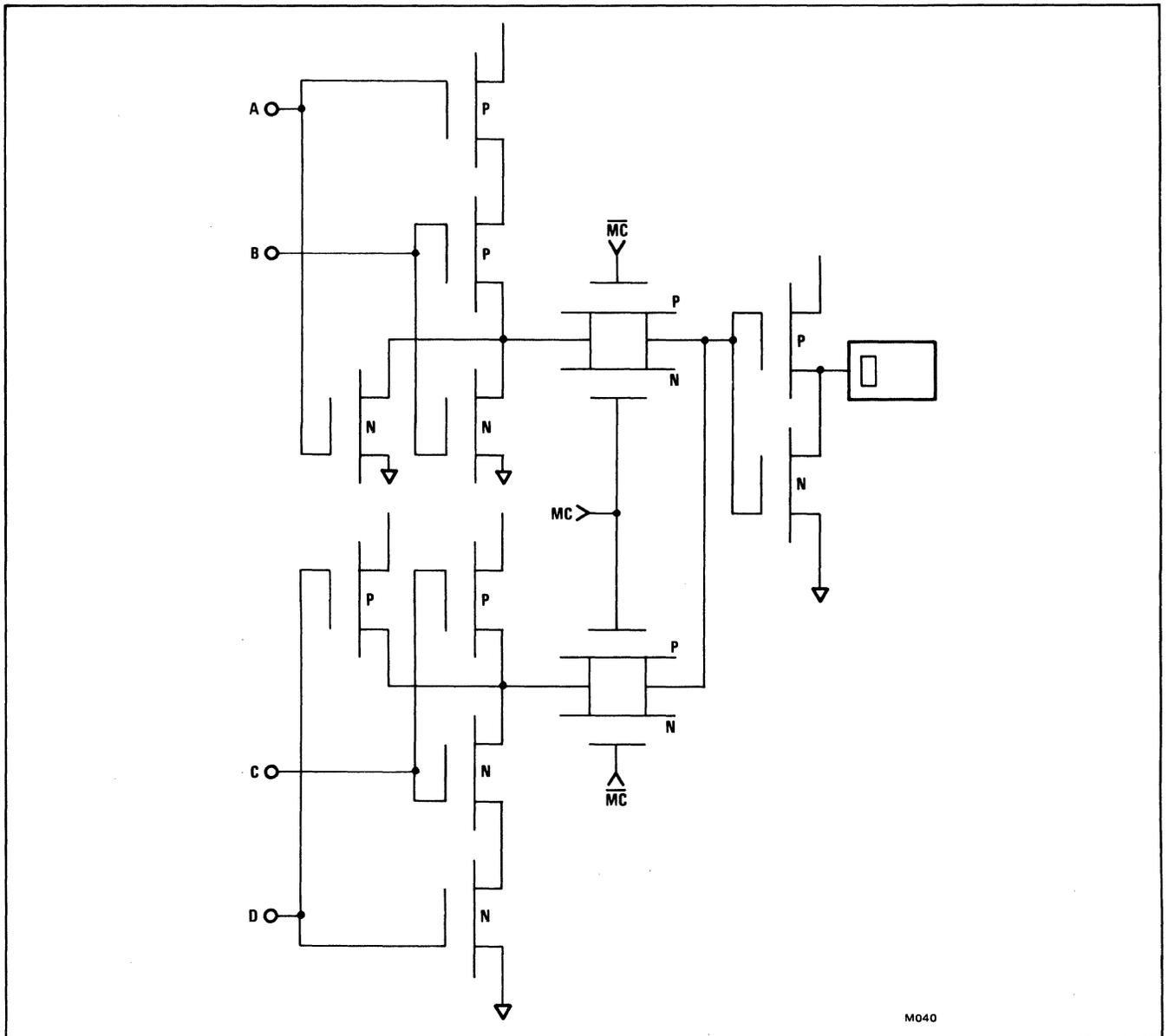
Figure 3-25.   Multiplexed CMOS Output Stage

M040
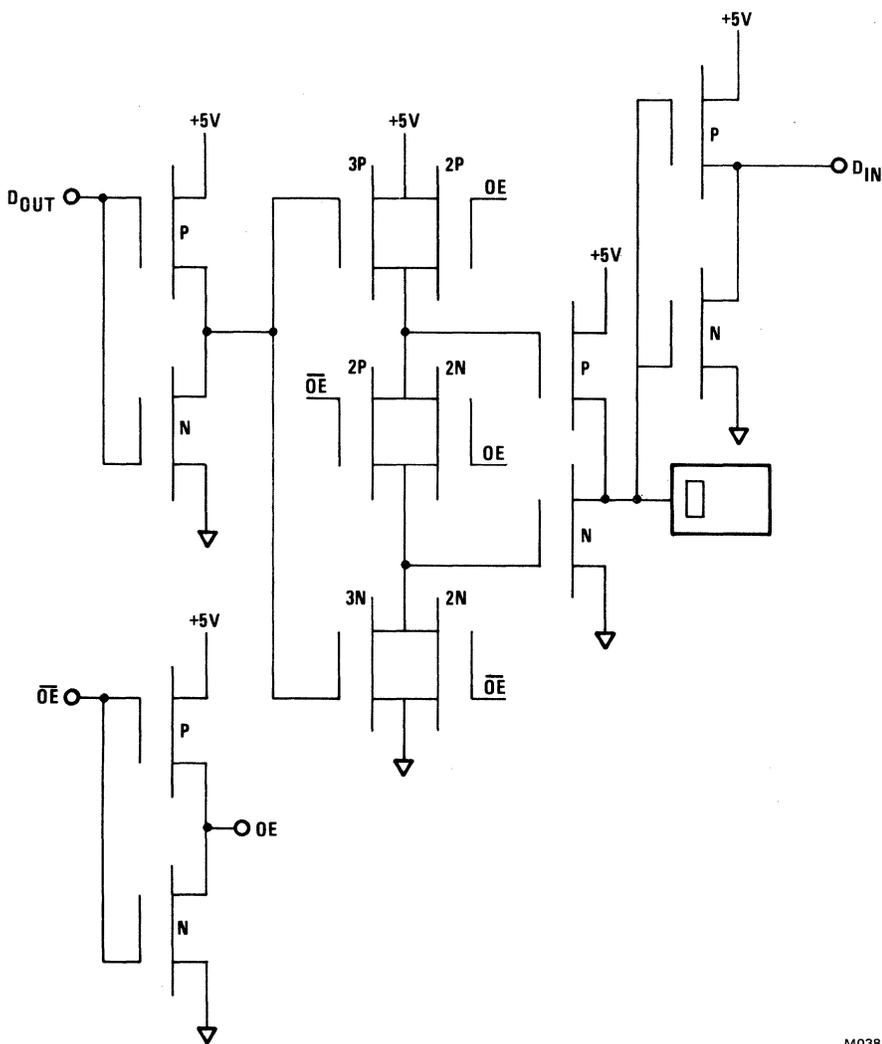
Performance Data from Simulation:

Load Capacitance 100 pf, V_{DD} = 4.75 v, V_{OL} = .8 v, V_{OH} = 4 v, T = 75°C;
T_{VOL} = 132 ns, T_{VOH} = 134 ns.

Where T_{VOL} is time to voltage output low; T_{VOH} is time to voltage output high.

Figure 3-26.   Tristate Output Buffer
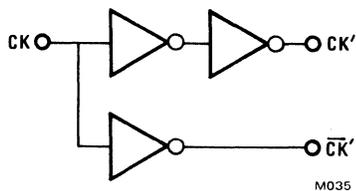
M035

Figure 3-27.   Clock Generators

SUMMARY OF MACRO CHARACTERISTICS

Table 3-1. Typical CMOS Gate Performances

Circuit Element	No. of Transistor Pairs	Tavg Into 1/3 pf (nsec)	Tavg Into 1 pf (nsec)
Simple Inverter	1	14**	18**
2-input NOR	2	29**	38**
3-input NOR	3	50**	65**
2-input NAND	2	20.5**	35**
3-input NAND	3	38**	53**
Transmission Gate	1	25**	
XOR (AND/NOR)	5	TBS	TBS
XOR (with Switches)	5	TBS	TBS
XNOR (OR/NAND)	5	TBS	TBS
XNOR (with Switches)	5	TBS	TBS
D-Latch	8		TBS
D-Latch with Reset	10		TBS
Ripple Counter	8 per stage		TBS
J-K Latch	17		TBS
Simple multiplexor	3		25**
4-1 Decode Tree	8		TBS
Input Buffer	1 (special)	15**	40**
8-input OR	11	TBS	TBS
8-input AND	11	TBS	TBS

NOTES: $T_{avg} = \dfrac{T_{on} + T_{off}}{2}$

Any pair of CMOS transistors (e.g., the CMOS inverter or one transistor pair in a gate) typically presents a load of 1/3 pf to the previous stage. A crossunder has a capacitance of 0.2 pf, and metal passes average 0.008 pf per contact. The switching time of a tristate output buffer is 130 nanoseconds into 100 pf.

* Measured.
** Simulated.
***Estimated.

GA2160 DC SPECIFICATIONS

Absolute Maximum Ratings, above which useful life may be impared.

Supply Voltage, V_{DD} 7.0V
Voltage on any input .... -0.5 to 7.0V
Current into any input... ±10ma
Storage Temperature .... -65°C — 150°C
Lead Temperature (soldering, 10 sec. max) .... 300°C
Operating Temperature .... -55°C — 125°C

DC CHARACTERISTICS

GA2160 CMOS technology is designed for power supply voltages of + 5 volts V_{DD} and 0 volts V_{SS}. Parametric limits are guaranteed for V_{DD} equal to 5 volts only.

Table 3-2. DC Characteristics

SYMBOL	PARAMETER	LIMITS			UNITS	TEMP	TEST CONDITIONS
		MIN	TYP	MAX			
V_{IH}	Input High Voltage	2.4			Volts	All	Guaranteed input high voltage.
V_{IL}	Input Low Voltage			1.5	Volts	All	Guaranteed input low voltage.
V_{OH}	Output High Voltage	4.99			Volts	25°C	I_{OH}=0ma, Inputs at 0 or 5V as per the Logic Function.
		4.95			Volts	75°C	
		4.0			Volts	All	I_{OH}=0ma, Inputs at 1.5 or 2.4V.
V_{OL}	Output Low Voltage			0.01	Volts	25°C	I_{OL}=0ma, Inputs at 0 or 5V as per the Logic Function.
				0.05	Volts	75°C	
				0.5	Volts	All	I_{OL}=0ma, Inputs at 1.5 or 2.4V.
I_{IN}	Input Current		TBS				
I_{OH}	Output High Current		TBS			−55°C +25°C +75°C	TTL Driver Output Buffer, Inputs at 0 or 5V as per the Logic Function.
I_{OH}	Output High Current		TBS			−55°C +25°C +75°C	CMOS Driver Output Buffer, Inputs at 0 or 5V as per the Logic Function.
I_Z	Output Leakage Current			10	μA	+75°C	V_{OUT}=5V

Chapter 4
Using the 2160

MACRO CELL DESIGN SUGGESTIONS

For the user of the macro library, certain macro interconnections have been worked out already. Here are some useful ones that are not supported as macros.

Basic Multiplexor Circuit

The basic multiplexor (select gate) circuit is shown in Figure 4-1. It operates as a 2-input multiplexor with a select input. The C input allows the A input to be connected to the output when true, and allows the B input through when false. The CMOS implementation uses three transistor pairs: two transmission gates ("switches") and an inverter. C switches the one transmission gate on when true, the other on when false. Note that there is no drive in this circuit — the drive must come from the previous stage.

This basic circuit element can be expanded for use in either of two dimensions, as shown in Figure 4-2, a 4-to-1 multiplexor in 8 CMOS transistor pairs. This circuit is relatively slow, as stray capacitances must be charged and discharged through several gates in series. Faster implementations of such circuits are possible; the trade-off is performance vs. complexity and number of transistor pairs.

Performance and Transistor Count

The delay through one stage of a basic multiplexor is approximately the same as through the transmission gate, 25 nanoseconds simulated. Delays through subsequent stages are estimated to be the same. The basic multiplexor element uses three transistor pairs; the 4-to-1 multiplexor eight.
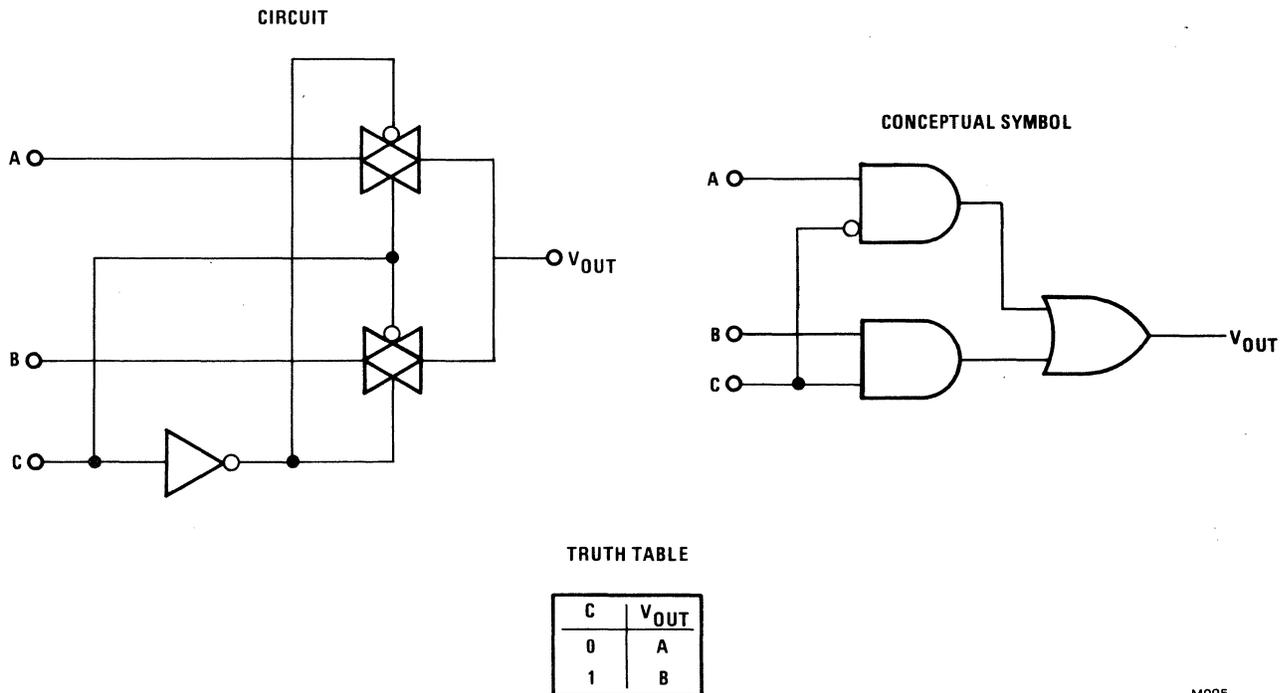

Figure 4-1.   Basic Multiplexor Circuit
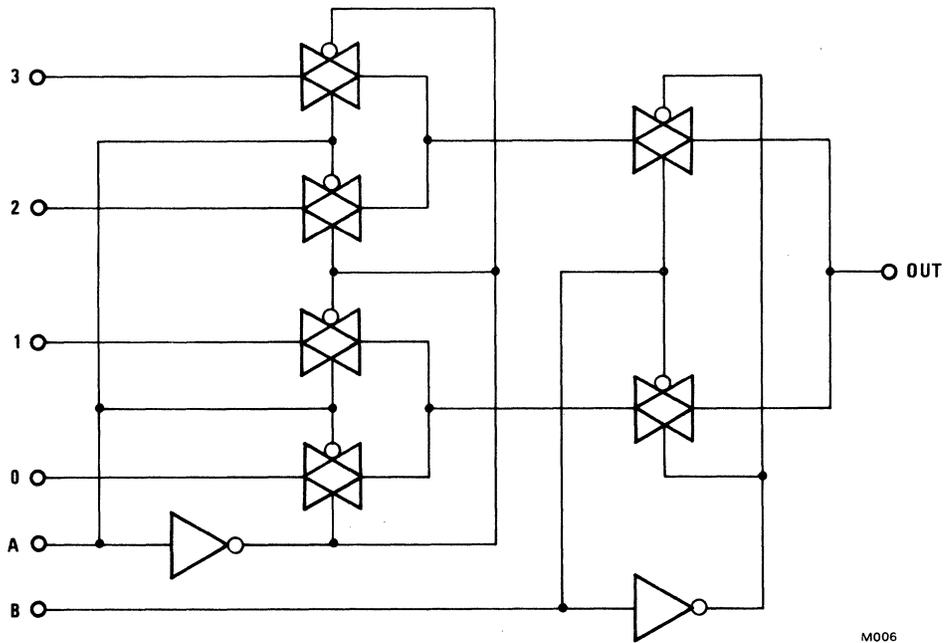
Figure 4-2.   4-to-1 Multiplexor

Ripple Counter

If the Q output of a D flip-flop is connected back to the D input, the flip-flop will change state each time the clock signal goes positive, and the output will toggle at half the clock frequency. Thus, a D flip-flop can be wired to act as a divide-by-two frequency counter. Counter chains of any length can be constructed by allowing the Q output of one stage to drive the clock input of the next stage. Thus, a divide-by-eight counter would have three stages, each made up of a D flip-flip with Q wired to D and to the next stage. This kind of counter is called a "ripple counter", because the toggle signal must ripple through each counter stage before the counting is complete. The advantage of such a counter is simplicity: no extra logic is needed. One disadvantage is that the circuit delay increases down the length of the chain, the later bits being delayed with respect to the early bits. However, this is of consequence only with high speed circuits. Figure 4-3 shows a four-stage ripple counter (divide by 16).

Divide by N Ripple Counters

A simple extension to the ripple counter is a divide-by-N counter, formed by decoding the desired count and using it as a reset for all the flip-flops in the counter sequence. See Figure 4-4 for a Divide-by-10 ripple counter and its timing. This approach has the advantage that no output spikes are produced when the counter resets to zero, and the reset logic is simple, even for long counter chains. Also, the circuit can be reconfigured easily via logic to change the counting frequency by controlling the inputs to the reset latch.
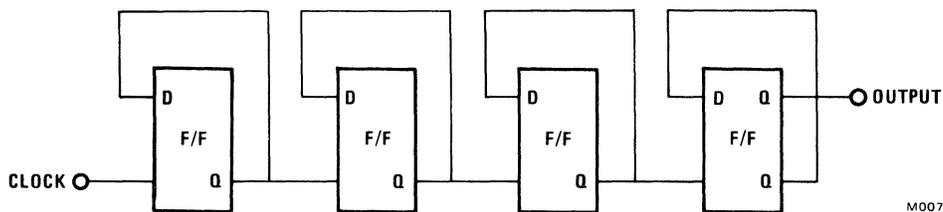

Figure 4-3.   4-Stage Ripple Counter

LOGIC CIRCUIT

LOGIC GATES

TRUTH TABLE

COUNT	Q1	Q2	Q3	Q4	D1	D2	D3	D4
0	0	0	0	0	1	0	0	0
1	1	0	0	0	0	1	0	0
2	0	1	0	0	1	1	0	0
3	1	1	0	0	0	0	1	0
4	0	0	1	0	1	0	1	0
5	1	0	1	0	0	1	1	0
6	0	1	1	0	1	1	1	0
7	1	1	1	0	0	0	0	1
8	0	0	0	1	1	0	0	1
9	1	0	0	1	0	0	0	0
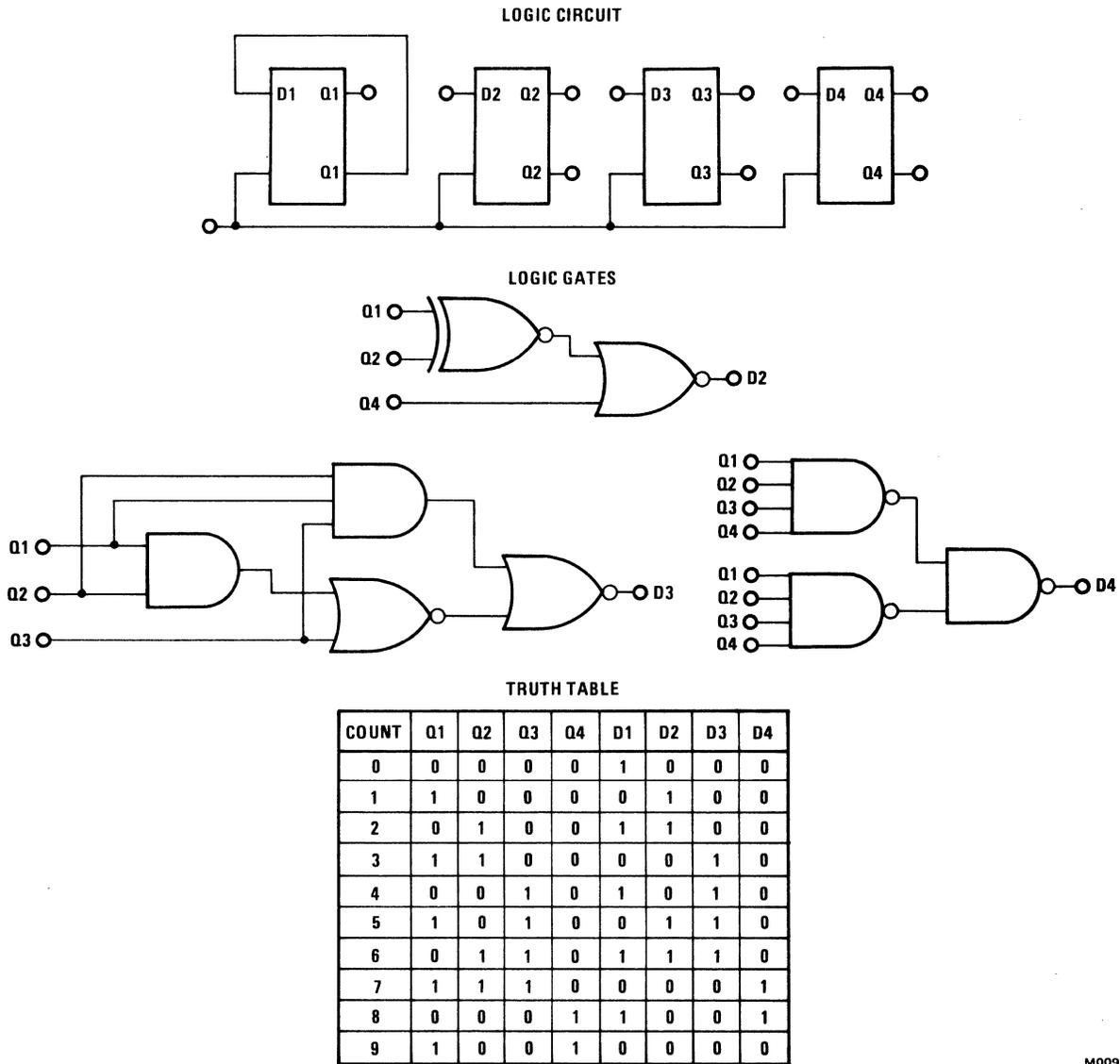
M009

Figure 4-4. Divide by 10 Ripple Counter

Synchronous Counters

The synchronous counter is designed by clocking D latches in parallel with the signal to be counted down, and connecting the D input of the stages together with the appropriate logic. In this sort of counter, each output changes state at the same positive-going clock transistion, thus avoiding the skew from early stage to late that is inevitable with a ripple counter. The logic gates needed for a counter of only a few stages will be relatively simple, but will be more complex for a longer counter. Synchronous counters require more logic than ripple counters and thus are used primarily in high-speed applications where skew between stages is undesirable. See Figure 4-5 for a Synchronous divide-by-10 Counter ("Decade Counter"). Note that the gating logic for this circuit is supported as macro logic elements. Other macros may be added if different counters are needed.

LOGIC CIRCUIT

TIMING
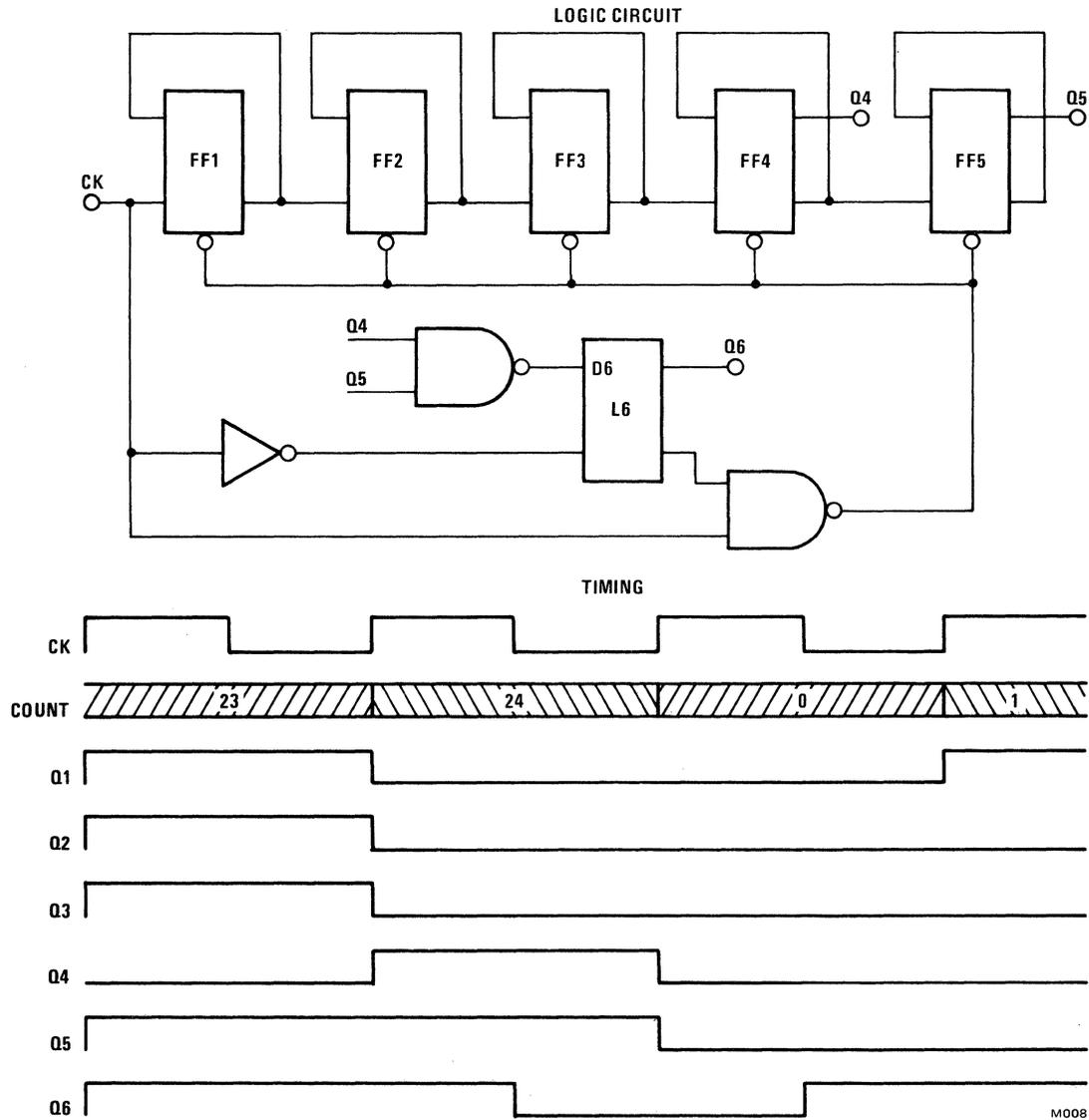
Figure 4-5.   Synchronous Divide by 10 Counter

Wide Gates

CMOS technology emphasizes the matching of on vs. off complementary transistor pairs for logic gates, to provide low quiescent power dissipation. One drawback of this approach is that it prevents the simple paralleling of elements to enhance performance: in any simple logic gate, there will be a serial charge or discharge path of length equal to the number of inputs to the gate (see the definitions of 2- and 3-input NAND and NOR gates in Chapter 3 for this concept). Such serial paths, be they for charging or discharging a node, are notoriously slow, the longer the slower. For this reason, in GA2160 logic, only two- and three-high NAND and NOR gates are supported directly.

A second reason for supporting only 2- and 3- high gates is the topology of the gate array chip itself: the natural organization of the cells on the chip is alternating pairs and triplets of complementary transistor pairs, and the topology of the interconnects allows for convenient routing of only two or three gates in series.

The need for wider gates (e.g., for wide OR gates as decoders) or equivalent functionality is recognized, however. The usual method of implementing wide OR and AND gates is discussed in this section, explaining the considerations that rule the approach.

Figure 4-6 shows an eight-high OR gate in CMOS, including the method of its implementation; Figure 4-7 shows a corresponding eight-high AND gate. The OR configuration is made up of three NOR gates into a NAND gate; this implementation is considerably faster than a single stage, eight-high CMOS gate would be for the corresponding NOR function. (Note that the combination of an inverting stage into a second inverting stage yields a non-inverting function.) This eight-high OR gate may be supported as one or more macros as future experience dictates, but initial plans call for implementing it as four separate macros: a 2-input NOR, two 3-input NORs, and a 3-input NAND, with the placement and metal routing between them to be determined at cell placement time. In general, laying out each wide gate as needed may prove better than supporting a one-of-a-kind macro. This is likely for two reasons: first, the routing of all the inputs for such a circuit would be difficult if the macro were given a compact configuration, and non-compact macros are not supported. Second, considering the interaction of capacitive loading and the drive capability of each transistor or transistor stack on each of the metal interconnects in the wide gate and its environs taken together (i.e., those feeding the wide gate, those within it, and its output), a less compact layout might prove more advantageous from a performance standpoint. Therefore, the logic designer is encouraged to use the eight-wide OR or AND gate symbol, and to consider the probable performance of the gate as it will be implemented, although the exact circuit configuration may be determined at chip layout time.

Performance and Transistor Count

Performance to be supplied. Twelve transistor pairs each.
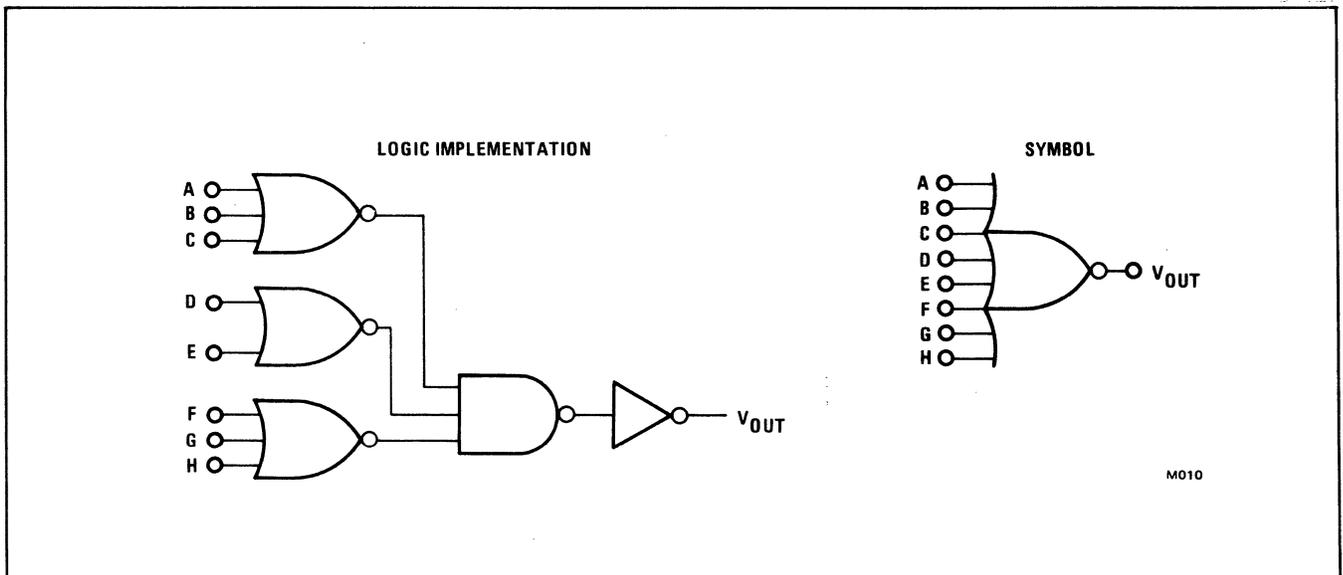
Figure 4-6.   Eight-Input NOR Gate

LOGIC IMPLEMEMTATION
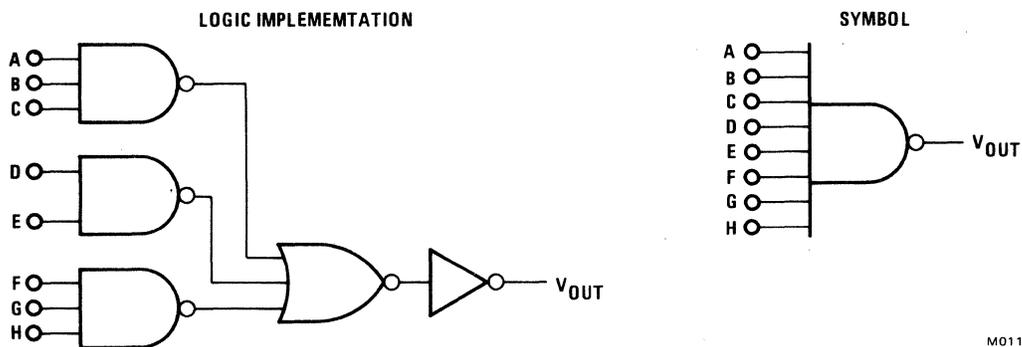
Figure 4-7. Eight-Input NAND Gate

D Latch with Enable

A typical application for transmission gates and clocking circuits is a D Latch with an enable input. This type of circuit may be used for synchronizing certain events; the latch is forced to recirculate its contents until an Enable signal is given. A method of implementation of this circuit is shown in Figure 4-8, using gating of the clock signals to achieve the required control. The transmission gate on the Enable signal is to synchronize the Enable to the clock.
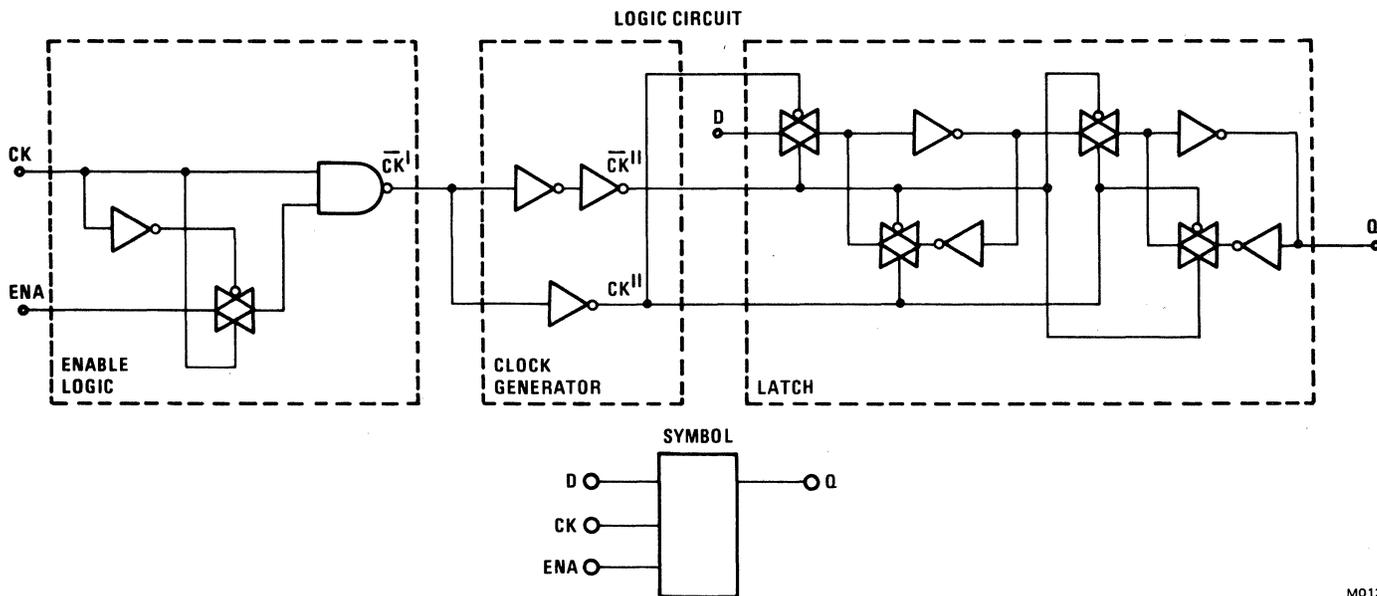

Figure 4-8. D Latch with Enable

BREADBOARDING

A well-constructed and tested breadboard is a useful tool for discovering documentation errors, design oversights, timing problems, and simple circuit errors in a digital circuit before it is cast into silicon. Changes made at the breadboard level can often be tested, verified, and documented in a few hours, where the same change made after the integration is complete might take weeks and be very expensive. Even for simple digital circuits, breadboarding is recommended. Some guidelines:

- Use standard CMOS parts. A good range of CMOS SSI and MSI circuits is available; use of the National Semiconductor 74C series is recommended. It may be unnecessary to reduce the circuit to the individual macro level if the desired function is available in MSI form, and the resulting smaller breadboard will be easier to build and check out.

- Document the breadboard logic carefully. Record pin numbers and IC part numbers for future reference. If changes are made, breadboard the changes.

- Record waveforms at key nodes. In any 2160 design that does not use the full complement of 82 data pins, it would be appropriate to bring out test points.

- Look for marginal timings. Vary supply voltages and loading to study the sensitivity of the design to parametric changes.

- Develop a test philosophy for the circuit. Initialization of internal latches is often a problem with LSI testing. Incorporating a power-on reset (and/or other resets) on internal flip-flops is recommended.

- Record input waveforms where critical, including realistic allowances for noise. Keep the breadboard and documentation for reference at test time.

COMPUTER TOOLS

The Four-Phase developed design rule checking program for LSI is currently being used. Programs are under development for logic verification of macro logic element cell placement and metal routing; for assistance at cell placement and metal routing; and simulation of logic operation at the transistor level. Assistance and documentation for the use of these programs will be provided.
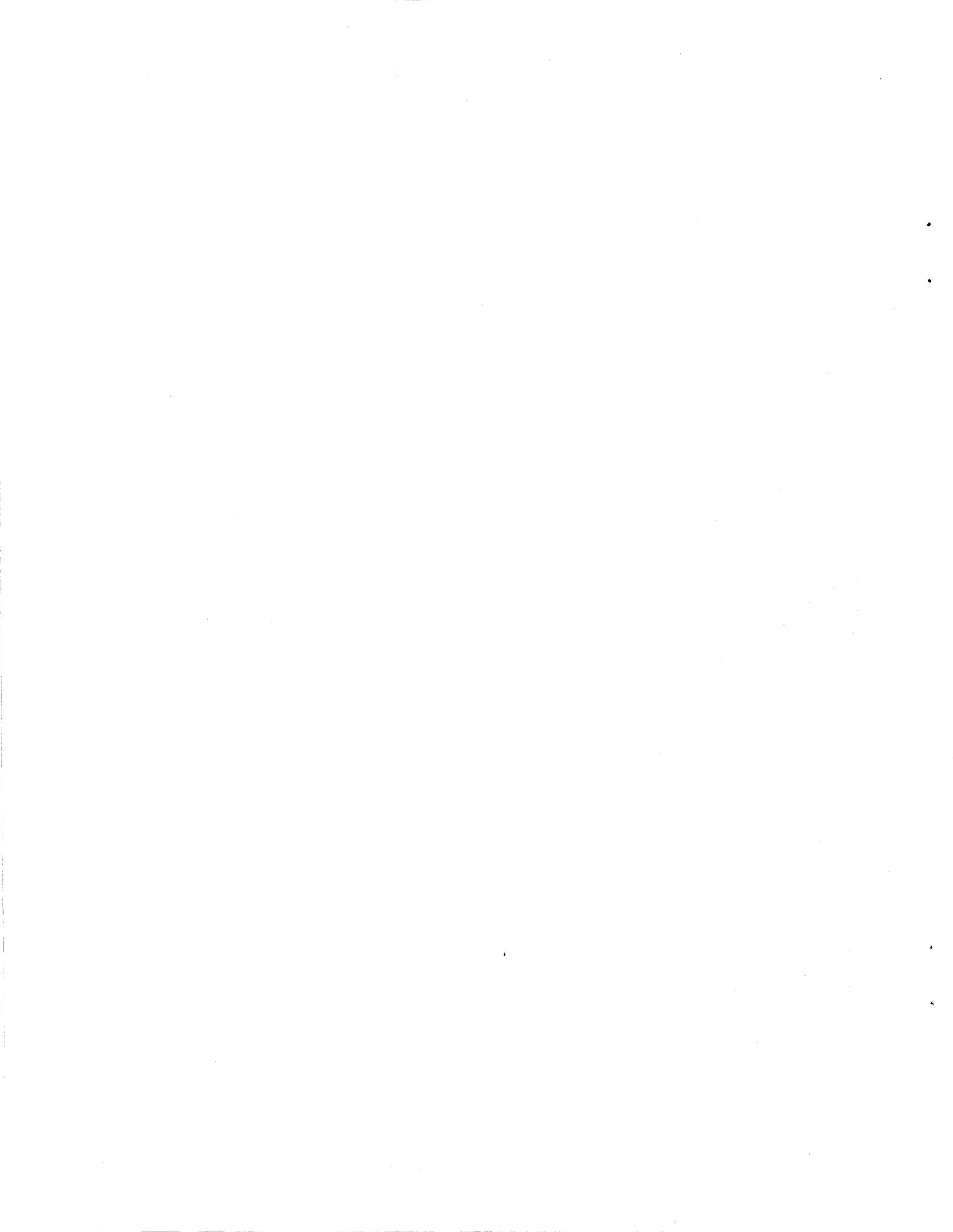
Chapter 5
Chip Design Procedures

The 2160 Gate Array is designed to support a variety of types of LSI semi-custom applications. Certain steps are required to take advantage of this flexibility and aid the chip layout process. Assuming that the circuit has been properly breadboarded, this section presents step-by-step procedures to aid the beginner in these tasks, and to help obtain a good chip design on the first try.

STEP 1:   DETERMINE PIN COUNT

From the breadboard documentation, prepare a complete list of inputs and outputs. Make sure the following are included: power supply pins, pins used for external components (resistors, capacitors, clocks, etc.), all circuit inputs and outputs, and test points. Indicate the source characteristics for all inputs and the load characteristics for all outputs. When this list is complete, a package size may be selected; 68 and 84 pin versions are supported.

STEP 2:   SIMPLIFY THE LOGIC

Using the breadboard documentation, prepare a detailed logic drawing using the macro blocks provided in this manual. In particular, MSI functions must be expanded to the supported macros and unused functions of the MSI parts eliminated. Rearrange AND and OR gates into supported NAND, NOR, and complex gate functions. If a NAND or NOR gate has more than three inputs, the logic must be reconfigured. Add buffers on heavily loaded clock and signal lines. Add output driver inverters to chip outputs. Redraw the logic diagram to reflect these refinements and check it aginst the original breadboard logic for functionality.

STEP 3:   ESTIMATE TRANSISTOR COUNT

Using the new logic diagram, assign the appropriate macro number to each macro logic element, and each chip input and output. From the macro count and the known number of transistor pairs per macro, determine the number of transistors used in the circuit. If the number of transistor pairs is no greater than 1700, the circuit should lay out without great difficulty. If it is significantly greater than 1700, a partitioning change should be considered.

STEP 4:   ASSIGN I/O PINS

Using the I/O list from Step 1, tentatively assign I/O pads. Where performance is at a premium, assistance in this area and later steps may be provided. The high current outputs are assigned first, followed by inputs. It may be necessary to assign inputs near to corresponding outputs. Power and ground pins are assigned to given locations. Test points may be assigned to any unused pins.

Chapter 6
Testing and Packaging

CHIP TESTING

The Four-Phase Universal Tester is adapted to test circuits designed using the GA2160. Logic simulations are provided by supported software, and the final output of the simulation serves as an input to the tester.

68-PIN PACKAGE

The GA2160 fits in the Four-Phase Standard 68-pin package, shown in Figure 6-1. The following information applies to this package:

Electrical Characteristics

Contact Bulk Resistance: 15 milliohm short, 20 milliohm long.

Capacitance: .5 picofarad.

Self-Inductance: 14 nanohenries short, 20 nanohenries long.

Mutual Inductance: 10 nanohenries.

Materials

Housing: glass-filled polyester.

Contact: .00005 millimeter gold plating over .00005 millimeter nickel in dimple area. Rest of contact: gold flash over .00005 millimeter nickel.

Dimensions

All dimensions are in inches [millimeters]. Dimensions A = 1.165 [29.59], B = 1.165 [29.59], C = .690 [17.53], D = 1.210 [30.73].

HOLD-DOWN
FRAME

PROBING
AREA

C

REGISTRATION
BOSSES

CONTACT NOSE
.050 [1.27]
CENTERLINE SPACINGS

.425
[10.8]

.300
[7.62]

B

CONTACT TAIL
.100 [2.54] SQ. GRID

A

LATCH

THRUSTER
CLIP

PACKAGING OUTLINE
INCLUDING TAILS FOR PROBING

.030 [0.76] MIN.
DIA. HOLE (TYP.)

.045 1.14]
DIA. PAD (TYP.)

PADS SHOWN FOR
PC BOARD
TO SUBSTRATE
RELATIONSHIP ONLY

D

.100
[2.54]
(TYP)

.100
[2.54]
TYP

.100
[2.54]
(TYP)

PC BOARD LAYOUT

.062 [1.57] DIA. HOLE
ACCEPTS ORIENTATION
BOSS OF HOUSING
DIAGONALLY OPPOSITE
THRUSTING CLIP IN HOUSING
(OPTIONAL)

M039

Figure 6-1.   68-pin Package