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		ADER /REFLER COMPT	OR HSPT PUN	СН/ СОНТ. ОН 1 (02-02	BH.NO. 0
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1. <u>IN</u>	TRODUCTION				
This spe The cont a partic the unit malfunct Table 1	cification covers rollers for these ular peripheral u (s) for which eac ions may be possi are used with a c	the entire family of systems are each des nit. Table 1 itemize h is designed. Contr ble if peripherals of ontroller.	f Punch/Reader signed to spec es each contro roller damage ther than thos	/Reeler Systems. ifically operate ller number and or operating e designated in	
		TABLE 1	a sura-sura algue suran com sun co stato cos su co sur su comato co co suo allegar e se	•	
Controller	GE Model 67 Reader or Digitronics Rea er Model 2500 With Positive Logic Unidirectional	d- *Digitronics Read er Model B2500 With Positive Logic Bidirectional	- Digitronics Reeler P4566ALCR	Teletype BRPE-11 Punch as specifi- ed in Teletype's Product Specific. 5C (8 Level 1 In. Tape, 63.3 cps, 110 VAC,no cover)	
32-028		x	x		
	hangkala laist angunt sa ang ang ang ang ang ang ata sa ang ata sa ang ang ang ang ang ata sa ang ata sa ang a		A	and and a second se	
32-072F03	X	n professional de la contratação da como a participa do calaborador (calaborador calaborador calaborador a cont	x	1.142-141.147 K. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1.	
<b>32-07</b> 2F02				Х	-
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Configura of the co unconnec	ation Table 2 show ombination Punch/ ted, or when part ystem by the custo , part number and	uld be referred to wh Reader/Reeler System of the system is sup omer. The table cont the specific control	nenever units of are shipped so oplied by GE an cains the produ ller, cable(s)	comprising of any eparately and nd the remainder uct number, des- , and peripheral(s)	
of the s cription used to : instruct: table als	form a system. The lons that specific so can be used whe	he last column refers cally apply to each p en adding peripherals	s to sections o product instal s to an existin	of the installation lation. This ng system.	
of the spectrum of the spectru	form a system. This ions that specifi- so can be used whe allation instruct: aids that can be us the unique and need	he last column refers cally apply to each p en adding peripherals ions consist of five used in conjunction w d not be directly rel	s to sections o product instal s to an existin sections with with the instru- lated to anothe	of the installation lation. This ng system. appropriate uctions. Each er.	
of the successful of the succe	form a system. Thions that specifies o can be used whe allation instruct: aids that can be used is unique and need urrently available	he last column refers cally apply to each p en adding peripherals ions consist of five used in conjunction w d not be directly rel	s to sections o product instal s to an existin sections with with the instru- lated to anothe	of the installation lation. This ng system. appropriate uctions. Each er.	PR
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SH NO. 2	CONT ON SHEET 3	LOCATION		PHOENIX	110ag 13, 1710	14/970	F-803-WA (5-68)
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R							
	Punch Reader (Uni) combina- tion	HSPT Punch	HSPT Reader Bidirectional with 8" Reeler	HSPT Reader Bidirectional With Fan Fold Bins	HSPT Reader Unidirectiona With 8" Reeler	HSPT Reader Unidirectional With Fan Fold Bins	Description
:	(02-031) -	(02-030)	(02-029) N/A	(02–027) N/A	(02-028) N/A	Q2-026)	Part Number
	32-072F01	32 <b>-</b> 072F02	32-028	32-028	32 <b>-</b> 072F03	32-072F03	Controller
	17-034F01	1 <b>7-</b> 017F02	17-034F02	17-034F01	17-034F02	17-034F01	Cable
	27-007F01	27-007F01 w/Punch & 11-034 Pane1					Punch Chassis
	GE Mod 67 or Digitro- nics Model 2500 with Positive Logic		Digitronics Model B2500 with Positiv Logic	Digitronics Model B2500 with Positiv Logic	GE Mod. 67 or Digitron- ics Model 2500 with Positive Logic	GE Mod. 67 or Digitron- ics Model 2500 with Positive Logic	HSPT Reader
	•		Digitronics Model 7e P4566ALCR	e	Digitronics Model P4566ALCR		Reeler
	2.1, 2.2, 2.4, 2.5	2.1, 2.2, 2.4, 2.5	2.1, 2.2, 2.5	2.1, 2.2, 2.5	2.1, 2.2, 2.5	2.1, 2.2, 2.5	Refer to Installa. Instruct. Sections
RE				TABLE 2			
	(02-026A20		PAC 30	OR GE-I	FIRST MADE F	SH NO.	CONT ON SHEET
2/ SH NO.	SPT PUNCH/READEI	ION FOR HS	ECIFICAT	LIATION SH	TITLE INSTA		NO.
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Panel           Punch/Reader (02-033) 32-072F01         17-034F01         27-007F02           (Uni) Control-70Al04048         17-017F02         w/o Punch           ler Only         6.43         Panel	roller only ORDER Reader (Uni- (02-0 directional) 70A104 Controller only 6.34 Punch Control-(02-0 ler Only 70A104	MADE BY W. WONG
Pane1           Punch/Reader (02-033) 32-072F01 17-034F01 27-007F02 (Uni) Control-70Al04048 ler Only 6.43         17-017F02 w/o Punch & 11-034 Pane1	roller only ORDEF Reader (Uni- (02-0 directional) 70A/04 Controller only G.34 Punch Control-(02-0 ler Only 70A/04	MADE BY
Pane1           Punch/Reader         (02-033)         32-072F01         17-034F01         27-007F02           (Uni)         Control-         70A104046         17-017F02         w/o Funch           ler         Only         G.43         Pane1	roller only ORDER Reader (Uni- (02-0 directional) 70A104 Controller only 6.34 Punch Control-(02-0 ler Only 70A104	
Pane1           Punch/Reader (02-033) 32-072F01         17-034F01         27-007F02           (Uni) Control-         70Al04048         17-017F02         w/o Punch           ler Only         6.43         Pane1         Pane1	roller only ORDER Reader (Uni- (02-0 directional) 70A104 Controller only G.34 Punch Control-(02-0 ler Only 70A104	•
(02-033)       32-072F01       17-034F01       27-007F02         70A104048       17-017F02       w/o Punch         6.43       Pane1	0RDEF (02-0 70AI041 1y G.34 -(02-0 70AI04	Description Reader (Bidirectional)Cont
Panel 32-072F01 17-034F01 27-007F02 17-017F02 w/o Punch & 11-034 Panel	2 34) 348 - 32) -048	Part Number -(02-035) - 5PEC
Pane 1 17-034F01 27-007F02 17-017F02 w/o Punch & 11-034 Pane 1	32-072F03 32-072F02	Controller 32-028
Pane1 27-007F02 w/o Punch & 11-034 Pane1	17-034F01 17-017F02	<b>Ca</b> ble 17-034F01
	27-007F02 w/o Punch	Punch Chassis
		HSPT Reader
		Reeler
2.1, 2.2, 2.3, 2.4, 2.5	2.1, 2.2, 2.5 2.1, 2.2, 2.3, 2.4,	Refer to Install. Instruct. Sections 2.1, 2.2, 2.5
TABLE 2 (Continued)		
REELER COMBINATIONS MADE FOR GE-PAC 30 (02-026A2	SH NO. FIRS	CONT ON SHEET
INSTALLATION SPECIFICATION FOR HSPT PUNCH/READER		NO.
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REV NO.		GENERAL 🏀 ELECTRIC	70A111133	
		TITLE	CONT ON SHEET 5 SH	<sub>NO.</sub> 4
		INSTALLATION SPECIFICATION FOR	OR HSPT PUNCH/READER/	
CONT ON SHEET	SH NO.	FIRST MADE FOR GE-PAC 30	(02-026A20)	
				REVISIONS
II.	INSTALLATION	TNSTRUCTTONS		
	2.1 Mother-H	oard Controller - 32-072FXX and 32-02	8 - Figure 1	
	A controller or expansion on the back p	board can be installed in any I/O slo card file. The jumper between termin panel must be removed in this location	t location of a main als 114-0 and 214-0	
	2.2 <u>Cable Co</u>	nnections and Reeler Hook-Up		
	Figure 1 show mother-board end of Punch 32-072FXX on1 mother-board 27-007F01 or	and the various Punch/Reader/Reeler c Cable 17-017F02 plugs into location 4 cy; the other end plugs into location 32-078, which is located on the Punch 27-007F02.	n a controller ombinations. One 7 on Controller 40 of the $\frac{1}{2}$ Chassis Assembly,	
	Reader Cable 32-072FXX or either Model with either r cable contain reader connec shows these d	17-034F01 is used to plug into locati 32-028; the other end connects to a D 2500 or B2500. If a Digitronics Reel eader model, reader cable 17-034F02 i s three additional wires, extending o tor, that must be connected to the Re etailed connections to the Reeler.	on 40 of contr. igitronics Reader, er P4566ALCR is used s necessary. This ut from the cable eler. Figure 1A	
	2.3 BRPE-11	Punch Modifications		
	<b>Certain</b> mecha it can be mou	nical modifications on the BRPE Punch	are necessary before	
		nted on the Punch Chassis. Refer to	Figure 2.	
	<ol> <li>Remov</li> <li>Mount</li> <li>Item drawi</li> <li>Insta</li> <li>Remov disca</li> </ol>	nted on the Punch Chassis. Refer to e tape guide and roller bracket, Item ing plate, Item 2, is placed in origi 3. Remount tape guide and roller bra ng on mounting plate. 11 extender arm, Item 4, on feed leve e chad cover and associated mounting b rd.	Figure 2. 1. nal roller holes. cket, as shown in r. bars, Item 5, and	
	<ol> <li>Remov</li> <li>Mount</li> <li>Item drawi</li> <li>Insta</li> <li>Remov disca</li> <li>Remov front</li> <li>Mount suppl</li> </ol>	nted on the Punch Chassis. Refer to e tape guide and roller bracket, Item ing plate, Item 2, is placed in origi 3. Remount tape guide and roller bra- ng on mounting plate. 11 extender arm, Item 4, on feed lever e chad cover and associated mounting f rd. e and discard stud, nut, and lock was shock mounts only, Item 6. shock mount adapter plate, Item 7, w ied with chassis.	Figure 2. 1. nal roller holes. cket, as shown in r. bars, Item 5, and her from the two ith 2-28 hardware	
	<ol> <li>Remov</li> <li>Mount</li> <li>Item drawi</li> <li>Insta</li> <li>Remov disca</li> <li>Remov front</li> <li>Mount suppl</li> <li>Secur</li> <li>Mount Figure</li> </ol>	nted on the Punch Chassis. Refer to e tape guide and roller bracket, Item ing plate, Item 2, is placed in origi 3. Remount tape guide and roller bra- ng on mounting plate. 11 extender arm, Item 4, on feed lever e chad cover and associated mounting rd. e and discard stud, nut, and lock was shock mounts only, Item 6. shock mount adapter plate, Item 7, w ied with chassis. e the two shock mounts, Item 8, with a and secure BRPE-11 Punch on punch cha e 3, Item 5.	Figure 2. 1. nal roller holes. cket, as shown in r. bars, Item 5, and her from the two ith ½-28 hardware screws specified. assis as shown in	
	<ol> <li>Remov</li> <li>Mount</li> <li>Item drawi</li> <li>Insta</li> <li>Remov disca</li> <li>Remov front</li> <li>Mount suppl</li> <li>Secur</li> <li>Mount Figur</li> <li>Item</li> </ol>	nted on the Punch Chassis. Refer to e tape guide and roller bracket, Item ing plate, Item 2, is placed in origi 3. Remount tape guide and roller bra- ng on mounting plate. 11 extender arm, Item 4, on feed lever e chad cover and associated mounting F rd. e and discard stud, nut, and lock was shock mounts only, Item 6. shock mount adapter plate, Item 7, w ied with chassis. e the two shock mounts, Item 8, with and secure BRPE-11 Punch on punch cha e 3, Item 5. 6, Figure 3. Connect P2 and J1 to BR	Figure 2. 1. nal roller holes. cket, as shown in r. bars, Item 5, and her from the two ith ½-28 hardware screws specified. assis as shown in PE-11 Punch.	
· · · · · · ·	<ol> <li>Remov</li> <li>Mount</li> <li>Item drawi</li> <li>Insta</li> <li>Remov disca</li> <li>Remov front</li> <li>Mount suppl</li> <li>Secur</li> <li>Mount Figur</li> <li>Item</li> </ol>	nted on the Punch Chassis. Refer to e tape guide and roller bracket, Item ing plate, Item 2, is placed in origin 3. Remount tape guide and roller bra- ng on mounting plate. 11 extender arm, Item 4, on feed lever e chad cover and associated mounting f rd. e and discard stud, nut, and lock was shock mounts only, Item 6. shock mount adapter plate, Item 7, w ied with chassis. e the two shock mounts, Item 8, with a and secure BRPE-11 Punch on punch cha e 3, Item 5. 6, Figure 3. Connect P2 and J1 to BR	Figure 2. 1. nal roller holes. cket, as shown in r. bars, Item 5, and her from the two ith $\frac{1}{2}$ -28 hardware screws specified. assis as shown in PE-11 Punch.	

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		INST REEL	ALLAI LER CO	ION SPECIFICAT MBINATIONS	TION FOR	HSPT PUNCH/READER/	
CONT ON SHEET	SH NO.	FIRST MADE F	FOR	GE-PAC 30		(02-026A20)	
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	2.4 Punch Chas	sis Install	ation				
	Refer to Figure	· 3.					
	<ol> <li>Two sup chassis and sup clips a support</li> <li>If fan "low pa secured the Pro Status</li> <li>The Pun through clips, the cab</li> <li>Refer t in fron shroud,</li> </ol>	port angles in any sta porting the nd screws, angles. fold bins a per" lever in an upri cessor to a indication. ch Chassis the front Item 2 and inet or rac o Figure 4. t of Punch Item 2, sn	, Ite ndard Punc Item re us locat ght p lways is in of th 4, se k. The Chass aps o	m 1, are provi 19" cabinet o h Chassis. If 2 and 3, can b ed instead of ed near the re osition. Fail receive a "De stalled onto t e cabinet or r cure the front front panel a is by means of nto the front	ded to mo r rack ca applicat e used to the punch ar of the ure to do vice Una he mounte ack. Fou of the p ssembly, four cap panel and	ount the punch apable of holding ble, four rack o secure the n tape reel, the e reel must be o this will cause vailable (DU)" ed support angles in screws and rack bunch chassis to Item 1, mounts otive screws. The d the chad box, Ite	2m
	5, 15 1 in plac 2.5 <u>System Cab</u> Figure 5 shows possible, depen	e by foam-b inet Config examples of ding on the	urati the numb	tape, Item 4. on various system er of peripher	cabinet	(s) installations expansion files	
	comprising a sy serve only as a should be consi	stem. Thes guide; eacl dered.	e con h cus	figurations ne comers' own op	ed not be timum pre	adhered to and acticability	
III.	CHECKOUT						
Run th 70A112	e system with the Puncture of	he appropria ch.	ate t	est tapes; 70Al	12456 fo	or the Reader and	
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DE BY	Nona	APPROVALS	סתת	ידיייייייייייייייייייייייייייייייייייי	DIV OR	704111133	Trainis
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1. 2.	The numbere inputs of t The lettere to the numb	d pins, 0-7, a he Address NA d pins denote ered pins as	are connect ND gate. the level shown in Ta	of the ble 2.	signal go:	ing		
	Figure 2.	Physical layo Mother-Board	ut of Addre	ss Fiel	ld on I/O			
		TA DEVICE	BLE 4 ADDRESSING		an oʻri ayna adaddari yiriyyiddin sa mamori y	ورو المعرفين المعرفين المعرفين المعرفين	na da antigan de servicio de la Competencia.	
NUMBERED PINS	LETTERED PINS	LEVEL	HEXADEC WEIGH	IMAL T	EXAMPLI ADDI	ES OF DEV RESSING	/ICE	_
					x'4C'	x	'2B'	
0	A	1		İ	0 To B	0	To B	
-	В	0	8	:	•			1
1	C D	1 0	4		1 To C	1	To D	
2	E F	1 0	2		2 To F	2	То Е	
3	G H	1 0	1		3 To H	3	То Н	-
4	J K	1 0	3		4 To J	4	To J	
5	L M	1 0	4		5 To L	5	То М	
6	N P	1 0	2		6 To P	6	To N	
7	R S	1 0	1		7 To S	7	To R	
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		1	HSPT UNIDII MAINTENANCI	RECTIONAL READER/PUNCH E SPECIFICATION	INTERFACE	
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#### I. INTRODUCTION

To increase Input/Output (I/O) capabilities of GE-PAC 30 Digital Systems, a High Speed Paper Tape Reader (HSPTR) and a High Speed Paper Tape Punch (HSPTP) are offered. By using these devices, paper tape handling capabilities and speed are increased substantially over the TTY Reader/Punch.

#### II. SCOPE

This maintenance specification is provided to describe the High Speed Reader/ Punch Controller in sufficient detail to allow a digital technician to maintain the system.

The following manuals will be of assistance in maintaining the system.

29-016 Operation and Programming Manual (Incorporated within the GE-PAC 30/3010 General Description Manual)

#### III. BLOCK DIAGRAM

It is necessary to examine the characteristics of the Paper Tape Reader and Paper Tape Punch to fully understand data handling and control features of the Device Controller. The line circuits in the HSPTR consist of nine parallel amplifiers. See Figure 1. There are eight amplifiers for data, and one channel for synchronizing from the tape feed holes.

For the HSPTP, the line circuit consists of nine solenoid drivers, plus gating to strobe the information from the Data Register to the Punch. See Figure 2. Eight of these solenoids are data channel controlled, the ninth is associated with the tape feed mechanism. All are controlled by an internal sync line from the Punch.

The interface block diagram is on Sheet 10 of Drawing 70BN3244. There are single line inputs to specify whether this is a Read or Write operation; to apply power to the Punch; and to alert the Processor to a Power Off or Load condition of the Reader (Device Unavailable - DU). The Tape Punch is operated in a closely monitored free-running mode. The tape reader maybe operated in either incremental or free-running mode. With the HSPTR/P interface, it is not possible to perform a Read/Write operation off-line.

#### IV. FUNCTIONAL DESCRIPTION

This section refers to the Functional Schematic 70B113244 & 70B113465.

4.1 Addressing

Prior to receiving any commands, the HSPTR/P Device Controller must

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		GENERAL (%) ELECTRIC	70A111229	
EV O.		TITLE	CONT ON SHEET 5 SH	ND. 4
		HSPT UNIDIRECTIONAL READER/PUNCE MAINTENANCE SPECIFICATION	H INTERFACE	
ONT ON SHEET	SH NO.	FIRST MADE FOR GE-PAC 30	<b>(02-031</b> A21)	
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rr ss A cr of f A h t e R T t d 4 T a I i i ( R a P P t	eceive its add equences which vailable Lines ontrol line 701 ail converters utput from this rom ADRSO to se fter a delay of igh. SYN1 is i he HSPTR/P has nables other mo equest, etc.) h he standard MPX he board. Refe etails on these .2 <u>Status</u> he definitions re shown in Tak nterface. The n the Local Mode n the Local Mode n the Local Mode n the Local Mode sy) is reset f egister. A Dat new character rocessor enters o output it to	ress and respond properly. This is do first send the preferred address X'12 (DAL's) 70BH3244-1 and then the AH BH3244-3. The DAL lines go through and address straps which drive a deco s decoding network is ANDed with the is et the Address flip-flop (AD). f approximately 200 nanoseconds, the S inverted and tested by the Processor to responded to its address. The AD flip odes of operation (e.g., Writing, Read by the HSPTR/P Interface. K-CH Bus circuits are located on the of er to the <u>Systems Interface Manual</u> , PO e common circuits. of the Status and Command bits for the ble 1. Five Status bits are provided Device Unavailable (DU) bit is high w e or AC power is off. In the HSPTP, D de or when a Low Tape condition exists for the HSPTR when a character is stro ta Request sets BSY. BSY is high exce in the register that has not been req the HSPTP, BSY is set when a character is the "Buffer Register and is awaiting the Punch. BSY is also set for approximation of the contact of the Status and compared the character the the punch. BSY is also set for approximation of the set of the contact of the set of the contact of the	one through micro- B' on the Data DRSO signal on the insingle-to-double oding network. The inverted signal SYN1 signal goes to determine if ip-flop being set ling, Status copper portion of CP-126, for further the HSPTR/P Interface by the HSPTR/P when the HSPTR is DU becomes active to The Busy bit obed into the Buffer ept when there is puested by the er from the g a strobing signal oximately one	REVISIO
m 1 T b n t l W F c in P c c u	oving (RN and F s set. he BSY, EX, DU, it position for bt use the EOM hat there are o hen NMTN is set or the HSPTR, a hto the Buffer cocessor. This haracter cannot hloades the Buf	Feed flip-flops both reset), the No Mo and EOM (End Of Message-Media) bits all Device Controllers. The HSPTR/P bit. The Examine Status (EX) bit is other Status conditions in the remaini t, EX is also set. In Overflow (OV) occurs if a new chara Register before the last character wa will not happen in the Incremental M arrive until the tape is started by fer Register.	occur in the same Interface does used to indicate ng four bits. cter is strobed s requested by the ode, since a new the DR signal that	

W. Wong	confuncy_	PROCESS	COMPUTER	DIV OR	70A111229	
may 20, 1970	May 6, 1970	PHEONIX,	ARIZONA	LOCATION	CONT ON SHEET $5$	sh no. 4
TH AND WA 14 MAY	0					CODE IDENT NO.

Note     TITLE     CONT ON SHEET     Son C S       HSPT UNIDIRECTIONAL READER/PUNCH INTERFACE     MAINTENANCE SPECIFICATION     Son C S       MAINTENANCE SPECIFICATION     FIRST MADE FOR     G2-031A21)       4.3     Commands       Any meaningful combination of commands can be simultaneously issued to the Device Controller. The specific command or combination of commands is sent on the DAL lines, followed by the CMDO signal on the control lines 708/13/244-3.     REVI       4.3     Command:     Command:     REVI       4.4     Command:     Command:     REVI       4.5     Interface     Control size:     REVI       4.5     Command:     Command:     REVI       4.6     Command:     Command:     REVI       4.7     Command:     Command:     REVI       4.8     Command:     Command:     REVI       4.9     Command:     Command:     Revi       4.9     Command:     Command:     Command:       This is inverted and ANDed with ADI to produce CMGO (Gated Command).     This signal is again inverted to gate the bits from the DAL's to the Command interface:       Command:     If a Read/Run is specified, the WT filp-flop 708/15244-5.     Sis rest; inhibiting a Write operation. If a Write/Run operation is specified, the WT filp-flop is set, enabling the Punch; disabling the read logic; and setting the ATN flip-flop.       TABLE				GENER/	AL 援 E	LECTRI	C	70A	111229	
OWN SHEET       SH MO.       FIRST MADE FOR       GE-PAC 30       (02-031A21)         4.3       Commands         Any meaningful combination of commands can be simultaneously issued to the Device Controller. The specific command or combination of commands is sent on the DAL lines, followed by the CMD0 signal on the control lines 70813244-3. CLO40 enters the controller as CMD0 (Command). This is inverted and ANDed with ADI to produce CMG0 (Gated Command).' This signal is again inverted to gate the bits from the DAL's to the Command flip-flops.         Because of the dual purpose of the interface (control of either Read or Write operations), a command to specify a particular operation must be given. If a Read/Run is specified, the WT flip-flop 70B113244-5. is reset, inhibiting a Write operation. If a Write/Run operation is specified, the WT flip-flop is set, enabling the PWR flip-flop; initializing the internal power supply of the Punch; disabling the read logic; and setting the ATN flip-flop.         TABLE 1         HIGH SPEED PAPER TAPE READER/PUNCH STATUS AND COMMAND BYTE DATA         BTT         NUMBER         0         NUMMER         0         NUMMER         NUMMER         OW         NUMMER         DECAUSE         BTT         OV         NMMEN <th>V ).</th> <th></th> <th>TITLE H</th> <th>SPT UNII AINTENAN</th> <th>DIRECTION NCE SPECI</th> <th>IAL READ</th> <th>ER/PUNCH</th> <th>CONT ON SHEE</th> <th>т бол shi СЕ</th> <th>NO. 5</th>	V ).		TITLE H	SPT UNII AINTENAN	DIRECTION NCE SPECI	IAL READ	ER/PUNCH	CONT ON SHEE	т бол shi СЕ	NO. 5
4.3 Commands         Any meaningful combination of commands can be simultaneously issued to the Device Controller. The specific command or combination of commands is sent on the DAL lines, followed by the CMD0 signal on the control lines 70B113244-3. CLG40 enters the controller as CMD0 (Command).' This is inverted and ANDed with AD1 to produce CMG0 (Gated Command).' This is inverted and ANDed with AD1 to produce CMG0 (Gated Command).' This signal is again inverted to gate the bits from the DAL's to the Command flip-flops.         Because of the dual purpose of the interface (control of either Read or Write operations), a command to specify a particular operation must be given. If a Read/Run is specified, the WT flip-flop 70B13244-5. is reset, inhibiting a Write operation from taking place and enabling of status outputs for a Read operation. If a Write/Run operation is specified, the WT flip-flop is set, enabling the PWR flip-flop; initializing the internal power supply of the Punch; disabling the read logic; and setting the ATN flip-flop.         TABLE 1         HIGH SPEED PAPER TAPE READER/PUNCH STATUS AND COMMAND BYTE DATA         BTT         OU         NUMBER         0         I a 2         A 4         GOMMAND         NUMBER         DECAUSE         BTT         OV         NMMIN         TATUS         STATUS	INT ON SHEET	SH NO.	FIRST M	ADE FOR	GE-I	PAC 30		(02	2-031A21)	
TABLE 1         HIGH SPEED PAPER TAPE READER/PUNCH         STATUS AND COMMAND BYTE DATA         BIT       0       1       2       3       4       5       6       7         BIT       0       1       2       3       4       5       6       7         STATUS       0       1       2       3       4       5       6       7         STATUS       0       1       2       3       4       5       6       7         STATUS       0V       NMTN       BSY       EX       DU         COMMAND       DUSABLE       ENABLE       STOD       BIN       INCE       SLEW       HETE       DEAD		4.3 <u>Commar</u> Any meaning the Device is sent on lines 70BH This is inv This signal Command fli Because of or Write op be given. is reset, i of status o specified, initializin read logic;	the DAL lin 3244-3. verted and A is again i p-flops. the dual puperations), If a Read/R nhibiting a outputs for the WT flip g the inter and settin	tion of The sp es, foll CLO40 er NDed wit nverted rpose of a comman un is sp Write of a Read of -flop is nal powe g the AT	commands becific of lowed by ters the th AD1 to to gate the int d to spe peration peration set, en er supply N flip-f	can be command of the CMD( control produce the bits erface cify a p the WT from ta abling to of the lop.	simulta or combi ) signal ller as e CMGO (d s from the (control particula flip-fla aking pla Write/Ru the PWR Punch; o	neously i nation of on the c CMDO (Com Gated Com he DAL's of eithe ar operat op 70BH ace and e un operat flip-flop disabling	ssued to commands control mand). to the r Read cion must 3244-5. mabling ion is ; the	REVIS
BIT       0       1       2       3       4       5       6       7         STATUS       OV       NMTN       BSY       EX       DU         COMMAND       DUSABLE       ENABLE       STOD       BUN       INCD       SLEW       UDITE       DEAD	• .		HIGH SPE STATU	TAB ED PAPER S AND CO	BLE 1 TAPE RE MMAND BY	ADER/PUN TE DATA	1 <b>C</b> H			
STATUS     OV     NMTN     BSY     EX     DU       COMMAND     DU     DU     DU     DU     DU				1	1		1			
COMMAND BYTE DISABLE ENABLE GTOD BIN INCO SLEU LIDITE DEAD	BIT NUMBER	0	1	2	3	4	5	6	7	
DILE DIGADLE ENABLE STOP KON   INCK   SLEW WATLE KEAD	BIT NUMBER STATUS BYTE	0 OV	1	2	3 NMTN	4 BSY	5 EX	6	7 DU	

		Dania 00 J	bii biboni					
BIT	R	EADER				PUNCH		
OV	The Overflow Buffer Regis the Reader 1 character ha This condit in the SLEW	w bit is set ster is load before the p as been tran ion can only mode.	t when the ded from previous nsferred. y happen		The Overf reset in	low bit is the Write	always Mode.	
	1. *							PRINTS TO
WADE BY W. Won	g	APPROVALS Leegevorg	PROCESS	COMPUTER	DIV OR	70A1112	29	E
FF-803-WA (5-68)	20,1970	May 9, 1970	PHOENIX.	ARIZONA 	LOCATION	CONT ON SHEET	0 9	CODE DENT NO.

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REV					CONT ON SHEET 7 S	HNO. F.
<b>NO</b> ,		HSPT MAIN	UNIDIRECTION	AL READER/PUNCH FICATION	INTERFACE	
JONT ON SHEET	SH NO.	FIRST MADE	FOR GE-PAC	30	(02-031A21)	
BIT		EADER			PUNCH	REVISIONS
NMTN	The No Motion the Reader 1 STOP command has stopped ter.	on bit is a has been is d and the f on the nex	set when ssued a tape kt charac-	The No Mot reset in t	tion bit is always the Write Mode.	S
BSY	The Busy bit fer Register an output fr	t is set wh c is empty com the Rea	nen the Buf- , waiting for ader	The Busy h Buffer Reg waiting fo from the H	oit is set when th gister is full, or an unload signa Punch.	al
EX	The Examine OV=1 or NMT	bit is set N=1.	whenever	The Examir reset in t	ne bit is always The Write Mode.	
DU	The Device W when the por tor is off, in the load	Jnavailable ver to the or the Rea position (	e bit is set Reader mo- ader lever is (straight up).	The Device set when t local stat eased), or tion exist inside the is no low fan fold b	e Unavailable bit the Punch is in a te (switch is rel- t a low tape cond ts on the tape rec te cabinet. There tape sensor on the pins.	is i- el ne
DISABLE	This command rupts from t ler from int Processor.	l inhibits the Device terrupting Interrupts	inter- Control- the are queued.	Same as fo	or the HSPTR.	
ENABLE	This command from the Dev interrupt th	l permits i vice Contro ne Processo	nterrupts ller to pr.	Same as fo	or the HSPTR.	
STOP	This command tion of the character ha next charact positioned of when the tap	l bit halts tape after is been rea er to be r over the se be stops.	the mo- the next d. The ead is ense lights	This comma punch moto	and bit turns the or off.	
RUN	This command moving and 1 ler in the F	starts th eaves the Cun mode.	e tape control-	This bit s motor.	tarts the punch	PRINTS TO
ADE BY	ç	APPROVALS MUMSTIA	PROCESS COMP	UTER DIV OR	70A111229	<b>L</b>
SSKED May	20,1970	1May 6 1910	PHOENIX, AR	TZONA LOCATION	CONT ON SHEET 7 SH	H NO. 6

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REV.		TITLE		CONT ON SHEET 8 SH	NO. 7
<b></b>		HSPT UNIDIRECTIONA MAINTENANCE SPECIF	L READER/PUNCH	H INTERFACE	
CONT ON SHEET	SH NO.	FIRST MADE FOR GE-PAC 30		(02-031A21)	
					REVISIONS
BIT	R	EADER		PUNCH	
INCR	In this mod tape is adv when the co Run mode an stops after character. stopped unt instruction and starts	e of operation, the anced one character ntroller is in the d BSY=1. The tape encountering one The tape remains il a Read Data , which resets BSY the tape moving again.	Not used.		
SLEW	In this mod tape is adv until stopp	e of op <b>erati</b> on, the anced continuously ed.	Not used.		
WRITE			Designates Paper Tape	the High Speed Punch.	
READ	Designates Tape Reader	the High Speed Paper			
	and the mode is Slew if set, one flip-flop reset with the tape mo If this control: set. DAL011 is flop. Interrupt strobed into the	specified by the SL (sle e character command increa- , either mode can be esta- ovement. ler is to be allowed inter ANDed with CMG1 to set the s are generated by this e Buffer Register from the	w) flip-flop ( ment if reset) blished withou rrupt service, he Interrupt E interface when e HSPT <b>R</b> ; upon	continuous Run . With the RN t interferring DAL bit one is nable (EBL) flip- a character is entering the	
	Write Mode; or winterface is real in the Attention interrupt condit	when a character has been ady for more data. The in h (ATN) flip-flop (Sheet tion onto the Processor I	output to the nterrupt condi 1). EBL gates /O Bus as ATNO	HSPTP and the tion is saved a saved ATN •	
	set. DALOO1 is may still be say MPX-CH Bus.	ANDed with CMG1 to reset yed in the ATN flip-flop,	EBL. Interru but ATN canno	pt conditions t be gated to the	
	The active condi- preferred states DT which is set.	tion on the Initialize Co by clearing all flip-flo	ontrol Line (Sops in the Con	CLRO) sets up troller except	
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ADE BY		APPROVALS		704111220	1
	wong	requiling PROCESS COMPU.	DEPT.	7UATTIZZ9	_
ma	420.1970	May (7, 1910 PHOENIX, ARIZ	CONA LOCATION C	CONT ON SHEET O SHI	NO. /
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G	E	N	E	R	A	L	H	EL	E	C	T	R	I	C	
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REV NO.	TITLE	CONT ON SHEET	ф.	SH NO. 8
	HSPT UNIDIRECTIONAL READER/PUNCH MAINTENANCE SPECIFICATION	INTERFACE		

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	SH NU.	TINST MADE FOR GE-PAC	30	(UZ=U3IAZI)	
	•				REVISIONS
	Whenever the F ATN, BA, EBL,	ead/Write Mode changes RN, and SL flip-flops a	, a partial initi and sets DT.	alize clears the	
	4.4 Read Oper	ation			
	In order to eft tape movement Processor. Th or Incremental Instruction.	fect a transfer of data must have been initiate e reading operation is Mode according to the	a from the HSPTR ed by a prior com then performed i configuration of	to the Processor, mand from the in the free-running the Command	
	In the free-ru and the BSY fl signal SFEEDO	nning mode of operation ip-flop is set because is active, and sets the	i, the RN and SL this is its init FEED flip-flop.	flip-flops are set ialize state. The	
	The movement of when signal CH from the photo the tape and if operations. S derives the ST produced whene of the Reader synchronously, Register by th RDLD1, which c BSY to go low. to the Process awaiting trans	f tape in the Reader is S1(70B113224-7) become -diode head in the Read s used by the HSPTR/P I ignal CHS1 goes through RBO and STRB1 signals. ver CSH1 goes active. comes into the HSPTR/P with CHS1, and is load e RDLDO signal (70B1132 auses the Device Transm When BSY goes low, th or that a character has mission to the Processo	detected by the s active. This ler, which senses interface to init a differentiato A 0.4 microseco The data from th Interface (CH011 led into the HSPT 24-2). RDLD0 is nitting flip-flop been read from or.	HSPTR/P Interface signal is derived the feed foles in iate the reading r circuit and nd STRB signal is e eight channels through CH081) R/P Buffer inverted producing (DT) to reset and is set, indicating paper tape and is	
	The Processor HSPTR/P Interf derivation of SYN1 signal af previously gat DRL bus lines of DRG1 pulse, reset output f STRB1. If the the next chara giving the Pro	requests data by activa ace responds to the Pro DRGO and its complement ter a 200 nanosecond de ed into the HSPTR/P Buf by the enabling action BSY again goes high. rom the DT flip-flop er Processor's request fo cter received from the cessor an indication th	ting the Control cessor's request (Sheet 3). DRG lay. The data with fer Register is of DRG1. In add It should be not ters a gate that or data was late Reader, OV1 woul at data has been	Line DRO. The through the O activates the hich has been unloaded onto the ition, at the end ed here that the is also fed by with respect to d become active, overwritten.	
	In the increme derived from t flip-flop (SLO Command to Run the FEED flip- data and Synch as it did in t	ntal mode, the SL flip- ne gate that is control ) (70B113224-5). When in the Incremental Mode flop. This in turn cau ronizing signal (CHS1) ne Slew Mode. However,	flop is reset and led by the reset the HSPTR Interfa , SFEEDO becomes ses the Reader to comes into the Ha when the STRB s	d the SFEEDO is side of the SL ace receives the active and sets o move tape. The SPTR/P Interface ignals become	PRINTS TO
W.	Wong	APPROVALS	OMPUTER dept.	70A111229	

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REV NO.		TITLE		CONT ON SHEET	sh no. 9
		HSPT U MAINTE	NIDIRECTIONAL RI NANCE SPECIFICAT	EADER/PUNCH INTERFACE FION	
CONT ON SHEET	SH NO.	FIRST MADE FOR	GE-PAC 30	(02-0314	21)

(02-031A21)

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active, STRB0 deactivates SFEEDO and STRB1 is now enabled through a gate to reset the FEED flip-flop which stops tape movement. As in the case of the Run Mode, BSY has become inactive and ATN set. The HSPTR will remain in this state until the Processor requests data and DRG1 is activated. At the end of DRG1, BSY and DT are set and SFEEDO is activated again to set the FEED flip-flop and allow another character to be read. Subsequent Data Requests by the Processor move the tape one character at a time in the manner just described.

#### 4.5 Write Operation

Prior to a Write operation, a RUN/WRITE Command is issued by the Processor. This command causes the WRT and PWR flip-flops to set (70B113244-5). With PWR1 active, an AC Relay Driver activates the Power Supply of the HSPTP. As soon as the HSPTP Power Supply is activated, VCKO becomes active, initiating a one second delay circuit. This delay raises BSY to inhibit a Write operation from taking place while the Punch mechanism comes up to speed. At the end of the one second delay, BSY1 is inactive, an interrupt is generated, and the HSPTP is ready for use.

(Note that when the PWR flip-flop is cleared, the one second timer is recycled and ready for use within ten milliseconds.)

The Processor transfers data from the DAL lines to the HSPTP by activating the DAO control line. DAO is inverted in the HSPTR/P Interface and used to derive the signal DAGO. Approximately 200 nanoseconds after DAGO goes high, SYN1 goes high. SYN1 is inverted and send to the Processor to indicate that the HSPTR/P Interface received the information sent. At this time, BSY1 is inactive due to either initialization, or completion of a previous Write or Read operation by the HSPTR/P Interface. DAGO is inverted and ANDed with the rest output from the Buffer Available (BA) flip-flop generating the signal GDAGO (70B113244-4). GDAGO is inverted(70B113244-6) and gates the information into the Buffer Register. At the same time GDAGO is used to toggle the BA flip-flop, indicating that a byte of data is waiting to be output to the Punch. BAl is then ANDed with WTl causing BSY to go high, and preventing further information to be sent by the Processor.

An internal Sync signal generated by the HSPTP is sent through a wave shaping circuit 70B113465 producing the 1.0 millisecond signal, PSYNO. When the Punch is ready to receive information, PSYNO goes low. PSYNO is inverted in the HSPTR/P Interface and ANDed with BAl (70B113244-4).

This output goes to the Timer (TM) flip-flop, causing TMO to become active. The output, TMO, then goes to a 4.5 millisecond delay, producting the gating control signals GPO, GPOA, and GP1. GPOA controls the output gating from the Buffer Register producing the signals

MADE BY APPROVALS DIV OR 70A111229 PROCESS COMPUTER Ung W. Wong \_ DEPT ISSU sh no. 9 LOCATION CONT ON SHEET 10 PHOENIX, ARIZONA CODE IDENT NO.

# GENERAL GENERAL E ELECTRIC 70A111229 MO. TITLE CONT ON SHEET 11 SH NO. 10 HSPT UNIDIRECTIONAL READER/PUNCH INTERFACE MAINTENANCE SPECIFICATION CONT ON SHEET SH NO. FIRST MADE FOR GE-PAC 30 (02-031A21) REVISIONS

PNCH011 through PNCH081. PNCH011 through PNCH081 are fed into eight solenoid drivers (70B113465) which activates the eight punches of the data channels. A PNCH signal going high, causes the solenoid driver to create a ground on the Punch, activating the Punch solenoid to produce a hold in the tape. The tape feed solenoid is controlled separately by the signal GP1 and is activated at each character output. The GP0 signal is fed back to the trigger of the BA flip-flop causing it to reset. With BA1 inactive, BSY1 becomes inactive and the HSPTR/P Interface is now ready to receive another byte of data from the Processor.

#### V. MAINTENANCE

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The High Speed Reader/Punch Controller requires no maintenance or adjustment. The Reader and Punch requires periodic maintenance such as cleaning and lubrication. For a procedure and the maintenance requirements, refer to the manufacturers operating and service manual

Performance tests of the system can be made on the system by using the diagnostic programs 70A112456and 70A112457. The diagnostic programs will assist in trouble-shooting the controller.

#### VI. TIMING DIAGRAM

The timing for the two operating modes of the Controller is shown in Figures 3 and 4.

![](_page_25_Figure_7.jpeg)

![](_page_26_Figure_0.jpeg)

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	HSPT UNIDIRECTI	ONAL READER/PUNCH I	NTERFACE		
	MAINTENANCE SPE	CIFICATION			
ONT ON SHEET	H NO. FIRST MADE FOR GE	-PAC 30	(02-0)	31421)	
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MNEMONIC	MEANING		LOCATION		
<b>M</b> ID	0		340112044	2 70	
GMDDCT	Command		708113244	275	
GMDRSI	Command Reset		705113244	100	
CMG	Command Gated		708113244	372	
DAI	Data Available		700113244	313	
DAGO	Gated Data Avai	lable	/08/13244	303	
DALOX	Data Available	Lin <b>e</b> s	708113244	1F2-1F7	
DR1	Data Request		708113244	314	
DRGO	Gated Data Requ	est	70B113244	304	
DRLOX	Data Request Li	nes	708113244	282-287	
DT	Device Transmit	flip-flop	70B113244	405	
DU	Device Unavaila	ble	70B113244	459	
DUP1	Data Available	Punch	70B113465	389	
DV <b>C</b> KO	De <b>la</b> y - Voltage	Check	70B113244	8E5	
EBL	Enable		70B113244	554	
FEED	Tape Feed flip-	flop	708113244	7KB	
FEED	Feed Coil	•	70B113465	3M1	
GDAG	Gate Data Availa	able	70B113244	4H5	
GND	Ground		70B113465	386	
GP	Gate to Punch		70B113744	3PI	
CP1	Gate To Punch		70B113465	3B3	
	Logd Data		708113244	687	
	No Motion Tane		708113244	7M1	
007	No motion lape	100	708113244	716	
DMOUOV1	Overriow rip-i	төр	700113244	802.900	
PNGHUX1 DNGUO11	Output to Punch		100113244	102	
PNCHUII			700112465	10.0	
through	Input To Punch		/00112403 t	nrough	
PNCH041				188	
PNCH051				2B3	
th <b>ro</b> ugh	Input To Punch		70B113465 t	hrough	
PNCH081				<b>2</b> B <b>8</b>	
P010				1M2	
through	Punch Output		70B113465 t	hrough	
P040				1M8	
P050				2M2	
<b>thro</b> ugh	Punch Output		708113465 t	h <b>ro</b> ugh	
P080	•			2M8	
PSYN0	Punch Sync		70B113465	385	
PSYNO	Punch Svnc		708113244	4KI	
PWR	Punch Power fli	o-flop	70B113244	5F8	
PWR1A	Punch Power	r	70B113465	387	
RACKO	Received Acknow	ledged	70B113244	348	
RDLD	Read Data Load I	Data	70B113244	6A7	
RMT	Remote		70BI 13465	3148	-
DM	Nemole Dun flin flor		70B112011	5N8	
ALN CATINIO	RUN IIIP-IIOP Cat Amm Elia El.		70000244 700112011	200	
SALINU	Set AIN FILP-FIC	yy Fratriali-a	700112011	110	Maat Marco - Adrima
SULKU	System Clear	initialize	TORNEONA	EAA	
9Г	Siew flip-flop		100100044		PRINTS
E BY	APPROVALS		704111220		
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	******	HSPT UNIDIRECTIONAL READER/PU MAINTENANCE SPECIFICATION	JNCH INTERFACE	
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MNEMONTO	1	MFANING	ΙΟΓΔΤΤΟΝ	
	•		LOOATION	
SRO	·	Status Request	70 B113244 3A4	
SRG		Gated Status Request	70B113244 3J3	
STRB		Strobe	70B113244 7F4	
TACK	•	Transmit Acknowledge	70B113244 3A9	
TCA		Timer Coil High	70B113465 3M6	
TCG		Timer Coil Ground	70B113465 3M6	
TM		Punch Timer flip-flop	70B113244 455	
WT		Write/Read flip-flop	70B113244 5H7	
VCKA		Voltage check of positive 15	70 B113244 785	
		volts from Reader.		
VCKO		Voltage check of negative 28	70 B113244 BP9	
		volts from Punch.		
VCK0		Voltage Check of Negative 28	70B113465 3B4	
		Volts from Punch.		
XRP		Device Controller common	70B113465 868	
		pullup resistor. Ties unused		
		gate input to positive 5 volts		
•		through a 1 kilohm resistor.		
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Publication Number 29-211R03 MODEL 2540

# HIGH SPEED PAPER TAPE READER/PUNCH UNIDIRECTIONAL INTERFACE MAINTENANCE MANUAL

Consists of:

Installation Specification Maintenance Specification Schematic Schematic 02-186A20 02-172A21 02-172R04D08 27-007F01B08

![](_page_29_Picture_5.jpeg)

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02-186A20 July 1970

# HIGH SPEED PAPER TAPE READER/PUNCH/REELER COMBINATION INSTALLATION SPECIFICATION

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## HIGH SPEED PAPER TAPE READER/PUNCH/REELER COMBINATION INSTALLATION SPECIFICATION

#### 1. INTRODUCTION

This specification covers the entire INTERDATA family of Punch/Reader/Reeler Systems. The controllers for these systems are each designed to specifically operate a particular peripheral unit. Table 1 itemizes each controller number and the unit(s) for which each is designed. Controller damage or operating malfunctions may be possible if peripherals other than those designated in Table 1 are used with a controller.

The configuration shown on Table 2 should be referred to whenever units consisting of any of the combination Punch/Reader/Reeler System are shipped separately, or when part of the system is supplied by INTERDATA and the remainder of the system by the customer. The table contains the product number, description, part number and the specific controller, cable(s), and peripheral(s) used to form a system. The last column refers to sections of the installation instructions that specifically apply to each product installation. This table also can be used when adding peripherals to an existing system.

#### 2. SCOPE

The installation instructions are in two sections. The first section (2) is in five parts, with appropriate drawing aids that can be used in conjunction with the instructions. Each section is unique and need not be directly related to another. The second section (4) is devoted to the various controllers with drawings showing proper cable connections between mother-board and peripheral unit(s).

#### 3. INSTALLATION INSTRUCTIONS

3.1 Mother-Board Controller 32-136FXX and 32-138FXX

A controller board can be installed in any I/O slot location of a main or expansion card file. The jumper between Terminals 114-0 and 214-0 on the back panel must be removed from this location. Refer to INTERDATA Publication Number 29-003, <u>Systems Interface Manual</u>, Sections on "Mechanical Layout and Wiring", "Interrupt Control", and "Multiplexor and Selector Channel Wiring Data".

#### 3.2 Cable Connections and Reeler Hook-Up

Figure 1 shows the proper cable connections between a controller mother-board and the various Punch/Reader/ Reeler combinations. One end of Punch Cable 17-017F02 plugs into location 47 on Controller 32-136FXX; the other end plugs into location 40 of the 1/2 mother-board 32-078, which is located on the Punch Chassis Assembly, 27-007F01, 27-007F02, or 27-007F04.

Reader Cable 17-107F01 is used to plug into location 40 of Controller 32-136FXX or 32-138FXX; the other end connects to a Digitronics Reader, either Model 2540 or B2540. If a Digitronics Reeler 6040A is used with either Reader model, Reader Cable 17-107F02 is necessary. This cable is necessary to connect Reader/Reeler combinations.

Controller	Digitronics Reader Model 2540 With Positive Logic Unidirectional	Digitronics Reader Model B2540 With Positive Logic Bidirectional	Digitronics Reeler 6040A	Teletype BRPE-11 Punch as specified in Teletype's Product Specification 5C (8 Level 1 Inch Tape, 63.3 cps, 110 VAC, no cover)
32-138		x	x	
32-136F03	x		x	
32-136F02				X
32-136F01	X		X	X

#### TABLE 1. CONTROLLERS AND PERIPHERALS

### TABLE 2. CONFIGURATION OF COMBINATIONS PUNCH/READER/REELER/CONTROLLER

Product Number	Description	Part Number	Controller	Cable	Punch Chassis	HSPT Reader	Reeler	Refer To Installation Instruction Sections
7-408	HSPT Punch 110V, 50 Hz	02-171F02	32-136F02	17-017F02	27-007F04 w/Punch and 11-034 Panel			3.4,3.2, 3.3,3.4, 3.5
7-409	Punch/Reader Unidirectional Combination 110V,50 Hz	02-172F02	32-136F01	17-107F01 17-017F02	27-007F04 w/Punch and 11-034 Panel	Digitronics Model 2540 with Posi- tive Logic		3.1,3.2, 3.3,3.4, 3.5
7-410	HSPT Reader Unidirectional With Fan Fold Bins 110V, 50/60 Hz	02-186F01	32-136F03	17-107F01		Digitronics Model 2540 with Posi- tive Logic		3.1,3.2, 3.5
7-410/7-415	HSPT Reader Unidirectional With 8" Reeler 110V,50/60Hz	02-182	32-136F03	17-107F02		Digitronics Model 2540 with Posi- tive Logic	Digitronics Model 6040A	3.1,3.2, 3.5
7-411	HSPT Reader Bidirectional With Fan Fold Bins 110V, 50/60 Hz	02-187F01	32-138	17-107F01		Digitronics Model B2540 with Posi- tive Logic		3.1,3.2, 3.5
7-411/7-415	HSPT Reader Bidirectional With 8" Reeler 110V, 50/60 Hz	02-183	32-138	17–107F02 <sup>-</sup>		Digitronics Model B2540 with Posi- tive Logic	Digitronics Model 6040A	3.1,3.2, 3.5
7-412	HSPT Punch 110V,60 Hz	02-171F01	32-136F02	17-017F02	27-007F01 w/Punch and 11-034 Panel			3.1,3.2, 3.3,3.4, 3.5
7-413	Punch/Reader Combination Unidirectional 60 Hz	02-172F01	32-136F01	17-107F01 17-017F02	27-007F01 w/Punch and 11-034 Panel	Digitronics Model 2540 with Posi- tive Logic		3.1,3.2, 3.3,3.4, 3.5
7-414	Reader (Bidi- rectional) Controller only 50/60 Hz	02-185	32-138	17-107F01				3.1,3.2, 3.5
7-416	Reader (Uni- directional) Controller only 50/60 Hz	02-184	32-136F03	17-107F01				3.1,3.2, 3.5
7-417	Punch Control- ler only 50/60 Hz	02-181F01	32-136F02	17-017F02	27-007F02 w/o Punch and 11-034 Panel			3.1,3.2, 3.5
7-418	Punch/Reader Unidirectional Controller only 50/60 Hz	02-188F01	32-136F01	17-107F01 17-017F02	27-007F02 w/o Punch and 11-034 Panel			3.1,3.2, 3.3,3.4, 3.5

![](_page_33_Figure_0.jpeg)

Figure 1. Cable Connections - Controller to Punch, Readers, and Reeler

3.3 BRPE-11 Punch Modifications

Certain mechanical modifications on the BRPE-11 Punch are necessary before it can be mounted on the Punch Chassis. Refer to Figure 2.

- 1. Remove tape guide and roller bracket, Item 1.
- 2. Mounting plate, Item 2, is placed in original roller holes.
- 3. Item 3. Remount tape guide and roller bracket, as shown in drawing on mounting plate.
- 4. Install entender arm, Item 4, on feed lever.
- 5. Remove chad cover and associated mounting bars, Item 5, and discard.
- 6. Remove and discard stud, nut, and lock washer from the two front shock mounts only, Item 6.
- Mount shock mount adapter plate, Item 7, with 1/4-28 hardware supplied with chassis.
- 8. Secure the two shock mounts, Item 8, with screws specified.
- 9. Mount and secure BRPE-11 Punch on Punch Chassis as shown in Figure 3, Item 5.
- 10. Item 6, Figure 3. Connect P2 and J1 to BRPE-11 Punch.

- 3.4 Punch Chassis Installation (Refer to Figures 3 and 4).
  - Two support angles, Item 1, are provided to mount the Punch chassis in any standard 19" cabinet or rack capable of holding and supporting the Punch chassis. If applicable, four rack clips and screws, Items 2 and 3, can be used to secure the support angles.
  - When fan fold bins are used instead of the Punch tape reel, the "low paper" lever located near the rear of the reel must be secured in an upright position. Failure to do this will cause the Processor to always receive a "Device Unavailable (DU)" Status indication.
  - 3. The Punch chassis is installed onto the mounted support angles through the front of the cabinet or rack. Four screws and rack clips, Items 2 and 4, secure the front of the Punch chassis to the cabinet or rack.
  - 4. Refer to Figure 4. The front panel assembly, Item 1, mounts in front of Punch chassis by means of four captive screws. The shroud, Item 2, snaps onto the front panel and the chad box, Item 3, is inserted between the two fan fold bins, where it is held in place by foam-backed tape, Item 4.

![](_page_34_Figure_0.jpeg)

Figure 2. Punch Modifications

![](_page_35_Figure_1.jpeg)

![](_page_36_Figure_0.jpeg)

![](_page_36_Figure_1.jpeg)

#### 3.5 System Cabinet Configuration

Figure 5 shows examples of the various system cabinet(s) installations possible, depending on the number of peripherals and expansion files comprising a system. These configurations need not be adhered to and serve only as a guide; each customer's own optimum practicability should be considered.

4. TEST

Run the system with the appropriate test program; 06–016 for the Reader and 06–037 for the Punch.

5. CONTROLLER INSTALLATION SPECIFICATION

#### 5.1 Reader/Punch

The controller can be installed in any I/O slot location of a main or expansion card file. The jumper between Terminals 114-0 and 214-0 on the back panel must be removed in the location selected.

Refer to the <u>Systems Interface Manual</u>, Publication Number 29-003, sections on "Mechanical Layou and Wiring", "Interrupt Control", and "Multiplexor and Selector Channel Wiring Data".

Figure 6 shows the proper cable connection between the mother-board controller and the peripheral units.

![](_page_36_Figure_11.jpeg)

Figure 5. System Cabinet Configuration

![](_page_37_Figure_0.jpeg)

Figure 6. Reader/Punch

If the Punch uses fan fold bins instead of the tape reel, the "low paper" lever near the Punch reel must be secured in an upright position. Failure to do this will cause the Processor to always receive a "low paper" status indication.

#### 5.2 Punch Mother-Board

The controller can be installed in any I/O slot location of a main or expansion card file. The jumper between Terminals 114-0 and 214-0 on the back panel must be removed in the location selected.

Refer to the <u>Systems Interface Manual</u>, Publication Number 29-003, sections on "Mechanical Layout and Wiring", "Interrupt Control", and "Multiplexor and Selector Channel Wiring Data".

Figure 7 shows the proper cable connection between the mother-board controller and the peripheral unit.

![](_page_37_Figure_7.jpeg)

Figure 7. Punch Mother-Board

If the Punch uses fan fold bins instead of the tape reel, the "low paper" lever near the Punch reel must be secured in an upright position. Failure to do this will cause the Processor to always receive a "low paper" status indication.

#### 5.3 Unidirectional Reader/Reeler

The controller can be installed in any I/O slot location of a main or expansion card file. The jumper between Terminals 114-0 and 214-0 on the back panel must be removed in the location selected.

Refer to the <u>Systems Interface Manual</u>, Publication Number 29-003, sections on "Mechanical Layout and Wiring", "Interrupt Control", and "Multiplexor and Selector Channel Wiring Data".

Figure 8 shows the proper cable connection between the mother-board controller and the peripheral devices.

![](_page_37_Figure_14.jpeg)

Figure 8. Unidirectional Reader/Reeler

#### 5.4 Bidirectional Reader/Reeler

The controller can be installed in any I/O slot location of a main or expansion card file. The jumper between Terminals 114-0 and 214-0 on the back panel must be removed in the location selected.

Refer to the <u>Systems Interface Manual</u>, Publication Number 29-003, sections on "Mechanical Layout and Wiring", "Interrupt Control", and "Multiplexor and Selector Channel Wiring Data".

Figure 9 shows the proper cable connection between the mother-board controller and the peripheral units.

![](_page_37_Figure_20.jpeg)

Figure 9. Bidirectional Reader/Reeler

#### 5.5 Unidirectional HSPTR

The controller can be installed in any I/O slot location of a main or expansion card file. The jumper between Terminals 114-0 and 214-0 on the back panel must be removed in the location selected.

Refer to the <u>Systems Interface Manual</u>, Publication Number 29-003, sections on "Mechanical Layout and Wiring", "Interrupt Control", and "Multiplexor and Selector Channel Wiring Data".

Figure 10 shows the proper cable connection between the mother-board controller and the peripheral units.

![](_page_38_Figure_4.jpeg)

![](_page_38_Figure_5.jpeg)

#### 5.6 Bidirectional HSPTR

The controller can be installed in any I/O slot location of a main or expansion card file. The jumper between Terminals 114-0 and 214-0 on the back panel must be removed in the location selected.

Refer to the <u>Systems Interface Manual</u>, Publication Number 29-003, sections on "Mechanical Layout and Wiring", "Interrupt Control", and "Multiplexor and Selector Channel Wiring Data".

Figure 11 shows the proper cable connection between the mother-board controller and the peripheral units.

![](_page_38_Figure_10.jpeg)

#### Figure 11. Bidirectional HSPTR

#### 5.7 Reader/Punch Mother-Board

The controller can be installed in any I/O slot location of a main or expansion card file. The jumper between Terminals 114-0 and 214-0 on the back panel must be removed in the location selected.

Refer to the <u>Systems Interface Manual</u>, Publication Number 29-003, sections on "Mechanical Layout and Wiring", "Interrupt Control", and "Multiplexor and Selector Channel Wiring Data".

Figure 12 shows the proper cable connection between the mother-board controller and the peripheral units.

If Punch uses fan fold bins instead of the tape reel, the "low paper" lever near the Punch reel must be secured in an upright position. Failure to do this will cause the Processor to receive a "low paper" status indication.

![](_page_38_Figure_17.jpeg)

Figure 12. Reader/Punch Mother-Board

## HIGH SPEED PAPER TAPE UNIDIRECTIONAL READER/PUNCH INTERFACE MAINTENANCE SPECIFICATION

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## HIGH SPEED PAPER TAPE UNIDIRECTIONAL READER/PUNCH INTERFACE MAINTENANCE SPECIFICATION

#### 1. INTRODUCTION

To increase Input/Output (I/O) capabilities of INTERDATA Digital Systems, a High Speed Paper Tape Reader and Punch are offered. By using these devices, paper tape handling capability and speed are increased substantially over the TTY Reader/Punch. The exact increase varies with the particular models chosen; several models of Readers and Punches are available. All models (Reader/Punch, Part Number 32-136 F01, Punch only, Part Number 32-136F02, and Reader only, Part Number 32-136F03) employ the same device controller and have the same interface requirements.

#### 2. SCOPE

This maintenance specification is provided to describe the High Speed Reader/Punch Controller in sufficient detail to allow a digital technician to maintain the system.

The following manuals will be of assistance in maintaining the system.

	Publication Number	Description
Reader	29-210	Uni-Directional Reader
Punch	29-097	Punch (215B)
	29-092	Punch Motor (295B)
	29-098	Parts List (1154B)
	29-016	Operation and Programming Manual

#### 3. BLOCK DIAGRAM

It is necessary to examine the characteristics of the Paper Tape Reader and Paper Tape Punch to fully understand data handling and control features of the Device Controller. The line circuits in the HSPTR consist of nine parallel amplifiers. See Figure 1. There are eight amplifiers for data, one channel for synchronizing from the tape feed holes.

For the HSPTP, the line circuit consists of nine solenoid drivers, plus gating to strobe the information from the Data Register to the Punch. See Figure 2. Eight of these solenoids are data channel controlled, the ninth is associated with the feed hole. All are controlled by an internal sync line from the Punch.

The interface block diagram is on Sheet 4 of Drawing 02-172D08. There are single line inputs to specify whether this a Read or Write operation, to apply power to the Punch, and to alert the Processor to a Power Off or Load condition of the Reader (Device Unavailable - DU). The Tape Reader and Punch are operated in a closed loop mode, not self stopping. All runstop controls come from the Device Controller. With the HSPTR/P Interface, it is not possible to perform a Read/Write operation off-line.

#### 4. FUNCTIONAL DESCRIPTION

This section refers to the Functional Schematic 02-172D08.

![](_page_41_Figure_0.jpeg)

![](_page_41_Figure_1.jpeg)

![](_page_41_Figure_2.jpeg)

Figure 2. HSPTP Block Diagram

#### 4.1 Addressing

Prior to receiving any commands, the HSPTR/P Device Controller must receive its address and respond properly. This is done through microsequences which first send the address on (32-136F01 - X'13', 32-136F02 - X'03', and 32-136F03 - X'03') on the Data Available Lines (DALs) (02-172D08). The DAL lines go through singleto-double rail converters and address straps which drive a decoding network. The output from this decoding network is ANDed with the inverted signal from ADRS0 to set the Address flip-flop (AD).

After a delay of approximately 200 nanoseconds, the SYN1 signal goes high. SYN1 is inverted and tested by the Processor to determine if the HSPTR/P has responded to its address. The AD flip-flop being set enables other modes of operation (e.g. Writing, Reading, Status Request, etc.) by the HSPTR/P Interface.

The standard MPX-CH Bus circuits, shown on Sheet 1, are located on the copper portion of the board. Refer to the <u>Systems Interface</u> <u>Manual</u>, Publication Number 29-003, for further details on these common circuits.

4.2 Status

The definitions of the Status and Command bits for the HSPTR/P Interface are shown in Table 1. Five Status bits are provided by the HSPTR/P Interface. The Device Unavailable (DU) bit is high when the HSPTR is in the Load Mode or AC power is off. In the HSPTP. DU becomes active in the Local Mode or when a Low Tape condition exists. The Busy bit (BSY) is reset for the HSPTR when a character is strobed into the Buffer Register. A Data Request sets BSY. BSY is high except when there is a new character in the register that has not been requested by the Processor. For the HSPTP, BSY is set when a character from the Processor enters the Buffer Register and is awaiting a strobing signal to output it to the Punch.

BSY is also set for approximately one second when power is applied to the Punch. Any time the HSPTR is not moving (RN and Feed flip-flops both reset), the No Motion (NMTN) bit is set.

The BSY, EX, DU, and EOM (End of Message - Media) bits occur in the same bit position for all Device Controllers. The HSPTR/P Interface does not use the EOM bit. The Examine Status (EX) bit is used to indicate that there are other Status conditions in the remaining four bits. When NMTN is set, EX is also set. For the HSPTR, an Overflow (OV) occurs if a new character is strobed into the Buffer Register before the last character was requested by the Processor. This will not happen in the Incremental Mode, since a new character cannot arrive until the tape is started by the DR signal that unloads the Buffer Register.

#### 4.3 Commands

Any meaningful combination of commands can be simultaneously issued to the Device Controller. The specific command or combination of commands is sent on the DAL lines, followed by the CMD0 signal on the control lines (02-172D08-1). Command enters the Controller as CMD0. This is inverted and ANDed with AD1 to produce CMG0 (Gated Command). This signal is again inverted to gate the bits from the DALs to the Command flip-flops.

Because of the dual purpose of the interface (control of either Read or Write operation), a command to specify a particular operation must be given. If a Read/Run is specified, the WT flip-flop (02-172D08-3) is reset, inhibiting a Write operation from taking place and enabling of status outputs for a Read operation. If a Write/Run operation is specified, the WT flip-flop is set, enabling the PWR flip-flop, initializing the internal power supply of the Punch, disabling the Read logic, and setting the ATN flip-flop.

Master control over tape movement for the Reader is achieved with the RN flip-flop. When set, the tape moves in a forward direction and the mode is specified by the SL (Slew) flip-flop (continuous Run Slew if set, one character command increment if reset). With the RN flip-flop reset, either mode can be established without interferring with the tape movement.

If this controller is to be allowed interrupt service, DAL bit one is set. DAL011 is ANDed with CMG1 to set the Interrupt Enable (EBL) flip-flop. Interrupts are generated by this interface when a character is strobed into the Buffer Register from the HSPTR, upon entering the Write Mode, or when a character has been output to the HSPTP and the interface is ready for more data. The interrupt condition is saved in the Attention (ATN) flipflop (Sheet 1). EBL gates a saved ATN interrupt condition onto the Processor I/O Bus as ATN0.

## TABLE 1.HIGH SPEED PAPER TAPE READER/PUNCHSTATUS AND COMMAND BYTE DATA

BIT NUMBE	ER 0	1	2	3	4	5	6	7	
STATU BYTE	s ov			NMTN	BSY	EX	· .	DU	
COMMA BYTE	ND DISABLE	ENABLE	STOP	RUN	INCR	SLEW	WRITE	READ	
BIT       READER         OV       The Overflow bit is set when the Buffer Register is loaded from the Reader before the previous character has been transferred. This condition can only happen in the SLEW Mode.						<u>PUNCH</u> The Overflow bit is always reset in the Write Mode.			
NMTN The No Motion bit is set when the Reader has been issued a STOP Command and the tape has stopped on the next character.			The No I Mode.	The No Motion bit is always reset in the Write Mode.					
BSY	The Busy bit is ty, waiting for a	set when the an output from	Buffer Regist n the Reader.	er is emp-	The Busy bit is set when the Buffer Register is full, waiting for an Unload signal from the Punch.				
EX	The Examine bi	t is set whene	ever OV = 1 o	$\mathbf{r}$ NMTN = 1.	The Examine bit is always reset in the Write Mode.				
DU	The Device Una to the Reader m is in the LOAD	vailable bit is notor is off, o position (stra	s set when the r the Reader ight up).	The Device Unavailable bit is set when the Punch is in the LOCAL state (switch is released), or a low tape condition exists on the tape reel inside the cabinet. There is no low tape sensor on the fan fold bins.					
DISABLE	This command i Controller from terrupts are que	inhibits interr 1 interrupting eued.	rupts from the the Processo	e Device r. In-	Same as	for the HSPT	R.		
ENABLE	This command p Controller to in	permits intern terrupt the Pr	rupts from the rocessor.	e Device	Same as	for the HSPT	R.		
STOP	This Command the nect charact ter to be read is the tape stops.	bit halts the m ter has been r s positioned o	notion of the t ead. The nex ver the sense	ape after st charac- lights when	This Con	nmand bit turn	ns the Punch	motor off.	
RUN	This Command the Controller i	starts the tap n the RUN Mo	e moving and de.	leaves	This bit	starts the Pun	ch motor.		
INCR	In this mode of character when and BSY = 1. T character. The Data Instruction tape moving aga	operation, the the controller he tape stops tape remains , which reset in.	e tape is adva r is in the RU after encount s stopped unti s BSY and sta	nced one N Mode ering one I a Read urts the	Not used	•			
SLEW	In this mode of a tinuously until s	operation, the topped.	e tape is adva	nced con-	Not used.	•			
WRITE					Designate	es the High Sp	eed Paper Ta	pe Punch.	
READ	Designates the H	ligh Speed Pa	per Tape Rea	der.		· · ·			

If this controller is to be denied interrupt service, DAL bit zero is set. DAL001 is ANDed with CMG1 to reset EBL. Interrupt conditions may still be saved in the ATN flip-flop, but ATN cannot be gated to the MPX-CH Bus.

The active condition on the Initialize Control Line (SCLR0) sets up preferred states by clearing all flip-flops in the Controller except DT which is set.

Whenever the Read/Write Mode changes, a partial initialize clears the ATN, BA, EBL, RN, and SL flip-flops and sets DT. The operation establishes known control states when changing between the Read and Write Modes, but may be used to clear these flip-flops without changing mode.

4.4 Read Operation

In order to effect a transfer of data from the HSPTR to the Processor, tape movement must have been initiated by a prior command from the Processor. The reading operation is then performed in the Slew or Incremental Mode according to the configuration of the Command Instruction.

In the Slew Mode of operation, the RN and SL flip-flops are set and the BSY flip-flop is set because this is its initialize state. The signal SPEED0 is active, and sets the FEED flip-flop.

The movement of tape in the Reader is detected by the HSPTR/P Interface when signal CHS1 (02-172D08-2) becomes active. This signal is derived from the photo-diode head in the Reader, which senses the feed holes in the tape and is used by the HSPTR/P Interface to initiate the reading operations. Signal CHS1 goes through a differentiator circuit and derives the STRB0 and STRB1 signals. A 0.4 microsecond STRB signal is produced whenever CHS1 goes active. The data from the eight channels of the Reader comes into the HSPTR/P Interface (CH011 through CH081) synchronously, with CH1, and is loaded into the HSPTR/P Buffer Register by the RDLD0 signal (02-172D08-2). RDLD0 is inverted producing RDLD1, which causes the Device Transmitting flip-flop (DT) to reset and BSY to go low. When BSY goes low, the ATN flip-flop is set, indicating to the Processor that a character has been read from the paper tape and is awaiting transmission to the Processor.

The Processor requests data by activating the Control Line DR0. The HSPTR/P Interface responds to the Processor's request through the derivation of DRG0 and its complement (Sheet 1). DRG0 activates the SYN1 signal after a 200 nanosecond delay. The data which has been previously gated into the HSPTR/P Buffer Register is unloaded onto the DRL bus lines by the enabling actions of DRG1 (02-172D08-2). In addition, at the end of DRG1 pulse, BSY again goes high. It should be noted here that the reset output from the DT flip-flop controls a gate that is also fed by STRB1. In the Processor's request for data was late with respect to the next character received from the Reader, OV1 would become active, giving the Processor an indication that data had been overwritten.

In the Incremental Mode, the SL flip-flop is reset and the SFEED0 is derived from the gate that is controlled by the reset side of the SL flip-flop (SL0)(02-172D08-2). When the HSPTR Interface receives the command to Run in the Incremental Mode, SFEED0 becomes active and sets the FEED flip-flop. This in turn causes the Reader to move tape. The data and Synchronizing signal ( 'HS1) comes into the HSPTR/P Interface as it did in the Slew Mode. However, when the STRB signals become active, STRB0 deactivates SFEED0 and STRB1 is now enabled through a gate to reset the FEED flip-flop which stops tape movement. As in the case of the Run Mode, BSY has become inactive and ATN set. The HSPTR will remain in this state until the Processor requests data and DRG1 is activated. At the end of DRG1, BSY and DT are set and SFEED0 is activated again to set the FEED flip-flop and allow another character to be read. Subsequent Data Requests by the Processor move the tape one character at a time in the manner just described.

#### 4.5 Write Operation

Prior to a Write operation using the HSPTP, a RUN/WRITE Command is issued by the Processor. This command causes the WRT and PWR flip-flops to set (02-172D08-3). With PWR1 active, the AC Relay Driver (27-007-3) activates the Power Supply of the HSPTP. As soon as the HSPTP Power Supply is activated, VCK0 becomes active, initiating a one second delay circuit. This delay raises BSY to inhibit a Write operation from taking place while the Punch mechanism comes up to speed. At the end of the one second delay, BSY1 is inactive, an interrupt is generated, and the HSPTP is ready for use.

(Note that when the PWR flip-flop is cleared, the one second timer is recycled and ready for use within ten milliseconds).

The Processor transfers data from the DAL lines to the HSPTP by activating the DA0 control line. DA0 is inverted in the HSPTR/P Interface and used to derive the signal DAG0. Approximately 200 nanoseconds after DAG0 goes high, SYN1 goes high. SYN1 is inverted and send to the Processor to indicate that the HSPTR/P Interface received the information sent. At this time, BSY1 is inactive due to either initialization, or completion of a previous Write or Read operation by the HSPTR/P Interface. DAG0 is inverted and ANDed with the reset output from the Buffer Available (BA) flip-flop generating the signal GDAG0 (02-172D08-2), GDAG0 is inverted (02-172D08-2) and gates the information into the Buffer Register. At the same time GDAG0 is used to toggle the BA flip-flop, indicating that a byte of data is waiting to be output to the Punch. BA1 is then ANDed with WT1 causing BSY to go high, and preventing further information to be sent by the Processor.

An internal Sync signal generated by the HSPTP is sent through a wave shaping circuit (27-007-3) producing the 1.0 millisecond signal, PSYN0. When the Punch is ready to receive information, PSYN0 goes low. PSYN0 is inverted in the HSPTR/P Interface and ANDed with BA1 (02-172D08-2).

This output goes to the Timer (TM) flip-flop, causing TM0 to become active. The output, TM0, then goes to a 4.5 millisecond delay, producing the gating control signals GP0, GPOA, and GP1. GP0A controls the output gating from the Buffer Register producing the signals PNCH011 through PNCH081.

PHCH011 through PNCH081 are fed into eight solenoid drivers (27-007-1, 2) which activates the eight punches of the data channels. A PNCH signal going high, causes the solenoid driver to create a ground on the Punch, activating the Punch solenoid to produce a hold in the tape. The tape feed solenoid is controlled separately by the signal GP1 and is activated at each character output. The GP0 signal is fed back to the trigger of the BA flip-flop causing it to reset. With BA1 inactive, BSY1 becomes inactive and the HPSTR/P Interface is now ready to receive another byte of data from the Processor.

#### 5. MAINTENANCE

The High Speed Reader/Punch Controller requires no periodic maintenance. The Reader and Punch requires periodic maintenance such as cleaning and lubrication. For a procedure and the maintenance requirements, refer to the operating and service manual.

Unidirectional Reader	29-210	Model 2540/2540B
Punch	29-097	Model 215B
Punch Parts	29-098	Model 1154B
Motor	29-092	295B

Performance tests of the system can be made on the system by using the diagnostic programs 06-016 and 06-037. The diagnostic programs will assist in troubleshooting the controller.

- 6. TIMING DIAGRAM
- The timing for the two operating modes of the Controller is shown in Figures 3 and 4.

![](_page_45_Figure_10.jpeg)

![](_page_45_Figure_11.jpeg)

![](_page_45_Figure_12.jpeg)

Figure 4. Reader/Punch Timing Read Mode

#### 7. MNEMONICS

The following list provides a brief description of each mnemonic found in the HSPTR/P Device Controller. The source on 02-172D08 and 27-007F01B08 of each signal is also provided. Unless otherwise indicated, source is on 02-172D08.

MNEMONIC	MEANING		LOCATION
AD	Address flip-flop		1.J.2
ADRS	Address		1A5
AGOX	Address Gate Inputs		1F1-1F4
ATN	Attention flip-flop		1 H9
ATSYN	Attention Sync		1K8
ВА	Buffer Active flip-flop		3R3
BROX	Buffer Register Output		2G3-2G7
BSY	Busy		3D8
CAGND	Cable Ground	<b>27-007F01B08</b>	3M2
CHMD	Change Mode	· · · · · ·	3D7
CHOX1	Reader Data Channels		2A2-2A6
CHS1	Channel Sync		2A2
CMD	Command		1D6
CMDRST	Command Reset		3G7
СМС	Command Gated		1D6
DA1	Data Available		1E6
DAG0	Gated Data Available		1E6
DALOX	Data Available Lines		1D1-1D5
DR1	Data Request		1E7
DRG0	Gated Data Request		1E7
DRLOX	Data Request Lines		181-184
DT	Device Transmit flip-flop		<b>2K</b> 9
DU	Device Unavailable		388
DUP1	Data Available Punch	27-007F01B08	3B9
DUR0	Device Unable		2A2
DUR1	Inverusion of Duro		2K1
DUN0	Run Flip-Flop		2N6
DVCK0	Delay - Voltage Check		3L8

	himble		301
FEED	Tape Feed flip-flop	· ·	2R5
FEED	Feed Coil	27-007F01B08	3M1
FWD1	Forward Control Line		27٨
GDAG	Gate Data Available		3 L 3
GND	Ground	27-007F01B08	3B6
GP	Gate to Punch		3 <b>S</b> 2
GP1	Gate to Punch	27-007F01B08	3B3
LD	Load Data		2 D9
NMTN	No Motion Tape		3C9
OV	Overflow flip-flop		2R3
PNCH0X1	Output to Punch		2J3-2
PNCH011 through PNCH041	Input To Punch	<b>27-007F01B08</b>	1B3 throu 1B8
PNCH051 .hrough PNCH081	Input To Punch	27-007F01B08	2B3 throu 2B8
PO10 through PO40	Punch Output	<b>27-007F01B08</b>	1M2 throuş 1M8
PO50 through PO80	Punch Output	<b>27-007F01B08</b>	2M2 throug 2M8
PSYN0	Punch Sync	<b>27-007F01B08</b>	3B5
PSYN0	Punch Sync		3F1
PWR	Punch Power flip-flop		3E6
PWR1A	Punch Power	27-007F01B08	3B7
RACK0	Received Acknowledged		1A8
REV1	Reverse Control Line		258
RDLD	Read Data Load Data		· 2E9
RMT	Remote	27-007F01B08	<b>3M</b> 8
RN	Run flip-flop		3C2
SATN0	Set ATN flip-flop		1G9
SCLR0	System Clear - Initialize		1G5

MNEMONIC	MEANING		LOCATION
SL	Slew flip-flop		3C3
SR0	Status Request		1A6
SRG	Gated Status Request		1 D6
STOPI	Stop Control Line		287
STRB	Strobe		2J2
ТАСК	Transmit Acknowledge		1E9
TCA	Timer Coil High	27-007F01B08	3M6
TCG	Timer Coil Ground	27-007F01B08	<b>3</b> M6
ТМ	Punch Timer flip-flop		3K1
WT	Write/Read flip-flop		3C4
VCK0	Voltage Check of Negative 28 Volts from Punch.		3G7
VCK0	Voltage Check of Negative 28 Volts from Punch.	<b>27-007F01B08</b>	3B4
XRP	Device Controller common pullup resistor. Ties unused gate input to positive 5 volts through a 1 kilohm resistor.		2A9

![](_page_49_Figure_0.jpeg)

![](_page_50_Figure_0.jpeg)

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![](_page_51_Figure_0.jpeg)

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![](_page_52_Figure_0.jpeg)

![](_page_53_Figure_0.jpeg)

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![](_page_54_Figure_0.jpeg)

![](_page_55_Figure_0.jpeg)

![](_page_56_Figure_0.jpeg)