



# **selector channel manual**



**GRI Computer Corporation**

320 NEEDHAM STREET, NEWTON, MASSACHUSETTS 02164

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GRI-909  
SELECTOR CHANNEL MANUAL

GRI Computer Corporation, 320 Needham Street, Newton, Massachusetts 02164

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CHAPTER ONE  
DESCRIPTION

1.1 Description:

The Selector Channel is a digital interface processor option useable with any GRI computer. It consists of a set of three PC boards known as Selector I, II, and III. Its function is to provide a DMA path for high speed, word oriented block transfer devices such as drums, discs and A to D converters.

Here is a summary of the basic features of the Selector Channel:

- .Sixteen bit entry and exit ports
- .Integral word count register
- .Integral core memory address register
- .Four function control lines
- .Interrupt and function sense lines

These features provide the following capabilities:

- .Monitors the number of memory accesses granted; signals end of last word transfer
- .Automatically tracks next core location that will be used
- .Device controller steers control words on data-out lines to proper registers in controller
- .Control flags provided

The DMA system of all GRI Computers provides a high speed, direct channel in and out of the main memory. One data word can

be transferred every 1.76us. Access is granted by the control program unit of the processor whenever a request appears on the DMRL (direct memory request bus) of the processor and the current instruction has been completed. Servicing of a DMA request has top priority over the other special access channels (external instruction and priority interrupt) to the computer. Priority of service among several devices connected to the DMA system is decided by the relative position of the device operator cards (selector channel cards) along the bus. Priority is established from left to right as viewed from the rear of the processor looking at the IO bus board. Under normal circumstances (no more than one DMA device active at a time), a DMA request will be granted within 8.8 usec (5 cycles) of the appearance of a DMRL signal on the processor bus. This time will be extended by one cycle (1.76us) for every DMA device of higher priority that has a request on the bus simultaneously (assuming that none of these devices can utilize 100% of the memory time). Once granted access, a device may have every consecutive memory cycle if it can supply data at the rate of a new word every 1.76us.

## 1.2 Description of Selector Channel Functions:

### 1.2.1 Word Count (WCT)

This register, connected between the computer's buses, may be manipulated by any applicable machine instruction (i.e. loaded, stored, incremented, complemented) other than shifting. The word count register is loaded with a two's complement number -n where n = number of data words to be transferred over the chan-

nel. The 16th bit of the register provides an end of transfer signal to the controller when the word count runs out. Every time a DMA cycle is granted to the device controller, the WCT register is incremented by one in preparation for the next cycle.

#### 1.2.2 Core Address (CAR)

The Core Address Register is a 16 bit register which is connected between the computer's buses and may be manipulated by any applicable machine instructions other than shifting. The CAR is loaded with the starting memory address of the block of words to be transferred in or out of the computer memory. It furnishes no information to the controller. Once the address is retrieved from the CAR, it is incremented in preparation for the next cycle.

#### 1.2.3 Function Register (FR)

A 4 bit register which is loaded from the CB bits in the processor during an FO (function output) instruction. This register provides four lines that may be used by the controller to steer 16 bit data words to various control registers in the controller. These lines may be used as unary lines (one out of every four) or decoded into all 16 combinations for control purposes in the controller until they are changed by the program issuing another FO instruction to the channel.

#### 1.2.4 Data Output Register (DOR)

A 16 bit register that is connected as a destination of data only. It may be loaded by any register reference instruction or by the DMA control logic during a data out transfer from memory.



This register is a general communications register for the controller. By using the function register, data on these lines may be steered to different registers in the controller. During the DMA cycles granted to the device, this register will carry data that has been read from memory. A strobe is also provided with this register after the data lines have stabilized.

#### 1.2.5 Function Sense Lines

A set of three lines is provided for connection of various controller flags such as error conditions, power failure, operability, etc. These lines may be sensed by the processor via an SF (sense function) instruction. The programmer may also test for the negative state of these lines so the designer should choose the affirmative state for connection to these lines (e.g. Power Fail should be connected to a sense line so that the programmer may test for power failure or NO power failure).

#### 1.2.6 Data Input Register (DIR)

A 16 bit set of input lines connected as a source of data only over which DMA data words may be transferred into the processor. These lines may also be used to access the contents of various control registers in the controller. By using the function register as a selector code, the controller's registers may be accessed under program control, e.g. status words may be read back by the programmer by selecting the register via an FO instruction and then issuing a register reference instruction.

#### 1.2.7 Miscellaneous Control Lines

Several lines are provided in the channel for generating in-

interrupts, establishing the direction of data transfer, and generating transfer requests.

#### 1.2.8 Selector Channel Signals

All signals are logic "0" for assertion where a "0" = 0 to 0.4v and a "1" = 2.4 to 5.25 volts.

CHAPTER TWO  
OPERATION

2.1 Channel Operation

2.1.1 Initiate Operation (Without bulk storage)

The channel is normally initiated by a stream of programmed setup commands to both the channel logic and the controller connected to the channel.

The word count (WCT) and core address registers (CAR) are set up by instructions such as %RASX language.

MRI -N, WCT

MR SA, CAR

Only the channel logic uses these instructions. The external controller itself will be inert during these transactions.

2.1.2 Initiate Operation (With bulk storage)

An address for search logic is required by bulk storage devices. Let us assume there are three such address registers in the device controller, called C0, C1, and C2 respectively. The controller also requires some kind of a control word to initiate its operation and mode. Let us assume there is one such register, C3, four such controllers are to be bussed to the same channel D0, D1, D2, and D3. The function register will be assigned the following decoded significance:

FR	3 2 1 0		CB code in FO instruction
	X X 0 1	-C0	X X 0 0
	X X 0 1	-C1	X X 0 1
	X X 1 0	-C2	X X 1 0
	X X 1 1	-C3	X X 1 1
	0 0 X X	-D0	0 0 X X
	0 1 X X	-D1	0 1 X X
	1 0 X X	-D2	1 0 X X
	2 2 X X	-D3	1 1 X X

A program to initialize and start Device Controller 1 is as follows:

D1 C0	TO	CHANNEL
WORD1	TO	CHANNEL
D1 C1	TO	CHANNEL
WORD2	TO	CHANNEL
D1 C2	TO	CHANNEL
WORD3	TO	CHANNEL
D1 C3	TO	CHANNEL
MR	STATUS	CHANNEL ; also provides start signal

The timing for the channel lines involved in these transactions is shown in Figure 1, Appendix A.

The programmer may wish to examine the status register of D0 before activating the controller. Assuming that an all 0 status word meant everything is OK, the following program might be used:

```
FO D0 C3, CHANNEL; gate status word into DIR lines
JC CHANNEL, NEZ, ALARM; NOT equal to zero
```

The timing for this operation is as shown in Figure 2, Appendix A.

The data on the input lines must be stable within 1.3 $\mu$ s of the issuance of the FR code.

NOTE: Judicious use of DIR15 will allow the programmer to test the word on the DIR lines for things like:

LTZ - BIT 15 = 1

GTZ - BIT 15 = 0 and BITS 14-0  $\neq$  0

GEZ - BIT 15 = 0 or BITS 15-0 = 0

LEZ - BIT 15 = 1 or BITS 15-0 = 0

### 2.1.3 Post Start-up Considerations

Once the device has been started, it is now free to generate transfer requests according to the timing in Figure 3, Appendix A.

To maintain consecutive memory cycles, the XFRG line may be held low by the controller, or simply returned to ground within 500ns of the ACK for the previous request as shown in Figure 4.

### 2.1.4 Sense Lines

The three sense lines SEN1,2,3 are provided for special error or status flags. There are no special timing requirements for these lines other than the general guideline that the program should be able to clear these conditions by loading a status register or initializing a new transfer. These lines may be sensed by a function instruction:

SF DIR,2

SF DIR, NOT 4

### 2.1.5 Interrupt Line

The interrupt line INT is provided for interrupt notification of special conditions such as parity error, data service late, etc. This interrupt is distinct from the interrupt that occurs when the WCT register has incremented to 0, indicating end of block transfer. This latter interrupt is internally generated in the channel logic and causes a distinct interrupt which differs from the one caused by

INT. The INT signal should be removed by loading a status register in the controller or starting a new transfer, etc. The flags for these interrupts may be sensed by a sense function instruction. Both interrupts have the same interrupt address.

#### 2.1.6 CLR Line

The CLR line is provided for initiating controllers. The line is pulled low when power is going down, coming up, or the START key on the console is depressed. It is often used as a master clear signal by controllers.

#### 2.1.7 EOT Line

The EOT line will be pulled low during the last transfer. It occurs within 400 ns of the ACK signal and will remain there until the programmer loads the word count register with a new count.

CHAPTER THREE  
THEORY OF OPERATION

3.1 General

The basic functions of the three selector channel I/O cards is as follows: Selector I contains the word count register, the interrupt service block, and the DM service block; Selector II contains the core address register, the data input register, and the sense function logic; and Selector III contains the data output register and the function register.

3.2 Selector I

3.2.1 WCT

The word count register is a 16 bit register loaded with the twos compliment of the number of words to be transferred. This is accomplished by a register reference instruction (ie. register to register or memory to register). At the start of each DM transfer, the register is incremented in preparation for the next transfer. When the register overflows an interrupt request will be generated (if interrupt is enabled and the EOT option is selected). The source and destination device address for the WCT register is 66 (octal).

3.2.2 INT Service Block (Refer to the System Reference Manual for the GRI computer you are utilizing for operation of interrupt.)

There are two interrupt modes on the selector channel:

- a. EOT (End of Transfer)
- b. INT (Interrupt Request from External Device)

The EOT ready flag is optional via the staple on J1 pin 11. If used the flag sets on WCT overflow.

The INT device ready flag is set from the external device

via F2 pin 3. The interrupt address for the selector channel is 60 (octal). Bit 14 is the interrupt status register bit.

3.2.3 DM Service Block (Refer to the System Reference Manuals for the GRI computer you are utilizing for operation of direct memory access.)

A DM request on the selector channel is made via XFRQL on D2 pin 3 from the external device. As long as this signal is low, the selector channel will hold the DM. If it is high when BISYNH is generated, the DM request will be released.

DIRC on D2 pin 9 also comes from the external device and determines the direction of word transfers. If DIRC is low word transfer is into core memory and if high word transfer is from core memory. ACKL informs the external device that its request has been acknowledged.

### 3.3 Selector II

#### 3.3.1 CAR

The core address register is loaded with the starting core address of the block of words to be transferred in or out of the computer's memory. The logic signal EASH interrogates the CAR at the start of each DM cycle. The CAR is incremented at P2 time of each DM cycle in preparation for the next cycle. The source and destination device address for the CAR is 67 (octal).

#### 3.3.2 DIR

The data input register is a 16 bit register used for the transfer of DM words into core memory. In conjunction with the the function register it may also be used to access the contents



of various control registers in the external device. EDSH is the logic signal that interrogates the DIR if DM transfer is into core. The DIR may also be accessed only as a source of data via a register reference instruction. The system device address is 40 (octal).

### 3.3.3 Sense Function

The three sense function lines are available to the external device for various flags. These lines may be sensed by the processor via an SF (sense function instruction). The source operator is 40 (octal).

## 3.4 Selector III

### 3.4.1 DOR

The data output register is a 16 bit register used for the transfer of DM words from core memory. It is also used in conjunction with the function register and a register reference instruction to steer control words (i.e. status word, starting sector, etc.) to the external device it therefore can only be a destination of data. EDDH is the logic signal along with DSTRH and SERV that loads the DM word from core into the DOR. DDAH and DSTRH load the DOR on register reference instructions. In both cases a 500 nsec pulse is generated to the external device 270 nsec after the word has been loaded into the DOR. The destination device address is 40 (octal).

### 3.4.2 FR

The function register is a 4 bit register loaded via an FO (function output) instruction. The FR selected is a function of the CB bits. The FR is used in conjunction with the DIR and

DOR to access various control registers and to send various control words to and from the external device. The destination operator is 40 (octal).

3.4.3 Timing (Refer to Figures 1 through 5 in Appendix A.)

3.4.4 Instruction Summary

SDA & DDA = 66	For Word Count Register
SDA & DDA = 67	For Core Address Register
SDA = 40	For Data Input Register
DDA = 40	For Data Output Register

Interrupt Address = 60

Sense end of transfer flag            66 0010 02

Sense external interrupt flag        66 0100 02

Clear end of transfer flag            02 0100 66

Clear external interrupt flag        02 0010 66

Interrupt Status Register = Bit 14 (i.e. 040000)

Function Register

- a) 02 0001 40            Generate FR00
- b) 02 0010 40            Generate FR01
- c) 02 0100 40            Generate FR02
- d) 02 1000 40            Generate FR03

Sense Function

- a) 40 0010 02            Sense Line 1
- b) 40 0100 02            Sense Line 2
- c) 40 1000 02            Sense Line 3

3.4.5

Glossary

<u>Name</u>	<u>DIR</u>	<u>Function</u>
DORO-15L	OUT	Data out lines for control words or DMA words.
DIRO-15L	IN	Data in lines for control words or DMA words.
FRO-3L	OUT	Function control lines used to steer control words off of DOR lines or onto DIR lines.
STROBEL	OUT	Used to strobe DOR lines into selected controller registers.
XFRQL	IN	A transfer request used to gain a DMA service cycle from the processor.
ACKL	OUT	Acknowledgement of the transfer request. Will be given when the DMA cycle is actually granted to the channel.
SEN1-3L	IN	Sense lines for up to three error conditions that may require special program attention.
DIRC	IN	Direction of transfer: Into memory = Low Out of memory = High
INTL	IN	A single interrupt line normally used to signal the processor via the interrupt system that an interrupt is being requested from the device.
CLRL	OUT	A master clear signal that occurs when processor power is going down, coming up, or when the START key is depressed.
EOTL	OUT	Indicates end of transfer.

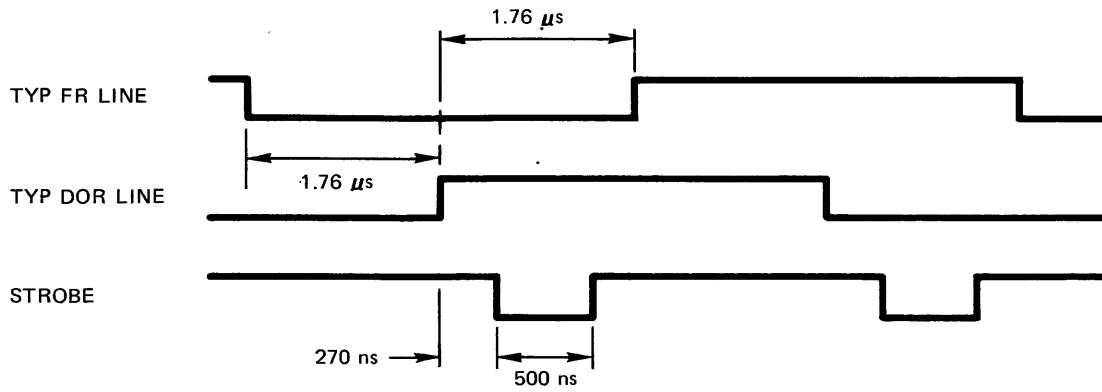


FIGURE 1

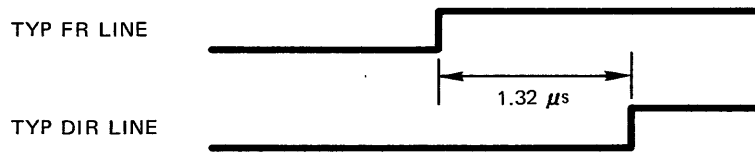


FIGURE 2

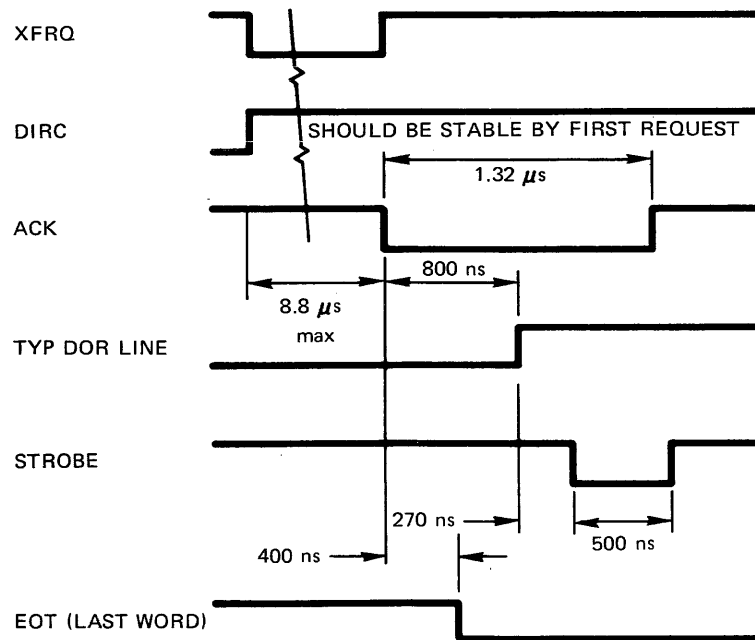
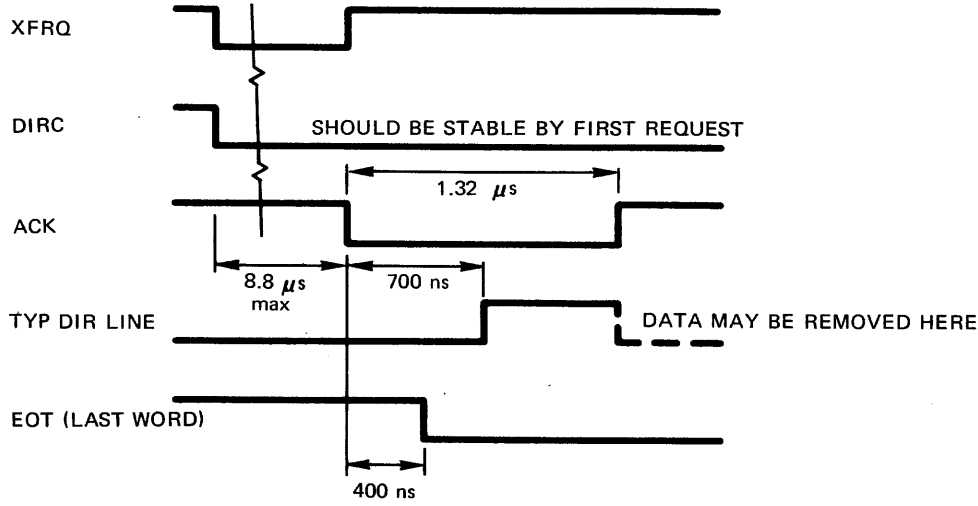
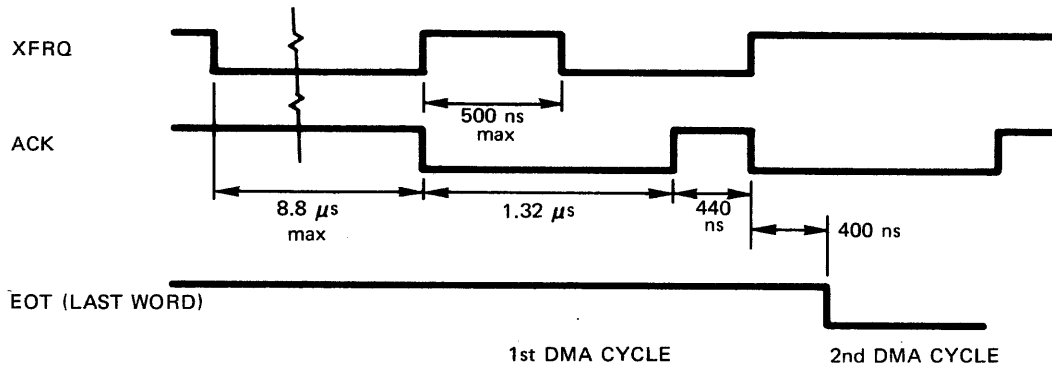


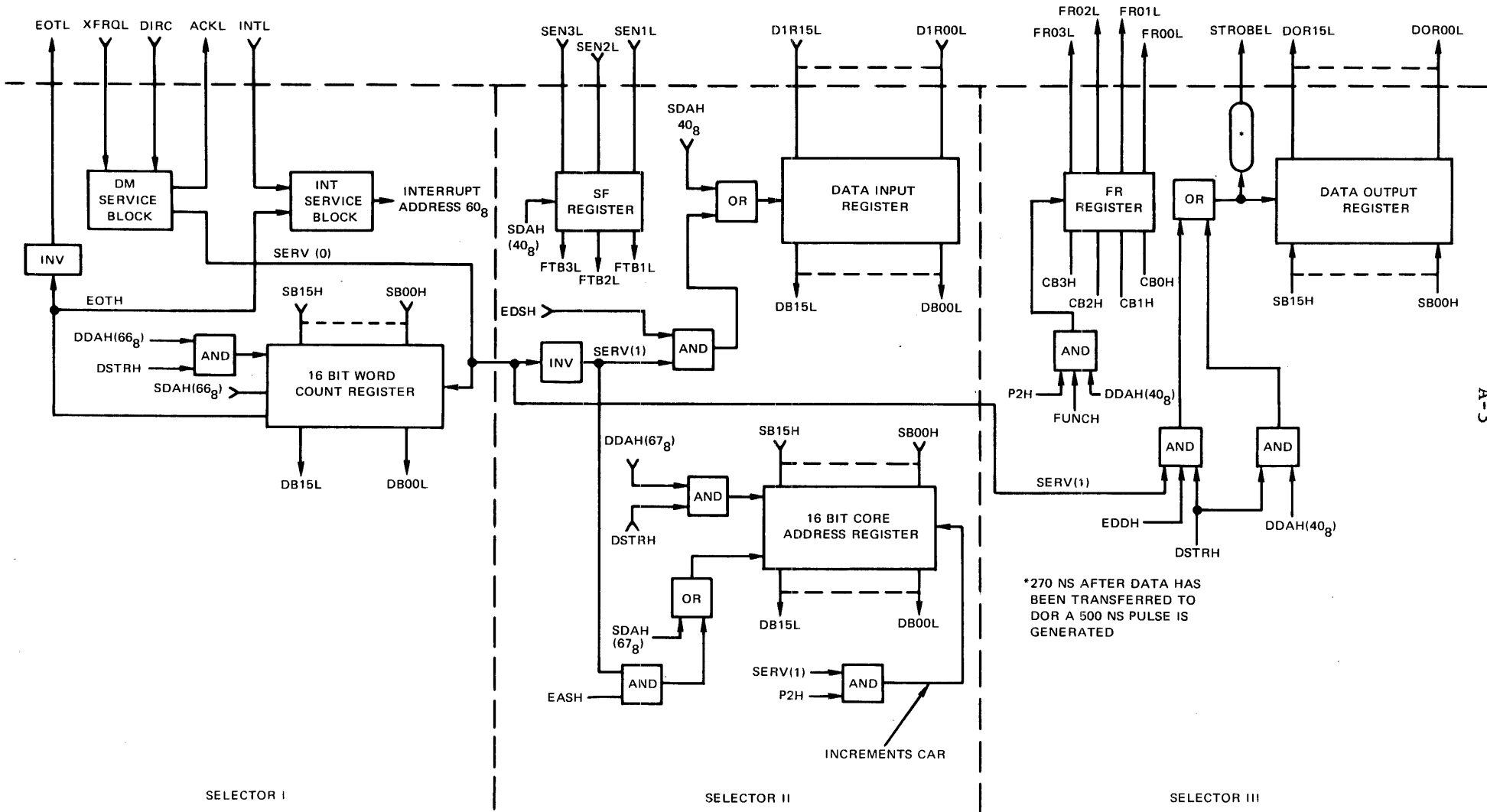
FIGURE 3  
DATA TRANSFERS OUT



DATA TRANSFERS IN  
FIGURE 4



CONSECUTIVE DMA CYCLES  
FIGURE 5



SELECTOR CHANNEL BLOCK DIAGRAM

SELECTOR CHANNEL EXTERNAL PIN ASSIGNMENT

I) SELECTOR CHANNEL I

<u>PIN</u>	<u>NAME</u>	<u>FUNCTION</u>
EA	CLRL(B)	MASTER CLEAR
EB	DEV SERV (0)	DEVICE IS IN SERVICE
EC	DIRC	DETERMINES DATA IN/OUT
ED	XFROL	REQUEST TRANSFER
EE		KEY
EF	ACKL	ACKNOWLEDGE TRANSFER REQUEST
EH - EZ	GROUND	GROUND
Ea	INTL	DEVICE INTERRUPT REQUEST
Eb	GROUND	GROUND
Ec	EOTL	WORD COUNT OVERFLOW
E1 - E25	GROUND	GROUND

## II) SELECTOR CHANNEL II

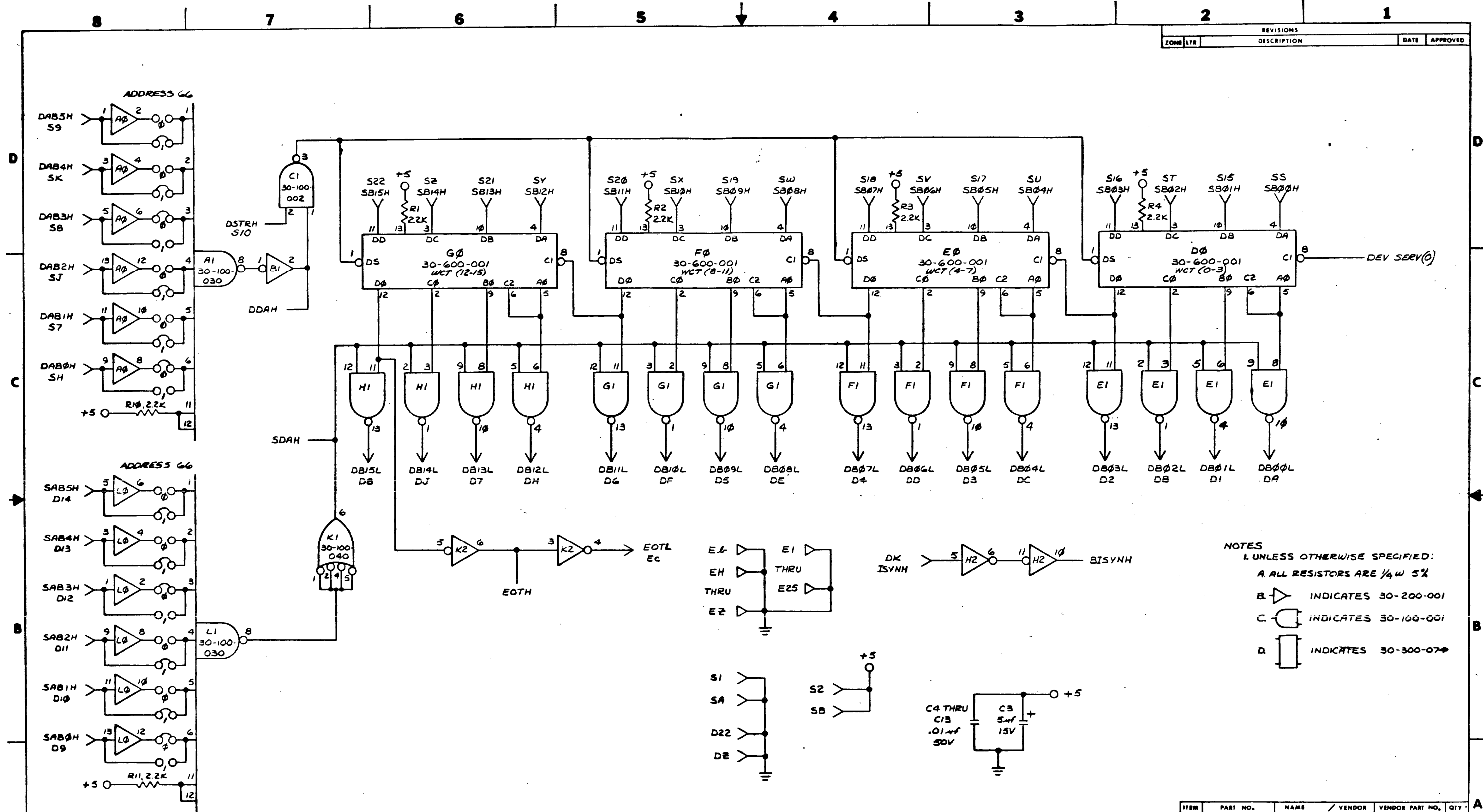
PIN	NAME	FUNCTION
E1, E3, -E25	GROUND	GROUND
EA, Ea, Eb, Ec	GROUND	GROUND
EB	DEV SERV (0)	DEVICE IS IN SERVICE
EC	D2R00L	DATA INPUT BIT 0
ED	D2R01L	DATA INPUT BIT 1
EE		KEY
EF	D1R02L	DATA INPUT BIT 2
EH	D1R03L	" " " "
EJ	D1R04L	" " " "
EK	D1R05L	" " " "
EL	D1R06L	" " " "
EM	D1R07L	" " " "
EN	D1R08L	" " " "
EP	D1R09L	" " " "
ER	D1R10L	" " " "
ES	D1R11L	" " " "
ET	D1R12L	" " " "
EU	D1R13L	" " " "
EV	D1R14L	" " " "
EW	D1R15L	DATA INPUT BIT 15
EX	SEN1L	SENSE LINE 1
EY	SEN2L	SENSE LINE 2
EZ	SEN3L	SENSE LINE 3



III) SELECTOR CHANNEL III

PIN	NAME	FUNCTION
EA	DOR00L	DATA OUTPUT BIT 0
EB	DEV SERV (0)	DEVICE IS IN SERVICE
EC	DOR01L	DATA OUTPUT BIT 1
ED	DOR02L	DATA OUTPUT BIT 2
EE		KEY
EF	DOR03L	DATA OUTPUT BIT 3
EH	DOR04L	" " " "
EJ	DOR05L	" " " "
EK	DOR06L	" " " "
EL	DOR07L	" " " "
EM	DOR08L	" " " "
EN	DOR09L	" " " "
EP	DOR10L	" " " "
ER	DOR11L	" " " "
ES	DOR12L	" " " "
ET	DOR13L	" " " "
EU	DOR14L	" " " "
EV	DOR15L	DATA OUTPUT BIT 15
EW	FRO0L	FUNCTION CONTROL BIT 0
EX	FRO1L	FUNCTION CONTROL BIT 1
EY	FRO2L	FUNCTION CONTROL BIT 2
EZ	FRO3L	FUNCTION CONTROL BIT 3
Ea	STROBEL	DATA STROBE FOR DOR LINES
Eb	GROUND	GROUND
Ec	GROUND	GROUND
E1-E25	GROUND	GROUND

REVISIONS		DATE	APPROVED
ZONE	LTR	DESCRIPTION	

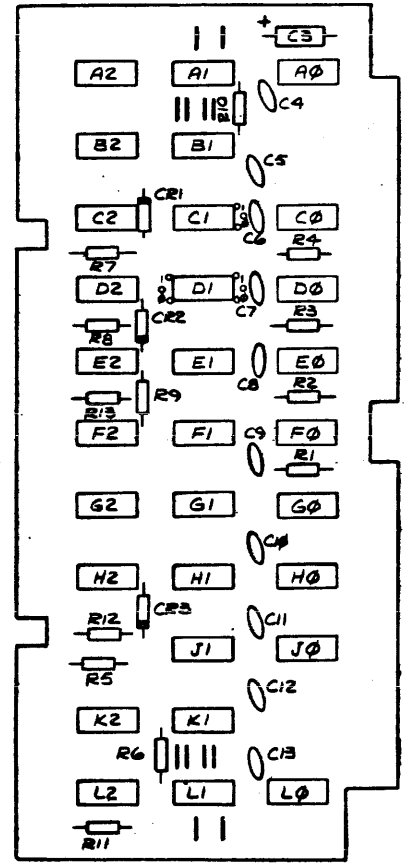
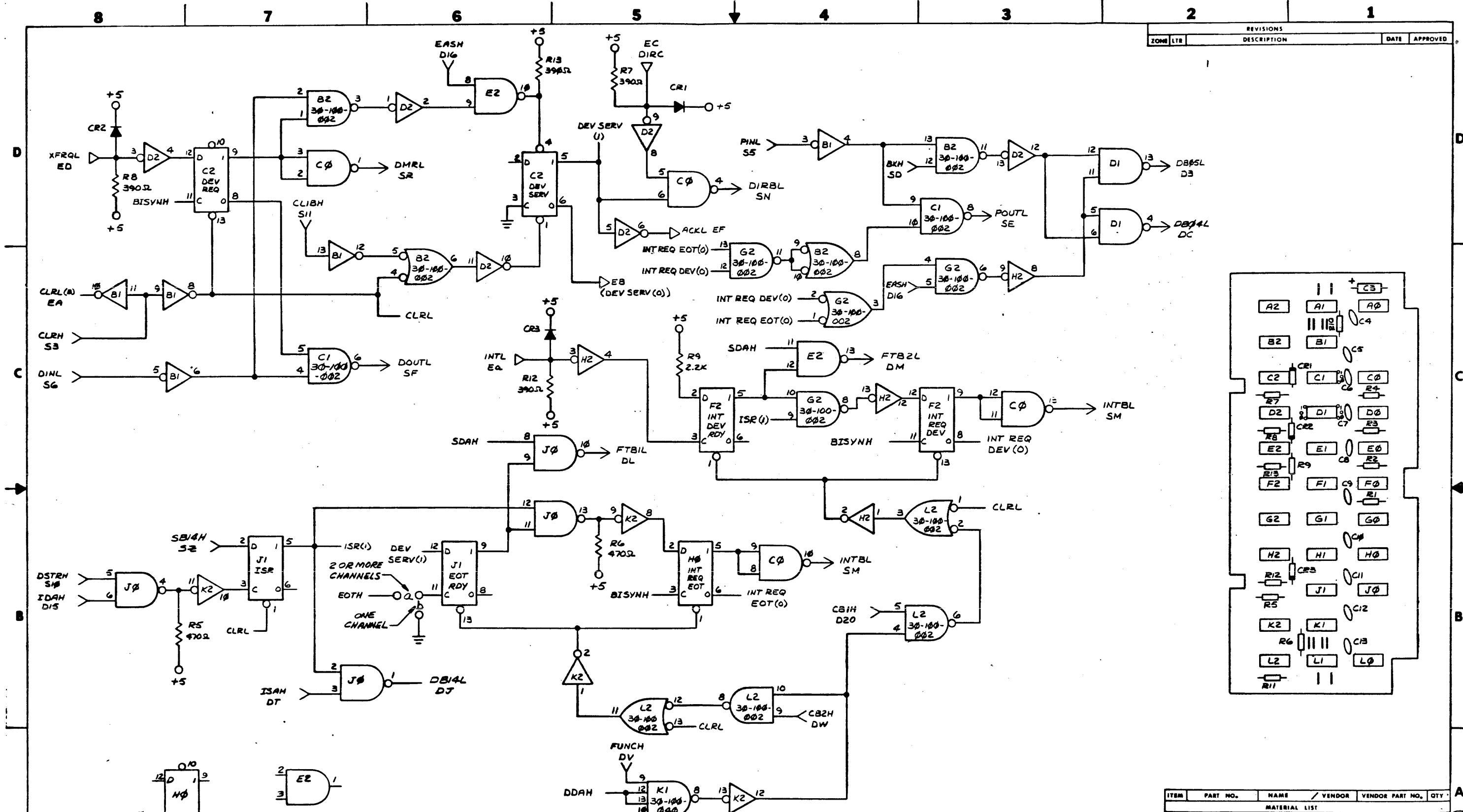


- NOTES**  
 1. UNLESS OTHERWISE SPECIFIED:  
 A. ALL RESISTORS ARE 1/4W 5%  
 B. INDICATES 30-200-001  
 C. INDICATES 30-100-001  
 D. INDICATES 30-300-07

ITEM	PART NO.	NAME / VENDOR	VENDOR PART NO.	QTY
MATERIAL LIST				
REF B.M				
UNLESS OTHERWISE SPECIFIED - DIMENSIONS ARE IN INCHES - TOLERANCES ON FRACTIONS ± 1/64 DECIMALS .X ± .03, .XX ± .01, .XXX ± .005 ANGLES ± 1/2°, BENDS 90° FABRICATE PER SPEC 89-002-000		CONTRACT AUTHENTICATION	DATE	
		DRN	GTD	11/14/77
		CHK		
		REVIEW		
		ENGR	Pa	2/23/72
		APPD	HarLi	2/23/72
MATERIAL -				
APPEARANCE -				
FINISH -				
NEXT ASST	REF SPEC'S			
APPLICATION				
GRI Computer Corp. NEWTON, MASS.		SELECTOR CHANNEL I LOGIC DIAGRAM		
SIZE	CODE IDENT NO.	DRAWING NO.		
D	11842	17-049-016-A		
SCALE	UNIT WT	SHEET 1 OF 2		

SYM	DESCRIPTION
	MOLE LEGEND

REVISIONS		DATE	APPROVED
ZONE	LTB	DESCRIPTION	
1			

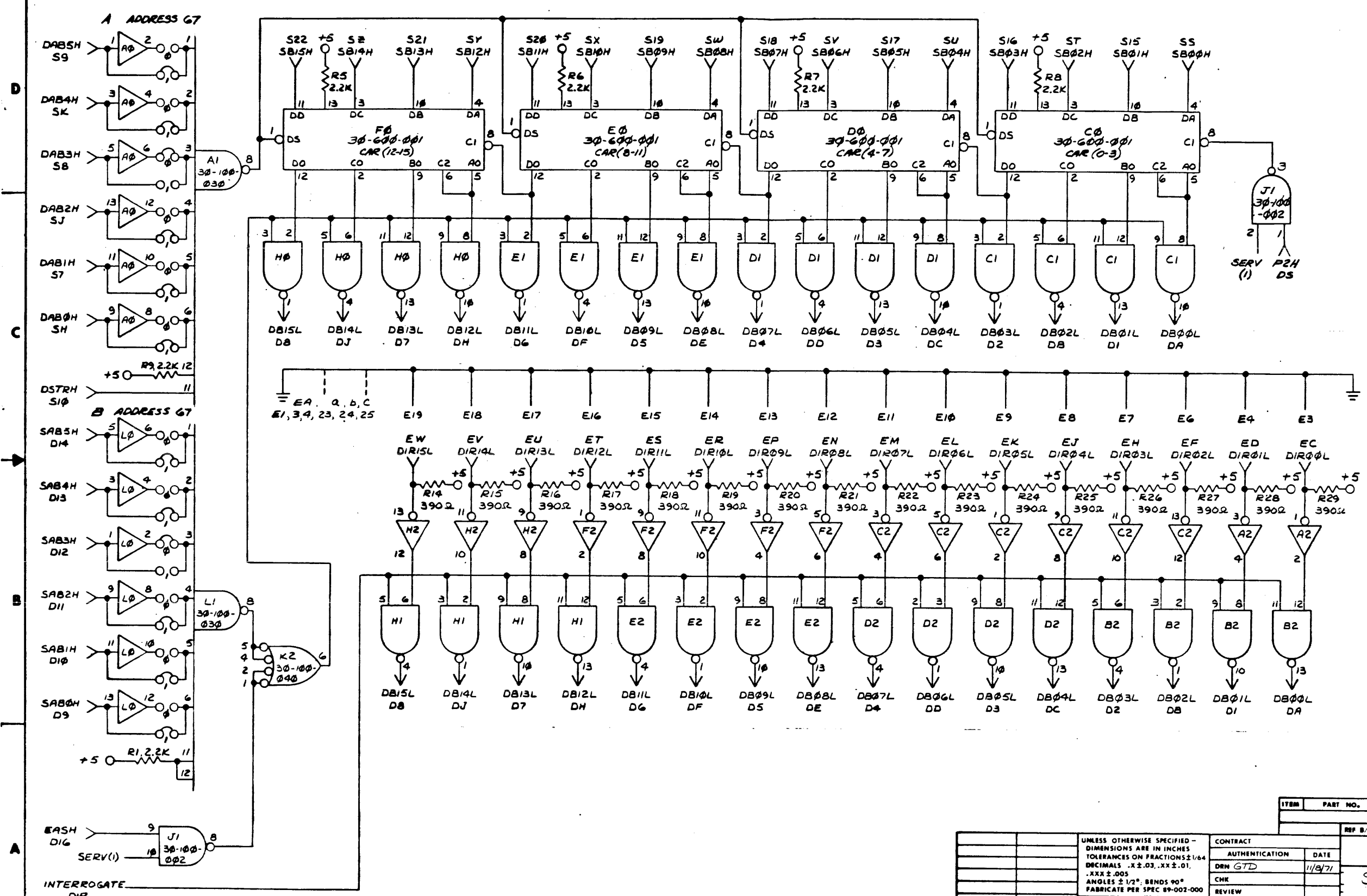


ITEM	PART NO.	NAME / VENDOR	VENDOR PART NO.	QTY
MATERIAL LIST				
REF B/M				
 <b>SELECTOR CHANNEL I</b> <b>LOGIC DIAGRAM</b>				
SIZE	CODE IDENT NO.	DRAWING NO.		
D	11842	17-049-016-A		
SCALE	UNIT WT	SHEET 2 OF 2		

UNLESS OTHERWISE SPECIFIED - DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS ± 1/64 DECIMALS .X ± .03, .XX ± .01, .XXX ± .005 ANGLES ± 1/2°, BENDS 90° FABRICATE PER SPEC 89-002-000		CONTRACT AUTHENTICATION	DATE
MATERIAL -		DRN GTD	11/16/71
APPEARANCE -		CHK	
FINISH -		REVIEW	
APPLICATION		ENGR (TJ)	2/2/72
NEXT ASSY		APPD	
REF SPEC'S			

SYM	DESCRIPTION	QTY
HOLE LEGEND		

REVISIONS		DATE	APPROVED
ZONE	LTR		



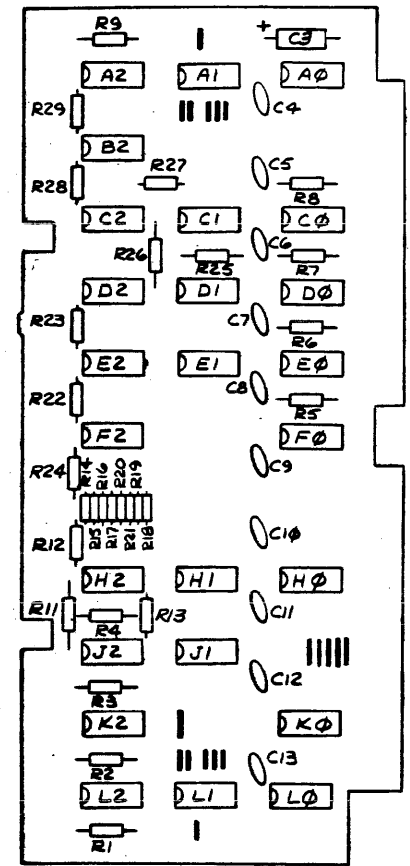
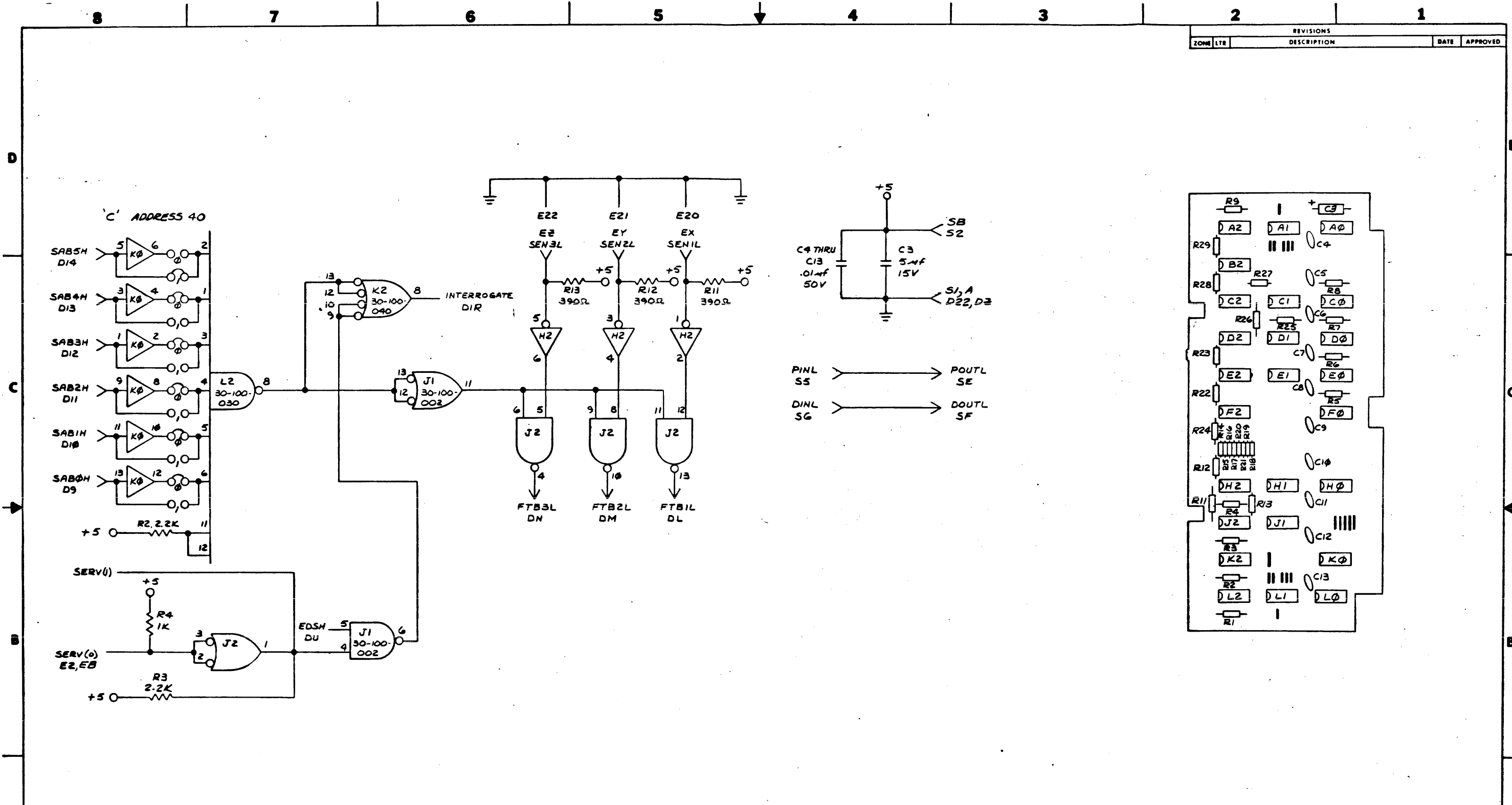
NOTES:  
 1. UNLESS OTHERWISE SPECIFIED:  
 A. ALL RESISTORS ARE 1/4W, 5%  
 B. INDICATES 30-200-001  
 C. INDICATES 30-100-001

ITEM	PART NO.	NAME	VENDOR	VENDOR PART NO.	QTY.
MATERIAL LIST					
REF B/M					

UNLESS OTHERWISE SPECIFIED - DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS ± 1/64 DECIMALS .XX ± .01 .XXX ± .005 ANGLES ± 1/2°; BENDS 90° FABRICATE PER SPEC 89-002-000		CONTRACT AUTHENTICATION DATE		GRI Computer Corp. NEWTON, MASS.
		DRN GTD	11/8/71	
MATERIAL -		CHK		SELECTOR CHANNEL II LOGIC DIAGRAM SF, DIR & CAR
APPEARANCE -		REVIEW		
FINISH -		ENGR Rq	2/2/72	SIZE CODE IDENT NO. DRAWING NO. D 11842 17-040-017-A
NEXT ASSY REF SPEC'S		APPD JOR K	2/2/72	
APPLICATION				SCALE UNIT WT SHEET 1 OF 2

SYM	DESCRIPTION	QTY
	HOLE LEGEND	

REVISIONS		DATE	APPROVED
ZONE	LTR	DESCRIPTION	

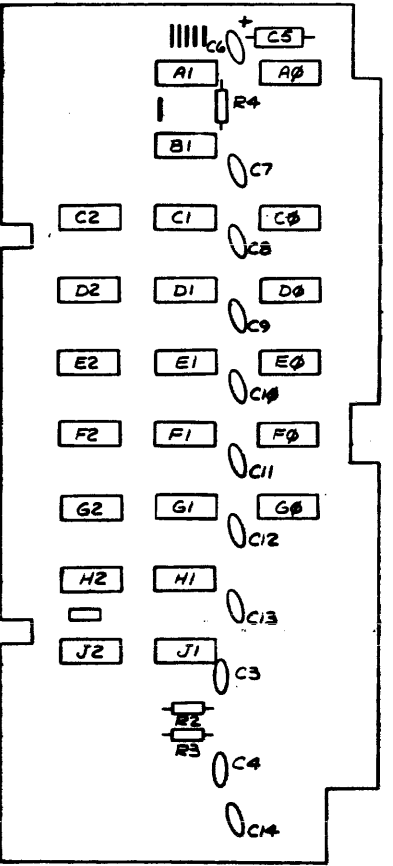
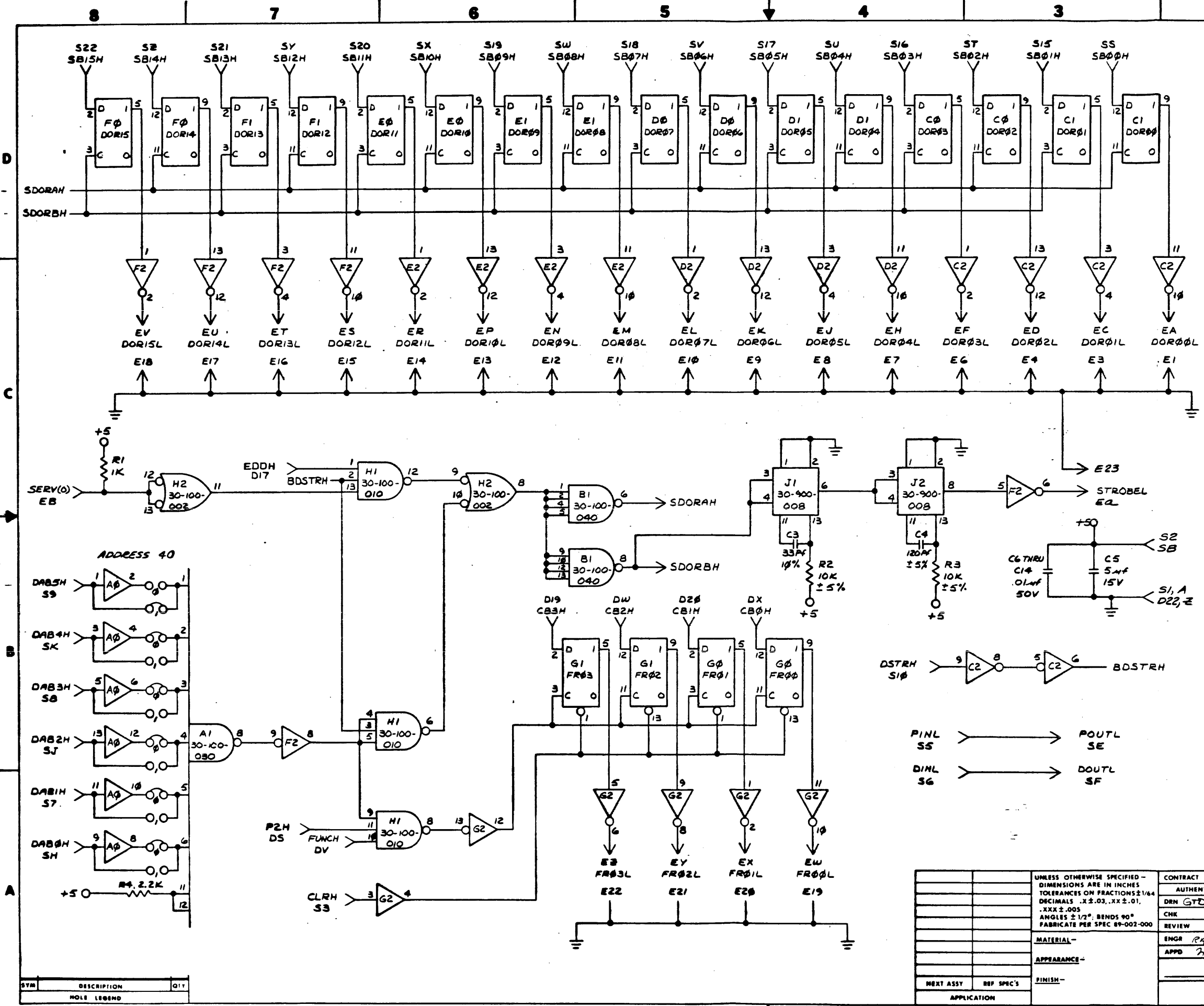


ITEM	PART NO.	NAME	VENDOR	VENDOR PART NO.	QTY
MATERIAL LIST					

UNLESS OTHERWISE SPECIFIED - DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS ± 1/64 DECIMALS .XX ± .01, .XXX ± .005 ANGLES ± 1/2°, BENDS 90° FABRICATE PER SPEC 89-002-000		CONTRACT AUTHENTICATION DATE 11/8/71		GRI Computer Corp. NEWTON, MASS.	
MATERIAL -		CHK REVIEW		ENGINEER R/A 2/22/72	
APPEARANCE -		APPD		DRAWING NO. 17-040-017-A	
FINISH -		NEXT ASSY REF SPEC'S APPLICATION		SIZE CODE IDENT NO. D 11842	
				DRAWING NO. 17-040-017-A	
				SCALE UNIT WT SHEET 2 OF 2	

SYM	DESCRIPTION	QTY
HOLE LEGEND		

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



- NOTES:
- UNLESS OTHERWISE SPECIFIED:  
A. ALL RESISTORS ARE 1/2 W, 5%  
B. INDICATES 30-200-001  
C. INDICATES 30-300-074

SYM	DESCRIPTION	QTY
	HOLE LEGEND	

ITEM	PART NO.	NAME	VENDOR	VENDOR PART NO.	QTY
MATERIAL LIST					
REF B/M					
UNLESS OTHERWISE SPECIFIED - DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS 21/64 DECIMALS .X 2-.03 .XX 2-.01 .XXX 2-.005 ANGLES 2 1/2°, BENDS 90° FABRICATE PER SPEC 89-002-000					
MATERIAL-					
APPEARANCE-					
FINISH-					
APPLICATION					

CONTRACT		DATE	
AUTHENTICATION			
DRN G7D		11/15/71	
CHK			
REVIEW			
ENGR R9		2/22/72	
APPD JRR		2/11/72	
SIZE		CODE IDENT NO.	DRAWING NO.
D	11842		17-049-018-A
SCALE		UNIT WT	SHEET 1 OF 1

**GRI Computer Corp.**  
SELECTOR CHANNEL III  
LOGIC DIAGRAM



 **GRI Computer Corporation**

320 NEEDHAM STREET, NEWTON, MASSACHUSETTS 02164

TEL: (617) 969-0800